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RESEARCH ARTICLE

Subthreshold Modeling of a Tunable CMOS Schmitt Trigger

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ABSTRACT In this article, the subthreshold characteristics of a tunable single input CMOS Schmitt trigger (ST) are modeled for the first time. The high-to-low and low-to-high hysteresis transition points are analytically determined as a function of the tuning voltages and the transistors' geometrical parameters. The derived expressions allow to design the ST with desired hysteresis width in subthreshold region. Furthermore, the proposed model allows to estimate the minimum supply voltage for which hysteresis occurs. The derived expressions also provide physical insight into the circuit behavior, by predicting the effect of supply voltage and temperature variations on the hysteresis width. The model is validated through simulations, and the maximum error between the analytical and simulated transition points is less than 5%. The model is also experimentally validated with an ASIC fabricated in AMS 0.35μm CMOS process. The maximum error between the analytical and measured transition points is below 6%. The analytical model allows performance optimization in subthreshold region for low power applications.

INDEX TERMS CMOS, hysteresis, low voltage, Schmitt trigger, subthreshold.

I. INTRODUCTION

The first Schmitt trigger (ST) was invented by Otto H. Schmitt in 1938, and it was intended to model the nerve membrane behavior [1], [2]. Although the primary application was in the biomedical field, Schmitt predicted that its circuit could be employed in various applications, such as thermostating, oscillography, and light control. Indeed, today STs are extensively implemented in both analog and digital systems [3]. For instance, they are used in triangular/square-wave generators [4], [5], [6], resistance-to-frequency converters [7], [8], capacitive-to-frequency converters [9], modulators [10], [11], SRAMs and latches [12], [13], [14], and different sensing and measuring applications [15], [16], [17], [18], [19], [20], [21], [22]. STs can work in current or voltage mode and be inverting or non-inverting. They can have single or differential input and have tunable hysteresis [23]. Currently, researchers are focusing on analyzing and modeling the subthreshold operation of STs [24], [25], [26], [27], [28], [29]. This is mainly due to the supply voltage reduction trend, which represents a key design technique in the power consumption optimization of electronic systems [30]. Operation at low voltages results in energy efficiency in battery-powered circuits, where the power consumption limits the system lifetime. In systems powered by energy harvesters, the level of the required supply voltage often determines the startup mechanisms. Lowering power consumption is also particularly advantageous in IoT enabling technologies, such as wireless sensor networks, where thousands of electronic devices are typically employed [31]. Supply voltage scaling is therefore critically important, considering that the number of connected devices is expected to increase to more than 30 billion in 2027 [32]. On the other side, subthreshold operation implies that MOSFETs are biased in weak inversion, which results in more complex analytical models [33]. In 2007, Kulkarni et al. implemented a modified version of the classical 6-transistor CMOS Schmitt trigger in 0.13μm CMOS process to implement an SRAM cell for subthreshold operation [34]. In 2012, Lotze and Manoli analyzed supply voltage reduction

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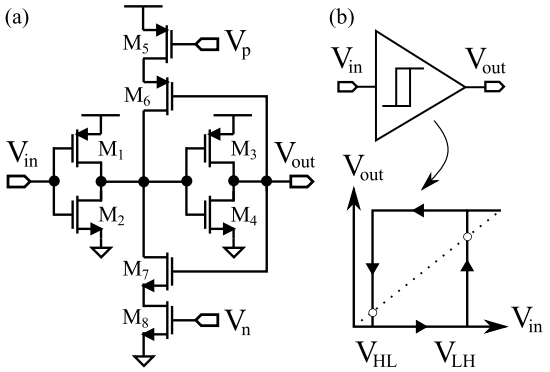

FIGURE 1. (a) Tunable CMOS Schmitt trigger (ST) circuit under analysis [40]. (b) Single input voltage mode ST symbol and characteristics. The bulk terminals are not shown for simplicity.

by considering ST logic, and analyzed the operation of digital circuits with a supply voltage of $62mV$ [35]. In 2017, the same authors proposed an in-depth analysis of ST gates in subthreshold, by considering the optimum transistors sizing [31]. In the same year, Melek et al. determined the DC transfer characteristic of the classical 6-transistor Schmitt trigger (0.18μm CMOS process) in subthreshold [24]. They analytically determined the hysteresis width and the minimum supply voltage ($2ln(2+\sqrt{5})k_BT/q = 75mV$ at room temperature) for which hysteresis occurs. One year later, Melek et al. analyzed the same ST in amplifier mode [26]. They theoretically found a minimum supply voltage of $31.5mV$ (at $300K$) for voltage amplification. In 2018, Bastan et al. proposed a subthreshold pseudo-differential ST in 0.18μm CMOS process, which consumes $150nW$ when operating at $0.4V$ [36]. In 2020, Radfar et al. presented a differential ST circuit (0.18μm CMOS process) with tunable hysteresis based on body biasing [28]. The circuit has a tuning range of approximately $110mV$, and it consumes $1.38\mu W$ with a supply voltage of $0.6V$. One year later, a less power consuming ($120nW$, with supply voltage of $0.4V$) differential ST circuit (0.18μm CMOS process) has been proposed by Nejati et al. [29]. In 2021, Fernandes et al. analyzed the subthreshold operation of a 3-inverter CMOS Schmitt trigger [25]. They analyzed the transition from amplifier mode to hysteresis mode, and they implemented a relaxation oscillator in 0.18μm CMOS process supplied by only $62mV$. In 2022, Sandiri et al. analyzed ST logic gates using Dynamic Threshold MOS (DTMOS) technique [37]. In the same year, we derived in [27], [38] an analytical model for the hysteresis voltage of the low power CMOS ST proposed by Al-Sarawi [39]. In this article, the subthreshold characteristics of the tunable single input CMOS Schmitt trigger proposed by Wang [40] in 1991 are modeled for the first time. The circuit under analysis is shown in Fig. 1(a) and is the first single input tunable CMOS ST modeled in subthreshold. In this article, the expressions for the low-to-high (V_{LH}) and high-to-low (V_{HL}) transition voltages, shown in Fig. 1(b), are analytically determined. These two voltages define the hysteresis width ($V_H = V_{LH} - V_{HL}$). The proposed analytical model allows the design of the ST with desired hysteresis as a function of the transistors' geometrical parameters and tuning voltages. Furthermore, it provides physical insight into circuit behavior by relating the supply voltage and the temperature to the transition voltages. Moreover, the analytical model can be used to estimate the minimum supply voltage for which hysteresis occurs. The derived expressions have been validated through simulations and measurements by prototyping an ASIC in AMS 0.35μm CMOS process. The analytical model is derived in Section II. In Section III the model is validated at simulation level, and the expressions are verified against tuning voltages. The model accuracy is also verified by considering supply voltage, temperature and process variations. The circuit power consumption has been also analyzed. The experimental results are reported in Section IV, while the conclusions are in Section V. Overall, the aim of this paper is to provide a deeper understanding of the subthreshold behavior of the analyzed Schmitt trigger, which is a common block in different analog and digital electronic systems.

II. ANALYTICAL MODEL

The subthreshold drain current expression (EKV [41]) is

$$I_{d,n(p)} = I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}} \cdot \left(e^{-\frac{V_{SB(BS)}}{\phi}} - e^{-\frac{V_{DB(BD)}}{\phi}} \right) \quad (1)$$

where:

$$I_{0,n(p)} = 2 \cdot n_{n(p)} \cdot \mu_{n(p)} \cdot C_{ox} \cdot \frac{W}{L} \cdot \phi^2 \cdot e^{-\frac{|V_{th,n(p)}|}{n_{n(p)} \cdot \Phi}} \quad (2)$$

- B, G, S and D refer to the bulk, gate, source and drain, respectively;
- $n_{n(p)}$ is the NMOS (PMOS) slope factor;
- ϕ is the thermal voltage (kT/q);
- $\mu_{n(p)}$ is the electron (hole) mobility;
- C_{ox} is the oxide capacitance;
- W/L is the transistor width to length ratio;
- $V_{th,n(p)}$ is the NMOS (PMOS) threshold voltage.

Equation (1) can be simplified when transistors are in saturation ($|V_{DS}| \geq 3 \cdot \phi$ [42]) as

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)} - n_{n(p)} \cdot V_{SB(BS)}}{n_{n(p)} \cdot \phi}}. \quad (3)$$

When $V_{SB(BS)} = 0V$, then (3) is further simplified to

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}}. \quad (4)$$

In the circuit under analysis, the bulks of all PMOS are connected to V_{dd}, while those of the NMOS are grounded. To simplify further analysis, the hysteresis transition points are assumed to be independent of each other, i.e. the high-to-low transition point (V_{HL}) depends only on the NMOS tuning transistor (M_8), while the low-to-high (V_{LH}) one only on the PMOS one (M_5). This assumption has been verified analytically, and through simulations and measurements. V_{HL} is

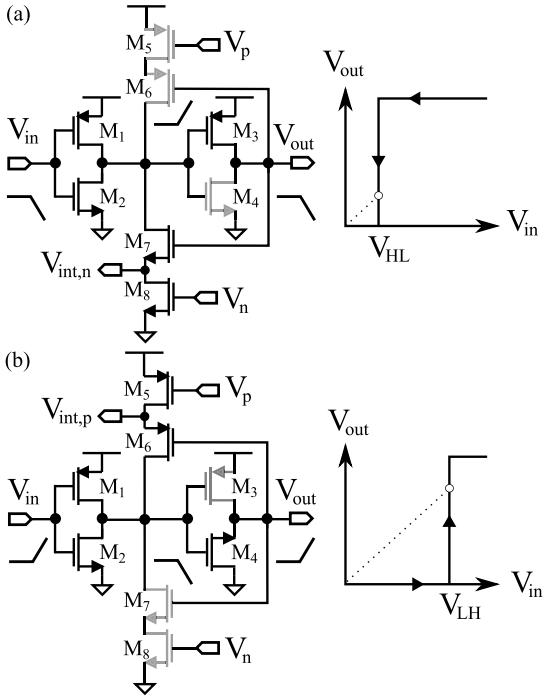

FIGURE 2. ST circuit and characteristics for (a) V_{HL} and (b) V_{LH} analysis.

analyzed first. At initial state when the input (V_{in}) is high, the output (V_{out}) is high as well, due to two cascaded inverters as shown in Fig. 2(a). As a consequence M_4 is off, while $M_{2,3,7}$ are conducting. M_8 conduction depends on the tuning voltage V_n. The input voltage at which the output switches from high-to-low (V_{HL}) can be determined by finding the switching voltage of the inverter composed of $M_{1,2}$, plus the contribution of M_7. Assuming transistors in saturation region during the transition [23], the current through $M_{1,2,7}$ is found using Kirchhoff's current law as

$$I_{0,n2}\cdot e^{\frac{V_{HL}}{n_n\cdot\phi}}+I_{0,n7}\cdot e^{\frac{V_{dd}-n_n\cdot V_{int,n}}{n_n\cdot\phi}}-I_{0,p1}\cdot e^{\frac{V_{dd}-V_{HL}}{n_p\cdot\phi}}=0 \quad (5)$$

where V_{dd} is the supply voltage. To solve (5), the slope factors are approximated as $n_n\approx n_p\approx n$ [43], and $I_{0,p1}$ is redefined as $I'_{0,p1}=I_{0,p1}\cdot exp(V_{dd}/(n\cdot\phi))$. Equation (5) is then divided by $I'_{0,p1}$ and rewritten as

$$\frac{I_{0,n2}}{I'_{0,p1}}\cdot e^{\frac{V_{HL}}{n\cdot\phi}}-e^{-\frac{V_{HL}}{n\cdot\phi}}=-\frac{I_{0,n7}}{I'_{0,p1}}\cdot e^{\frac{V_{dd}-n\cdot V_{int,n}}{n\cdot\phi}}. \quad (6)$$

To solve (6), it is necessary to determine the drain-source voltage across M_8, i.e. $V_{int,n}$. The latter can be obtained by equating the currents in $M_{7,8}$ and solving for $V_{int,n}$:

$$I_{0,n7}\cdot e^{\frac{V_{dd}-n\cdot V_{int,n}}{n\cdot\phi}}=I_{0,n8}\cdot e^{\frac{V_n}{n\cdot\phi}}\cdot\left(1-e^{-\frac{V_{int,n}}{\phi}}\right), \quad (7)$$

$$V_{int,n}=\phi\cdot log\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right). \quad (8)$$

As can be observed in (8), $V_{int,n}$ is linearly dependent on the thermal voltage, and so directly proportional to the temperature. Instead the dependence on the dimensions of $M_{7,8}$ and the tuning voltage V_n is logarithmic. By substituting (8) in (6) the following equation is obtained:

$$\frac{I_{2,n}}{I'_{0,p1}}\cdot e^{\frac{V_{HL}}{n\cdot\phi}}-e^{-\frac{V_{HL}}{n\cdot\phi}}=-\frac{I_{0,n7}}{I'_{0,p1}}\cdot e^{\frac{V_{dd}-n\cdot\phi\cdot log\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right)}{n\cdot\phi}}. \quad (9)$$

Next the following temporary variables are defined:

$$x=\frac{V_{HL}}{n\cdot\phi}, \quad (10)$$

$$a=\frac{I_{0,n2}}{I'_{0,p1}}, \quad (11)$$

$$b=-\frac{I_{0,n7}}{I'_{0,p1}}\cdot e^{\frac{V_{dd}-n\cdot\phi\cdot log\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right)}{n\cdot\phi}}=-\frac{I_{0,n7}}{I_{0,p1}}\cdot\frac{1}{1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}}. \quad (12)$$

Equation (9) can be then rewritten as in (13) and solved for the variable x:

$$a\cdot e^x-e^{-x}=b, \quad (13)$$

$$x=-log\left[\frac{1}{2}\cdot\left(\sqrt{4\cdot a+b^2}-b\right)\right] \quad (14)$$

Finally by replacing all the temporary variables in (14), the analytical expression (15), as shown at the bottom of the next page, for V_{HL} is obtained. Regarding the low-to-high transition voltage (V_{LH}), its expression is shown below that of V_{HL} in (16), as shown at the bottom of the next page, and its derivation is complementary. Referring to Fig. 2(b), first $V_{int,p}$ is determined by equating the current in $M_{5,6}$:

$$I_{0,p5}\cdot e^{\frac{-V_p}{n\cdot\phi}}\cdot\left(1-e^{-\frac{V_{dd}-V_{int,p}}{\phi}}\right)=I_{0,p6}\cdot e^{-\frac{V_{dd}-V_{int,p}}{\phi}}, \quad (17)$$

$$V_{int,p}=V_{dd}-\phi\cdot log\left(\frac{I_{0,p6}}{I_{0,p5}}\cdot e^{\frac{V_p}{n\cdot\phi}}+1\right). \quad (18)$$

Next the currents in $M_{1,2,6}$ are equated:

$$I_{0,p1}\cdot e^{\frac{V_{dd}-V_{LH}}{n\cdot\phi}}+I_{0,p6}\cdot e^{\frac{V_{dd}-n\cdot\left(V_{dd}-V_{int,p}\right)}{n\cdot\phi}}=I_{0,n2}\cdot e^{\frac{V_{LH}}{n\cdot\phi}}. \quad (19)$$

Then, (18) is substituted in (19), and the resulting expression is divided by $I'_{0,p1}$. Next the temporary variables are defined, and the expression in (16) is finally obtained. Both derived expressions, (15) and (16), are linearly dependent on the slope factor and the thermal voltage, and logarithmically dependent on the tuning voltages and the transistors' dimensions. The high-to-low transition point depends on $M_{1,2,7,8}$ and V_n, while the low-to-high one on $M_{1,2,5,6}$ and V_p. Therefore, the analytical model is based on the assumption that the hysteresis transition voltages can be independently adjusted.

III. SIMULATION RESULTS

The proposed analytical model has been validated through simulations in AMS 0.35μm CMOS process. All the simulation results refer to post-layout simulations. The simulated NMOS threshold voltage is $V_{th,n} = 515.8mV$, while the PMOS one is $-731.3mV$. The supply voltage has been initially fixed to $V_{dd} = 0.45V$ to guarantee subthreshold operation. As can be observed in (15) and (16), the M_1 aspect ratio (included in $I_{0,p1}$ as defined in (2)) is at the denominator of the terms inside the logarithms; this implies that a wider PMOS transistor will lead to a higher V_{LH} and V_{HL}. Therefore, the PMOS have been sized 20/1, while the NMOS 1/1, to obtain a larger hysteresis during the measuring phase. When computing $I_{0,n(p)}$, the extracted slope factors $n_{n(p)} = 1.25(1.3)$ are used. Instead, when computing the other terms in (15) and (16), the average value ($n \approx 1.28$) is considered [43]. This last approximation is required in order to solve (5). The NMOS extracted transconductance parameter ($\beta_{n(p)} = \mu_{n(p)} \cdot C_{ox} \cdot W/L$) is $162.26\mu A/V^2$, while the PMOS one is $1.01mA/V^2$. The simulated $V_{LH,HL}$ are extracted by sweeping the input voltage from $0V$ to V_{dd}, and vice versa. In Fig. 3(a), the analytical and simulated V_{HL} as a function of V_n are shown. As can be observed, the analytical model resembles the simulated behavior. The same holds for V_{LH}, which is shown in Fig. 3(b). The transition voltages are evaluated for $V_{n(p)} < 0.3V$, because for higher tuning voltages V_{out} does not toggle (i.e. no high-to-low transition), while V_{LH} is almost constant, for the given design. It has been verified through simulations that the hysteresis transition voltages are strongly independent of each other, i.e. $V_{HL(LH)}$ does not vary with $V_{p(n)}$, as assumed by the proposed analytical model. To evaluate the error between the two curves, the maximum absolute and relative errors between the analytical ($V_{HL(LH)}$) and simulated ($V_{HL(LH),sim}$) transition points are defined:

$$\Delta_{HL(LH)} = |V_{HL(LH)} - V_{HL(LH),sim}|, \tag{20}$$

$$\delta_{HL(LH)} = \left| \frac{V_{HL(LH)} - V_{HL(LH),sim}}{V_{HL(LH),sim}} \right| \cdot 100\%. \tag{21}$$

Δ_{HL} is $2.2mV$ while Δ_{LH} is $2.4mV$. Instead, δ_{HL} is 1.3% while δ_{LH} is 0.8%. Relatively to the supply voltage

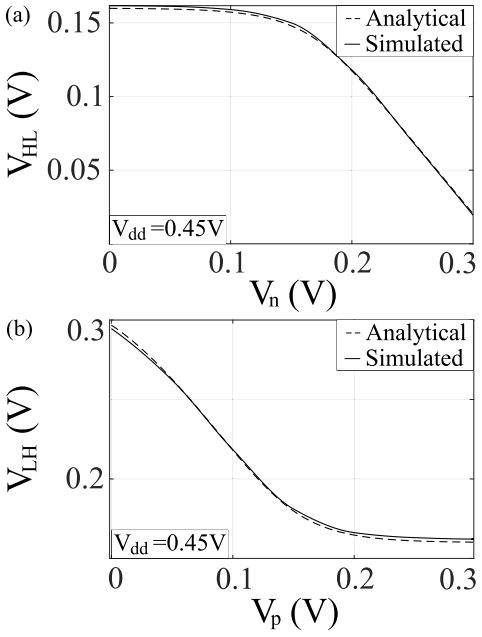

FIGURE 3. Analytical and simulated (a) V_{HL} vs V_n and (b) V_{LH} vs V_p ($V_{dd} = 0.45V$).

($\Delta_{HL(LH)}/V_{dd}$), the maximum errors are below 0.5%. The error between the curves is mainly attributed to the considered approximation $n_n \approx n_p \approx n$. The analytical model has also been verified by considering different designs, shorter channel lengths (e.g. $L = 0.35\mu m$) and narrower transistors, and the maximum error resulted to be in the same order of magnitude of that of the reported design. The derived expressions have been validated by also considering data provided by the datasheet of the AMS 0.35μm CMOS process. Results similar to those obtained with the extracted ones have been obtained, i.e. errors in the same order of magnitude. Although the proposed analytical model has been validated with a relatively old CMOS process technology, the same EKV model has been used to correctly model STs in 0.18μm technology [25], as well as analyze circuits in lower technological nodes (e.g. 90nm and 65nm) [44], [45].

$$V_{HL} = -n \cdot \phi \cdot log\left[\frac{1}{2} \cdot \left(\sqrt{4 \cdot \frac{I_{0,n2}}{I_{0,p1}} \cdot e^{-\frac{V_{dd}}{n \cdot \phi}} + \left(\frac{I_{0,n7}}{I_{0,p1}}\right)^2 \cdot \frac{1}{\left(1 + \frac{I_{0,n7}}{I_{0,n8}} \cdot e^{\frac{V_{dd}-V_n}{n \cdot \phi}}\right)^2}} + \frac{I_{0,n7}}{I_{0,p1}} \cdot \frac{1}{1 + \frac{I_{0,n7}}{I_{0,n8}} \cdot e^{\frac{V_{dd}-V_n}{n \cdot \phi}}}\right)\right] \tag{15}$$

$$V_{LH} = -n \cdot \phi \cdot log\left[\frac{1}{2} \cdot \left(\sqrt{4 \cdot \frac{I_{0,n2}}{I_{0,p1}} \cdot e^{-\frac{V_{dd}}{n \cdot \phi}} + \left(\frac{I_{0,p6}}{I_{0,p1}}\right)^2 \cdot \frac{1}{\left(1 + \frac{I_{0,p6}}{I_{0,p5}} \cdot e^{\frac{V_p}{n \cdot \phi}}\right)^2}} - \frac{I_{0,p6}}{I_{0,p1}} \cdot \frac{1}{1 + \frac{I_{0,p6}}{I_{0,p5}} \cdot e^{\frac{V_p}{n \cdot \phi}}}\right)\right] \tag{16}$$

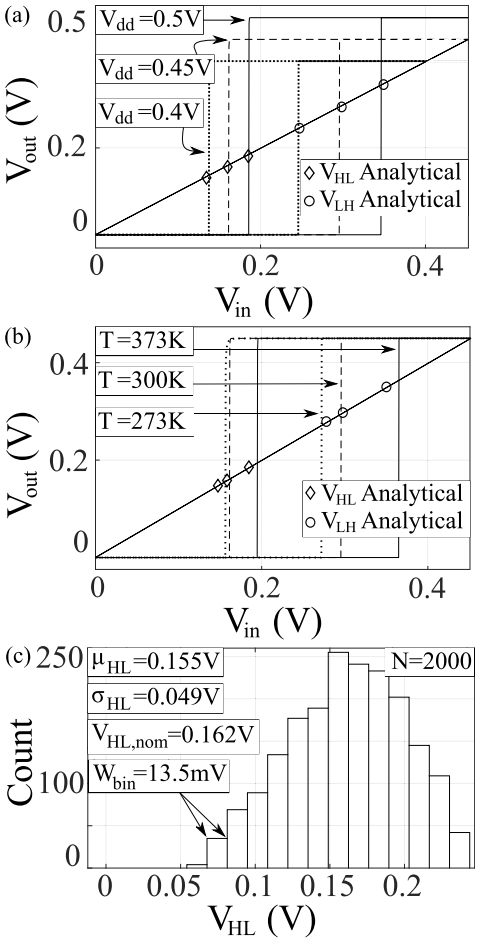

FIGURE 4. Simulated V_{out} vs V_{in} for: (a) different V_{dd} and $T = 300K$; (b) different T and $V_{dd} = 0.45V$. (c) Histogram associated to the Monte Carlo simulations for V_{HL} ($V_{DD} = 0.45V$).

A. SUPPLY VOLTAGE, TEMPERATURE AND PROCESS VARIATIONS

To verify the accuracy of the model, different simulations have been performed by considering supply voltage, temperature and process variations. In Figs. 3(a) and (b), the maximum error occurs when $V_{n(p)} = 0V$. Therefore, in the following the tuning voltages have been fixed to zero volts. In Fig. 4(a), the ST transfer characteristics are depicted for different supply voltages. The error associated to V_{HL} is maximum for $V_{dd} = 0.4V$, while that associated to V_{LH} for $V_{dd} = 0.5V$. Nevertheless, the maximum error relative to V_{dd} is below 3% in the analyzed V_{dd} range. The simulations have been performed with steps of $50mV$ in V_{dd}, but only the extrema are reported, where the error is maximum. For supply voltages below $0.4V$, the circuit does not toggle correctly for certain tuning voltages. In Fig. 4(b), the ST transfer characteristics are depicted for different temperatures ($V_{dd} = 0.45V$). The circuit is sensitive to temperature variations, and for both transition points the maximum error occurs at $T = 373K$. Nevertheless, the relative errors are 4.8% and 3.7% for V_{HL} and V_{LH}, respectively. Finally, Monte Carlo simulations have been performed in order to observe the deviation of the analytical transition voltages from the simulated ones, when considering both process and mismatch variations. The number of iterations was set to $N = 2000$. The histogram associated to V_{HL} is shown in Fig. 4(c). The nominal V_{HL} is $0.162V$. The mean and standard deviation are $0.155V$ and $0.049V$, respectively. Regarding V_{LH}, its nominal value is $0.294V$, while the mean and standard deviation are $0.278V$ and $0.097V$, respectively. The analytical V_{HL} and V_{LH} are within one standard deviation.

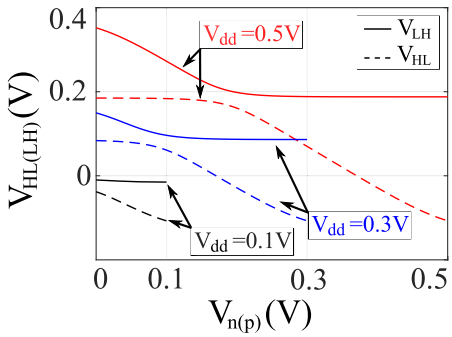

FIGURE 5. Analysis of the minimum supply voltage for which hysteresis occurs. Analytical $V_{HL(LH)}$ vs $V_{n(p)}$ for different supply voltages. No transition occurs when the curves become negative.

B. MINIMUM SUPPLY VOLTAGE AND HYSTERESIS

The proposed analytical model can be used to estimate the minimum supply voltage for which hysteresis occurs. As can be observed in Fig. 4(a), when the supply voltage is decreased, both transition voltages decrease as well. Eventually, when the supply voltage is decreased to a certain value, the high-to-low transition will not occur. However, the low-to-high transition will still occur. In Fig. 5, the analytical high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages are plotted as a function of the tuning voltages, for different supply voltages. When $V_{DD} = 0.5V$, a hysteretic behavior is guaranteed only for $V_n < 0.37V$, because for higher tuning voltage the analytical V_{HL} becomes negative, i.e. it is not defined. This means that when sweeping the input voltage from high to low, no transition in the output voltage is observed. When the supply voltage is $0.3V$, the high-to-low voltage is above zero volts until $V_n \approx 0.17V$. When $V_{dd} = 0.1V$, both analytical curves are below zero volts, i.e. no transition is observed for whatever combination of V_n and V_p. It should be remarked that the minimum supply voltage for which hysteresis occurs also depends on transistors' dimensions. For the given design, the minimum supply voltage for which hysteresis occurs is approximately $0.15V$, i.e. when $V_{dd} = 0.15V$, V_{LH} is defined but V_{HL} is below zero volts for whatever V_n. All the presented analysis has been verified through simulations.

IV. EXPERIMENTAL RESULTS

An ASIC in AMS 0.35μm CMOS process has been fabricated through EUROPRACTICE MPW to experimentally validate

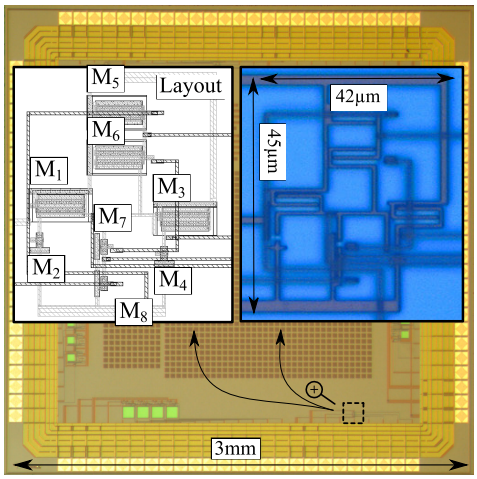

FIGURE 6. Layout and micrograph of the ST (AMS 0.35μm CMOS process).

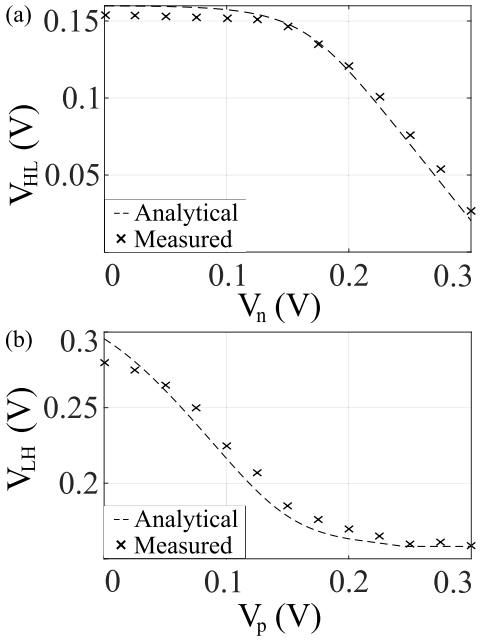

FIGURE 7. Analytical and measured (a) V_{HL} vs V_n and (b) V_{LH} vs V_p ($V_{DD} = 0.45V$).

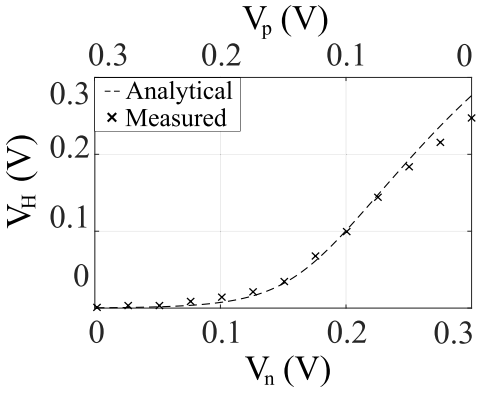

FIGURE 8. Analytical and measured hysteresis width V_H as a function of the tuning voltages $V_{n(p)}$ ($V_{DD} = 0.45V$).

the proposed analytical model. The ST circuit occupies an area of $42\mu m \times 45\mu m$. The PMOS transistors are sized 20/1, while the NMOS 1/1, i.e. same dimensions associated to the curves in Figs. 3(a) and (b). The layout and the micrograph of the circuit are shown in Fig. 6. Due to technology rules, the PMOS transistors are fabricated with two gates, each with a $10u$ width stripe. The voltages have been measured through a KEYSIGHT InfiniiVision DSOX3024T, by applying a $1Hz$ triangular wave at the input of the circuit. The analytical and measured V_{HL} as a function of V_n are shown in Fig. 7(a). The model resembles the measured behavior, although for increasing V_n, the measured V_{HL} is less linear. The same holds for the low-to-high transition point, shown in Fig. 7(b). For small V_p the measured V_{LH} is less linear than the analytical one. The maximum absolute error ($\Delta_{HL,meas} = |V_{HL,meas} - V_{HL}|$) between the analytical and measured V_{HL} is $5mV$, while the relative one ($\delta_{HL,meas} = |\Delta_{HL,meas}/V_{HL}|$) is 3.1%. Regarding the low-to-high transition point, the maximum absolute error is $16mV$, while the relative one is 5%. The difference between the analytical and measured transition points is attributed to circuit parasitics and process variations (e.g. change in the slope factor). As can be observed in Figs. 7(a) and (b), both V_{HL} and V_{LH} are maximum for $V_{n(p)} = 0V$ and minimum for $V_{n(p)} = 300mV$. The maximum hysteresis width ($V_{H,max}$) occurs when $V_n = 0.3V$, and $V_p = 0V$, as can be observed in Fig. 8. $V_{H,max,meas}$ is $253mV$, while the analytical one is $276mV$, i.e. the maximum error between the measured and analytical hysteresis voltages is $23mV$. It has been verified through measurements that the hysteresis transition voltages are strongly independent of each other, i.e. $V_{HL(LH)}$ does not vary with $V_{p(n)}$, in agreement with the analytical model assumptions. The maximum operating frequency is $20Hz$ for the implemented design. Therefore, the circuit is suitable for low frequency applications, e.g. low frequency waveform generators. The circuit power consumption is mainly due to the switching currents during the transitions. Due to the very small amplitude of these currents, they could not be measured precisely. Therefore, the circuit power consumption has been analyzed through simulations only. When switching from low-to-high, the maximum power consumption occurs when $V_p = 0V$ (i.e. M_5 is on), and the switching current has a peak value of $416pA$. Instead, when switching from high-to-low, the maximum power consumption occurs when $V_n = 0.3V$ (i.e. M_3 is on), and the switching current has a peak value of $423pA$. When the same circuit is simulated with the nominal supply voltage for the considered CMOS process ($3.3V$), the maximum peak current has a value of $259\mu A$ and $287\mu A$, during the low-to-high and high-to-low transitions, respectively. Therefore, when the circuit is operated in subthreshold region, the power consumption improves by five orders of magnitude with respect to the case in which the transistors are biased in strong inversion.

V. CONCLUSION

In this article, the subthreshold characteristics of a tunable CMOS Schmitt trigger have been modeled for the first time. The analytical model relates the hysteresis transition voltages to the transistors' geometrical parameters and tuning voltages, allowing the design of the circuit with desired hysteresis width in subthreshold region. Furthermore, it allows optimization of the circuit operation by including the supply voltage and the temperature dependencies in its formulation. The proposed analytical model is based on the assumption that the high-to-low and low-to-high hysteresis transition points are strongly independent of each other. This assumption has been verified both at simulation and experimental level. Supply voltage, temperature and process variations have been considered. Moreover, a simple method for the estimation of the minimum supply voltage for which hysteresis occurs is reported. The maximum error between the analytical and simulated transition points resulted to be less than 5%. The model has also been experimentally validated with an ASIC in AMS 0.35μm CMOS process fabricated through EUROPRACTICE MPW. The maximum error between the analytical and measured transition points is below 6%. The power consumption has an improvement of five orders of magnitude, while the maximum operating frequency is limited to 20Hz, for the given design. Overall, the proposed analytical model provides a deeper understanding of the circuit subthreshold operation for low power and low frequency applications.

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