Beyond CMOS: Ternary and mixed radix CNTFET circuit design, simulation and verification

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Beyond CMOS: Ternary and mixed radix CNTFET circuit design, simulation and verification

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***Abstract*—For three-valued or ternary computing to be an alternative for binary, new multiple valued logic (MVL) electronic design automation (EDA) tools are needed. In this article we present a novel MVL logic synthesis tool to generate binary, ternary and hybrid (mixed radix) circuits using carbon nanotube FETs (CNTFETs). The web-based open source EDA tool aids in design, simulation and verification aspects including a direct netlist export to HSPICE. We demonstrate a fundamental building block of a balanced ternary computer using the tool, a ternary D flip-flop. We show that mixed radix design can reduce transistor count.**

***Keywords*-Multiple-valued logic, ternary computing, CNTFET architectures, design automation**

I. Introduction

What use is the continuation of Moore's Law to double transistor density if transistor utilization cannot keep up? The amount of heat that needs to be dissipated is slowly increasing every technology node while cooling solutions are not improving at the same pace [1]. Since the 32 nm node, power density $D = Power/Area$ is not constant as required for ideal Dennard scaling. To mitigate thermal problems, transistors are disabled (dark silicon) or operate at lower frequency (dim silicon). With modern 5 nm nodes it is estimated that chip designers can only use around 10 % of the chip hardware resources at a given time, the rest being dim/dark silicon [2].

Total power consumption in modern CMOS chips can be simplified to two terms: dynamic power, the energy needed for switching transistor states (moving data), and static power, the energy needed to maintain these states [3]. For dynamic power an estimated 90 % is dissipated in the interconnects [4]. Historically brief short circuits and (dis)charging capacitive loads across transistor gates were major factors. For static power, heat is dissipated even if the transistor is switched off (leakage current). As devices shrink at every node, leakage current becomes more prominent [5]. With increasing transistor density and thus dark silicon, static power consumption dominate total power consumption.

This brief and heavily simplified state-of-affairs show a need for a shift in computer paradigms, which is discussed in greater detail at the International Roadmap for Devices and Systems (IRDS) [1].

[1]https://irds.ieee.org/home/what-is-beyond-cmos

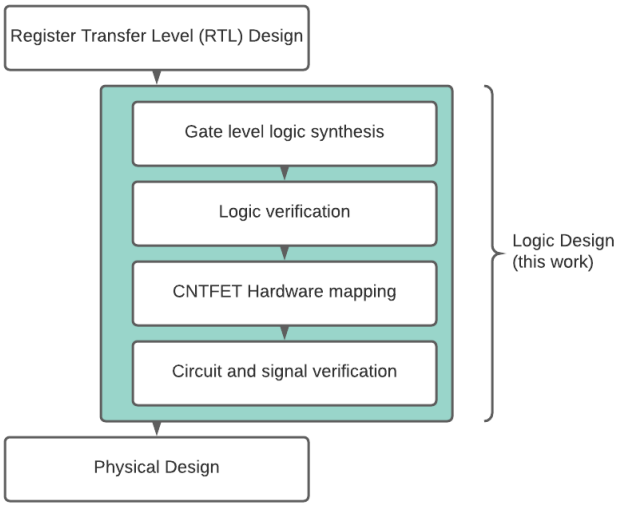

Fig. 1: **Scope of this work.** Logic design of CNTFET-based binary, ternary and mixed radix integrated circuits

Carbon nanotube field effect transistors (CNTFETs) have been proposed in literature to be a viable successor to CMOS transistors [6] [7], in part due to their low $V_{threshold}$ operation and small size. Furthermore, by controlling the diameter of carbon nanotubes, $V_{threshold}$ can be controlled, making multiple-valued logic (MVL) such as ternary circuits possible [8]. Similar to frequency modulation, by considering more discrete signal levels through the same wire, interconnects can be used more efficiently – at the cost of smaller noise margins. Less interconnects results in less dynamic power and better layout designs. For memory MVL has already proven to be a good approach. Modern solid state drives already use multiple bits per cell and this keeps increasing [9]. For logic, MVL has seen limited success despite being researched since the 1950's [10]. In large due to transistor fabrication challenges, it was never feasible to create single devices that inherently had more than 2 stable states with less than $log(3)/log(2) = 1.58$ or 58 % total overhead in the case of ternary. From the radix economy [11] follows that for fair comparison to base 2 (binary) parameters like transistor

count, size, switching speed, delay and fabrication cost should not exceed that overhead. Recent breakthroughs with ternary CMOS [12], graphene transistors, memristors (eg. 6.5 bits on a single memristor [13]) and CNTFET with memristor design [14] show that non-binary logic is possible, paving the way for a possible beyond CMOS roadmap.

Designing post-binary circuits requires new electronic design automation (EDA) tools. These tools cannot ignore the nearly 80 year old legacy of binary development and CMOS process optimization. The integrated circuit (IC) design cycle starts with a specification and register transfer level design that are expressed in a hardware description language like VHDL or Verilog (see Fig. 1). In the next abstraction level, gate level logic synthesis, high level behavior is converted to logic gates. These are hardware implementation agnostic, but not radix agnostic. For example, in binary only 16 dyadic (2 input, 1 output) logic gates such as the AND, OR, XOR gate exist while in ternary there are $3^{3^2} = 19683$ unique dyadic logic gates. Binary logic gates are a (very small) subset of the ternary logic gates. Physical binary signals are simply the extremes of ternary signals. This realisation makes it possible to mix binary and ternary logic gates, which will prove instrumental to reduce transistor count. For example the enable/disable signal of a ternary-valued register is inherently binary.

II. Related Work

Logic design is a well established field within computer engineering. Commercial suits like Synopsis Design compiler, Cadence Genus and MentorGraphics LeonardoSpectrum have been around for a while. In academia logic design and the development of electronic design (EDA) tools is still an active area of research. From improved logic representations to Darpa's ambitious OpenROAD project [15] to develop open EDA's.

Important historical synthesis tools are Berkeley's Multi-Valued Logic Synthesis (MVSIS), Logisim and Digital Logic Simulator(DLS) and ABC [16]. Some of these tools have a graphical interface and some allow non-binary valued representations. Work on this multi and mixed radix EDA tool was started in 2020 as the authors could not find any existing EDA tool that targeted mixed radix design with CNTFETS, was open source and exported netlist for a better verification workflow with industry standard tools.

III. The Mixed Radix Circuit Synthesizer

We present the Mixed Radix Circuit Synthesizer (MRCS), a no-installation browser-based EDA tool that streamlines multiple-valued circuit design, simulation and verification workflows. With a permissive GPLv3 open source license, users are free to modify and use it for research or commercial purposes. In the design stage users can create hierarchies of monadic, dyadic, and triadic (ie. 1,2 or 3 input - 1 output) functions represented as truth tables. Large truth tables can quickly become unfeasible. In ternary, with 19683 dyadic and 3^{3^3} triadic functions, many truth tables become functional

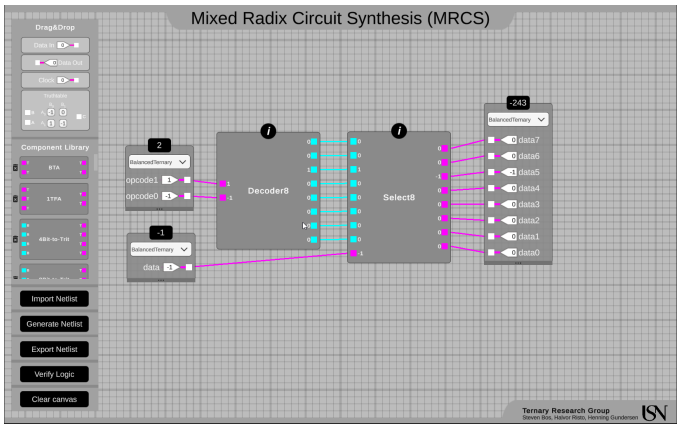

Fig. 2: **Main user interface.** The decoder8 and select8 components are part of a 8:1 balanced ternary multiplexer component that is shown at abstraction level 1. Circuits can be stored as components in the component library and become part of larger logic networks/hierarchies. Fig. 4 shows a binary SR latch component at abstraction level 0, the lowest.

unit blocks. When connecting these blocks in a logic network representation they become highly scalable hierarchies. These logic networks are mapped to CNTFET schematics with a logic synthesis algorithm we describe in detail in [17] [18]. Our algorithm is inspired by the work of [8] and uses the same rules to create 2 pull-up and pull-down and 2 pull-up-half and pull-down-half networks. It uses a different approach to optimize the "don't care" values and optimize away input inverters. We have not yet incorporated the body-effect modification as described in [19] to further reduce static power consumption. With 3 different CNT diameters that activate at different thresholds and an optional pull-up-half and pull-down-half network that functions as a voltage divider to create the middle value, any binary or ternary logic function can be constructed by the logic synthesis algorithm. The designed circuits can be tested through simulation for functional correctness by manually inputting data and visually inspecting the entire output trace through the logic network. This process can also be automated by providing input-output relations in CSV format. The circuits are exported as Netlist files and are directly usable for signal verification in a SPICE simulator like HSPICE [20]. This reduces the time from logic gate design to CNTFET circuit implementation. Both asynchronous and clock based simulations are supported.

A. Core features[2]

- Drag and drop logic gate design using monadic, dyadic, and triadic multi-radix truth tables
- Create large logic networks by saving one or more logic gates as new components.
- Interactive and traceable input-output behavior through manual and automated state simulation

[2]A video demonstration can be found in [21]

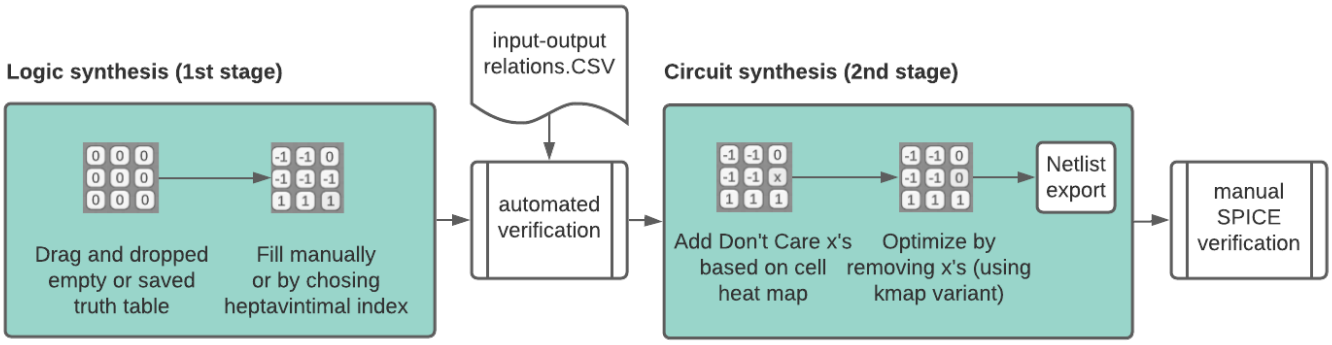

Fig. 3: **Design flow.** Two stage design with simulation and verification

- Support for various interpreted IO signals such as (un)signed binary and (un)balanced ternary.
- Visualisation of the complete CNTFET circuit showing active and inactive transistor paths of the current inputs
- Automated synthesis of full-circuit netlists files making designs simulation-ready for HSPICE
- Export, share and import designs as ZIP file
- Insight on transistor count, (unique) logic gates count and logic gate utilization with heatmap

B. *Work flow*

Figure 3 shows a typical 2-stage workflow. The first stage is verified by a manual or automated functional simulation, while the second stage is verified on the signal level using HSPICE. In Fig. 4 the steps for logic synthesis stage and manual functional simulation are shown. With a working functional design from the first stage, the design is mapped to a hardware implementation. In this version we integrated the CNTFET circuit synthesis engine discussed above, but other hardware mappings such as with CMOS transistors are imaginable. We optimized the circuit synthesis step for lower transistor count by looking at the heat map of the logic gates. Cells that are not used for all tested inputs have background color white and can be marked with X for "don't care". These x-cells are transformed to an optimal value by the circuit synthesis engine after pressing the *Generate Netlist* button. The generated netlist files can then be loaded by HSPICE for signal verification using the Stanford CNTFET model and parameters published in [22].

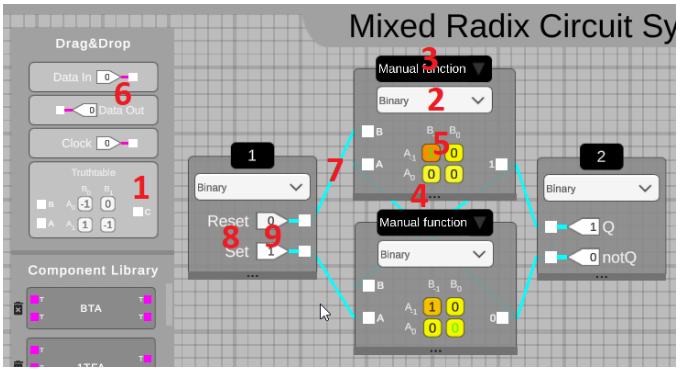

Fig. 4: **Design instructions for a binary SR-latch 1)** Drag and drop one or more truth tables on the canvas. **2)** Select radix from dropdown **3)** (Optional) Use heptavintimal-notation for shorthand truth table's selection. **4)** Change arity of TT by pulling bottom container edge. **5)** Toggle through valid logical transitor values including 'x' indicating "don't care". **6)** Drag and drop I/O containers. Change size by pulling bottom container edge. The counter on top interprets the container as a whole. **7.** Wire the circuit by first selecting a start terminal. Start terminals can have 0-n connections, end terminals can have 0-1. **8)** (Optional) Label the I/O containers. The labels are used in the generated netlist. **9.** Simulate the circuit behavior by clicking on the input to toggle its value. Notice that the currently active truth tables cell value is colored green such that the truth tables output is traceable. The cell background color ranges from white to red and illustrates transistor usage.

IV. Design of a Ternary Data Flip-Flop

A data or D flip-flop is an essential circuit for any clock-based processor design, allowing data to be changed in the low-to-high *flip* stage and safely *read* in the high-to-low *flop* stage. We started our design with a binary SR-latch shown in Fig. 4. We modified it to a standard binary D latch by adding two more AND gates. Next was finding the ternary equivalent by starting with an empty triadic truth table and experiment with different cell values and connections to achieve the desired behavior. We found that a ternary valued data latch can be made by the ternary function ZD0xxxPPP, where xxx are "don't care" values and can be optimized to PPP. The data latch can be configured in a master-slave configuration flip-flop by duplicating the latch and adding a binary inverter to select which latch should be enabled by the binary clock signal, mixing two different radix gates (Fig. 5).

With a functionally correct design we can click the Generate Netlist button. Statistics of the circuit and the transistor layout (Fig. 6) of logic gates of the generated component can now be inspected by clicking the information button **i** as seen in Fig. 2. Interacting with the inputs of circuit will change the active transistor paths in the color coded transistor layout, enabling a

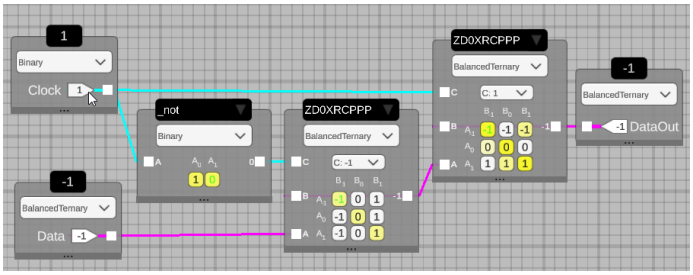

Fig. 5: **Balanced ternary flip-flop**. Rising edge (RE) master-slave (MS) configuration. A single D latch is 18 transistors and requires 5 inverters of 2 transistors that can be shared with multiple components for a total of 28 transistors. The flip-flop uses a total of 54 transistors since 1 inverter is shared between two inputs. An equivalent 8 NAND + 2 inverter binary flip-flop design uses 36 transistors.

deeper understanding of the various voltage thresholds of the 3 different CNTFET transistors.

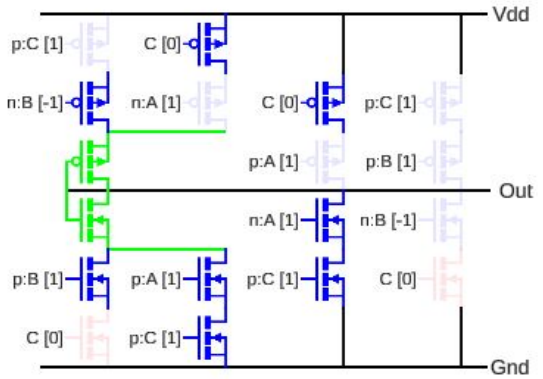

Fig. 6: **Transistor layout with active transistor path of logic gate ZD0PPPPPP**. Shown are 18 transistors of which 10 are active when clock (input C) is 0 and data (input A) is -1. Input B is a feedback input critical for temporarily connecting the output buffer to input A when input C changes from low-to-high. The output is -1 or 0 volt as can be seen by the pull down network connecting with ground. P and N are positive or negative ternary input inverters. The three colors are CNTFET diameters explained in [17], resulting in different $V_{threshold}$.

With a generated netlist a signal verification of the flip-flop can be ran in HSPICE (Fig. 7). This requires manual editing of the main.sp file to set the desired input pattern, test duration and other simulation parameters.

V. Discussion

By reusing SPICE verified components in a logic network, larger and more complex circuits can be constructed while at the same time verifying subcircuit correctness through piecemeal functional logic and signal verification. Although various binary and ternary flip-flops were generated in the span of days, the tool and design workflow have not been tested for very large circuits. The largest circuit we have currently designed and simulated contained 1760 transistors. This 25GB/s binary to balanced ternary radix converter [23] consumed 97.8 μW of power and had a 5GHz input frequency. Note that full circuit functional verification is not a requirement by the tool to proceed to the 2nd stage. Designing large circuits, navigating the logic network and exporting as netlist of large mixed radix circuits is fully supported. Recent research by [24] indicate that the interconnect wire length of a ternary circuit was reduced with 37 % compared to binary and is maintained in larger and more complex circuits. The generated D flip-flop presented here uses 54 transistors compared to an equivalent binary one of 36. For fair comparison transistor count should be normalized as higher bases have increased information density. If we assume all other variables such as PDP, size, and process cost to be equal than $54/36 <= log(3)/log(2)$. For this mixed radix design a 8.5 % saving is realised. A smaller transistor count can be expected when more binary functionality is added to a ternary or higher base circuit such as a read/write flag or scan-enable flag typically found in registers that are suitable for a Design-For-Test (DFT) approach. This advantage scales linearly when comparing to higher bit-architectures (eg. 64 bit) resulting in less interconnects, smaller required chip estate and lower power consumption.

TABLE I: **Comparison to binary**. The radix is given in subscript with mixed being binary and ternary logic gates. Ternary-To-Equivalent-Binary transistor overhead (multiply binary transistor count with 1.585 and rounded down) is shown in parenthesis. Ternary or mixed radix transistor count that is lower than the binary equivalent transistor count with overhead outperform binary. The transistor count includes shareable input inverters.

Circuit	Transistors	Avg. Power
Full $Adder_2$ [18]	52	7.02E-07 W
Full $Adder_3$ [18]	118 (52*1.585=82)	2.55E-06 W
D $Latch_3$	28 (16*1.585=25)	6.15e-07 W
RE MS D $Flip\text{-}flop_{mixed}$	54 (36*1.585=57)	1.24e-06 W

VI. Conclusion

In this work we present Mixed Radix Circuit Synthesizer (MRCS), a novel open source EDA tool to design, simulate and verify binary, ternary and mixed radix circuits made from CNTFETs. The tool aims to create a streamlined design-time workflow to help reduce complexity and ultimately design time and improve understanding of binary and post-binary technology. Secondly, we demonstrate the design and verification of a ternary computer building block, the ternary flip-flop with binary clock. The flip-flop was built following the presented design workflow. The graphical user interface makes tracing logic at various abstractions possible, aiding in the understanding of the behavior of the circuit. The open sourced code [21] and WebGL [25] platform support positions the tool as a pedagogical instrument. Finally, in Table I a

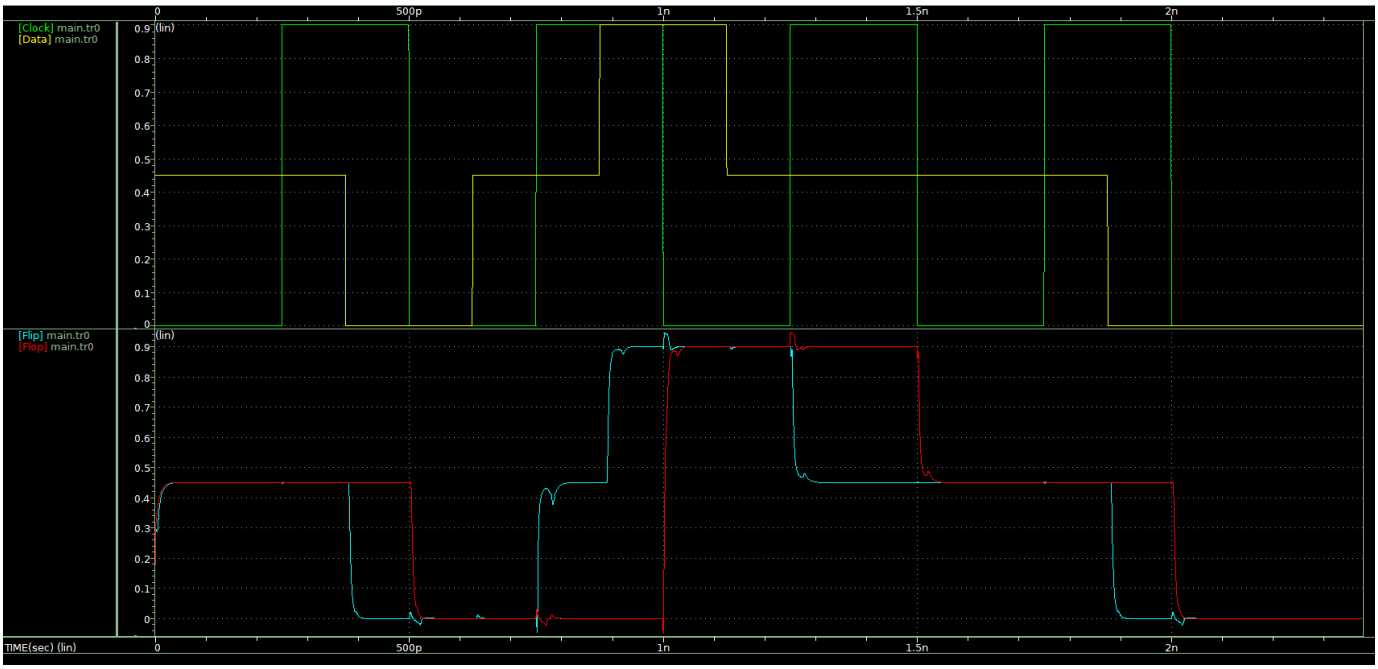

Fig. 7: **HSPICE Transient analysis without load.** (Top) Binary clock and ternary data signals. Clock frequency is 2 GHz. (Bottom) Flip and Flop signals. Note that in high clock periods the Flip latch copies the data signal, while in low clock periods the Flip latch is disconnected and the Flop latch copies from the Flip latch.

brief comparison to binary is given, showing an improvement in transistor count of 8.5 % for a standard implementation of the rising-edge master slave data flip-flop. Further research in mixed radix design is needed to determine if MVL technology for logic can earn a spot on the beyond CMOS roadmap.

VII. Future work

A complete balanced ternary CPU architecture is currently being worked on. Early results using the same design process discussed here are promising with ALU's, multiplexers (Fig. 2), registers and bi-directional shifters. The tool has no circuit satisfiability (SAT) solving functionality and misses several useful metrics such as PDP and estimated chip area. A callback from HSPICE to MRCS after signal analysis has completed could allow further user-centered workflow automation.

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