Analysis of a Low Power Inverting CMOS Schmitt Trigger Operating in Weak Inversion

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***Abstract*—This article analyzes the operation of a low power inverting CMOS Schmitt trigger in weak inversion. The analysis is based on an earlier proposed analytical model, which relates the hysteresis voltages to the transistors' dimensions, the supply voltage, and the temperature. The maximum error between the analytical and simulated transition voltages is below 10%, relative to the supply voltage. By optimizing the device sizes, the error reduces to 4%. The operation of the Schmitt trigger in weak inversion is also experimentally validated through an ASIC fabricated in AMS 0.35µm CMOS process. The maximum error between the modeled and measured transition voltages is below 7%. Furthermore, the power consumption as a function of the supply voltage is analyzed. Overall, the proposed model may be used to optimize the operation of the analyzed Schmitt trigger circuit for low power operation.**

***Index Terms*—CMOS, hysteresis, low voltage, low power, Schmitt trigger, subthreshold, weak inversion**

I. Introduction

Supply voltage scaling represents one of the most effective techniques for reducing the power consumption of electronic circuits [1]. When the supply voltage is reduced to values below the threshold voltage of the transistors, the system operates in the subthreshold region. At device level, subthreshold operation means that transistors are biased in weak inversion. From an analytical point of view, subthreshold operation implies that alternative models have to be used to correctly describe and understand the behavior of the circuits [2]. A widely implemented circuit, both in digital and analog systems, is the Schmitt Trigger (ST) one. The symbol of a single input inverting voltage mode Schmitt trigger is shown in Fig. 1 (a). The characteristic of Schmitt trigger circuits is typically hysteretic, as can be shown in Fig. 1 (b). STs are implemented in many different circuits, such as comparators, oscillators, converters, and others [3]. Recently researchers have also presented models of Schmitt trigger circuits in weak inversion [4]–[10] for low voltage and low power applications. By developing analytical model for ST circuits, designers can have a physical insight into the circuit behavior, thus allowing optimization of the circuit performance. In this article we analyze the subthreshold operation of the inverting CMOS Schmitt trigger circuit proposed by Al-Sarawi, shown in Fig. 1 (c) [11]. The bulk terminals of the PMOS transistors are connected to the supply voltage, while those of the NMOS transistors to ground. They are not shown for simplicity. In our previous work [12], we derived a simple analytical model for the high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages, which define the hysteresis width, as shown in Fig. 1 (b). This article is an extended version of the work presented in [12], and provides a more accurate discussion about the proposed analytical model. In particular, the model assumptions are investigated, by analyzing two different design cases, and by validating simplified equivalent circuits. Furthermore, we provide an analysis of the circuit power consumption. The article is organized as it follows. In Section II we report the proposed analytical model, which is then validated with simulations and measurements in Section III. In Section IV the circuit power consumption is analyzed, while the conclusions are in Section V.

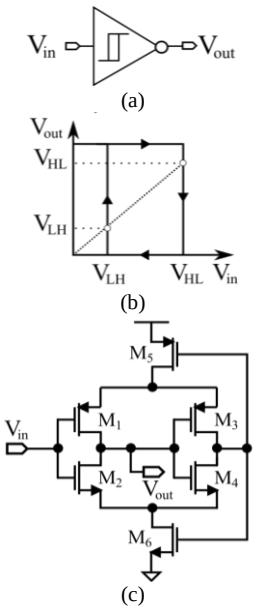

Fig. 1. Schmitt trigger: (a) Single input inverting voltage mode symbol, (b) typical V_{out} vs V_{in} of (a), and (c) Schmitt trigger circuit under analysis. The bulk terminals are not shown for simplicity.

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II. Analytical Model

The MOSFET drain current in weak inversion can be modeled using the Enz-Krummenacher-Vittoz (EKV) model in [13] expressed as

$$I_{d,n(p)} = I_{0,n(p)} e^{\frac{V_{\mathrm{GB(BG)}}}{n_{n(p)}\phi}} \left(e^{-\frac{V_{\mathrm{SB(BS)}}}{\phi}} - e^{-\frac{V_{\mathrm{DB(BD)}}}{\phi}} \right) \quad (1)$$

$$I_{0,n(p)} = 2n_{n(p)}\mu_{n(p)}C_{\mathrm{ox}} \frac{W}{L}\phi^2 e^{\frac{-\left|V_{\mathrm{th},n(p)}\right|}{n_{n(p)}}} \quad (2)$$

- G → gate, D → drain, S → source, B → bulk;
- $n_{n(p)}$→ is the NMOS (PMOS) slope factor;
- ϕ→ thermal voltage;
- $\mu_{n(p)}$→ NMOS (PMOS) carrier mobility;
- C_{ox}→ oxide capacitance;
- W/L→ MOSFET width to length ratio;
- $V_{\mathrm{th},n(p)}$→ NMOS (PMOS) threshold voltage.

In saturation ($|V_{\mathrm{DS}}| \geq 3\phi$ [14]) expression (1) can be simplified to

$$I_{d,n(p)} \approx I_{0,n(p)} e^{\frac{V_{\mathrm{GB(BG)}} - n_{n(p)}V_{\mathrm{SB(BS)}}}{n_{n(p)}\phi}}. \quad (3)$$

Assuming the bulk-source voltage is equal to zero, the expression (3) can be further simplified as

$$I_{d,n(p)} \approx I_{0,n(p)} e^{\frac{V_{\mathrm{GB(BG)}}}{n_{n(p)}\phi}}. \quad (4)$$

Fig. 2 shows the circuit behavior for both threshold voltages of the Schmitt trigger, i.e., low-to-high voltage (V_{LH}), and high-to-low voltage (V_{HL}). The high-to-low voltage (V_{HL}), i.e. when the output voltage (V_{out}) goes from high to low is shown in Fig. 2 (a). In this state V_{in} is low initially and V_{out} is high since the circuit is an inverting ST. In this case, M_1 is on, M_3 is off, and M_5 pulls $V_{m,p}$ to the supply voltage (V_{dd}) since M_4 is on as well. Therefore M_5 is excluded from the figure and M_6 becomes diode-connected. V_{HL} can be determined by finding the switching voltage of the inverter composed of M_1 and M_2, by considering the finite voltage $V_{m,n}$ across M_6 [3]. Assuming that all MOSFETs are in saturation, then M_1 and M_2 are related by:

$$I_{0,p_1} e^{\frac{V_{\mathrm{dd}} - V_{\mathrm{HL}}}{n_p \cdot \phi}} = I_{0,n2} e^{\frac{V_{\mathrm{HL}} - n_n V_{m,n}}{n_n \phi}}. \quad (5)$$

The unknown variable in (5) is the voltage across M_6, i.e. $V_{m,n}$. To determine $V_{m,n}$, we can equate the current in M_2 and M_6:

$$I_{0,n6} e^{\frac{V_{m,n}}{n_n \phi}} = I_{0,n2} e^{\frac{V_{\mathrm{HL}} - n_n V_{m,n}}{n_n \phi}} \quad (6)$$

$$V_{m,n} = \frac{V_{\mathrm{HL}} + n_n \phi \log\left(\frac{I_{0,n2}}{I_{0,n6}}\right)}{1 + n_n}. \quad (7)$$

Next (7) is substituted into (5), and solved for V_{HL} as

$$V_{\mathrm{HL}} = \frac{n_n \left\{ V_{\mathrm{dd}}(1 + n_n) - n_p \phi \left[\log\left(\frac{I_{0,n_2}}{I_{0,p_1}}\right) + n_n \log\left(\frac{I_{0,n_6}}{I_{0,p_1}}\right) \right] \right\}}{n_n^2 + n_n + n_p}. \quad (8)$$

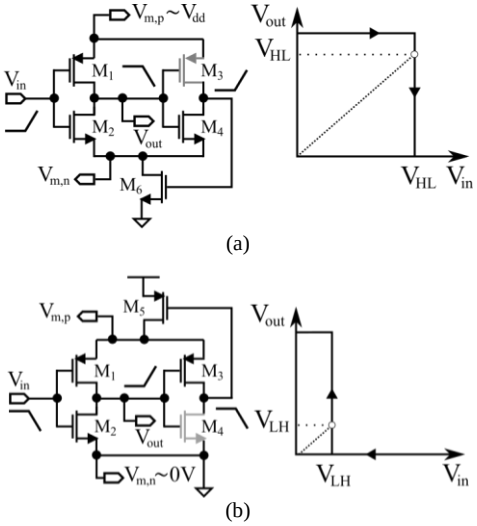

Fig. 2. ST circuits for (a) high-to-low (V_{HL}) and (b) low-to-high (V_{LH}) transition voltages derivation.

From (8) we can read that V_{HL} is linearly dependent on the supply voltage, the thermal voltage, and the temperature. On the other hand, the dependence on the transistors' dimensions is logarithmic. The derived model is simple, and it is based on two assumptions, that M_3 and M_4 do not influence V_{HL} and that $V_{m,p}$ is pulled up to V_{dd}, i.e. M_5 does not influence V_{HL}. As can be noted in (8), if the ratios inside the logarithms are equal to one, then V_{HL} would be dependent only on the slope factors and the supply voltage. In practice, matching these transistors is not trivial, due to process variations and typically different slope factors. The derivation of the low-to-high transition voltage (V_{LH}) is complementary since the transistors are symmetrically arranged. Referring to Fig. 2 (b), when V_{in} is high, V_{out} is low. Therefore, it results that M_4 is off and M_3 is on. M_6 is on which pulles $V_{m,n}$ to gnd, i.e., M_6 does not influence the threshold voltage V_{LH}. As for V_{HL}, we can determine an expression for V_{LH} by initially imposing that:

$$I_{0,p_1} e^{\frac{V_{\mathrm{dd}} - V_{\mathrm{LH}} - n_p(V_{\mathrm{dd}} - V_{m,p})}{n_p \phi}} = I_{0,n_2} e^{\frac{V_{\mathrm{LH}}}{n_n \phi}}. \quad (9)$$

Next we equate the currents in M_1 and M_5, to determine $V_{m,p}$:

$$I_{0,p_1} e^{\frac{V_{\mathrm{dd}} - V_{\mathrm{LH}} - n_p(V_{\mathrm{dd}} - V_{m,p})}{n_p \phi}} = I_{0,p_5} e^{\frac{V_{\mathrm{dd}} - V_{m,p}}{n_p \phi}} \quad (10)$$

$$V_{m,p} = \frac{V_{\mathrm{LH}} + n_p \left[V_{dd} + \phi \log\left(\frac{I_{0,p_5}}{I_{0,p_1}}\right) \right]}{1 + n_p}. \quad (11)$$

Substituting (11) in (9), and solving for V_{LH} the expression in (12) is finally obtained as

$$V_{\mathrm{LH}}=\frac{n_n\left\{V_{\mathrm{dd}}-n_p\phi\left[n_p\log\left(\frac{I_{0,n_2}}{I_{0,p_5}}\right)+\log\left(\frac{I_{0,n_2}}{I_{0,p_1}}\right)\right]\right\}}{n_p^2+n_p+n_n}. \quad (12)$$

As for V_{HL}, V_{LH} is linearly dependent on the supply voltage, the thermal voltage, and on the temperature and logarithmic on the transistors' dimensions. V_{HL} depends on M_1, M_2, and M_6. Instead V_{LH} depends on M_1, M_2, and M_5. Therefore the proposed analytical model provides physical insight into the circuit behavior, since it relates the hysteresis transition voltages (Thresholds) to the power supply and the temperature. From a design point of view, the derived expressions allow designers to optimize the ST circuit under analysis. For instance, by minimizing the terms inside the square brackets in (8) and (12), the circuit can be made more insensitive to temperature variations. Clearly, the model is valid under the assumptions that the second inverter does not influence the transition points and that the resistances of M_5 and M_6 are negligible during the high-to-low and low-to-high transitions, respectively. As will be verified in the next section, these assumptions are validated when the transistors are wide with respect to the channel length. This is due to the fact the wide transistors present lower ON resistance.

III. Model Validation

To verify the derived expressions, simulations have been performed. First we show a worst-case design (Design 1), i.e., we implement a ST with not optimized transistors dimensions. Next we provide an optimized design (Design 2), which respects the model assumptions. To quantify the error between the analytical and simulated voltages, we introduce the absolute and relative errors as

$$\mathrm{AE}_{\mathrm{HL(LH)}}=\left|V_{\mathrm{HL(LH)}}-V_{\mathrm{HL(LH),sim}}\right| \quad (13)$$

$$\mathrm{RE}_{\mathrm{HL(LH)}}=\frac{\mathrm{AE}_{\mathrm{HL(LH)}}}{V_{\mathrm{HL(LH),sim}}}\times 100\%. \quad (14)$$

The relative errors are computed against $V_{\mathrm{HL(LH),sim}}$, i.e. the simulated transition voltages are considered as reference values.

A. Design 1

The simulation parameters used for Design 1 are shown in Table I, second column. The slope factors of transistors n_n and n_p are 1.25 and 1.3, respectively. The transconductance is defined as $\beta_{n(p)}=\mu_{n(p)}C_{\mathrm{ox}}W/L$. V_{HL} is extracted for supply voltages V_{dd} ranging from 0.5V to 0.6V, therefore all the modeled transistors (M_1, M_2, and M_6) are in weak inversion. For $V_{\mathrm{dd}}>V_{\mathrm{th,2}}$, the transistor M_2 is still in weak inversion because the resulting voltage at its source ($V_{m,n}$) is greater than $3\,\phi \approx 78$mV at the initial circuit state (when V_{in}=0V). This has been verified through simulations, as can be seen in Fig. 3 (b). Regarding M_4, it should not influence V_{HL}, according to the model assumptions. The analytical and simulated V_{HL} as a function of V_{dd} are shown in Fig. 3 (a). The model resembles the simulated behavior, and V_{HL} is linearly related to the supply voltage, as expected from (8). The maximum absolute error for V_{HL} in Design 1 is $\mathrm{AE}_{\mathrm{HL,1}}$=19mV, while the relative one is $\mathrm{RE}_{\mathrm{HL,1}}$=8%, when V_{dd}=0.5V. The analytical and simulated V_{LH} as a function of V_{dd} are shown in Fig. 3 (c). In this case both offset and gain errors are present. The maximum absolute error is $\mathrm{AE}_{\mathrm{LH,1}}$=48mV, while the relative one is $\mathrm{RE}_{\mathrm{LH,1}}$=66%. The error is attributed to M_3, M_4, M_5 and M_6. As previously explained, the model assumes that M_3 and M_4 act as ideal switches, forcing M_5 and M_6 in diode-connected configuration.

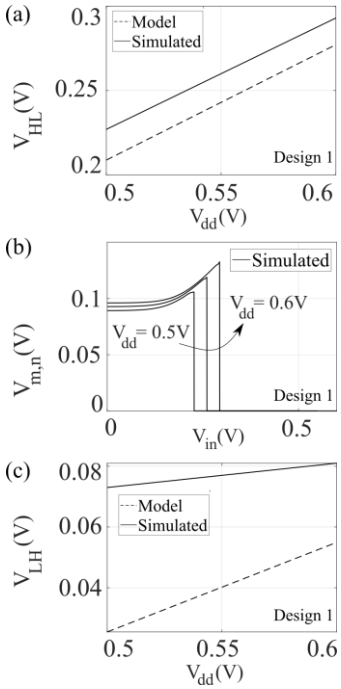

Fig. 3. Design 1: (a) modeled and simulated V_{HL} vs V_{dd}, (b) simulated $V_{m,n}$ vs V_{in} for different V_{dd}, and (c) modeled and simulated V_{LH} vs V_{dd}.

TABLE I: Simulation Parameters

Parameter	Design 1	Design 2
	Value	Value
L	0.5μm	0.5μm
$W_{2,4,6}$	1μm	20μm
$W_{1,3,5}$	2μm	40μm
$V_{\mathrm{th,2}}$	559mV	574.2mV
$V_{\mathrm{th,6}}$	533.4mV	563.7mV
$V_{\mathrm{th,1,5}}$	−744.1mV	−734.5mV
$\lvert\beta_{1,5}\rvert$	174.2μA/V^2	1.795mA/V^2
$\beta_{2,6}$	303μA/V^2	6.834mA/V^2

Furthermore, it assumes that the ON resistances across M_5 and M_6 are negligible as shown in Fig. 2.

B. Design 2

In Design 2 we increase the width of the transistors, to validate the model assumptions. The widths of M_1, M_3, and M_5 are set to 40μm, while those of M_2, M_4, and M_6 to 20μm. The simulation parameters used for Design 2 are shown in Table I, third column. The analytical and simulated V_{HL} and V_{LH} as a function of V_{dd} are shown in Fig. 4 (a) and Fig. 4 (b). The maximum absolute error for

V_{HL} is $AE_{HL,2}$=20mV, while the relative one is $RE_{HL,2}$=8%, when V_{dd}=0.5V. The maximum absolute error for V_{LH} in is $AE_{LH,2}$=20mV, while the relative one is $RE_{LH,2}$=33%. $RE_{LH,2}$ is higher than $RE_{HL,2}$ because $AE_{LH,2}$ is divided by a smaller number since V_{LH} occurs for lower voltages, with respect to V_{HL}. On the basis of this analysis it can be concluded that the model is more accurate when the transistors in the ST circuit are large as compared to the minimum channel length. In Design 2 we enlarged the widths of all transistors, although the model only requires M_3, M_4, M_5 and M_6 to be enlarged. We also considered the case in which M_3, M_4, M_5 and M_6 are large, while M_1 and M_2 are small. What we observed is that if the transistors of the first inverter are too small as compared to the transistors in the feedback, the error does not improve as in the case in which all transistors are enlarged. Nevertheless, the error relative to V_{dd}, i.e. $AE_{HL(LH)}/V_{dd}$, is always below 10% for the designed circuits, implying that the worst case analysis is relatively the worst.

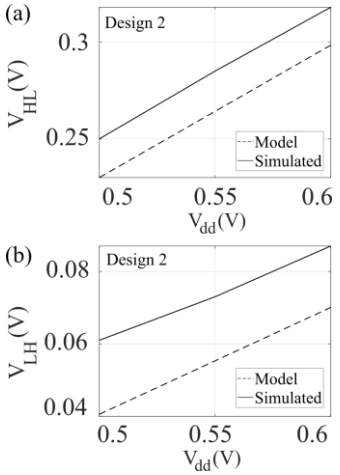

Fig. 4. Design 2: modeled and simulated (a) V_{HL} vs V_{dd} and (b) V_{LH} vs V_{dd}.

C. Simplified Equivalent Circuits

To further analyze the model assumptions, the simplified equivalent circuits in Fig. 5 (a) and Fig. 5 (b) are simulated. The circuits in Fig. 5 (a) and Fig. 5 (b) are the simplified equivalent circuits associated to those Fig. 2 (a) and Fig. 2 (b), respectively. These circuits approximate the circuit behavior at the initial state, i.e. V_{in}=0V for V_{HL} and V_{in}=V_{dd} for V_{LH}. The transistors are sized as in Design 2. In Fig. 5 (c) the simulated V_{out} vs V_{in} of the full circuit for different V_{dd} are shown. As can be observed, the output swings between the supply rails. In Fig. 5 (d) the simulated V_{out} vs V_{in} of the simplified equivalent circuit in Fig. 5 (a) is shown. The output does not reach 0V since in the simplified circuit M_6 is always diode-connected. Nevertheless, V_{HL} is almost the same for both full and simplified circuits since the maximum difference is below 2mV. In Fig. 5 (e) the simulated V_{out} vs V_{in} of the simplified equivalent circuit in Fig. 5 (b) is shown. As can be observed, the output does not reach V_{dd}. This is attributed to M_5, which is always on. Nevertheless, V_{LH} is almost the same for both full and simplified circuits since the maximum difference is below 2mV, as for V_{HL}. On the basis of these results it can be concluded that the simplified equivalent circuits correctly describes the ST circuit under analysis, when the transistors are correctly sized.

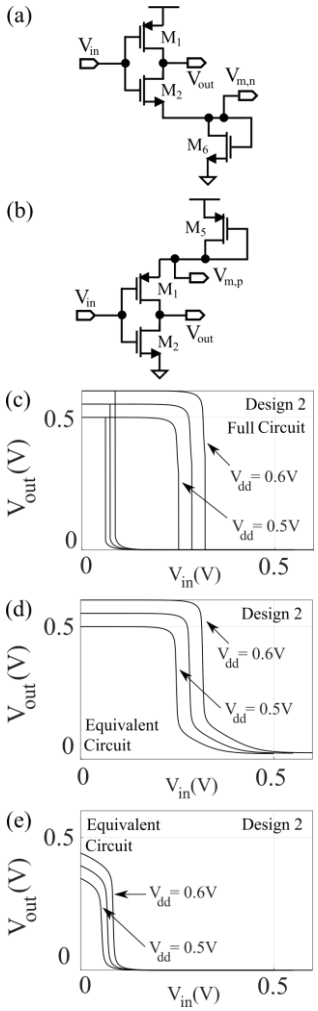

Fig. 5. Simplified equivalent circuits for (a) V_{HL} and (b) V_{LH} analysis. Design 2: (c) simulated V_{out} vs V_{in} for different V_{dd} when considering the full circuit; simulated V_{out} vs V_{in} for different V_{dd} when considering the simplified equivalent circuits for (d) V_{HL} and (e) V_{LH}.

D. Experimental Validation

A prototype realized in AMS 0.35µm CMOS process has been tested. The fabricated circuit and the layout are shown in Fig. 6 (a). The area occupied by the circuit is 49µm×25µm. The channel length is 1µm, while the NMOS and PMOS transistors are sized 1/1 and 18/1, respectively. This design provides the desired hysteresis for further applications. The transition voltages have been extracted at V_{dd}=0.6V, by applying a low frequency ($1/f$=5s) triangular wave, as shown in Fig. 6 (b). For this design, the analytical V_{HL} is 317mV, while V_{LH}=96mV. The measured transition voltages are $V_{HL,meas}$=329mV and $V_{LH,meas}$=131mV. Therefore, we have that $AE_{HL,meas}$=12mV and $AE_{LH,meas}$=35mV. The larger errors in the measured transition voltages are mainly attributed to the experimental setup, e.g. parasitic components associated to the ASIC pads.

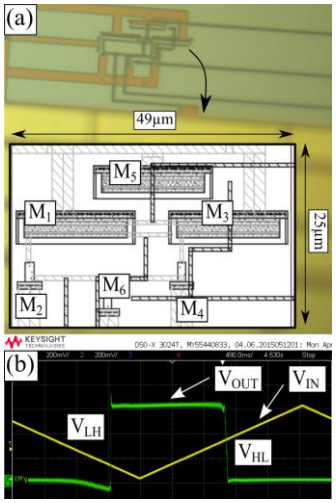

Fig. 6. Fabricated circuit (AMS 0.35 µm CMOS Process): (a) Photograph and layout of the ST circuit, and (b) measured V_{out} vs V_{in}.

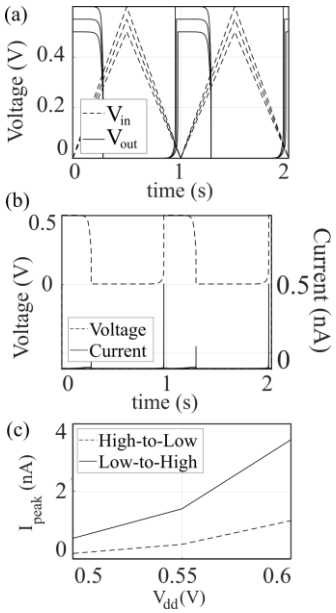

Fig. 7. Simulation results: (a) V_{out} and V_{in} for different V_{dd}, (b) current drawn from V_{dd}, and V_{out} when V_{dd}=0.5V, and (c) maximum peak currents during the high-to-low and low-to-high transitions for different V_{dd}.

IV. Power Consumption

In this section, we analyze the power consumption of the ST circuit. The transistors are sized according to Design 2. We performed a transient analysis by applying a 1Hz triangular wave at the input of the ST circuit loaded by a capacitance of 1pF. In Fig. 7 (a) the output and input voltages are depicted, for different supply voltages. In Fig. 7 (b) the current drawn by the supply voltage is shown for V_{dd}=0.5V. As can be observed, the peaks in the current occur during the high-to-low and low-to-high transitions. This is expected since the power consumption of a ST is mainly due to the switching current. During the high-to-low transition, the peak current has a value of 159pA, while during the low-to-high transition, the peak value is 615pA. The higher power consumption during the low-to-high transition is attributed to transistors M_5, which is in diode-connected configuration during the transition. The maximum peak currents are shown in Fig. 7 (c). As can be observed, the peak currents associated to the low-to-high transition are higher than those associated to the high-to-low one. The peak current can be decreased by reducing the widths of the transistors in the PMOS branch. When the same circuit is driven at 3.3V, which is the nominal voltage of the considered CMOS process, the maximum peak of the current has a value of 1.74mA, which is more than six orders of magnitude larger than the case in which the supply voltage is 0.5V. Therefore, the proposed model allows to optimize the performance of the circuit for low power operation, since the presented analysis shows the contribution of the transistors during the switching phase (Fig. 5 (a) and Fig. 5 (b)).

V. Conclusion

In this article, we analyzed the subthreshold operation of an inverting CMOS Schmitt trigger. We derived analytical expressions of the high-to-low and low-to-high hysteresis transition voltages. The model provides physical insight into the circuit behavior, i.e., the transition voltages are linearly related to the supply voltage and the temperature and logarithmically dependent on the transistors' dimensions. We analyzed the model limitations by investigating different designs. When the widths of the transistors are large as compared to the minimum channel length, the error between the analytical and simulated transition voltages is reduced. When the transistors' dimensions are optimized, the maximum absolute error for both transition voltages is 20mV. Instead, the error relative to the supply voltage is below 10%. The model assumptions have been validated by analyzing simplified equivalent circuits. The error between the full circuit and the simplified ones is below 2mV, when the model assumptions are respected. A prototype in AMS 0.35 µm CMOS process has been fabricated to experimentally validate the derived expressions, providing a maximum error below 36mV. The power consumption of the circuit has been analyzed by performing transient simulations for different supply voltages. When the subthreshold operation is exploited (V_{dd}=0.5V), the performance of the circuit has an improvement of more than six orders of magnitude in the switching current, with respect to the case in which the supply voltage is 3.3V.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

A. Nowbahari derived the analytical model, and performed simulations and measurements; L. Marchetti and M. Azadmehr supervised the work; all authors had approved the final version.

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