Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks

Nowbahari, Arian; Marchetti, Luca; Azadmehr, Mehdi
Department of Microsystems - University of South-Eastern Norway

This is an Accepted Manuscript of an article published by IEEE Online in *2022 11th International Conference on Communications, Circuits and Systems (ICCCAS)* on July 18, 2022, available online: https://doi.org/10.1109/ICCCAS55266.2022.9825344

Nowbahari, A., Marchetti, L. & Azadmehr, M. (2022, May 13-15). *Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks* [Conference presentation]. 2022 11th International Conference on Communications, Circuits and Systems (ICCCAS), Singapore. IEEE. https://doi.org/10.1109/ICCCAS55266.2022.9825344

Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks

Arian Nowbahari
Department of Microsystems (IMS)
University of South-Eastern Norway
Borre, Norway
arian.nowbahari@usn.no

Luca Marchetti
Department of Microsystems (IMS)
University of South-Eastern Norway
Borre, Norway
luca.marchetti@usn.no

Mehdi Azadmehr
Department of Microsystems (IMS)
University of South-Eastern Norway
Borre, Norway
mehdi.azadmehr@usn.no

***Abstract*—Wireless sensor networks (WSNs) generally consist of thousands of sensor nodes, each one supplied by a battery or harvested energy. To prolong the lifetime of wireless sensor networks, wake-up receivers (WuRxs) are typically employed. WuRxs can selectively activate sensor nodes, by decoding a signal called wake-up call (WuC). Therefore they optimize the power management of WSNs, by allowing communication when requested. In this article an ultra-low power implementation of a sequential WuRx concept is proposed. The WuRx is composed of AND gates, switches and monostable circuits. The monostable circuit is implemented through a transistor which generates a pulse according to a simple RC network and a switch. The proposed WuRx decodes the WuC signal by comparing the duty cycle of the received signal with the output signals of the monostable circuits. The ultra-low power implementation is validated at simulation level. The WuRx consumes 32.8nW when decoding a 3-bit wake-up call signal, and 153nW when decoding 11 bits.**

***Index Terms*—CMOS, low power, monostable, sensor node, wake-up receiver, wireless sensor network**

I. Introduction

The Internet-of-Things paradigm is mainly enabled by wireless sensor networks (WSNs), which consist of groups of sensors with processing and communication capabilities, called sensor nodes (Fig.1(a)) [1], [2]. The network size ranges from few units up to thousands, depending on the application. WSNs are extremely versatile in terms of applications, since they are employed in agriculture, smart buildings, animal and vehicle tracking, security, surveillance, health care and many other application areas [3]. From an architecture point of view, a sensor node is generally composed of four units, i.e. wireless communication, sensing, processing and power management units, as shown in Fig.1(b) [4]. The wireless communication unit is in charge of transmitting and receiving data and/or power. The sensing unit acquires data from the environment. The acquired data are then elaborated by the processing unit, which usually is a microcontroller. All these blocks are typically supplied by a power management unit, which can be a simple battery or a more complex circuit based on energy harvesting [5]. Generally the most power consuming unit is the processing one, which therefore represents the bottleneck of the sensor node architecture. Therefore the power management unit is critically important, since it determines the network lifetime by managing the supplied power [6]. Researchers proposed different solutions for improving the network lifetime such as: topology control, power management optimization, data reduction, energy-efficient acquisition, mobile-sink, mobile-relay, routing, data gathering and network coding [7]–[11]. At hardware level a typical power-efficient approach consists into implementing wake-up receivers (WuRxs). WuRxs can selectively activate a sensor node when a well defined signal, the wake-up call (WuC) signal, is decoded [12]–[14]. They therefore allow activation of sensor nodes on demand. From an architecture

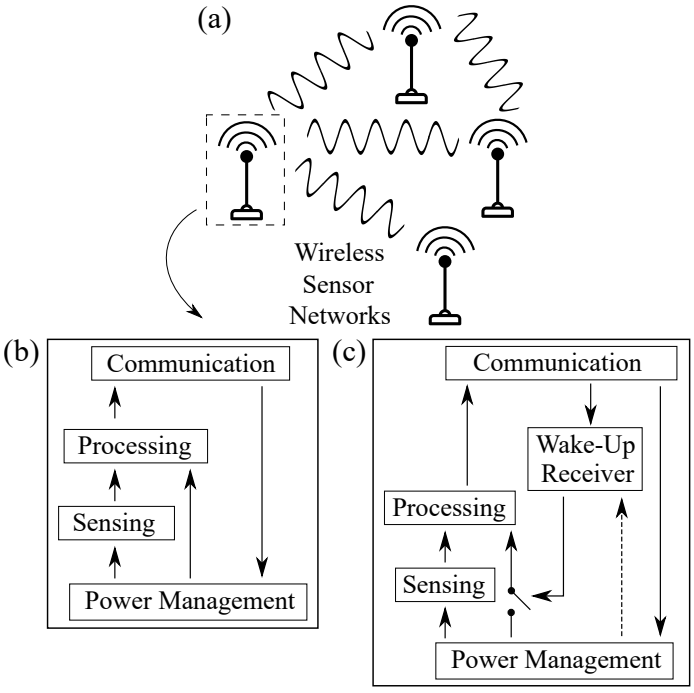

Fig. 1. (a) Wireless sensor network. (b) Typical sensor node architecture. (c) Integration of wake-up receivers (WuRxs). The arrow between the WuRx and the power management unit is dashed because in some architectures WuRxs are powered by the communication unit.

This work was supported by the Research Council of Norway [273248].

point of view, they enable the link between the processing and power management units, i.e. when the correct WuC signal is detected, they wake up the processing unit, which sends the elaborated data to the communication unit, as shown in Fig.1(c). In the latter figure the WuRx is supplied by the power management unit. But depending on the architecture, WuRxs can also be powered by the WuC signal too. The WuC can be based on radio, optical and acoustic signals depending on the medium of transmission. In our previous work, we proposed an ultra-low power WuRx based on a NOR-based monostable multivibrator topology for acoustic applications [15]. In this article we report a simpler and less power consuming monostable circuit, composed of only two transistors, two resistors and a capacitor. Instead the monostable in [15] is composed of six transistors, one capacitor and one resistor. The proposed circuit is verified by simulations, by considering an acoustic WuC signal with carrier frequency of $40kHz$. The WuRx consumes $32.8nW$ when detecting the WuC signal 101, where each level has a duration of $1.5ms$. For such a code, the WuRx requires 22 transistors. We also evaluated the average power consumption for more complex WuC signals. The average power consumption and the number of implemented transistors linearly increase with the number of bits in the WuC signal. When considering 11 bits, the WuRx consumes $153nW$ and it requires 94 transistors. The proposed circuit is described in Section II. The simulations results are reported in Section III, and in the same section the proposed WuRx is compared with other WuRxs in the literature. The conclusions are in Section IV.

II. Circuit Description

The proposed WuRx decodes the WuC signal by measuring its duty cycle. The WuC signal consists of a series of bursts. We associate the high logic value 1 to the presence of the burst, and the low logic value 0 to the absence of the burst. To explain the WuRx operation it is assumed that the WuC signal is 101, which is the simplest code that can be decoded. The block diagram associated to this example is shown in Fig.2(a). In real application scenarios, the sensor node are placed far away from each other. This implies that the communication unit can be unable to manage the amplitude of the received bursts. Thus a Step-Up block is considered. After passively amplifying the received burst (S_{RX}), the signal goes into the block Rectification. The latter generates the signal S_R which has a duration equal to that of the received burst. The first received burst triggers Monostable 1, which in response generates the pulse S_{m_1}. The monostable is designed so that its output duration is equal at least to the burst period. To decode the second value in the WuC signal (i.e. the 0 in 101), the AND operation is performed between the inverted rectified signal and the first monostable output. This closes Switch 1, which connects the rectified signal with the second monostable. To detect the last value of the WuC signal (i.e. the last 1 in 101), the AND operation between the rectified signal and the output of Monostable 2 is performed. The final output is the interrupt signal, which wakes up the sensor node

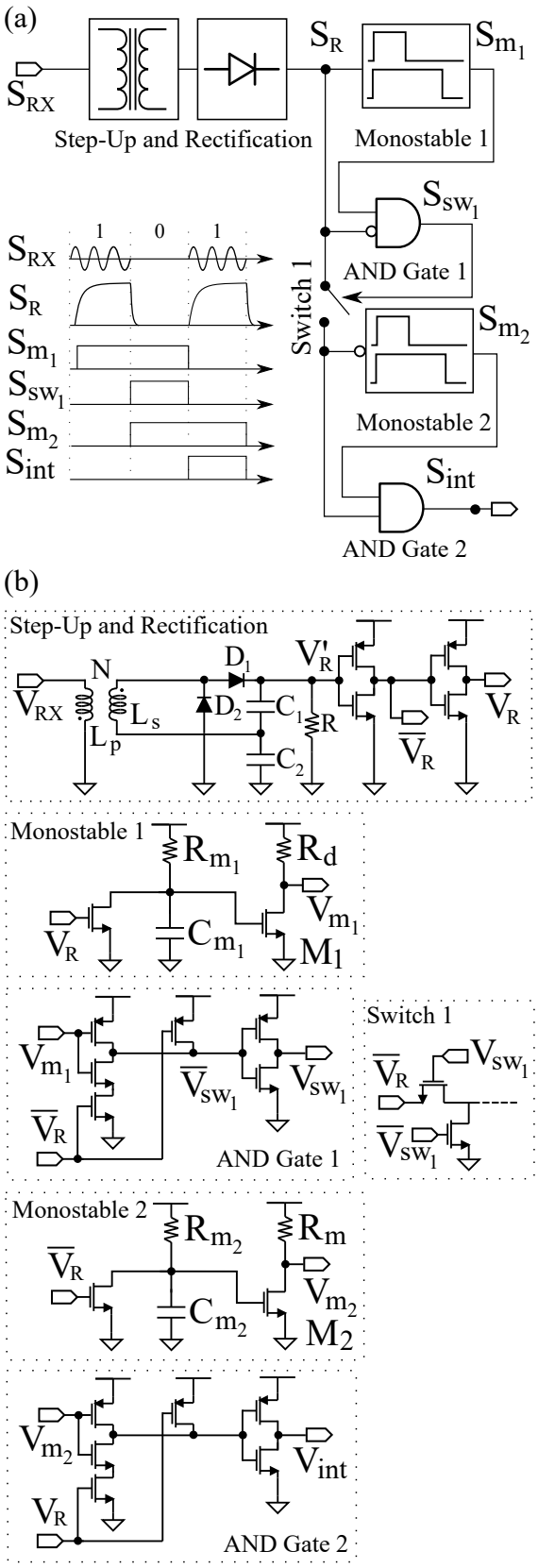

Fig. 2. (a) WuRx block diagram and example of waveforms when assuming that the WuC signal is 101. (b) Associated WuRx circuit implementation.

by connecting the processing unit to the power management one. The proposed architecture is modular, i.e. a longer WuC signal can be decoded by cascading other monostables, AND gates and switches. For an N-value WuRx, $N-2$ switches and $N-1$ monostables and AND gates are necessary. The process through which the WuC signal is decoded is sequential, so if a wrong bit is detected the successive stages are not activated. The circuit associated to this example is shown in Fig.2(b). The passive amplification and rectification is performed through a loaded voltage doubler. A CMOS buffer is used to smooth the received voltage, and to generate the inverted rectified voltage. The AND gate is an inverted NAND. The switch circuit also avoids floating gate at the input of the monostables. As reported in the introduction, this WuRx concept has been proposed in our previous work [15]. The novelty of this work is the simplification of the monostable circuit. Instead of using a NOR-based monostable multivibrator (6 transistors, 1 capacitor, 1 resistor) [16], we use a simpler circuit composed of 2 transistors, 1 capacitor and 2 resistors. This monostable works as it follows: once V_R reaches the first monostable circuit, the capacitor C_{m_1} is discharged and transistor M_1 is switched off. As soon as V_R goes down, C_{m_1} gets charged with a time given by $C_{m_1} \times R_{m_1}$. Once the threshold voltage of M_1 is reached, V_{m_1} goes low. Therefore it works as a simple timer, triggered by the received voltage. The same reasoning applies for the others monostable circuits, which are enabled through the switches.

III. Simulations Results

The proposed circuit implementation is validated at simulation level, by considering a TSMC-180nm CMOS process. An acoustic WuC signal is considered, with frequency $f = 40kHz$. The duration of the high and low logic values influences the design of the step-up and rectification circuits as well as the time constant of the monostables. The minimum duration of a logic value has be greater than the period of the input signal, i.e. $T = 25\mu s$, for a correct rectifier operation. In our previous work we fixed the duration of the logic value to $1.5ms$. Clearly a shorter or longer duration can be considered, since the time constant of the monostables is a design variable. In order to make a comparison with the previously proposed NOR-based monostable multivibrator, we fixed the the duration of the logic values to $1.5ms$, and the burst period to $3ms$. Initially the WuC signal 101 is considered. The parameters used for the simulations are shown in Table I. The supply voltage is $1.2V$. The rectifier is designed so that its time constant is fast enough to be aligned with the associated burst. The monostable is designed so that its output signal is high during the comparison with the voltages V_R and $\overline{V}_R$. The transistors are sized to minimize the power consumption. Resistors with very high resistance ($100M\Omega$) are used for minimizing the average current and so the power consumption. Clearly these resistors are not feasible for Integrated Circuits, but they can be eventually mounted off-chip. In Fig.3(a) the voltage V_{RX} is shown. It consists of three burst with frequency $40kHz$ and amplitude $300mV$. As previously described, the burst duration is $1.5ms$, and the burst period is $3ms$. The voltage V_R' is the voltage across the resistor in the rectifier in Fig.2(b). This voltage has to be higher than the threshold voltage of the CMOS buffer. Thus the voltage after the buffer, i.e. V_R, ranges from zero volts to V_{DD} as required. As can be observed V_R is aligned with V_{RX} and so with the WuC signal. In Fig.3(b) the output voltage of the first monostable (V_{m_1}) is shown. As can be observed, once V_R goes low, $V_{m,1}$ slowly goes low too. But around $3ms$ the output of the first monostable goes high again, since the capacitor C_{m_1} gets discharged by the last 1 in the WuC signal. This phenomenon does not affect the decoding mechanism, since the logic gate compares $\overline{V}_R$ with V_{m_1} during the time window $[1.5ms - 3.5ms]$. As expected, V_{sw_1} closes Switch 1, resulting in the triggering of the second monostable. The latter generates V_{m_2}, which is then compared with V_R to produces V_{int}, as shown in Fig.3(c).

A. Power Consumption

When decoding the WuC signal 101, the simulated 3-value WuRx consumes $27.3nA$ at which corresponds an average power consumption of $32.8nW$. Clearly the power consumption is a function of the WuC signal complexity. In order to characterize the power consumption as a function of the number of decoded bits, different simulations have been performed. In particular, we considered five different N-value WuRxs, with N ranging from 3 up to 11, with steps of 2. This means that the less complex considered WuC signal is 101, decoded by a WuRx with 2 monostables and AND gates and 1 switch; while the more complex one is 10101010101, decoded by a WuRx with 10 monostables and AND gates and 9 switches. The average power consumption as a function of the decoded bits is shown in Fig.4(a). As can be observed, the power consumption linearly increases with the number of bits. When 3 bits are considered, the power consumption is $32.8nW$, while when 11 bits are considered, the power consumption is $153nW$. Each stage introduces about $15nW$ to the power consumption. In our previous work the computed average power consumption when decoding a 4-value WuC was about $800nW$, while the new implementation consumes about $47nW$ when decoding a WuC signal with the same complexity. Therefore the proposed monostable implementation is about 17 times more efficient than the NOR-based one. Regarding the number of required transistors, a 3-value WuRx needs 22 transistors, i.e. 9 per decoded bit, plus 4 transistors

TABLE I
Parameters used in the Simulations

Supply Voltage	V_{DD}	$1.2V$
Transformer	L_p	$4\mu H$
	L_s	$400\mu H$
Rectifier	C	$200nF$
	R	300Ω
Monostable	C_m	$51pF$
	R_m	$100M\Omega$
	R_d	$100M\Omega$

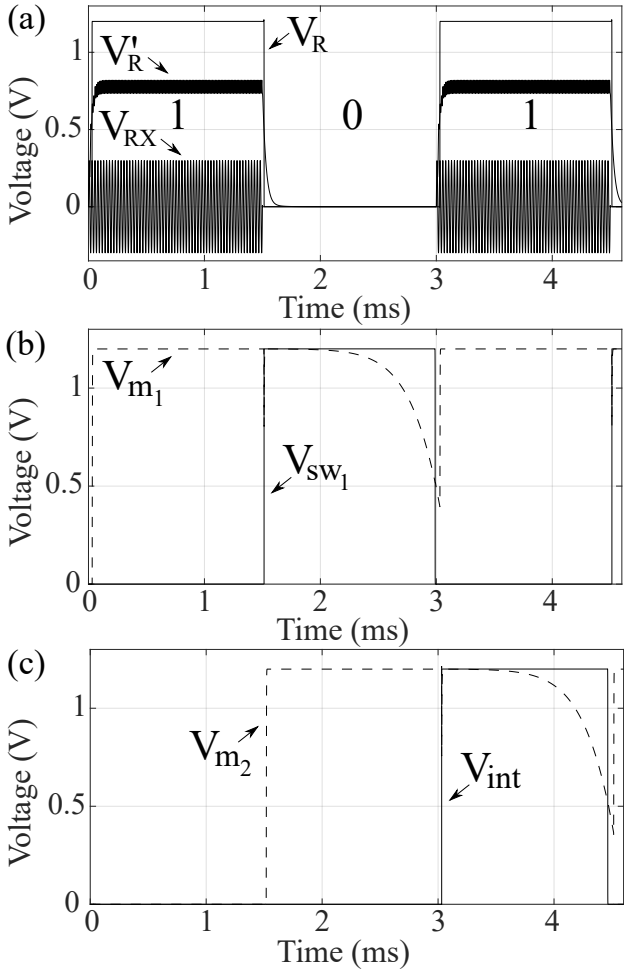

Fig. 3. Simulations results when the WuRx decodes the WuC signal 101: (a) V_{RX}, V_R' and V_R. (b) V_{m_1} and V_{sw_1}. (c) V_{m_2} and V_{int}.

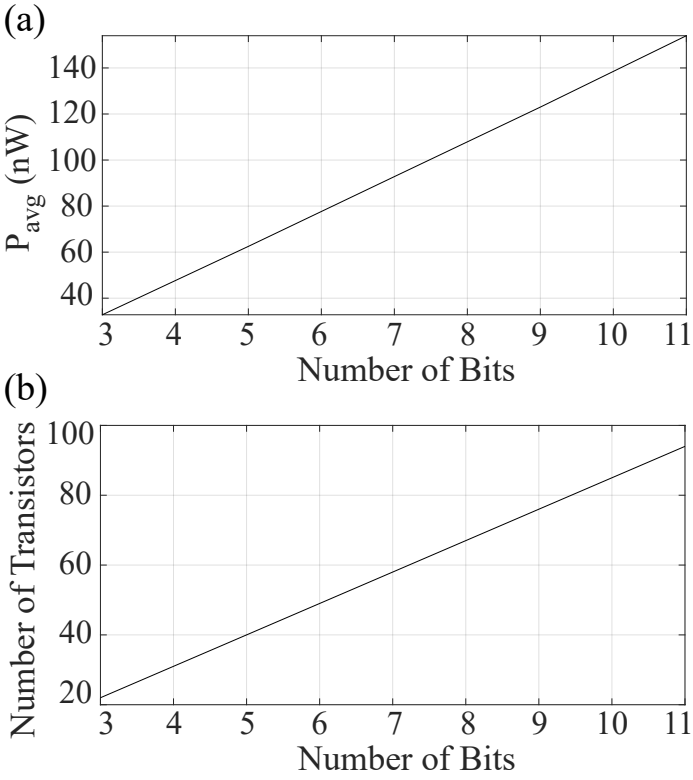

Fig. 4. (a) Average power consumption as a function of number of bits. (b) Number of transistors required as a function of number of bits.

TABLE II
PERFORMANCE COMPARISON

$\mathbf{P_{active}}$	$\mathbf{f_{input}}$	$\mathbf{V_{dd}}$	**Work**
$32.8nW$	$40kHz$	$1.2V$	This
$8.1\mu W$	$85kHz$	$3.3V$	[18]
$420\mu W$	$20kHz$	$3V$	[19]
$14\mu W$	$40kHz$	$2V$	[20]
$4\mu W$	$43kHz$	$0.6V$	[21]
$8nW$	$57kHz$	$0.5V$	[17]
$1\mu W$	$41kHz$	$0.3V$	[22]

in the CMOS buffer. As previously explained, the first bit is used to trigger the system. For a 5-value WuRx the number of required transistors will be 40. For a 11-value WuRx 94 transistors are required. As can be observed in Fig.4(b), the number of transistors linearly increases with the number of bits. We compared the performance of the proposed WuRx with prior art in Table II. We considered WuRxs working in the same frequency range of the implemented one. As can be observed the proposed WuRx is ultra-low power, although it is not the less power consuming since the work in [17] consumes $8nW$. In the latter work the supply voltage is $0.3V$, i.e. four times the one used in this work. By reducing the supply voltage in our circuit to $0.6V$, increasing the amplitude of the transmitted voltage to $400mV$ and increasing R_m to $200M\Omega$, the power consumption of our architecture lowers to $7.2nW$. Clearly a fabricated WuRx would require a more precise design, due to leakages and parasitics.

IV. CONCLUSIONS

In this article we proposed an ultra-low power monostable-based wake-up receiver for wireless sensor networks. The implemented circuit uses a simple timer for wake-up call decoding. It consumes $32.8nW$ when decoding 3 bits, and $153nW$ when decoding 11 bits at $V_{DD} = 3.3V$. The power consumption lowers to $7.2nW$ when the supply voltage is scaled down to $2V$. Future work will focus on ASIC integration and circuit optimization.

REFERENCES

[1] N. Khalil, M. R. Abid, D. Benhaddou, and M. Gerndt, "Wireless sensors networks for Internet of Things," in *2014 IEEE Ninth International Conference on Intelligent Sensors, Sensor Networks and Information Processing (ISSNIP)*, 2014, pp. 1–6.

[2] S. M. Oteafy and H. S. Hassanein, "Resource Re-use in Wireless Sensor Networks: Realizing a Synergetic Internet of Things." *J. Commun.*, vol. 7, no. 7, pp. 484–493, 2012.

[3] S. R. Jino Ramson and D. J. Moni, "Applications of wireless sensor networks — A survey," in *2017 International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology (ICEEIMT)*, 2017, pp. 325–329.

[4] W. Dargie and C. Poellabauer, *Fundamentals of wireless sensor networks: theory and practice*. John Wiley & Sons, 2010.

[5] F. K. Shaikh and S. Zeadally, "Energy harvesting in wireless sensor networks: A comprehensive review," *Renewable and Sustainable Energy Reviews*, vol. 55, pp. 1041–1054, 2016.

[6] F. Engmann, F. A. Katsriku, J.-D. Abdulai, K. S. Adu-Manu, and F. K. Banaseka, "Prolonging the lifetime of wireless sensor networks: a review of current techniques," *Wireless Communications and Mobile Computing*, vol. 2018, 2018.

[7] G. Anastasi, M. Conti, M. Di Francesco, and A. Passarella, "Energy conservation in wireless sensor networks: A survey," *Ad hoc networks*, vol. 7, no. 3, pp. 537–568, 2009.

[8] H. Yetgin, K. T. K. Cheung, M. El-Hajjar, and L. H. Hanzo, "A Survey of Network Lifetime Maximization Techniques in Wireless Sensor Networks," *IEEE Communications Surveys Tutorials*, vol. 19, no. 2, pp. 828–854, 2017.

[9] S. M. Chowdhury and A. Hossain, "Different energy saving schemes in wireless sensor networks: A survey," *Wireless Personal Communications*, vol. 114, no. 3, pp. 2043–2062, 2020.

[10] F. D. Tolba and P. Lorenz, "Based Energy-Efficient for Extending Mobile Wireless Sensor Networks Lifetime," *Journal of Communications*, vol. 14, no. 12, 2019.

[11] N. Lavanya and T. Shankar, "Energy efficient cluster head selection using hybrid squirrel harmony search algorithm in WSN," *Energy*, vol. 10, no. 12, 2019.

[12] R. Piyare, A. L. Murphy, C. Kiraly, P. Tosato, and D. Brunelli, "Ultra Low Power Wake-Up Radios: A Hardware and Networking Survey," *IEEE Communications Surveys Tutorials*, vol. 19, no. 4, pp. 2117–2157, 2017.

[13] H. Bello, Z. Xiaoping, R. Nordin, and J. Xin, "Advances and opportunities in passive wake-up radios with wireless energy harvesting for the internet of things applications," *Sensors*, vol. 19, no. 14, p. 3078, 2019.

[14] I. Demirkol, C. Ersoy, and E. Onur, "Wake-up receivers for wireless sensor networks: benefits and challenges," *IEEE Wireless Communications*, vol. 16, no. 4, pp. 88–96, 2009.

[15] A. Nowbahari, L. Marchetti, and M. Azadmehr, "An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks," in *2021 IEEE 7th World Forum on Internet of Things (WF-IoT)*, 2021, pp. 380–384.

[16] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*. John Wiley & Sons, 2019, ch. 18, pp. 539–540.

[17] A. S. Rekhi and A. Arbabian, "Ultrasonic Wake-Up With Precharged Transducers," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1475–1486, 2019.

[18] A. Sánchez, S. Blanc, P. Yuste, A. Perles, and J. J. Serrano, "An Ultra-Low Power and Flexible Acoustic Modem Design to Develop Energy-Efficient Underwater Sensor Networks," *Sensors*, vol. 12, no. 6, pp. 6837–6856, 2012.

[19] A. Bannoura, F. Höflinger, O. Gorgies, G. U. Gamm, J. Albesa, and L. M. Reindl, "Acoustic Wake-Up Receivers for Home Automation Control Applications," *Electronics*, vol. 5, no. 1, p. 4, 2016.

[20] E. Lattanzi, M. Dromedari, V. Freschi, and A. Bogliolo, "A sub-μA ultrasonic wake-up trigger with addressing capability for wireless sensor nodes," *International Scholarly Research Notices*, vol. 2013, 2013.

[21] K. Yadav, I. Kymissis, and P. R. Kinget, "A 4.4uW wake-up receiver using ultrasound data communications," in *2011 Symposium on VLSI Circuits - Digest of Technical Papers*, 2011, pp. 212–213.

[22] H. Fuketa, S. O'uchi, and T. Matsukawa, "A 0.3-V 1-μW Super-Regenerative Ultrasound Wake-Up Receiver With Power Scalability," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 9, pp. 1027–1031, 2017.