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Weak Inversion Model of an Inverting CMOS Schmitt Trigger

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***Abstract*— In this article the subthreshold characteristics of an inverting single input CMOS Schmitt trigger circuit are analyzed. Analytical expressions for the low-to-high and high-to-low hysteresis transition voltages are determined. The analytical model provides physical insight into the circuit behavior. The derived expressions are linearly dependent on the supply voltage and the temperature, and logarithmically dependent on the dimensions of the transistors. Simulation results validated the proposed model, with a maximum error between the analytical and simulated transition points smaller than 14mV. An ASIC in AMS 0.35µm CMOS process has been fabricated to experimentally validate the derived expressions. The maximum error between the analytical and measured transition points is below 36mV.**

Keywords—CMOS, hysteresis, low voltage, Schmitt trigger, subthreshold, weak inversion.

I. INTRODUCTION

The Internet-of-Things paradigm is continuously raising attention both in industry and academia. According to the McKinsey Global Institute the IoT is expected to have an economic impact of $11.1 trillion by 2025 [1], with more than 30 billion units connected. At hardware level, one critical challenge is to optimize the energy efficiency of the implemented electronic devices. Considering, for instance, wireless sensor networks, which are one of the main IoT enabling technologies, the power consumption of the employed devices represents the main limitation in terms of network lifetime [2]. Different solutions have been proposed for optimizing the energy efficiency of these networks [3], [4]. At device level, a widely implemented technique consists into scaling the supply voltage, thus reducing the power consumption of the circuits [5]. When the supply voltage becomes lower than the threshold voltages of the transistors, the latter are said to work in subthreshold region. When this occurs, transistors do not operate in strong inversion, but in weak inversion. This implies that different analytical models have to be used to correctly describe the behavior of the electronic circuits [6]. Both in analog and digital applications, a widely implemented circuit is the Schmitt trigger (ST) one. The symbol of a single input voltage mode ST circuit is shown in Fig. 1(a), while its typical hysteretic characteristic is shown in Fig. 1(b). STs are implemented in comparators, oscillators, converters and many others circuits [7]. Due to the voltage supply scaling trend, many researchers are modeling and employing Schmitt trigger circuits in weak inversion [8]–[14]. In this article we analyze the subthreshold characteristics of the Schmitt trigger circuit proposed by Al-Sarawi in 2002 [15]. The circuit under analysis is a single input inverting CMOS Schmitt trigger, and it is shown in Fig. 1(c). The bulk terminals are not shown for simplicity. The PMOS transistors have the bulk terminals connected to the supply voltage, while the NMOS transistors to the ground. This circuit has not been yet modeled in weak inversion. We have chosen to model the subthreshold characteristics of this circuit because is a low power Schmitt trigger circuit [7]. In this article we derive simple expressions for the high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages, which define the hysteresis of the ST, as can be observed in Fig. 1(b). The derived expressions have been validated with simulations and measurements, by testing a ST circuit fabricated in AMS 0.35µm CMOS process, through EUROPRACTICE MPW.

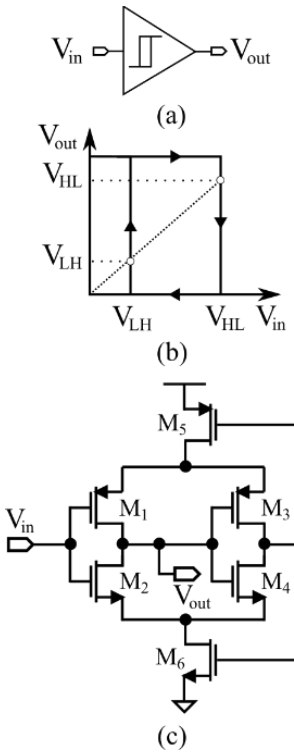

Fig. 1. (a) Schmitt trigger symbol. (b) Typical V_{out} vs V_{in}. (c) Schmitt trigger circuit analyzed in this work.

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The derived mathematical model provides physical insight into the circuit behavior, allowing designers to have a clear understanding of the influence of the involved parameters. The expressions show the relationship between the hysteresis transition voltages and the supply voltage. Furthermore, they also show the dependence on the temperature, through the thermal voltage. The model is derived in Section II, and validated through simulations and experiments in Section III. The conclusions are in Section IV.

II. Analytical Model

In weak inversion, the MOSFET drain current, according to EKV model [16], can be expressed as

$$I_{d,n(p)} = I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}} \cdot \left(e^{-\frac{V_{SB(BS)}}{\phi}} - e^{-\frac{V_{DB(BD)}}{\phi}} \right) \quad (1)$$

$$I_{0,n(p)} = 2 \cdot n_{n(p)} \cdot \mu_{n(p)} \cdot C_{ox} \cdot \frac{W}{L} \cdot \phi^2 \cdot e^{-\frac{|V_{th,n(p)}|}{n_{n(p)}}} \quad (2)$$

where:

- G → gate, D → drain, S → source, B → bulk;
- $n_{n(p)}$ → is the NMOS (PMOS) slope factor;
- ϕ → thermal voltage;
- $\mu_{n(p)}$ → NMOS (PMOS) carrier mobility,
- C_{ox} → oxide capacitance;
- W → MOSFET width;
- L → MOSFET length;
- $V_{th,n(p)}$ → NMOS (PMOS) threshold voltage.

When in saturation ($|V_{DS}| \gtrsim 3 \cdot \phi$ [17]), the drain current expression (1) can be simplified to

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)} - n_{n(p)} \cdot V_{SB(BS)}}{n_{n(p)} \cdot \phi}}. \quad (3)$$

Moreover, if the bulk-source voltage is equal to zero volts, the last equation can be expressed as

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}}. \quad (4)$$

First we show how to derive the high-to-low voltage (V_{HL}), i.e. the input voltage at which V_{out} goes from high to low. According to Fig. 2(a), when the input (V_{in}) is low, V_{out} is high since the ST circuit under analysis is an inverting one. Under these assumptions, M_3 is off, while $M_{1,4,5}$ are conducting. V_{HL} can be then determined by finding the switching voltage of the inverter composed of $M_{1,2}$, with finite voltage $V_{m,n}$ across M_6 [7]. Assuming all transistors in saturation, the equation relating transistors M_1 and M_2 is given by:

$$I_{0,p1} \cdot e^{\frac{V_{dd} - V_{HL}}{n_p \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{HL} - n_n \cdot V_{m,n}}{n_n \cdot \phi}} \quad (5)$$

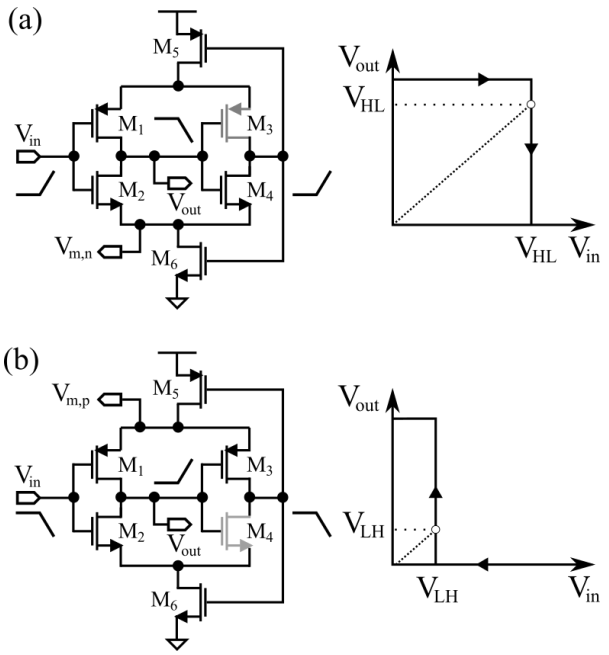

Fig. 2. Schmitt trigger circuits for (a) high-to-low (V_{HL}) and (b) low-to-high (V_{LH}) transition voltages analysis.

where V_{dd} is the supply voltage. As can be observed, the voltage across M_6 ($V_{m,n}$) is unknown in (5). To determine $V_{m,n}$, we can equate the current in M_2 and M_6:

$$I_{0,n6} \cdot e^{\frac{V_{m,n}}{n_n \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{HL} - n_n \cdot V_{m,n}}{n_n \cdot \phi}}, \quad (6)$$

$$V_{m,n} = \frac{V_{HL} + n_n \cdot \phi \cdot log\left(\frac{I_{0,n2}}{I_{0,n6}}\right)}{1 + n_n}. \quad (7)$$

Now that an expression for $V_{m,n}$ is determined, we can substitute (7) in (5), and solve for V_{HL}. The final result is shown in (8).

$$V_{HL} = \frac{n_n \cdot \left\{ V_{dd} \cdot (1 + n_n) - n_p \cdot \phi \cdot \left[log\left(\frac{I_{0,n2}}{I_{0,p1}}\right) + n_n \cdot log\left(\frac{I_{0,n6}}{I_{0,p1}}\right) \right] \right\}}{n_n^2 + n_n + n_p} \quad (8)$$

As can be observed, V_{HL} is linearly dependent on the supply voltage and the thermal voltage. Instead, the dependence on the transistors dimensions is logarithmic. Interestingly, if the ratios $I_{0,n2}/I_{0,p1}$ and $I_{0,n6}/I_{0,p1}$ are equal to one, then V_{HL} would be determined only by the slope factors and the supply voltage. The proposed model is simple, and it does not include the influence of the second inverter, composed of M_3 and M_4, on the high-to-low transition voltage. The derivation of the low-to-high transition voltage (V_{LH}) is complementary, due to the symmetrical configuration of the transistors. Considering Fig. 2(b), when V_{in} is high, V_{out} is low. This results in M_4 off and M_3 on. As for V_{HL}, we can obtain an expression for V_{LH} by initially imposing that:

$$I_{0,p1} \cdot e^{\frac{V_{dd} - V_{LH} - n_p \cdot (V_{dd} - V_{m,p})}{n_p \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{LH}}{n_n \cdot \phi}}. \quad (9)$$

Next $V_{m,p}$ is determined, by equating the currents in M_1 and M_5:

$$I_{0,p1} \cdot e^{\frac{V_{dd}-V_{LH}-n_p\cdot(V_{dd}-V_{m,p})}{n_p\cdot\phi}} = I_{0,p5} \cdot e^{\frac{V_{dd}-V_{m,p}}{n_p\cdot\phi}}, \quad (10)$$

$$V_{m,p} = \frac{V_{LH} + n_p \cdot \left[V_{dd} + \phi \cdot log\left(\frac{I_{0,p5}}{I_{0,p1}}\right)\right]}{1+n_p}. \quad (11)$$

So we substitute (11) in (9), and finally by solving for V_{LH} the expression in (12) is obtained.

$$V_{LH} = \frac{n_n \cdot \left\{V_{dd} - n_p \cdot \phi \cdot \left[n_p \cdot log\left(\frac{I_{0,n2}}{I_{0,p5}}\right) + log\left(\frac{I_{0,n2}}{I_{0,p1}}\right)\right]\right\}}{n_p^2 + n_p + n_n} \quad (12)$$

As for V_{HL}, V_{LH} is linearly dependent on the supply voltage and the thermal voltage. The dependence on the transistors dimensions is logarithmic. V_{HL} depends on M_1, M_2 and M_6. Instead V_{LH} depends on M_1, M_2 and M_5. Designers can use the derived analytical expressions to optimize the design of the Schmitt trigger circuit under analysis. For instance, to make the low-to-high transitition voltage more insensitive to temperature variations, the terms inside the square bracket in (12) should be minimized. This can be done by increasing the size of M_5 and M_1. Instead, for V_{HL} the dependence on the temperature can be minimized by increasing the size of M_1.

III. Model Validation

To validate the proposed model, simulations in AMS 0.35µm CMOS process have been performed. The threshold voltage of the NMOS transistor ($V_{th,n}$) is $515.8mV$, while $V_{th,p} = -731.3mV$. The slope factors are $n_n = 1.25$ and $n_p = 1.3$. The transconductance parameters ($\beta_{n(p)} = \mu_{n(p)} \cdot C_{ox} \cdot W/L$) are $|\beta_{1,5}| = 908\mu A/V^2$ and $\beta_{2,6} = 160\mu A/V^2$. The PMOS transistors are sized 18/1, while the NMOS transistors 1/1. We have chosen these dimensions because this design provides the required hysteresis voltage for further applications. In order to characterize the derived model, we extracted the transition voltages for different supply voltages. The simulated V_{HL} as a function of the supply voltage is shown Fig. 3(a). V_{dd} ranges from $0.5V$ to $0.6V$, therefore all the modeled transistors are in weak inversion since the threshold voltage of the PMOS is greater, in absolute value, than 700mV and the NMOS threshold voltage is approximately 516mV. One can argue that for $V_{dd} > 0.516mV$ the transistor M_2 is not weak inversion. But as can be observed in Fig. 3(b), the resulting voltage at the source of M_2 (i.e. $V_{m,n}$) is greater than $3\cdot\phi \approx 78mV$ at the initial circuit state (i.e. $V_{in} = 0V$). Regarding M_4, it should not have influence on the transition voltage, under the considered assumptions during the model derivation. As can be observed in Fig. 3(a), the model resembles the circuit behavior, and the transition voltage is linearly related to the supply voltage. However an offset can be observed. To quantify the error between the modeled and simulated transition voltages, we define the absolute and relative errors:

$$AE_{HL(LH)} = \left|V_{HL(LH)} - V_{HL(LH),sim}\right|, \quad (13)$$

$$RE_{HL(LH)} = \frac{AE_{HL(LH)}}{V_{HL(LH),sim}} \cdot 100\%. \quad (14)$$

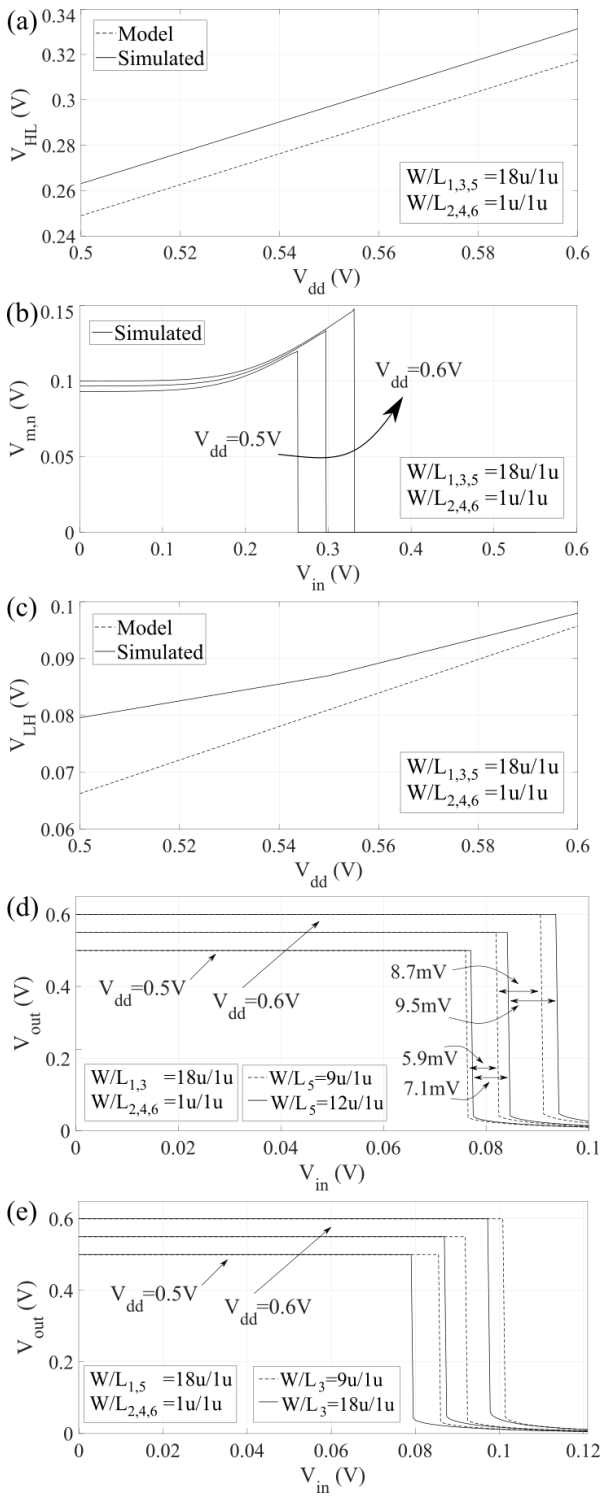

Fig. 3. Modeled and simulated (a) V_{HL} vs V_{dd}. (b) Simulated $V_{m,n}$ vs V_{in} for different V_{dd}. (c) Modeled and simulated V_{LH} vs V_{dd} . (d) Simulated V_{out} vs V_{in} for different V_{dd} and widths of M_5. (e) Simulated V_{out} vs V_{in} for different V_{dd} and widths of M_3.

For V_{HL}, we have that AE_{HL} = $13.9mV$ and RE_{HL} = 7%. Regarding V_{LH}, the simulated and modeled transition voltages as a function of V_{dd} are shown in Fig.3(c). At $V_{dd} = 0.5V$ we have the maximum errors, i.e. AE_{LH} = $13mV$ and RE_{LH} = 17%. As can be observed, for V_{dd} ranging from $0.55V$ to $0.6V$, both

curves are linear, but in the range [$0.5V$−$0.55V$] the simulated curve becomes less linear. This phenomenon has been initially attributed to transistor M_5, as can be observed in Fig.3(d), where the simulated V_{out} vs V_{in} is plotted for different V_{dd} and widths of M_5. The solid line refers to the case in which M_5 has a width of $12u$, while the dashed one to the case in which the width is $9u$. As can be observed, the difference between the curves for $V_{dd} = 0.5V$ and $V_{dd} = 0.55V$ is $7.1mV$, when the width is $12u$. When the width is $9u$ this step reduces to $5.9mV$. When the width is $18u$, the step is $7.4m$V. Instead, the distance between the curves for $V_{dd} = 0.55V$ and $V_{dd} = 0.6V$ is $9.5mV$ when M_5 has a width of $12u$, $8.7mV$ when M_5 has a width of $9u$, and $11mV$ when the width is $18u$. This clearly implies that M_5 has an influence on the transition voltage which is not included in the simple derived model. Moreover, also the inverter composed of M_3 and M_4 has an influence on the characteristics. In Fig.3(e), we can observe how a variation in the width of M_3 causes a variation in the output voltage. It is therefore clear that the assumption that M_3 has no influence on the transition voltage is wrong. Unfortunately, the model at this stage does not include the influence of M_3 on the transition voltages. This represents the main limitation of the simple proposed model. An ASIC in AMS 0.35µm CMOS process has been fabricated through EUROPRACTICE MPW for model validation. A photograph of the circuit and the associated layout are shown in Fig. 4. The circuit occupies an area of $49\mu m \times 25\mu m$. We tested the Schmitt Trigger circuit by applying a $1Hz$ triangular wave at the input, considering $V_{dd} = 0.6V$. For this supply voltage, the analytical $V_{HL,model}$ is $317mV$, while $V_{LH,model} = 96mV$. Instead the measured values are $V_{HL,meas} = 329mV$ and $V_{LH,meas} = 131mV$. Therefore the errors between the modeled and measured transition voltages are $AE_{HL,meas} = 12mV$ and $AE_{LH,meas} = 35mV$. The larger errors in the measured transition voltages are mainly attributed to parasitic effects.

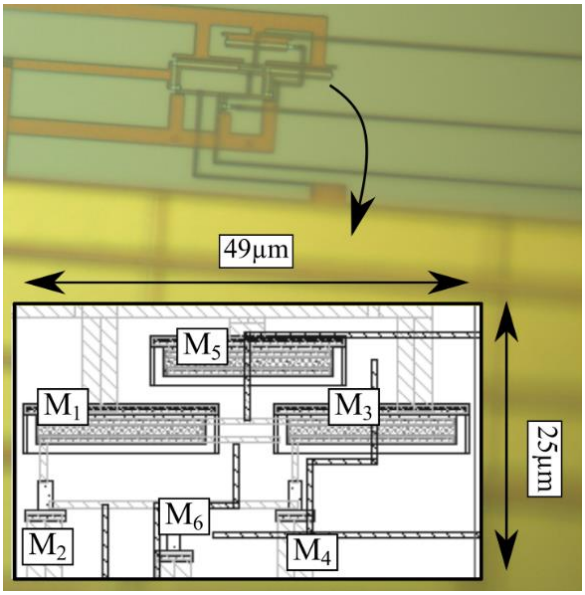

Fig. 4. Photograph of the fabricated circuit in AMS 0.35µm CMOS process (EUROPRACTICE MPW) and associated layout.

IV. Conclusions

In this article we analyzed the subthreshold characteristics of an inverting CMOS Schmitt Trigger circuit. We derived simple equations for the high-to-low and low-to-high transition voltages. The derived expressions are linearly dependent on the supply voltage and the thermal voltage, and logarithmically dependent on the transistors dimensions. The model allows designers to have a clear understanding of the influence of the involved parameters. For instance it allows to optimize the design of the Schmitt trigger circuit against power supply and temperature variations. We performed simulations in AMS 0.35µm CMOS process to verify the proposed analytical model. The maximum error between the analytical and simulated transition points is smaller than 14mV. An ASIC in AMS 0.35µm CMOS process has been fabricated to experimentally validate the derived expressions. The maximum error between the analytical and measured transition points is below 36mV. Future work will focus on model improvement.

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