# An Oscillator-Based Wake-Up Receiver for Wireless Sensor Networks

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# An Oscillator-Based Wake-Up Receiver for Wireless Sensor Networks

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***Abstract*—The Internet of Things (IoT) concept is mainly enabled by wireless sensor networks (WSNs), which are continuously gaining attention, due to their multidisciplinary applications. To enhance the WSNs energy efficiency, different solutions have been proposed. One of them is the integration of wake-up receivers (WuRxs), which activate the sensor nodes through an identity-based approach. In this work a low power oscillator-based WuRx architecture is presented, and verified by simulations in TSMC-180nm CMOS process. The WuRx sequentially verifies if the received signal resembles the wake-up call (WuC) one by means of oscillators, counters and logic gates. It consumes 16.1µW when detecting a 1.6ms WuC signal, and 1.2nW in idle mode.**

***Keywords*—Logic circuits, low-power electronics, oscillators, receivers, wireless sensor networks.**

## I. Introduction

The Internet of Things (IoT) paradigm is continuously raising attention both in academia and industry: by the end of 2026, the number of IoT connections is expected to be about 26.9 billion [1]. One of the main IoT enabling technologies is the wireless sensor network (WSN) one, which refers to a group of wirelessly connected sensor nodes [2]. The latter are able to collect, elaborate, and transmit signals, and are typically battery-powered. The sensor node power management is critically important, since it determines the WSN energy efficiency and lifetime. The latter can be increased by optimizing the network power consumption, implementing energy harvesting techniques, and employing backscatter networks [3]. A largely employed energy-saving protocol is the duty-cycled Medium Access Control (MAC) one, which consists in turning on/off the sensor nodes during specific time windows. Such a protocol intrinsically suffers from idle listening (sensor nodes are on even if no access is required) and overhearing (a sensor node receives a message not intended to it). These issues could be solved by integrating wake-up receivers (WuRxs), which wake up the sensor nodes from sleep mode only when the wake-up call (WuC) signal is received (Fig. 1) [4]. This implies that the sensor nodes are on only when required, resulting in an energy efficient solution [5]. WuRxs can be RF based or non-RF based, depending on the application. Most of the reported WuRxs are RF based [6]–[10], but also optical [11]–[14] and acoustic receivers have been proposed [15]–[21]. In this work a low power oscillator-based WuRx concept is proposed. The architecture block diagram is described in section II. A circuit implementation is presented in section III. The simulations results are in section IV, while the conclusions are in section V.

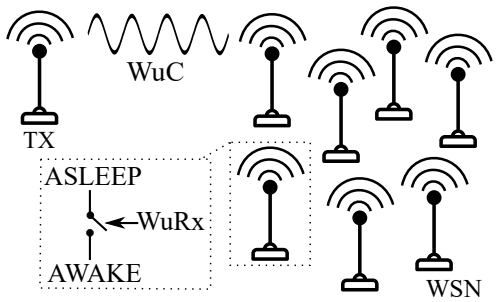


Fig. 1. A wireless sensor network integrating WuRxs.

## II. Architecture

The proposed architecture is shown in Fig. 2. The transmitter sends the WuC signal ($S_{WuC}$), which typically consists of sinusoidal bursts. The burst duration establishes the number of high states ('1's) associated to that burst, while the time interval between two bursts establishes the number of low states ('0's) associated to that time interval. The amplitude of $S_{WuC}$ is typically affected by losses (e.g. attenuation) during the transmission. Therefore the amplitude of the received signal ($S_{in}$) could be increased through a step-up transformer ($S_{up}$). Next this signal is rectified ($S_{rect}$), and sent into the pulse extractor. The latter generates $N$ square waves (e.g. $S_{1,2,3}$ in Fig. 2), with duration equal to that of the received '0's and '1's. After the extraction, the first pulse ($S_1$) is sent into the first pulse meter ($P_1$), which is composed of a switch, an oscillator, two counters and a one shot monostable. The pulse meters verify if the received signal ($S_{in}$) resembles the wake-up call one: the oscillators, in conjunction with the counters, measure the duration of the extracted pulses. The verification process is sequential, i.e. if the duration of the first extracted pulse does not resemble the first state of the WuC signal, the successive pulse meters are not enabled. To explain the WuRx operation, suppose that the WuC signal is a sequence of $N = 3$ states (e.g. '101'), and that $M$ oscillations are associated to the correct detection of each state. Assume also that the switches $sw_{1,2,3}$ are all initially closed, and that all the counters are divide-by-$M$ counters. Considering the first pulse meter, at the oscillator 1 output three cases can be distinguished:

- case 1: there are less than $M$ oscillations;
- case 2: there are more than $M$ oscillations;

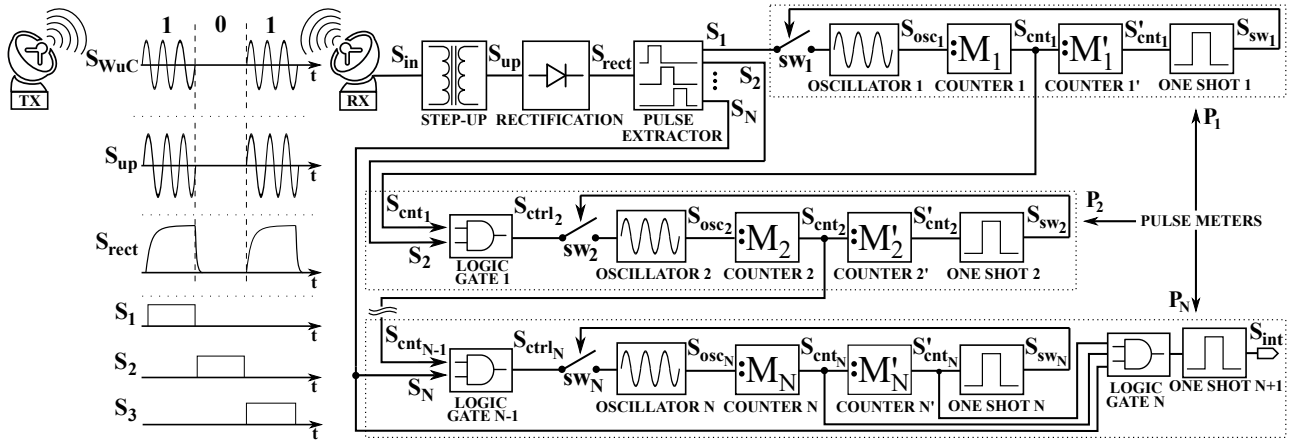


Fig. 2. Oscillator-based wake-up receiver architecture.

- case 3: there are exactly $M$ oscillations.

In case 1, the oscillator 1 output ($S_{osc_1}$) has less than $M$ oscillations. Consequently both the counters and one shot 1 are off. The output of counter 1 ($S_{cnt_1}$) goes, together with the second extracted pulse ($S_2$), into logic gate 1. Since counter 1 is off, the logic gate 1 output ($S_{ctrl_2}$), which is the control signal of oscillator 2, is not asserted. Hence the second pulse meter ($P_2$) is not enabled. In case 2, there are more than $M$ oscillations at the counter 1 input. Therefore also the counter $1'$ output ($S'_{cnt_1}$) is asserted. The latter activates one shot 1, which opens the switch $sw_1$. Counter $1'$ and one shot 1 are used to avoid extra oscillations, thus minimizing the power consumption. In case 3, the counter 1 output is asserted, since exactly $M$ oscillations are present at its input, while counter $1'$ and one shot 1 are off. As a consequence logic gate 1 will let $S_2$ reach the second oscillator, thus enabling $P_2$. The control signal ($S_{ctrl_2}$) coincides with the second pulse ($S_2$) only if exactly $M$ oscillations are detected. As before, oscillator 2, in conjunction with the counters and one shot 2, verifies if $S_2$ resembles the WuC signal. If this is the case, logic gate 2 will let $S_3$ reach the last oscillator. If the last state is correct (i.e. $S_3$ causes $M$ oscillations), the logic gate 3 output will be asserted, and one shot 4 will finally generate the wake-up interrupt signal ($S_{int}$), which activates the sensor node. For an $N$ states WuC signal, the proposed architecture has: $N$ switches, oscillators, and logic gates, $2N$ counters and $N+1$ one shots. All the pulse meters have a logic gate at their input, except the first one ($P_1$), which is by default enabled. The last pulse meter ($P_N$) has an additional logic gate and one shot for interrupt signal generation.

## III. Circuit Implementation

In this section the circuit implementation of an oscillator-based WuRx with $M = 2$ is proposed. A Delon voltage doubler, shown in Fig. 3(a), is implemented to step up ($V_{up}$) and rectify ($V'_{rect}$) the received input voltage ($V_{in}$) [22]. The resistor ($R$) is used to discharge $V'_{rect}$, which is then buffered. The buffer output ($V_{rect}$) is sent into the pulse extractor. The latter is designed according to the predefined WuC signal.

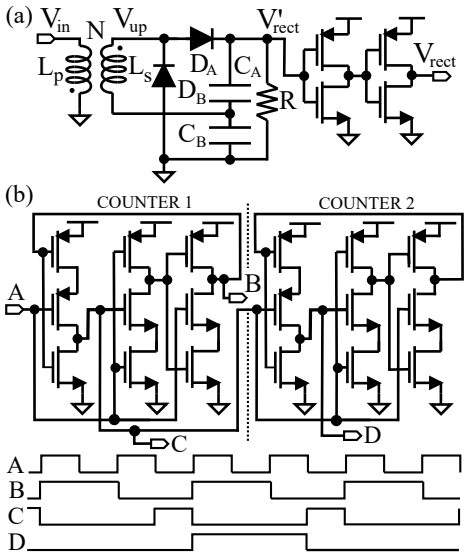


Fig. 3. (a) Delon voltage doubler. (b) Cascade of divide-by-two counters.

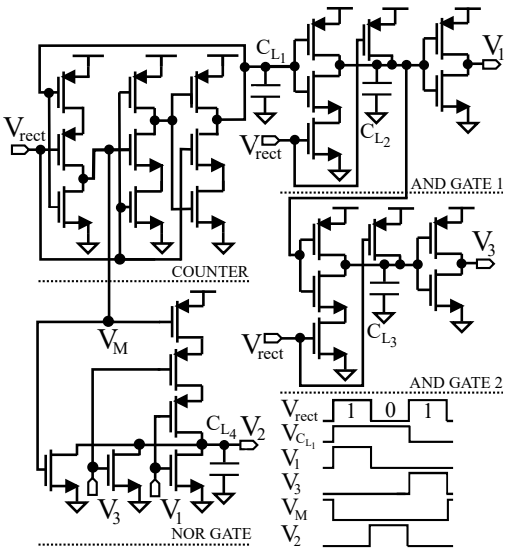


Fig. 4. Circuit implementation of a '101' pulse extractor.

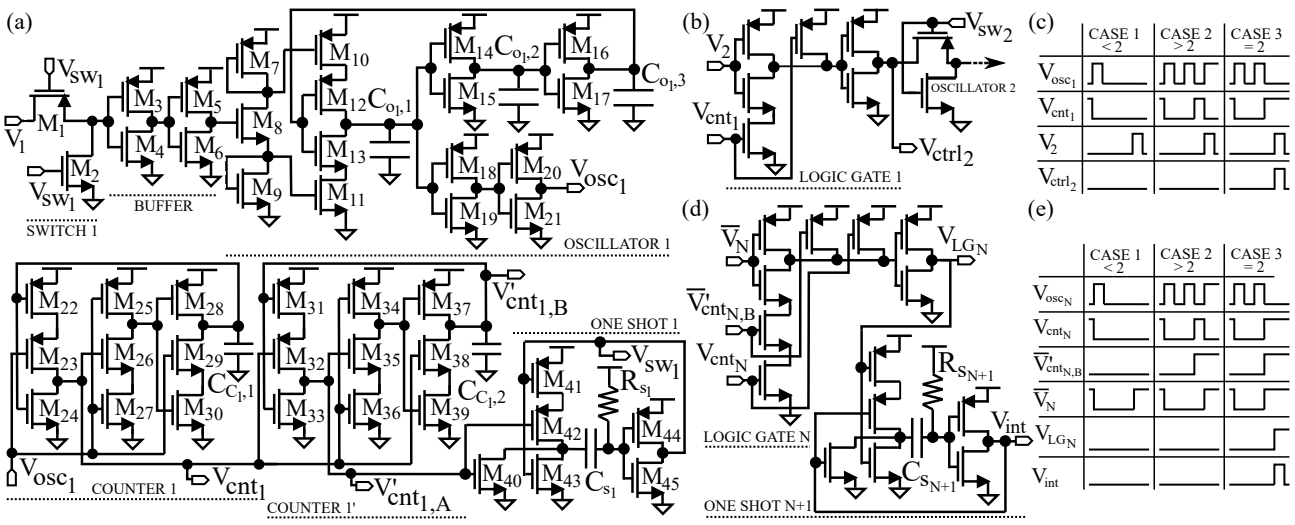


Fig. 5. (a) Pulse meter 1 ($P_1$). (b) Logic gate 1 and (c) its waveforms. (d) Logic gate $N$ and (e) its waveforms.

A possible approach consists into using logic gates, and the CMOS counter shown in Fig. 3(b) [23]. A '101' pulse extractor implementation is shown in Fig. 4. The counter has two outputs: $V_{C_{L_1}}$ and $V_M$, i.e. signals $B$ and $C$ in Fig. 3(b). The first pulse ($V_1$) could be extracted through the AND logical operation $V_{C_{L_1}} \cdot V_{rect}$. The third pulse ($V_3$) could be obtained through the AND logical operation $\overline{V_1} \cdot V_{rect}$, where $\overline{V_1}$ is the inverted first pulse. The pulse associated to the state '0' could be obtained by using the NOR logical operation $\overline{V_M + V_1 + V_3}$. Longer WuCs could be extracted by simply implementing more counters and logic gates. After the extraction process, the first pulse is sent into the first pulse meter ($P_1$), shown in Fig. 5(a). Transistors $M_{1-2}$ implement the switch $sw_1$ in Fig. 2, while transistors $M_{3-6}$ implement a buffer. Oscillator 1 ($M_{7-21}$) is implemented as a current starved ring oscillator with output-switching [24]. Counter 1 ($M_{22-30}$) and 1′ ($M_{31-39}$) are divide-by-two counters (Fig. 3(b)), while the transistors $M_{40-45}$, the resistor $R_{S_1}$ and the capacitor $C_{S_1}$ implement one shot 1 [25]. The adopted counter topology implies that the extracted pulse has to cause two oscillations (i.e. $M = 2$) for a correct pulse detection. If more oscillations are detected, the output of counter 1′ ($V'_{cnt_1,A}$) will be asserted. Consequently one shot 1 will be triggered, and its output ($V_{sw_1}$) will disconnect, trough $M_{1-2}$, oscillator 1 from the pulse extractor. According to Fig. 2, the counter 1 output goes, together with the second extracted pulse, into logic gate 1, which is implemented as an AND gate (Fig. 5(b)). The latter is present at the input of all the pulse meters, except the first one, which is by default enabled (Fig. 5(a)). As shown in Fig. 5(c), the logic gate 1 output ($V_{ctrl_2}$) is asserted only if exactly two oscillations are detected by counter 1. Other input combinations lead to zero volts. The last pulse meter ($P_N$) is the one that asserts the wake-up interrupt voltage ($V_{int}$). As compared to the other pulse meters, it presents an additional logic gate and one shot, shown in Fig. 5(d). The interrupt signal is asserted only if the last pulse ($V_N$) causes two oscillations. Logic gate $N$ receives also the inverted last pulse ($\overline{V_N}$) in order to not trigger the one shot $N+1$ when case 2 happens.

## IV. Simulation Results

To verify the proposed architecture, a WuRx with $N = 3$ states has been simulated in TSMC-180nm CMOS process. The simulation parameters are in Table 1. The input, stepped up and rectified voltages are shown in Fig. 6(a). The WuC signal is '101', with each burst having a frequency of $100kHz$ and a duration of $0.5ms$. WuRxs working with frequencies ranging from $20kHz$ to $100kHz$ are typically acoustic ones. A burst with higher frequency would imply different Delon voltage doubler components, as well as a different oscillator design. The supply voltage ($V_{DD}$) is $1.2V$, and the inverters are sized with symmetric switching point around $V_{DD}/2$. The logic gates transistors are sized with unit width and length. The oscillator bias stage is sized in order to oscillate $M = 2$ times for each state. All the one shots resistors are implemented through a cascade of two diode-connected PMOS with minimum width and length. A buffer has been added to the last one shot. The simulations results validated the proposed concept. Considering $P_1$, when $V_1$ is longer than expected, more than two oscillations ($V_{osc_1}$) are observed (Fig. 6(b)). So the counter

Table 1. Circuit simulation parameters.

| Component | Parameter | Value |
|---|---|---|
| Voltage Doubler | $L_{p,s}$ | $4\mu H$,$400\mu H$ |
| | $C_{A,B}$ | $200nF$ |
| | $R$ | $500\Omega$ |
| Pulse Extractor | $C_{L,1,2,3,4}$ | $5pF, 1pF, 15pF, 1pF$ |
| Pulse Meter 1 | $C_{o_1,1,2,3}$ | $180pF$,$520pF$,$1.8nF$ |
| | $C_{C_1,1,2}$ | $5pF, 1pF$ |
| | $C_{s_1}$ | $3pF$ |
| Pulse Meter 2 | $C_{o_2,1,2,3}$ | $100pF$,$570pF$,$2.1nF$ |
| | $C_{C_2,1,2}$ | $5pF, 1pF$ |
| | $C_{s_2}$ | $3pF$ |
| Pulse Meter 3 | $C_{o_3,1,2,3}$ | $320pF$,$550pF$,$900pF$ |
| | $C_{C_3,1,2}$ | $5pF, 1pF$ |
| | $C_{s_{3,4}}$ | $3pF, 3.4pF$ |

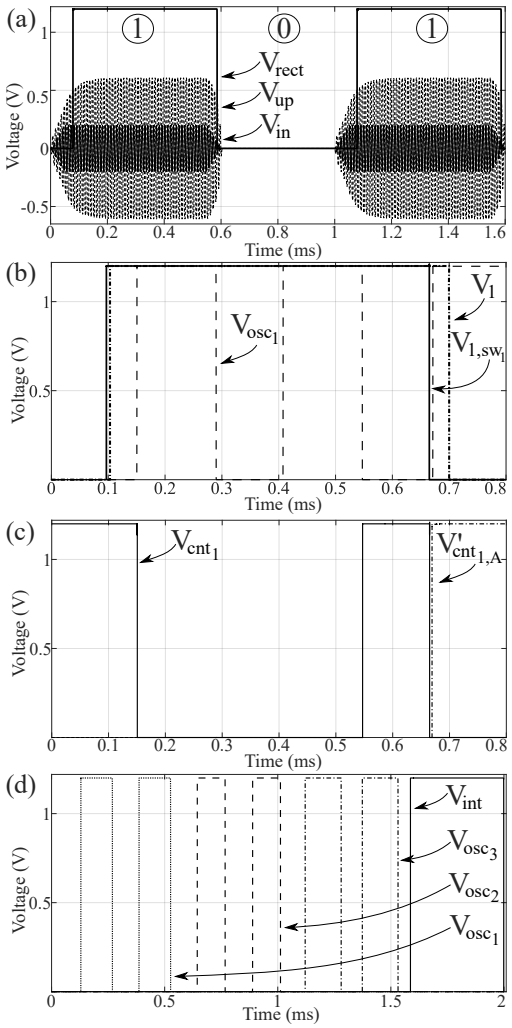


Fig. 6. (a) $V_{in}$, $V_{up}$ and $V_{rect}$. (b) $V_{osc_1}$, $V_1$ and $V_{1,sw_1}$ (case 2). (c) $V_{cnt_1}$ and $V'_{cnt_{1,A}}$(case 2). (d) $V_{osc_{1,2,3}}$ and $V_{int}$ (case 3).

$1'$ output ($V'_{cnt_{1,A}}$) goes high, as shown in Fig. 6(c). As a consequence the one shot 1 opens switch $sw_1$, and the resulting voltage ($V_{1,sw_1}$) after the switch is shorter, thus preventing extra oscillations, and so higher power consumption. If all the extracted pulses cause two oscillations per pulse meter, finally the interrupt voltage ($V_{int}$) is generated (Fig. 6(d)). The duration of $V_{int}$ is set by the $RC$ group of one shot 4, and is application dependent. In active mode (i.e. when detecting the $1.6ms$ WuC signal), the WuRx consumes $13.4\mu A$, at which corresponds an average power consumption of $16.1\mu W$. In idle mode (i.e. $V_{in} = 0V$), the WuRx consumers $1nA$, at which corresponds an average power consumption of $1.2nW$. The power consumption in the active mode is dependent on the complexity of the WuC signal and on the adopted counter topology. A longer WuC signal would imply more pulse meters, while a higher measurement precision would require more counters per pulse meter. A comparison with other WuRxs working in the same frequency range is reported in Table 2. The proposed circuit implementation is low power in active mode, and ultra-low power in idle mode.

Table 2. Power consumption comparison.

| $\mathbf{P_{idle}}$ | $\mathbf{P_{active}}$ | $\mathbf{f_{input}}$ | $\mathbf{V_{dd}}$ | **Work** |
|---|---|---|---|---|
| $1.2nW$ | $16.1\mu W$ | $100kHz$ | $1.2V$ | This |
| $3\mu W$ | $8.1\mu W$ | $85kHz$ | $3.3V$ | [18] |
| $1.64\mu W$ | $14\mu W$ | $40kHz$ | $2V$ | [17] |
| – | $4\mu W$ | $43kHz$ | $0.6V$ | [15] |
| $45\mu W$ | $420\mu W$ | $20kHz$ | $3V$ | [19] |

## V. Conclusions

In this work an oscillator-based wake-up receiver concept for wireless sensor networks is proposed. The WuRx extracts pulses associated to the duration of the received states. So it uses oscillators in conjunction with counters and logic gates to sequentially verify if the received signal resembles the WuC signal. The WuRx is able to manage cases in which the pulse measurement is not correct, avoiding unnecessary power consumption. Simulations in TSMC-180nm CMOS process verified the architecture. For the detection of a $1.6ms$ WuC signal it consumes $16.1\mu W$, while in idle mode only $1.2nW$. Future research directions will focus on power consumption optimization and experimental validation.

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