Thinning and readout during bending of a custom silicon IC

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***Abstract*— This contribution presents a solution on how to interconnect, thin and bend a monolithic integrated circuit (IC) for use in the Inner Tracker System v3 (ITS3) of the ALICE experiment at the European Organization for Nuclear Research (CERN). Verification of the system operations was done by building a dedicated readout system. The technology is demonstrated by thinning a 30 mm x 15 mm x 130 µm monolithic active pixel sensor to 45 µm and curving the chip to a radius of 20 mm while monitoring the internal registers and current consumption.**

Keywords—ALPIDE, DRIE, Si, IC, bending, thinning

I. Introduction

The ALICE (A Large Ion Collider Experiment) detector is designed to track particles generated from proton–proton, proton–nucleus and nucleus–nucleus collisions at the CERN LHC to explore the physics of strongly interacting matter, and in particular the properties of the Quark-Gluon Plasma [1]. The Inner Tracking System version two (ITS2) of ALICE consists of seven sensor layers that are concentric arranged in a cylindrical formation with radial coverage from 22 mm to 400 mm with z-lengths ranging from 27 cm to 1.5 m, covering about 10m^2 with ≈ 12.5 billion pixels. The ALICE Pixel Detector (ALPIDE) [2] is a Monolithic Active Pixel Sensors (MAPS) designed for the ITS2. The ALPIDE pixel cells (Figure 1) can detect charged particles crossing its epitaxial layer. The crossing will be registered by the sensor as a hit that is to be combined with hits from other sensors in the concentric cylindrical sensor array where particle tracking algorithms is applied to extract the 3D path of the moving particle. The ALPIDEs for the ITS2 are produced with a thickness of 50µm and 100µm. Using a low material budget for the first detection layer of the ITS is particularly important for the impact parameter resolution[1]. The ALPIDE chips in layer 0 to 2 has 50µm thickness, while the chips in layer 3 to 6 has a thickness of 100µm. The overall minimal thickness of the ALPIDE is determined by the height of the epitaxial layer (nominal value 18 µm) plus the CMOS stack height (≈ 10 µm).

Reducing the overall material budget by thinning the substrate of the ALPIDE and bending the chip will allow the tracking performance and momentum resolution to be improved compared to the ITS2, but it increases the complexity of manufacturing and handling of the chips[3].

This study describes how to test, transform and assemble a 130 µm ALPIDE to 45µm ALPIDE curved to a radius of 20mm. The main challenges addressed, was how to minimize the crystallographic defects introduced during DRIE thinning and how to suppress the shock effects during assembly, handling and bending. The findings in this article will contribute to future development and production of an upgraded ITS3 as proposed in the "Letter of Intent for an ALICE ITS Upgrade in LS3" [4].

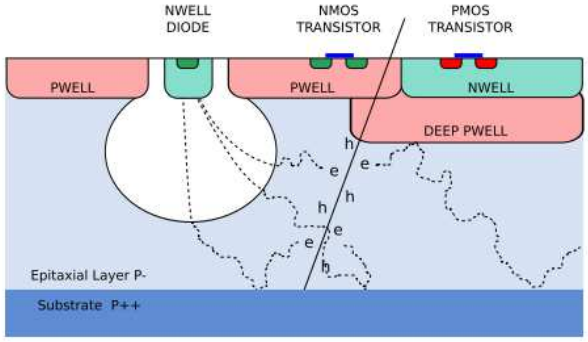

Figure 1 Schematic cross section of a MAPS pixel [1]

II. ALPIDE Bending

The ALPIDE measures 15 mm x 30 mm and mostly consist of silicon with a ≈ 10 µm CMOS and insulation layer on top. The silicon layer is the most brittle part and the one most likely to fracture when the chip is about to be bent. A practical test by bending a 130 µm ALPIDE to a radius of 20mm resulted in fractures as verified by similar experiments [5] on Si chips.

Reducing the thickness of a silicon chip increases the amount of curving that is possible without breaking the chip. Bending of a silicon chip, will generate both compressive and tensile stress [6]. Reducing the curving radius by bending the chip, will gradually increase the tensile stress until it reaches 7.0 GPa (silicone's tensile yield strength) [4], and the chip will fracture. The minimum radius of curvature R for a curved piece before fracture can be expressed as:

$$R = E\frac{d}{2S} \quad (1)$$

where E is the young modulus of elasticity from 168GPa to 130GPa depending of the crystal direction [7], d is the silicon thickness and S is the maximum tensile yield strength (7.0 GPa [3]). The practical bending radius of Si chips is considerably larger than the theoretical limit [5], due to irregularities in the edges and surfaces.

III. Thinning Process

Silicon Deep Reactive Ion Etching (DRIE) was selected in this study to ensure high chip strength and limit accidental fractures during handling, assembly and bending of the ALPIDE. Thinning by mechanical grinding might be the most cost-effective method[8], but plasma etching will create smaller irregularities in the chips surfaces than what could be achieved by grinding or polishing. Irregularities induced in the chips surface would weaken the silicon strength [9], while reducing the minimum curving radius causing fracture.

For this study, the ALPIDE thickness was selected to 45µm, a value close to the minimum, while leaving a safety margin, to reduce the risk of fractures during handling. The minimum thickness for a functioning ALPIDE curved to a radius of 20mm, would be ≈ 30 µm (epitaxial layer plus CMOS stack height), while the maximum size is expected to be the range of 55-110µm (from other conducted experiment [5]).

This study used 130µm thick ALPIDE chips with a polished surface and a 9µm top insulation layer. It was prepared for DRIE by placing the topside on a Si wafer prepared with a small droplet of Polyphenyl Ether (PPE) [Santovac 5]. The PPE protects the topside from being etched and fixes the chip to the Si wafer. The correct amount of applied solution provides sharp edges and protects the top side of the ALPIDE.

It was discovered that DRIE processing with insufficient amount of PPE would lead to damages of the chips top surface (Figure 2(a)) and curves edges. (Figure 2(b))

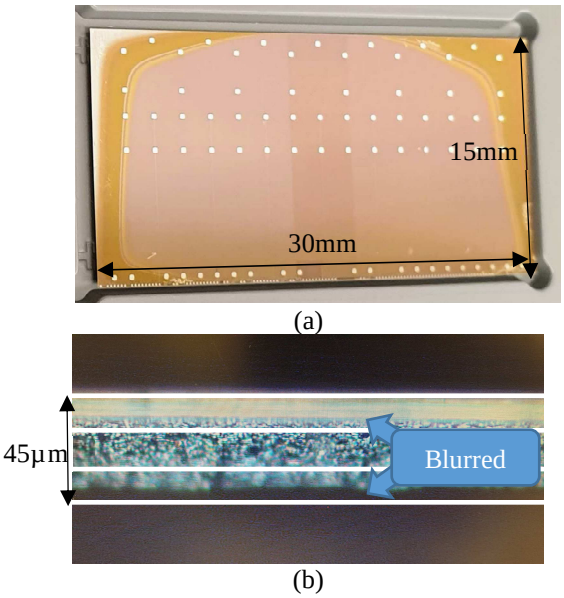

Figure 2 Top Etched chip: (a) Top of ALPIDE; (b) Edges

Traces of dried PPE near the edges (Figure 3(a)), is a visible result of DRIE processing with an excessive amount of PPE. The chip edges that has been in contact with PPE, will be damaged (Figure 3(b)). Damages of the edges would reduce the chip strength and make the chip more vulnerable to fractures and increases the minimum chip bend radius before fracturing.

Correct amount of applied PPE, ensures DRIE processing of only the ALPIDE substrate, leaving the edges sharp and square (Figure 4).

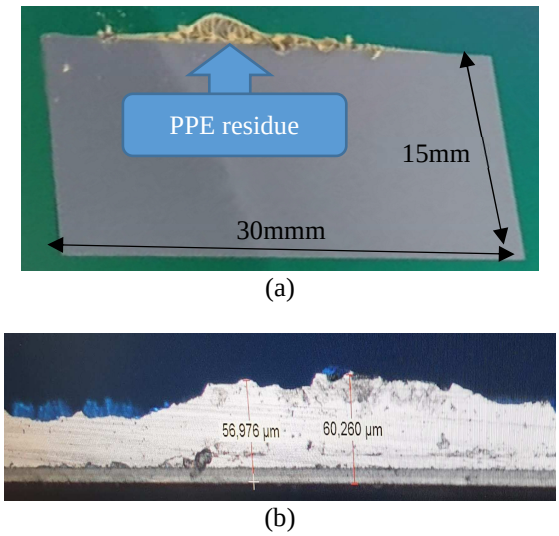

Figure 3 ALPIDE after DRIE: (a) ALPIDE mounted on wafer; (b)ALPIDE edge covered with PPE

Figure 4 ALPIDE after ALPIDE edge with no excess PPE

IV. Chip bending test

The verification of successfully curving a 45µm thick ALPIDE to a radius of 20mm without not producing brittle fractures was necessary before proceeding to functional testing of the ALPIDE. The length, width and unique CMOS layer of the ALPIDE differs from tests that has been conducted by others [5][10][11]. To ease the handling and protect the ALPIDE from accidental twisting (easily induces brittle fractures), the following method was developed:

A. *Placing the ALPIDE chip on a frame of dicing tape [ELP UE-11] (Figure 5 (a)).*

B. *Adding a PLA frame (Figure 5 (b)) around the on ALPIDE (Figure 5 (c)).*

C. *Removing excessive tape around PLA frame.*

Verification of curving the ALPIDE to a radius of 20mm without suffering brittle fractures, was done by curving the tape frame containing the ALPIDE round a polished steel cylinder with a radius of 20mm (Figure 5 (d)). The ALPIDE was flexed and curved several times before it was optically inspected for fractures. The inspecting showed no visible fractures. The successfull curving of the ALPIDE enables further investigation on how curving will affect the CMOS logic.

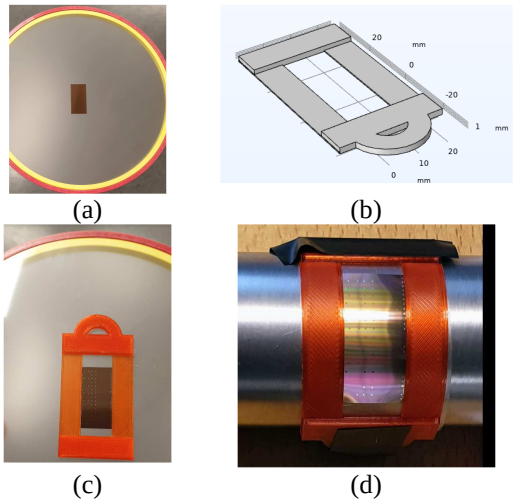

Figure 5 Chip bend test preparation: (a) ALPIDE frame; (b) ALPIDE mounted on tape frame; (c) ALPIDE and frame taped; (d) ALPIDE and small frame bend on cylinder (r=20mm)

V. Chip Interfacing

The ALPIDE was interfaced to the readout electronics using a custom-made Flexible Printed Circuit Board (FPCB). The FPCB provides flexibility, twistability and low mass while enabling wire bonding to the ALPIDE via exposed gold pads. On the other end, the FPCB connects to the readout system using an FPC (Flexible printed cable) connector.

The FPCB and ALPIDE were aligned and mounted on a frame of dicing tape [ELP UE-11], where the bonding was done using 25µm gold wires between the FPCB and ALPIDE. The tape membrane was fixed to the bonding machine using vacuum, to avoid poor bonding strength and possible damages to the ALPIDE chip. After bonding, a smaller frame was connected to the tape and the new frame and circuit was cut out of the tape (Figure 6).

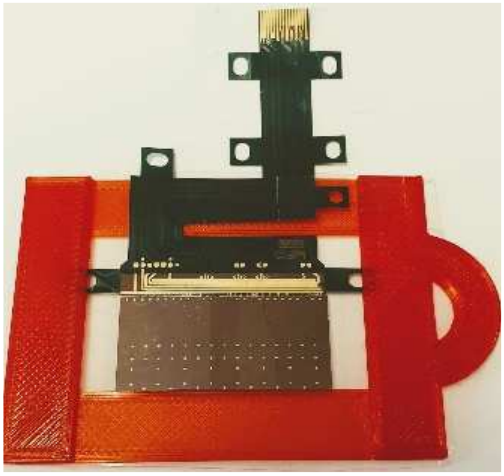

Figure 6 Flex ALPIDE Interface

VI. Readout System

The ALPIDE readout system shown in Figure 7 was designed to verify the functioning of the ALPIDE when it was curved and flexed. The input voltage and the total current consumption of the ALPIDE was monitored using two FLUKE 45 Multimeters. Monitoring the current is used to observe changes in the current when the chip is curved due to changes in the transistors geometry and mobility [6] and to identify possible errors. If the electrical current consumption of the ALPIDE operating in idle mode, deviates from the expected value, we would be able to determine if the circuit is broken or that there is an error in the wiring to the power supply or missing grounding of the substrate.

The ALPIDE is controlled by a microcontroller module (Arduino Nano[12]) that communicates with a computer where ALPIDE data is timestamped and stored.

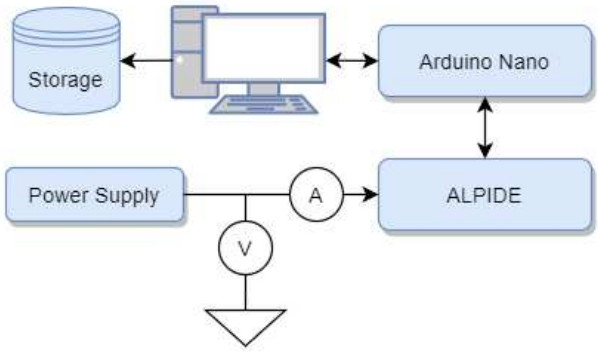

Figure 7 ALPIDE readout system

A. *ALPIDE error detection inside the digital logic*

The Arduino microcontroller module will at startup overwrite the default ALPIDE_VCASN2 register value (from 0x0040 to 0x0039). Every second the microcontroller forwards the ALPIDE_VCASN2 the result to a computer that stores the current Coordinated Universal Time (UTC) value together with the received ALPIDE_VCASN2 value formatted as comma-separated values (CSV) file. If the register value field is changed from 0x0039 an error is detected. If the value is equal to the ALPIDE_VCASN2 default value (0x0040) the ALPIDE has experienced a reset. Receiving any other values would indicate a communication failure with the microcontroller.

B. *Electronic interfacing*

The microcontroller module Arduino Nano V2.8 [12] was selected as a readily available and low-cost interface between the ALPIDE and the computer to test the basic ALPIDE functions.

The microcontroller ATmega328[13], used in Arduino Nano module uses a 16MHz ±20ppm crystal oscillator as its system clock that limits the I/O speed. Verification of the basic ALPIDE operation does not require the same high speed I/O device used under normal data taking operation at CERN. The built-in “Control Port” of the ALPIDE is a synchronous serial interface that enables read/write access to the ALPIDE memories and registers as well as executing commands. In this readout system the “Control Port” is used to configure and verify the basic operations of the ALPIDE.

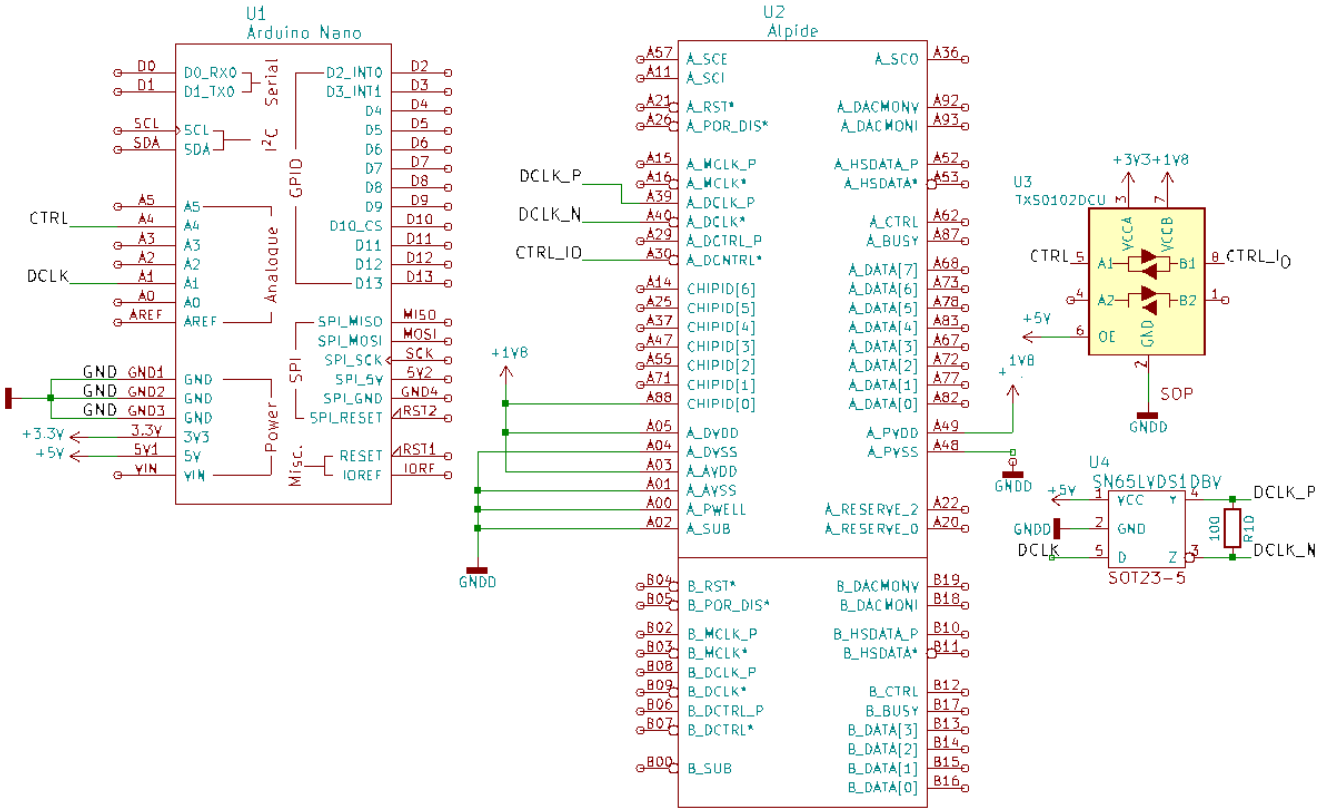

Figure 8 Schematic view of the ALPIDE readout system

The serial interface of the ALPIDE conforms to the TIA/EIA- 899 Electrical standard for Multipoint-Low-Voltage Differential Signaling (M-LVDS) and needs to be interfaced to the TTL level used by the Arduino Nano's I/O pins. The interfacing between the ALPIDE and Arduino Nano is shown in the schematics in Figure 8.

The data control signal DCRTL, is bidirectionally voltage-level translated between the ALPIDE (1.8V) and the Arduino nano (5V) using TXS0102DCU [14]. The system clock signal (DCLK) is translated from the Arduino single 5V TTL output to a differential 1.8V output, using the differential line drivers SN65LVDS1DBV[14]

VII. Results

It was confirmed that DRIE processing of a 130 µm thick ALPIDE to 45µm, was able to survive repeated curving to a radius of 20mm.

The readout system verified that the digital logic of the ALPIDE was not affected by repeated bending. The readout system tested the ALPIDE continuously every second for 48 hours when curved to a radius of 20mm and 48 hours flat without detecting any error of reading the ALPIDE_VCASN2 register.

The total current consumption of the ALPIDE operating at 1.80V in idle mode, was observed to change from 22.6mA to 23.3mA. It was expected that the current consumption of the ALPIDE would change with different curvatures, due to geometric changes in the gate oxide layer, interface effects and mobility [10]. The digital processing inside the ALPIDE was not affected by the electrical changes due to bending, but further investigation on the effects of the analog circuits should be conducted. The increased power consumption of 3% should not be of any major concern. The ALPIDE has been curved more than 50 times without any change to total current consumption or errors observed in the digital logic.

VIII. Conclusions

This study shows that repeated flexing and bending of a 30mm x 15mm x 45µm ALPIDE to a minimum radius of 20mm did not influence the chip's digital logic. The importance of proper application of Polyphenyl Ether to the top-layer of ALPIDE before tinning using DRIE was explored. An assembly technique for mounting the ALPIDE to a flexible/stretchable substrate together with a custom-FPCB was developed, and a low-cost readout system was developed to verify the digital logic when curving the ALPIDE.

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