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Characterization of high-precision resistive voltage divider and buffer amplifier for ac voltage metrology

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Abstract. A high-precision voltage buffer and a 10:1 resistive voltage divider have been constructed for use in ac voltage and electrical power metrology. Long-term stability of the buffer's dc response has been demonstrated by two dc sweeps performed 20 days apart, with best-fit linearized gain varying less than 1 μV/V. The absolute ac gain has been measured using a high-precision digital multimeter for 10 Hz and 1 kHz with results consistent with dc within 5 μV/V. This value agrees with the characterization of ac–dc difference using thermal converters from different producers with a variety of resistance for various voltages from 1 V to 5 V. The ac–dc difference was further characterized better than 40 μV/V for the same voltages up to 100 kHz and better than 100 μV/V for 3 V at 1 MHz. Absolute ac gain and ac–dc difference has also been measured for the voltage divider and buffer combination from 10 V to 50 V, with similar agreement up to 1 kHz. The ac–dc difference from 10 Hz to 100 kHz of this combination shows an agreement well within 30 μV/V in this entire voltage span with a total response not exceeding 125 μV/V. This make the voltage divider and buffer combination suitable for sampling electrical powers for a wide range of voltages.

Keywords: ac voltage metrology / traceability / voltage buffer / resistive voltage divider

1 Introduction

Today's developments within the electronics industry have greatly advanced the performance of analogue-to-digital and digital-to-analogue converters in terms of speed, resolution, accuracy and power consumption. Consequently, the accuracy requirements for the calibration of these instruments have become even greater. This has driven the need to improve both measurement standards and methods of traceability transfer, so that more accurate calibrations can be delivered.

Although extensive efforts have been made to push pulse-driven Josephson setups to synthesize ac voltages beyond 1 V [1–3], standards and techniques to transfer the traceability are also needed to perform more accurate calibrations. In practice, more convenient instruments, such as thermal converters (TCs), and digital multimeters (DMMs), such as Fluke 5790A and Keysight 3458A, are used to perform every-day calibrations. The most precise of these are the TCs, which transfer traceability from dc to ac, by making a thermal comparison between applied ac and dc voltage (or current). These have long been the preferred standards for ac voltage, where voltages up to 1000 V can be traced by coupling the TC in series with range resistors (RRs).

In a similar manner, a voltage divider and voltage buffer combination can be used to extend the traceability range. Whereas a RR serves as current limiter for the TC, a voltage divider has a given division ratio, which it applies to the input voltage. Consequently, a divider and buffer combination can be used to extend the traceability range for a much wider range of instruments.

Good examples of previously constructed voltage buffers are those made by Budovsky et al. [4,5]. These voltage buffers have been made in different varieties intended for different loads. Budovsky et al. have also constructed a few resistive as well as inductive voltage dividers for ac–dc transfer and power metrology [6,7]. Another buffer has been constructed together with a 120:4 resistive voltage divider by Lei et al. [8], where they have characterized it using a Fluke 5790A. An array of resistive voltage dividers have also been made at the Swedish metrology institute (RISE, earlier SP) [9,10].

Through the previous EMRP project "Power & Energy", current shunts and a few resistive voltage dividers were constructed at Justervesenet (JV). The current shunts proved quite successful [11], whereas only one 100:1 divider turned out satisfactory. A further development of the previous work has been initiated,

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with dividers ranging from 10:1 up to 1000:1, all specified to give out nominal voltages in the range 0.5 V to 5 V. A first prototype of the 10:1 divider and a voltage buffer amplifier have been constructed. In this paper, these have been characterized on both absolute gain and ac–dc difference.

In the future, we intend to use the voltage divider and buffer together with current shunts [11] to sample a wider rang of applied electrical powers [12]. For this application, it is important that a given range of applied powers only has a small impact on the divider's division ratio, so that the response can be accurately compensated. Therefore, it is important to characterize the voltage divider and buffer on absolute gain, as well as ac–dc difference. We also intend to use the voltage divider and buffer to divide a wider range of applied voltages from a calibrator, to compare the signal generated from Josephson-based setups.

2 The ac–dc difference

For traceability in ac voltage metrology, thermal transfer via ac–dc difference measurements are still the industry standard, even though Josephson-based ac voltage waveform synthesizers are beginning to become a part of traceability chain. The ac–dc difference (for voltage) is measured by setting two objects (a reference and a test object) in parallel to each other, and simultaneously measure the heat deposition from the load resistance from alternately applied ac and dc voltage. The heat is indirectly measured by a thermocouple. The ac–dc difference is measured either directly using a TC-based DMM, or indirectly using a TC with an external DMM. The TC can be used alone or together with RR, buffer or voltage divider. In any case, the amplitude of the applied ac voltage is adjusted, so that the dissipated power (E_{ac}) matches the dissipated power (E_{dc}) of the dc voltage, in the reference. The measured ac and dc voltage in the test object, denoted V_{ac} and V_{dc}, respectively, are inserted into equation (1) to calculate the ac–dc difference, δ. A more thorough explanation of measurements of ac–dc difference can be read in [13].

$$\delta = \frac{V_{\mathrm{ac}} - V_{\mathrm{dc}}}{V_{\mathrm{dc}}}, E_{\mathrm{ac}} = E_{\mathrm{dc}}. \quad (1)$$

3 Voltage buffer design

The buffer design described in this paper is depicted in Figure 1, and it is a further development of the versions described in [14,15]. Its core module is based on two complimentary Sziklai pairs with diode-coupled (base-collector is shorted) feedback. This is a similar design to those often found in audio amplifiers. Whereas a Darlington pair consists of either an NPN transistor driving another NPN, or a PNP driving another PNP, a Sziklai pair [16] consists of an NPN driving a PNP, or vice versa. Both Sziklai and Darlington pairs are used to amplify the signal applied to the input twice on its way to the output. Furthermore, using two complementary pairs, as have been done in this design, a push-pull configuration is made,

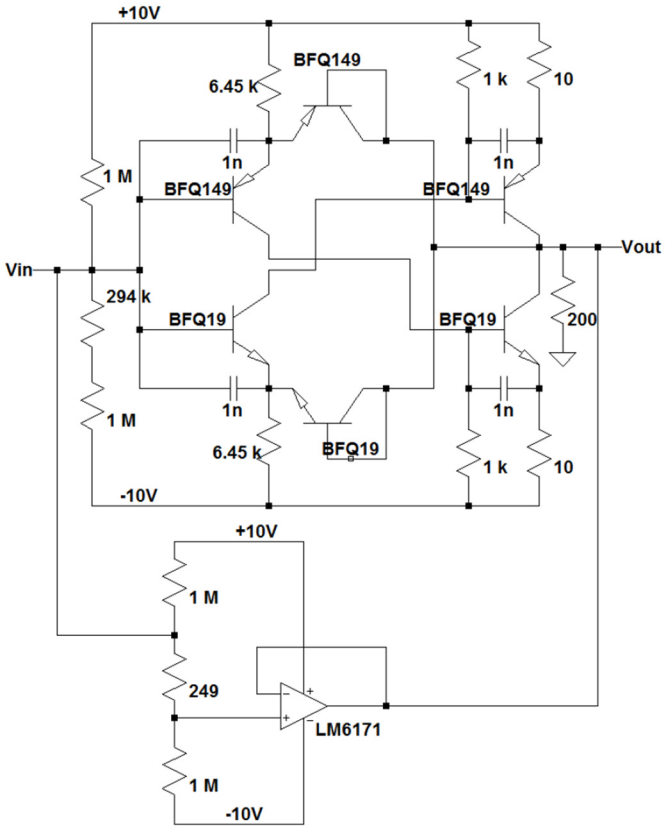

Fig. 1. Schematic of the voltage buffer where Vin is the input female N-connector and Vout is the output male N-connector. The ground on the power supply is coupled to the chassis and outer conductor of the N-connectors. The main buffer core is the push-pull coupled Sziklai pairs (NPN: BFQ19, PNP: BFQ149) with diode-coupled (base-collector is shorted) feedback. The module based on the LM6171 operational amplifier serves as a voltage follower which senses and corrects for the errors in the output waveform produced by the previously mentioned buffer core. The non-inverting input has been shifted downwards in voltage to compensate for the internal offset in the LM6171.

which amplifies the signal more equally for both positive, and negative voltages. This is a good wideband design, because fewer stages generally cause only a short time delay. The transistors selected have a relatively similar operation specs with specifications up to 100 mA collector current, and with maximum operational frequencies of 5 GHz and 5.5 GHz for PNP (BFQ149) and NPN (BFQ19), respectively. This should have a relatively flat frequency response up into the MHz range.

However, contrary to what is normal for audio amplifier circuits, this buffer must be able to amplify both ac and dc voltages rather than just ac signals. For strictly ac usage, large capacitors are generally placed on both input and output in order to avoid dc current sourcing. This cannot be done in a design like this as dc voltages also must be applicable. Because of this, the sourcing is minimized by tweaking the input resistance to compensate for the leakage.

Transistors in general have an exponential current–voltage (IV) characteristic, whereas an amplifier have to be

linear in order to put out a pure voltage waveform. For metrology in particular, avoiding distortion is of utmost importance, so the transistor characteristics is dragged into more linear operation points, to the cost of higher supply power consumption. Also, for a push-pull configuration, the risk is that the operation points of the transistors are not set appropriately, so that either a horizontal or vertical plateau in the IV-characteristic may occur in the cross-over point. Individual mismatch between the threshold voltages of the transistors, may cause an uneven transition of operation between them. In other words; the individual mismatch of the transistors could cause one of the in- or output transistors to either shut or leak when it is not supposed to do so, and thus lead to a spike around 0 V input. This is an issue that might be present in a physical circuit, but not the simulated one.

Most of the current needed to drive the load is provided by the main buffer-core. However, its gain is slightly dependent upon the applied voltage, which distorts the output waveform. To rectify this error, a high-speed, low-distortion, unity-gain amplifier has been added as a correctional stage. This amplifier has been coupled as a non-inverting voltage follower where the working point for the non-inverting input has been shifted in order to compensate for its internal offset. The purpose of this stage is to correct the non-linearity of the buffer core stage by sensing, and then equalizing the difference in voltage level between the buffer's input and output.

The buffer has been designed to optimize two features, namely good dc and ac gain linearity. For this purpose, a simulation model was made in LTspice version 4.23l based on transistor models created by the original producer, Philips Semiconductors, and the model of the operational amplifier created by National Semiconductor, Inc. This simulation model takes into consideration the parasitic contributions of the transistorsa and connectors. Generally, parasitic contributions do not make too much of an impact however; in a feedback circuit, such as this buffer, these contributions may lead to undesired oscillations. In fact, before these parasitic contributions were included into the model, constructed prototypes had a tendency to oscillate at frequencies above 100 MHz, where as this behavior was not mirrored in the model. After introducing these parasitics into the model, the oscillations started to show up in the simulation results as well. These oscillations were quenched in both the model and the prototypes by including 1 nF base-emitter capacitors.

As stated previously, good dc-gain linearity is important for ac–dc comparisons, even for low frequencies. The dc-gain of an amplifier is expected to be constant, hence the output voltage follows:

$$V_{\text{out}} = a * V_{\text{in}} + b, \tag{2}$$

where V_{out} is the output voltage, V_{in} is the input voltage, a is the gain and b is the offset. Simulation of the dc gain linearity in the range from −1.5 V to 1.5 V is presented to the top of Figure 2 as the output voltage subtracted by the linearized gain of the buffer (Eq. (2)). The sweep is presented this way in order to magnify any non-linear tendencies in the dc gain. For a load equivalent to an HP 3458A DMM, the linearization gave $a = 0.999\,722$ V/V and $b = 249\,\mu$V and variation within $\pm 1\,\mu$V.

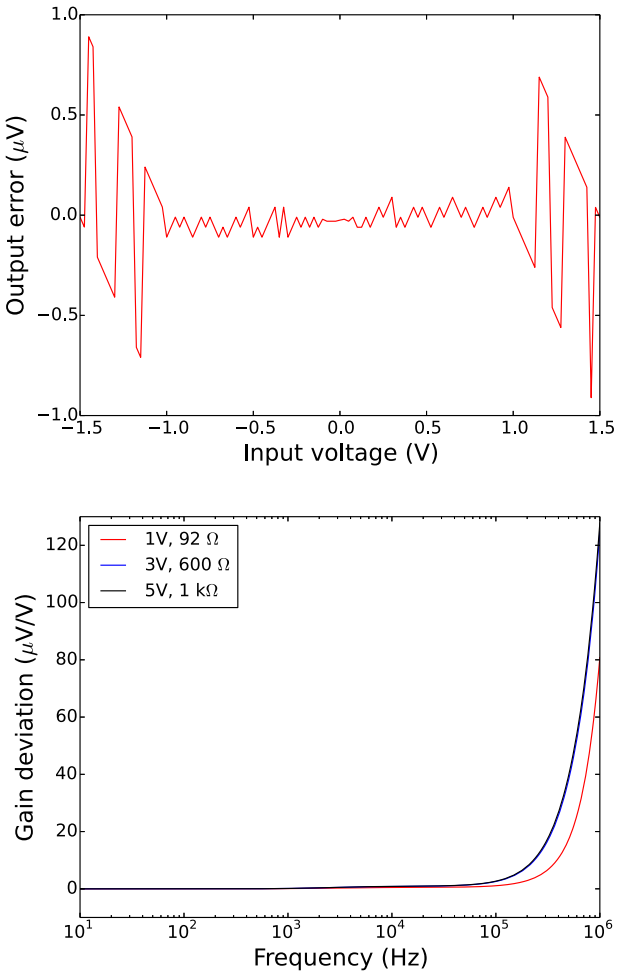

Fig. 2. Simulation results from the optimized buffer model. The top graph is the simulation of error in dc gain linearization according to equation (2). The bottom graph is the simulation of ac gain deviation from 10 Hz for 1 V, 3 V and 5 V input voltage with loads equal to the TCs used in equivalent measurements of ac–dc difference.

Table 1. Simulated ac gain at 10 Hz of the voltage buffer for the three cases of 1 V, 3 V and 5 V input voltage.

Input voltage (V)	Load resistance (Ω)	Gain (V/V)
1	92	0.999 706
3	600	0.999 719
5	1k	0.999 720

To ensuring a good ac gain linearity is to make the output of ac at higher frequencies (in metrology above 100 kHz) comparable to that of lower frequencies, as well as dc. Simulation of the ac gain is shown to the bottom of Figure 2, for 1 V (92 Ω load), 3 V (600 Ω load), and 5 V (1 kΩ load) input as deviation from the gain at 10 Hz. The gain at 10 Hz is shown in Table 1 for each of the three cases. The loads are chosen to mimic the TCs used for equivalent measurements of ac–dc difference.

4 Voltage divider design

The voltage divider is designed to attenuate signals up to 50 V and 1 MHz by a factor 10 V/V with a minimal dependance upon frequency and magnitude. In general, the signal will be supplied by calibrators such as Fluke 5730 or 5700. These calibrators can provide currents up to 35 mA, which means that the resistance of the divider must be selected large enough that this limit is not exceeded at 50 V.

The in- and output stages of the divider were set to be 1.8 kΩ and 200 Ω, respectively, so that the current drawn at 50 V dc would be no greater than 25 mA. However, the divider is to be directly loaded by the voltage buffer, which was described in the previous section. According to simulations, the input impedance of the buffer is 155 kΩ||16 pF. This load comes in parallel with the output stage of the divider, and it must be compensated to avoid a situation where the division ratio greatly depends upon frequency. Also, the geometry of the output stage of the divider contributes with parallel parasitic capacitance, which adds to the total output capacitance. To avoid a phase shift between the in- and output stages, relatively large capacitive components are added to the input stage as well. The aim is to have the product of resistance and capacitance of the input (R_i and C_i, respectively) equal that of the output (R_o and C_o, respectively):

$$R_i C_i = R_o C_o. \tag{3}$$

A simple calculation of the stray capacitance of the output geometry can be performed according to

$$C = \epsilon_0 \epsilon_r \frac{(r_o^2 - r_i^2)\pi}{d}, \tag{4}$$

where ϵ_0 and ϵ_r(=4.4) are the permittivity of vacuum and relative of FR4 (Flame retardant 4, circuit board material), respectively, r_o (=4 cm) and r_i (=1 cm) are the outer and inner radii, respectively, of the disc-shaped output plate, inside the divider, and d (=3.2 mm) is the thickness of two one-layered 1.6 mm thick FR4 boards (inside and outside the divider). Although the output of the divider has a lager disc on the outside than on the inside, the stray output capacitance is calculated according to the lesser disc. By putting these numbers into equation (4), the output stage stray capacitance becomes 57 pF. Added with the input capacitance of the buffer, the total added parasitic capacitance ends up at 73 pF. However, the exact total parasitic capacitance is difficult to accurately predict, and the commercially available capacitors generally have quite a wide tolerance (often up to ±5% of the nominal value). Therefore, the best capacitive compensation must be fine-tuned by a trial-and-error approach.

The voltage divider described in this paper has a cylindrical design with an outer shielding of copper. Both the input resistors and capacitors are mounted to a total of 8 narrow copper-plated FR4 strips, in parallel, 7 strips with resistors, and 1 with capacitors, as depicted in Figure 3. The reason for using only narrow strips is to reduce metal surface in the divider, and hence reduce capacitive leakage,

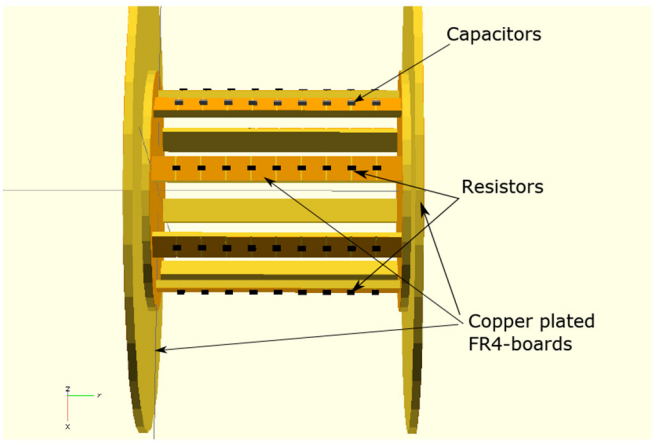

Fig. 3. Simplified model of the Voltage Divider's inner body. The black and grey prisms respectively represent 1.4 kΩ resistors and 330 pF capacitors.

which tends to have a great impact on the division ratio when approaching 1 MHz. The strips are mounted to the input and output planes of the divider, both going directly to their respective female and male N-connectors. The output resistors are mounted on the output connector, directly between the center conductor to a copper film on the flange.

In regards to the set resistance value of the input stage, surface mounted device (SMD) resistors of value 1.4 kΩ were selected, so that the equivalent circuit resistance became 1.4 kΩ*9(series)/7(parallels) = 1.8 kΩ. SMD capacitors of value 330 pF were used for the capacitive strip with an equivalent circuit capacitance of 300 pF/7(series) = 36.7 pF. For the output stage, the resistors were mounted in star formation across the N-connector from the central pin to the copper film on its flange. To form a 200 Ω output resistance, 5 resistors of 1 kΩ were put in parallel. As mentioned previously in this section, the best fit output stage capacitance must be arrived at by trial-and-error. For this reason, the easiest approach to insert this compensation is to couple it in parallel with the divider's output, in a separate box, in a similar fashion to that has been done by RISE [10]. This way, capacitors can be freely added or removed with no fear of altering any other parameters.

For these selected component values, and following equation (3), the theoretically correct total output stage capacitance (parasitic+buffer+compensation) should be 330 pF, and missing this with only a small amount will cause a substantial shift in the division ratio when approaching 1 MHz. The absolute value of the impedance of a parallel RC-junction can be written as

$$|Z| = \frac{R}{\sqrt{1 + (2\pi f)^2 C^2 R^2}}, \tag{5}$$

where R is the resistance, C is the capacitance, f is the frequency, and $|Z|$ is the resulting absolute value of the junction impedance Z. From this, and because the phase in the impedance will be chosen to be more or less the same for

Table 2. Results form the linear regression of the two dc sweeps. The parameters a and b represent gain and offset respectively.

Sweep no.	a (V/V)	b (μV)
1	0.999 701	–770
2	0.999 701	–778
Sim.	0.999 722	249

in- and output, the division ratio can be approximately expressed as

$$\frac{|Z_{\text{out}}| + |Z_{\text{in}}|}{|Z_{\text{out}}|} \tag{6}$$

where Z_{in} and Z_{out} refer to the in- and output stage impedance respectively. For the ideal case where all component values are perfectly nominal, missing the output capacitance by only 1 pF, will lead to a division ratio deviation of about 4000 μV/V at 1 MHz according to the equations (5) and (6).

The approach used to fine-tune the capacitive compensation is to aim for the lowest possible ac–dc difference, by using high-precision TCs. Quick series were measured, where the output capacitance of the voltage divider was tweaked to obtain the response of the ac–dc difference closest to 0 μV/V for the highest frequencies. The best fit was a nominal capacitance of 285 pF.

5 Results

In order to ensure that the gain linearity is good, two dc sweeps were performed 20 days apart, from −1.5 V up to +1.5 V, in steps of 25 mV. Both in- and output voltages were measured using a Keysight 3458A DMM as load. In an optimal buffer, the gain should be perfectly constant. A real buffer however, may have some variation in the gain, which gives rise to distortion of the output waveform. The input voltage versus output voltage for these two sweeps can again be expressed as the linear function in equation (2). The parameters found for each sweep is found in Table 2 together with the simulated values.

The results of the two sweeps are shown in Figure 4 as the output voltage, subtracted by the linear expression, using the corresponding parameter values of a and b. As alluded to in Section 3, such a plot should expose any non-linear tendencies in the buffer.

Two sweeps were performed to check whether or not the buffer had a tendency to over or under amplify any voltage regions, as well as to detect possible drift. Other than a narrow region around 0 V input, all deviations seem to be random. The gain remained within 1 μV/V the same however, as can be seen in Table 2, the offset had shifted downwards about 8 μV. This change is attributable to re-adjustments of the power supply between the two sweeps. The spike in the response in the cross-over point has already been alluded to in Section 3, and is most likely due to the variation of the production of the transistors. Still,

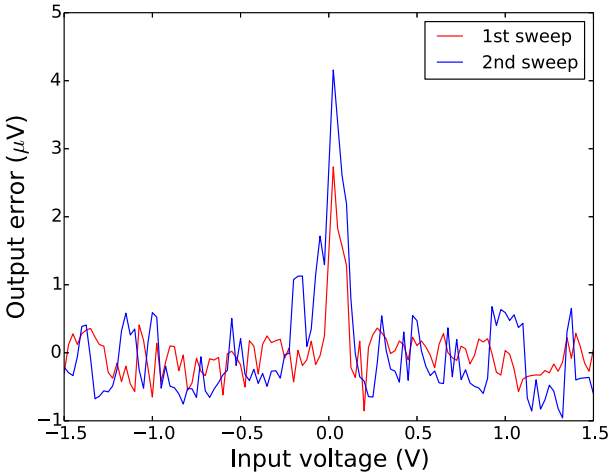

Fig. 4. Resulting error in the linear regressions (parameters found given in Tab. 1) of the two dc sweeps performed on the buffer. The first sweep is in red and the second sweep is in blue. The deviation is well within the ±1 μV band over the entire sweep between ±1.5 V with the exception of small section around 0 V. Here the output deviation peaks, but it is still less than 5 μV, and is due to the slight mismatch in the manufacturing of the transistors themselves since this feature is not found in the simulation presented on the top of Figure 2.

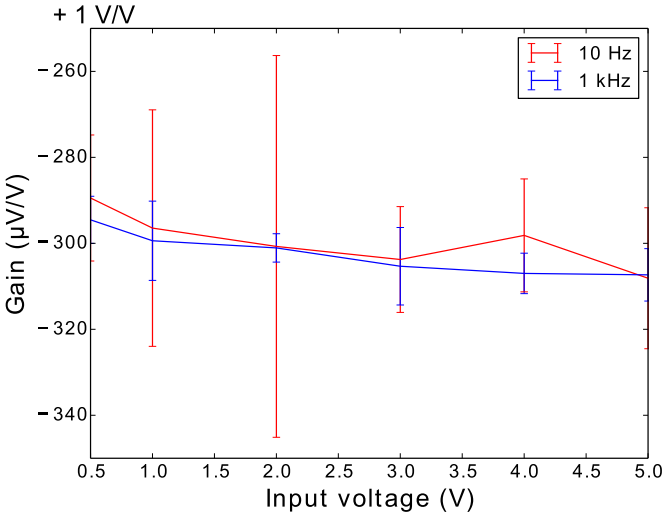

Fig. 5. Resulting absolute ac voltage gain of the buffer. The 10 Hz sweep is in red and the 1 kHz sweep is in blue.

the peak is less than 5 μV in the span of only a few hundred millivolt input voltage, which makes it insignificant compared to the total rms-integral for a nominal 1 V ac.

The absolute gain of the buffer was measured for voltages ranging from 500 mV up to 5 V at 10 Hz and 1 kHz using a Fluke 5790A as load. The signal was applied using a calibrated Fluke 5700A calibrator. The gain linearity of both series are presented in Figure 5 as absolute gain deviation from 1 V/V. The gain consistency was within 19 μV/V and 13 μV/V for 10 Hz and 1 kHz, respectively. For a nominal 1 V input, the gains were 0.999 704 V/V and 0.999 701 V/V for 10 Hz and 1 kHz, respectively.

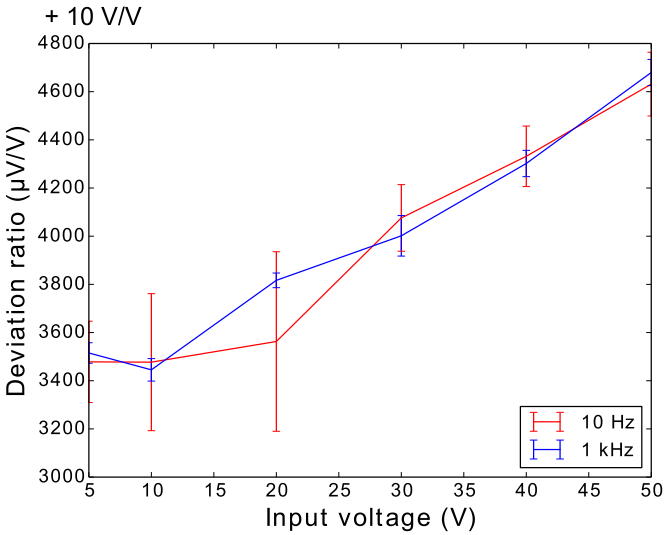

Fig. 6. Resulting absolute ac voltage division ratio of the divider and buffer combination. The 10 Hz sweep is in red and the 1 kHz sweep is in blue.

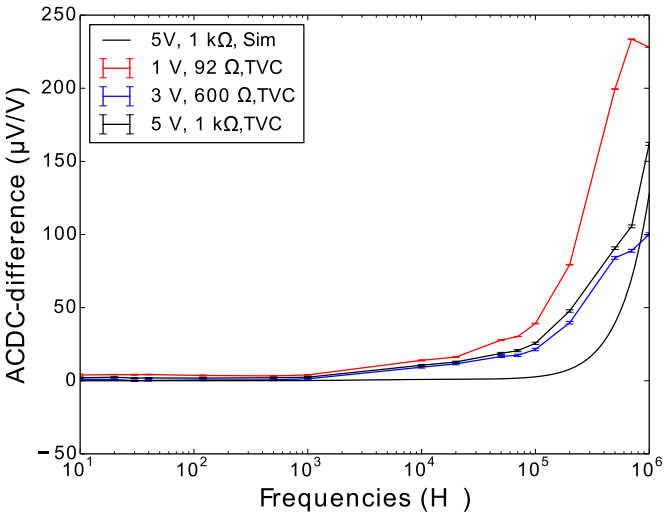

Fig. 7. Resulting ac–dc difference for the buffer from 10 Hz up to 1 MHz. The red curve contains the measurements for 1 V, the blue curve contains the measurements for 3 V, and the black curve contains the measurements for 5 V. The equivalent simulation of applied 5 V has been included in black, without error-bars.

The absolute gain was also measured for the combination of voltage divider and buffer from 5 V up to 50 V for 10 Hz and 1 kHz, in the same fashion as the buffer alone. Here however, it is more appropriate to present the data in terms of division ratio. The results are shown in Figure 6 as the absolute division ratio deviation from 10 V/V. The division ratio consistency was within 1150 µV/V around 10.003 48 V/V for 10 Hz and 1230 µV/V around 10.003 45 V/V for 1 kHz, both for nominally 10 V input.

In order to demonstrate the buffers all-round capability, it was characterized using three sets of TCs. The first set consisted of two 92 Ω TVs from Leibniz-Institut für Photonische Technologien (IPHT Jena), used at 1 V. Next were two sets from National Institute of Standards and Technology (NIST), a set of two 600 Ω TCs and a set of two 1 kΩ TCs, used for 3 V and 5 V, respectively. The characterizations were performed for the traceable frequencies from 10 Hz up to 1 MHz, with 4 measurements per frequency. The results of these characterizations are presented combined in Figure 7. The most noteworthy result is the measurement of 3 V with an ac–dc difference within 100 µV/V at 1 MHz.

For the ac–dc characterization of the voltage divider and buffer combination, the characterisation was performed for 10 V, 30 V and 50 V, using the same TCs as for 1 V, 3 V and 5 V, respectively, as loads for the buffer. As the reference, a combination of RRs (4 kΩ for 10 V and 12 kΩ for 30 V and 50 V) from Balentine and 600 Ω TCs from NIST were used. The results of these measurements are shown together in Figure 8 for frequencies up to 100 kHz. The variation of the ac–dc difference for these various loads and applied voltages is well within 30 µV/V from one another up to 100 kHz with frequency response not exceeding 125 µV/V.

The ac–dc difference for the divider and buffer combination, has a relatively large offset for lower frequencies compared to the buffer alone. The introduction

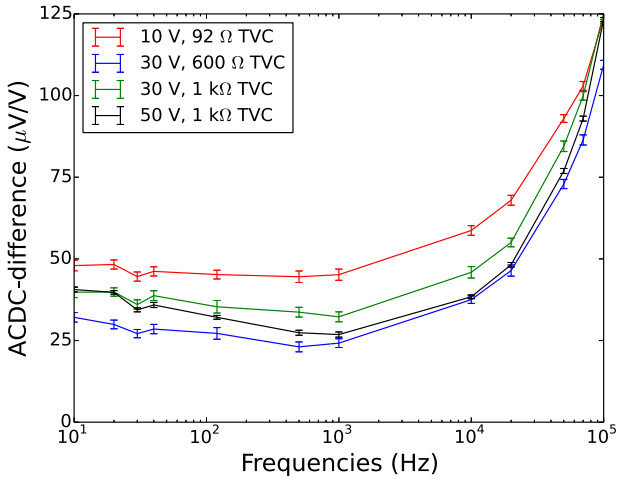

Fig. 8. Resulting ac–dc difference for the divider and buffer combination from 10 Hz up to the maximum capability of the calibrator. Red curve contains the measurements for 10 V, blue curve contains the measurements for 30 V, and black curve contains the measurements for 50 V. The green curve contains the measurements for 30 V, by using the references used for 50 V.

of a fully passive voltage divider should in principal not add to the low frequency response. One reason for this offset could be that the buffer sources current in both in- and output. When using the buffer alone, this sourcing could make an even impact on the reference and object TCs, whereas when the voltage divider is attached to the input of the buffer, the sourcing from the buffer's input is absorbed by the output stage of the divider. Other reason could be either leakage current to ground in the divider or some large induction in the divider itself.

6 Discussion

The real strength of the buffer, is its relatively low variance in both absolute gain and ac–dc response in a wide spectrum of voltages and load impedance. The ac gain varied less than 20 μV/V over an entire decade of voltages from 500 mV to 5 V for both 10 Hz and 1 kHz. For both ac and dc, the gain at 1 V differ less than 4 μV/V, which is especially good as they are loaded by two vastly different DMMs. This robustness is also shown in the ac–dc response, where the applied voltage spans half a decade and the load resistance of the TCs span more than a decade. From 10 Hz up to 1 kHz the ac–dc response for all three measurement series are within 5 μV/V. Comparing this to the just mentioned variation in absolute gain at the same frequencies, it agrees within 5 μV/V in the same direction (meaning slightly higher gain for 10 Hz), and hence good consistency and robustness in the buffer for various voltages and loads.

Combining the voltage divider and buffer, the absolute division ratio for 10 Hz and 1 kHz differed less than 40 μV/ V from each other at 10 V, and less than 3500 μV/V from the nominal 10 V/V division division ratio. Compared to the ac–dc difference at 10 V using the 92 Ω TC as load, the response varies within 5 μV/V (corresponding to a deviation of 50 μV/V in absolute division ratio) in the entire span from 10 Hz to 1 kHz. From 10 V to 50 V the division ratio increases almost linearly but equally for both series, and differing only about 50–100 μV/V at 30 V and 50 V. Again, comparing this to the equivalent measurements of ac–dc difference, from 10 Hz to 1 kHz these measurements only vary within 10 μV/V (corresponding to a deviation of 100 μV/V in absolute division ratio) as well. From this, it can be concluded that in the frequency range 10 Hz to 1 kHz both the measurements of absolute division ratio and ac–dc difference are in good agreement for both the buffer alone and the divider and buffer combination.

Up to 10 kHz, the ac–dc response of the voltage divider and buffer is flat and consistent, although with an offset. In electrical power metrology, the uncertainty requirement is less strict than for ac voltage. This makes it suitable for sampling of electrical power up 100 kHz.

Although the voltage buffer has a relatively good response, improvements can still be made, especially with regards to sourcing and fine-tuning the bias for each of the individual transistor. This could be performed by replacing the 1 kΩ resistors from the supply voltages to the bases on the output transistors with potentiometers with for example a 4.7 kΩ maximum resistance. Also, the input resistors on the buffer core could be replaced by a series of a fixed 1 MΩ resistor and a 1 MΩ potentiometer from signal to each supply voltage. It would also be worthwhile to handpick individual transistor units with the least production variance, especially when it comes to gain and base-emitter threshold voltage. Obviously, consistency in the gain of the transistors equalizes the gain for the two voltage polarities, and equal threshold voltage ensures correct voltage level of the feedback.

The voltage dependence on the measured ac division ratio of the voltage divider can be explained in terms of the increased power and hence thermal heating of the resistors. Future voltage dividers can be improved in the range above 10 V by replacing FR4 with a ceramic material such as Al_2O_3 or AlN. This will insure better heat dissipation and less electrical leakage. In addition, components with lower thermal coefficients should be chosen to reduce the resistance alteration caused by the internal heat development.

For a future 100:1 divider, or a second generation 10:1 divider, these two above-mentioned should be introduced, as well as the inclusion of a capacitive, protective guard for the resistive divider elements. The guard has to be carefully constructed, to form the same voltage profile, as that which is intended for the divider, to exclude capacitive leakage from the divider element. This becomes even more crucial for higher division ratios, since the leakage current becomes proportional to the applied voltage, whereas the applied current has to be limited to what the source can produce. The ratio between leakage and applied current must be reduced to avoid uncertainty in the division ratio.

7 Conclusion

A high-precision voltage buffer and a 10:1 resistive voltage divider have been constructed for use in ac voltage and electrical power metrology. The dc gain of the buffer was measured to be 0.999 701 V/V in the range ±1.5 V, varying less than 1 μV/V over the span of 20 days, including reattachment of the buffer into the setup. Absolute gain and ac–dc difference have been measured for the buffer alone, and for the divider and buffer combination, where both agree within 10 μV/V in the overlapping areas, despite both loads and measurement schemes being vastly different. For the ac–dc difference, voltages from 1 V up to 50 V have been characterized using a variety of thermal converters from different producers, with load impedance ranging from 92 Ω to 1 kΩ. The buffer alone was characterized for 1 V, 3 V and 5 V with responses within 40 μV/V for frequencies up to 100 kHz, and less than 100 μV/V for 3 V at 1 MHz. Improvements can be made by manually fine-tuning the biasing points of the individual transistors, manually, using potentiometers. The divider and buffer combination was characterized for 10 V, 30 V and 50 V, all agreeing well within 30 μV/V of each other from 10 Hz to 100 kHz, with a maximum response less than 125 μV/V. This make the voltage divider and buffer combination suitable for sampling of electrical powers up to 50 V and 10 kHz, and even 100 kHz, albeit with a larger uncertainty.

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