Ultrasound Transmit-Receive Electronics: Study and Upgrade

Sudha Shrestha

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Department of Micro and Nano System Technology,
Buskerud and Vestfold University College, Norway
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We are stuck in technology when what we really want is the stuff that work.

-Douglas Adams.

Abstract

The ultrasonic investigation using transmission of ultrasounds and receiving of the back-scattered echoes is a recognized measurement technology since from the decades. One of the heavy and bulky instrumentation parts in a conventional ultrasound transmit-receive system are the function generators along with power amplifiers required to provided appreciable signal for ultrasound transducer excitation. Technology today where miniaturization has become the prime essence, system design in digital hardware by exploiting programmable logic devices is attractive. This work presents the ultrasound transmit-receive instrumentation designed for flexible user interface, portability and ability to be adopted in various types of ultrasound interrogation. The preliminary design of the ultrasound transmitter using a complex programmable logic device has been accomplished. The essential features for making Doppler velocity measurement has been considered in the system design. Some primary acoustic measurement made with the designed instrumentation is illustrated here. The flexibility, challenges and possible upgrade of the design instrumentation for various field of applications is also discussed in the work.

Acknowledgements

I want to show my sincere acknowledgements to my supervisor Professor Lars Hoff who introduce me with the subject matter. Thanks for his guidance, encouragements and productive discussions. I am sincerely oblige for his cooperation and guidance along the way.

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Contents

List of Figures

List of Tables

1 Introduction

This section introduces the theory behind the Ultrasound and its instrumentation briefly along with short description of some of its field of application and the limitations challenged by the system. The more digging and discussion of ultrasound building block instrumentation is done in the sections following it.

1.1 Ultrasound Overview

Acoustic inspection goes way behind in the history regarding search and testing purposes. Starting with the general sense of hearing the perception of acoustics has reached a wider dimension now, connecting it to mechanical vibrations, Sound Navigation And Ranging (SONAR), seismic noise and ultrasounds. Acoustic waves found its importance preliminary in SONAR and underwater research and search system. Due to its non-invasive nature it is greatly valued for materials flaws detection, testing and also in sensitive field like medical diagnosis. Moreover, the development of ultrasound imaging system came forth along with introduction of Radio wave Detection And Ranging (RADAR) which works in the principle of electromagnetic wave propagation.

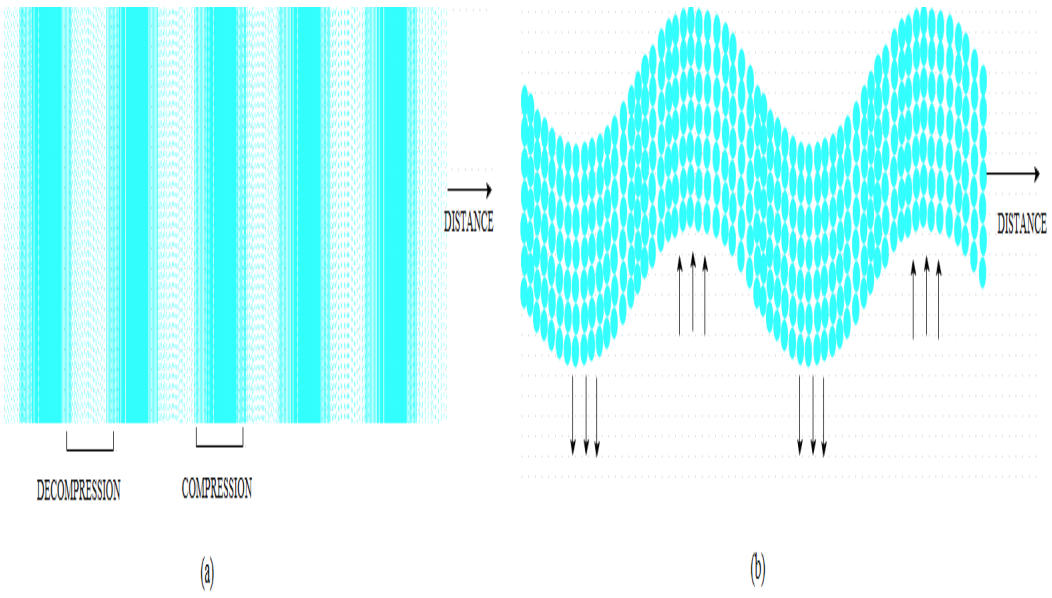

Figure 1: Sound wave propagation; Longitudinal wave (Left), Transverse wave (Right).

Ultrasound is generally described as the sound waves with frequencies above the audible range (15-20 KHz).The sound wave can be basically of two types; longitudinal wave and transverse or shear wave. For the first type, the particles in the medium of wave propagation vibrates along the direction of the wave motion or distance creating the pressure difference in the medium known as compression and decompression. They are often known as the pressure waves (P-wave) and are exclusively used in all ultrasound measurements undertaken in fluids. For latter type i.e. S-wave, the particle vibrates in the perpendicular direction of the wave propagation and comprises for the acoustic wave only in solid medium. This two fundamental phenomenon of the sound wave propagation is illustrated in Figure 1. In general the acoustic wave energy is possessed by the oscillation of the particle of the medium around the equilibrium position. It can be viewed as the mechanical vibration of the medium through which it propagates. Since the phenomenon of acoustic wave follows the law of conservation of mass and momentum along with consideration of the density ρ and the adiabatic compressibility k of the medium though which it propagates, velocity of sound wave(c) is given as in Equation 1[5]. It illustrates that the velocity of sound wave propagation depends on the material through which it travels.

$$c = \sqrt{\frac{1}{\kappa\rho}} \tag{1}$$

Further, the velocity c of acoustic wave propagation can be related to its the frequency oscillation f and the corresponding spatial period of the wave λ as shown by Equation 2. Here the frequency f of the oscillation being inversely proportional to its period λ, it implies that the velocity of wave propagation c increases directly with increase in its oscillation frequency. Then considering the physics of Radio Frequency (RF) wave propagation tells that the attenuation of the wave is considerable with the increase in frequency or short λ i.e. the acoustic wave dies out along the depth of its propagation in the target. But the higher frequency is desired for achieving better spatial resolution during signal processing. Thus trade-offs remains in the depth penetration and spatial resolution provided by specific RF wave.

$$f = \frac{c}{\lambda} \tag{2}$$

In general the principle of ultrasound measurement system is based on the measurement of ultrasound echoes, transmitted or reflected from the stationary or moving targets. The phenomenon of reflection of ultrasound arises due to the variation in the characteristic acoustic impedance of the materials

through which the ultrasound wave propagates. The characteristic acoustic impedance is described as the ratio of acoustic pressure P at a point in the medium to the particle speed at the same point u [6] as given in Equation 3.

$$Z = \frac{P}{u} \tag{3}$$

It can also related to mass density ρ of the medium to the ultrasonic wave of velocity c as given in Equation 4[5].

$$Z = \sqrt{\rho\, c} \tag{4}$$

It is worthwhile to mention some of the major fields of application for ultrasound technology which will give glimpse of its evolution and approaches.

- **Ultrasound For Underwater:** Acoustic waves dominates in underwater communication (detection and location) analogized to the electromagnetic waves for land communication. The reason being quite obvious that they being the mechanical waves are less attenuated in seawater than the electromagnetic radiation which are heavily attenuated by the salt water. For instance, study of the seabed topography, oceanographic conditions, underwater communications with ships and submarines, classification and detection of fish and mines are some of the numerous applications achieved by use of ultrasounds for underwater investigation.

- **Ultrasound For Medicine:** Ultrasonic diagnosis is widely used in field of medicine due to its minimal side effects. Ultrasonic which is the term use for ultrasound in medical diagnosis is the ongoing field where approaches are developed year after year to make the imaging practice in medicine more efficient, both qualitatively and quantitatively. Medical diagnosis using ultrasound imaging is preferred method among the available technology, such as X-ray, Nuclear or Magnetic ultrasound imaging because of its non-invasive nature, capability of real time imaging, soft tissue and blood flow imaging [7]. Also the low cost and ease of building equipment requirements makes it more attractive. Ultrasonography or the ultrasound imaging in medical term is the well know term in the field of medical diagnosis for the evaluation of the heart, blood vessels, neonatal brain, glands, breast, organs of abdomen and pelvis [7]. Although advance electronic instrumentation and signal processing has been developed in the field of medical ultrasound imaging, the

limitation still remains as ultrasound cannot penetrate through bone setting limitations on chest and abdominal imaging as the ultrasound imaging cannot be performed in air [5].

- **Ultrasound For NDT :** Ultrasound technology has been extensively used in Non-Destructive Testing (NDT) as for examples; ultrasonic flaw detection, material characterization, pipeline inspection, surface testing for fatigue and environmental cracking in the civil engineering structures. In the last decades various acoustic or ultrasonic system has come forth as a successful NDT system, for instance air-coupled system, optical interferometric detection, laser generation, non-contact acoustical transducers and hybrid combination of the above [8]. Traditional ultrasound system mostly uses some fluids as a coupling media between the ultrasound transducer and the target, since they provides better coupling and low damping for ultrasound transmission. This has been established as an exclusive measure in making ultrasound measurement. Today approaches and researches are being ongoing extensively in the field of air-coupled ultrasound system which uses air as the coupling medium between ultrasound transducer and the target. Air coupled ultrasound has physical importance for NDT as they provide possibilities for the tests to be performed under hostile and inaccessible geometries. Also they are valued for noninvasive and non intrusive measure in the measurement process. It provides ease in ultrasound measurement process as the coupling medium like fluids for acoustic impedance matching is not crucial here. As to mention some examples, it is valued greatly in the measurement of the operating condition within the industrial process plant, particularly in nuclear and chemical industry for pure and sterile processes [9]. But the challenges remains as air-coupled ultrasound induces high acoustic impedance mismatch in the ultrasound measurement. such system demands for high level signal for ultrasound transducer excitation to provide acceptable level of Signal to Noise Ratio (SNR). They require more scientific research and extensive verification before being standardized as a ultrasonic NDT measure.

- **Ultrasound For Velocity Measurement:** The measurement of velocity of fluid flow using ultrasound is done using PW or Continuous Wave (CW). The PW and CW ultrasound measurement system is often known as Doppler measurement as they exploits some artifact of the Doppler effect. The Doppler Effect comes from the sense when investigating the frequency of the back scatter signal from the moving

target. Since, for the moving target the frequency of the back scattered signal is altered from the transmitted frequency, there is a Doppler shift in the received frequency as shown by the following Equation 5[5]:

$$f_d = \frac{2\, f_o\, v\, cos\theta}{c} \tag{5}$$

Where, f_d is the Doppler shift, f_o is the frequency of the transmitted ultrasound beam, c the ultrasound wave velocity, v velocity of scatter and θ is the angle between the ultrasound beam transmission and the velocity direction of the flow. The CW ultrasound instrument uses this Doppler effect to detect the moving object which scatters the ultrasound wave e.g blood [6]. Here, the ultrasound wave is continuously transmitted from one crystal of the transducer element and the back-scatter ultrasound echoes from the target is continuously received by another crystal in the transducer element [6]. The received signal when multiplied by the transmitted (CW) signal followed by the low pass filtering results a signal with frequency being proportional to the velocity of the moving target [6]. This method of using CW for velocity measurement does not put any limitation on the maximum velocity measurable but the drawback remains in its inability to provide the range resolution in the velocity measurement of the moving targets i.e. the inability to distinguish between the two nearby targets or to give the accurate direction of the flow.

On other hand the PW ultrasound system does not employ the Doppler frequency shift of the ultrasound echoes to detect the velocity of the moving target. In PW ultrasound the pulse burst of ultrasound is transmitted often using a single element ultrasound transducer and the back-scattered ultrasound echoes received by the same element [6]. The sampling is actually performed once for every pulse transmission which implies that the sampling frequency of the PW ultrasound signal corresponds to the Pulse Repetition Frequency (PRF) of the transmitter. Hence, the shift in the position of the scatter is detected here rather than the shift in the transmission frequency. Mover over, as requirement of the Nyquist criteria for the error free reconstruction of the sampled signal, the ultrasound frequency f_o given in Equation 8 must be less than half of the sampling frequency i.e the (PRF).This criteria to avoid the frequency aliasing in Doppler measurement is given in

relation 6.

$$f_o < \frac{PRF}{2} \tag{6}$$

The limitation put forth by Nyquist limit shown in Equation 6 is on the bandwidth of the Doppler signal i.e the PW of ultrasound ultrasound and the maximum measurable velocity. As the limitation put forth by the Nyquist limit (6), aliasing in the velocity measurement is given in Equation 7 [5] which directly relates to the PRF or the sampling frequency. Often the low PRF doppler is preferred to have better range resolution while the high PRF Doppler is for measuring higher velocities. An appropriate choice of pulse width PW, PRF or Pulse Repetition Time (PRT) for the Doppler signal forms the state-of-art for the instrumentation in the Doppler measurement.

$$V_a < \frac{PRF\ c}{4\ f_o\ cos\theta} \tag{7}$$

In the Doppler velocity measurement using PW, as the imaging is done in local range using short pulse, the PW ultrasound measurement gives good range resolution in the velocity measurement of the target. Hence, it is often use as an exclusive method for velocity measurement e.g color flow imaging [6]. The main drawback here is the limitation on the maximum measurable velocity as aliasing will be encountered for the higher velocity of the target. The relation of the maximum velocity limit in the PW ultrasound of ultrasound frequency f_o with velocity of ultrasound in the target c from the maximum range D is given in relation 8:

$$V_{max} = \frac{c^2}{8\ f_o\ D\ K} \tag{8}$$

Here, K is the correction factor for allowing the reverberations of backscatter ultrasound to disappear (K is normally choosen in range 2 to 5) [6]. Hence, lowering the frequency f_o of the ultrasound signal is desirable for higher velocity measurement. As shown in Equation 5, the Doppler shift is directly related to the radial velocity component $Vcos\theta$, it allows the measurement of the velocity of the range cell as long as the beam transmission perpendicular to the velocity direction is avoided.

1.2 Imaging Modes

The brief description of some of the different imaging modes that has been developed in ultrasound imaging are mentioned below:

- **A-Mode:** The earliest ultrasound imaging mode developed is the A-mode imaging which use the intensity or amplitude of the ultrasound echoes received. The ultrasonic pulse is transmitted into the target and the back-scattered signal are picked by the same transducer which forms the one dimensional line image [5].

- **M-Mode:** M-mode is the motion mode in which the received echoes are plotted against time. So it displays the echoes to image the target that are not static as for example heart [5]. Here, the depth in the target is displayed along one axis with respect to the time in other axis and the amplitude of the back scattered signal is shown in the gray scale.

- **B-Mode:** In B-mode imaging the intensity or amplitude of the received ultrasound echoes are displayed as the brightness of the image formed. It is the two dimensional amplitude imaging of the ultrasound signal where the amplitude of the back-scattered signal is coded in gray scale along the axis of beam direction on the display [5].

- **Doppler-Mode:** The common Doppler mode can be either PW or CW as described before in section 1.1. Other Doppler modes like as Multi Range Gated (MRG) also exist but is seldom used in ultrasound system which already include gain control in its instrumentation.

- **Three Dimension (3D)-Mode:** The 3D ultrasonic imaging being proposed already in 50's provides efficient processing and visualization of the image model with the aid of morden computer display technology [5]. The 3D image is formed by collection of many Two Dimension (2D) image scan lines. Thus, it is a rather slower mode for moving targets since it takes considerable amount of time to collect data for image formation.

Conventional ultrasound system possess some inherent uncertainties since the imaging model are assumed planar while the ultrasound beam reaches considerable thickness (approximately 10mm). Even performing 3D imaging, the chances of error still holds as the images are extremely prone to speckle noises and uncertain imaging artifacts. Also, error in the instrumentation or calibration inaccuracies adds significant error. As for instance, a constant speed of sound assumption and envelope sampling of the RF data [10].

1.3 Electronics Surrounding Ultrasound System

The principle of ultrasound imaging had been established very early in the history but the underlying instrumentation corresponding for different appli-

cation desired is still the field of research and development. Looking back in the past, ultrasound instrumentation used to be very bulky and large to provide appreciable signal measurements. For example, the conventional high power amplifier in ultrasound system uses transformer as voltage step-up and impedance matching element for excitation of the ultrasound transducer [11]. The large truns of coil in the transformer eventually leaves the ultrasound system with the large power amplifier box. Although the principle of ultrasound system being very simple, the diversity in its field of applications demands for more stringent electronics, transducer and associate signal processing. As for instance, the ultrasound system while using different imaging modes often requires multiple channels e.g approximately 100 to 200 channels for two dimensional imaging, above 300 channels for three dimensional scanning. Thus miniaturization is prime essence here to make the ultrasound system portable, less expensive and overall flexiblity in operation.

Regarding the above facts, development of ultrasonic electronics spurred along with development of Integrated Circuit (IC) and holds challenges for its upgrading and optimization. Dedicated IC electronics for ultrasound instrumentation electronics have been developed by established manufactures like Analog Devices, National Instruments, Maxim, Texas Instruments. Moreover, micro-processor control based instrumentation is much favored in present context as they enhances functionality, multiple channel signal transmission and processing, flexibility of instrumentation, portability and provides ease in user interface. The ease in development time, cost reduction and design optimization is also accountable here. Such instrumentation exploits digital hardware designing with logic synthesis using Hardware Description Language (HDL) like VHDL and Verilog which allows for the realization of a programmable hardware design. This technique greatly helps in optimization of the design, minimization of cost and development time with less alteration in circuit's hardware. The digital designing of the circuit provides the design much more robust configuration as mounting and soldering of the discrete hardware components to complete the design is greatly reduced. The common hardware bug in the design of analog circuit like a false open circuit or short circuit, poor solder connection are eliminated. Thus for the compactness, robustness and overall celerity provided by such programmable hardware, miniaturization of the electronics here is ultimate.

Today more convenient implementation of the digital integrated electronics using HDL programming are carried out on Programmable Gate Array (PLA)s or Programmable Logic Device (PLD)s comparing to the Application Specific Integrated Circuit (ASIC) design which take much more development time and expense with very less flexibility for design alteration. The short description of the two established PLDs are described here as

follow:

CPLD

The CPLD single chip consist of several programmable logic devices (PLD) which can be programmed. The switch matrices are provided to make connection among the PLDs. It supports interfacing to diverse logic levels as for example 2.5V, 5V, 18V in the XC9572XL−5VQ44 (IC CPLD 72MC 5NS 44VQFP, Xilinx Inc., San Jose, CA, USA) CPLD and allows Joint Test Action Group (JTAG) interface. Examples of some of the leading manufacturers of the CPLD chips are Xilinx, Lattice, Altera [12]. The main strength of CPLD lies in the procession of inbuilt Read Only Memory (ROM) which makes the HDL design configured in it non-volatile. The fast and reliable clock distribution and standard JTAG interface feature allows programming, erasing and verification of the design for high performance application anywhere anytime. On the other hand, space consumption is considerable due to inbuilt memory in semiconductor logic in CPLD, so there is limitation in the number of available flip-flops and the input-output pins that it can offer for the design configuration.

File Programmable Gate Array (FPGA)

FPGA were introduced in the mid 1980's by Xilinx. It allows to customize design architecture which can be modified whenever as being named field programmable. The dissimilarities of FPGA with the CPLDs lies in the storage technology, architecture, the built in features and cost. The FPGA are composed of numbers of Configurable Logic Blocks (CLB) surrounded by array of input-output blocks. It is inherently volatile due to the absence of inbuilt memory but provides advantage in wide variety of off chip storage. As for instance Static Random Access Memory (SRAM)memory based are provided from manufactures like Xilinx and Altera, anti-fuse memory based form Actel and Quick Logic are also available. Its operation is normally based on the Look Up Tables (LUT)s where the designs are implemented [12].

Hence, the above mentioned features of CPLD and FPGA makes them both a possible digital hardware for ultrasound instrumentation. An example of a HDL use in programming these PLDs is described in the following topic.

1.4 Hardware Description Language VHDL

VHDL is a hardware description language use to describe the digital electronic system. Its origin came from the Very High Speed Integrated Circuits (VHSIC) program and was subsequently developed as a standard language under Institute of Electrical and Electronic Engineers (IEEE) [13]. First, it allows the description of the system structure by fragmentation and their interconnection. Secondly, means for the specification of the system's function with familiar programming language is provided. Thirdly, it allows the simulation of the design of the system before fabrication process which gives option for alternatives comparison and test for the correctness without expense of hardware prototyping and time. Lastly, the synthesis of the detailed structure of the design is allowed reducing the development time and providing strategic design decision. The Figure 21 gives the understanding of the design flow in the VHDL language. Unlike the high level programming languages like as C (ANSI C, Dennis Ritchie & Bell Labs), C++ (ANSI C) which are sequential, the VHDL code are inherently concurrent i.e execution is parallel. The concurrent feature of the VHDL programm provides an advantage for parallel processing of the digital design implemented in the corresponding PLDs. This ultimately leads to faster signal processing in application where speed is the prime specification of the design.

1.5 Function Generator

The basic function of the function generator in the ultrasound system is to transmit the desired signal functions of various frequencies chosen according to the specific requirements of the ultrasound investigation undertaken. The signal generated are ultimately used in the excitation of the ultrasonic transducer. Two methods are commonly used in signal generation in ultrasound application; spike and burst. Generally the spike signal is the single delta pulse while the burst signal can be of few cycles of sine wave or three level bipolar pulse. The three level bipolar pulse are more common practice in the ultrasound system. There are different types of standard function generator used in the ultrasound transmitter system available from various manufactures. Figure 2 shows the block diagram of some function generators.

Table 1 list some features of conventional analog function generators e.g. 5800PR (Olympus corp., Shinjuku, Tokyo, Japan) along with the digital pulser demo-board MD1210+TC6320 (Supertex Inc., Bordeaux Drive Sunnyvale, CA, USA) which has been used as the replacement for the function generator in this design.

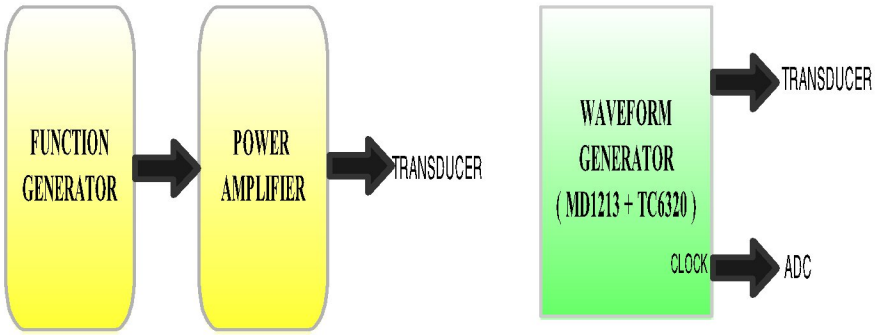

Figure 2: Block diagram of conventional analog function generator (left) and the digital waveform generator (right).

PULSER(Transmit-Recive)	Pulse Type	Available Voltage (No load)	Weight
5800PR [14]	Negative Impulse	300V	6 kg
5900PR [14]	Negative Impulse	220V	7.27 kg
5627Rpp-1 [14]	Negative Impulse	150V	7.27 kg
MD1210+TC6320 [1]	3-level Pulse (Programmable)	Dual 100V	approximately 100 gm

Table 1: Examples of some pulsers.

1.6 Ultrasound Transducer

The ultrasound transducer is an active part of the ultrasound measurement system. Its principle function is the conversion of energy from electrical domain to the mechanical domain and vice-versa. There exist a variety of ultrasound transducer using various methods for mechanical and electrical coupling, for example piezoelectric transducer and capacitive transducer [15]. Their diversity also exist in the shape, aperture diameter (lable D in Figure 3) and the number of active element used i.e. single element, linear or phased array for different mechanism of beam focusing and steering [5]. The choice of specific transducer in a ultrasound investigation is often application oriented. For example medical ultrasound often uses 1D or 2D array transducer, underwater SONAR system uses array elements transducer while the fish finding mostly employs a single element transducer, NDT uses either single

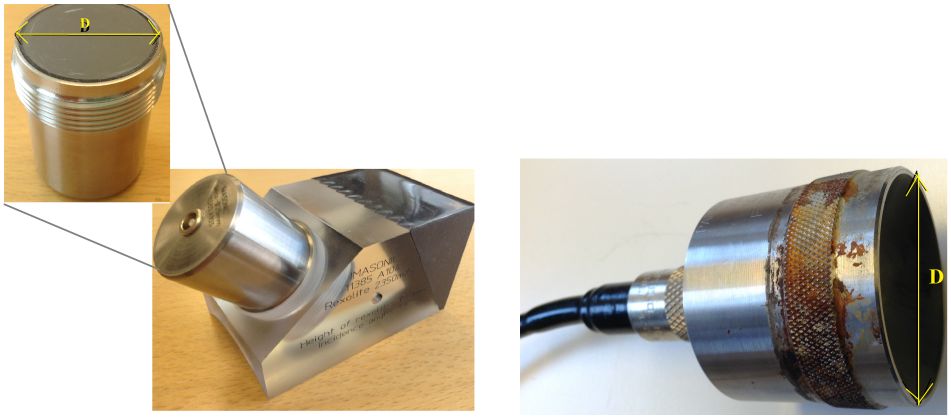

Figure 3: Single element ultrasound transducers.

element or array transducer depending on the applications. Today, there exist variety of configuration on the transducer design provided by established manufacturers like Olympus, Vermon, Imasonic for ultrasound interrogation in different applications. The conventional ultrasound transducer exploits piezoelectric effects for the electro-mechanical coupling. The piezoelectric materials like Rochelle Salt, Barium Titanate and quartz are able to generate ultrasonic waves with frequencies above 1MHz [5]. Today's ultrasound transducer are made of ceramic materials e.g Lead Zirconium Titanate (PZT) which also provides good resistant to heat and radiation [9] being is beneficial in many NDTs. Figure 4 shows the basic ultrasound beam from a single element ultrasound transducer. Moreover the available apperature D of the ultrasound transducer is only a limited number of wavelengths λ i.e. a in Figure 4 of the corresponding ultrasound ultrasound [5].

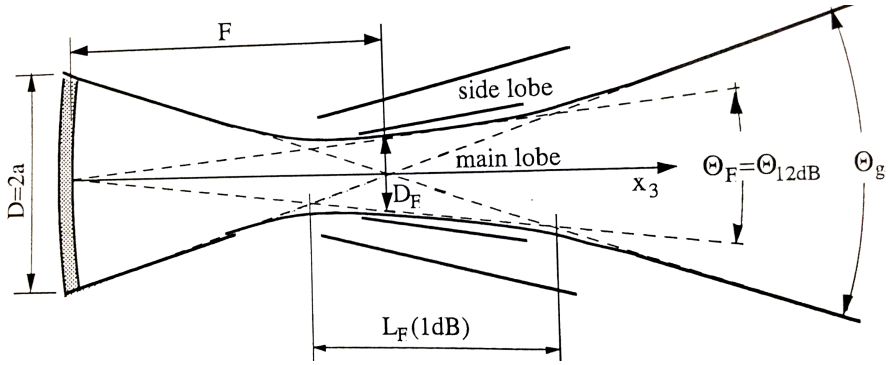

Figure 4: Ultrasound beam focusing from spherical shell disc (D is aperture, a is wavelength of the ultrasound) [5].

Apart of the choice of crystal for ultrasound, other factor that are considered in ultrasound transducer is impedance matching for optimum power transfer during energy conversion. The impedance matching should consider the acoustic impedance mismatch between the transducer and the target and also the function generator or pulser. The acoustic impedance matching for the transducer as shown in Figure 3 is often maintain using backing and the matching layer [6]. Employing an Electrical Impedence Matching (EIM) network for Acoustic Impedence Matching (AIM) is a common practice in improving the bandwidth of the transducer in applications e.g in acoustic emission detection and in medical imaging [16]. So, a special circuit can be used for the purpose of matching the complex impedance of the transducer with the pulser circuit. Since, the modelling of the transducer as a ultrasound device refers to the RLC ultrasound circuit, a dedicated circuit for complex impedance matching of the transducer can be done by using transformer ratio along with the RLC circuit.

The appropriate choice of the ultrasound transducer is more of application oriented. To have the desired beam profile and sensitivity trade-off often come forth for bandwidth and sensitivity they can provide.

2 System Description

This section mentions the motivation for the work undertaken in the background topic. The associate system in the design is elaborated under subsequent topics. Introducing the initiation of work, the short discussion of the overview of ultrasound transmitter system designed and lastly some limitations in the system design is presented here.

2.1 Background

There are numerous valuable motivation for formalizing the task of designing a ultrasound transmit-receive system. This project started as upgrading the building block electronics for the air-coupled ultrasound NDT. Moreover this work was aimed to aid in possible optimization of the electronics in the ultrasound transmitter system for NDT and probably replace the large boxes like as power amplifiers and function generators used in the conventional ultrasound measurement system. Latter it evolved as a generic single channel transmit-receive electronics for ultrasound system which can aid in many ultrasound applications. For example in the Doppler velocity measurement, a general purpose laboratory kit for studying and analysing ultrasonic measurements and so on. Similar system has been used in Rikshospitalet University Hospital (Oslo, Norway) for continuous observation of cardiac function during and after cardiac surgery [17]. The dedicated analog electronics and software used in this system provided the background and motivation to start the task of designing the building blocks for ultrasound system. Here main focus has been done in providing flexibility in function generator that transmits the ultrasonic waveform such that this system can be adopted in many ultrasonic applications. Also optimizing of the transmitter for the Doppler measurement was desired as this transmitter system is intended to be included in the Doppler velocity measurement of oil or fluids in pipelines by Kongsberg Devotek As (Kongsberg, Norway). The field of application of the purposed ultrasound transmit-receive instrumentation seemed to be wide and genuine which provided a good motivation for the system designed.

2.2 System Hardware

The hardware of the designed system was aimed to scale the sizes of analog power amplifier and function generators, see Figure 2, used in ultrasound measurement system down to the PCB level. Figure 5 shows the outlook of the purposed system. The transmit-receive hardware block features ana-

log and digital hardware of the system designed which is also the main task undertaken. This block provides output signals like HVOUT a high voltage signal to drive ultrasound transducer and the CLOCK to be used as synchronous sampling signal for ADC and SYNCOUT which can be used for the trigger. This output features are valued for making accurate Doppler measurements. It provides additional flexibility and features for different ultrasound inspection processes. Figure 6 shows the detail components of the transmit-receive hardware which are discussed in the following topics.

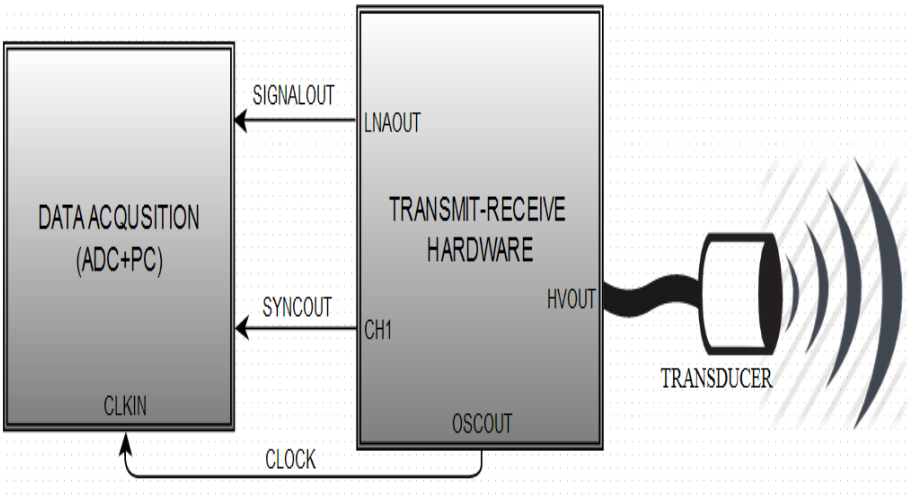

Figure 5: The overall system block diagram.

2.2.1 Transmitter Board [1]

The transmitter board is a factory manufactured PCB prototyped of Supertex's MD1210DB demo board (Supertex Inc.), see Figure 7. It provides the ultrasonic pulses of desired frequencies as programmed which is used to interrogate with the target cell. Referring to the data-sheet of MD1210+TC6320 demo board, it is capable of transmitting high speed of 100 MHz, high voltage dual 100V ultrasound pulses with output current sourcing of 2A. Its PCB layout avoid any parasitic coupling from the high voltage outputs to the low voltage inputs by using solid ground plane, good signal and power routing on the board. As depicted in Figure 8, the embedded CPLD when configured with tri-state pulser firmware (see Section 3.3) along with the level translator i.e. MD1213(Supertex Inc.) high speed driver and the power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) amplifier TC6320(Supertex Inc.) stands as a possible replacement for the function

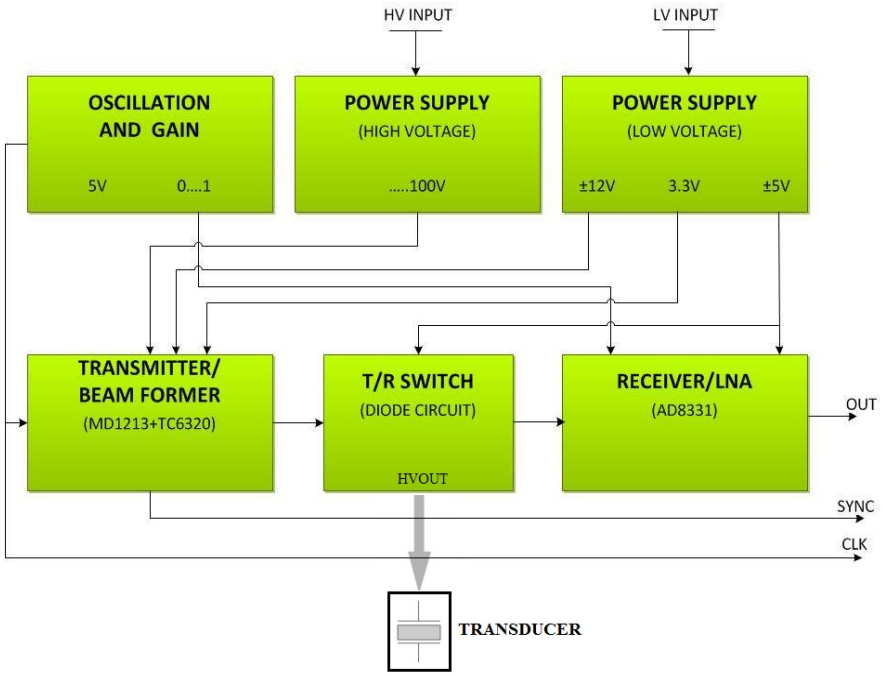

Figure 6: The ultrasound transmit-receive system block diagram .

generator and the power amplifier blocks in the ultrasound system, see Figure 2.

The level translator [1] or the high speed driver MD1210DB (Supertex Inc.) circuitry provides multiple signal levels e.g logic level of range 1.8V to 3.3V for the high speed performance up-to 100 MHz and line level of optimum range dual 10V to 100V for DC coupling. Its input logic level being Complementary Metal-Oxide Semiconductor (CMOS) logic compatible i.e. 1.2V to 5V is favourable for low power and high speed logic solution. The high speed driver allows for the pulse settling time i.e. the rise and fall time down to the order of nanoseconds e.g. 6ns. Its output swing below ground level allows for transmitting the three level bipolar pulse while its logical inputs (INA and INB) can remain in ground reference. Further with all its features and appropriate a appropriate CPLD design configuration can make it an appropriate ultrasound transmit-receive instrumentation for velocity measurements.

The design specification of the output signals from the waveform generator is described as following:

1. The logic supply of 3.3V for the input logic.

2. The low voltage supply of 12V for output stage in amplifying the output

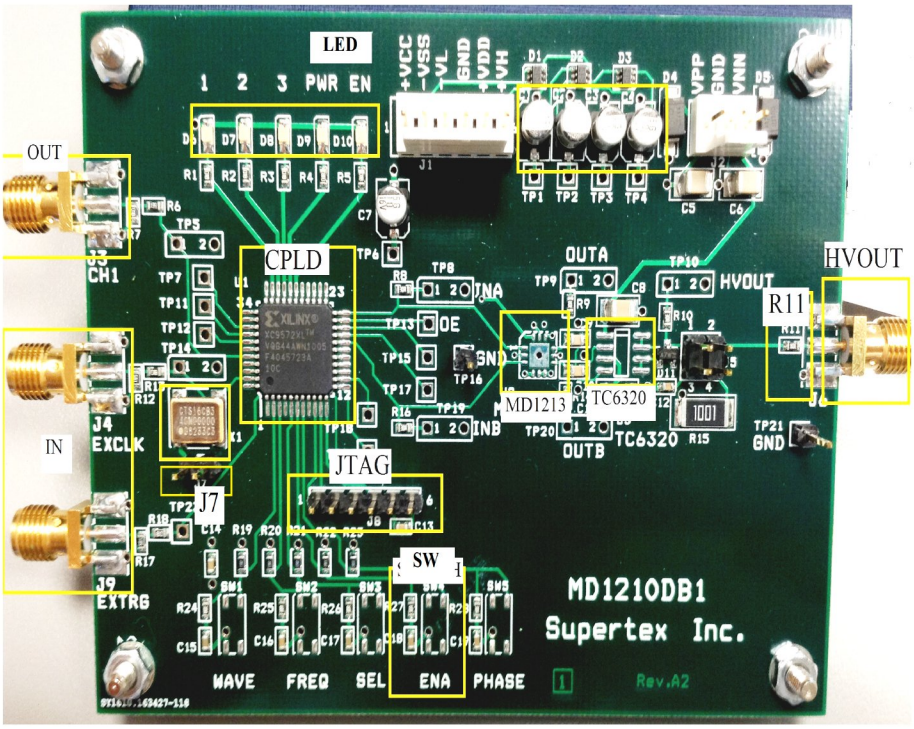

Figure 7: The MD1210DB transmitter board [1].

pulse under low voltage level.

3. The high voltage supply of typical 100V for output stage in amplifying the output pulse under high voltage level.

4. The two pulse burst output from the pulse generator (INA and INB from CPLD in Figure 8) of few cycles of the desired ultrasound frequency transmitting at a constant repetition rate and are phase inverted with each other but also with the delay of half cycle of the ultrasound frequency between them, see Figure 9.

5. The three level bipolar high voltage pulse burst transmitting at the constant repetition rate output (HVout in Figure 8) from the board for ultrasonic transducer excitation.

6. The sync output (CH1 in Figure 7) which can be used as a triggering signal while investigating input or output waveforms.

7. The enable signal (OE) to turn the transmitter ON and OFF with the on board switch select can be seen in same Figure 7.

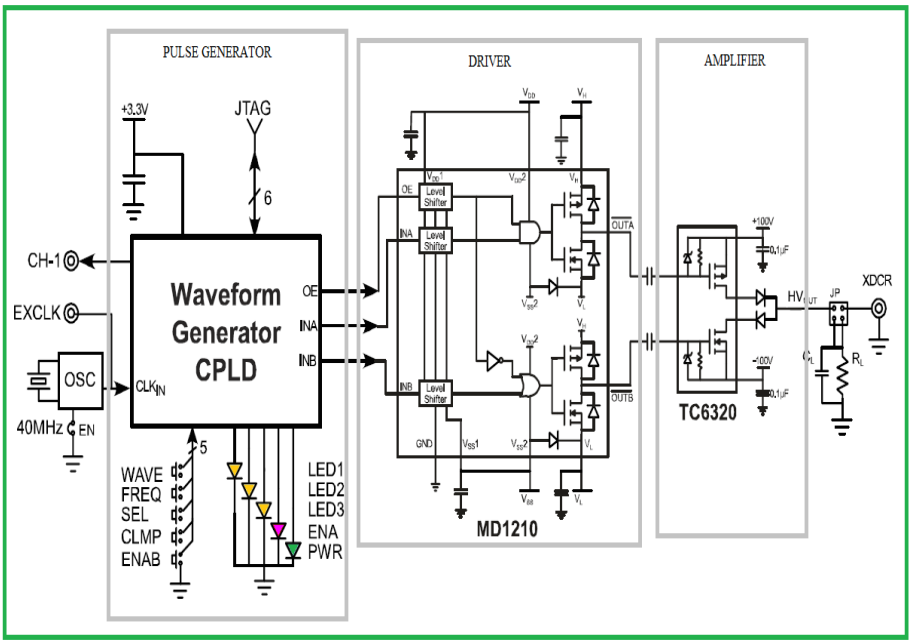

Figure 8: The MD1210DB transmitter board circuit diagram [1].

8. The on board Light Emitting Diode (LED) indication to display the normal functioning of the MD1210DB board.

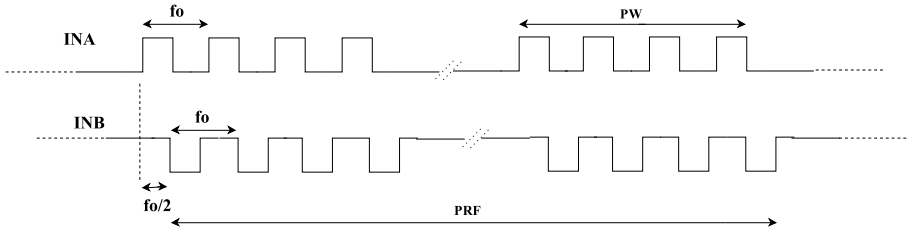

Figure 9: The outputs INA and INB from the CPLD.

The three levels of the output pulse i.e. HVout in Figure 8, from the MD1210DB board relates to the three different states of the output pulse encoded using two logic inputs (INA and INB in same Figure 8) [1].The summary of this states is shown in Table 2 where bit values 0 and 1 has been used to refer low and high state of the logical inputs respectively.

As shown by the pulser Disable state in the Table 2, when MD1213 is disabled i.e. OE=0, the positive and negative supply voltage (Vh and Vl) sourced from the power supply board for the purpose of pulse amplification are connected to the outputs by default. This subsequently keeps the

Logic Input			Transmitter Output		
OE	INA	INB	OUTA	OUTB	STATE (3-Levels)
1	0	1	1	0	Ground (0V)
1	1	1	0	0	Positive peak (+12V)
1	0	0	1	1	Negative peak (-12V)
1	1	0	0	1	Avoided
0	X	X	1	0	Diasable

Table 2: Truth table of logical states for digital pulser.

P-channel and N-channel power MOSFETs (see TC6320 in Figure 8) turn on which helps to complete the power supply path. Thus, when the level translator chip MD1213 is enabled i.e. OE=1, the logical input should never meet the state Avoided as this will turn off the P-channel and N-channel power MOSFETs leading to short circuit of the power supply which might be fatal for the MD1210DB board. The procedure undertaken for meeting these design specifications is discussed in synthesizable VHDL design part 3.3.

2.2.2 Transmit-Receive Switch

The T/R switch dedicated for ultrasound application are manufactured today by different established manufactures. As for example, the multichannel high speed T/R switch IC for embedded system LM96530 (Texas Instrument Inc., Dallas Texas, USA), MAX4936/MAX4937 (San Jose, California, USA). The model of the passive T/R switch shown in Figure 11 is referenced from the T/R switch passive circuit configuration of these IC switch. Figure 10 shows the single channel T/R switch for the ultrasound transmit-receive system designed and the corresponding circuit diagram is shown in Figure 11.

In the ultrasound transmit-receive system, it is often critical to separate the high power signals from the transmitter end from reaching the receiver circuity such that any possible damage of the receiver electronics is avoided. Since the transmitted signals are in the range of hundreds of volts while the received signal is in the rage of few milivolts. This is often achieved by introducing a transmit-receive switch between transmit and receive hardware in the system path. The T/R switch functions with integrated clamping diodes capable of protecting the receiver's Low Noise Amplifier (LNA) amplifier from high voltage pulse from the transmit channel. The single channel T/R switch, see Figure 10 receives the high voltage signal input from the pulser output (Figure 7). The series noise limiter diodes (1 and 2 in Figure 11)

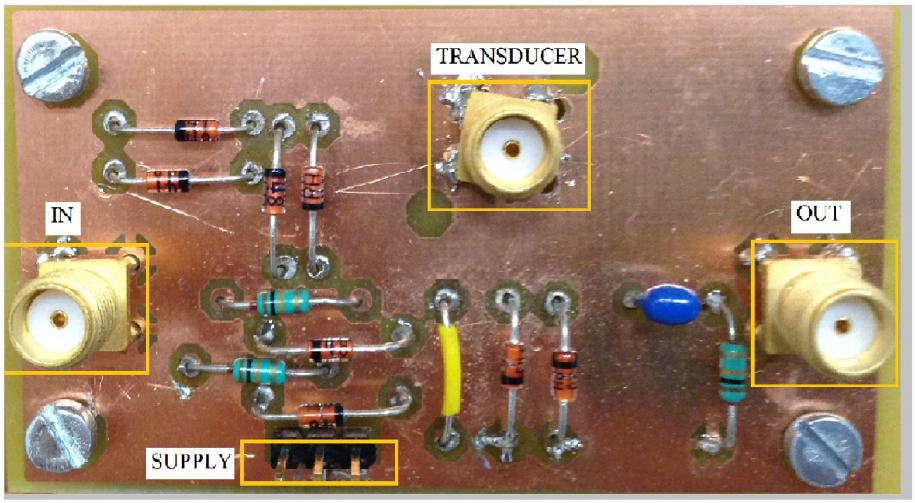

Figure 10: A single channel T/R switch PCB.

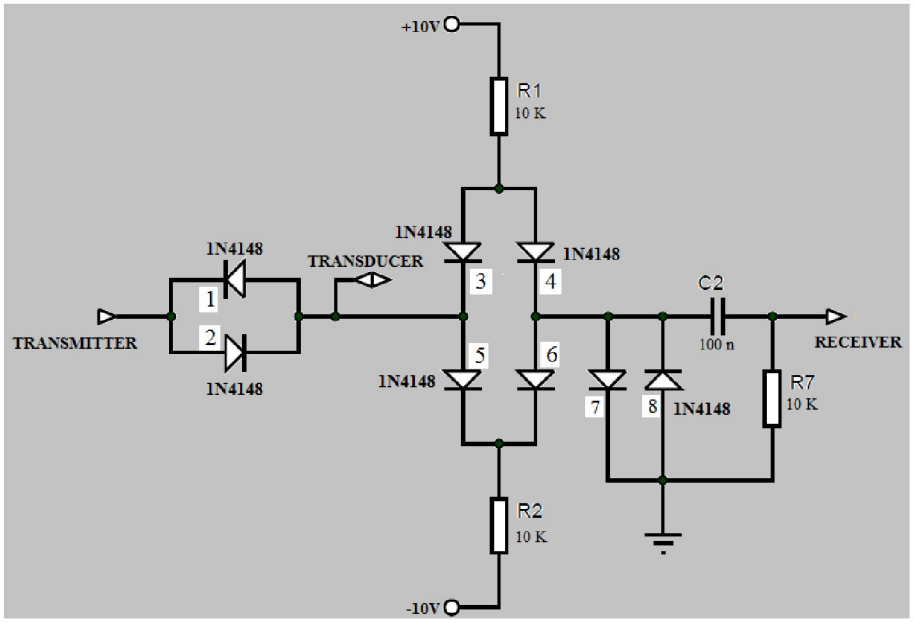

Figure 11: A single channel T/R switch passive circuit.

limits noise RF input pulse and regulates the necessary signal level to drive the ultrasound transducer. The clipping diodes (see 3, 4, 5, 6, 7 and 8 in Figure 11) reduces the high voltage signal level of hundreds of volts to the low level of around 700 millivolts. Thus this passive diode switch basically uses the voltage drop over diodes to isolate the transmitter and receiver.

2.2.3 Receiver

The receiver block in the ultrasound system is used to receive and amplify the back-scattered ultrasound echoes received from the transducer. It can be a single channel or multichannel depending on the number of received RF scan-lines from the ultrasound transducer that it can process. Since the received RF signals from the targets are the low level signals whose strength are depth or time dependent i.e. echoes from larger depths are weak than the near ones or signals from larger depths are received latter in time than the near ones. To compensate these factors, its prime function is often to provide the low noise variable gain or time gain amplification of the received signal. Today various type of dedicated receiver for ultrasound application are provided by established manufactures e.g. Analog Device, Texas Instruments which can be readily implemented in the ultrasound measurement signal path. Figure

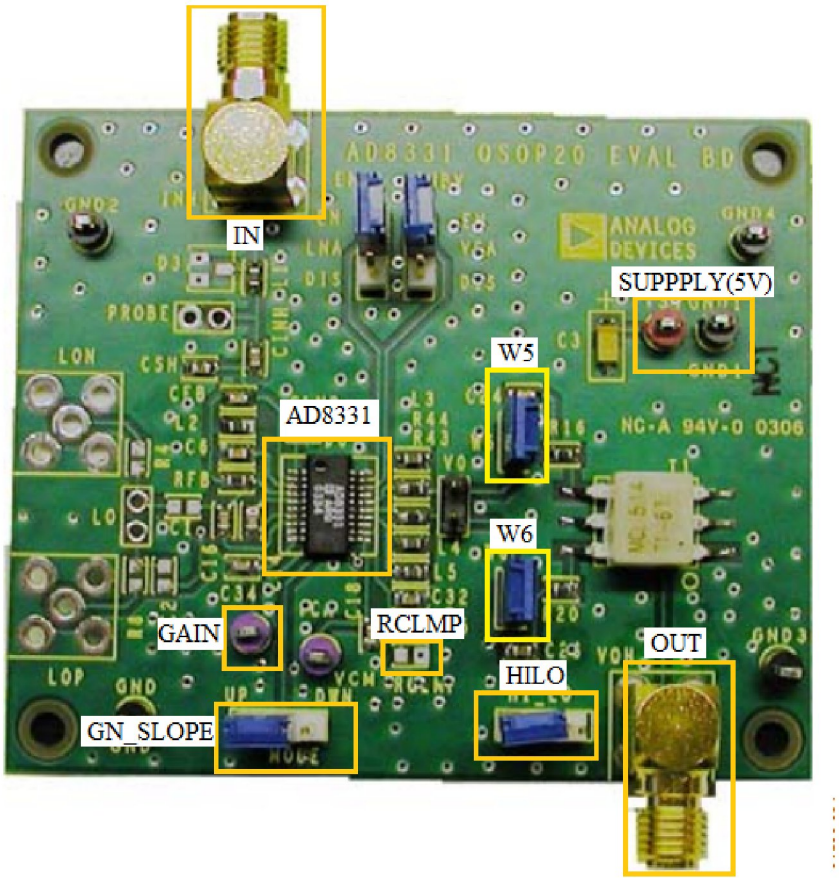

Figure 12: The dedicated AD8074 evaluation board for ultrasound receiver from Analog Device. [2]

12 shows the single channel ultra low noise amplifier AD8331 (Analog Device Inc., Norwood MA, USA) evaluation board which is a dedicated platform for gain control of the received signals in ultrasound and SONAR applications. The circuit diagram of AD8331, see Figure 13 comprises of a ultra low noise amplifier LNA followed by variable gain amplifier Variable Gain Amplifier (VGA) and a logic programmable amplifier (PA) at its output stage. The LNA plays critical role in minimizing the noise level and user-adjustable impedance matching at the input stage. The ultra low noise characteristic of this preamplifier helps in maintaining the good noise performance in the overall signal chain of AD8331. It provides default impedance of 50 Ω to match the impedance with function generators and network analyzers or data acquisition board [2] beneficial for maintaining low noise and better performance. Also, the option for programming the input impedance to 6 kΩ is allowed on the evaluation board. The VGA of AD8331 input is capacitive

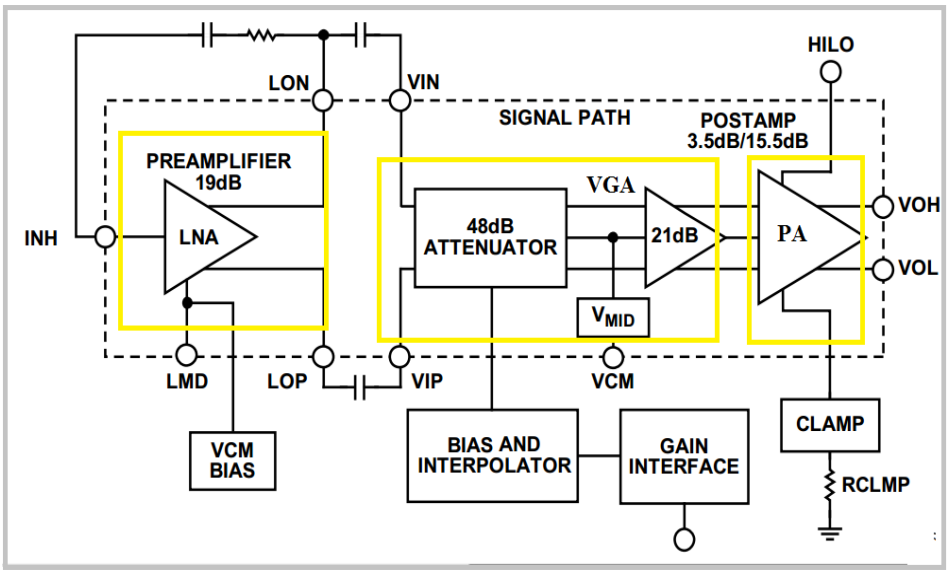

Figure 13: The circuit diagram of AD8074 evaluation board from Analog Device. [2]

coupled to the preamplifier (LNA) output as shown in Figure 13. It serves in matching the attenuation of the input ultrasound by providing the variable gain amplification to the received signals. It provides precise interpolation with excellent linear gain and low noise to the input signal. This feature optimizes low gain error, maintains uniform bandwidth and low distortion in signal path which is essential in Timing Gain Control (TGC) of ultrasound measurement system. It features linear -3 db bandwidth of 120 MHz which is ideal for general ultrasound measurement purpose. The analog gain control

voltage (Vgain) controls the gain of VGA which can range from 40 mV to 1V. The Vgain input should be maintain between the range 0.1V to 0.95V for minimum error in gain. This feature is meet by the designed oscillator and gain board, see Figure 14 which can supply the gain voltage between 0V and 1V. The option for up (high) and down (low) slope of the VGA gain is provided by GN_SLOPE pin on the evaluation board, see Figure 12 which provides negative or positive slope of the gain respectively. The negative gain slope i.e up is favourable for the TGC in ultrasound measurement.

The final output stage of AD8331 i.e. the logic programmable amplifier performs post amplification function. It allows the selection of output noise floor and adjustment of the gain range with the HILO logic pin, see Figure 13. The LO and HI modes option allows for optimization of high speed ADC drive. The HI mode can be suitable in driving ADC with higher noise floor while the LO mode is suitable in driving ADC with lower input noise floor. It also allows the desired output signal clamping with an appropriate resistor value in the RCLMP test pin provided on the board, see Figure 12 which is useful on limiting overloading of the following ADC if necessary. All these characteristic features of the AD8331 receiver board is ideally suitable in ultrasound measurement system. Some of them e.g. HILO, Vgain was exploited in the designed.

2.2.4 Oscillator and Gain Board

The oscillator and gain board (PCB4) is desired in the ultrasound transmit-receive system to have the local oscillation of desired frequencies for the transmitted signal and the gain control voltage for the received signal. This local oscillation can also be used to provide the synchronizing clock in sampling for further signal processing by ADC. Figure 14 shows the PCB prototype of oscillator and gain board and the corresponding circuit diagram is shown in Figure 15. The referenced circuit is shown in appendix 37 which was upgraded in the design i.e. modifying the local oscillator circuit part using AD8074 (Analog Devices Inc.).

The local oscillator circuit part provides the external input clock signal for the MD1210DB board input logic i.e. EXCLK in Figure 8 and also the reference sampling signal for data acquisition in ADC i.e. CLKIN in Figure 17. The clock signal EXCLK input for the MD1210DB board is required to have the desired ultrasound frequency in ultrasound transducer excitation and the common oscillation signal is required for sampling by the ADC as to avoid the jitter during any Doppler velocity measurements. Here, the on board crystal oscillator can be changed to have the oscillation of different frequencies as desired. The triple video buffer AD8074 used allows buffer-

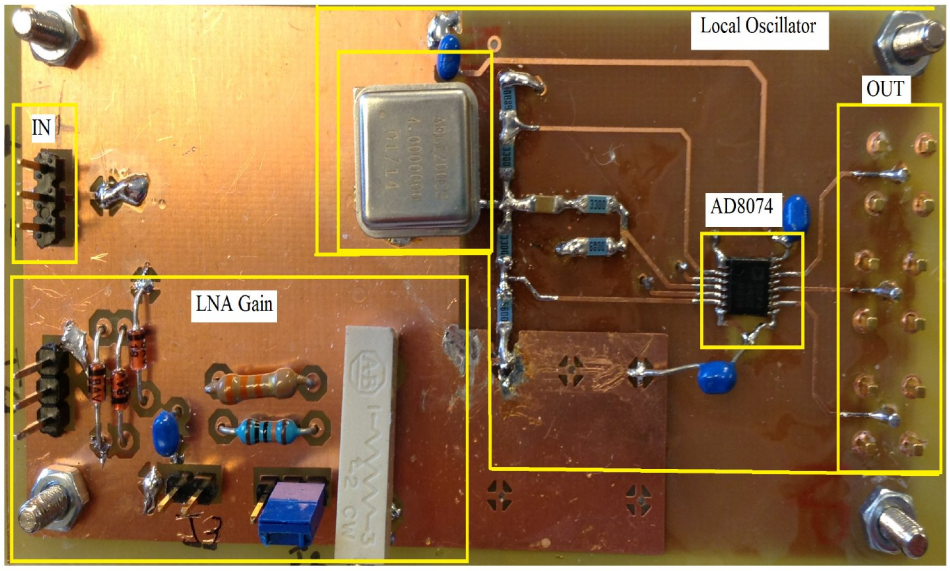

Figure 14: The oscillator and gain board.

ing of the oscillator output to 50 Ω loads. The three outputs provided by the AD8074 buffer are two DC coupled and a AC coupled with 50Ω termination, see Figure 14. The DC output can be used for the clock signal of the MD1210DB board while the AC coupled output can be used for sampling signal by ADC. AD8074 feature provides -3dB full signal bandwidth of 450MHz with output settling time of 4ns [18]. This extreme bandwidth and high slew rate is an advantage in driving the high speed input logic of the MD1210DB board and also for providing the local oscillation as a clock input for the ADC.

The LNA gain circuit, see Figure 15 provides the voltage for gain of the receiver's LNA. The gain network using a voltage divider circuit of 100 KΩ potentiometer, see Figure 14, can provide gain voltage in range of 0V to 1V in the design.

2.2.5 Power Supply Board

A power supply board plays a vital role for overall system functioning and performance by supplying the necessary power. It provides the electrical energy required for normal operation of all the system components.

There exist different topologies in the design of a power supply, e.g. a linear power supply or a switch mode power supply. Most of the power supplies today are switch mode using a complex switch circuit and has better efficiency and wide range of input dynamics. But they are often very noisy

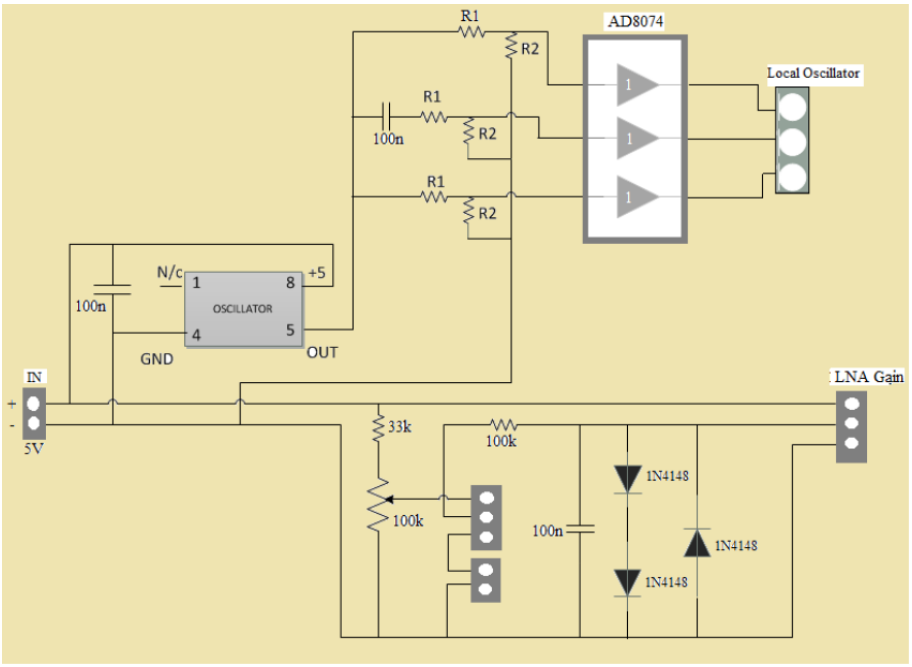

Figure 15: The oscillator and gain board circuit diagram.

due to switching topology they exploits for upgrading their efficiency. The conventional power supplies are more of linear types with simple construction i.e. using capacitors and regulators. They are less efficient than switched power but the noise level and AC ripples are considerably low. The low efficiency implies that there is a power dissipation which should be removed using heat sinks.

A linear low noise regulated power supply is favourable in the ultrasound measurement system where the input stages are sensitive to noise. It also needs to provide enough overhead for all the load constantly since any voltage drop or fluctuation will lead to an error in output voltage supplied to the system which can introduce error in the measurement undertaken. Thus a linear low noise power supply for the system designed is shown in Figure 16. The design specification for the low voltage power supply board is given in Table 3.

2.2.6 Data Acquisition using ADC [3]

One of the primary data acquisition functions in the ultrasound measurement system is the analog to digital conversion. It is to convert the analog signal into discrete from which can be stored and represented in the digital device like a PC for instance. The digitizer NI PCI-5122 (National Instruments

Regulated Output(DC)	Description
5V dual	Input supply for PCB2,PCB3 and PCB4 (6)
12V dual	voltage amplification supply logic for PCB1 (6)
3.3V single	Input logic for pulse generator (CPLD 7)

Table 3: Design specifications for power supply board.

Crop., Austin, Texas, USA) used in digitizing the receiver output is shown in Figure 17. It provides simultaneous digitization of two channels at a maximum sampling rate of 100 Mega Sample per Second (MS/s). It allows high resolution with 14-bits and real-time streaming of the acquire data. It is a dedicated electronics for applications like RF data streaming. It is ideal for both time and frequency domain analysis. Its feature for multiple recording of the received samples is an advantage for any ultrasound data processing. The measurement and analysis function is provided on the software drive or can be interfaced by designing Virtual Instrument (VI) programs in software like LabView.

2.3 Transducer

The ultrasound transducer performs the critical function of electromechanical coupling i.e. conversion of the transmitted high voltage PW into transmitted ultrasound pulse in the target and electrical signal conversion of the received back-scattered echoes from the target. The ultrasound measurement system exploits different types of ultrasound transducer according to the requirement of the specific application.A single element ultrasound transducer of 1 MHz ultrasound frequency, see Figure 18 (left) was used for the corresponding function. The aperture D of the transducer can vary considerably according to desired beam focusing under desired ultrasound investigation. Figure 18 shows some examples of the ultrasonic transducer which will be used along with the designed ultrasound instrumentation in making ultrasonic measurement.

2.4 Software Tools In The Design

For the completion and simulation of the design involving digital and analog part of the system, some software tools were used. This are described briefly below:

ISE Design suite

The ISE Design suite V14.3 (Xilinx Inc., San Jose, CA, USA) provides the ground for analysis, design and synthesis of the digital part of the ultrasound transmit-receive system designed. The ISE Design Suite is the development tool from Xilinx which provides a complete front-to-back design environment along with the Register Transfer Level (RTL) to bit-stream design flow suitable in logic design. The upgraded versions available today e.g. Vivado (Xilinx Inc.) can also provide the high-level synthesis like C, C++ specifications directly into the target PLDs without requiring to manually program the RTL as in the HDL program. It is an industry-proven solution for Xilinx all programmable devices. So it was used as the tool for design and implementation of the ultrasound transmitter configuration in XC9572XL−5VQ44 (Xilinx Inc.). As the implementation tools for the specified PLD, it is driven by the corresponding timing requirements. The tool assign design constraints e.g. registers, flip-flops, input-output ports for the design. It exerts the appropriate amount of the of effort required to ensure the fulfilment of the timing requirements e.g. the propagation delays in the target PLD, signal slack time constraint. However over constraining of the timing requirements e.g negative slack in signal path. The routing and mapping of the signals should be correctly by providing a proper user constraint file (.ucf) in the design tool. By properly constraining the target PLD resources the programmed hardware description language e.g. VHDL, Verilog is implemented in the target PLD without ambiguity. Moreover when the timing requirements are over-constraints, the effort to meet this requirements are also significantly increased leading to increased memory use, tool run-time. It can also result in degradation in the performance of the particular requirement as well as other requirements applied to the design. So all the requirements including the timing constraint e.g. signal propagation delay, signal slack should be proper applied according to the specifications provided by the corresponding PLD.

In the firmware design of a single channel PW ultrasound transmitter design, the resources of XC9572XL−5VQ44 was successfully constraint by providing the proper net-list of the user constraint file i.e. the .ucf file and speed grade i.e. −5 in ISE Design tool. The use of ISE tool for VHDL programming to configure the specified firmware is more detailed in the experiment section.

Proteus Professional

The analysis for the functionality and prototyping the layout for fabrication of the analog electronic circuits of the ultrasound transmit-receive system was desired to complete the design. The Protetus Professional V8 (Labcenter Electronics Ltd., Grassington, North Yorkshire, England) software was used in hardware prototyping and simulation of the analog electronics part of the transmit-received ultrasound system designed. It is an Electronic Design and Automation (EDA) tool from Labcenter that allows for design and simulation of the hardware/software in embedded system [19]. It consist of many service modules which offers different functionality e.g schematic capture, PCB layout. The ISIS schematic capture module allows for interactive circuit simulation of the design which can be exported for PCB production with Advance Routing and Editing Software (ARES) or other PCB layout software. ARES as PCB layout module of the Proteus Design Suite which allows a complete netlist based PCB design.

Laboratory Virtual Instrument Engineeering Workbench (LabVIEW)

LabView (National Instruments Crop.) software was used as an optional interface in the PC for the observation of the received ultrasound signal investigation in the designed system. It also allows for further signal processing of the digitized RF signals from the ADC. It provides an option to adopt the designed system for different ultrasound measurements modes e.g. M-Mode, Doppler Mode. As a signal processing tool, it aids in manipulation of digital signal by setting up the corresponding Data Acquisition (DAQ) assistant software to configure the voltage channel from the DAQ e.g. ADC to the PC. Thus the motive here is to provide more flexibility in signal processing at the output stage.

LabView is a visual programming language platform and development environment provided by National Instruments. It is graphically-based programming language which provides an ideal workbench for test and measurement, instrumentation, automation and control system, data acquisition and data analysis applications [20]. The programs in LabView are called Virtual Instruments (VI) since it provides graphical interface for its comprehensive set of tools e.g. oscilloscope, multimeters. It can simulate hardware devices and also provides different built-in-libraries for advance analysis and data visualization by creating the VI programs.

2.5 Limitations of Designed System

The ultrasound transmit-receive electronics designed was a mixed system type i.e. including both analog and digital system. The main focus was to upgrade the system for adopting in different ultrasound applications and miniaturization for its portability. Regarding these goals, the comprehension of a complex system entirely in digital hardware is physically not possible with the technology available today. Thus trade-offs between hardware and software are often unavoidable in mixed system design. The major limitation is often encounter due to the sample rates in the digital system comparing to the analog counterpart. The hardware/software trade-off for cost and performance, power and efficiency is encounter in the design. As for instance, the conventional analog function generator are more robust, simple to operate and cheaper but lacks in efficiency, flexibility and portability. Likewise its possible digital e.g. MD1210DB board counterpart provides flexible user interface, efficiency and portability but holds challenge for arbitrary functions and are costly, see Figure 2 in section 1.5. The analog function generator used in excitation of the ultrasonic transducer, see Figure 6 allows the use of low supply voltage, inexpensive low voltage MOSFETs for switched mode amplification. On the other hand, it can provide significant SNR as being able to produces high level signals e.g. 400V peak-to-peak signal [11]. This optimistically leads for robust configuration to the system block and availability of higher signal level at the output for ultrasonic transducer excitation. On the pessimistic side, it makes the system block huge and bulky creating inconvenience in the overall system portability. It can also basically generates any arbitrary functions i.e. signal of any desired functions but the control of the transmitted signal's phase, length is often challenging. Also the operation bandwidth is often limited for low frequency ultrasonic application (100KHz to 2 MHz [11]) which is not always desirable.

Comparing to these facts, implementing the digital board e.g. Figure 7 allows for miniaturization, system block portability, wider frequency bandwidth for operation and more programmable control of the transmitted waveforms. There is also possibility for providing additional features for further signal processing in digital system e.g. providing the synchronizing sampling clock for Doppler velocity measurement. The shape or function e.g. sinusoidal and strength of the output signal provided for ultrasonic transducer excitation is limited to the pulse shape. However the three level bipolar waveforms are common and acceptable for most of the ultrasonic interrogation. So designing the waveform generator for the ultrasound transmitter seems to be a better approach although some trade-offs are accountable.

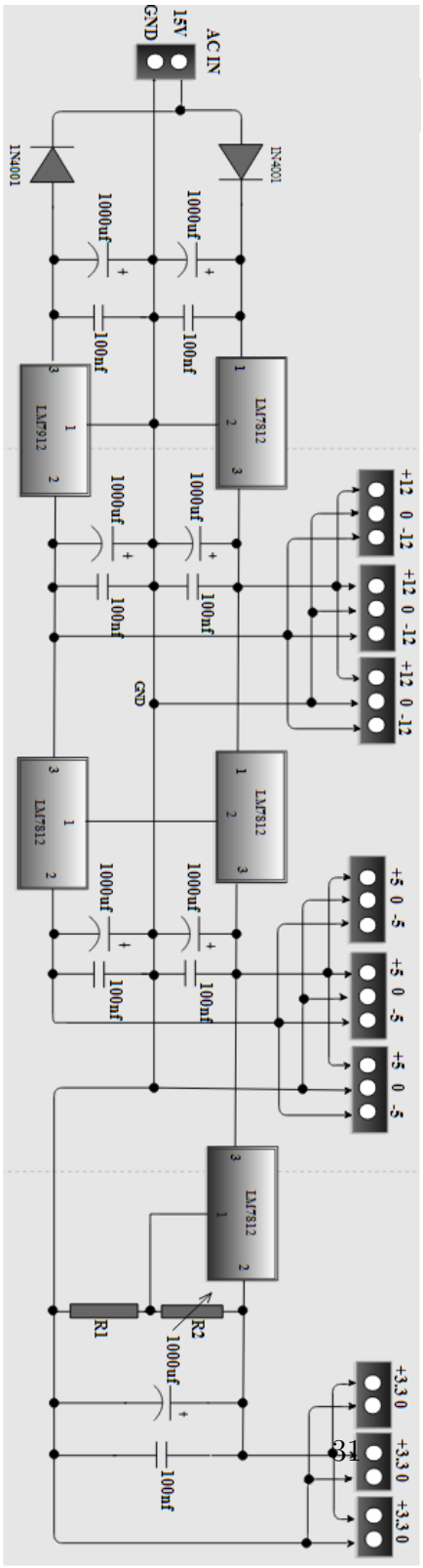
GND
15V
AC IN
1N4001
1N4001
1000uf
100nf
LM7912
LM7812
+12 0 -12
+5 0 -5
+3.3 0
R1
R2

Figure 17: The 14-bit 100MS/s digitizer from National Instruments(NI PCI-5122).[3]

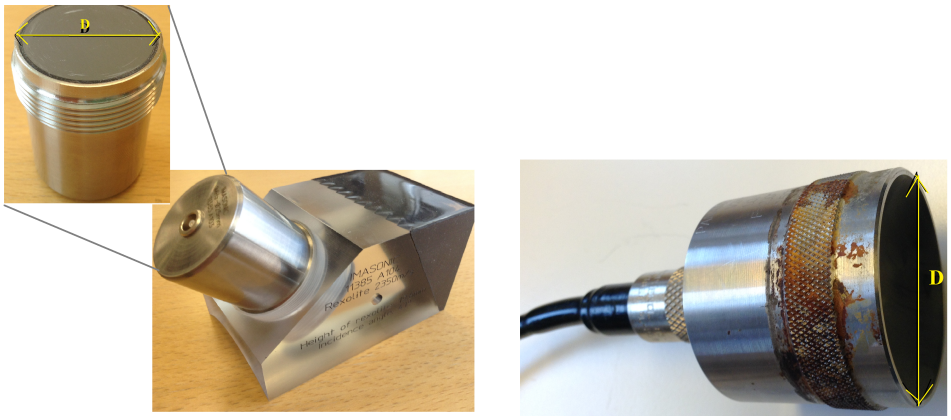

Figure 18: Single element ultrasound transducers.

3 Experiment Method

This section elaborates the practical measures undertaken to design the ultrasound transmitter system. The means for software and hardware that has been exploited for the work is explained briefly. The synthesizable VHDL (IEEE Standard) design for the ultrasound transmitter is discussed here. The design flow procedure undertaken in ISE tool for the design implementation in corresponding hardware is illustrated. Also the methods involved in hardware prototyping of different blocks of electronics surrounding the design is discussed in short.

3.1 Experiment Setup

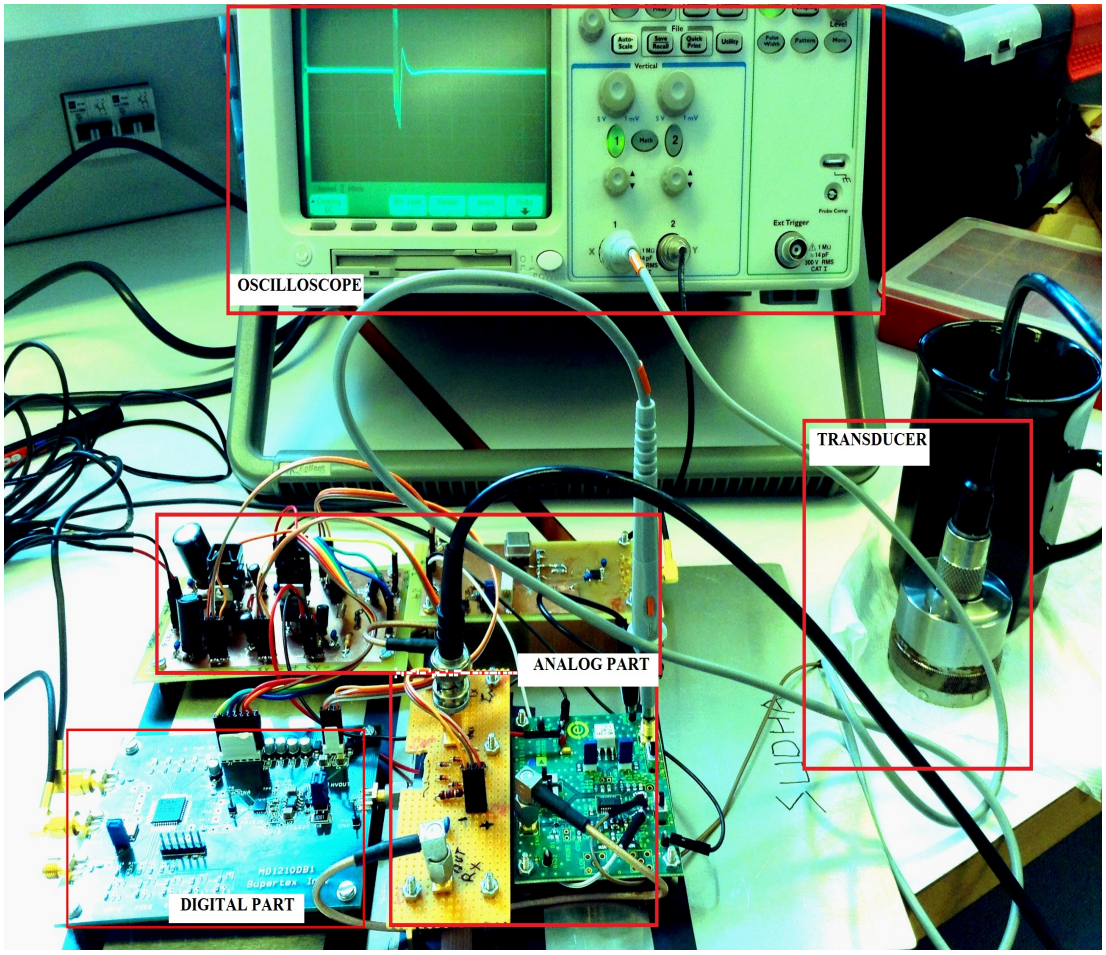

Figure 19: The Ultrasound Test Setup with the designed system.

The ultrasound test setup in laboratory is depicted in Figure19. The transducer i.e. the single element 1MHz to make ultrasound tests, the oscilloscope Lecroy LT342L (Teledyne LeCroy, Chestnut Ridge, New York, USA) and the water beaker to investigate the ultrasound measurement with the designed system are also included here. The output waveforms on the oscilloscope provides real time observation of the waveforms so that their characteristics can be properly analyzed. The objective of ultrasound trans-

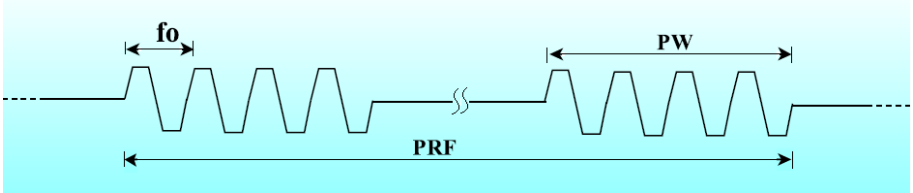

Figure 20: The output waveform of the transmitter.

mitter system design was undertaken in two parts; the digital design of the MD1210DB transmitter board and the analog design for electronics surrounding the ultrasound transmit-receive system. In the digital part, CPLD chip XC9572XL−5VQ44 embedded on the MD1210DB board, see Figure 7 was configured by using VHDL program to generate three level ultrasound pulses as shown in Figure 20. This served the purpose of the waveform generator for generating PW of desired ultrasound fo with the repetition frequency of PRF in the design. The analog design part includes the design, analysis, simulation or fabrication of the rest of the PCB blocks i.e. the power supply, the T/R switch, the oscillator and receiver gain shown in Figure 6). The receiver block in the same figure was attained by ultra-low noise preamplifier AD8331-EVALZ (Analog Device Inc.), as seen in Figure 12 whose functionality was analysed and implemented according to our system requirement.

3.2 Using ISE Tool

For the firmware design of the waveform generator, an EDA tool was essential in the design. As mentioned above in section 2.4, the implementation of the function generator, see PCB1 in Figure 6 was done by configuring the CPLD chip XC9572XL−5VQ44 embedded in the Supertex evaluation board MD1210DB. The VHDL programming file for the design was created using the ISE design suit V14.3 (Xillinx Inc.). The design flow of the ISE design tool for the design synthesis and simulation is depicted in Figure 21 which was adopted from [13].

In ISE design suite, initially the design properties for the target chip e.g device name, speed grade, HDL language being used was input in the target

chip properties as shown in Figure 22. The CPLD speed grade as given as −5 was chosen to be the correct value for accurate delay in timing simulation and the design synthesis, see figure 22.

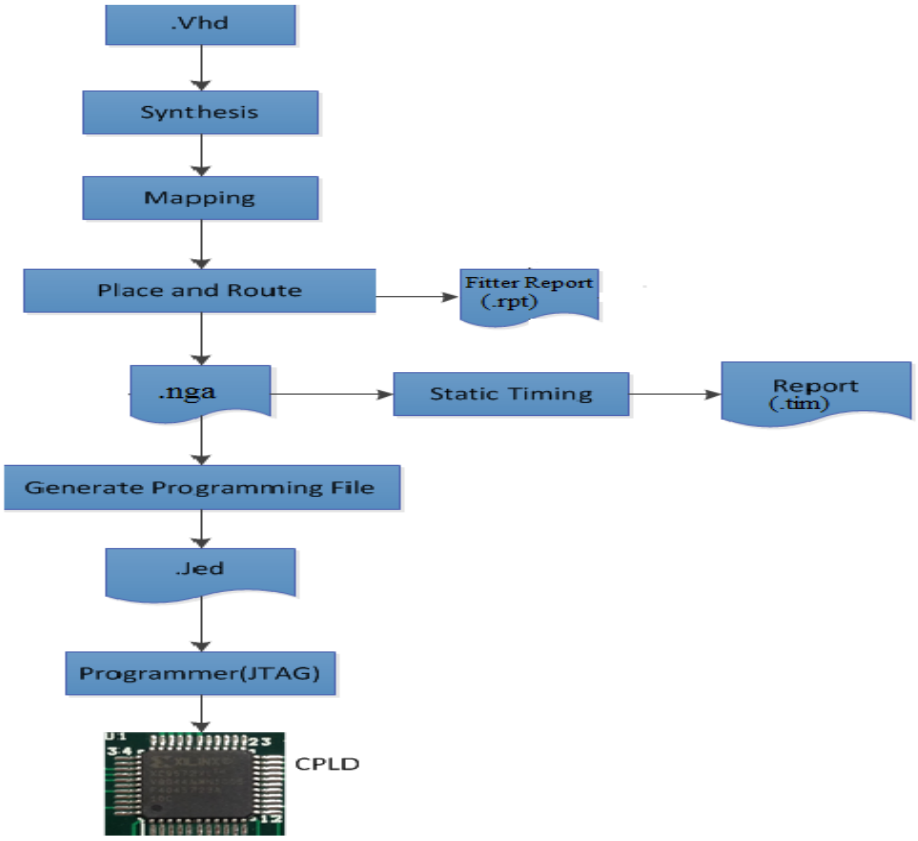

Figure 21: The VHDL design flow in ISE design suite.

As shown in Figure 21, first the VHDL code was written on the target CPLD to generate three level ultrasound pulses, see Figure 20 according to the design specifications of the MD1210DB board mentioned in section 2.2.1. Then the behaviour simulation was performed as the test bench to check for the proper performance of the design within the design specification. Some of the behavioural simulation results is depicted in the result section, see Figure 30. The synthesizable VHDL code was programmed in order to implement the design in the targeted device which is discussed in the following and the corresponding source code is attached in the appendix 6. This VHDL program in appendix (6) was interfaced on the CPLD by

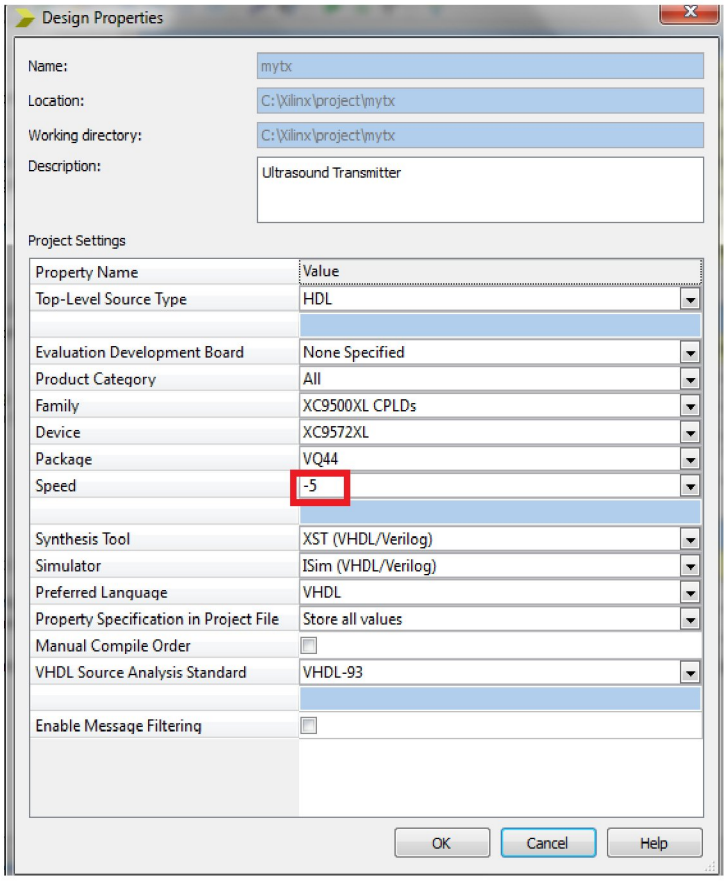

Figure 22: The design properties configuration of the CPLD chip in ISE design suite.

JTAG(IEEE 1532 standard for In-System-Programming (ISP)) interfacing provided in ISE design suite. The procedure of the design implementation in brief is as follows:

1. Open ISE design suite impact to configure target device.
2. Run impact.
3. Do boundary scan.
4. Initialize chain.
5. Program the target by programming with Joint Electron Device Engineering Council (JEDEC) (.JED) file (Global Standards for the Microelectronics Industry) created by the ISE design suite compiler.

The output waveforms INA and INB from the CPLD with the synthesized VHDL program was viewed in the oscilloscope first, see Figure 32. Finally, the high voltage output stage MD1213 (Xilinx Inc.) as the modification to the MD1210DB board and TC6320 IC were mounted on the MD1210DB board, see Figure 7 to complete the transmitter.

Performance Summary	
Min. Clock Period	10.000 ns.
Max. Clock Frequency (fSYSTEM)	100.000 MHz.
Limited by Clock Pulse Width for w.Q	
Clock to Setup (tCYC)	6.600 ns.
Pad to Pad Delay (tPD)	5.700 ns.
Clock Pad to Output Pad Delay (tCO)	6.900 ns.

RESOURCES SUMMARY

Macrocells Used	Pterms Used	Registers Used	Pins Used	Function Block Inputs Used
38/72 (53%)	98/360 (28%)	37/72 (52%)	4/34 (12%)	40/216 (19%)

Figure 23: CPLD timing report(up) and resources utilization(down) in ISE too.

3.3 Synthesizeable Design for Ultrasound Transmitter Electronics

The ultimate target of the project was to design a firmware in CPLD embedded in Supertex evaluation board MD1210DB (Xilinx Inc.) so that it can be the possible replacement for the analog power amplifier and function generators in the ultrasound transmitter system, see Figure 2. A synthesizeable VHDL model than can be implemented in the CPLD which will be able to transmit burst of ultrasound pulses of different frequency and number of cycles to drive the transducer in different application was programmed in the ISE tool source window. According to the design specification requirement for the transmitter mentioned under section 2.2.1 on page 17. The following algorithm was followed for VHDL coding in configuring the transmitter design:

1. The on board 40 MHz clock as the input clock and synchronizing clock.
2. The on board enable signal ena switch state as input sw signal.
3. Frequency division by 4 of the input clock to output the ultrasound frequency of 10 MHz.

4. Frequency division by 4000 of the ultrasound frequency to get the PRF of 2.5 KHz.

5. Pulse output INA, see Figure 8 of 4 cycles of the ultrasound frequency 10MHz repeating at the PRF of 2.5 KHz.

6. Pulse output INB, see Figure 8 of 4 cycles of the ultrasound frequency 10MHz repeating at the PRF of 2.5 KHz.

7. Route output INA to the CH1 output, see Figure 7 as sync output.

8. OE signal output high (1) or low (0) with the sw input high or low.

9. PWR signal output to power LED, see Figure 7 with the sw signal input.

As mentioned in the Algorithm 3.3, here the choice of ultrasound frequency f_o, pulse repetition frequency PRF and pulse length PW, see Figure 20 was chosen to be 10 MHz, 2.5 KHz and 4 respectively. This parameters can be changed in the VHDL program according to the requirements of the ultrasound investigation. Thus, the flexibility of adjusting the ultrasound ultrasound frequency f_o, the PRF and PW cycles has been provided separately in the VHDL program which is explained below.

The designed VHDL architecture was a synchronous digital model as they are simpler to code and creates less ambiguity in timing performance of the system. As shown in Figure 24 the synthesized VHDL design architecture consists of a MAIN module i.e. the top level hierarchy in the design which includes three other modules or components i.e. CLK, PRT, PW of the design. Here in the Figure, the process OE, ENA and PWR are present in the main module for enabling the transmission and for the on board LED indications. For example, when the board switch input SW is turn on (high), the enable signal OE to MD1213 and the LED output signals i.e. EN and PWR LED on the MD1210DB board are enabled accordingly. The PWR LED indicates green light when the CPLD is functioning properly, otherwise it shows yellow light indication. Likewise, the EN LED indicates pink light when the transmitter board is transmitting its output [1]. Similarly the mapping and fitting of the signals to the input-output ports was correctly applied as mentioned in section 2.4 by providing the appropriate user constraint file in the ISE design tool source window. This allows the fitting of the VHDL design correctly synthesized.

MAIN being the top level hierarchy which invokes all the components and process, see Figure 25. Here all of the modules in the design executes concurrently with the common reference clock input i.e. clk_hd. Figure

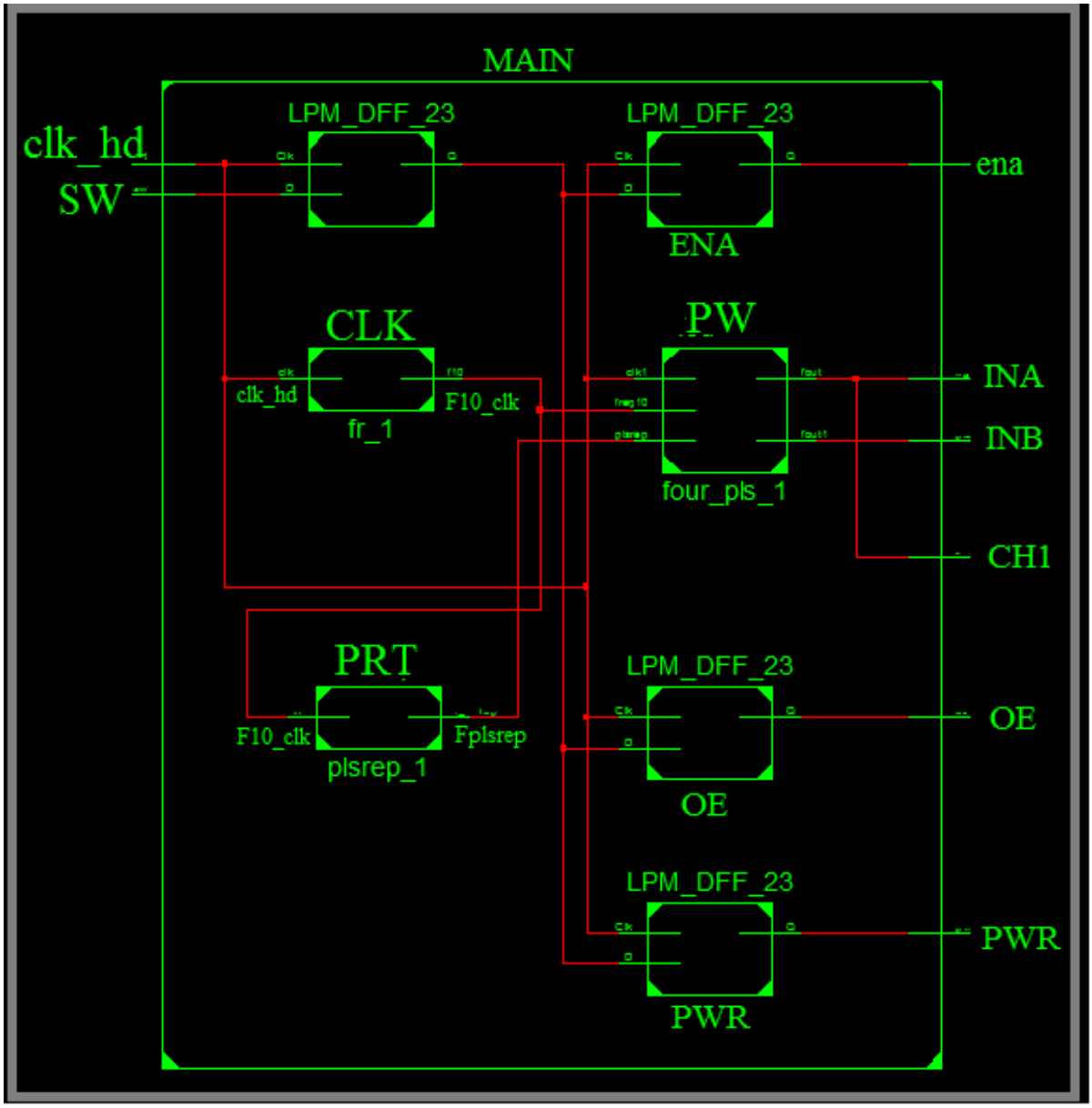

Figure 24: The overall RTL description of the VHDL design for the system.

25 depicts the flow chart of the MAIN module of this synchronous design. As mentioned earlier, the process OE to enable or disable the MD1210DB board i.e. to start or stop transmitting is synchronized with the reference clock (clock_hd) to avoid the metastability state while board input switch SW in Figure 7 is used [13]. Hence the MAIN module is enable or disable with this input sw corresponding to the parallel execution of the CLK, PRT

and PW modules, see Figure 25.

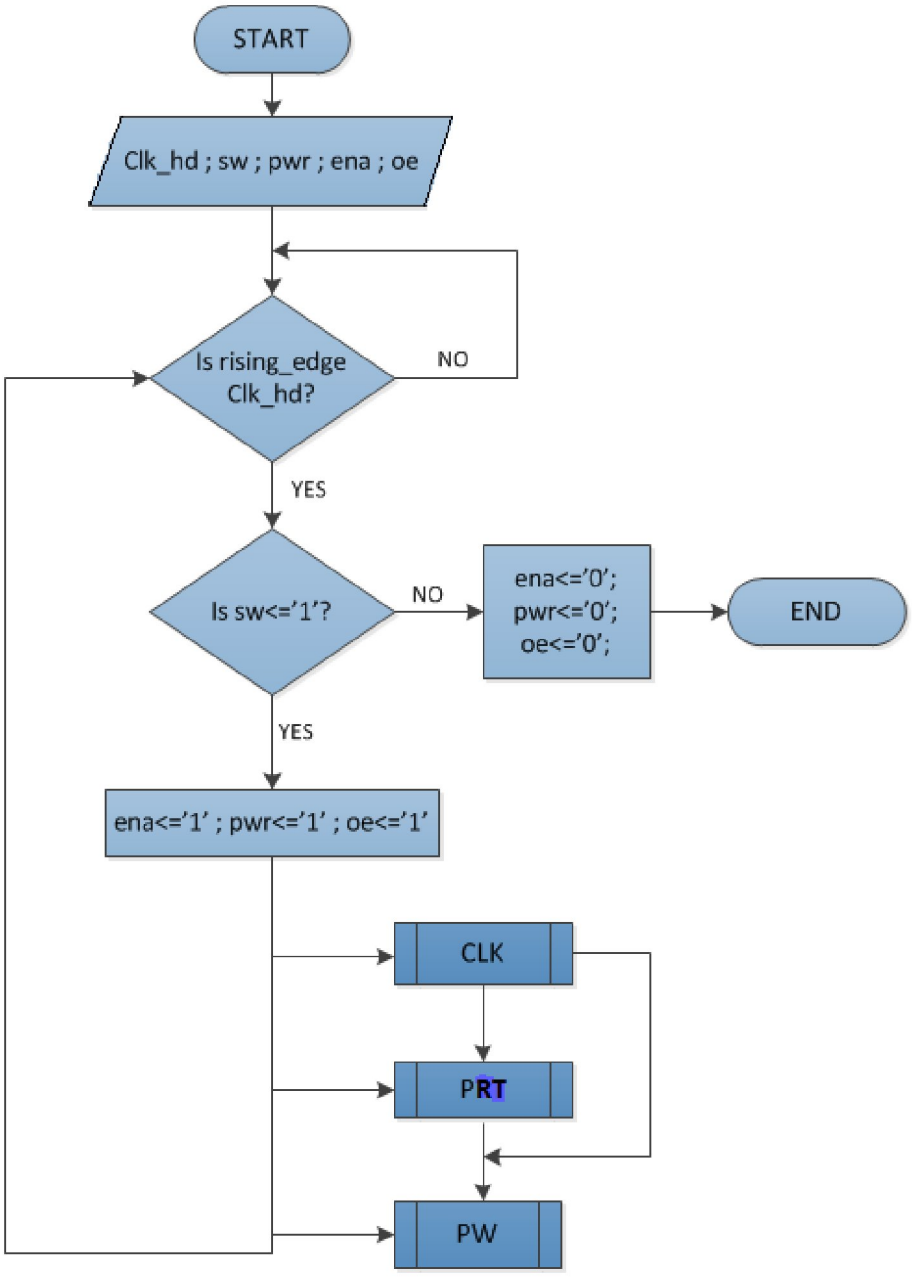

Figure 25: The flow char of the top level process MAIN in the design.

Figure 26 shows the flowchart of component CLK which is called from the top level module MAIN. It is responsible to output the ultrasound ultrasound frequency f_o i.e. 10 MHz in the design. This is performed here with frequency division by factor 4 of the input clock signal clk_hd of 40MHz by using a

synchronous counter Count_F10. As for the synchronous design, assignment to the signals only on rising of the reference clock is chosen in the program. This implies that the counter stage count_F10 is upto 2 for frequency division by factor 4, see Figure 26 or counter count_plsrep is upto 2000 for frequency division by factor 4000, see Figure 27. The input clock signal clk_hd is provided by the on board oscillator of 40 Mhz. It can also be supplied from oscillator and gain board as the external clock input i.e EXCLK when other ultrasound frequency is desired. This option to choose the on board oscillator or the external clock is provided on the evaluation board i.e. Jumper J7 in Figure 7. Here with the CLK model, the output ultrasound frequency f_o will be scaled by division of four accordingly with the frequency of the input clock signal i.e. the ultrasound frequency will be 1/4 of the input oscillation. For example for input clock of 40 MHz the output ultrasound ultrasound frequency will be 10MHz. This 10MHz sampling frequency can a good number for many application e.g. in tissue imaging were critical factor in ultrasound imaging is resolution [5]. But changing the local oscillation to 4MHz with EXCLK input, the ultrasound ultrasound frequency will be scaled down to 1MHz. This is a suitable ultrasound frequency in making Doppler investigation using ultrasound where strength of the ultrasound signal is more critical than the axial resolution [5]. This comes from the fact that trade-off exist between penetrating power and resolution of the RF wave with the frequency as mentioned in section 1.1.

Figure 27 shows the flowchart for component PRT which runs from the MAIN module. This component process the PRF by frequency division of the ultrasound frequency f_o by the factor of 4000 i.e. with the ultrasound frequency of 10 MHz, the PRF will be 2.5 KHz. Thus the ratio between PRF and ultrasound frequency f_o is maintained to 4000 which can be a good value for repetition of the samples taken in ultrasound processing. This ratio can be scaled up or down by changing the PRF i.e by changing the count_plsrep counter in PRT. However scaling of the PRF should be done carefully to maintain the range ambiguity limit as given by Equation 6 e.g. in Doppler velocity measurement, see section 1.1. When investigating high velocity Doppler measurement, high PRF are often desired [5]. In such situation this ratio can be scaled down i.e the PRF can be made much higher by changing the count_plsrep parameter in the VHDL code for PRT process.

The PW module is invoked by the MAIN module. It provides the final output stage of the CPLD i.e. INA and INB in Figure 8. The RTL description of the PW module is shown in Figure 28 where the synchronous digital system is described as set of state elements connected by the combination logic blocks. Here the DATAPATH manipulates the flow of signal with the control signal inputs e.g. f1, f2 from the CONTROLLER. The CON-

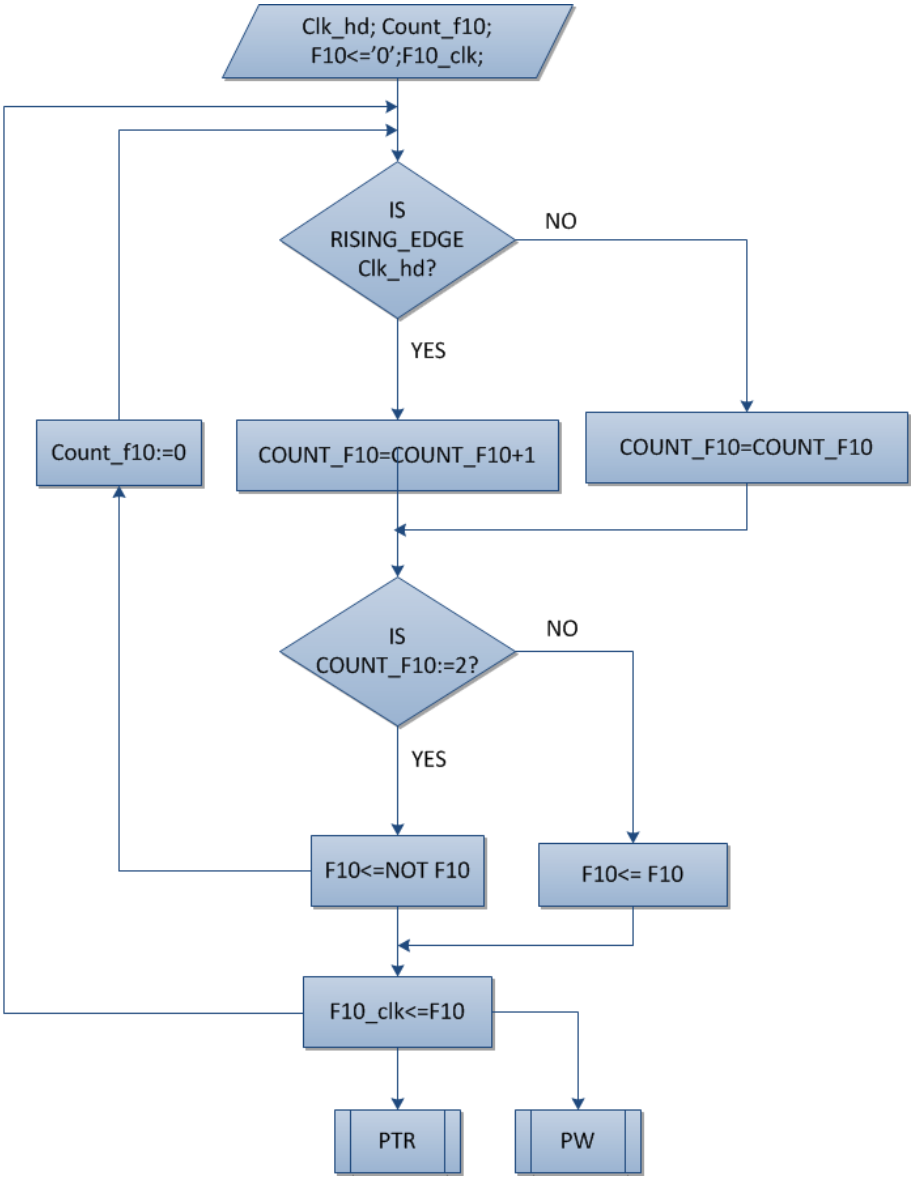

Figure 26: Flow chart of the CLK module use to get the ultrasound frequency in the design.

TROLLER here present a state machine which generates the control signals to sequence the signal flow in the DATAPATH. It provides windows f1 and f2 of length corresponding to the desired PW cycles i.e. the 4 cycles of 10 MHz ultrasound. This two windows f1 and f2 are synchronized with the reference clock i.e. clk_hd but are in exact delay of half of the ultrasound frequency i.e. 50ns in the design with each other, see Figure 32. So a synchronous counter

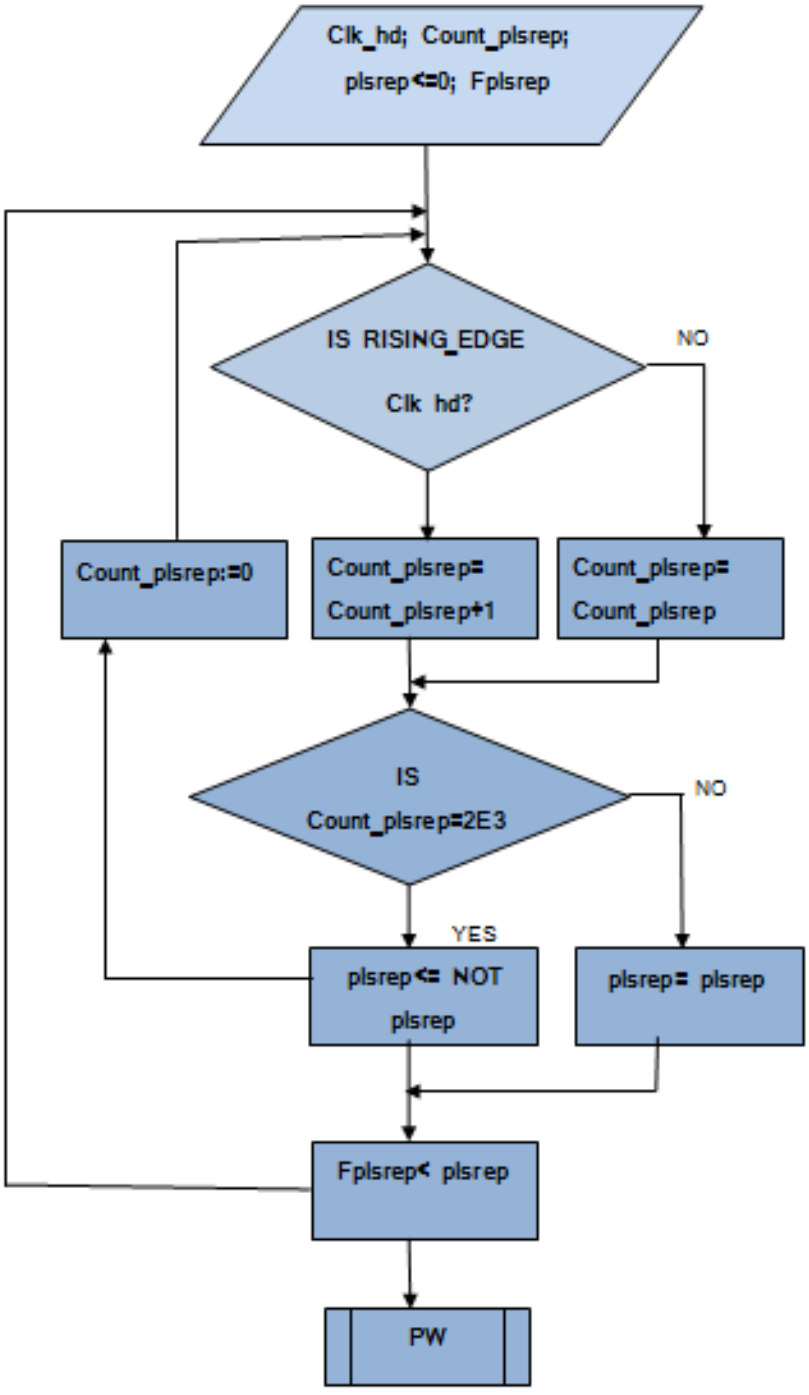

Figure 27: The flow chart for pulse repetition rate PRT module in the design.

process was suitable here to get the desired PW. The pulse waveform of 4 cycles in the PW process, was chosen as might provide good sampling in Doppler measurement. For applications where much longer cycles of pulses or narrower is beneficial, the length or the number of PW cycles can be increased to higher number e.g. 8 or 16 by adjusting the count_reg value in PW process model, see Figure 33. Likewise the PW cycles can be decreased for applications were shorter pulses or larger bandwidth is favourable.

Finally the two outputs of the CPLD i.e INA and INB as provided by the synthesized VHDL program discussed above are fed as input signal to MD1213 followed by TC6320. MD1213 when enabled by the OE output signal from the CPLD gives high voltage output HVOUT to drive the ultrasound transducer i.e. 22V peak-to-peak in this particular design.

3.4 Transmitter Board Design

[1] In the ultrasound measurement system, a function generator is desired to provide the excitation signal for the ultrasound transducer. The MD1210DB board in the designed system was aimed to supplement such function generators, see Figure 2. Figure 7 shows the waveform generator used in the designed system which is the Gerber file (De facto standard, RS-274X) copy of the Supertex's MD1210DB evaluation board. So it was the factory manufactured PCB prototype of the Gerber file in which the high voltage driver stages MD1210DB was replaced by MD1213. This replacement of the flip-chip IC i.e. MD1210DB for the MD1210DB was performed in the MD1210DB board, since MD1213 is claimed to be more robust and stable than MD1210DB by the manufacture (Supertex). Also the power MOSFET IC TC6320 was surface mounted on the MD1210DB board to complete the MD1210DB board circuit, see Figure 8. Then to get the desired PW signal out of the MD1210DB board, the embedded CPLD chip was configured with VHDL program as explained in the section 3.3. The multi-voltage supply i.e. 3.3V for input CPLD logic, dual 12V supply for driver and amplifier, see Figure 8 for the MD1210DB board was provided from the regulated power supply board. The safe loading at the output stage was maintained using the resistor R11, see Figure 7 during waveform investigation. Later on making the acoustic measurements, the 200Ω on board load resistor at output was replaced with much smaller loading of around 20Ω resistor to have appreciable signal level out from the board without any possible overloading. The resistor R11 although being a small value is essential to avoid any harm to the output stage and hence was not left short circuited.

3.5 T/R switch Design

The transmit-receive switch in the ultrasound investigation is desired to provide isolation between the high level transmitted signal and the low level received signal. Such switch provides the minimum noise interference between the signals for error free measurement and the protection of the sensitive output stage in the ultrasound transmit-receive system by isolating the transmit and receive part in the system.

The T/R switch in this particular design uses a passive diode circuit as a single channel switch which was referenced from the IC circuit MAX4963(Maxim Inc.) or LM96530 (Texas Instrument), see Figure 11. The dedicated IC for the ultrasound transmit-receive switch e.g. MAX4963, LM96530 are multichannel switch. Such switch could also have been used as an embedded IC in this particular design. Also active switches using transistor for better performance e.g. low ringing in the signals from the switch could have been employed for the purpose of the ultrasound transmit-receive switch. This was considered not very essential in this particular single channel transmitter design as they would demand for cost and complexity. So a passive diode switch circuit being simple and readily configurable was chosen as a transmit-receive switch in this design. The single channel passive diode circuit, see Figure 11 was simulated and its prototype version was made in PCB using Proteus 8 professional (Labcenter Electronics Ltd., North Yorkshire, England). The simulation and hardware prototyping of the T/R switch in Proteus software is briefly explained below:

- **Simulation of the T/R switch:** To understand the working principle of the T/R switch passive circuit its simulation was performed first in Proteus. Figure 38 attached in the Appendix shows a simulation result for the T/R switch in Proteus.

- **Testing of the prototype board:** The T/R switch in this design was required to be operated in high frequency of few MHz i.e. 1 MHz or 10MHz in this design with high voltage signal of 22V peak-to-peak by providing clipping at the receiver side. It was desired to test the board with a high voltage input from the function generator or the MD1210DB board. So that the possible output could be observed before implementing in the ultrasound system signal chain. The testing was done by providing the high voltage pulses from a laboratory function generator and the viewing of T/R switch output-input was performed in the oscilloscope.

3.6 Oscillator and Gain Board Design

The local oscillator and gain circuit, see Figure 14 was desired for two purpose. First to provide the oscillation of desired frequency for the waveform generator i.e. Figure 7. Second to supply the same common oscillation also for the ADC board i.e Figure 17. This was an essential feature to be included for making this designed system flexible in Doppler Ultrasound measurement purpose. So the prototype PCB to have local oscillator of desired frequency as triggering input to the MD1210DB board and voltage gain from 0V to 1V for LNA gain of the ADC was designed. Figure 14 shows the designed oscillator and gain board. This board is the improved version of the circuit, see Figure 37 in the Appendix used in the ultrasound measurement system, Rikshospitalet University Hospital (Oslo, Norway) to provide similar function of oscillation and gain voltage. The modification done in the circuit was a high speed triple video buffer IC AD8074 (Analog Device Inc.) which provided three output stages with a proper 50Ω load termination. The Proteus simulation of this circuit, see Figure 15 was not performed as the AD8074 IC was not programmable in the Proteus. So the testing for the functionality of this circuit was done directly on hardware using an oscilloscope.

Here the local oscillator circuit part comprises of a crystal oscillator AEL1200CS (AEL Crystals Ltd, Salfords, UK) of 4 MHz frequency, a resistive divider circuit and high speed three input buffer AD8074 to have 3.3V local oscillation output from the oscillator and gain board, see Figure 14. One of its outputs was provided as high speed input signal logic for the MD1210DB board while one was provided as the clock input for ADC. The value of the resistor R1 and R2 on the board, see Figure 15 were chosen by using Equation 9 to have the desired voltage level of 3.3V for the local oscillator output.

$$Voltage\ output = Voltage\ input \frac{R2}{R1 + R2} \tag{9}$$

Since the crystal oscillator AEL1200CS in Figure 14 being Transistor Transistor Logic (TTL) logic requires current sink of approximately 10mA at its output [**?**], the resistance value of R1 and R2 was choosen to be approximately 330 Ω and 680 Ω respectively. So as to get 3.3V output from the input supply of 5 Volts as given by Equation 9. The resistors value for the LNA Gain circuit part of this oscillator and gain board was also choose using the same Equation 9 to get the output voltage of 0V to 1V, selectable by the potentiometer included in this resistive network i.e. the LNA Gain part in Figure 15.

Proper care was given also in the prototyping of the PCB layout for this board circuit e.g. for routing the ground plane and power distribution [18]. A wide solid ground plane was provided considering the reference and return paths for both inputs and outputs of the buffer AD8074. It was made wide enough to keep its impedance at minimum and the input-output signals were routed in a straight path to minimize any parasitic . The power plane was also made wide to allow minimum inductance necessary for providing high-slew-rate to the signals.

3.7 Power Supply

The power supply board in the ultrasound system is required to supply the necessary power with minimum noise as the inputs of ultrasound measurement are sensitive to noise. The power supply board to power up the designed ultrasound system was made using linear voltage regulators and capacitors as shown in Figure 16. Here a conventional linear regulator circuit with low noise was chosen over the available modern switch regulators which might introduce some noise levels as discussed in section 2.2.5. The linear, noiseless and stable regulator supply designed for stable functioning of the overall system provided the supply of 3.3V, 5V dual and 12V dual from a 15V wall adapter i.e. AC to AC adapter. This fulfiled the designed system specifications for the power supply board given in Table 3, see section 2.2.5. The outputs from this designed power supply board were viewed under an oscilloscope to check for the linearity and AC ripple. A simple block diagram illustration of this design is shown in Figure 29.

The high voltage power supply board i.e. PCB5 in Figure 6 is required for the high level excitation of the ultrasonic transducer. As for this prototype design, the design of PCB5 was skipped although the headroom for high voltage level of 200V peak-to-peak could have been used in the pulse generation from the pulser board ([1]).

3.8 Ultrasound Receiver

[2] A receiver circuit is desired in the ultrasound measurement signal chain to receive the ultrasound echoes back from the ultrasound transducer. It should be able to output the RF signal suitable to be used in further signal processing e.g. analog to digital conversion. The received ultrasound echoes are the low level signals which are directly related to depth of the target or time interval between transmit-receive. So the receiver circuit should be able to give appropriate TGC or VGA for this low level signals. The minimum

noise during the amplification of these signals is required for maintaining the good signal level in the following signal path.

To meet this requirement an assembled and tested evaluation board AD8331-EVALZ (Analog Device Inc.), see Figure 12 was used as the ultrasound receiver in this design. The LNA and VGA of AD8331 was enabled on the evaluation board to complete the low noise amplification signal chain. The on board jumpers pins, see W5 and W6 in Figure 12 were short circuit to connect the AD8331 outputs with the evaluation board output pins [2]. The linear input supply of 5V was provided from the power supply board. The gain voltage Vgain was supplied from the gain output LNAOUT of the oscillator and gain board, see Figure 14 which could be adjusted between 0V to 1V as explained in section 3.6. The UP gain option was selected for GN_SLOPE in making gain increment directly proportion with the gain voltage. The GN_HI_LO option was chosen to be HI (high) for high gain mode. The Voltage Common Mode (VCM) option on the evaluation board was left floating while observing the output waveforms in the oscilloscope. The input signal to the receiver was provided from the T/R switch to ensure its safe mode operation. The (SubMiniature version A (SMA)) connectors were used in this board to ensure good signals routing between thePCBs and for output observation in the oscilloscope.

3.9 ADC

[21] The ADC for the ultrasound measurement signal chain provides the digitized RF signal lines. The RF lines so produced can be further processed as desired for different application using a suitable interfacing software e.g LabView and thus can be adopted for desired ultrasound measurement.

In this design the digitization of the signal out from the LNA was done aided by a dedicated ADC package for RF signal, NI PCI-5122(National Instruments Corp., Austin, Texas, USA), see Figure 17. It is a 14-bit digitizer with sample rate of 100 mega-sample per second (MS/s). This multi-record feature of NI PCI-5122 along with the common sampling clock input from the oscillator circuit is beneficial during the Doppler measurement signal processing. The digitized received echo signals outputs from this ADC used in the design was demodulated by implementing appropriate VI program in the LabView software provided in the laboratory computer of Hgskolen i Buskerud og Vestfold (HBV) and the output waveform were observed in the PC. The Low Voltage (LV) virtual instrument allowed for the oscilloscope view of 1MΩ AC, 50Ω or 1MΩ DC and ground coupling and also the M-Mode view. Its features were used in making some basic ultrasound measurement with the design system i.e measuring the back-scattered echoes from the

bottom of a water beaker using a 1MHz single element transducer.

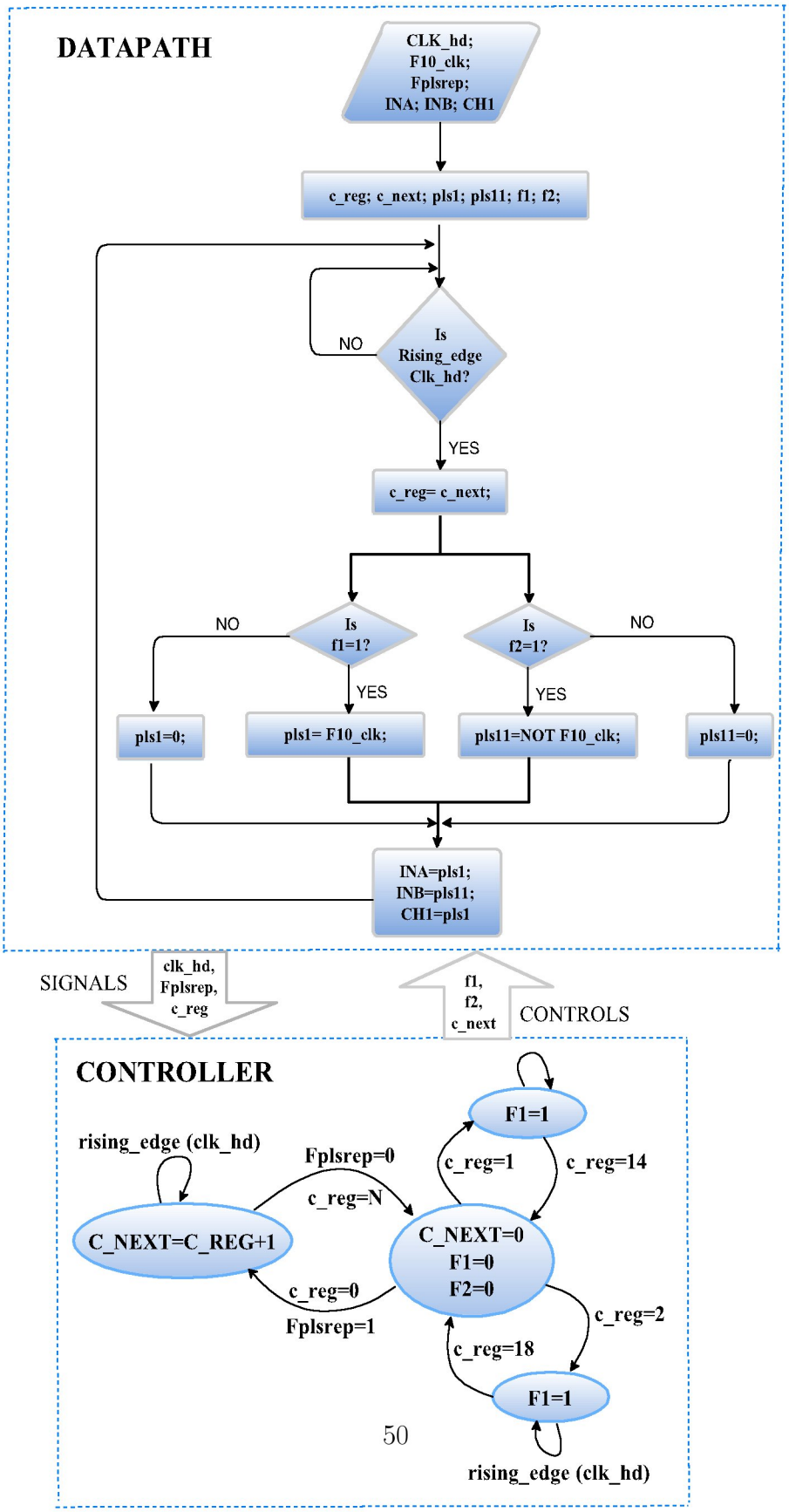

Figure 28: The pulse lenght of four cycles.

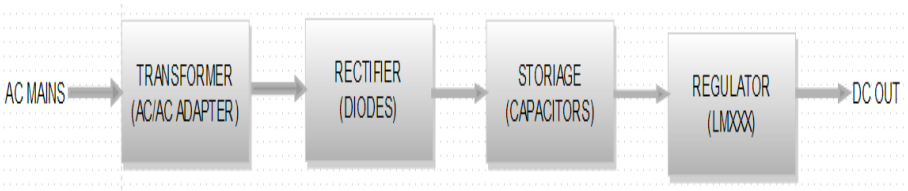

Figure 29: The regulated power supply board block diagram.

4 Experiment Result

This section presents the outcome of the task undertaken for ultrasound system transmit-receive electronics and result of some acoustic measurements performed with the designed system.

4.1 Simulation In ISE Tool and Digital Design with VHDL

Figures 30 shows the behavioural simulation result for the four pulse waveform designed by VHDL program in the ISE tool. It also shows the signals like reference clock i.e. clk, and the ultrasound resonance frequency of 10 MHz i.e. fclk. The two outputs of four cycles of the same resonance frequency, which are the inverse of each-other and also in exact phase but half cycle delay with each-other i.e. pls_1 and pls_11 are also shown in the figure.

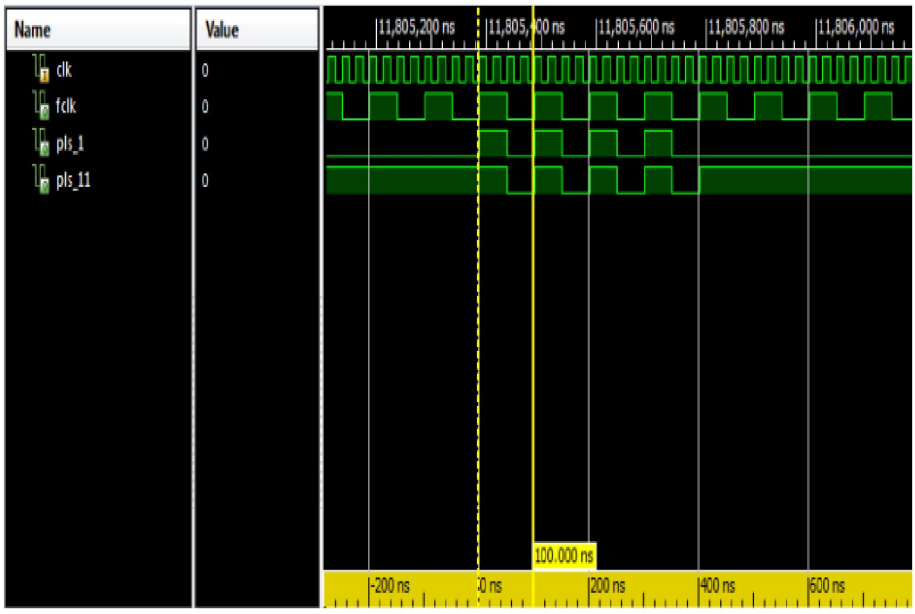

Figure 30: The behaviour simulation of the beamformer for the for the four pulse cycle.

Figures 31 shows the behavioural simulation result for eight cycles in the ISE tool using the same VHDL program but changing the pulse length from four to eight.

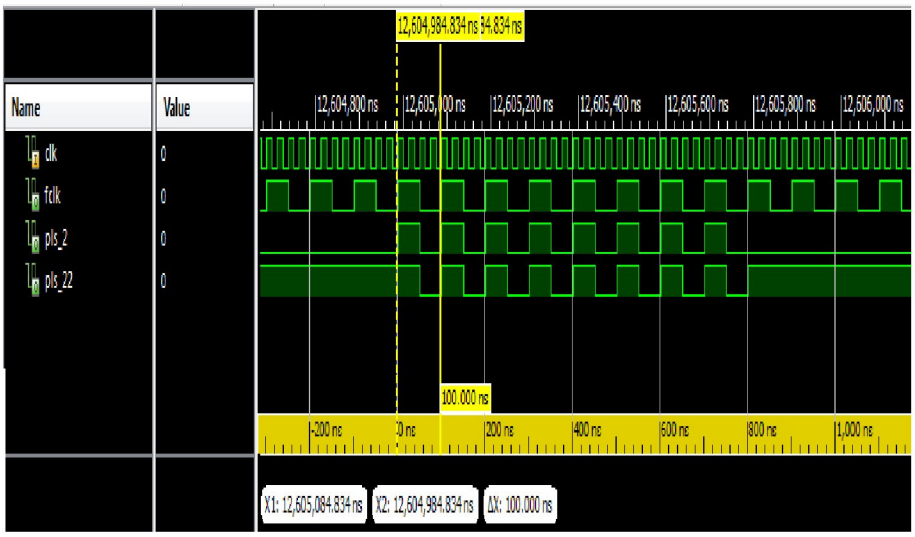

Figure 31: The behaviour simulation of the beamformer for the eigh pulse cycle.

4.2 Real Time Measurement Using Oscilloscope

Figure 32 shows the output waveforms from the CPLD observed in the oscilloscope which shows the same outputs as given by the simulation result in Figure 30.

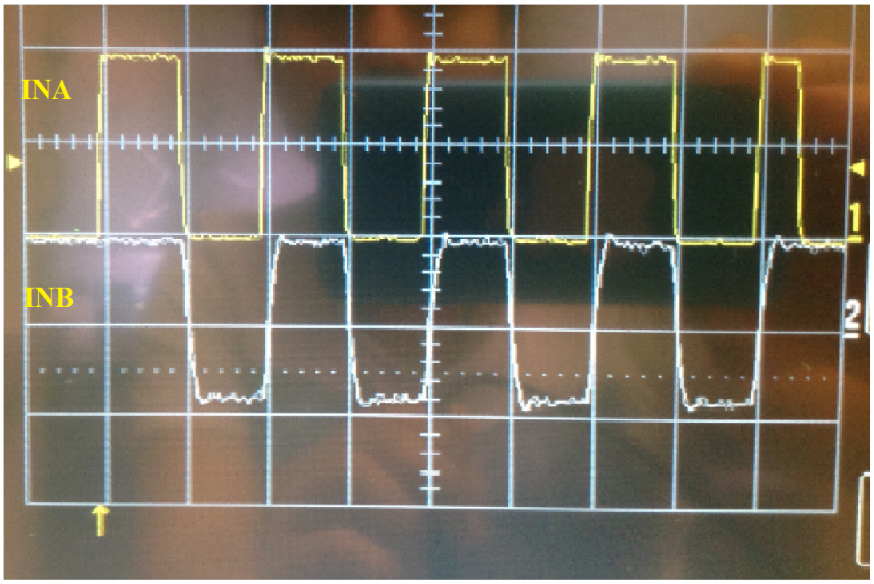

Figure 32: The output from CPLD for 4 pulse cycle.

Figure 33 is the outputs observed under the oscilloscope which corresponds to pls_1 and pls_11 outputs shown in the Figure 31. The result here is not a perfect pulse because a normal oscilloscope probe were used in the viewing instead of the higher attenuator probe for RF signals observations

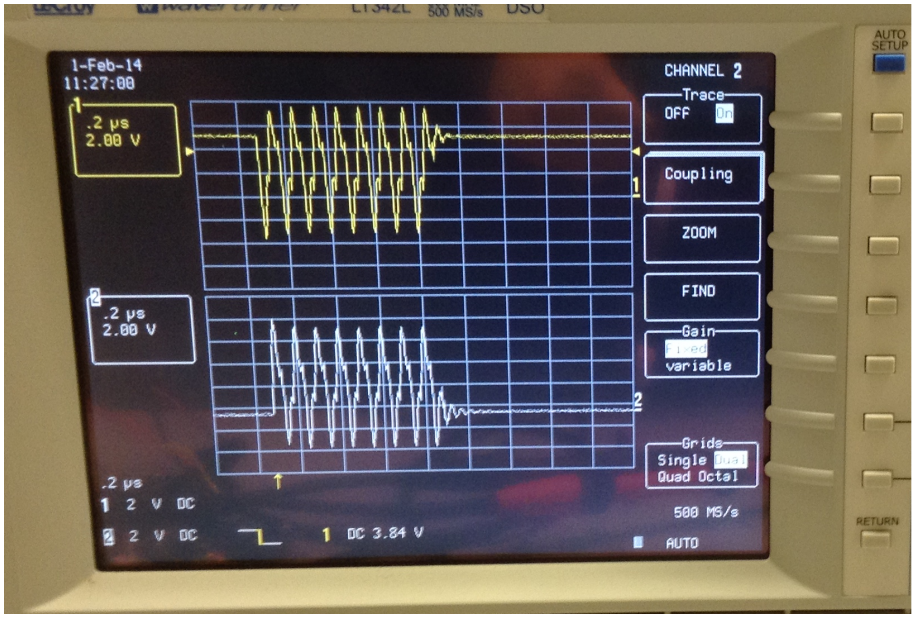

Figure 33: The output from CPLD for 8 pulse cycle.

Figure 34 is the output from the oscillator and gain board i.e.CLK in the Figure along with the MD1210DB board output i.e. HVOUT in the Figure. The CLK here is the low level signal of 3.3V peak-to-peak with oscillation of 40 MHz while HVOUT is the high voltage signal of 22V peak-to-peak with four cycles of 10 MHz oscillation.

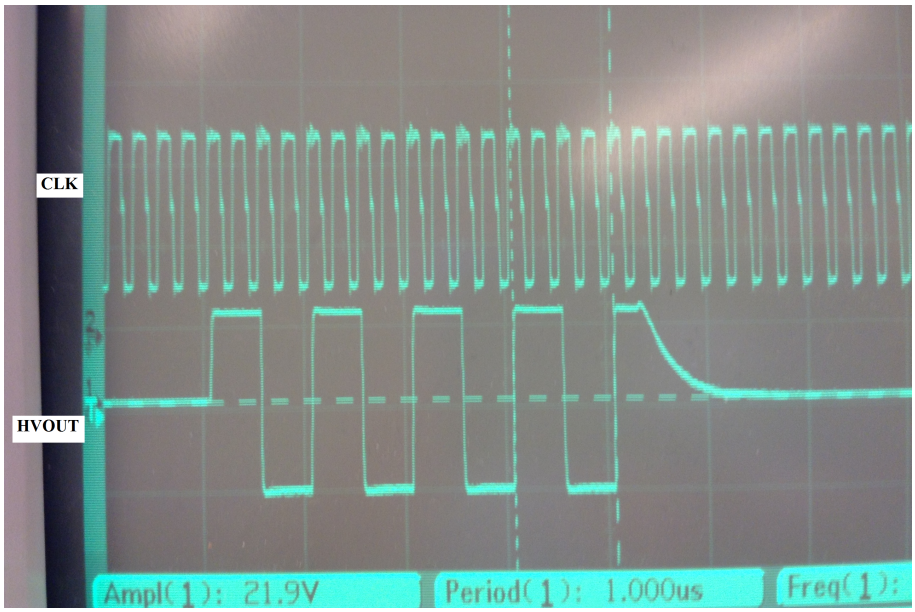

Figure 34: The AC coupled local oscillation output (top) from PCB4(Figure 6) and the HVOUT (bottom) from PCB1(Figure 6).

4.3 Measurement Interfaced with PC

Figure 35 shows the LabView result of ultrasound measurement done under the same setup shown in Figure 19 using 1 MHz single crystal transducer. Referring to the Channel0 output in the Figure 35, the transducer excitation signal (left) is followed by the echoes from the bottom of the water beaker along with some small reverberation that are visible.

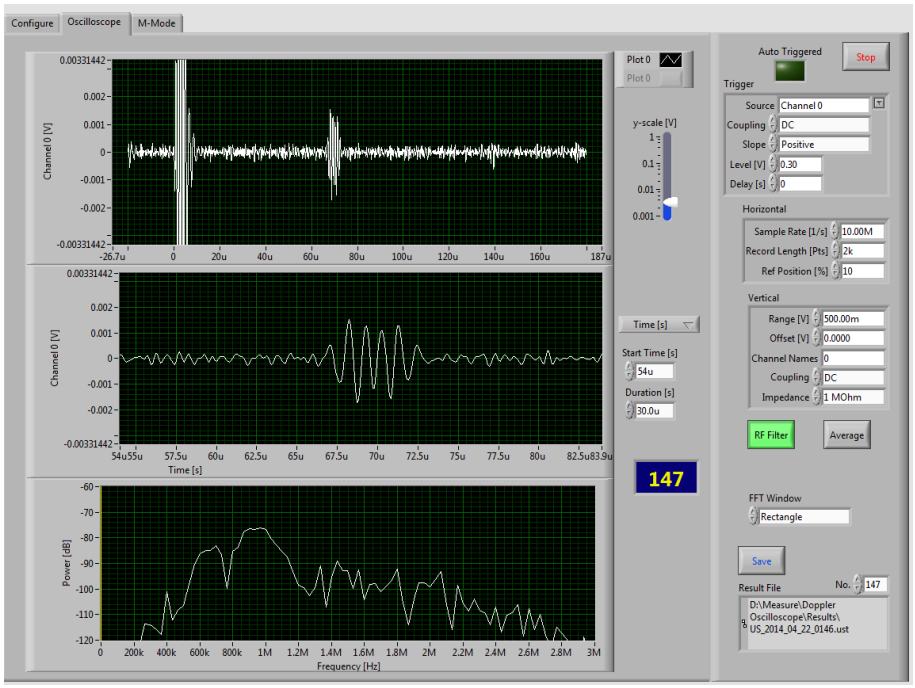

Figure 35: Ultrasound investigation using 1 MHz single element transducer in water.

Figure 36 shows the motion mode (M-mode) result in LabView of the same result in Figure 35. Here the wavefornts of the backscattered echoes from the water beaker bottom surface can be seen. The wavefronts seen here are weak as we have used small high voltage excitation of 12V dual supply for transducer excitation.

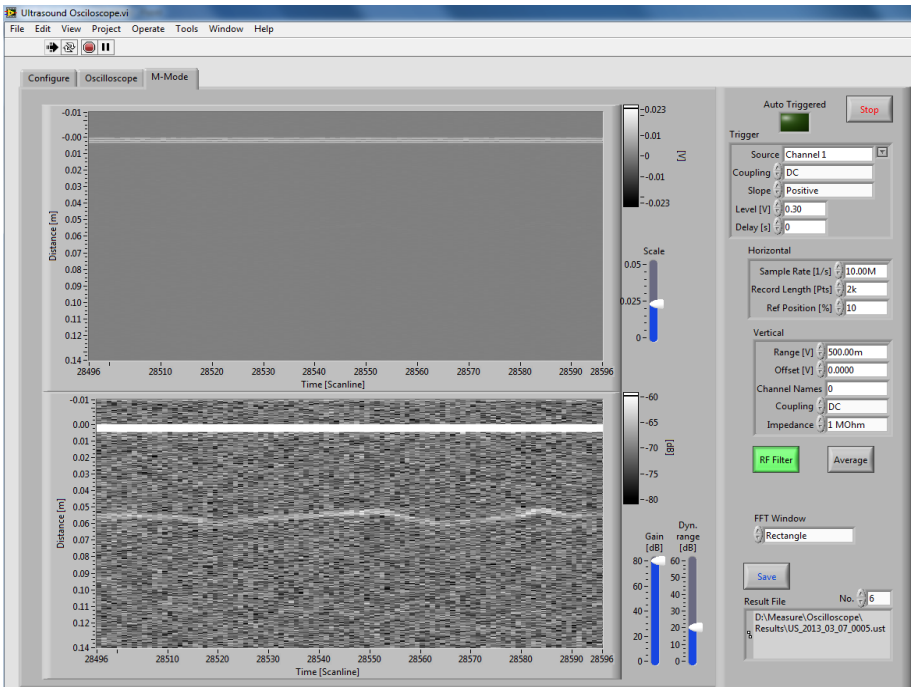

Figure 36: M-mode ultrasound investigation for 1 MHz single element transducer in water.

5 Discussion

Ultrasound Transmitter Design Using VHDL

The goal of making a digital circuit using VHDL was to make a flexible and miniaturized ultrasound transmitter system. The transmitter design could have been implemented entirely in hardware but this would call for numerous counters for clock, multipliers and comparators in the design. So more flexible approach in the transmitter design by firmware configuration on CPLD XC9572XL−5VQ44 was chosen. Here the resources provided by the CPLD i.e 34 input-output pins, 72 registers for storage and 216 flip-flops for functional inputs, see Figure 23 can be exploited in an optimum way for fulfilling the design requirements. An FPGA could also have been used for this purpose which could provide larger resources i.e. more numbers of flip-flops, external memory, input-output pins for the design. The trade-off could have been the cost for a CPLD and an FPGA. Moreover, the Gerber file copy of the Supertex MD1210DB MD1210DB board already had the layout for embedded CPLD XC9572XL−5VQ44 pin-outs. So it was convenient to use the CPLD for the single channel MD1210DB board design.

Understanding of the HDL and digital circuit was important for the transmitter designed in the firmware. Although there were numerous possibilities to design the desired hardware using the digital circuit, the ultimate goal remained in programming a synthesizable design that can be implemented on the targeted chip XC9572XL−5VQ44. For this purpose synchronous system design using VHDL provided simple design with less timing ambiguity. Here, all the processes in the system was triggered with a single reference clock transition. So the inherent concurrent VHDL code synchronized with a single reference clock signal provided the output signal in phase with the referenced clock signal. This identical sampling clock and transmitter signal is also an advantage for Doppler velocity measurement. The constant propagation delay on the signal assignment set by the corresponding hardware is 6ns [1] which can be consider not critical for normal applications e.g Doppler measurement or tissue imaging. Since the outputs and the sampling clocks are in exact phase with each other. The summary of the CPLD resources exploited in the design can be seen in Figure 23 which shows enough resources available in the CPLD if further modification in the design is necessary.

As digital design optimization remains in the domain of either performance speed or resources utilization. So trade-offs are always accounted between different parameters according to desired requirements. The flexibility of adjusting the ultrasound ultrasound frequency fo, the PRF and PW cycles has been provided separately in the VHDL program.So that other

values for these parameters could be employed according to the application requirements, than the one specified in this design i.e. 10 MHz ultrasound ultrasound of 4 cycles in the constant repetition of 2.5 KHz. For instance, here the ratio between the PRF and ultrasound ultrasound frequency as given by the PRT process has been chosen to be 4000 which is a good value for repetition of the samples taken in ultrasound processing. When investigating Doppler measurement e.g. higher velocities of fluids in pipeline, this ratio can be scaled down to 1000 or 2000 along with careful consideration of aliasing limit set by Equation 6 for the high PRF. Likewise, the PW of 4 pulses provided in PW process might provide good sampling in Doppler measurement. For applications where much higher sampling is beneficial, the length or the number of PW cycles can be increased to higher number 8 or 16 as described in 3.3.

Synthesis With ISE Tool

The ISE tool was use for VHDL programming to configure the CPLD chip embedded in the MD1210DB board for the design of the waveform generator. It was used to output the signals INA, INB and OE from the CPLD according to the design specifications mentioned in section 3.3. Since there are different ways in designing the ultrasound transmitter in the PLD. It was noticed that all the design procedure was not always synthesizable for implementation in the target device. In some design approach e.g. using an inverter to get the delay between outputs INA and INB as half the cycle of their resonance frequency could give correct output observation during simulation in the ISE design suite. But the corresponding output as the one observed in the simulator could not be archived while in viewing the output in real-time using an oscilloscope. Here only the inversion between of the outputs was observed but not the delay of half cycle of their resonance frequency. This might be because the the inverters implemented in the CPLD hardware can provide the physical delay corresponding to the propagation delay of the flip-flops which is as low as 6ns [1]. So realizing the delay of half the cycle of the resonance frequency i.e. 50 ns in this particular design by using such inverter were unable to provide the desired delayed output in the real hardware although of the correct outputs were provided and the successful synthesis of the corresponding VHDL program in the ISE simulator.

Also learning of the VHDL language provided some glimpse in the digital hardware design of the electronic system. As for instance in this particular design, it was noticed that some of the VHDL statements e.g. wait for, wait until that might sound appropriate to provide the desired delay between the required output signals are not compiled by the ISE 14.3 Design

suite. These statements are only for testing in the ISE test bench i.e. the behavioural simulation. By learning the VHDL language, it was also noticed that while configuring the single edge flip-flops of the CPLD, the valid signal transition is only for a single edge transition of the referenced clock for the synthesis purpose. If both edge transition of the referenced clock signal is exploited then error will be encountered during synthesis as the signal can hold its value only during a single transition for these flip-flops. This again implies that the the required delay of half cycle i.e. 50ns in this design between the two outputs INA and INB could not be achieved while trying to output them using the both transition edge i.e. the rising edge and the falling edge of the resonance frequency i.e. 100ns in this design. Hence realizing the synchronous counters for programming or buffering the delay between the output signals was one of the solutions. Further, the violation of metastability criteria as explained before on page 40 will cause the fitting error i.e. signal mapping to the desired destination ports. Moreover new options and different approaches to the design requirements should always be reached out for optimum resources exploitation and better performance.

Analog PCB Design

The analog design circuits i.e. PCB2, PCB4, PCB6 were mostly the upgraded version of some already working circuits e.g. ultrasound instrumentation used in Rikshospitalet University Hospital for cardiac monitoring during surgery and some existing standard dedicated ICs in ultrasound system e.g. LM96530. The oscillator and gain board as designed to have identical input clock signal to the transmitter and the sampling clock for the ADC gave appreciable output with the AD8074 buffer. The transmit-receive switch was desired to provide isolation between the transmitted and received signals in ultrasound investigation. The multichannel IC switch like LM96530 or MAX4963, manufactured from established companies could have been used as the T/R switch. Using such available switches IC would have been more complicated since only a single channel switch was required in this particular design. Here the passive diode circuit was easy to implement with few simple components i.e diode 1N4148 (NPX Semiconductors, Eindhoven, Netherlands). Also those diodes were ideal for high speed application and providing better off isolation. So the passive diode circuit designed using high speed switching diodes fulfilled the requirement for the single channel transmit-receive ultrasound system designed.

6 Conclusion And Future Work

Digital Design of Ulrasound Transmitter

The waveform generator to transmit three level bipolar pulse waveform for the ultrasonic transducer excitation was accomplished successfully by designing a frimware in xc9572xl_vq44 CPLD. The waveform generator with the CPLD firmware along with MD1213 and TC6320 served the purpose of the function generator and power amplifier in the conventional ultrasound system instrumentation. This was done by making a synchronous digital design which comprises of cascaded sequential resistors along with the combination logic required for the design. Designing the system in digital hardware provided development time consumption and had offered means to alter the design without any change in the real hardware. The future work on the transmitter design could be to make the VHDL programme more efficient for optimum use of the CPLD resources. The PW of 4 cycles could be maintain for 8 or 16 cycles for higher sampling. Also possible replacement of the CPLD by an FPGA could enhance the available resources for the digital design. Then it might be possible to design multiple channel ultrasound transmitter with a single FPGA chip along with the multiple driver (MD1213 +TC6320) stages per channel designed.

Analog Electronics

The PCBs prototyping for the electronics surrounding the ultrasound transmitter designed seem to work within the design specification. The line regulated power supply board provided low noise level with a low heat dissipation that could be removed with heat sinks. The oscillator and gain board with the high speed buffers(AD8074) provided the driving signal for the MD1210DB board, synchronizing clock signal for the data acquisition board and proper load termination of 50 Ω at its outputs. The use of such buffer instead of designing a local oscillator was beneficial for the system as it saved time and space. The transmit-receive single channel analog switch provided appreciable switching and isolation of the high level output signal to the transducer and low level receiver's input signal. As for the further outlook on the analog hardware of the system, the circuit for matching capacitive impedance of the ultrasound transducer could be designed and added in the system. The 100V dual supply as the high voltage supply from the power supply board i.e PCB5 in Figure 6 could be designed to have optimum signal level to drive the ultrasound transducer. The analog T/R switch could be made multichannel for different transducer excitation or can also be replaced by multichannel

IC switch e.g. MAX4963, LM96530 for better space consumption and performance.

Appendices

A.VHDL Source Code

```
-----------MAIN
   ----------------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE ieee.numeric_std.all;
USE ieee.std_logic_unsigned.all;

entity main is
        port(
             clk_hd:in std_logic;
                  sw:in std_logic;
                  pls_1,pls_11:out std_logic;
                  pwr,en,oe:out std_logic;
                  trg:out std_logic
                  --pls_2,pls_22:out std_logic
                  );
end main;

architecture Beh_main of main is

        component fr is
         port (
              clk:in std_logic;
                        f10 : out std_logic
                        );
        end component;

        component plsrep is
        port (
             f_clk:in std_logic;
                  f_plsrep :out std_logic
                   );
        end component;

                  component four_pls is
     --generic(N:integer:=3);
```

```
            port(
        clk1,freq10: in std_logic;    ---10mhz
                  plsrep:in std_logic;         ---2.5khz
                  fout,fout1:out std_logic
        );
        end component;

       signal p,x,y,w,z:std_logic;

    begin
    fr_1:fr port map(clk_hd,w);      -----POSITIONAL
       MAPPING
    plsrep_1:plsrep port map(w,z);
    four_pls_1:four_pls port map(clk_hd,w,z,x,y);
    pls_1<=x;
         pls_11<=y;
         trg<=x;
switch: process(sw,clk_hd)          ---%%%PROCESS TO
   AVOID METASTABILITY STATE WHILE BOARD INPUT SWITCH
   ARE USED
        variable tmp_pwr:std_logic;
                  variable tmp_en:std_logic;
                  variable tmp_oe:std_logic;
        begin
        if rising_edge(clk_hd)then
                     pwr<=tmp_pwr;
                          en<=tmp_en;
                          oe<=tmp_oe;
                          tmp_pwr:=sw;
                          tmp_oe:=sw;
                          tmp_en:=sw;
                  end if;
       end process switch;
end Beh_main;
--
   ------------------------------------------------------------------


--------CLK-----------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity fr is
       port (
            clk:in std_logic;
                 f10: out std_logic
                 );
end fr;

architecture behav_fr of fr is
       signal f:std_logic := '0';
begin
     process(clk)
          variable count: integer range 0 to 5;
          begin
          if (clk'event and clk='1')then
                  count:= count+1;
                  if(count=2)then      ---40MHz to 10
                     MHz--
                  count:=0;
                  f<=not f;
                  end if;
     end if;
     end process;
     f10<=f;
end behav_fr;
--
   ------------------------------------------------------------


----------PRT-------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity plsrep is
       port(
            f_clk:in std_logic;
                 f_plsrep :out std_logic
                 );
end plsrep;

architecture bev_plsrep of plsrep is
       signal f:std_logic := '0';
```

```
begin
       process(f_clk)
       variable count: integer range 0 to 5E3;
            begin
            if (f_clk'event and f_clk='1')then
                count:= count+1;
                          if(count=2E3)then       ---10
                             mhz to 2.5 khz
                             count:=0;
                             f<=not f;
                          end if;
         end if;
         end process;
f_plsrep<=f;
end bev_plsrep;
--
   ------------------------------------------------------------------


---------------PW
   ------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.all;
USE ieee.std_logic_arith.all;

entity four_pls is
     --generic(n:integer:=3);
          port(
     clk1,freq10: in std_logic;    ---10mhz
          plsrep:in std_logic;         ---2.5khz
          fout,fout1:out std_logic
     );
end four_pls;

architecture Beh_four of four_pls is
     signal count_next :std_logic_vector(23 downto 0);
     signal count_reg :std_logic_vector(23 downto 0);
     signal pls :std_logic_vector(23 downto 0);
     signal f,f1,f2:std_logic := '0';
```

```
          signal f_freq10:std_logic;
begin
    process(clk1)
    begin
    if(clk1'event and clk1='1') then
       count_reg<=count_next;
       if(count_reg=B"00000000000000000000001")then
            f<='1';
       elsif(count_reg=B"00000000000000000000010")
          then
               f<='1';
       elsif(count_reg=B"00000000000000000000011")
          then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000000100")then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000000101")then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000000110")then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000000111")then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000001000")then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000001001")then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000001010")then
            f<='1';
                 elsif(count_reg=B"
                    00000000000000000001011")then
            f<='1';
            elsif(count_reg=B"00000000000000000001100
               ")then
           f<='1';
```

```
            elsif(count_reg=B"
               00000000000000000001101")then
     f<='1';
            elsif(count_reg=B"
               00000000000000000001110")then
     f<='1';
else
    f<='0';
            end if;

if(count_reg=B"00000000000000000000011")then
        f1<='1';
elsif(count_reg=B"00000000000000000000100")
   then
         f1<='1';
elsif(count_reg=B"00000000000000000000101")
   then
     f1<='1';
     elsif(count_reg=B"00000000000000000000110
        ")then
     f1<='1';
     elsif(count_reg=B"00000000000000000000111
        ")then
     f1<='1';
            elsif(count_reg=B"
               00000000000000000001000")then
     f1<='1';
     elsif(count_reg=B"00000000000000000001001
        ")then
     f1<='1';
            elsif(count_reg=B"
               00000000000000000001010")then
     f1<='1';
            elsif(count_reg=B"
               00000000000000000001011")then
     f1<='1';
            elsif(count_reg=B"
               00000000000000000001100")then
     f1<='1';
            elsif(count_reg=B"
               00000000000000000001101")then
```

```
            f1 <='1';
                  elsif(count_reg=B"
                     00000000000000000001110")then
            f1 <='1';
                  elsif(count_reg=B"
                     00000000000000000001111")then
            f <='1';
                  elsif(count_reg=B"
                     00000000000000000010000")then
            f1 <='1';
                  elsif(count_reg=B"
                     00000000000000000010001")then
            f <='1';
                  elsif(count_reg=B"
                     00000000000000000010010")then
            f1 <='1';
        else
            f1 <='0';
            end if;
    end if;
end process;
    --pls<=conv_std_logic_vector(2E3,24); -------CAN
       USE THIS STATEMENT ON CHANCING N GENERIC--
      pls<=B"000000000001111101000000";      ------N
         ---
        count_next <=count_reg+'1' when(count_reg=B"
           000000000000000000000000" and plsrep='1')
           else
      count_reg when (count_reg=B"
         000000000000000000000000") else
      count_reg+'1' when (count_reg<pls)else
           B"000000000000000000000000";
      f2<=f1 and freq10 ;
           f_freq10<=not freq10;
           fout<= f and f_freq10;
                fout1<= not f2;
end Beh_four;
--
   ------------------------------------------------------------------
```

B. Figures Figure 37 is the reference circuit diagram for the oscillator and gain board.

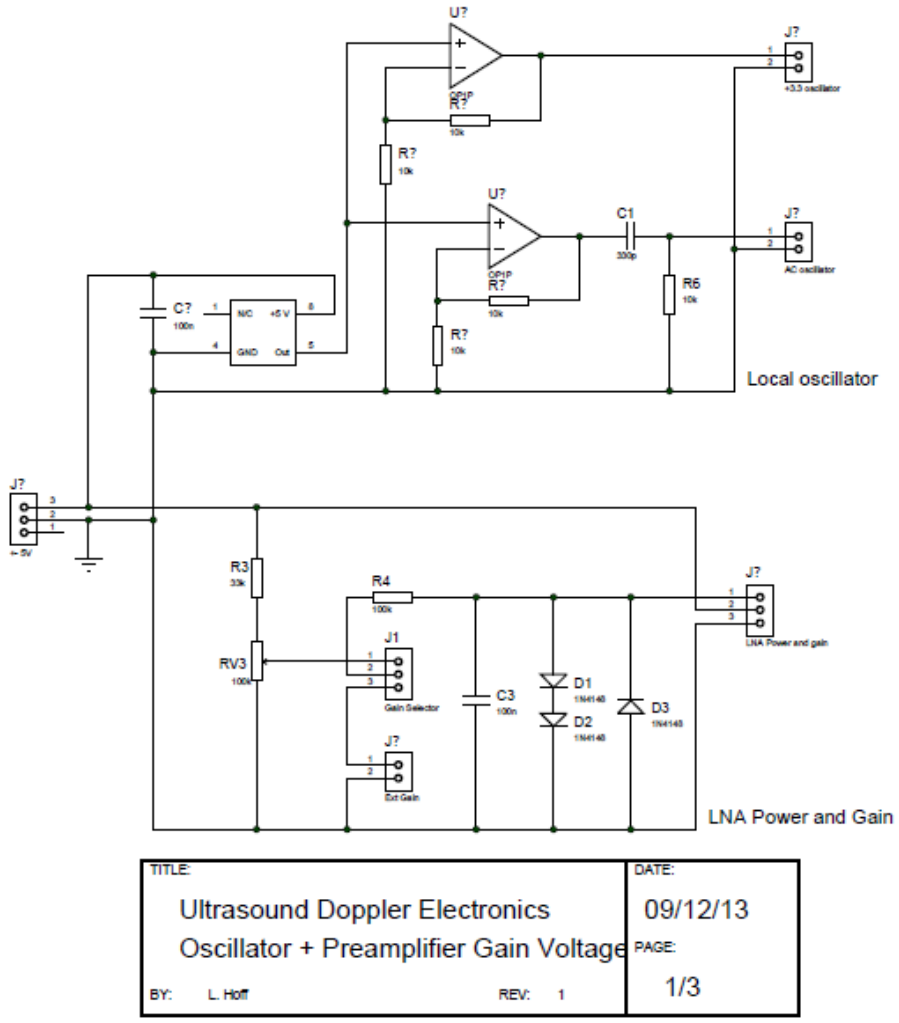

Figure 37: Oscillator and gain board reference circuit [4]

Figure 38 is the simulation result for the T/R switch in Proteus Professional 8. Here the sinusodial excitation of 44V-peak to-peak of frequency 10MHz was used which was clipped by the diode circuit to 683 millivolts.

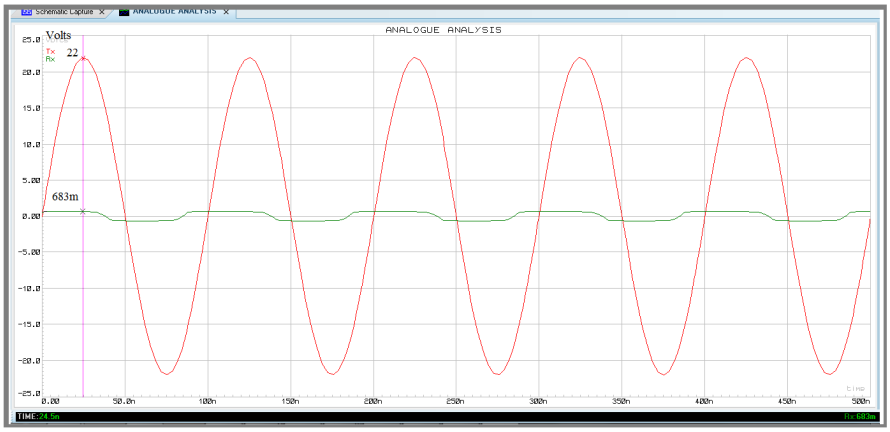

Figure 38: The simulation of T/R switch in Protetus.

List of Acronyms

NDT Non-Destructive Testing

HDL Hardware Description Language

VHSIC Very High Speed Integrated Circuits

IEEE Institute of Electrical and Electronic Engineers

ASIC Appplication Specific Integrated Circuit

LabVIEW Laboratory Virtual Instrument Engineeering Workbench

ARES Advance Routing and Editing Software

CPLD Complex Programmable Logic Device

PLD Programmable Logic Device

PLA Programmable Gate Array

FPGA File Programmable Gate Array

EDA Electronic Design Automation

T/R Transmit-Receive

VHDL (VHSIC Hardware Description Language

IC Integrated Circuit

ISE Integrate Software Environment

PZT Lead Zirconium Titanate

JEDEC Joint Electron Device Engineering Council

JTAG Joint Test Action Group

RADAR Radio wave Detection And Ranging

SONAR Sound Navigation And Ranging

TGC Time Gain Compensation

ISP In-System-Programming

PRT Pulse Repetition Time

PRF Pulse Repetition Frequency

RF Radio Frequency

2D Two Dimension

3D Three Dimension

VI Virtual Instrument

LV Lab View

LNA Low Noise Amplifier

ADC Analog to Digital Converter

AC Alternating Current

RTL Register Transfer Level

CLB Configurable Logic Blocks

LUT Look Up Tables

SRAM Static Random Access Memory

ROM Read Only Memory

PW Pulsed Wave

MS/s Mega Sample per Second

CW Continuous Wave

PC Personal Computer

MRG Multi Range Gated

SNR Signal to Noise Ratio

MOSFET Metal Oxide Semiconductor Field Effect Transistor

CMOS Complementary Metal-Oxide Semiconductor

PCB Printed Circuit Board

LED Light Emitting Diode

LV Low Voltage

VCM Voltage Common Mode

TTL Transistor Transistor Logic

TGC Timing Gain Control

EIM Electrical Impedence Matching

SMA SubMiniature version A

AIM Acoustic Impedence Matching

VGA Variable Gain Amplifier

HBV Hgskolen i Buskerud og Vestfold

DAQ Data Acquisition

RF Radio Frequency

EDA Electronic Design and Automation

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