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Graphene synthesized on porous silicon for active electrode material of supercapacitors

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Abstract

We present graphene synthesized by chemical vapour deposition under atmospheric pressure on both porous nanostructures and flat wafers as electrode scaffolds for supercapacitors. A 3nm thin gold layer was deposited on samples of both porous and flat silicon for exploring the catalytic influence during graphene synthesis. Micro-four-point probe resistivity measurements revealed that the resistivity of porous silicon samples was nearly 53 times smaller than of the flat silicon ones when all the samples were covered by a thin gold layer after the graphene growth. From cyclic voltammetry, the average specific capacitance of porous silicon coated with gold was estimated to $267\,\mu\mathrm{F}/cm^2$ while that without catalyst layer was $145\,\mu\mathrm{F}/cm^2$. We demonstrated that porous silicon based on nanorods can play an important role in graphene synthesis and enable silicon as promising electrodes for supercapacitors.

1. Introduction

Supercapacitors have attracted great interest for their high power density compared to batteries and high energy density compared to traditional capacitors [1-2]. Generally supercapacitors have an energy density 10 to 100 times larger than electrolytic capacitors, and less charging time than batteries, as well as longer charge- and discharge-cycle life [3-4]. Therefore, supercapacitors are broadly used in computer systems, grid power buffers, street lights, automobiles, and other power supply systems. Graphene is very popular for building carbon-based supercapacitors. It is an atomically thin two-dimensional sheet of sp2 bonded carbon atoms which gives rise to exceptional electronic, magnetic, and optical properties. Each atom has four bonds, one σ bond with each of its three neighbours and one π-bond that is oriented out of plane [5]. Chemical vapour deposition (CVD) has been extensively explored to grow high quality graphene layers of large area and allows growth of single or multiple layers of graphene directly on a substrate (usually metal) using hydrocarbon precursors. However, the graphene layer must usually be transferred to other preferred substrates for subsequent use and is easy to damage during the segregation from the growth substrate. Recently it has been reported that graphene can be grown on silicon templates thus transforming the substrates into stable electrodes for electrochemical devices while avoiding the exfoliation from the templates [6]. A major restriction of direct graphene growth on silicon-based

substrates is that the pristine silicon is chemically inert due to the weak reaction between silicon and hydrocarbons. Hence application of surface engineering techniques for the CVD growth of graphene becomes an enabling process when silicon is used as a substrate.

2. Process for graphene growth

In this work, we propose to synthesize graphene on porous silicon through a CVD process with a catalysis mechanism. We apply a layer of gold as the catalyst. Gold has a high melting point of 1337.33K and a relatively low thermal expansion coefficient of 13. Therefore it can stay solid during the CVD process and introduce ignorable thermal stress within the graphene layer. In addition, gold doesn't react with oxygen so there is no worry about oxidation inside the reaction chamber even if the process gas is not entirely oxygen-free [7]. Yet a thick layer of metal catalyst will compromise the main advantage of a high surface area of porous silicon by filling voids and thereby reducing area. In our case, a gold layer catalyst thickness of 3 nm was chosen based on the dimension of the nanostructures. The layer was deposited with an AJA sputtering system.

Subsequently the samples were loaded into a CVD system and placed at the center of the tube furnace. The system provided an inert environment under temperatures ranging from 35℃ to 850℃. Argon and Hydrogen were mixed and introduced in the tube to maintain atmospheric pressure with a flow rate of 1 SLM and 100 SCCM respectively. Then 10 SCCM of acetylene was added after reaching 650℃. The furnace was then heated to 750℃ and 850℃ internally with a holding time of 15 minutes in both temperature stages. Then acetylene was shut off and the samples were cooled off to room temperature in the presence of Argon and Hydrogen.

3. Results and discussion

Scanning electron microscopy (SEM) was carried out using Scanning Electron Microscope SU3500 with an acceleration voltage of 5 to 15kV to identify graphene layers on porous silicon. The SEM images show the nanoscale features on porous silicon. It is clearly illustrated in figure 1(a) and figure 1(b) that there is a thin layer (bright field) on the nanorods (grey field) on porous silicon after graphene growth process. More clearly, the cross-sectional images of porous silicon of figure 2(a) and figure 2(b) show obvious difference before and after direct-graphene coated process and indicate a continuous layer covered on the nanorods although it was not as smooth as might have been expected.
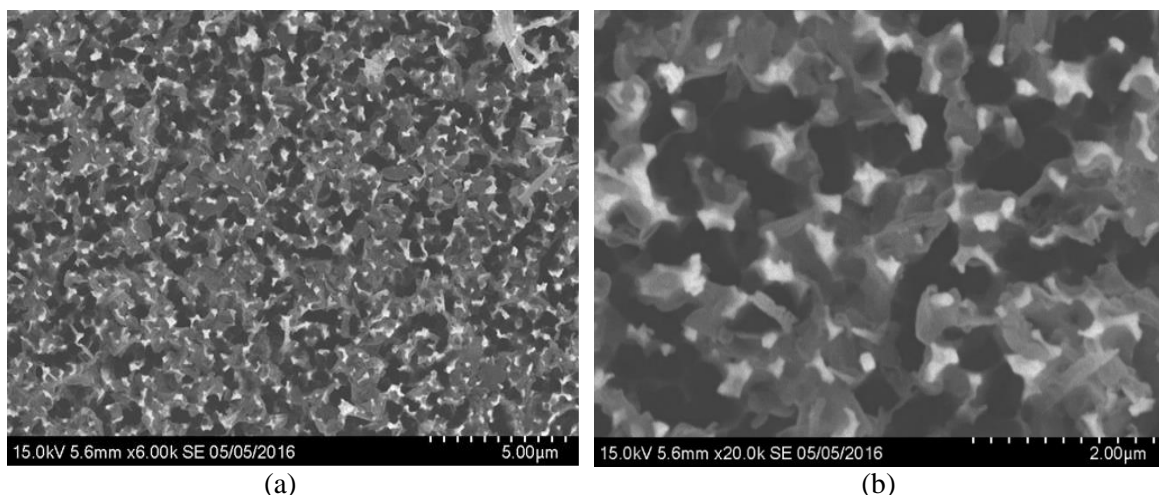

(a)	(b)

Figure 1 SEM images of porous silicon showing the graphene layer coated on the nanorods, (a) in a small magnification; (b) in a large magnification.

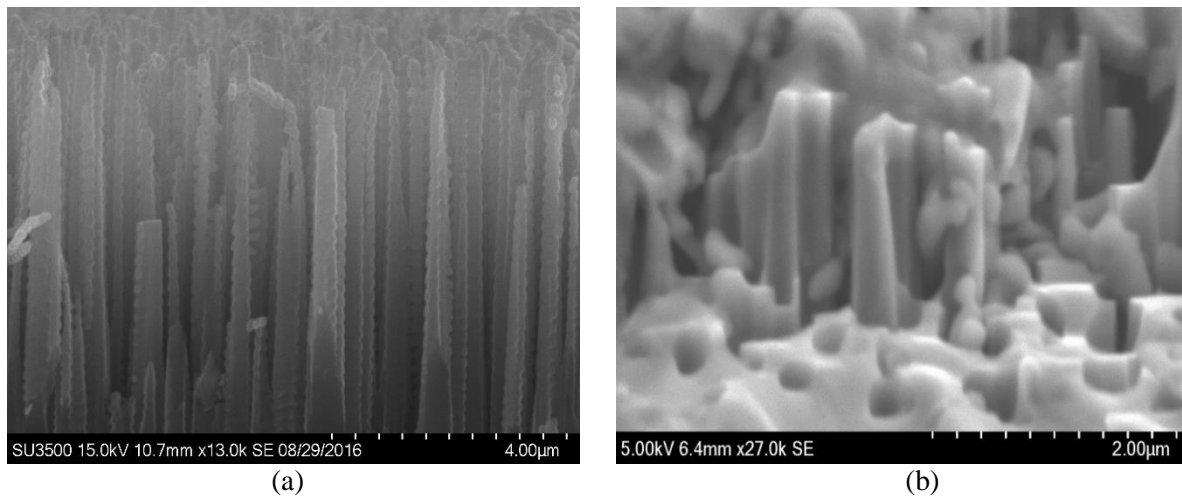(a)   (b)

Figure 2 SEM images of (a) cross-section of porous silicon before direct-graphene coated process, (b) cross-section of porous silicon after direct-graphene coated process indicating layers coated between the nanorods.

Four-point-probe measurements were conducted to provide qualitative analysis on the conductivity of direct-graphene coated and catalyst-graphene coated flat silicon and porous silicon respectively. Measurements of the resistance of the prepared samples were performed in a collinear configuration. The ratio of voltage and current, the slope in the figure 3, presents the resistance of the tested samples. Among the P-doped flat silicon substrates, the resistance is almost 0.15Ω after catalyst-graphene coating and 1.56Ω after direct-graphene coating. The results are consistent with the expectation that pure silicon is not a good substrate for graphene growth due to the low carbon solubility in silicon while the gold is a good substrate due to the adsorption of C atoms on its surface. This adsorbing behaviour further accelerates the graphene growth when acetylene was introduced [8].
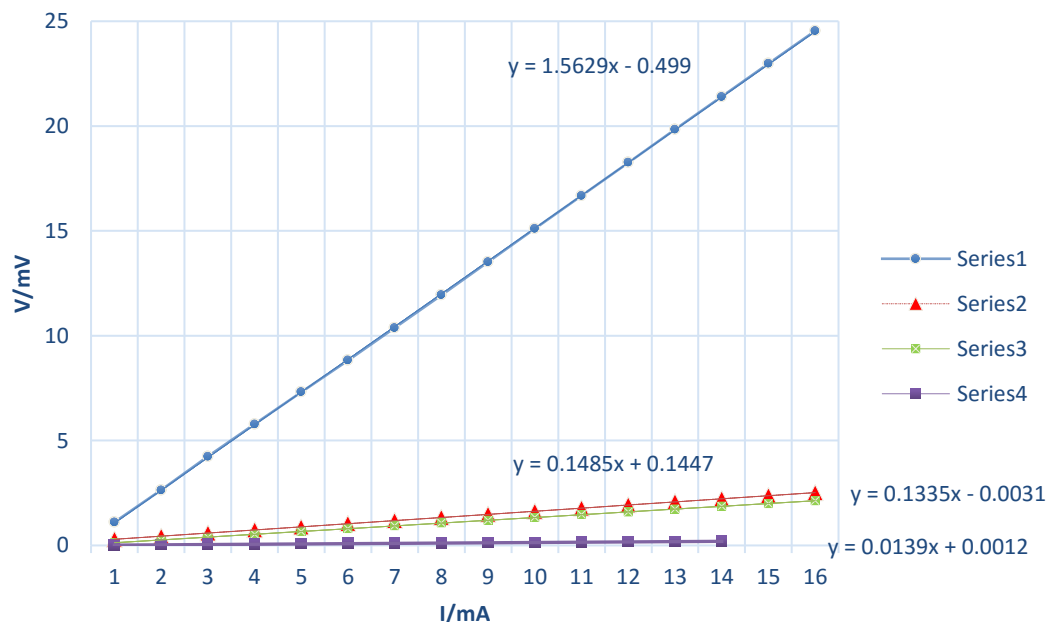

Figure 3 Four-point-measurement results for tested samples of direct-graphene coated silicon (series 1), catalyst-graphene coated silicon (series 2), direct-graphene coated porous silicon (series 3) and catalyst-graphene coated porous silicon (series 4).

For the porous silicon, figure 3 shows that the direct-graphene coated porous silicon has the resistance reduced to approximately 0.13Ω compared to 1.56Ω of the direct-graphene coated flat silicon. The improvement on the conductivity largely benefited from the nanoporous structure on the surface of the porous samples. Because the nanoporous structure enlarges the surface area, carbon atoms have greater opportunity to adsorb on the surface when the reactive gases flow over the samples in the furnace. Therefore, the nanoporous structure can be seen as a pool of carbon atoms, which provided an effective path of supplying carbon source for graphene growth. In addition, for the porous silicon samples, figure 3 also shows that the catalyst-graphene coated porous silicon has resistance greatly reduced to 0.0028Ω. This significantly improved conductivity can be attributed to both the gold catalyst layer and the nanoporous structure, which allowed more C atoms to be incorporated for coating on the sample surface, thus resulting in continuous graphene film. The results reveal that porous silicon with the gold catalyst layer can be considered as an excellent functional structure base for graphene growth and can be a candidate for active electrodes of supercapacitors [9].

As the active electrodes for supercapacitors, the electrochemical performance, e.g., the electrochemical double layer capacitance (EDLC) of the samples was investigated by cyclic voltammetry (CV). The catalyst-graphene coated porous silicon exhibits almost double the specific capacitance of the direct-graphene coated porous silicon (figure 4). The average specific capacitance of the catalyst-graphene coated porous silicon was estimated to be 267µF/cm^2 while that of the direct-graphene coated porous silicon was 145µF/cm^2. Xia al. have conducted an experimental determination of EDLC capacitance of graphene to be $21\,\mu F/cm^2$ [10]. The results attained in this experiment indicate a substantial improvement on the electrochemical performance of both the catalyst-graphene coated and direct-graphene coated porous silicon samples, which suggests the porous silicon yields a reliable functional structure to graphene formation. An ideal CV curve of EDLC capacitor should be approximately rectangular in shape. The samples of both catalyst-graphene coated and direct-graphene coated porous silicon exhibited resistive behaviour, which makes the CV plots differ from the shape of an ideal EDLC capacitor.
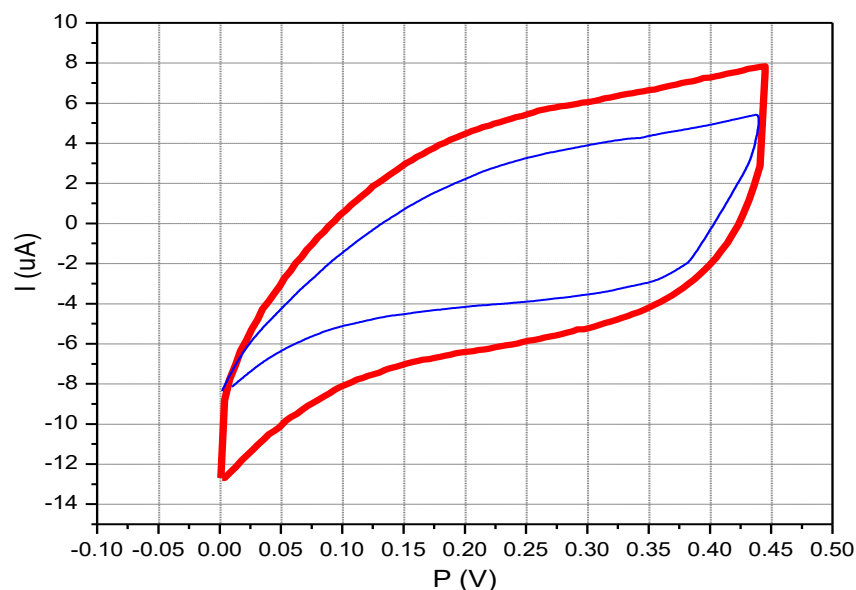

Figure 4 Cyclic voltammetry plots for catalyst-graphene coated porous silicon (thicker line) and direct-graphene coated porous silicon (thinner line).

4. Conclusions

In summary, we have successfully managed to grow graphene on nano structured silicon samples for making active electrodes for EDLC supercapacitors. The conductivity of the direct-graphene coated porous silicon was 10 times better than that of the direct-graphene coated flat silicon, which can be explained by a high quality graphene layer because the nano structure provides large surface area, thus resulting in a large amount of carbon atoms segregating on the surface of the samples. A gold catalyst layer can further effectively promote the formation of graphene layer on the nano structure surface, which is supported by the observation of 100 times lower resistance in catalyst-graphene coated porous silicon than the one in direct-graphene coated flat silicon. Subsequently, cyclic voltammetry proved the superiority of graphene as active electrode materials for electrochemical double layer capacitors, indicating an EDL capacitance of 145μF/cm^2.

Acknowledgement

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