Low power electronic interface for electrostatic energy harvesters

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Low power electronic interface for electrostatic energy harvesters

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Abstract. This paper presents design and simulation of a power electronic interface circuit for MEMS electrostatic energy harvesters. The designed circuit is applicable to highly miniaturized electrostatic harvesters with small transducer capacitances below 10 pF. It is based on comb-drive harvesters with two anti-phase capacitors that are connected as charge pumps and uses a flyback-path scheme. Controlled activation and deactivation of sub-circuits, some by help of clocking, were exploited to reduce power consumption down to 1.03 μW. Net power generation can be achieved with as low initial voltage as 3.0 V.

1. Introduction

Harvesting energy from the environment is not a new concept and has been widely explored in various applications such as wireless sensor nodes [1], structural health monitoring [2] or implantable biomedical devices [3]. Among ambient energy sources, kinetic energy is abundant and therefore an attractive alternative motivating a number of studies [4, 5]. Commonly used mechanisms for energy conversion in kinetic energy harvesters are electromagnetic, piezoelectric and electrostatic transduction [6]. Capacitive electrostatic harvesters are attractive due to their suitability for microfabrication and their potentially small chip sizes. These harvesters suffer from correspondingly small variable capacitances, limited by standard fabrication processes and device size, which are obstacles for effective energy conversion. To design an effective micro energy harvesting system, not only the generator design and fabrication should be optimized, but also the power electronic interface for the generator. The electronic interface circuitry in a micro energy harvester system must be highly effective and power conservative as it is supplied by the harvester system. Due to the limited power available in the microscale electrostatic generators, designing effective power electronic interface is especially challenging.

There have been published several interesting studies on the interface circuits for capacitive transducers, especially for those with large capacitances. Meninger *et al.* [7] proposed a synchronous capacitive energy harvester consisting of two active switches to charge and discharge a variable capacitor through an inductor. Complexity of control circuitry and power dissipation for synchronization are main concerns for this architecture. Miyazaki *et al.* [8] improved this topology by proposing timing-capture scheme instead of programmable controller with delay locked loop (DLL) feedback. A, by now, classic circuit topology was proposed by Yen *et al.* [9] in which a charge pump was used with a flyback circuit to store and transfer extracted energy.

This topology was further investigated by Galayko *et al.* [10], focusing on design of the control circuit to optimize the flyback switching sequence. Other architectures used voltage-constrained topology by Torres *et al.* [11], and modified storage capacitor in the charge pump part by Kempitya *et al.* [12].

In this work, an interface circuit for a MEMS electrostatic energy harvester with transducer capacitance range below ∼10 pF is presented. The interface circuitry is based on the aforementioned flyback technique and automatically detects the switching instants for optimal power transfer through the flyback path without using any external control signals. A circuit alternative to the comparators that are used in other implementations of this architecture is investigated. The need to power the circuitry by extracted power only and the limited available power due to a highly miniaturized MEMS harvester makes low power consumption of the circuit a main design driver. All the simulations presented were made with Tanner Tools using models for the high-voltage AMS035 CMOS process.

2. Power electronic interface

2.1. Overview

The circuit topology is an adaption of Yen's circuit [9] to anti-phase capacitive structure with double, instead of single charge pumps. Figure 1 shows the block diagram of the whole circuit which consists of three main elements: double charge pump, flyback path and switch controller. In this topology, optimization of switching sequence in the flyback has significant effect on harvested power from electrostatic transducer. Thus, the control circuitry presented is designed to detect these optimal switching instants and then turn on/off the switch correspondingly.

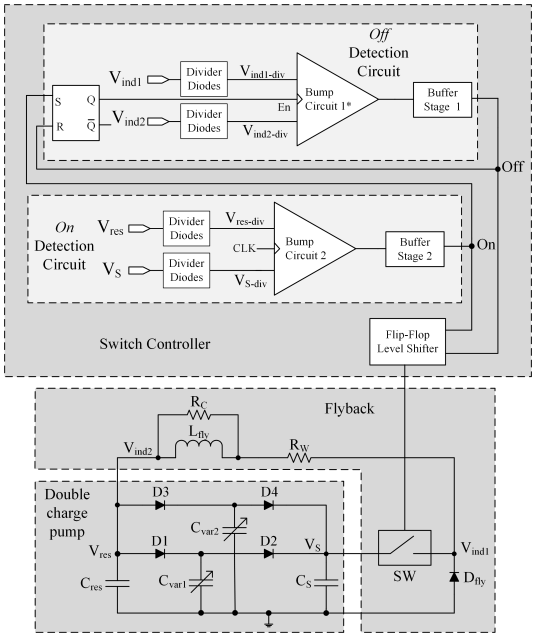

Figure 1. Block diagram of proposed circuit.

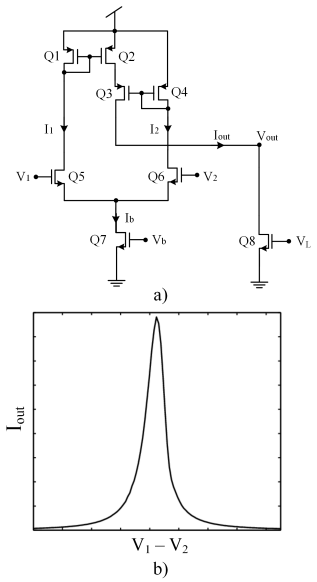

Figure 2. *a*) Bump circuit. *b*) Input-output characteristics of bump circuit. (After Delbruck [13])

2.2. Double charge pump

The double charge pump is used because two capacitors varying with opposite of phases are found in many electrostatic harvesters. Operation of the double charge pump is similar to the case of one pumping capacitor except that it exploits the entire mechanical cycle by transferring

charges into the store capacitor C_s during both half cycles. The voltage V_s on the store capacitor after n cycles of vibration is

$$V_{s,n} = V_{res}[(1 - \frac{C_{max}}{C_{min}})(\frac{C_s}{C_{min} + C_s})^{2n} + \frac{C_{max}}{C_{min}}] \quad (1)$$

where V_{res} is the voltage across the reservoir capacitor and C_{max}/C_{min} are the maximum and minimum capacitances of the transducer during one vibration cycle.

2.3. Flip-flop level shifter

As the voltage across the harvesting capacitor and the flyback switch are much higher than the voltage controlling the switch, a level shifter is needed to match these two. A flip-flop is also needed to hold the switch state after receiving the *on* or *off* signal at the input of level shifter. Dudka *et al.* [14] proposed a flip-flop level shifter that fulfills these requirements and has a zero static power consumption.

2.4. Circuit detecting on event

Assume $V_s = V_{res} = V_0$ at startup when $t = 0$ and define $V_1 = V_s$ $(t = t_1)$ as the optimal V_s at which the switch should be turned on. Similar to the power obtained from a single transducer as calculated in [10], the power harvested from the two anti-phase transducers here is

$$P = \frac{C_s(1 + \frac{C_s}{C_{res}})V_0^2}{T} \ln \frac{C_s}{C_{min} + C_s} \frac{(1 - \theta)^2}{\ln \frac{\theta - \alpha}{1 - \alpha}} \quad (2)$$

where T is the vibration period, $\theta = V_1/V_0$ and $\alpha = C_{max}/C_{min}$. There is an optimal value $\theta = \theta_{opt}$ at which the power is maximum. It is given by

$$2 \ln \frac{\theta_{opt} - \alpha}{1 - \alpha} = \frac{\theta_{opt} - 1}{\theta_{opt} - \alpha}. \quad (3)$$

To detect when V_s reaches the optimal value and the switch should be turned on, V_s is first divided by θ_{opt}, then a bump circuit [13], as shown in figure 2, is used to trigger switching when the obtained value is equal to V_{res}. The bump circuit is a voltage similarity detector which produces a signal when the two inputs are equal. A diode-connected voltage divider is used to downscale the voltage to a suitable level at the input of bump circuit.

2.5. Circuit detecting off event

When the switch is turned on, the circuit has C_s, L_{fly} (including parasitics) and C_{res} in a series configuration. In order to optimize the power transfer, the switch should be turned off when the inductor current reaches maximum value, i.e. when voltage across L_{fly} is equal to zero. To detect this instant, a bump circuit is connected to the two terminals of the inductor. The bump circuit's output voltage goes high when its two inputs are equal. In order to reduce power consumption, this bump circuit is activated only during the on-time of the switch. The bump circuit deactivates itself after it detects the *off* event. The bias voltage V_b of the bump circuit is used for activation/deactivation.

3. Simulation results

In the simulations, we adopt transducer parameters of the small-scale electrostatic harvester prototype published in a previous work [15]. The transducer is a comb-drive capacitance with a maximum capacitance $C_{max} = 8.62$ pF and a minimum capacitance C_{min}=2.16 pF, ignoring parasitic capacitances. The operating frequency of the harvester is f_0 =650 Hz. The optimal value θ_{opt}=3.15 is then found from (3).

3.1. Basic operation

Figure 3 a) demonstrates the basic operation without the flyback path. When the capacitances vary, V_s increases to a saturated value as the charge is built up on C_s. With the flyback path, V_s is prevented from saturation by discharging it through flyback path as illustrated in figure 3 b) where the switch is periodically turned on by an external signal.

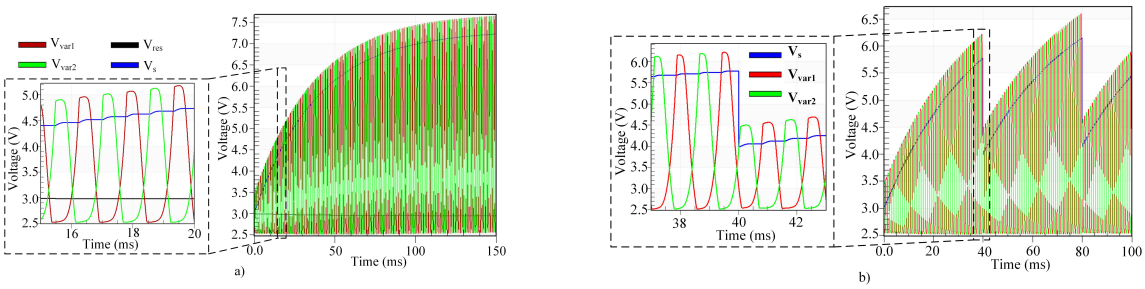

Figure 3. Voltage waveforms across capacitors in double charge pump circuit: *a*) without flyback path and *b*) with flyback path and periodically closing switch.

3.2. With control circuitry

We now consider operation with the control circuitry described in the previous section. We let the *on*-detection bump circuit stay enabled all the time as it is unknown when it needs to do its comparison, except for the short duration when the switch is already on. Figure 4 shows that the pulse *off* occurs when V_{ind1} approaches V_{ind2}. The *on* detection circuit detects when V_s/V_{res} reaches 3 and then generates the pulse *on* as shown in figure 5. However, the power consumption of the control circuitry in this configuration is 97.2 μW. It is too high to be supported by the harvested power so an external source was used in the simulation. Most of the consumption is in the second bump circuit which is enabled all the time.

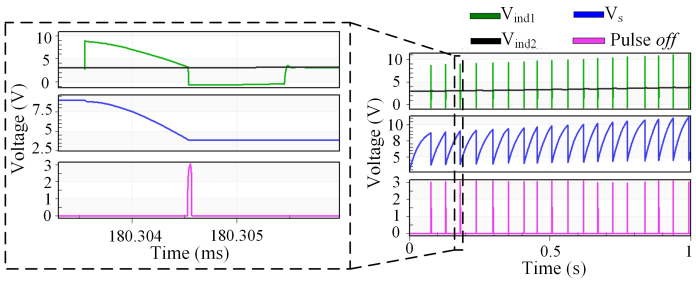

Figure 4. The switch is turned *off* when V_{ind1} approaches V_{ind2}.

3.3. Clocking technique for lowering power consumption

Reduced power consumption can be obtained by clocking the enable signal of the second bump circuit, as shown in figure 1. By choosing a small duty cycle, the circuit is kept mostly in off-mode. The reduced power comes at the expense of accuracy in the timing of the switch, but is controlled by clock frequency. With a duty cycle of 0.005%, the power consumption of the control circuitry is reduced to 1.03 μW which is comparable to that of the circuit in [16].

With an initial voltage of 3.0 V, the system power-budget is balanced with a small margin of 8.3 nW as shown in figure 6. We estimate the power required to drive the second bump circuit's

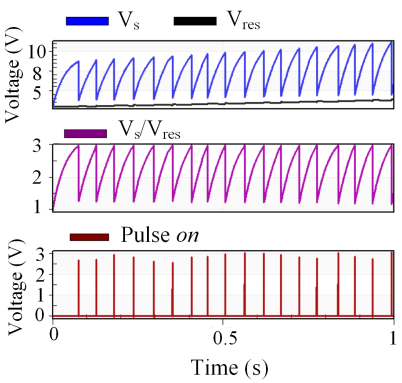

Figure 5. The switch is turned *on* when $V_s/V_{res} = 3$.

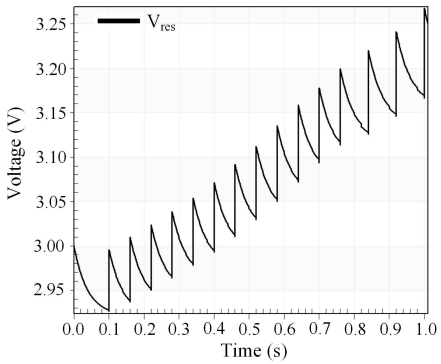

Figure 6. Voltage waveform on C_{res} of the designed circuit when using harvested energy to power control blocks.

enable port to about 150 pW. The clock generator was not simulated, but state-of-the-art low power oscillators can have a power consumption in the nW-range [17] and could therefore be driven by the small power margin found here. Hence, the capacitance variation and initial voltage here constitute a break-even case for operation of this circuit.

4. Conclusions

A low power electronic interface for MEMS electrostatic energy harvesters was designed using bump circuits. The design consists of double charge pumps and a flyback switch with an associated switch controller. The controller automatically detects the optimal switching instant solely based on internal voltages. The power consumption of the entire circuitry was reduced by a factor about 94 by using clocking. Simulations showed that with an initial bias voltage of 3.0 V, the interface circuitry could be powered by a harvester with less than 10 pF capacitance without need for external bias sources.

Acknowledgment

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