Nano fabricated silicon nanorod array with titanium nitride coating for on-chip supercapacitors

Pai Lu (1), Per Ohlckersa (1), Lutz Müller (2), Steffen Leopold (2), Martin Hoffmann (2), Kestutis Grigoras (3), Jouni Ahopelto (3), Mika Prunnila (3), Xuyuan Chen (1)

1 Department of Micro- and Nanosystem Technology, University College of Southeast Norway, Campus Vestfold, Raveien 215, 3184 Borre, Norway
2 Chair of Micromechanical Systems, IMN MacroNano ®, Ilmenau University of Technology, PF 100565, D-98694 Ilmenau, Germany
3 VTT Technical Research Centre of Finland, P. O. Box 1000, FI-02044 VTT, Espoo, Finland

Accepted version of article in
Electrochemistry communications. 2016, 70 51-55.

Nano fabricated silicon nanorod array with titanium nitride coating for on-chip supercapacitors

Pai Lu[a], Per Ohlckers[a], Lutz Müller[b], Steffen Leopold[b], Martin Hoffmann[b], Kestutis Grigoras[c], Jouni Ahopelto[c], Mika Prunnila[c], Xuyuan Chen[a,*]

[a] Department of Micro- and Nanosystem Technology, University College of Southeast Norway, Campus Vestfold, Raveien 215, 3184 Borre, Norway

[b] Chair of Micromechanical Systems, IMN MacroNano®, Ilmenau University of Technology, PF 100565, D-98694 Ilmenau, Germany

[c] VTT Technical Research Centre of Finland, P. O. Box 1000, FI-02044 VTT, Espoo, Finland

* Corresponding author. E-mail address: Xuyuan.Chen@hbv.no

Abstract

We demonstrate high aspect ratio silicon nanorod arrays by cyclic deep reactive ion etching (DRIE) process as a scaffold to enhance the energy density of a Si-based supercapacitor. By unique atomic layer deposition (ALD) technology, a conformal nano layer of TiN was deposited on the silicon nanorod arrays as the active material. The TiN coated silicon nanorods as a supercapacitor electrode lead to a 6 times improvement in capacitance compared to flat TiN film electrode.

Keywords: Supercapacitor, Silicon nanorod array, TiN nano film, DRIE, ALD

1. Introduction

The recent boom of Si-based micro energy harvesting systems has promoted an intense technological trend for pursuing self-powered electronic devices [1–4]. In this regard, micro energy storage systems are indispensable, as they will play a crucial role in storing and managing the harvested energy [5–8]. Electrochemical energy storage systems may be one of the best candidates due to their high energy utilization efficiency [9–11]. Currently, microbatteries are the major power source for micro electronic devices even though they suffer from poor rate performance and limited cycle life [12, 13]. Supercapacitor, which represents a class of electrochemical energy storage device with high power density and excellent cycling stability, has attracted tremendous interest [14–16]. On-chip supercapacitor with in-plane thin film electrodes now is showing a pathway to replace microbattery utilized previously in microelectronic integrated circuits (IC) [17, 18].

Many different materials have been considered for the tailored nanostructures for on-chip electrodes, such as polypyrrole [19, 20], carbide-derived porous carbon [21], carbon nanotube forests [22], onion-like carbon [23], and graphene [24]. However, these materials are typically realized by deposition strategies that leave the underlying Si substrate unused and involve non IC compatible processes. This has stimulated development of supercapacitors based on silicon, where energy density was enhanced by nanofabricating porous silicon [25] and silicon nanowires [26, 27]. However, pristine silicon nanostructures suffer from low conductivity and poor chemical stability. Different coating strategies, such as carbonization of the Si nanostructure

surface [28, 29] and ALD technology [30–34], have been investigated to solve these show-stopper issues, which are suitable for coating high aspect ratio structures required for supercapacitor electrodes. However, carbonization of the Si surface does not provide low resistance and this leads to limited power [28, 31]. Whereas, it has been shown recently that TiN coating by ALD solves the resistance and stability issues simultaneously [30–34] resulting in performance comparable to the best graphene based devices [34]. In addition of the material studies, porous Si based supercapacitors have been combined with microelectronics [35] and solar cells [36] by joining two separate Si chips. Recently, two TiN coated porous Si electrodes and electrolyte have been also directly integrated inside a silicon chip thereby forming an in-chip supercapacitor device [34].

Grass-like silicon nanorods (Si-NR) are well-known as the unwanted nanostructured by-product generated during the DRIE of silicon [37] in IC and micro-electro-mechanical system (MEMS) technology. DRIE Si-NR has not been considered as a candidate for supercapacitor electrode because of its unpredictable structure and relatively small aspect ratio (10~50) [38]. However, the DRIE Si-NR possesses the feature of two dimensional micro/nano array with open channel in the vertical direction of the array plate. Used as the electrode scaffold, the DRIE Si-NR is favorable for fast ion diffusion in and out. In this study, taking use of the advantages of the IC compatible process and one-dimensional ion diffusion characteristic of Si-NR, we developed a high performance on-chip supercapacitor by utilizing a high aspect ratio Si-NR with well-defined array of nano structures as the electrode scaffold.

The active electrodes were engineered by conformal coating nano layer TiN on the scaffold at lower temperature instead of using carbon materials. In comparison with silicon nanowires and nanoporous Si coated with carbon material, no expensive metal catalysts, high-temperature condition in chemical vapor deposition [26, 27], and electrochemical etching [25, 28–34] are needed. Our proof-of-concept device demonstrates the feasibility for fabricating the on-chip supercapacitors by monolithography integration.

2. Experimental

2.1. Nanostructure fabrication

To fabricate Si-NR with well controlled nano-structure and rod density on wafer scale, we developed a cyclic DRIE route [39, 40], which was performed on an inductively coupled plasma system. To obtain Si-NR with depth as high as ~20 μm, extended 75 etching cycles were performed in this study.

After machining the Si-NR on heavily boron doped Si, the pristine Si-NR went through a hydrogen smoothing step, the annealing was kept at 1100 °C for 5 minutes, and the flow rate of hydrogen was controlled at 40 sccm. Aluminum contact pads were fabricated at the substrate backside via thermal evaporation.

Conformal TiN films were deposited by ALD in the spirit of Refs. [30, 32, 34]. The ALD coating was carried out at 450 ^{o}C in a Picosun reactor Sunale R-150B using $TiCl_4$ and NH_3 as the precursors and N_2 as carrier gas. The enhanced diffusion time of the precursor gases was implemented, enabling a conformal coating of high aspect

ratio Si-NR. The ALD process for 1400 cycles resulted in TiN film with sheet resistivity of approximately 47 Ω/square.

2.2. Material characterization and electrochemical measurement

A Hitachi SU-3500 scanning electron microscope (SEM) equipped with electron dispersive X-ray (EDX) analysis was used to observe the morphologies and analyze the element compositions of materials.

Three-electrode set-up was employed to study the supercapacitor behavior of fabricated working electrodes. Pt counter electrode, and Ag/AgCl (in saturated KCl) reference electrode were used for test. A Zahner IM6 electrochemical workstation was used for electrochemical measurements. Cyclic voltammogram (CV) and galvanostatic charge/discharge (GCD) measurements were conducted in 1 M Na_2SO_4 electrolyte. Electrochemical impedance spectra (EIS) were measured from 100 kHz to 100 mHz with a perturbation of 10 mV at the open circuit potential. The specific capacitance (SC) of the electrodes was calculated by integrating the reductive part of the CVs and the galvanostatic discharge curves.

3. Results and discussion

Fig. 1a reveals the uniformity of the created Si-NR by cyclic DRIE, emerging as regular nanorod arrays, vertically arranged on the Si substrate. The diameter of Si-NR is 100–200 nm, shown in Fig. 1b. Taking their height of ~20 μm into account (Fig. 1c), the aspect ratio is ranging from 100 to 200. The obtained pristine Si-NR was found to possess sharp tips (Fig. 1d), which would make this nano scaffold

mechanically unstable. To remove the tips, hydrogen smoothing process was performed, thus leading to the formation of smooth rounded tips on nanorods (Fig. 1e). EDX result (inset of Fig. 1b) represents the purity of obtained Si-NR, only Si element can be detected. Fig. 1f–g display the morphology of as-formed Si-NR/TiN hybrid, from which it can be found the original morphology of Si-NR was maintained after ALD deposition, indicative of the conformal growth of ~30 nm TiN nano layer (inset SEM image in Fig. 1f). The inset in Fig. 1g shows the EDX spectrum recorded from Si-NR/TiN nanorods. Besides the Si signal, Ti and N elements can also be detected, which illustrates the successful growth of TiN on Si-NR.

Fig. 2 demonstrates the performance comparison of Si-NR/TiN, Si/TiN (TiN film on flat Si substrate) hybrids and the pristine Si-NR as supercapacitor electrodes. CV curves recorded at 100 mV/s are shown in Fig. 2a. Their rectangular shape manifests the nearly ideal capacitor behavior of both Si-NR/TiN and Si/TiN electrodes. No redox peaks ascribed to the pseudo-capacitive behavior can be found in the CV curves, indicative of their electric double layer characteristics. From the amplified CV curves of Si-NR (Fig. 2b), its reactivity in aqueous electrolyte is indicated by the redox peaks, which essentially inhibits its use for stable double layer charge storage. In contrast, the active silicon surfaces on Si-NR that suffer oxidation in electrochemical environment can be passivated by TiN layer for Si-NR/TiN and Si/TiN hybrids, so that the energy storage behavior relying on electric double layer can be realized as in Refs. [30, 32, 34]. The capacitance against scan rate is plotted in Fig. 2c. Benefiting from the abundant accessible electro-active sites offered by the high aspect ratio

Si-NR matrix, with deep open channels that are spaced by nanorods in the vertical direction, the areal SC of Si-NR/TiN is about 6 times that of Si/TiN. Specifically, when swept at 20, 50, 100 mV/s, the areal SC of 1.23, 1.14, and 1.08 mF/cm^2 can respectively be afforded by Si-NR/TiN. The gravimetric SC of 1.03 F/g~20 mV/s, 0.95 F/g~50 mV/s, and 0.90 F/g ~100 mV/s was obtained, normalized to the weight of both TiN and Si-NR. Those results are better than silicon nanowire supercapacitor (36.7 μF/cm^2) [26], and carbon coated silicon nanowire electrode (105 μF/cm^2) [41], also compare well with the results for diamond coated silicon nanowire electrode (1.5 mF/cm^2) [42]. As for Si/TiN electrode, 0.21, 0.18, and 0.15 mF/cm^2 were delivered at the corresponding test conditions. To understand the electrochemical performance characteristics, the EIS study was performed (Fig. 2d). No prominent semi-circle areas appeared in the high-frequency range, in accordance with the fast charge transfer process for these hybrid electrodes favored by the high quality TiN nano layer with good electric conductivity. Compared with Si/TiN, Si-NR/TiN electrode exhibited better capacitor behavior as indicated by the larger slope in the low-frequency range. In contrast, Si/TiN electrode displayed a typical ion diffusion controlled behavior. The superiority of Si-NR/TiN electrode in this regard is mainly attributable to the favorable nanostructures of Si-NR scaffold for ion diffusion, as sketched in Fig. 2c. The opened inter-rod spaces can serve as the reservoir for electrolyte ions, which can help shorten the diffusion pathway and facilitate their fast diffusion along the one-dimensional channels.

Fig. 3a and 3b respectively show CVs and GCD curves of Si-NR/TiN electrode,

from which the calculated capacitance is presented in Fig. 3C. Owing to the superior electric conductivity of TiN nano layer and opened nanostructures offered by Si-NR, rapid ion diffusion and electron transfer were both favored, which led to a good rate performance. When the CV scan rate was increased from 2 mV/s to 1000 mV/s, the initial areal SC of 1.55 mF/cm^2 decayed to 0.95 mF/cm^2, representing a 61% capacitance retention. With the GCD current density increasing from 3.5 μA/cm^2 to 87.5 μA/cm^2, the original capacitance of 1.53 mF/cm^2 decayed to 1.13 mF/cm^2. It should be noted that one main reason contributing to the power loss is the insufficient electric conductivity (0.01~0.015 Ω cm) of the doped silicon substrate especially at ultrafast discharge rate. For the future work in on-chip device design, silicon will be avoided as the current collector, which can be realized by fabricating interdigital electrode configuration [19, 20]. Fig. 3d displays the cycling performance test. From the 1st and the 2000th CV cycle curve, it can be found the main capacitance decay occurred in the potential range of 0.6–0.8 V when charged, which may be ascribed to several possible reasons, e.g., the irreversible oxidation of uncovered silicon active sites, slight surface oxidation of TiN, or the presence of impurities on the electrode surface or in the electrolyte. After 2000 cycles swept at 100 mV/s, the SC decreased from the initial 1.08 mF/cm^2 to 1.03 mF/cm^2, 95.2% of the capacitance retention was achieved.

4. Conclusions

We illustrated a TiN coated DRIE Si-NR electrode with improved performance

(1.55 mF/cm^2~2 mV/s, 0.95 mF/cm^2~1000 mV/s), which successfully demonstrates a new avenue to develop on-chip supercapacitors with high aspect ratio Si-NR as the scaffold that can help enhancing the performance. More significantly, the developed cyclic DRIE process for Si-NR and ALD technique for conformal TiN deposition herein are fully compatible with IC technology. With the use of Si-NR as scaffold, the device pattern can also be readily transferred on the chip via MEMS process.

Acknowledgment

Fruitful discussions with Professor Einar Halvorsen are acknowledged. Oili Ylivaara and Riikka Puurunen are acknowledged for their help in ALD process. Financial support from the Research Council of Norway under Grant No. 229716 is acknowledged. Financial support from the Academy of Finland through the Atomic Layer Deposition Centre of Excellence project is acknowledged.

References

[1] B. P. Nabar, Z. Celik-Butler, D. P. Butler, Piezoelectric ZnO nanorod carpet as a NEMS vibrational energy harvester, Nano Energy 10 (2014) 71–82.

[2] X. Y. Li, M. X. Chen, R. M. Yu, T. P. Zhang, D. S. Song, R. R. Liang, Q. L. Zhang, S. B. Cheng, L. Dong, A. L. Pan, Enhancing light emission of ZnO-nanofilm/Si-micropillar heterostructure arrays by piezo-phototronic effect, Adv. Mater. 27 (2015) 4447–4453.

[3] C. P. Le, E. Halvorsen, O. Sorasen, E. M. Yeatman, Wideband excitation of an

electrostatic vibration energy harvester with power-extracting end-stops, Smart Mater. Struct. 22 (2013) 075020.

[4] C. P. Le, E. Halvorsen, MEMS electrostatic energy harvesters with end-stop effects, J. Micromech. Microeng. 22 (2012) 074013.

[5] P. Simon, Y. Gogotsi, Materials for electrochemical capacitors, Nat. Mater. 7 (2008) 845–854.

[6] T. M. Dinh, A. Achour, S. Vizireanu, G. Dinescu, L. Nistor, K. Armstrong, D. Guay, D. Pech, Hydrous RuO_2/carbon nanowalls hierarchical structures for all-solid-state ultrahigh-energy-density micro-supercapacitors, Nano Energy 10 (2014) 288–294.

[7] C. Heubner, C. Lammel, N. Junker, M. Schneider, A. Michaelis, Microscopic in-operando thermography at the cross section of a single lithium ion battery stack, Electrochem. Commun. 48 (2014) 130–133.

[8] A. Varpula, S. Laakso, T. Havia, J. Kyynäräinen, M. Prunnila, Harvesting vibrational energy using material work functions, Sci. Rep. 4 (2014) 6799.

[9] K. Chen, D. Xue, Materials chemistry toward electrochemical energy storage, J. Mater. Chem. A 4 (2016) 7522–7537.

[10] T. Q. Lin, I. W. Chen, F. X. Liu, C. Y. Yang, H. Bi, F. F. Xu, F. Q. Huang, Nitrogen-doped mesoporous carbon of extraordinary capacitance for electrochemical energy storage, Science 350 (2015) 1508–1512.

[11] T. Menanteau, C. Benoit, T. Breton, C. Cougnon, Enhancing the performance of a diazonium-modified carbon supercapacitor by controlling the grafting process,

Electrochem. Commun. 63 (2016) 70–73.

[12] K. Yoshima, H. Munakata, K. Kanamura, Fabrication of micro lithium-ion battery with 3D anode and 3D cathode by using polymer wall, J. Power Sources 208 (2012) 404–408.

[13] Z. L. Wang, Piezopotential gated nanowire devices: piezotronics and piezo-phototronics, Nano Today 5 (2010) 512–514.

[14] P. Lu, F. Liu, D. Xue, H. Yang, Y. N. Liu, Phase selective route to $Ni(OH)_2$ with enhanced supercapacitance: performance dependent hydrolysis of $Ni(Ac)_2$ at hydrothermal conditions, Electrochim. Acta 78 (2012) 1–10.

[15] L. Li, J. B. Zhang, Z. W. Peng, Y. L. Li, C. T. Gao, Y. S. Ji, R. Q. Ye, N. D. Kim, Q. F. Zhong, Y. Yang, H. L. Fei, G. Ruan, J. M. Tour, High-performance pseudocapacitive microsupercapacitors from laser-induced graphene, Adv. Mater. 28 (2016) 838–845.

[16] F. Liu, S. Y. Song, D. Xue, H. J. Zhang, Folded structured graphene paper for high performance electrode materials, Adv. Mater. 24 (2012) 1089–1094.

[17] Z. S. Wu, X. L. Feng, H. M. Cheng, Recent advances in graphene-based planar micro-supercapacitors for on-chip energy storage, Nat. Sci. Rev. 1 (2014) 277–292.

[18] J. Lin, Z. W. Peng, Y. Y. Liu, F. Ruiz-Zepeda, R. Q. Ye, E. L. G. Samuel, M. J. Yacaman, B. I. Yakobson, J. M. Tour, Laser-induced porous graphene films from commercial polymers, Nat. Commun. 5 (2014) 5714.

[19] W. Sun, X. Y. Chen, Preparation and characterization of polypyrrole films for

three-dimensional micro supercapacitor, J. Power. Sources 193 (2009) 924–929.

[20] W. Sun, R. L. Zheng, X. Y. Chen, Symmetric redox supercapacitor based on micro-fabrication with three-dimensional polypyrrole electrodes, J. Power. Sources 195 (2010) 7120–7125.

[21] J. Chmiola, C. Largeot, P. Taberna, P. Simon, Y. Gogotsi, Monolithic carbide-derived carbon films for micro-supercapacitors, Science 328 (2010) 480–483.

[22] D. N. Futaba, K. Hata, T. Yamada, T. Hiraoka, Y. Hayamizu, Y. Kakudate, O. Tanaike, H. Hatori, M. Yumura, S. Iijima, Shape-engineerable and highly densely packed single-walled carbon nanotubes and their application as super-capacitor electrodes, Nat. Mater. 5 (2006) 987–994.

[23] D. Pech, M. Brunet, H. Durou, P. Huang, V. Mochalin, Y. Gogotsi, P. Taberna, P. Simon, Ultrahigh-power micrometre-sized supercapacitors based on onion-like carbon, Nat. Nanotech. 5 (2010) 651–654.

[24] Z. S. Wu, K. Parvez, X. L. Feng, K. Mullen, Graphene-based in-plane micro-supercapacitors with high power and energy densities, Nat. Commun. 4 (2013) 2487.

[25] S. Desplobain, G. Gautier, J. Semai, L. Ventura, M. Roy, Investigations on porous silicon as electrode material in electrochemical capacitors, Phys. Stat. Sol. C 4 (2007) 2180–2184.

[26] F. Thissandier, L. Dupre, P. Gentile, T. Brousse, G. Bidan, D. Buttard, S. Sadki, Ultra-dense and highly doped SiNWs for micro-supercapacitors electrodes,

Electrochim. Acta 117 (2014) 159–163.

[27] N. Berton, M. Brachet, F. Thissandier, J. L. Bideau, P. Gentile, G. Bidan, T. Brousse, S. Sadki, Wide-voltage-window silicon nanowire electrodes for micro-supercapacitors via electrochemical surface oxidation in ionic liquid electrolyte, Electrochem. Commun. 41 (2014) 31–34.

[28] L. Oakes, A. Westover, J. W. Mares, S. Chatterjee, W. R. Erwin, R. Bardhan, S. M. Weiss, C. L. Pint, Surface engineered porous silicon for stable, high performance electrochemical supercapacitors, Sci. Rep. 3 (2013) 3020.

[29] S. Chatterjee, R. Carter, L. Oakes, W. R. Erwin, R. Bardhan, C. L. Pint, Electrochemical and corrosion stability of nanostructured silicon by graphene coatings: toward high power porous silicon supercapacitors, J. Phys. Chem. C 118 (2014) 10893−10902.

[30] K. Grigoras, J. Keskinen, J. Ahopelto, M. Prunnila, Porous silicon electrodes for high performance integrated supercapacitors, in: Proceedings of the Electronics System-Integration Technology Conference (ESTC), 2014, pp.1–3.

[31] D. S. Gardner, C. W. Holzwarth III, Y. Liu, S. B. Clendenning, W. Jin, B. K. Moon, C. Pint, Z. Chen, E. Hannah, R. Chen, C. P. Wang, C. Chen, E. Mäkilä, J. L. Gustafson, Integrated on-chip energy storage using porous-silicon electrochemical capacitors, Presented at the International Electron Devices Meeting (IEDM), 2014.

[32] K. Grigoras, J. Keskinen, L. Grönberg, J. Ahopelto, M. Prunnila, Coated porous Si for high performance on-chip supercapacitors, J. Phys. Conf. Ser. 557 (2014)

012058.

[33] D. S. Gardner, C. W. Holzwarth III, Y. Liu, S. B. Clendenning, W. Jin, B. Moon, C. Pint, Z. Chen, E. C. Hannah, C. Chen, C. Wang, E. Mäkilä, R. Chen, T. Aldridge, J. L. Gustafson, Integrated on-chip energy storage using passivated nanoporous-silicon electrochemical capacitors, Nano Energy 25 (2016) 68–79.

[34] K. Grigoras, J. Keskinen, L. Grönberg, E. Yli-Rantala, S. Laakso, H. Välimäki, P. Kauranen, J. Ahopelto, M. Prunnila, Conformal titanium nitride in a porous silicon matrix: a nanomaterial for in-chip supercapacitors, Nano Energy 26 (2016) 340–345.

[35] A. Douglas, N. Muralidharan, R. Carter, K. Share, C. L. Pint, Ultrafast triggered transient energy storage by atomic layer deposition into porous silicon for integrated transient electronics, Nanoscale 8 (2016) 7384–7390

[36] A. P. Cohn, W. R. Erwin, K. Share, L. Oakes, A. S. Westover, R. E. Carter, R. Bardhan, C. L. Pint, All silicon electrode photocapacitor for integrated energy storage and conversion, Nano Lett. 15 (2015) 2727–2731.

[37] X. G. Liu, P. R. Coxon, M. Peters, B. Hoex, J. M. Cole, D. J. Fray, Black silicon: fabrication methods, properties and solar energy applications, Energy Environ. Sci. 7 (2014) 3223–3263.

[38] M. Gharghi, S. Sivoththaman, Formation of nanoscale columnar structures in silicon by a maskless reactive ion etching process, J. Vac. Sci. Technol. A 24 (2006) 723–727.

[39] L. Mueller, I. Kapplinger, S. Biermann, W. Brode, M. Hoffmann, Infrared

emitting nanostructures for highly efficient microhotplates, J. Micromech. Microeng. 24 (2014) 035014.

[40] S. Leopold, L. Mueller, C. Kremin, M. Hoffmann, Online monitoring of the passivation breakthrough during deep reactive ion etching of silicon using optical plasma emission spectroscopy, J. Micromech. Microeng. 23 (2013) 074001.

[41] F. Gao, G. Lewes-Malandrakis, M. T. Wolfer, W. Muller-Sebert, P. Gentile, D. Aradilla, T. Schubert, C. E. Nebel, Diamond-coated silicon wires for supercapacitor applications in ionic liquids, Diam. Relat. Mater. 51 (2015) 1−6.

[42] D. Aradilla, F. Gao, G. Lewes-Malandrakis, W. Muller-Sebert, D. Gaboriau, P. Gentile, B. Iliev, T. Schuber, S. Sadki, G. Bidan, C. E. Nebel, A step forward into hierarchically nanostructured materials for high performance micro-supercapacitors: Diamond-coated SiNW electrodes in protic ionic liquid electrolyte, Electrochem. Commun. 63 (2016) 34–38.

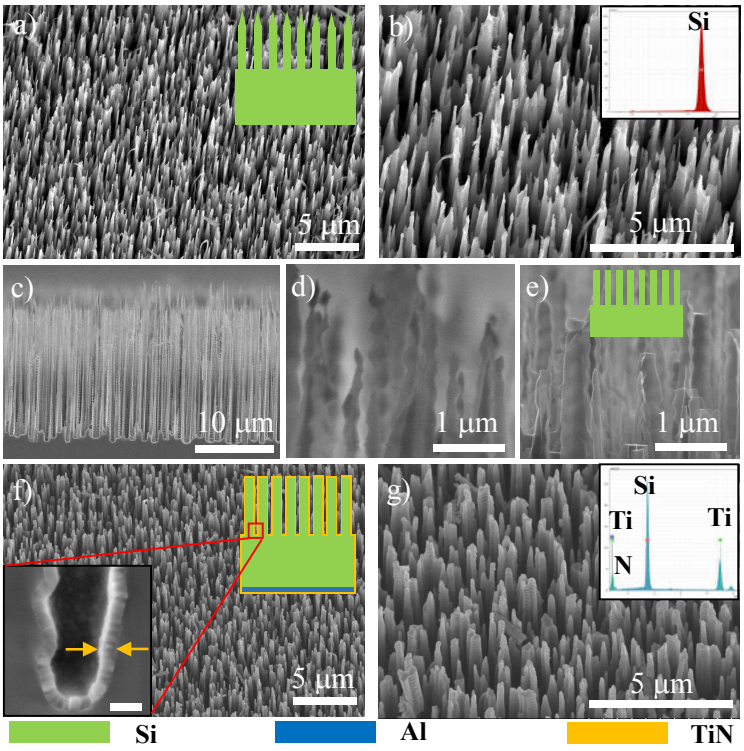

Fig. 1. SEM images: (a–b) Top view, and (c) cross-section view of pristine Si-NR. Si-NR tips before (d) and after (e) hydrogen smoothing. (f–g) Si-NR/TiN electrode. Inset sketches in (a), (e), (f) respectively illustrate the configuration of pristine Si-NR, smoothed Si-NR, Si-NR/TiN. Inset cross-section SEM image in (f) shows the TiN nano layer with ~ 30 nm thickness (scale bar: 50 nm). Insets in (b) and (g) display the EDX spectrums.

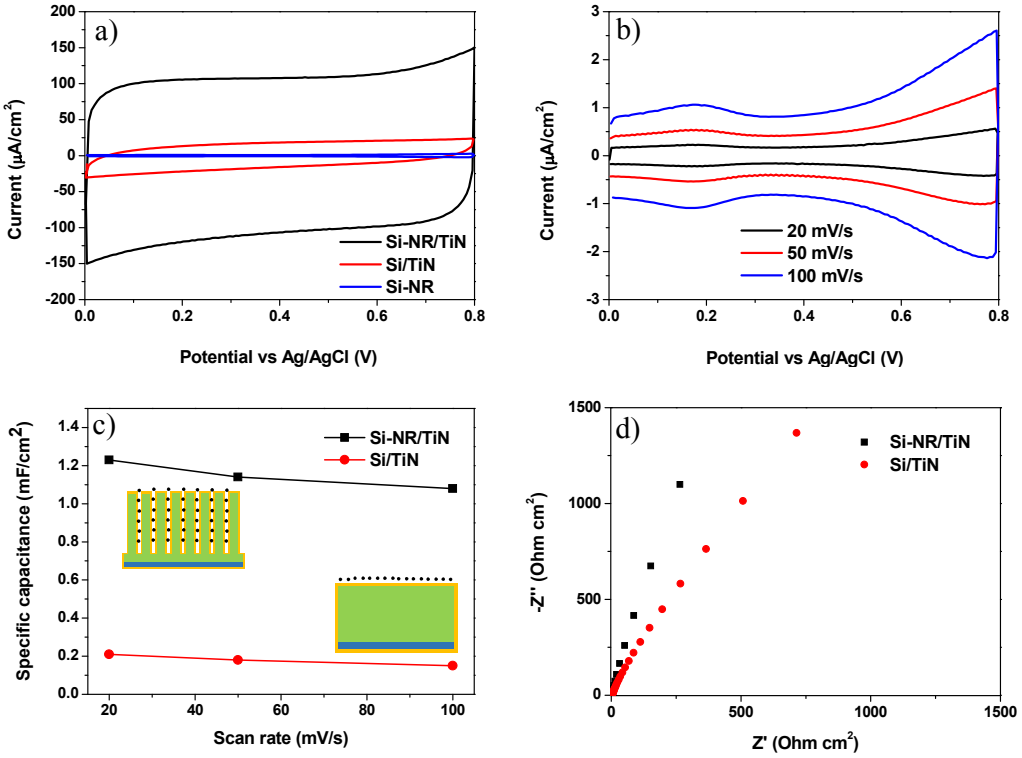

Fig. 2. (a) CV curves recorded at 100 mV/s, (b) CV curves of Si-NR at varying scan rates. (c) Capacitance of Si-NR/TiN and Si/TiN. (d) EIS study.

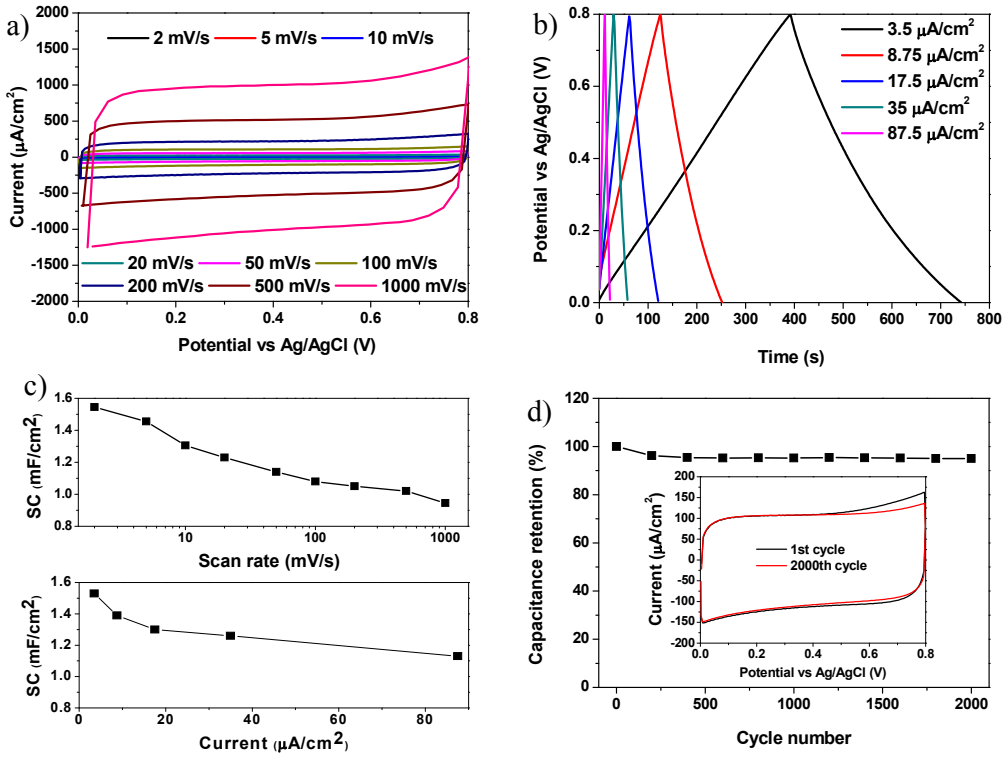

Fig. 3. (a) CV curves and (b) GCD curves of Si-NR/TiN electrode, (c) Calculated capacitance, (d) Cycling performance evaluated at 100 mV/s.