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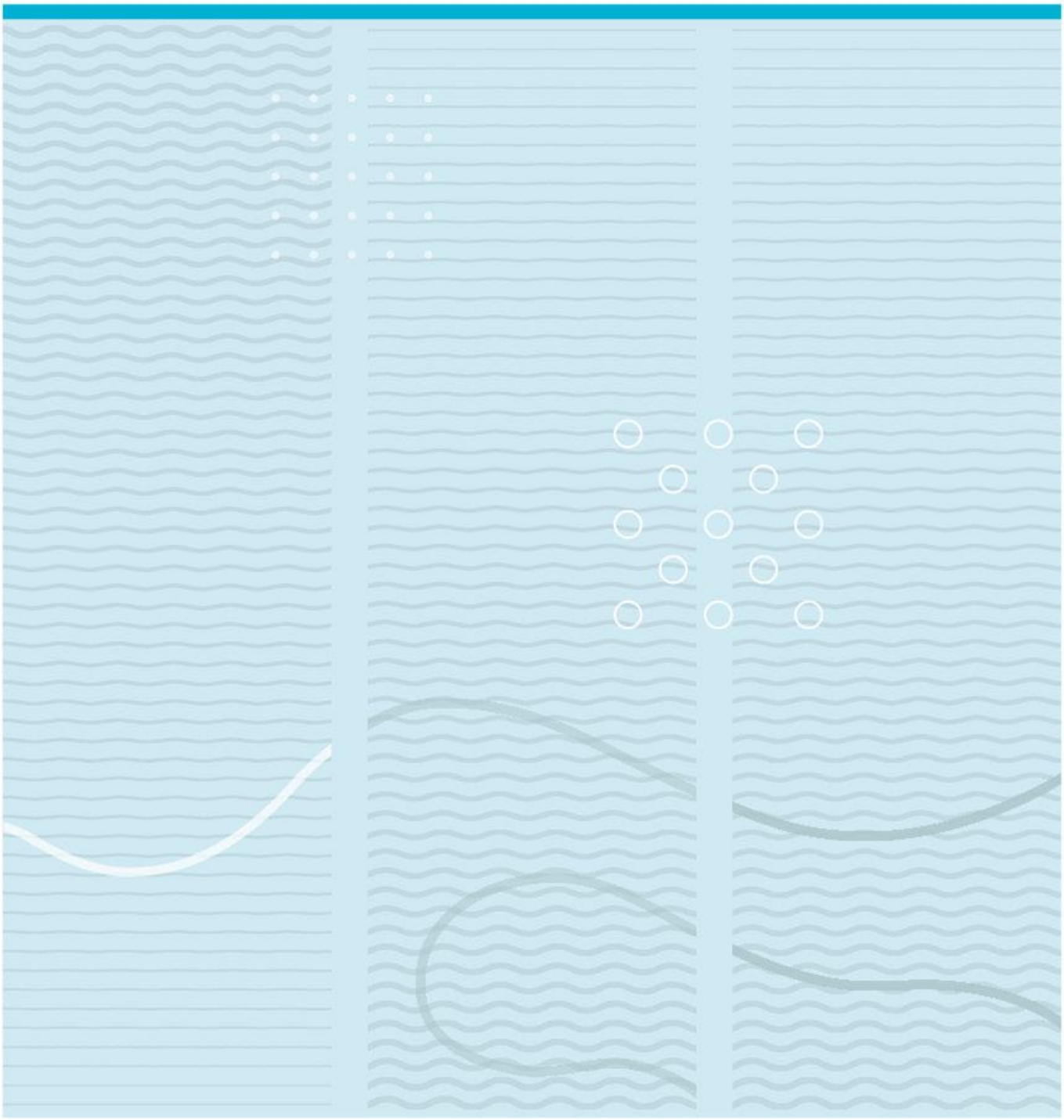
Low Noise Amplifier Design for Hybrid Ultrasound CMUT/Piezoelectric Probes.

CMUT receiver amplifier designs in AMS-0.35µm CMOS process



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This work is dedicated to my parents and my sisters, for their immense support.

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Summary

This thesis focuses on the analysis and design of low-noise amplifiers (LNAs) specifically tailored for medical ultrasound imaging. The objective is to develop amplifiers that can effectively sense signals from a Capacitive Micromachined Ultrasonic Transducer (CMUT) used in the Dual-Frequency Hybrid Ultrasonic Transducer (DHUT) system. Two amplifier topologies, namely the common source (with resistive feedback) and common gate configurations, were implemented using the AMS-0.35µm CMOS process.

To facilitate the amplifier design, an existing analytical model for a collapsed CMUT array was adapted to investigate the CMUT's frequency response and determine its center frequency. The small signal model and noise characteristics were thoroughly analyzed to guide design parameter decisions, employing the g_m/I_D based design methodology for CMOS analog circuits.

The common source amplifier achieved a minimum noise figure of 4.52 dB, which increased to 6.98 dB with the inclusion of resistive feedback. The common gate amplifier achieved a minimum noise figure of 12.49 dB. Various g_m/I_D combinations for the transistors in each amplifier were explored, with a focus on noise performance. Additional performance metrics such as gain, unity gain frequency, and power consumption were evaluated for each design point.

The resistive feedback common source amplifier exhibited a low-frequency gain of 25 dB, a gain of 20 dB at the center frequency (7 MHz), and an approximate unity gain frequency of 85 MHz with a 10 pF capacitive load. The common gate amplifier featured a low-frequency gain of approximately 35 dB, a gain of 24 dB at the center frequency, and an approximate unity gain frequency of 114 MHz with the same capacitive load. Both amplifiers consumed approximately 189 µW of power.

Contents

1 Introduction

Medical ultrasound imaging has experienced significant advancements marked by improvements in image quality and data acquisition speed, resulting in its increased adoption. Also, the adoption of digital imaging systems has further enhanced image quality. The flexibility of digital imaging systems enables the adoption of various algorithms for tasks such as image enhancement, image reconstruction and analysis. However, the quality of the acquired data constrains the effectiveness of these algorithms.

A major component of digital ultrasound imaging systems is the analog front-end, which includes the transducer and associated electronics. The analog front-end connects the digital system and the target under examination. Although digital signal processing techniques can improve imaging capabilities, the analog front-end generally determines the performance limits of the overall system. Among the challenges faced by analog front-ends, the low noise amplifier is often a bottleneck. Its primary objective is to amplify the signal from the transducer with minimal introduction of noise and distortion.

For ultrasound transducers in medical applications, various amplifier designs have been proposed in literature. The focus of these works has been to ensure that the amplifier's noise is relatively low, while having a high linearity by utilizing various topologies and schemes. In [1], a design which includes an inverter-based OTA (Operational Transconductance Amplifier) input stage, a common source stage, current reuse techniques via current mirrors for the active load of the common source stage and a common mode feedback architecture was proposed. The input stage was based on the OTA in [2] and the amplifier has a single-ended to differential operation. Also, a relevant scheme found in literature was noise cancellation, which has been achieved via a feedforward network [3]–[7], and a single-ended to differential network [8]–[11].

A general architecture of the feedforward noise cancellation scheme is shown in Figure 1 - 1. It consists of a matching stage, which matches the resistance of the source (transducer) for maximum power transfer, an auxiliary, voltage sensing or noise cancelling stage which also amplifies the input, and combining or summing network which sums the output signal from the matching auxiliary amplifier. Noise is cancelled via this architecture because the matching stage and auxiliary stage amplifier topologies are selected such that the noise generated in both amplifiers are antiphase and would therefore cancel out in the summing stage [3]–[7]. Also, this scheme cancels harmonic distortion, as demonstrated in [3], [6].

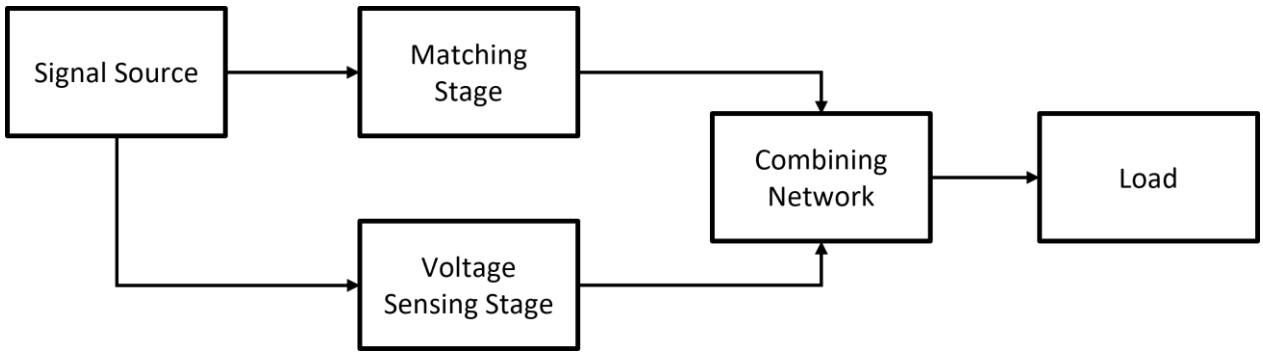

Figure 1 - 1 General Feedforward Noise Cancellation Scheme [3], [7].

The noise cancellation single-ended to differential amplifiers utilize the CG-CS (Common Gate – Common Source) topology shown in Figure 1 - 2. In this topology, the common gate stage is used to match the signal source's resistance and the common source stage cancels the noise in the common gate stage by ensuring the noise signal appear at its output. The noise is therefore cancelled in the common mode of the differential signal at the output [8]–[11]. Also, due to its differential nature, second harmonic distortion is minimized, resulting in improved linearity and improved fidelity for received second harmonic echoes utilized in some ultrasound imaging schemes.

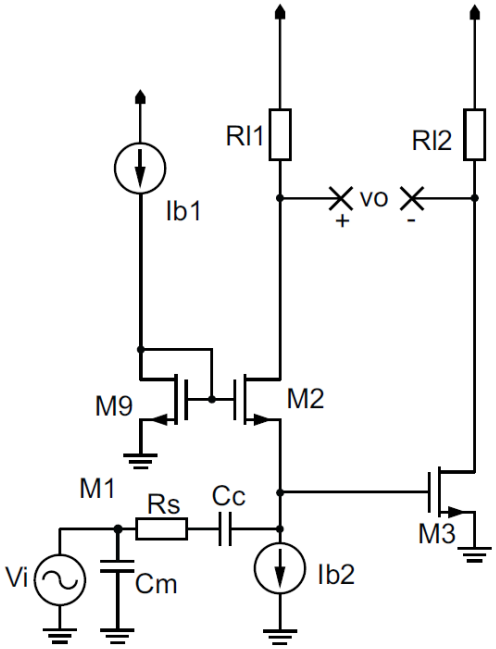

Figure 1 - 2 Typical CG-CS Topology [8]–[11].

Considering these designs [1]–[11], the observed building blocks in the amplifier topologies are the common source and common gate amplifiers. Therefore, this thesis aims to design and analyze the

common source and common gate amplifier topologies suitable for interfacing with the Capacitive Micromachined Ultrasonic Transducer (CMUT) discussed in Section 2.3.2. This was driven by the need to gain a fundamental understanding of their behavior, particularly focusing on noise performance, to facilitate the proper development of more complex topologies. To achieve the aims of this thesis, an existing analytical (circuit) CMUT model was adapted for the CMUT as discussed in Section 2.3.2, to understand its behaviour and determine the center frequency, and specifications for the amplifier were developed in consideration of the CMUTs behaviour, available constraints, and the CMOS process. Furthermore, the noise analysis and the design of the common source and common gate amplifier based on the specifications using the g_m/I_D methodology [12], [13] discussed in Section 2.5, was carried out.

The thesis is outlined as follows: Chapter 2 introduces ultrasound, ultrasound imaging, including a discussion on transducers and the modelling of the CMUT, as well as considerations for amplifier design, which includes noise and linearity. Building upon this foundation, Chapter 3 presents the amplifier specifications and details the design process for each amplifier, including the design decisions made. The outcomes of the designed amplifiers and their corresponding analysis and discussions are presented in Chapter 4. In Chapter 5 conclusions and recommendations for future work are presented.

2 Theory and Background

2.1 Acoustic Basics – Brief Overview

Acoustic waves in the frequency range of 20 Hz to 20 kHz are generally acknowledged as falling within the audible spectrum for the human auditory system. However, when the frequency of acoustic waves exceeds 20 kHz, they are classified as ultrasonic signals or ultrasound, beyond the perception of humans. These acoustic signals possess wave-like characteristics that facilitate their description using parameters such as wavelength, amplitude, period, velocity, energy, and power [14].

The velocity of acoustic signals experiences variability as they propagate through different media, establishing the foundational principles for a wide range of ultrasound technologies and applications. In contrast to electromagnetic waves (not considering the particle duality), acoustic waves manifest as pressure waves that travel through a medium, undergoing attenuation or a decrease in intensity and amplitude. This attenuation primarily arises from the conversion of energy in the propagating acoustic wave to heat, as well as losses due to the expanding wavefront of the propagating acoustic wave in the medium, commonly known as beam spreading loss [15], characterized by decreased energy per unit area.

An important property which defines the interaction between a medium and propagating acoustic waves is the characteristic acoustic impedance. It quantifies the medium's resistance to the transmission of acoustic energy or its resistance to changes caused by mechanical disturbances and is calculated as the product of the medium's density and the speed of sound in the medium [14]. The unit of measurement employed to quantify the characteristic acoustic impedance is referred to as the Rayl.

2.2 Ultrasound Imaging System

Ultrasound imaging involves a series of essential processes, which include the transmission of ultrasound signals directed towards a target or sample, the reception and detection of the resulting echoes, and subsequent processing of the received ultrasound signals through various schemes. In ultrasound systems, the imaging process involves the integration of several hardware blocks or modules. Figure 2 - 1 illustrates a widely employed hardware architecture for ultrasound systems, showing the general arrangement of these constituent modules.

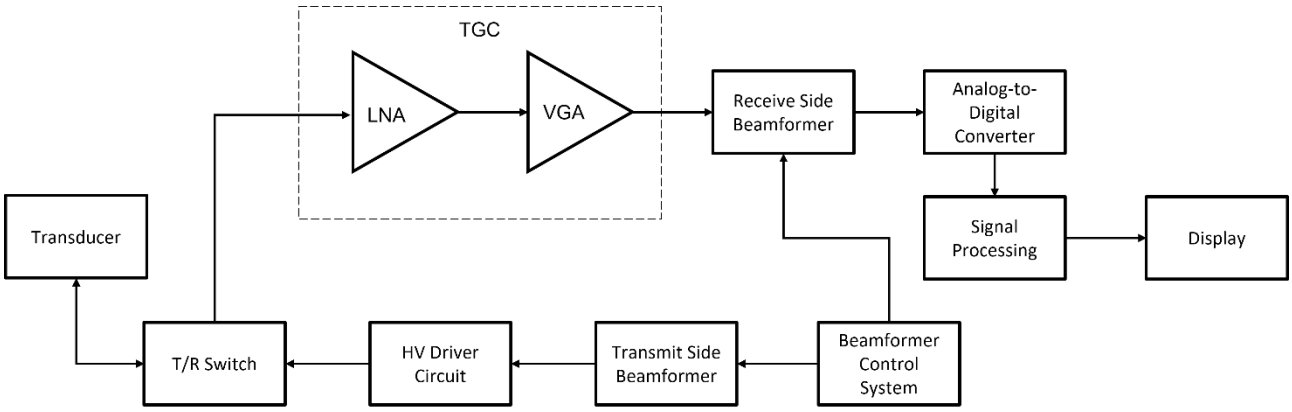

Figure 2 - 1 Ultrasound System Hardware Architecture [16].

First, for transmitting ultrasound signals, the transmit beamformer circuit plays a vital role. It generates a delay pattern in the time domain and complex weights in the amplitude domain, which are based on the desired characteristics of the ultrasound beam to be transmitted [16]. These characteristics determine factors such as beam direction and focusing [17]. The outputs of the transmit beamformer are then amplified by the transducer driving circuit, increasing their voltage to several tens of volts. The waveform that drives the transducer elements can take various shapes, such as square pulses which is the most common, sine waves, or Gaussian pulses, depending on the desired ultrasound transmission. Generally, square pulses are generated using level shifters which could increase the voltage level in one step or several steps. The generated voltages are several tens of volts; therefore, High Voltage CMOS process technologies are generally employed in the design and fabrication of level shifters [18].

For receiving the ultrasound echo, a critical component is the transmit/receive (T/R) switch. Its purpose is to isolate and protect the low-voltage receive circuitry from the high-voltage pulses generated during transmission. By selectively routing the signals, the T/R switch ensures that the receive circuitry is protected from potential damage caused by the high voltages from the transmission circuit. Passive diode networks find frequent application as T/R switches, leveraging the voltage disparity between transmit and receive signals. Also, while a single high voltage NMOS can function as a T/R switch [19], to ensure effective bidirectional isolation between the transmit and receive circuitry, a typical approach involves employing two high-voltage transistors connected in a back-to-back configuration, serving as a T/R switch or the core of other complex switching networks. Another essential component on the receive frontend is the low-noise amplifier (LNA) which is the focus of this work. It plays a crucial role in amplifying the weak ultrasound echoes received by the transducer. Following this, the next component in the signal chain is the variable gain amplifier, which

is used to implement a feature called time-gain compensation (TGC), enhancing the accuracy of the received echoes. TGC adjusts the amplification of the received signals at different time intervals, compensating for the attenuation of the ultrasound waves as they propagate through different tissues. In some architectures, the LNA itself incorporates the TGC feature for linear-in-dB operation [20], [21], while in some other architectures the LNA's gain is "damped" by varying feedback impedance stepwise resulting in discrete gain values [22], [23].

Similar to the transmit frontend, the receive frontend also employs a beamformer. The receive phase beamformer is responsible for generating the appropriate delays and complex weights for the received echoes. This operation complements the transmit beamformer's functionality and helps shape and steer the reception of the ultrasound signals [16].

Finally, the analog-to-digital converter (ADC) performs the crucial task of converting the analog ultrasound signals into a digital format, enabling further post-processing and analysis. The conversion facilitated by the ADC allows for various signal processing techniques to be applied, including filtering, image formation, and enhancement, among others.

2.3 Ultrasonic Transducers

As mentioned earlier, ultrasonic signals are high-frequency sound waves, and as such mechanical vibrations. Ultrasonic transducers convert these vibrations (mechanical energy) into electrical energy, and vice versa, allowing for the transmission and reception of ultrasound waves for use in various applications.

Ultrasound Imaging applications mainly utilize an array of transducer elements, which are arranged and classified based on the specific imaging application. Some of these arrays include linear arrays – whose shape determines the shape of the displayed image, phased arrays – useful for electronic beam steering and 2D arrays – which can scan a volume with no movement [16]. Also, an important rule of thumb with respect to transducer arrays is that the spacing between each element must not be larger than half a wavelength of the operating ultrasound frequency, to minimize grating lobes [24]. Furthermore, it is worth highlighting that 2D arrays exhibit a higher element density per unit area compared to alternative array types. Also, this area reduces with an increase in the selected frequency of operation, resulting in increased electrical resistance, reduced capacitance, however, an overall increase in impedance.

In this work, the designed amplifier is intended to interface with a Dual-Frequency Hybrid Ultrasonic Transducer (DHUT), which consists of a Piezoelectric Ultrasonic Transducer and a Capacitive

Micromachined Ultrasound Transducer (CMUT). The sections that follow give brief descriptions of these transducers.

2.3.1 Piezoelectric Ultrasonic Transducer

Implied in its nomenclature, the Piezoelectric Ultrasonic Transducer utilizes the piezoelectric effect, a phenomenon which describes the generation of an electric field as result of an applied mechanical stress. This phenomenon occurs in materials called piezoelectric materials such as quartz crystals, lead zirconate titanate and polyvinylidene difluoride (PVDF) [25]. The piezoelectric effect is exploited to generate images by transducing ultrasound waves reflected from a sample into electric signals which can be amplified and processed. Also, a complementary phenomenon referred to as the reverse piezoelectric effect which implies resulting mechanical deformations due to an applied electric field, is employed in the generation of the ultrasound waves used for probing the target or sample [14].

In Figure 2 - 2, the basic structure of a Piezoelectric Ultrasonic Transducer for use in ultrasound imaging applications is shown. The transducer consists of a piezoelectric layer which would have electrodes for the application and sensing of electric fields, an impedance matching layer which optimizes the transmission and reception of ultrasound waves by minimizing the acoustic impedance mismatch between the piezoelectric layer and the surrounding medium, and a backing layer designed to have a high acoustic impedance and provide sufficient mechanical damping in other to attenuate reverberations from the piezoelectric layer which can cause distortion in the transmitted ultrasound or interference in the received ultrasound signals [26].

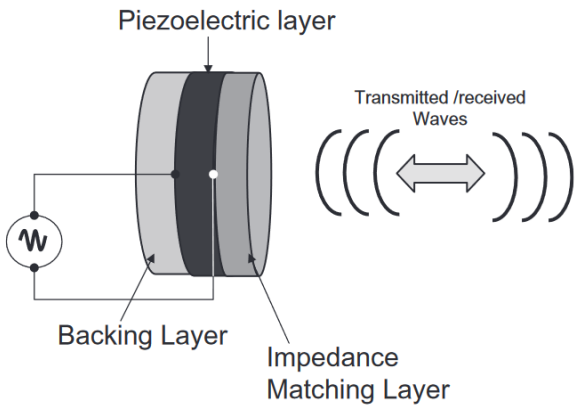

Figure 2 - 2 Basic PZT Structure [26].

To design Piezoelectric Ultrasonic Transducers, finite element modelling is majorly applied, however relevant analytical models in the electrical domain such as the Butterworth-Van Dyke (BVD) model, which models the piezoelectric transducer's behaviour around resonance were developed prior to software models. The BVD model shown in Figure 2 - 3 consists of a capacitance C_0 which is the capacitance of the transducer connected across a resonant series RLC network which represents the mechanical properties of the PZT, where R_1 models the mechanical losses, while L_1 and C_1 model the transducer's behaviour at resonance [27].

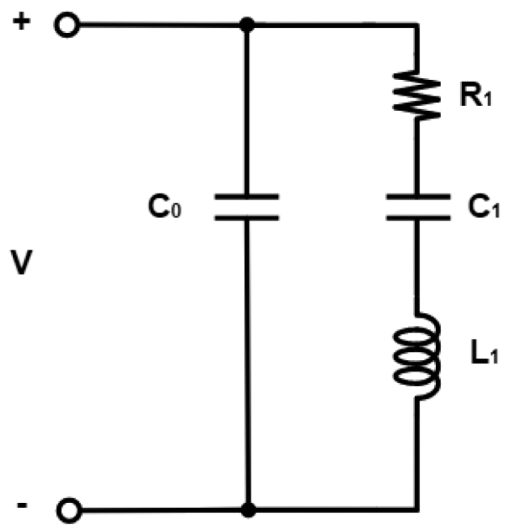

Figure 2 - 3 Butterworth Van Dyke Model for the PZT [28].

2.3.2 Capacitive Micromachined Ultrasonic Transducer

In a CMUT, multiple cells are interconnected in parallel to form a CMUT element. Each individual cell depicted in Figure 2 - 4, comprises a flexible top plate, also known as the top electrode, which is securely anchored along its edges. A small gap exists between this flexible top plate and a stationary bottom plate (electrode). The electrodes are conductive, enabling the formation of a capacitor by utilizing the gap, and since the top electrode is flexible and sensitive to mechanical vibrations, the capacitance of the CMUT cell varies. Conversely, when an alternating voltage is applied to the electrode, the created alternating electric field results in electrostatic attraction and subsequently, vibration of the flexible top electrode [29]. However, electrostatic forces are always attractive, resulting in a vibration which is twice the frequency of the applied voltage [30]. As a result, it is necessary to provide a DC bias voltage that exceeds the amplitude of the applied voltage [30].

Figure 2 - 4 Basic CMUT Cell [31].

The changing capacitance due to impinging mechanical vibrations due to ultrasound is utilized for sensing ultrasound signals as results in changes in voltage or current (depending on the readout circuit) under the constant DC bias. Also, the vibrations due to applied alternating voltage with frequency in the ultrasound range, generate ultrasound waves in the medium around it. The mechanical impedance of the top electrode while vibrating is relatively low, enabling highly efficient coupling of the ultrasound waves into the surrounding medium – an inherent advantage of the CMUT over the PZT, which requires a matching layer [30].

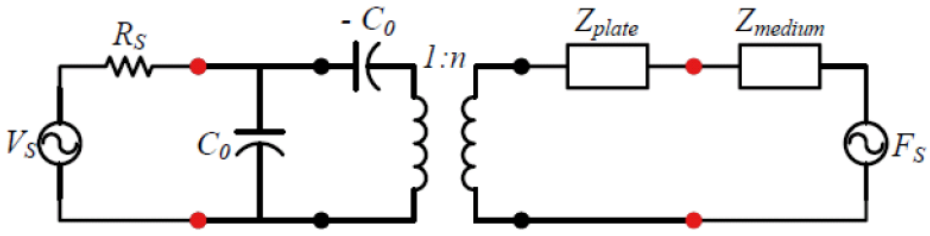

Figure 2 - 5 CMUT Small Signal Electrical Equivalent Circuit [29].

Analytically, the CMUT can be modelled in the electrical domain, using large signal and small signal or linear equivalent circuit models. The linearized (small signal) 1D model of a CMUT cell is shown in Figure 2 - 5. It consists of a transformer, which highlights the electromechanical conversion, a voltage source V_s which drives the CMUT in transmission and its resistance R_s, the capacitance of the CMUT C_0, a negative capacitance $-C_0$ representing the spring softening effect, Z_{plate} the mechanical impedance of the CMUT, the acoustic impedance of the medium Z_{medium} and F_s represents the acoustic pressure force in receive mode [29]. In transmit mode, F_s is replaced with a probe to characterize the transmission properties of the CMUT, conversely, in receive mode, V_s is replaced with a probe for reception characterization.

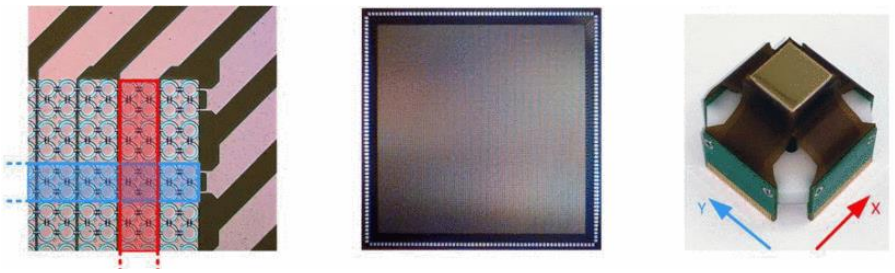

Figure 2 - 6 120+120 Element Crisscross CMUT Array [32].

This thesis focuses on amplifier design for a single element in the 120-element 1D CMUT array shown in Figure 2 - 6. A single element of the 1D array consists of 240 circular CMUT cells parallelly interconnected, with a $100\ \mu m$ pitch for adjacent CMUT cells, and element length of $13.2\ mm$. The combined small signal model of the element would incorporate an acoustic impedance matrix for the interactions between each CMUT cell in the element. This model was simulated in Advanced Design Systems, utilizing previous work done on the design of analytical small and large signal models for collapsed circular CMUT arrays. The receive sensitivity frequency response of the CMUT is shown in Figure 2 - 7, and CMUT's capacitance deduced from the impedance response was 33 pF.

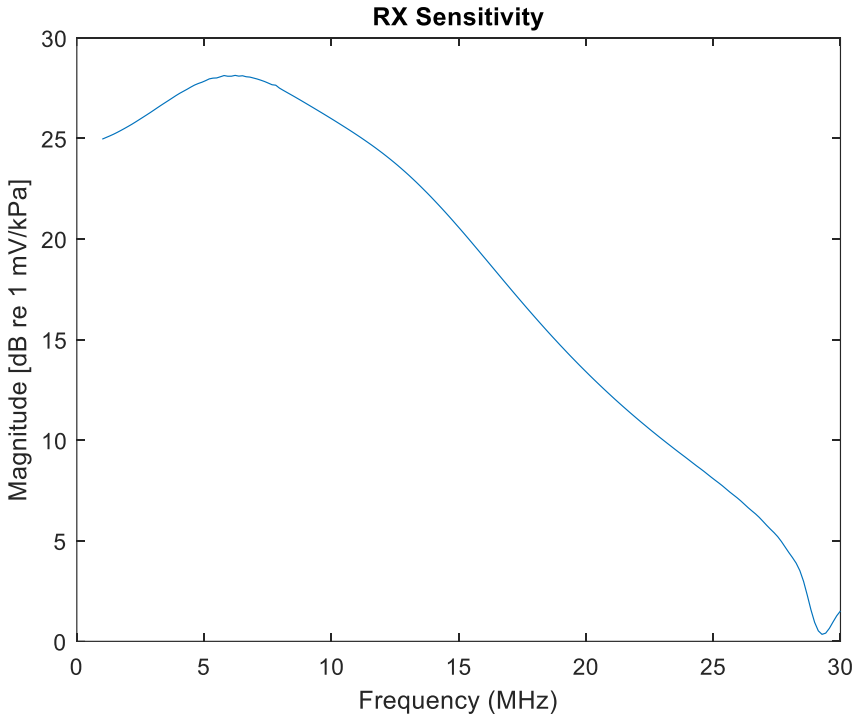

Figure 2 - 7 Simulated CMUT Receive Sensitivity.

2.3.3 Dual-Frequency Hybrid Ultrasonic Transducer

In [33], a design concept of a Dual-Frequency Hybrid Ultrasonic Transducer (DHUT) that incorporates different technologies for separate frequency bands was explored. The hybrid structure presented in Figure 2 - 8, consists of a piezoelectric stack for the lower frequency band and a CMUT array for the higher frequency band, with the CMUT place on top of the piezoelectric stack. The FEM simulations of the structure revealed that the piezoelectric stack introduces ripples in the higher frequency band, and that the introduction of a Room Temperature Vulcanizing (RTV) lens on the device effectively mitigates the interference of CMUT vibrations with the lower frequency band [33]. Furthermore, an array of the DHUT stack was fabricated to validate the simulation results.

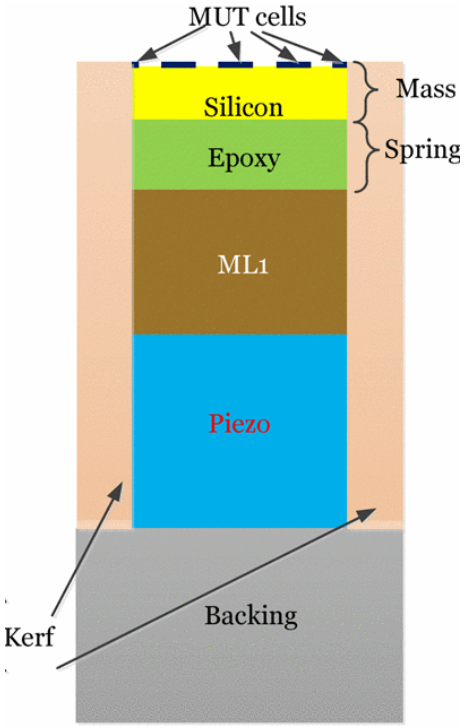

Figure 2 - 8 Dual-Frequency Hybrid Ultrasonic Transducer Structure [33].

Furthermore, the DHUT configuration was improved (structure and prototype shown in Figure 2 - 9) and investigated via simulations and experiments in [34]. Finite Element Modeling (FEM) was employed to design the DHUT stack, with a low-frequency band centered at 7 MHz and a high-frequency band centered at 14 MHz. A DHUT prototype shown Figure 2 - 9 was fabricated, along with two additional prototypes: a single element PZT and a single element CMUT. Electrical impedance measurements in air-coupled operation, as well as transmit and receive acoustic responses in water-coupled operation, were conducted on the fabricated prototypes. Comparative analysis between the

DHUT's low-frequency and high-frequency elements and the pure single-element transducers revealed the effectiveness of the proposed approach in increasing the receive frequency bandwidth.

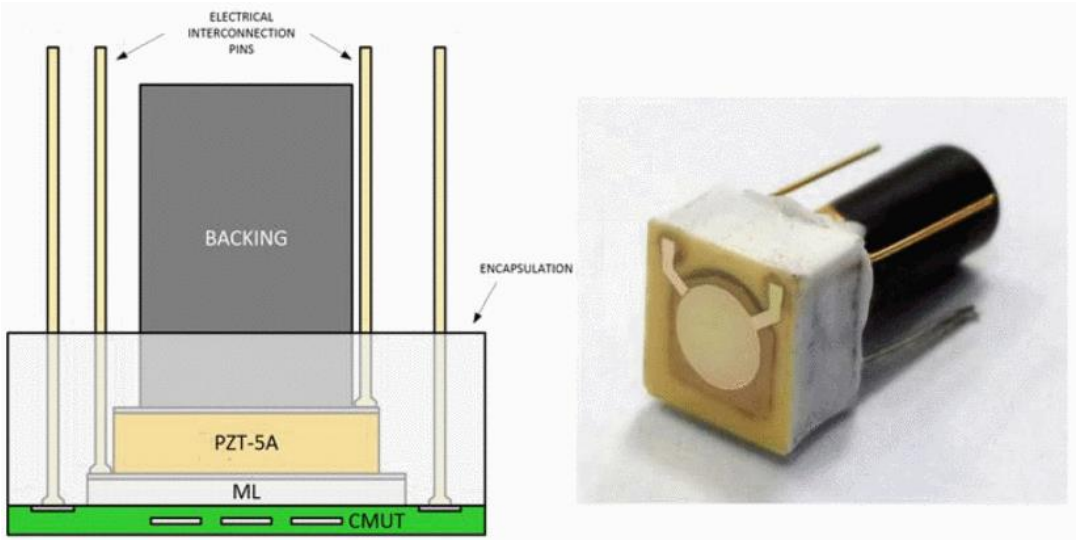

Figure 2 - 9 Improved DHUT and Prototype [34].

Now, for the next iteration in the DHUT's design, the CMUT described in Section 2.3.2 is being utilized and the readout low noise amplifier design is the focus of this work.

2.4 Amplifier Design Considerations

2.4.1 Frequency Response – Gain and Bandwidth

Typically, amplifiers increase the level of the signal at their input, thereby applying a gain to the input signal. However, the gain value varies across frequencies due to factors such as the nature of the active amplifying device or component, the network surrounding the active device, and the load connected to the amplifier's output. The behaviour of the gain of any amplifier over a range of frequencies characterizes its frequency response and in the case of a first order system, its bandwidth. A simplifying perspective is to consider the first order response of an amplifier as system consisting of a gain and a low-pass filter as shown in Figure 2 - 10.

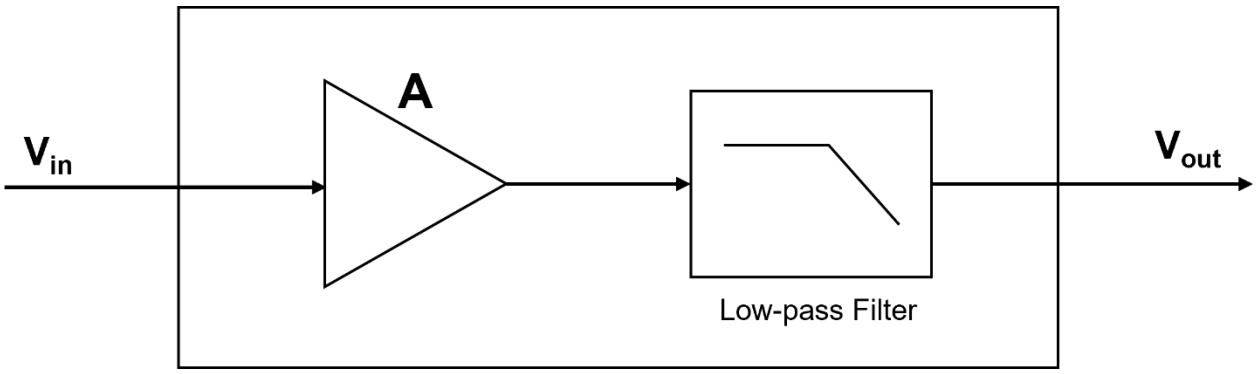

Figure 2 - 10 Simplified Amplifying System.

At low frequencies, the system can be reduced to only the gain component, which has an output conductance – $G_{K,out}$ and therefore a system transconductance – $G_{K,m}$, since the input voltage is converted to a current at the output, which in combination with and the output conductance gives the output voltage, expectedly having a higher level than the input voltage. Therefore, the gain K can be expressed as

$$|K_0| = G_{K,m}/G_{K,out} \tag{2.1}$$

Transiting to higher frequencies, the low-pass filter can now be included. Since this is a first order system, the cutoff frequency of the filter can now be considered dependent on output capacitance of the amplifier, which could be an intrinsic capacitance and/or a load capacitance – C. This can be expressed as,

$$f_{cutoff} = \frac{G_{K,out}}{2\pi C} \tag{2.2}$$

Following this, the frequency response – $|K(f)|$ of the amplifier can be expressed as,

$$|K(f)| = \frac{K_0}{\sqrt{1 + \left(\frac{f}{f_{cutoff}}\right)^2}} \tag{2.3}$$

Furthermore, the unity-gain frequency of the amplifier can be expressed as,

$$f_{ug} = \frac{G_{K,m}}{2\pi C} \tag{2.4}$$

Considering Equation (2.1), it can be observed that for a fixed system transconductance – $G_{K,m}$, the low frequency gain can be defined by properly designing the amplifier to have a specific output conductance – $G_{K,out}$. Also, Equation (2.4) shows that for a fixed system transconductance – $G_{K,m}$, the speed of the amplifier, characterized by its unity gain frequency can be defined by appropriately selecting a corresponding output capacitance.

2.4.2 Noise

In electronics, noise refers to an undesired interference or disturbance present in an electrical signal, which encompasses everything except the intended or desired signal. Noise can originate from diverse sources, leading to various types of noise. In various electronic components, noise sources include low frequency or flicker noise, thermal noise and shot noise. Each of these noise types has distinct characteristics and mechanisms of generation, related to the components present in the circuit, and specifically, the material physics and behaviour of the components in the circuit [35], [36]. "Noise" arises from random processes which cannot be distinctly predicted in the time domain, as a noise signal has multiple frequency components, however, a measure of the power spectrum (power spectral density) of the noise signal at the output of a system has been the important tool used in quantifying the system's noise [36], [37]. Since the generation of noise is a stochastic process, it is important consider the relationship between noise sources in a system. This implies the association between the noise sources in the time domain, or in technical terms, the correlation between the noise sources, which determines the contribution of their noise power densities to the total noise in the system [36]. For a system having only uncorrelated noise sources, the total noise can be expressed as,

$$V_{n,total}^2 = V_{n,1}^2 + V_{n,2}^2 + V_{n,3}^2 + \cdots + V_{n,i}^2 \tag{2.5}$$

Where $V_{n,i}^2$ is the power spectral density of the i^{th} noise source in the system, and $V_{n,total}^2$ is the power spectral density of the total noise in the system. Furthermore, a consideration of a system having two correlated noise sources yield a total noise density given as,

$$V_{n,total}^2 = \left(V_{n,1} + V_{n,2}\right)^2 = V_{n,1}^2 + V_{n,2}^2 + 2CV_{n,1}V_{n,2} \quad (2.6)$$

Where C is the correlation coefficient and has values ranging from -1 to 1, with $C = 0$ implying totally uncorrelated sources, $C = 1$ implying fully correlated sources and $C = -1$ implies that the noise signals are out of phase (180 degrees) [36]. A general form of Equation (2.6) can be expressed as

$$V_{n,total}^2 = \left(V_{n,1} + V_{n,2} + V_{n,3} + \cdots + V_{n,i}\right)^2 \quad (2.7)$$

Where $V_{n,i}$ is the noise "voltage" generated by the i^{th} noise source.

Understanding and mitigating noise is crucial in electronics to ensure optimal signal quality and minimize unwanted disturbances. Following this, brief discussions on the types of noise, as well as how they are represented in important components for this work are presented in the following sections.

2.4.2.1 Thermal Noise

The phenomenon of thermal noise was initially documented by John B. Johnson, who observed a stochastic fluctuation of electrical potential across the terminals of a conductor. This fluctuation was attributed to the random movement of electric charges within the conductor induced by thermal agitation, having similarity with Brownian motion [38]. Johnson's experimental investigations yielded significant observations, demonstrating a direct correlation between the resistance and absolute temperature of the conductor and the magnitude of the mean-square fluctuations in potential experienced throughout the conductor.

As earlier mentioned, the power spectral density of the noise signal has been effective in the analysis of noise in circuits. In resistors, the thermal noise density can be modelled either as a voltage source in series with a "noiseless" resistor or a current source connected parallel to the resistor as shown in Figure 2 - 11.

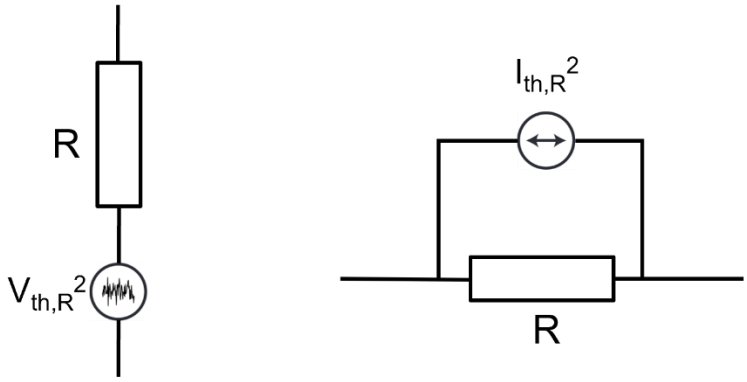

Figure 2 - 11 Thermal Noise Model for a Resistor [35]–[37].

The noise voltage and current density are expressed in Equations (2.8) and (2.9).

$$V_{th,R}^2 = 4kTR \tag{2.8}$$

$$I_{th,R}^2 = 4kT/R \tag{2.9}$$

Where k is the Boltzmann's constant, T is the temperature, R is the resistance of the resistor and the thermal noise voltage and current spectral densities are represent by $V_{th,R}^2$ and $I_{th,R}^2$ respectively. A consideration of a MOSFET as a resistor whose value is controlled by the voltage on third terminal implies that thermal noise is also generated in the MOSFET. In [39], the thermal noise in Field-Effect transistors was modelled as a current source in parallel to the transistor's output (drain-source) as shown in Figure 2 - 12.

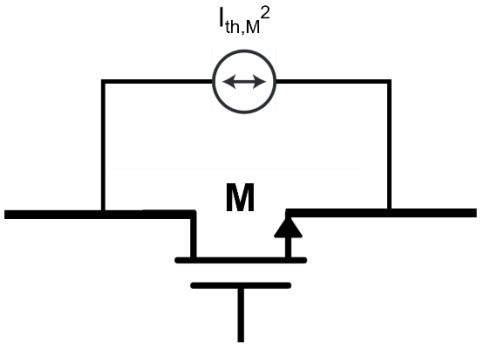

Figure 2 - 12 Thermal Noise Model for MOSFETs [35]–[37].

The noise density was calculated for zero drain voltage and was shown to be proportional to the drain conductance, however with a scaling factor or coefficient which slightly depends on the drain voltage and the transistor's length [39]. The current noise density is expressed as,

$$I_{th,M}^2 = 4kT\gamma_M g_{d0} \quad (2.10)$$

Where g_{d0} represents the conductance across the drain and source for $V_{ds} = 0$, and γ_M the scaling parameter, which has value ranging from $2/3$ to 2. In the saturation region, long channel transistors generally have a γ_M of 2/3 [37].

2.4.2.2 Flicker Noise

Also referred to as to as low-frequency noise, flicker noise is characterized by an unbounded spectral density as the frequency of operation decreases [36]. In semiconductor devices, the primary source of flicker noise is associated with the surface or interface between the materials in the device. This is because the generation and recombination of charge-carriers also occur at the interface between materials in the device, which also implies an interaction between energy states. Extra energy states called surface states are created at the interface, which results in the random entrapment of charge-carriers, which are then later released randomly [36], [37]. In the case of MOSFETs, the interaction between the energy states at the gate-oxide and silicon substrate interface produce flicker noise the transistor's drain current [37].

Improved surface treatment during the manufacture of semiconductor devices can help reduce flicker noise. However, due to process technology variations, the level of flicker noise in each process technology also varies. In MOSFETs, a voltage source at the transistor's gate models the flicker noise in the transistor as shown in Figure 2 - 13.

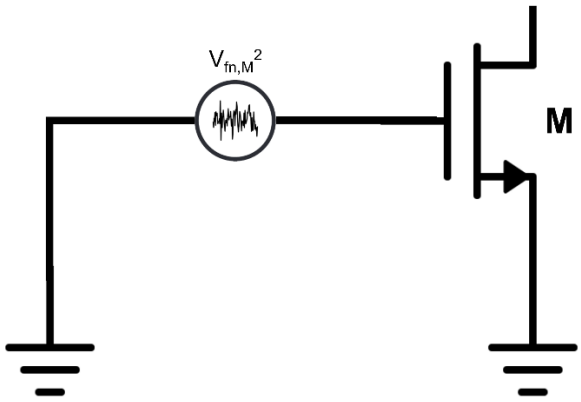

Figure 2 - 13 Flicker noise Model for MOSFETs [35], [37].

The noise voltage density shown in Figure 2 - 13 can be expressed as

$$V_{fn,M}^2 = \frac{1}{f}\frac{K_M}{C_{ox}WL} \tag{2.11}$$

Where f is the frequency of operation, W and L are the transistors width and length respectively, K_M is a process-dependent constant and C_{ox} is the gate oxide capacitance [37].

2.4.2.3 Shot Noise

In semiconductor devices, the flow of current consists of pulses caused by the movement of charge carriers (electrons and holes), with each carrier carrying one electronic charge. These pulses of current can occur when the charge carriers are generated, recombined, or when they traverse a potential barrier or a pn-junction. As a result of these pulses, fluctuations in the current above its average value can arise. These fluctuations in the current values for each pulse are what constitute shot noise [35], [36], [40]. The power spectral density of shot noise is given as a noise current density and expressed as Equation (2.12) [40].

$$I_{shot}^2 = 2qI_{DC} \tag{2.12}$$

Where q is the electronic charge and I_{DC} is the direct current flowing through the device. The power spectral density of shot noise is flat and is therefore white noise [35], [36]. Furthermore, it is modelled by a noise current source connected across a specific property/quantity (usually, a computed resistance) of the semiconductor device [35], [36].

2.4.2.4 Noise Performance

In the analysis of the inherent noise in an electronic circuit, the total noise expression derived at the output is not sufficient to evaluate the circuit's noise performance when compared to other circuits. In the case of amplifiers, the gain of the system also appears in the noise formulation, which could imply that an amplify with low gain would have low noise, which is not the case since a higher gain would mean a higher signal level at the output. Therefore, the output noise or output-referred noise is not necessarily a proper metric for comparing the noise performance of different circuits.

2.4.2.4.1 Input-Referred Noise

One effective metric of comparison which would ensure that system properties (such as gain) are eliminated from comparison is the so-called input-referred noise. The input-referred noise is a measure that quantifies the level of noise present at the input of a circuit or device with an assumption that all the noise in the circuit is generated only at the input. The analysis or determination of the input-referred noise is done such that it produces the same output noise for the circuit being analysed as illustrated in Figure 2 - 14.

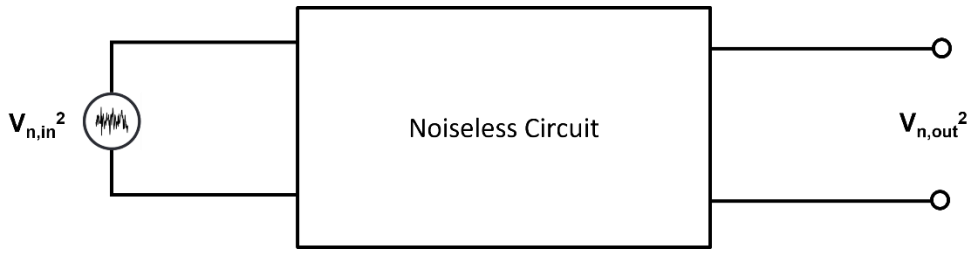

Figure 2 - 14 An Illustration of the Input-referred Noise [37].

2.4.2.4.2 Noise Factor and Noise Figure

An important noise performance metric is the Noise Factor (F) or Noise Figure (NF). It is a measure of the degradation of the Signal-to-Noise Ratio (SNR) from the input of the circuit to the output of the circuit. The SNR of a circuit immediately gives a measure of the quality, fidelity, or clarity of a signal in the presence of noise signals, quantifying the level of the desired signal relative to that of the noise in the circuit. Quantitatively, SNR is calculated as the ratio of the signal power to noise power as expressed in Equation (2.13) and in decibels, Equation (2.14).

$$SNR = S/N \tag{2.13}$$

$$SNR_{dB} = 10\log_{10}(S/N) \tag{2.14}$$

Where S is the signal power and N is the noise power. In cases where voltage is the available quantity, then SNR can be expressed as,

$$SNR_{dB} = 10\log_{10}\left(\frac{V_s^2}{V_n^2}\right) = 20\log_{10}\left(\frac{V_s}{V_n}\right) \quad (2.15)$$

Where V_s and V_n are the rms values of the signal and noise respectively.

In electronic circuits analysis, isolation of the specific circuit is always done, however, it is important to remember that the circuit in question is part of a signal chain, therefore the preceding circuit or stage's output SNR becomes its input SNR, and the Noise Factor and the Noise Figure for the analyzed circuit can be expressed as

$$F = {SNR_{in}}/{SNR_{out}} \quad (2.16)$$

$$NF = 10\log_{10}(F) \quad (2.17)$$

When comparing noise performance of different circuits, it is important to note a lower noise figure implies better noise performance.

2.4.2.4.3 Input/First Stage Noise Performance

In cascaded networks, the noise performance of the input or first stage is very important. This can be observed by considering the noise factor expression in Equation (2.18) developed by Harold Friis [41].

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_i - 1}{G_1 G_2 \cdots G_i} \quad (2.18)$$

Where, G_i is the i^{th} stage's available power gain, F_i is the noise factor of the i^{th} stage and F_{total} is the total noise factor of the system. The expression indicates that a low noise factor and a high gain in the input stage would ensure a low overall noise factor, implying a good noise performance for the system.

In Section 2.2, the ultrasound receive chain was described, and the amplifier is the first stage in the receive chain, therefore, it must be designed to have as low noise as possible.

2.4.3 Linearity

With respect to amplifiers, nonlinearity in the amplifier's gain is an important factor for consideration. In amplifiers, this manifests as gain compression, resulting from the amplification of harmonics of the input signal at different rates [42]. Generally, memoryless, nonlinear systems can be represented by the polynomial in Equation (2.19).

$$f(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \cdots + a_n x^n(t) \qquad (2.19)$$

For an harmonic signal $x(t)$, such that $x(t) = X\cos\omega t$, the a third order polynomial approximation can be expressed as

$$f(t) = a_1 X\cos\omega t + a_2 X^2 cos^2\,\omega t + a_3 X^3 cos^3\,\omega t \qquad (2.20)$$

$$f(t) = \frac{a_2 X^2}{2} + \left(a_1 X + \frac{3a_3 X^3}{4}\right)\cos\omega t + \frac{a_2 X^2}{2}\cos 2\omega t + \frac{a_3 X^3}{4}\cos 3\omega t \qquad (2.21)$$

Considering Equation (2.21) and comparing it with the small signal gain of an amplifier, several observations can be made. Firstly, if either a_1 or a_3 is negative, the gain associated with the fundamental component decreases. Conversely, if both a_1 and a_3 are positive (or negative), the gain increases when the input signal's amplitude is significantly high.

Furthermore, when the signal amplitudes are high, the presence of harmonics becomes significant and can potentially interfere with other signals at the harmonic frequencies. For instance, in medical ultrasound imaging, second harmonic imaging is a preferred method for imaging. This method generates images from the second harmonics produced within the body tissue, demanding higher levels of linearity compared to conventional ultrasound imaging techniques. However, it is important to note that the fundamental component is also reflected from the target. Therefore, in the case of an interface amplifier exhibiting considerable harmonic distortion, the second harmonic signal generated by the amplifier can interfere with the second harmonic signal from the target, which carries important image information.

2.4.4 Negative Feedback

Feedback is an integral part of most physical systems. Interestingly, the theory of negative feedback originated from the field of electronics engineering. In 1928, Harold Black, an electronics engineer at the Western Electric Company, developed the feedback amplifier while searching for stable gain methods for transatlantic telephone repeaters [43]. Since then, feedback techniques have become ubiquitous in electronic circuits, playing a crucial role in their design.

In amplifiers, negative feedback involves a continuous loop where the output signal, or a portion of it, is fed back to the input via a "feedback network". This feedback signal is subtracted from the input signal, generating an error signal. The amplifier then corrects this error signal to generate the desired output signal [44]. Negative feedback plays a crucial role in stabilizing the gain of an amplifier amidst various factors such as process variations, temperature changes, and supply voltage fluctuations [37], [43]–[45]. Additionally, it impacts the input and output impedances, reduces distortion and nonlinear effects, and widens the bandwidth of the amplifier [37], [43]–[45]. However, while reaping these benefits, the overall gain of the amplifier is diminished almost proportionally. To counterbalance this decrease in gain, it is often necessary to introduce an additional amplifier stage [44]. Furthermore, careful design is essential to prevent potential oscillation issues that may arise. Negative feedback is also referred to as degenerative feedback because it curtails or diminishes the output signal [44].

An ideal model of a negative feedback amplifier is depicted in Figure 2 - 15. It consists of an amplifier having a gain – A, referred to as the open loop gain, a feedback network with a gain – β, input signal – u, output signal – y, feedback signal – v and the closed loop gain – A_{CL} [45].

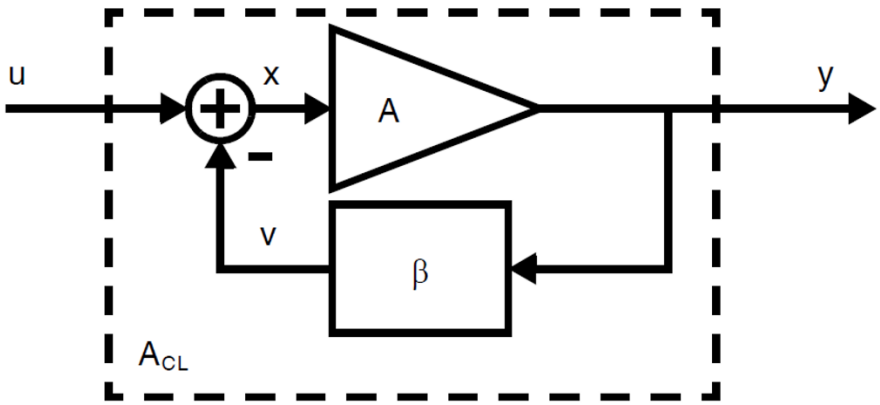

Figure 2 - 15 Negative Feedback Model [45].

Considering the model in Figure 2 - 15, the closed loop gain can be expressed as in Equation (2.22) [45].

$$A_{CL} = \frac{A}{1 + A\beta} \tag{2.22}$$

The term $A\beta$ is referred to as the loop gain, and for $A\beta \gg 1$, the closed loop gain is approximately given as

$$A_{CL} \approx \frac{1}{\beta} \tag{2.23}$$

This implies that for a sufficiently large loop gain, the closed loop gain of the system tends to become independent of the open loop gain. This is desirable, as the open loop gain is susceptible to variations in process, supply voltage and temperature. Furthermore, it is important to state that a large loop gain requires a large open loop gain.

2.5 The g_m/I_D Based Design of CMOS Analog Circuits

The building block of modern CMOS analog circuits is the MOSFET (Metal Oxide Semiconductor Field Effect Transistor), which is in general, a three terminal device that allows for the control of the quantity (voltage, current or resistance) between two terminals, by a third terminal. In the design of various CMOS analog circuits, transistor topologies, operating points or regions, and aspect ratio (refers to the width and channel length of the MOSFET) are necessary factors, as they enable analog electronics designers achieve specific designs for general or specific applications. With respect to this, various analytical models of the MOSFET's behaviour have been developed. These models aim to describe the behaviour of the MOSFET in its various regions of operation. An analytical expression that models the behaviour of the n-channel MOSFET in the saturation region is expressed in Equation (2.24) [37], [43], [45].

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{2.24}$$

Where I_D is the drain current, μ_n is the charge mobility coefficient, C_{ox} is the gate oxide capacitance, W and L are the widths and lengths of the MOSFET respectively, V_{GS} refers to the potential between

the gate and source of the transistor, and V_{th} is the threshold voltage of the transistor, V_{DS} is the drain-source voltage and λ is the channel length modulation coefficient . This expression in Equation (2.24) holds for the transistor in saturation, in which there is no dependence of the transistor's drain current on the drain-source voltage and is characterized by $V_{DS} > V_{GS} - V_{th}$. Also, in the saturation region, the MOSFET's transconductance (g_m) which is defined as the change in its drain current (I_D) with respect to change in the applied gate-source voltage (V_{GS}) can be expressed as Equation (2.25) [37], [43], [45].

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{th})(1 + \lambda V_{DS}) \qquad (2.25)$$

Another region of operation is the triode or linear region, in which the transistor behaves as a voltage-controlled resistor, with $V_{GS} - V_{th}$ being the control voltage. This region is characterized by $V_{DS} < V_{GS} - V_{th}$ and its analytic model expressed as Equation (2.26) [37], [43], [45].

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (2.26)$$

MOSFETS operating in the linear and saturation operating regions are generally referred to as operating in strong inversion. Other inversion regions are weak inversion which implies subthreshold ($V_{GS} < V_{th}$ and $V_{th} - V_{GS} > 100\ mV$) operation and moderate inversion, which lies between weak and strong inversion region of operation. In the subthreshold region, the drain current relationship is no longer a square-law relationship as is the case in the strong inversion region given in Equations (2.24) and (2.26), but is exponentially related to $V_{GS} - V_{th}$, and can be approximated by Equation (2.27) [45].

$$I_D = (n-1)\mu_n C_{ox} \left(\frac{W}{L}\right) V_T^2\, e^{(V_{GS} - V_{th})/nV_T} \qquad (2.27)$$

where V_T is the thermal voltage indicating the subthreshold conduction dependence on temperature and n is a constant with values ranging from 1 to 2 [43], [45].

Other more involved models developed for the MOSFET are the charge sheet model, which applies to long-channel MOS transistors and EKV model which includes allowances for nanoscale design. These models are rather complex, having multiple parameters and further increasing the complexity of hand calculations. Also, the square-law models in Equations (2.24) and (2.26) are also not accurate, as designing with them requires multiple iterations with simulations. This mismatch between the square-law models are due to its inability to model transistors in moderate inversion (an middle ground design region), short channel effects due to nanoscale design, complex structures of modern transistor and the previously mentioned subthreshold conduction [13].

Therefore, several methodologies have been proposed to improve the design experience, and relevant to this work is the g_m/I_D based design methodology [12]. The g_m/I_D parameter can be considered as the transistor efficiency for a specific operating point, as it gives a measure the "amount" of transconductance that is gotten from a transistor for a specific drain bias current, indicating the trade-off between the operating point current and the transconductance [12]. The main motivation for using this methodology is that the g_m/I_D parameter is approximately constant for different CMOS processes, implying that a gm/ID value corresponds to the same regions in the available CMOS process technologies [13]. Furthermore, the g_m/I_D parameter is usually extracted from the available software models for a CMOS processes, and since the design of the CMOS analog circuits is done using these software models, it provides a way to link the device geometry (related to g_m) and bias current to transistor software model and circuit.

In g_m/I_D based design, the g_m/I_D parameter is the knob for design, in that sense, its value for a transistor is selected based on the design problem and has specific connotations. In Figure 2 - 16, the plot g_m/I_D against V_{GS} extracted from the AMS-0.35µm process used in this work is presented. The curve is for the typical NMOS transistor available in the CMOS process for length $L = 0.4\ \mu m$, the curves for other lengths are not shown, but the trend is similar.

As mentioned earlier, the value of the g_m/I_D parameter corresponds to operating regions driven by the inversion level. The g_m/I_D values above 20 for a transistor indicate operation in weak inversion, g_m/I_Dranging from 10 to 20 indicates moderate inversion operation, while g_m/I_D values below 10 indicate strong inversion operation [13].

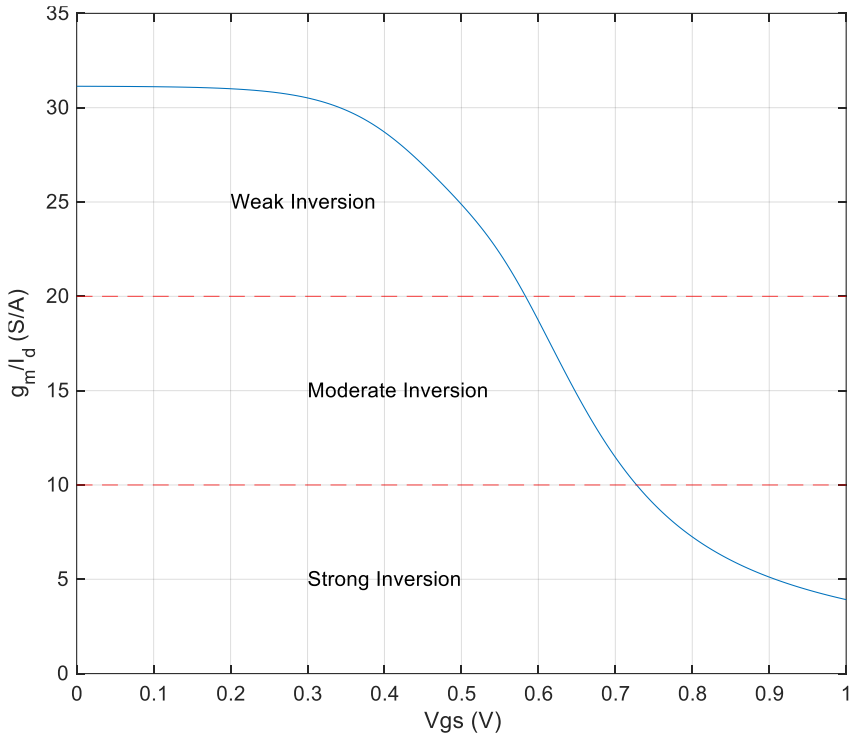

Figure 2 - 16 Extracted g_m/I_D vs V_{GS} curve for NMOS ($L = 0.4\ \mu m$).

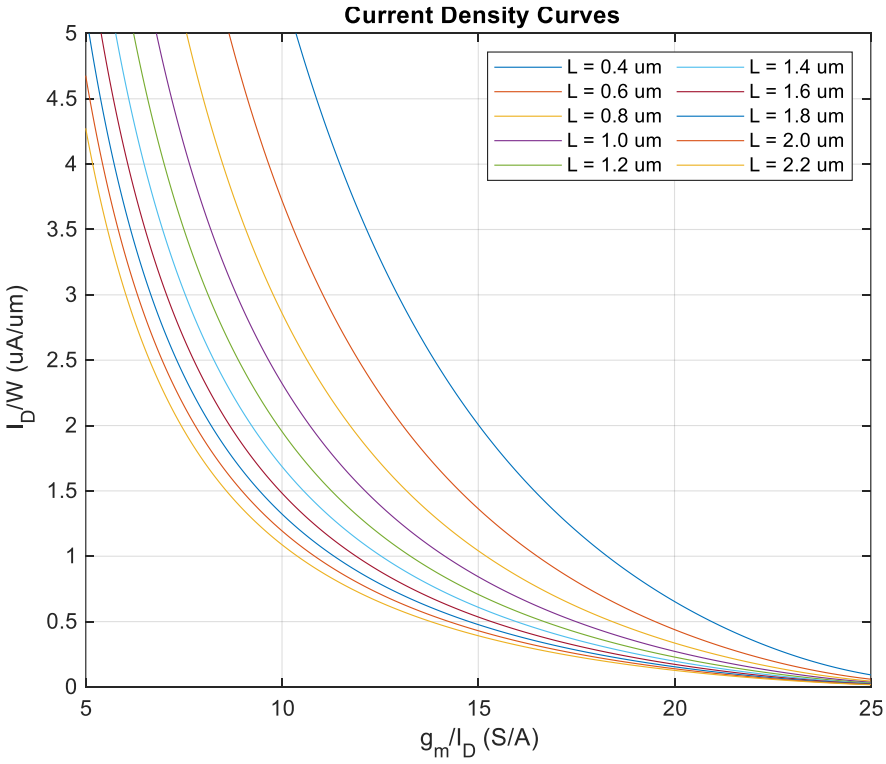

Figure 2 - 17 Extracted I_D/W against g_m/I_D curves for NMOS.

The g_m/I_D parameter being the independent variable in this methodology allows for the control of other important design parameters such as the transistor's current density which defines a measure of the amount of current per unit width (I_D/W) for the transistor to operate at a specified inversion level, and usually measured in $\mu A/\mu m$. Since the inversion level can be specified by the g_m/I_D, then for a specific transistor length and for a specific g_m/I_D (desired level of inversion), the current density (I_D/W) of the transistor can be looked up from the curves of I_D/W against g_m/I_D shown in Figure 2 - 17.

Furthermore, the parameters such the intrinsic gain (g_m/g_{ds}) and transit frequency which determine the speed of the design can be looked up based on the specified inversion level. These parameters are mostly sufficient for designing (sizing) a transistor for a specific role in a circuit's topology.

3 Amplifier Design

As previously discussed, the target of this thesis is to design Low-noise amplifiers (LNA) for Dual-Frequency Hybrid Ultrasound Transducers. The amplifier interfaces a CMUT in receive mode, described in Section 2.3.2, and is designed in the AMS 0.35µm CMOS Process. In this chapter, the design decisions, assumptions, equations, and implementation of the amplifier are reported. This includes the specifications for the amplifier, exploration of simple amplifier technologies and the justification for doing so, as well as the sizing decisions for the transistors in the amplifiers.

3.1 Specifications

To determine the specifications for the amplifier, it is important to understand the properties of the input device, which is the CMUT. Therefore, an initial analytical model of the CMUT was simulated in Advanced Design Systems (ADS) described in Section 2.3.2, with the resulting frequency response shown in Figure 3 - 1.

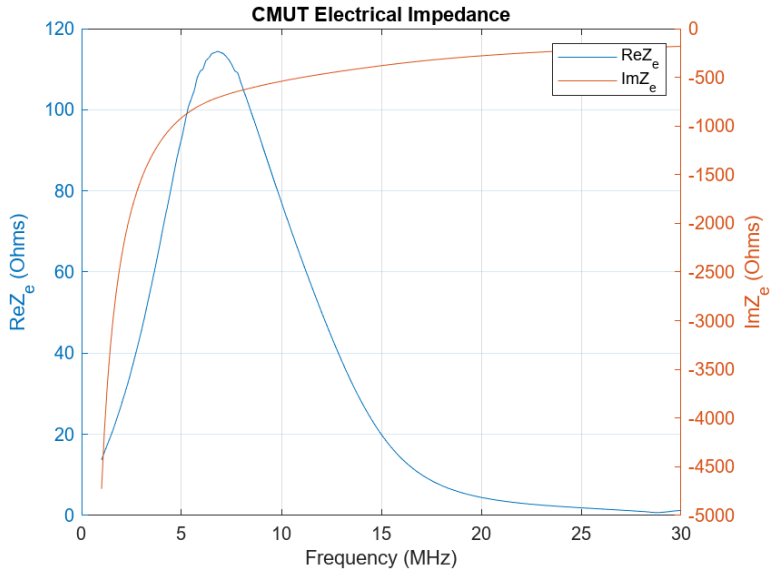

Figure 3 - 1 CMUT Electrical Impedance Frequency Response

The response indicates that the CMUTs resonance frequency is at approximately 7 MHz and having an impedance of 717.76 ∠ 80.83° Ohms, implying a center frequency of 7MHz for the amplifier. For a reasonable fractional bandwidth design, a bandwidth of 10 MHz was specified for the amplifier.

Prior to this work, a test kit had been developed for characterizing the performance of the CMUT. The maxim integrated MAX14822 ultrasound Low-Noise Operational Amplifier was used to amplify

the CMUT response from individual elements in the 1D CMUT array. The IC has 16 channels, with a typical power consumption rating of 5.9 mW and maximum power consumption rating of 9.5 mW in receive mode per channel and was utilized such that one channel is connected to one element in the array. This dictated the power consumption constraint of the designed LNAs.

Furthermore, a major condition for the amplifier is that it introduces as little noise as possible into the signal chain. For this reason, a noise figure less than 3 dB was specified for the amplifiers. Also, power supply specification is given by the CMOS process Technology which is 3.3 V. The maximum area of the amplifier is constrained by the area of one element in the CMUT array, noting that the designed amplifier would be replicated 120 times, which is the number of elements in the CMUT array. This is because each element in the CMUT array requires an interfacing amplifier. The area of one element in the CMUT array is 0.11 mm x 13.2 mm as observed from the specification sheet of the CMUT. This area constrains the size of the amplifier per element, however, the amplifier would be designed to smaller area than this specification because of the possibility of interfacing other electronic components, such as the transducer driver circuitry for other imaging schemes.

To determine the gain requirement for the amplifier, it is crucial to know the signal amplitude range of the CMUT. This was not readily available, however, information from commercial CMUT manufacturers indicates signal amplitudes in the 10-mV range, therefore 100 mV amplitude was selected as the output amplitude of the signal from the amplifier, which indicates a voltage gain of at least 20 dB at the center frequency. A summary of the target amplifier specifications is given in Table 3 - 1.

Table 3 - 1 Target Amplifier Specifications

Parameter	*Specification*
Supply Voltage	3.3 V
Center Frequency	7 MHz
Bandwidth	10 MHz
Noise Figure	< 3 dB
Gain	> 20 dB
Load Capacitance	10 pF
Max Power Consumption	5.9 mW
Area	0.11 mm x 13.2 mm

3.2 Topology Considerations

As aforementioned, the designed amplifier is expected to be replicated for each of the CMUT elements. Therefore, the chosen qualitative parameters for selecting the desired topology are noise, simplicity, and area. Although simple topologies are selected, it is important to ensure that the design is robust and meets the desired specifications. To address this, an analysis of single stage amplifiers topologies was carried out, with each amplifier topology designed to meet the specified requirements in Table 3 - 1. The investigated amplifier topologies are the common source amplifier and common gate amplifiers, as they form the building blocks for various complex amplifier topologies [1]–[11].

3.3 Common Source Amplifier

An important property of the Common Source Amplifier is its wideband operation which is characterized by the input/main transistor's transit frequency [3], [37], [42]. Also, intrinsically, the topology offers a high input impedance [37], which indicates that it does not load the preceding stage in the signal chain.

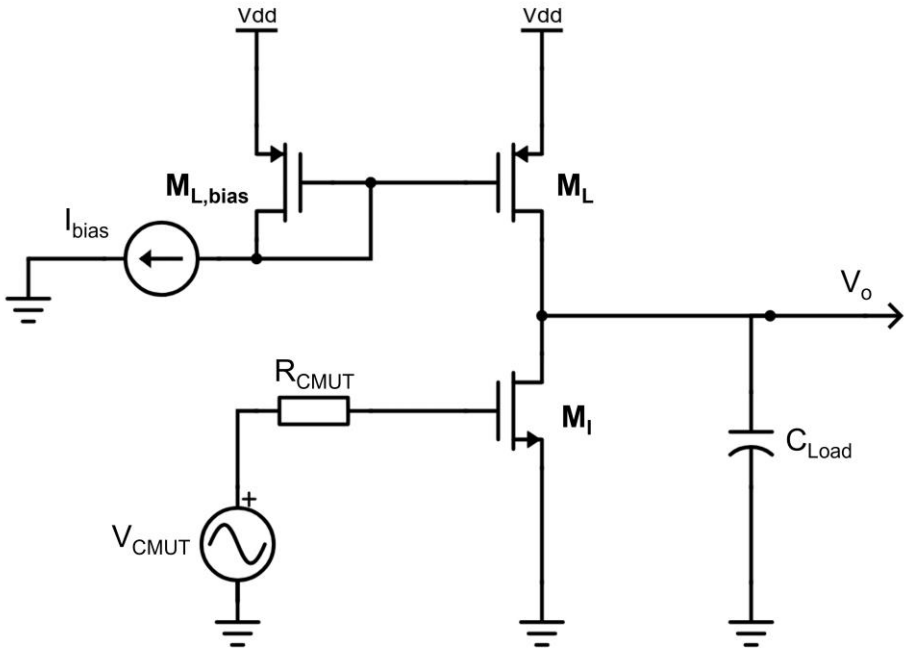

Figure 3 - 2 Common Source Amplifier with CMUT signal, Biasing and Capacitive Load [37], [43], [45].

The designed common source amplifier is shown in Figure 3 - 2. It is a common source amplifier having a current source load and consists of an input transistor – M_I, load transistor – M_L. The load transistor is biased in a current mirror configuration via the load bias transistor – $M_{L,bias}$ and the bias current reference – I_{bias}. The signal from the CMUT is represented by the AC voltage source – V_{CMUT}, having a resistance – R_{CMUT}.

3.3.1 Small Signal Frequency Response

The small signal high frequency model of the common source stage is depicted in Figure 3 - 3. The model shows the intrinsic capacitances of the input transistor, which include gate-source capacitance – $C_{gs,I}$, gate-bulk capacitance – $C_{gb,I}$, gate-drain capacitance – $C_{gd,I}$ and the drain-bulk capacitance - $C_{db,I}$, as well as a current source which is dependent on the input transistor's transconductance – $g_{m,I}$ and input small signal voltage – V_{CMUT} of the input transistor. Conductances $g_{ds,I}$ and $g_{ds,L}$ represent the output conductance of the input transistor – M_I and load transistor – M_L respectively.

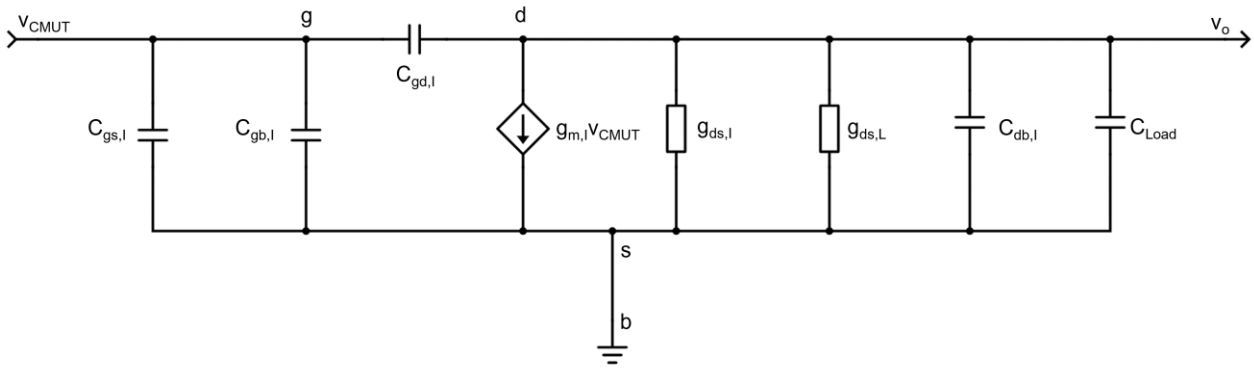

Figure 3 - 3 Common Source Amplifier Small Signal Model [13], [37], [43], [45].

To analyze the model, a simplifying assumption that can be made is that the load capacitance C_{Load} is large when compared to the intrinsic capacitances of the input stage, implying that it is the dominant pole in the model's frequency response. This makes the model a first order model, and further analysis would make decisions based on this assumption.

From the model, a Thevenin's equivalent of $g_{m,I}v_{CMUT}$ and $g_{ds,I} + g_{ds,L}$ in combination with the load capacitance C_{Load} is equivalent to a first order low-pass filter [44]. The corresponding corner frequency of the filter is expressed as

$$f_c = \frac{g_{ds,I} + g_{ds,L}}{2\pi C_{Load}} \tag{3.1}$$

The term $g_{ds,I} + g_{ds,L}$ indicates the output conductance of the amplifier, and it particularly sets the low frequency gain of the amplifier by scaling the $g_{m,I}$ (transconductance of the input MOSFET), which is expressed in Equation (3.2) [13], [37], [43], [45].

$$|A_{v0}| = \frac{g_{m,I}}{g_{ds,I} + g_{ds,L}} \tag{3.2}$$

Following this, the approximate frequency response of the model can be expressed as in Equation (3.3) [44].

$$A_v(j2\pi f) = \frac{A_{v0}}{1 + j\frac{f}{f_c}} \tag{3.3}$$

With consideration that the model has an approximate first order response, a simplifying perspective is to consider the 0 dB crossover frequency as the corner frequency of a first order response which has a gain of unity. Now, from the low frequency gain expression, it can be deduced that for unity gain,

$$g_{m,I} = g_{ds,I} + g_{ds,L} \tag{3.4}$$

Therefore, at unity gain, the corner frequency is given as,

$$f_{c,ug} = \frac{g_{m,I}}{2\pi C_{Load}} \tag{3.5}$$

Where, $f_{c,ug}$ is the unity gain frequency or gain bandwidth of the amplifier.

In this work, the bandwidth specification for the amplifier is 10 MHz, and at this frequency, the specified gain should be greater than 10 and should drive a $10\ pF$ capacitive load. This implies that,

$$f_{c,ug} \geq 100\ MHz \tag{3.6}$$

Therefore,

$$g_{m,I} = 2\pi f_{c,ug} C_{Load} = 2\pi \times 100\ MHz \times 10\ pF \tag{3.7}$$

$$g_{m,I} = 6.3\ mS \tag{3.8}$$

The transconductance in Equation (3.8) is a fixed design parameter which would be utilized in the upcoming sections for sizing the transistors. This is because the combination of the transconductance of the input transistor and the load capacitance sets the speed of the amplifier, characterizing by the unity gain frequency as mentioned in Section 2.4.1. Also, with a fixed transconductance, the output conductance or resistance can be used to set the low frequency gain of the amplifier.

3.3.2 Noise Considerations

In the common source stage, the flicker or low-frequency noise and thermal noise are important noise sources to be considered [36], [37], [44]. A “pseudo” equivalent noise model of the common source stage is shown in Figure 3 - 4.

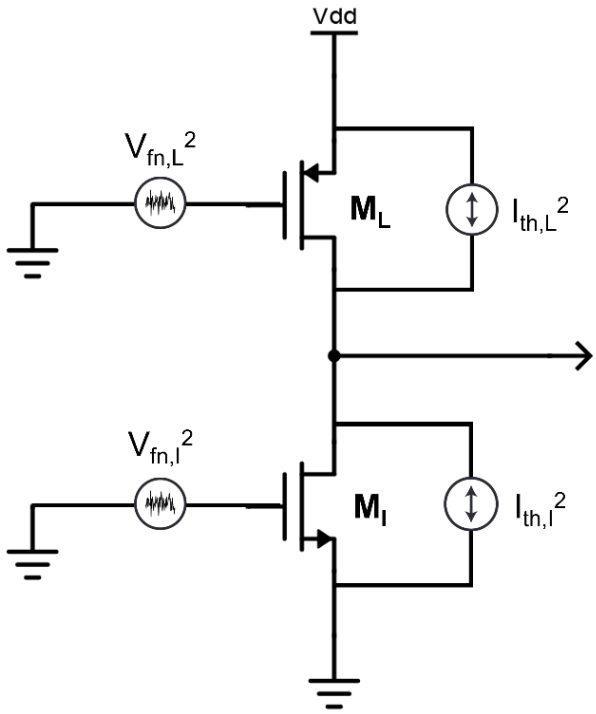

Figure 3 - 4 Common Source Amplifier with Noise Sources [36], [37], [44].

As discussed in Section 2.4.2, the flicker or low frequency noise density is modelled as voltage sources at the gate of both transistors, while the thermal noise density is modelled as current sources parallel to the drain and source of each transistor. Referring the flicker noise voltage sources to the output and noting that they are non-correlated noise sources, the flicker noise current in the amplifier is,

$$I_{fn}^2 = I_{fn,I}^2 + I_{fn,L}^2 \tag{3.9}$$

$$I_{fn}^2 = \frac{1}{f}\frac{g_{m,I}^2 K_N}{(WL)_I} + \frac{1}{f}\frac{g_{m,L}^2 K_P}{(WL)_L} \tag{3.10}$$

Therefore, the total flicker noise voltage density at the output is,

$$V_{fn}^2 = \frac{I_{fn}^2}{g_o^2} = \frac{1}{f}\frac{1}{C_{ox}}\left(\frac{g_{m,I}^2 K_N}{(WL)_I} + \frac{g_{m,L}^2 K_P}{(WL)_L}\right)\frac{1}{\left(g_{ds,I} + g_{ds,L}\right)^2} \tag{3.11}$$

Referring the voltage noise density to the input,

$$V_{fn,in}^2 = \frac{V_{fn}^2}{A_v^2} = \frac{1}{f}\frac{1}{C_{ox}}\left(\frac{K_N}{(WL)_I} + \frac{g_{m,L}^2 K_P}{g_{m,I}^2 (WL)_L}\right) \tag{3.12}$$

Also, the thermal noise current sources across the drain and source of both transistors are non-correlated sources and at the output, the combined thermal noise from both transistors is,

$$I_{th}^2 = I_{th,I}^2 + I_{th,L}^2 = 4kT\gamma_I g_{m,I} + 4kT\gamma_L g_{m,L} \tag{3.13}$$

From this expression, the total output thermal noise voltage at the output is,

$$V_{th}^2 = \frac{I_{th}^2}{g_o^2} = \frac{4kT\gamma_I g_{m,I} + 4kT\gamma_L g_{m,L}}{\left(g_{ds,I} + g_{ds,L}\right)^2} \tag{3.14}$$

Referring the thermal noise voltage density to the input,

$$V_{th,in}^2 = \frac{V_{th}^2}{A_v^2} = 4kT\left(\frac{\gamma_I}{g_{m,I}} + \frac{\gamma_L g_{m,L}}{g_{m,I}^2}\right) \tag{3.15}$$

Now, since the thermal and flicker noise are non-correlated noise sources, the total input-referred noise of the amplifier is,

$$V_{n,in}^2 = V_{fn,in}^2 + V_{th,in}^2 \tag{3.16}$$

$$V_{n,in}^2 = \frac{1}{f}\frac{1}{C_{ox}}\left(\frac{K_N}{(WL)_I} + \frac{g_{m,L}^2 K_P}{g_{m,I}^2 (WL)_L}\right) + 4kT\left(\frac{\gamma_I}{g_{m,I}} + \frac{\gamma_L g_{m,L}}{g_{m,I}^2}\right) \quad (3.17)$$

From the expression, maximizing $g_{m,I}$ and minimizing $g_{m,L}$ improves the noise performance of the amplifier. This is advantageous, as M_L in the amplifier is a current source load and its transconductance is not instrumental in amplifying signals as there are no small signal variations at its gate. Also, the flicker noise component in the expression implies that having relatively large transistors reduces the flicker noise. However, in this work, the amplifier is expected to operate at a 7 MHz centre frequency, and the inverse proportionality of the flicker noise with frequency, implies that the proportion of the flicker noise component in the total noise in the amplifier may be negligible.

Furthermore, to include the signal source (the CMUT) in the noise formulations, a consideration of the noise figure is necessary. Since the reactive components of CMUT impedance does not contribute to its thermal noise, we consider the CMUT as a signal source having a source resistance connected to the amplifier as shown in Figure 3 - 5.

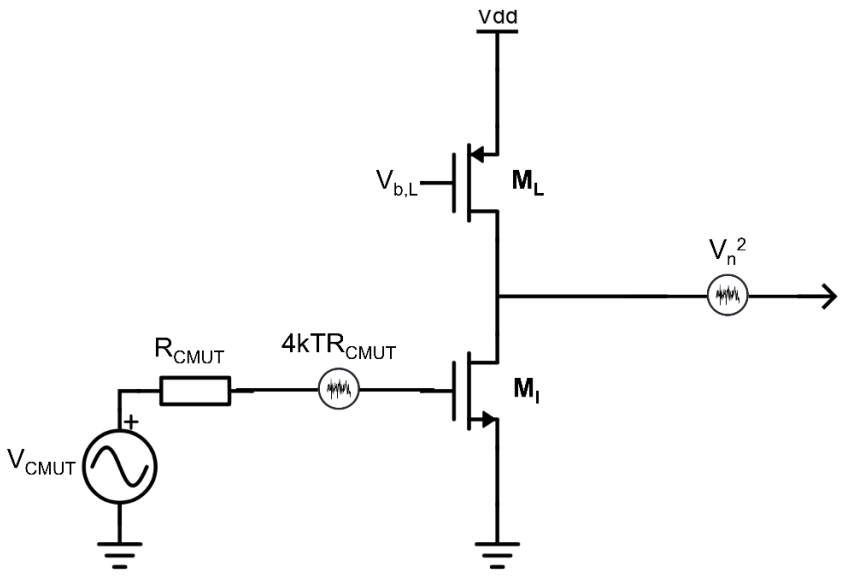

Figure 3 - 5 Common Source Amplifier setup for Noise Figure Analysis [42].

In Figure 3 - 5, the amplifier is considered noiseless, but connected at the output is its total noise voltage density. Also, it is assumed that the gate of the input transistor has an infinite impedance and would not attenuate the signal at the input to the amplifier.

Therefore, the signal power and noise power at the input can be expressed as

$$S_{in} = V_{CMUT}^2 \tag{3.18}$$

$$N_{in} = 4kTR_{CMUT} \tag{3.19}$$

At the output, signal power and noise power expressions are,

$$S_o = A_v^2 V_{CMUT}^2 \tag{3.20}$$

$$N_o = 4kTR_{CMUT}A_v^2 + V_n^2 \tag{3.21}$$

Following this, the noise factor expression for the system can be expressed as,

$$F = {S_{in}/N_{in}}\Big/{S_o/N_o} \tag{3.22}$$

Therefore,

$$F = 1 + \frac{V_{n,out}^2}{4kTR_{CMUT}A_v^2} \tag{3.23}$$

$$NF = 10\log(F) \tag{3.24}$$

3.3.3 Sizing the Common Source Amplifier

For a specified load capacitance, gain and bandwidth, the frequency response of the common source stage can be characterized by the transconductance (g_m) and intrinsic gain – g_m/g_{ds}, where the relationship between g_m and the gain-bandwidth yields the transconductance, and the intrinsic gain describes the low frequency gain of the amplifier. This makes it possible to size the transistors in the amplifier using the transconductance efficiency – g_m/I_D [13].

An important objective for this design is to optimize for low noise, therefore, the initial decision of the g_m/I_D for each transistor in the stage was made by considering input referred noise expression

for the common source stage, which indicates that minimizing the transconductance of the current source load minimizes the noise in the stage. The transconductance in Equation (3.8) is selected for the input transistor with varied considerations for its g_m/I_D from strong inversion to moderate inversion, with a selected g_m/I_D of 10 S/A for the load transistor, which implies sizing in moderate inversion.

The sizing procedure involves first selecting a g_m/I_D for the input transistor, the first case being $(g_m/I_D)_I = 14\ S/A$, then the drain current is calculated as,

$$I_{D,I} = \frac{g_{m,I}}{(g_m/I_D)_I} = \frac{6.3\ mS}{14\ S/A} = 450\ \mu A \tag{3.25}$$

Afterwards, the extracted g_m/g_{ds} against g_m/I_D curves shown in Figure 3 - 6 for the NMOS transistor were used to estimate the channel length. The specified low frequency gain is greater than 30, therefore from the curves, a length is selected which satisfies that requirement for the specified g_m/I_D. In Figure 3 - 6, all curves satisfy the requirement, therefore the minimum length is selected, implying $L_I = 0.4\ \mu m$.

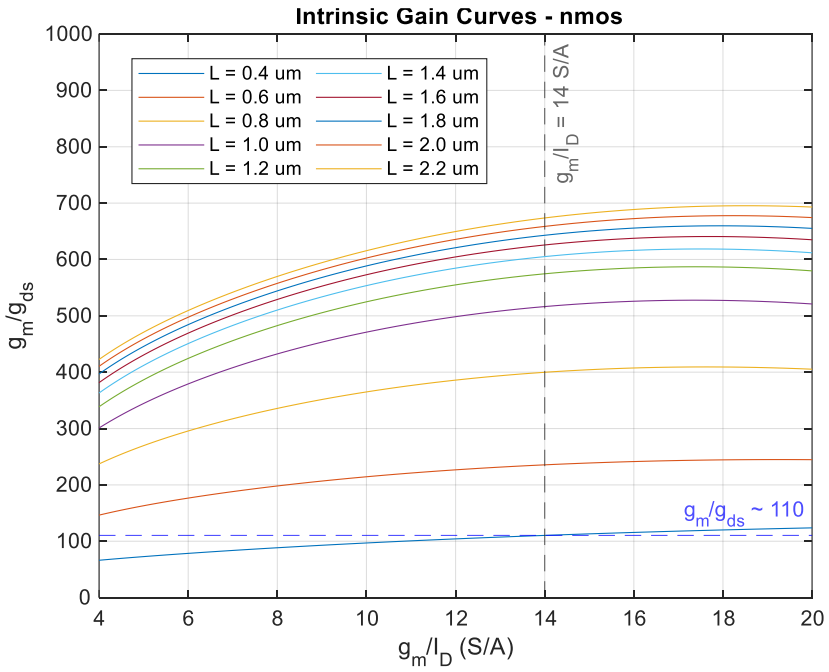

Figure 3 - 6 Extracted Intrinsic gain (g_m/g_{ds}) curves for the n-channel MOSFET.

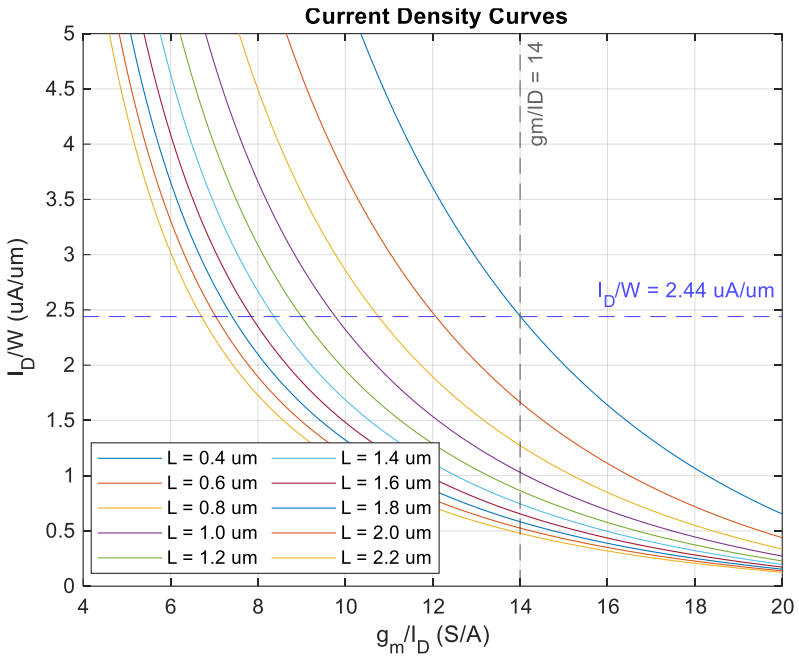

Figure 3 - 7 Current Density (I_D/W) curves for the n-channel MOSFET.

Next, the width of the input transistor is sized by utilizing the NMOS current density (I_D/W) against g_m/I_D curves shown in Figure 3 - 7. The procedure involves retrieving a specific current density for the selected length in the preceding step, which is $0.4\ \mu m$ and the input transistor's g_m/I_D. In the current case, the lookup is the $L = 0.4\ \mu m$ curve and $g_m/I_D = 14\ S/A$, which yields a current density of approximately $2.44\ \mu A/\mu m$, from which the transistor's width can be calculated as,

$$W_I = \frac{I_{D,I}}{(I_D/W)_I} = \frac{450\ \mu A}{2.44\ \mu A/\mu m} = 184\ \mu m \tag{3.26}$$

Continuing, the current source load is sized by first considering the desired low frequency gain and utilizing it to determine the value of the output conductance of the amplifier as expressed in Equation (3.27).

$$|A_{v0}| = \frac{g_{m,I}}{g_{ds,I} + g_{ds,L}} \geq 30 \tag{3.27}$$

For $g_{m,I} = 6.3\ mS$,

$$g_{ds,I} + g_{ds,L} \leq 210\ \mu S \tag{3.28}$$

An assumption can be made that $g_{ds,I} = g_{ds,L}$, which implies that $g_{ds,I}$ and $g_{ds,L}$ should be less than $105\ \mu S$, which is a rough estimate for output conductance of the current source load. Next, in this case, the selected g_m/I_D for the current source load is 10 S/A and $I_{D,L} = I_{D,I}$ which implies that,

$$g_{m,L} = (g_m/I_D)_I \times I_{D,L} = 10\ S/A\ \times 450\ \mu A \tag{3.29}$$

$$g_{m,L} = 4500\ \mu S \tag{3.30}$$

From this, the intrinsic gain of the current source load can be estimated to be,

$$(g_m/g_{ds})_L \geq \frac{4500\ \mu S}{105\ \mu S} = 42.86 \tag{3.31}$$

Now, the curves of g_m/g_{ds} against g_m/I_D shown Figure 3 - 8 is looked up for a length curve that satisfies $g_m/g_{ds} \geq 42.86$ at $g_m/I_D = 10\ S/A$. For the $L = 0.4\ \mu m$ curve, a g_m/I_D of 10 S/A corresponds to approximately a g_m/g_{ds} of 46, which satisfies the condition, therefore, for M_L, the length $L_L = 0.4\ \mu m$ is selected.

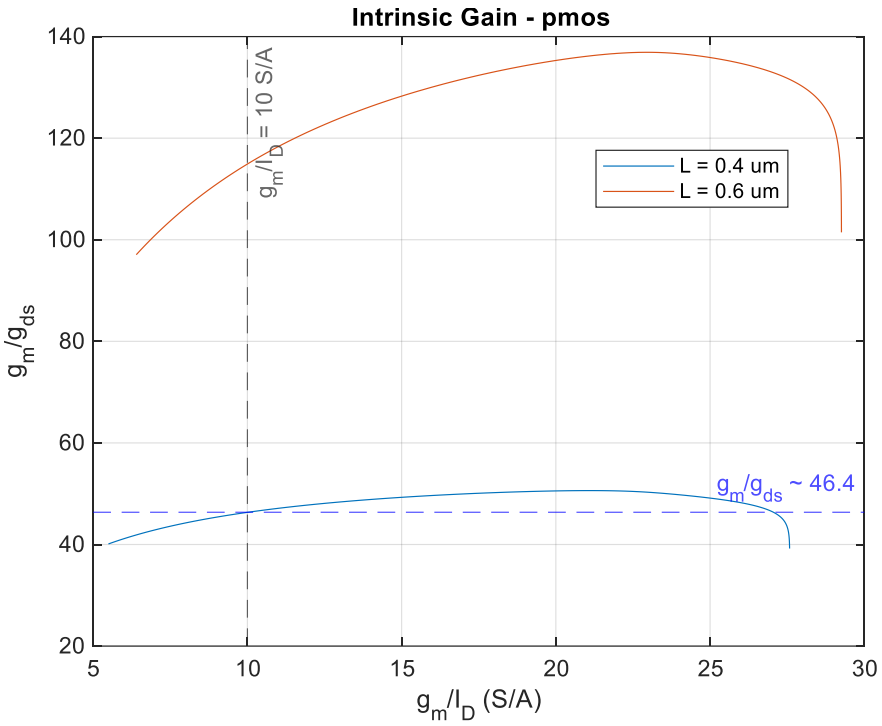

Figure 3 - 8 Intrinsic Gain (g_m/g_{ds}) curves for the p-channel MOSFET.

For the transistor's width, utilizing the current density curves for the PMOS shown in Figure 3 - 9, a lookup for $g_m/I_D = 10\,S/A$ on the $L = 0.4\,\mu m$ curve yields $I_D/W = 2.1\,\mu A/\mu m$ from which the width is calculated as,

$$W_L = \frac{I_{D,L}}{(I_D/W)_L} = \frac{450\,\mu A}{2.1\,\mu A/\mu m} = 214\,\mu m \tag{3.32}$$

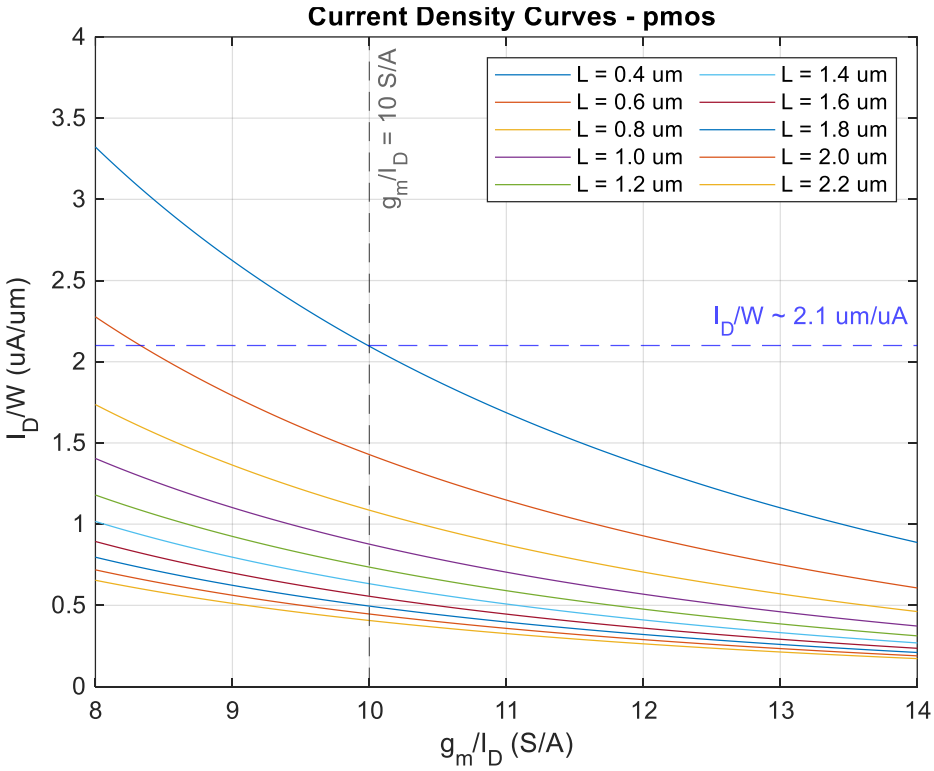

Figure 3 - 9 Current Density (I_D/W) curves for the p-channel MOSFET.

Furthermore, a lookup of the respective gate-to-source voltage for each transistor can be carried out by utilizing the V_{gs} against g_m/I_D curves for the respective transistor length and type.

For the range of $(g_m/I_D)_I$ values for fixed $(g_m/I_D)_L = 10\,S/A$, the described sizing procedure was done for each design point, and a summary of the respective transistor sizes is presented in Table 3 - 2.

Table 3 - 2 Transistor Sizes for varying $(g_m/I_D)_I$ at $(g_m/I_D)_L = 10\ S/A$

$(g_m/I_D)_I$	$L_I\ (\mu m)$	$W_I\ (\mu m)$	$L_L\ (\mu m)$	$W_L\ (\mu m)$	$I_D\ (\mu A)$
14	0.4	184	0.4	214	450
16	0.4	242	0.4	188	394
18	0.4	330	0.4	167	350
20	0.4	485	0.4	150	315
22	0.4	818	0.4	136	286

The variations presented in Table 3 - 2 also implies varied drain current, hence varying power consumption. The following sizes were simulated and transistor size with the lowest noise figure was at $(g_m/I_D)_I = 22$. To further improve the noise figure, $(g_m/I_D)_L$ was varied as well as summarized in Table 3 - 3.

Table 3 - 3 Transistor Sizes for varying $(g_m/I_D)_L$ at $(g_m/I_D)_I = 22\ S/A$

$(g_m/I_D)_L$	$L_L\ (\mu m)$	$W_L\ (\mu m)$
10	0.4	136
9	0.4	109
8	0.4	86.1
7	0.4	66.8
6	0.4	50.4

3.3.4 Resistive Feedback

To ensure that the preferred gain for the amplifier is set and robust enough to withstand changes due to process, voltage or temperature variations, negative feedback was introduced to the common source amplifier. The resistive feedback common source amplifier is shown in Figure 3 - 10.

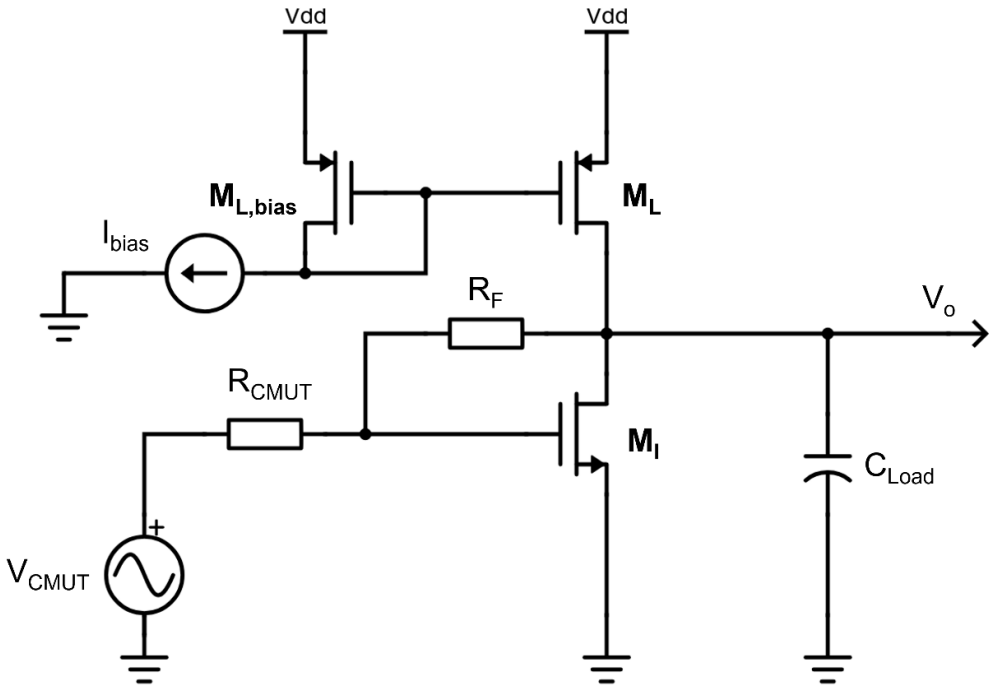

Figure 3 - 10 Resistive Feedback Common Source Amplifier [6], [42].

3.3.4.1 Small Signal Analysis

The low frequency small signal model of the amplifier is shown in Figure 3 - 11. It consists of the low frequency components of the small signal model of open loop amplifier (shown in Figure 3 - 3) and the feedback resistor – R_F, which is connected between the drain and gate of the input transistor – M_I.

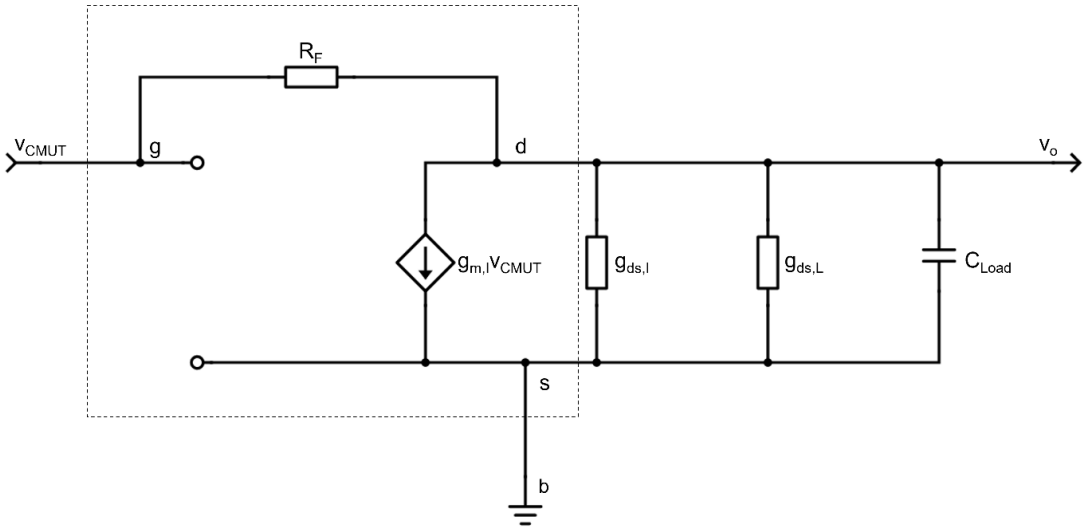

Figure 3 - 11 Resistive Feedback Small Signal Model [37], [42].

To determine the closed loop gain of the amplifier, applying KCL at the drain node – d, yields

$$\frac{v_{in} - v_o}{R_F} = g_{m,I} v_{in} + \left(g_{ds,I} + g_{ds,L}\right) v_o \tag{3.33}$$

which yields,

$$\frac{v_o}{v_{in}} = \frac{1 - g_{m,I} R_F}{1 + \left(g_{ds,I} + g_{ds,L}\right) R_F} \tag{3.34}$$

For a reasonably high gain, an assumption can be made that $\left(g_{ds,I} + g_{ds,L}\right)$ is very small compared to $g_{m,I}$ and $1/R_F$, therefore, the small signal gain of the amplifier can be expressed as

$$A_v \approx \ 1 - g_{m,I} R_F \tag{3.35}$$

Next, an evaluation of the gain experienced by the signal is necessary, as the input impedance can no longer be assumed to be infinite as in the open-loop case. For the input resistance, an observation of the input transistor – M_I and feedback resistance – R_F connection highlighted in the dashed box in Figure 3 - 11 indicates a diode-connected transistor topology. Therefore, the low frequency impedance seen at the input can be expressed as

$$Z_{in} = \frac{1}{g_{m,I} + g_{ds,I} + g_{ds,L}} \approx \frac{1}{g_{m,I}} \tag{3.36}$$

Furthermore, it can be observed that the source resistance – R_CMUT and the input impedance form a voltage divider at the input of the amplifier. Therefore, the amplifier's gain is attenuated and can be expressed as

$$A_{v,s} = \frac{1 - g_{m,I} R_F}{1 + \left(g_{ds,I} + g_{ds,L}\right) R_F} \left(\frac{Z_{in}}{R_{CMUT} + Z_{in}}\right) \tag{3.37}$$

which yields,

$$A_{v,s} = \frac{1 - g_{m,I} R_F}{\left(1 + \left(g_{ds,I} + g_{ds,L}\right) R_F\right)\left(1 + \left(g_{m,I} + g_{ds,I} + g_{ds,L}\right) R_{CMUT}\right)} \tag{3.38}$$

For $\left(g_{ds,I} + g_{ds,L}\right) \ll g_{m,I}$, the signal gain can be approximated as

$$A_{v,s} \approx \frac{1 - g_{m,I}R_F}{1 + g_{m,I}R_{CMUT}} \approx \frac{-R_F}{R_{CMUT}} \tag{3.39}$$

$$A_{v,s} \approx \frac{-R_F}{R_{CMUT}} \tag{3.40}$$

The expression in Equation (3.40) implies that the closed loop gain is dependent on ratio and is therefore expected to be controlled and/or constant as the effect of process variations may be cancelled.

3.3.4.2 Noise Considerations

As analyzed for the open loop case, the noise formulations for the resistive feedback common source amplifier would be derived. Consider the noise model in Figure 3 - 12, with the thermal noise in the transistors modelled as noise current sources, while noise voltage sources model the flicker noise. Also, a noise voltage source models the thermal noise of the feedback resistor.

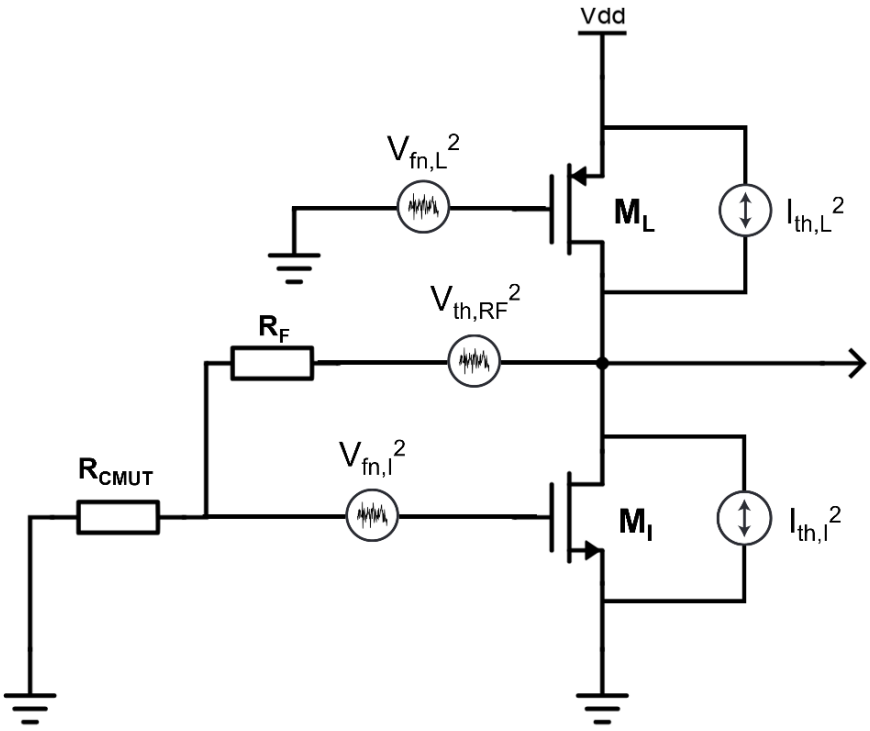

Figure 3 - 12 Resistive Feedback Noise Model [42].

For the thermal noise in the amplifier, a consideration for the thermal noise at the output due to the thermal noise of the feedback resistor is given as,

$$V_{th,CMUT}^2 = \ 4kTR_{CMUT} \tag{3.41}$$

Furthermore, for the thermal noise in the transistors, a consideration that the sum of the thermal noise currents (non-correlated) would flow in the amplifiers output resistance implies that the thermal noise in the amplifier produced by the transistors can be expressed as

$$V_{th,M}^2 = \ \left(I_{th,I}^2 + I_{th,L}^2\right)/G_o^2 \tag{3.42}$$

To determine the output conductance – G_o, consider the modified small signal model for noise analysis shown in Figure 3 - 13.

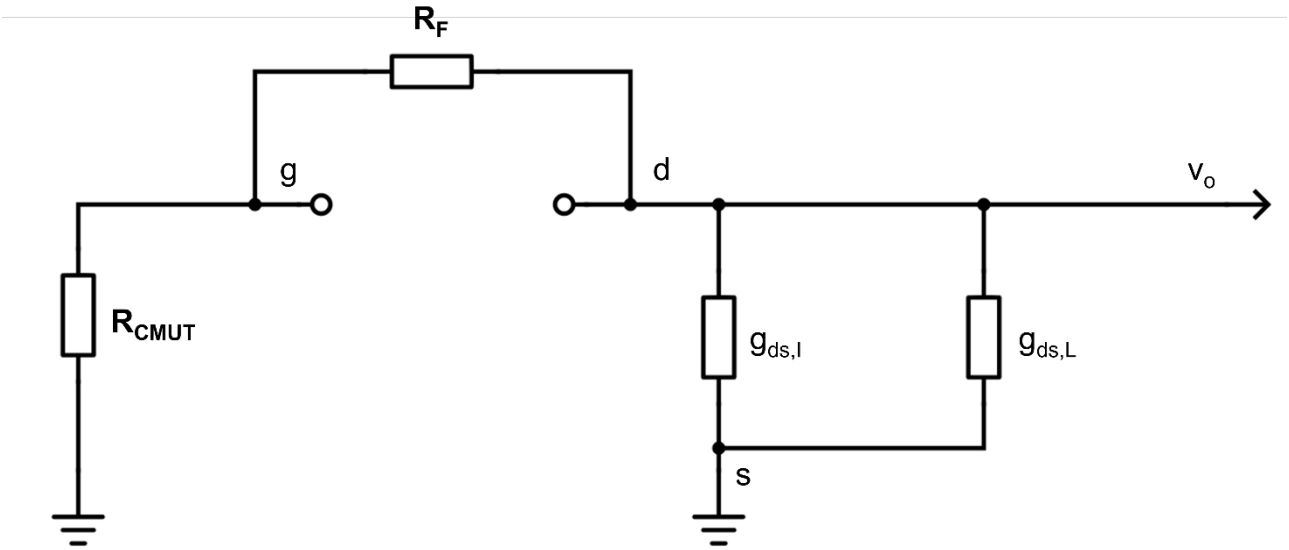

Figure 3 - 13 Small Signal Output Conductance

The signal source is set to zero and grounded, therefore the dependent current source that utilizes the transconductance and input voltage into the amplifier is set to zero (open-circuited). Therefore, the output conductance can be expressed as

$$G_o = \frac{1}{R_F + R_{CMUT}} + g_{ds,I} + g_{ds,L} \tag{3.43}$$

Assuming that the sum of the intrinsic output conductance of both transistors are very small (due to expected high gain at low frequencies) compared to the other term in the expression. The output conductance can be approximated as Equation (3.44).

$$G_o \approx \frac{1}{R_F + R_{CMUT}} \tag{3.44}$$

Following this, the output thermal noise due to the transistors can be expressed as,

$$V_{th,M}^2 = 4kT\left(\gamma_I g_{m,I} + \gamma_L g_{m,L}\right)(R_F + R_{CMUT})^2 \tag{3.45}$$

Therefore, the total output thermal noise in the amplifier can expressed as

$$V_{th,o}^2 = 4kT\left[R_F + \left(\gamma_I g_{m,I} + \gamma_L g_{m,L}\right)(R_F + R_{CMUT})^2\right] \tag{3.46}$$

Referring the output thermal noise to the input, yields

$$V_{th,in}^2 = \frac{4kT\left[R_F + \left(\gamma_I g_{m,I} + \gamma_L g_{m,L}\right)(R_F + R_{CMUT})^2\right]}{\left(1 - g_{m,I}R_F\right)^2} \tag{3.47}$$

Similar consideration can be made for the flicker noise in the amplifier, implying that referring the flicker noise voltages at the gate of each transistor to the drain as noise current sources, it can be expected that both noise currents flow through the output resistance of the amplifier. Therefore, the output flicker noise voltage in the amplifier can be expressed as

$$V_{fn,M}^2 = \left(I_{fn,I}^2 + I_{fn,L}^2\right)R_o^2 \tag{3.48}$$

$$V_{fn,M}^2 = \frac{1}{f}\frac{1}{C_{ox}}\left(\frac{g_{m,I}^2 K_N}{(WL)_I} + \frac{g_{m,L}^2 K_P}{(WL)_L}\right)(R_F + R_{CMUT})^2 \tag{3.49}$$

Referring the output flicker noise to the input, yields Equation (3.50).

$$V_{fn,M}^2 = \frac{1}{f}\frac{1}{C_{ox}}\left(\frac{g_{m,I}^2 K_N}{(WL)_I} + \frac{g_{m,L}^2 K_P}{(WL)_L}\right)\left(\frac{R_F + R_{CMUT}}{1 - g_{m,I}R_F}\right)^2 \tag{3.50}$$

The total input-referred noise for the amplifier is then a sum of the expressions in Equation (3.47) and Equation (3.50).

Furthermore, as is the case for the open-loop amplifier, a consideration for the noise figure of the system is analyzed. To begin, the amplifier is set up as shown in Figure 3 - 14, which includes the CMUT and a representation of its thermal noise as a voltage source, and the total noise in the amplifier referred to the output and modelled as a noise voltage source.

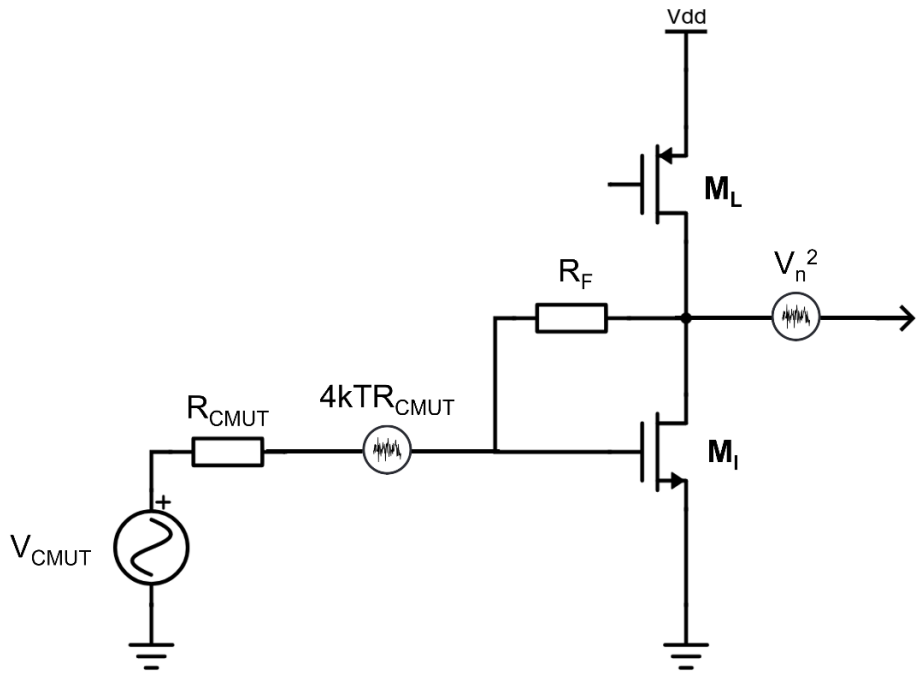

Figure 3 - 14 Resistive Feedback - Noise Figure Analysis [6], [37], [42].

In the noise figure analysis of the common source amplifier in Section 3.3.2, an assumption of an infinite input impedance for the amplifier was made, however, this is not the case for this feedback amplifier. Therefore, the signal from the CMUT is attenuated and the signal into the amplifier expressed as

$$V_{in} = \frac{Z_{in}V_{CMUT}}{R_{CMUT} + Z_{in}} = \frac{V_{CMUT}}{1 + g_{m,I}R_{CMUT}} \qquad (3.51)$$

Therefore, the signal and noise power at the input can be expressed as Equation (3.52) and Equation (3.53) respectively.

$$S_i = \left(\frac{V_{CMUT}}{1 + g_{m,I}R_{CMUT}}\right)^2 \tag{3.52}$$

$$N_i = \frac{4kTR_{CMUT}}{\left(1 + g_{m,I}R_{CMUT}\right)^2} \tag{3.53}$$

Subsequently, the output signal and noise power are given by Equation (3.55) and Equation (3.56) respectively.

$$S_o = A_v^2\, S_i = \left(1 - g_{m,I}R_F\right)^2 \left(\frac{V_{CMUT}}{1 + g_{m,I}R_{CMUT}}\right)^2 \tag{3.54}$$

$$S_o = \left\{\frac{\left(1 - g_{m,I}R_F\right)V_{CMUT}}{1 + g_{m,I}R_{CMUT}}\right\}^2 \tag{3.55}$$

$$N_o = \frac{4kTR_{CMUT}\left(1 - g_{m,I}R_F\right)^2}{\left(1 + g_{m,I}R_{CMUT}\right)^2} + V_n^2 \tag{3.56}$$

Therefore, the noise factor can be expressed as

$$F = \frac{S_i/N_i}{S_o/N_o} = 1 + \frac{V_n^2\left(1 + g_{m,I}R_{CMUT}\right)}{4kTR_{CMUT}\left(1 - g_{m,I}R_F\right)^2} \tag{3.57}$$

An observation of the noise factor expression indicates that increasing the feedback resistance results improves the noise performance of the system.

3.3.4.3 Sizing the Resistive Feedback Amplifier

The determination of the dimensions of the transistors was done using the same procedure described for the common source amplifier in Section 3.3.3. However, the targeted open loop gain in this case is higher, to ensure a higher loop gain, which improves the robustness of the amplifier. Furthermore, the selected g_m/I_D value for the input transistor – M_I is 22 S/A, and that of the load transistor – M_L, 6 S/A. These values correspond to the last design point for the open-loop amplifier. In the selection

of the feedback resistance value, a parametrization operation was performed on the amplifier to arrive at the target gain of approximately 20 dB at the 7 MHz, which is the center frequency. Table 3 - 4 presents a summary of the sizing parameters for the components of the feedback amplifier.

Table 3 - 4 Resistive Feedback Amplifier Sizing Summary

Parameter	*Value*
W_I	$818\ \mu m$
L_I	$0.4\ \mu m$
W_L	$71.5\ \mu m$
L_L	$0.6\ \mu m$
R_F	$4\ k\Omega$

3.4 Common Gate Amplifier

An important property of the common gate amplifier is its high output impedance, which ensures that it does not load the input of the next stage in the signal chain [37], [43]–[45]. Also, it has a wideband operation, and can be utilized as a current buffer or a non-inverting voltage amplifier. Furthermore, it has a low input impedance as the input is sensed at the source of the transistor, which makes it useful as the first stage in the signal chain for some applications, as it can be used to match resistance of the input device before the main stage in the signal chain [42], [45].

The designed common gate amplifier is shown in Figure 3 - 15. The input to the amplifier is at the gate of input transistor – M_I, which is current source biased via transistor – M_B and loaded with current source transistor – M_L. Transistors M_I, M_L and M_B are current mirror biased via transistors $M_{I,bias}$, $M_{L,bias}$ and $M_{B,bias}$ respectively from the reference current sources I_{bias1} and I_{bias2}. Also, capacitors $C_{I,bias}$, $C_{L,bias}$ and $C_{B,bias}$ shunts the noise generated in the biasing transistors $M_{I,bias}$, $M_{L,bias}$ and $M_{B,bias}$ respectively to ground. Furthermore, the signal from the CMUT represented by the voltage source V_{CMUT}, having a resistance R_{CMUT} is ac coupled via the coupling capacitor – C_{in}.

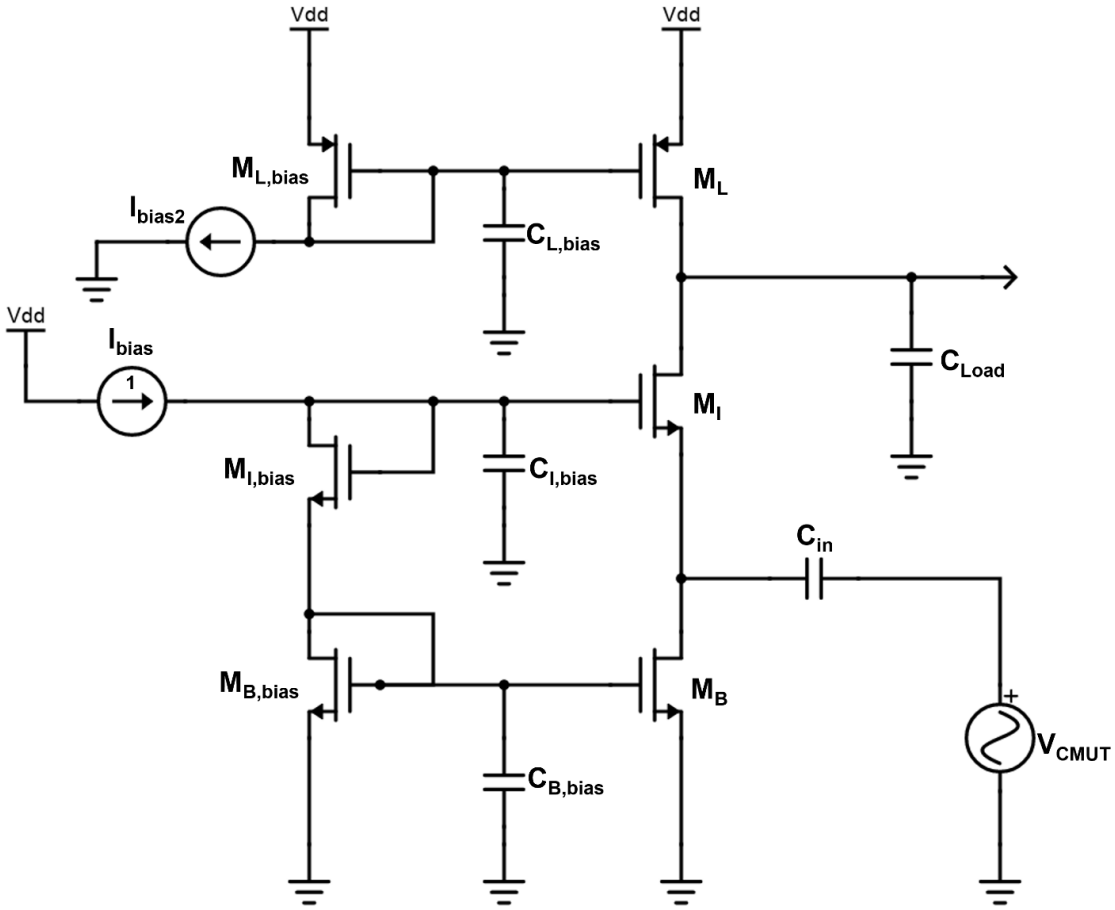

Figure 3 - 15 Designed Common Gate Amplifier [37], [42]–[45].

3.4.1 Small Signal Frequency Response

The small signal model of the common gate amplifier in Figure 3 - 15 is shown in Figure 3 - 16. The nodes labelled s, d and g represent the source, drain and gate of the input transistor - M_I respectively. The signal from the CMUT – v_{CMUT} is connected to the source node – s. Also, since there are no small signal variations at the gate of transistor M_B, the conductance seen from the node s to ground is its output conductance – $g_{ds,B}$. The gate of the input transistor – M_I is also connected to ground due to the absence of small signal variations at its gate. The dependent current sources $g_{m,I}v_{CMUT}$ and $g_{mb,i}v_{CMUT}$ represent part of the current generated in the drain of the input transistor – M_I due to its transconductance and body effect respectively. Conductances $g_{ds,I}$ and $g_{ds,L}$ are the output conductance of the input transistor – M_I and the current source load transistor – M_L respectively.

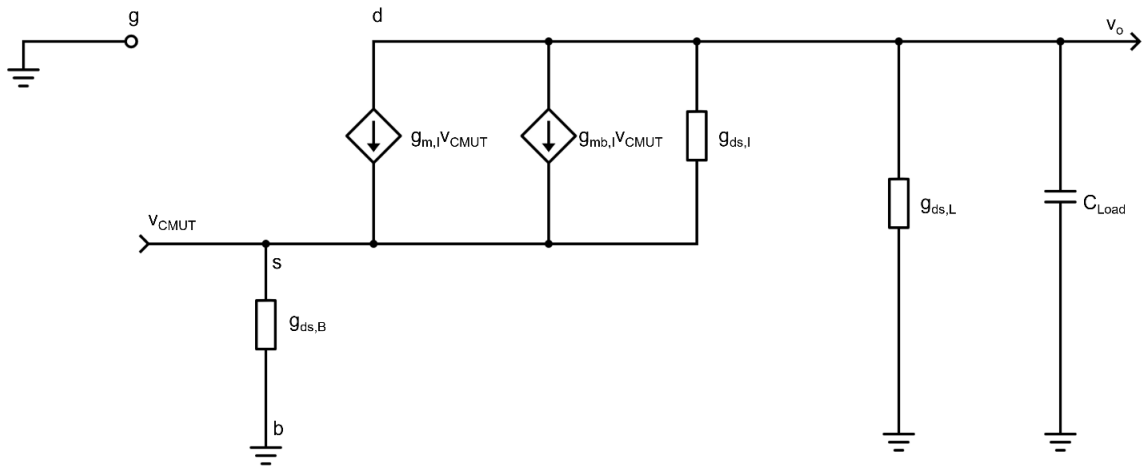

Figure 3 - 16 Common Gate Amplifier Small Signal Model [37], [42]–[45].

From the small signal model in Figure 3 - 16, the low frequency gain can be deduced by applying KCL at node v_o, which yields,

$$i_o = -i_d \tag{3.58}$$

With the analysis for i_o and i_d resulting in,

$$i_o = g_{ds,L} v_o \tag{3.59}$$

$$i_d = \left(g_{m,I} + g_{mb,I} + g_{ds,I}\right) v_{in} + g_{ds,I} v_o \tag{3.60}$$

This implies that,

$$-g_{ds,L} v_o = \left(g_{m,I} + g_{mb,I} + g_{ds,I}\right) v_{in} + g_{ds,I} v_o \tag{3.61}$$

Therefore,

$$A_{v0} = \frac{v_o}{v_{in}} = \frac{g_{m,I} + g_{mb,I} + g_{ds,I}}{g_{ds,I} + g_{ds,L}} \tag{3.62}$$

If the body effect is neglected, and the intended design is for a high gain, then the low frequency gain can be approximated as,

$$A_{v0} \approx \frac{g_{m,L}}{g_{ds,I} + g_{ds,L}} \tag{3.63}$$

This implies that for a fixed transconductance of the input transistor, the output conductance of the load and bias transistors sets the low frequency gain of the amplifier.

Furthermore, the Norton's equivalent conductance at the output, which can be determined by evaluating the short circuit current and open circuit voltage is,

$$g_o = \frac{g_{m,I}(g_{ds,I} + g_{ds,L})}{g_{m,I} + g_{ds,L}} \tag{3.64}$$

With the same considerations as is the case for the low frequency gain, the output conductance can be approximated as,

$$g_o \approx g_{ds,I} + g_{ds,L} \tag{3.65}$$

The output conductance and the load capacitance constitute a low pass filter. The corner frequency of the filter is,

$$f_c = \frac{g_o}{2\pi C_{Load}} \tag{3.66}$$

Furthermore, as previously mentioned, the unity gain frequency of the amplifier for a single pole approximation can be considered as the corner frequency when the gain is unity, implying that,

$$g_o = g_{m1} \tag{3.67}$$

Therefore, the unity gain frequency can be defined as

$$f_{c,ug} = \frac{g_{m,I}}{2\pi C_{Load}} \tag{3.68}$$

Considering the target specification for the amplifier, which requires a GBW = 100 MHz and is expected to drive a capacitive load of 10 pF, the transconductance of the input transistor, $g_{m,I}$ is calculated as,

$$g_{m,I} = 2\pi f_{c,ug} C_L = 2\pi \times 100\ MHz \times 10\ pF = 6.3\ mS \tag{3.69}$$

Equation (3.69) defines the transconductance of the input transistor which would be considered a fixed design parameter and would be utilized in the upcoming sections for sizing the transistors.

3.4.2 Noise Considerations

Consider the noise model of the common gate stage in Figure 3 - 17, the thermal noise in each transistor is modelled as noise current sources across the transistor's channel.

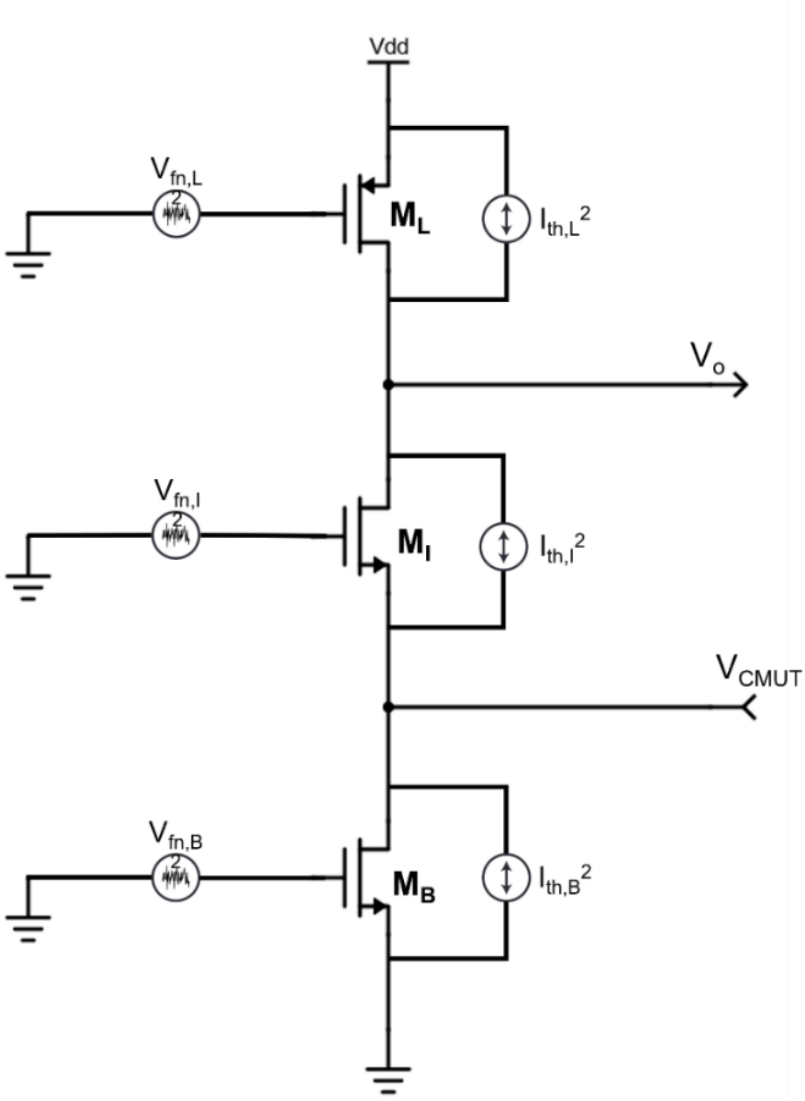

Figure 3 - 17 Common Gate Noise Sources [36], [37], [44].

The analysis can be started by short-circuiting the input of the amplifier to ground to determine the thermal voltage noise density at the output, V_{th}^2. As a result, the current source bias transistor M_B is bypassed, and the transistors M_I and M_L can be considered as regular common source stage. The short-circuit thermal noise current density of the amplifier is therefore expressed as,

$$I_{th,sc}^2 = 4kT\gamma_I g_{m,I} + 4kT\gamma_L g_{m,L} \tag{3.70}$$

Therefore, the output noise voltage density can be expressed as,

$$V_{th}^2 = \frac{I_{th,sc}^2}{g_o^2} = \frac{4kT\gamma_I g_{m,I} + 4kT\gamma_L g_{m,L}}{(g_{ds,I} + g_{ds,L})^2} \tag{3.71}$$

Referring this to the input,

$$V_{th,in}^2 = \frac{V_{th}^2}{A_v^2} \tag{3.72}$$

$$V_{th,in}^2 = 4kT\left(\frac{\gamma_I}{g_{m,I}} + \frac{\gamma_L g_{m,L}}{g_{m,I}^2}\right) \tag{3.73}$$

Next, the input-referred thermal noise current of the amplifier is determined by leaving the input opened. In this case, from the output node, the source of transistor M_I can be considered as been degenerated by transistor M_B. With this consideration, the voltage gain is small when compared to the gain of the amplifier, which also ensures that the noise modelled at the gate of M_I referred to its drain-to-source (channel) becomes negligible. Therefore, total thermal noise current at the output is a result of adding the non-correlated current noise sources of M_B and M_L yielding,

$$I_{th}^2 = I_{th,B}^2 + I_{th,L}^2 = 4kT\gamma_B g_{m,B} + 4kT\gamma_L g_{m,L} \tag{3.74}$$

Since the input is open, the input-referred thermal noise current approximately equals the output noise current. Therefore,

$$I_{th,in}^2 = I_{th}^2 = 4kT(\gamma_B g_{m,B} + \gamma_L g_{m,L}) \tag{3.75}$$

Considering Figure 3 - 17, the flicker noise density in the transistors is modelled as noise voltage sources connected at the gate of each amplifier. Applying a short-circuit to the amplifier's input, the

output flicker noise voltage density at the output would result from the flicker noise of transistor's M1 and M3, since transistor M2 is bypassed by the short-circuit. Therefore,

$$V_{fn}^2 = \frac{1}{f}\frac{1}{C_{ox}}\left(\frac{g_{m,I}^2 K_N}{(WL)_I} + \frac{g_{m,L3}^2 K_P}{(WL)_L}\right)\frac{1}{\left(g_{ds,I} + g_{ds,L}\right)^2} \tag{3.76}$$

Referring to the input,

$$V_{fn,in}^2 = \frac{V_{fn}^2}{A_v^2} \tag{3.77}$$

$$V_{fn,in}^2 = \frac{1}{f}\frac{1}{C_{ox}}\frac{1}{g_{m,I}^2}\left(\frac{g_{m,I}^2 K_N}{(WL)_I} + \frac{g_{m,L}^2 K_P}{(WL)_L}\right) \tag{3.78}$$

Similarly, the expression for the input-referred flicker noise current can be determined by keeping the input open, resulting in

$$I_{fn,in}^2 = \frac{1}{f}\frac{1}{C_{ox}}\left(\frac{g_{m,B}^2 K_N}{(WL)_B} + \frac{g_{m,L}^2 K_P}{(WL)_L}\right) \tag{3.79}$$

An important parameter for quantifying the noise performance of the amplifier is the noise figure, which also considers the noise and signal power from the CMUT and therefore gives an indication of the signal-to-noise ratio degradation from the CMUT to the output of the amplifier.

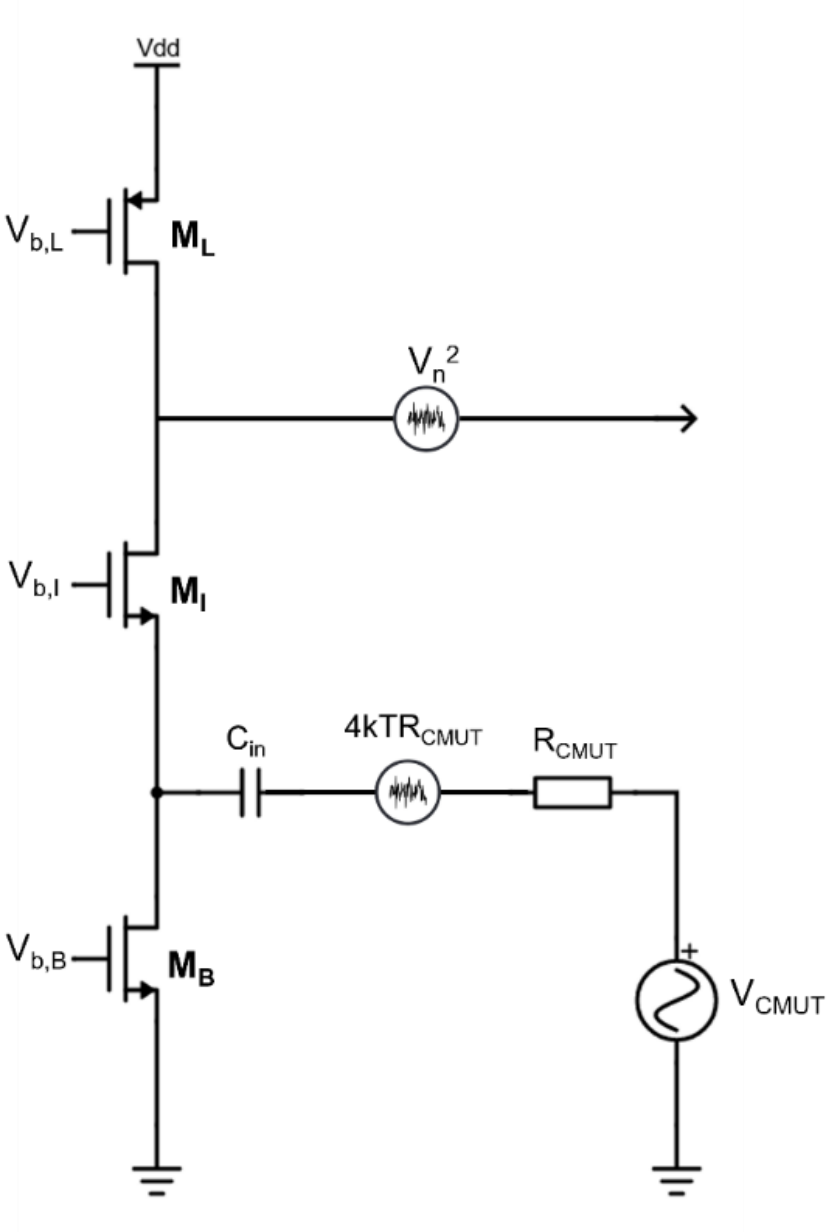

Figure 3 - 18 Common Gate Amplifier Noise Figure Analysis Setup [42].

To begin, consider Figure 3 - 18, which incorporates the signal from the CMUT as a voltage source and includes its resistance. The amplifier is considered noiseless, and a noise voltage source at the output represents the total noise power density of the amplifier. Also, since the input of the amplifier is not at a transistor's gate, the input impedance of the transistor is not particularly high and can be approximated as,

$$R_{in} \approx \frac{1}{g_{m,I}} \tag{3.80}$$

As a result of this, the signal power and noise power from the CMUT are attenuated and are expressed as

$$S_{in} = \left(\frac{V_{CMUT}}{1 + g_{m,I}R_{CMUT}}\right)^2 \tag{3.81}$$

$$N_{in} = \frac{4kTR_{CMUT}}{\left(1 + g_{m,I}R_{CMUT}\right)^2} \tag{3.82}$$

At the output, the signal power and noise power can be expressed as

$$S_{out} = \left(\frac{A_v V_{CMUT}}{1 + g_{m,I}R_{CMUT}}\right)^2 \tag{3.83}$$

$$N_{out} = \frac{A_v^2\, 4kTR_{CMUT}}{\left(1 + g_{m,I}R_{CMUT}\right)^2} + V_n^2 \tag{3.84}$$

Finally, the noise factor of the amplifier can be expressed as

$$F = {S_{in}/N_{in}}\Big/{S_o/N_o} \tag{3.85}$$

$$F = 1 + \frac{V_n^2\left(1 + g_{m,I}R_{CMUT}\right)^2}{4kTR_{CMUT}A_v^2} \tag{3.86}$$

$$NF = 10\log(F) \tag{3.87}$$

3.4.3 Sizing the Common Gate Amplifier

The transconductance of the input transistor in Equation (3.69) and the noise formulations in Section 3.4.2 can be utilized to determine the dimensions of the transistor. The input-referred noise sources indicate that minimizing the transconductance of the load and current source transistors improves noise performance. This implies that both transistors should be sized in strong inversion (small g_m/I_D values) and have low drain current. The drain current is determined by the gm/ID and transconductance of the input transistor. Sizing for a low drain current for the input transistor implies selecting a large g_m/I_D, however, this implies possibly sizing in weak inversion.

The procedure illustrated for sizing the common source amplifier in Section 3.3.3 is adapted for the common gate amplifier, with lookup at the g_m/g_{ds} and I_D/W curves for the transistors performed with respect to the gain requirements expressed in Equation (3.63). For transistors M_L and M_B, a $g_m/I_D = 10\ S/A$ (strong/moderate inversion boundary) was initially selected, and the g_m/I_D of the input varied as presented in Table 3 - 5, which also contains the sizes at the specific g_m/I_D design points.

Table 3 - 5 Transistor Sizes for varying $(g_m/I_D)_I$ *at* $(g_m/I_D)_L = 10$ *and* $(g_m/I_D)_B = 10$

$(g_m/I_D)_I$	$L_I\ (\mu m)$	$W_I\ (\mu m)$	$L_B\ (\mu m)$	$W_B\ (\mu m)$	$L_L\ (\mu m)$	$W_L\ (\mu m)$	$I_D\ (\mu A)$
14	0.4	184	0.4	83.5	0.4	214	450
16	0.4	242	0.4	73.1	0.4	188	394
18	0.4	330	0.4	64.9	0.4	167	350
20	0.4	485	0.4	58.4	0.4	150	315
22	0.4	818	0.4	53.1	0.4	136	286

A further reduction in the g_m/I_D for the load transistor M_L and current bias transistor M_B is still possible. An approach may be to select a specific $(g_m/I_D)_I$ and $(g_m/I_D)_B$ values, while varying $(g_m/I_D)_L$. This could also be done such that specific $(g_m/I_D)_I$ and $(g_m/I_D)_L$ values are selected, while varying $(g_m/I_D)_B$.

Table 3 - 6 Transistor Sizes for simultaneously varying $(g_m/I_D)_L$ and $(g_m/I_D)_B$ at $(g_m/I_D)_I = 20$

$(g_m/I_D)_B$	$(g_m/I_D)_L$	$\mathbf{L_B}$ (μm)	W_B (μm)	$\mathbf{L_L}$ (μm)	W_L (μm)
10	10	0.4	58.4	0.4	150
9	9	0.4	47.2	0.4	120
8	8	0.4	38.0	0.4	94.9
7	7	0.4	29.9	0.4	73.6
6	6	0.4	22.7	0.4	55.6

However, since the objective is to reduce the transconductance of M_B and M_L, then a specific $(g_m/I_D)_I$ value is selected and both $(g_m/I_D)_B$ and $(g_m/I_D)_L$ are varied simultaneously. Table 3 - 6 and Table 3 - 7 summarize the transistor sizes for two specific g_m/I_D values ($(g_m/I_D)_I = 20$ and $(g_m/I_D)_I = 22$) of the input transistor.

Table 3 - 7 Transistor Sizes for simultaneously varying $(g_m/I_D)_L$ and $(g_m/I_D)_B$ at $(g_m/I_D)_I = 22$

$(g_m/I_D)_B$	$(g_m/I_D)_L$	$\mathbf{L_B}$ (μm)	W_B (μm)	$\mathbf{L_L}$ (μm)	W_L (μm)
10	10	0.4	53.1	0.4	136
9	9	0.4	42.9	0.4	109
8	8	0.4	34.5	0.4	86.1
7	7	0.4	27.1	0.4	66.8
6	6	0.4	20.6	0.4	50.4

4 Results and Discussion

The simulation results for the studied amplifiers are presented in this chapter. These results include the frequency response (gain and bandwidth), noise performance and transient analysis of the amplifier with respect to the varying aspect ratios of the transistors involved in the design. Furthermore, a discussion of the important results obtained is presented.

4.1 Noise Performance

From the amplifiers' target specification, a noise figure of less than 3dB was specified to describe the noise the preferred noise performance. To determine this for the various g_m/I_D combinations for each amplifier, the small signal noise analysis tool on Cadence Virtuoso's Analog Design Environment was utilized. A noise analysis over a range of frequencies was done for each amplifier and data including the noise figure, noise summary and output noise of the amplifier is presented in this section. As described in the Chapter 3, the design of the amplifiers utilized the g_m/I_D "knob", essentially exploring a design space of possible g_m/I_D values for the input, load, and biasing transistors.

4.1.1 Common Source Amplifier

This section presents the Noise Figure at each design point for the common source amplifier, as well as a visualization of the noise figure around the center frequency for selected g_m/I_D design points. The Noise Figure values are presented in Table 4 – 1 and Table 4 - 2.

Table 4 – 1 Common Source Amplifier Noise Figure at 7MHz for varying g_m/I_D of Input Transistor

$(g_m/I_D)_I$ for $(g_m/I_D)_L = 10$	NF at f_c = 7 MHz
14 S/A	5.79 dB
16 S/A	5.52 dB
18 S/A	5.32 dB
20 S/A	5.16 dB
22 S/A	5.04 dB

Table 4 - 2 Common Source Amplifier Noise Figure at 7MHz for varying g_m/I_D of Load Transistor

$(g_m/I_D)_L$ for $(g_m/I_D)_I = 20$	NF at f_c = 7 MHz
10 S/A	5.16 dB
9 S/A	5.03 dB
8 S/A	4.89 dB
7 S/A	4.74 dB
6 S/A	4.60 dB

$(g_m/I_D)_L$ for $(g_m/I_D)_I = 22$	NF at f_c = 7 MHz
10 S/A	5.04 dB
9 S/A	4.91 dB
8 S/A	4.78 dB
7 S/A	4.65 dB
6 S/A	4.52 dB

The Noise Figure curves visualizing the trend of the Noise Figure response for $(g_m/I_D)_I = 18\,S/A$, $20\,S/A$ *and* $22\,S/A$ at $(g_m/I_D)_L = 10$ is shown in Figure 4 - 1, while the Noise Figure response at $(g_m/I_D)_L$ = 22 for $(g_m/I_D)_I = 6\,S/A,\ 7\,S/A$ *and* $8\,S/A$ are presented in Figure 4 - 2.

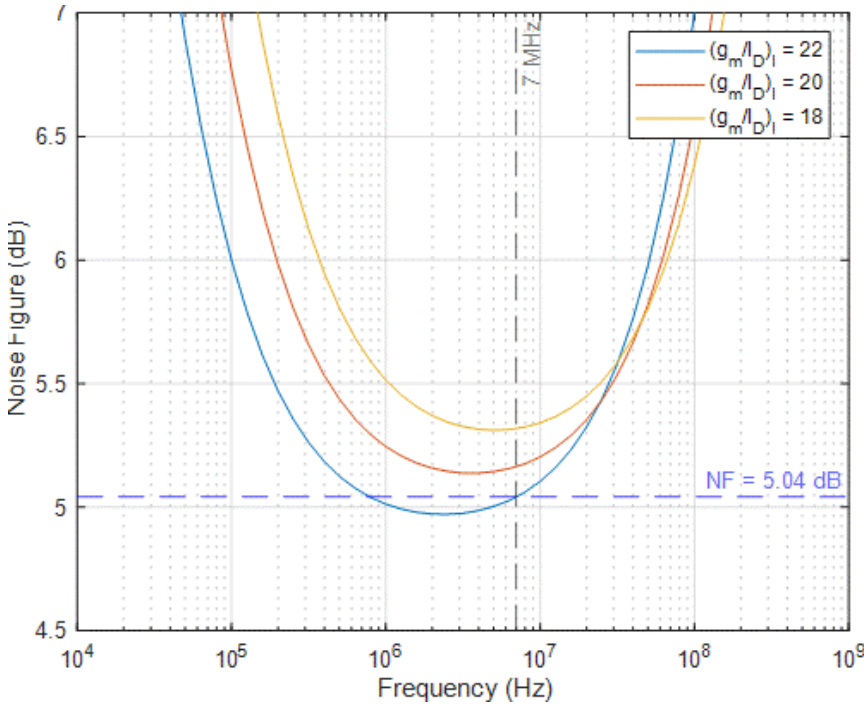

Figure 4 - 1 Common Source Amplifier Noise Figure Curves - $(g_m/I_D)_I$ varied for fixed $(g_m/I_D)_L = 10$

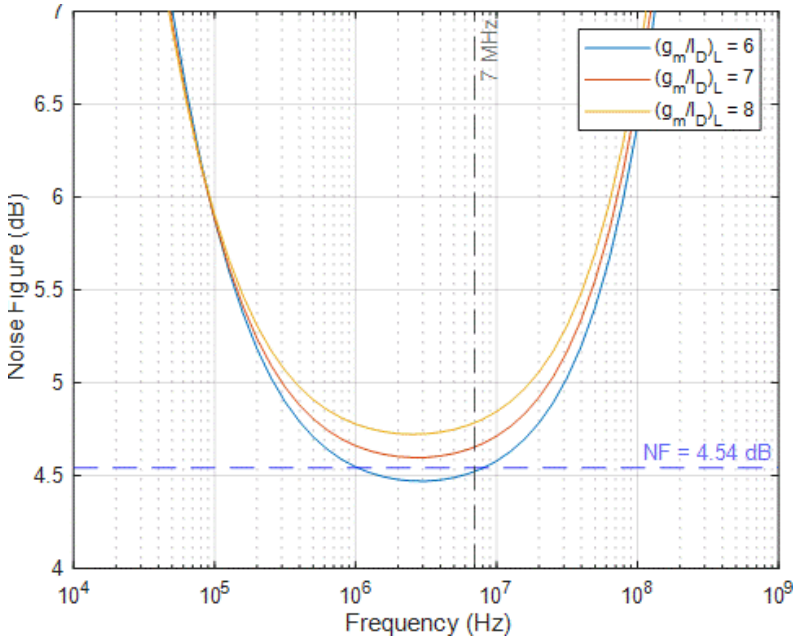

Figure 4 - 2 Common Source Amplifier Noise Figure Curves – $(g_m/I_D)_L$ varied for fixed $(g_m/I_D)_I = 22$

Furthermore, the Noise Figure response for the resistive feedback amplifier analyzed and designed in Section 3.3.4 is presented in Figure 4 - 3.

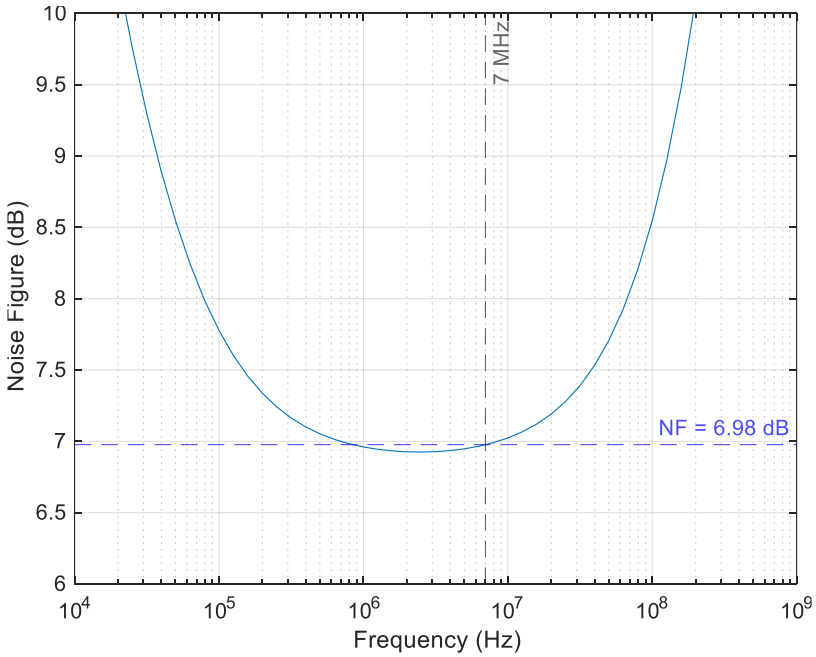

Figure 4 - 3 Noise Figure - Resistive Feedback Amplifier

4.1.2 Common Gate Amplifier

In this section, the Noise Figure values for the Common Gate Amplifier are presented (Table 4 - 3 and

Table 4 - 4). Also, Noise Figure curves showing the trend around the center frequency for selected g_m/I_D design points are shown in Figure 4 - 4 and Figure 4 - 5.

Table 4 - 3 Common Gate Amplifier Noise Figure at 7MHz for varying g_m/I_D of Input Transistor

$(g_m/I_D)_I$ for $(g_m/I_D)_B = 10$ and $(g_m/I_D)_L = 10$	NF at f_c = 7 MHz
14 S/A	16.02 dB
16 S/A	15.47 dB
18 S/A	14.98 dB
20 S/A	14.54 dB
22 S/A	14.16 dB

Table 4 - 4 Common Gate Amplifier Noise Figure at 7MHz for varying g_m/I_D of Load and Bias Transistors

$(g_m/I_D)_B$ and $(g_m/I_D)_L$ for $(g_m/I_D)_I = 20$	NF at f_c = 7 MHz
10 S/A	14.55 dB
9 S/A	14.17 dB
8 S/A	13.77 dB
7 S/A	13.34 dB
6 S/A	12.87 dB

$(g_m/I_D)_B$ and $(g_m/I_D)_L$ for $(g_m/I_D)_I = 22$	NF at f_c = 7 MHz
10 S/A	14.16 dB
9 S/A	13.78 dB
8 S/A	13.39 dB
7 S/A	12.96 dB
6 S/A	12.49 dB

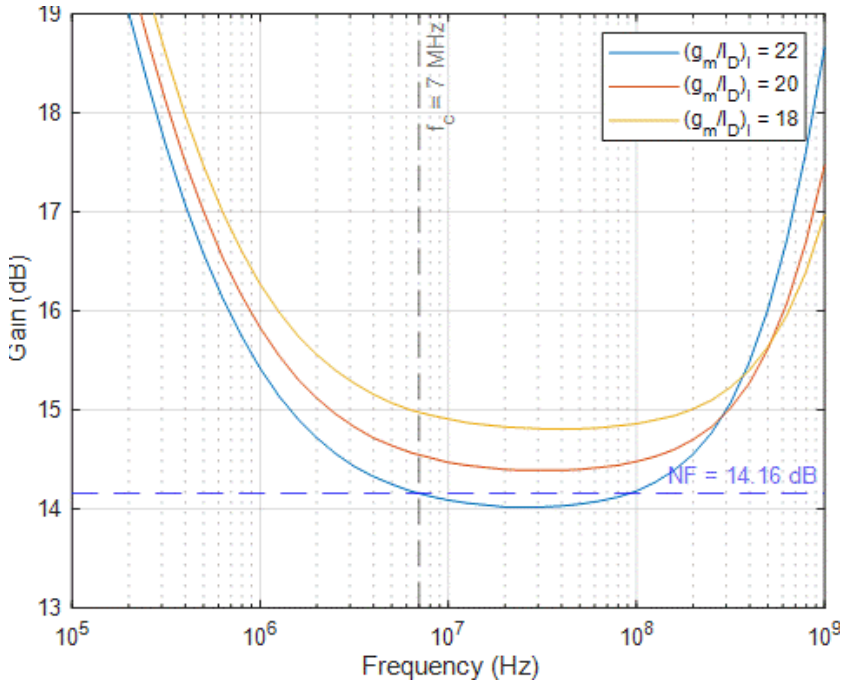

Figure 4 - 4 Common Gate Amplifier Noise Figure Curves - $(g_m/I_D)_I$ varied for fixed $(g_m/I_D)_B = 10$ and $(g_m/I_D)_L = 10$

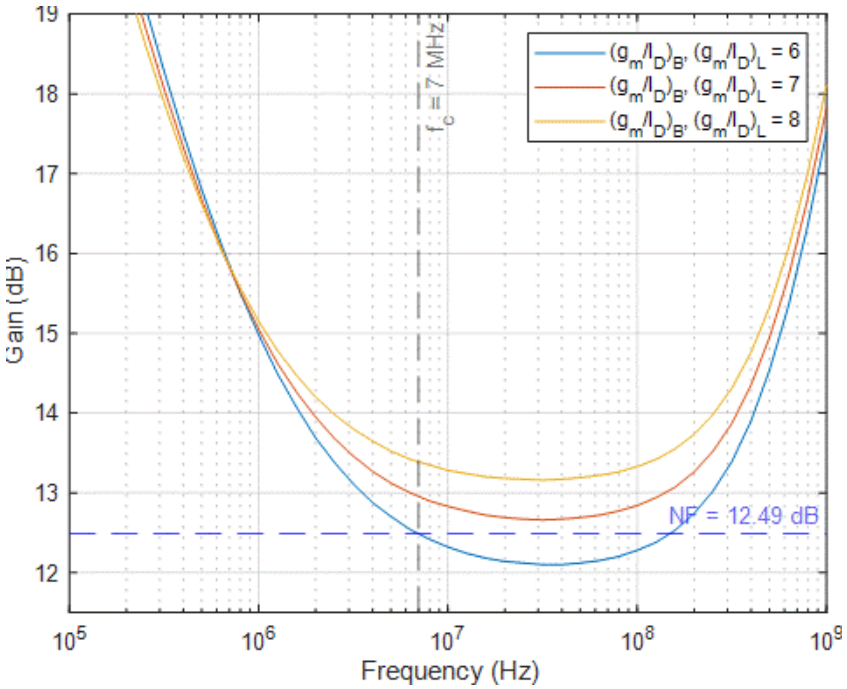

Figure 4 - 5 Common Gate Amplifier Noise Figure Curves – $(g_m/I_D)_B$ and $(g_m/I_D)_L$ varied for fixed $(g_m/I_D)_I = 22$

4.1.3 Discussion

A first look at the Noise Figures presented in the tables for both amplifiers indicates the superior noise performance of the common source amplifier, as worst-case noise figure (5.79 dB) of the common source amplifier at the design point ($(g_m/I_D)_I = 14$, $(g_m/I_D)_L = 10$) is much lower than the best-case noise figure of the common gate amplifier which is 12.49 dB at the design point ($(g_m/I_D)_I = 22$, $(g_m/I_D)_B = 6$ and $(g_m/I_D)_L = 6$).

Also, in Table 4 – 1, the noise figure for the common source amplifier reduces as $(g_m/I_D)_I$ is maximized. It is necessary to note that increasing $(g_m/I_D)_I$ increases the width of the transistor for a fixed length. Considering the noise analysis of the amplifier which yielded Equation (3.17), it can be inferred that the improvement (decrease) in the noise figure of the amplifier is due to the reduction of flicker noise in the amplifier since the area of the input transistor increases. Furthermore, it should be noted that the transconductance of the load transistor is minimized by this sweep as well, therefore, the thermal noise of the amplifier is also slightly minimized. However, as a counter argument, it should also be considered that the width of the load transistor is minimized as the g_m/I_D of the input transistor is maximized, indicating that the reduction in flicker noise by increasing the area of the input transistor is cancelled. However, an observation of the reduction trend of the load transistor's width suggests that its rate of reduction is less than the rate of increase of the input transistor's width.

Furthermore, an observation of Table 4 - 2 also shows a minimization of the noise figure as the g_m/I_D for the load transistor is minimized. In this case, the width of the input transistor is fixed, while that of the load transistor is also minimized, therefore, a tunnel-vision based observation would be to say that the flicker noise in the transistor should increase, thereby degrading the noise performance of the amplifier. However, minimizing the g_m/I_D of the load transistor also minimizes its transconductance, which one can suggest would oppose the increase in flicker noise as a result of a reduction in area, and additionally reduce its thermal noise.

Again, considering the noise figures in Table 4 - 3 for the common gate amplifier, the slight improvement in the noise performance due to minimizing the g_m/I_D of the input transistor can be attributed to a reduction in the thermal noise of the load and bias transistors. This is because of the decrease in their transconductances. Although the widths of both transistors decrease, which could effectively increase their flicker noise, the minimized transconductance reduces the effect of the width on the flicker noise. This is also the case of the noise performance trend in Table 4 - 4.

Also, another argument can be made for reducing the flicker noise in the common gate amplifier by increasing the length of the load and bias transistors, however, to maintain the g_m/I_D for a particular transistor, increasing the length also requires increasing the width of the transistor. At first glance, since increasing the width and the length of the transistors, leads to increase in area, then further reduction in flicker noise could be achieved. However, it should be noted that the g_m/I_D for bias and load transistors indicates that they should operate in strong inversion, which effectively means that their transconductances increase thereby reversing the expected flicker noise reduction and further increasing the amplifier's thermal noise.

Furthermore, in Figure 4 - 3, the noise figure curve for the resistive feedback common source amplifier is shown. The noise figure at 7 MHz is 6.98 dB which is higher than that of the open loop amplifier for the same g_m/I_D design point, indicating that feedback does not improve the noise figure of an amplifier system as demonstrated in [36].

4.2 Gain and Bandwidth

The desired minimum gain and bandwidth are important specifications for the design of amplifiers; therefore, it is necessary to verify that the designed amplifier matches the specifications. To do so, the small signal frequency response simulations were done via the ac analysis tool in Cadence Virtuoso's Analog Design Environment to simulate the response of the amplifiers to a range of frequencies, specifically 1 Hz to 1 GHz.

In Figure 4 - 6, the small signal gain response of the common source amplifier for a couple of g_m/I_D design points are presented. As expected, the low frequency gain for each point is more than 30 dB, thereby fulfilling the design expectations. Also, the unity gain frequencies for the design points are approximately 100 MHz, which also fulfills the gain bandwidth requirements. Furthermore, the most important feature is the gain at 7 MHz which lies between 22.80 dB to 23.00 dB for the design points in the figure. This fulfills the requirement for having a small signal gain greater than 20 dB at the center frequency.

Also, to ensure the robustness of the gain of the common source amplifier, resistive feedback was introduced. Figure 4 - 7 shows the gain response of the feedback amplifier, having a gain of 20.04 dB at the center frequency, which fulfils the target specifications. Also, it should be noted that the open loop amplifier gain values in Figure 4 - 6 can change considerably due to process, voltage, and temperature variations.

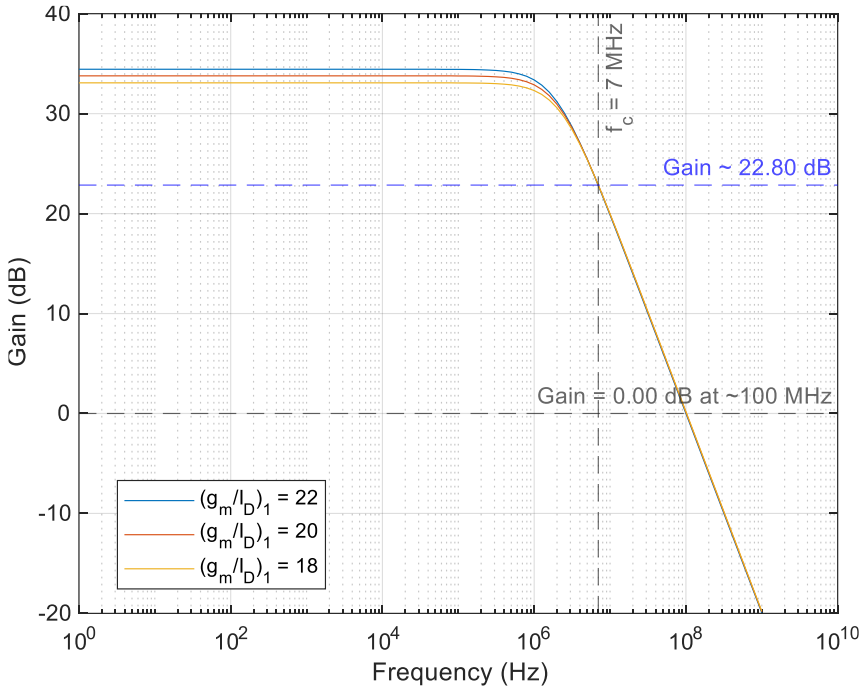

Figure 4 - 6 Gain Frequency Response of the Common Source Stage (varying $(g_m/I_D)_I$ at $(g_m/I_D)_L = 10$)

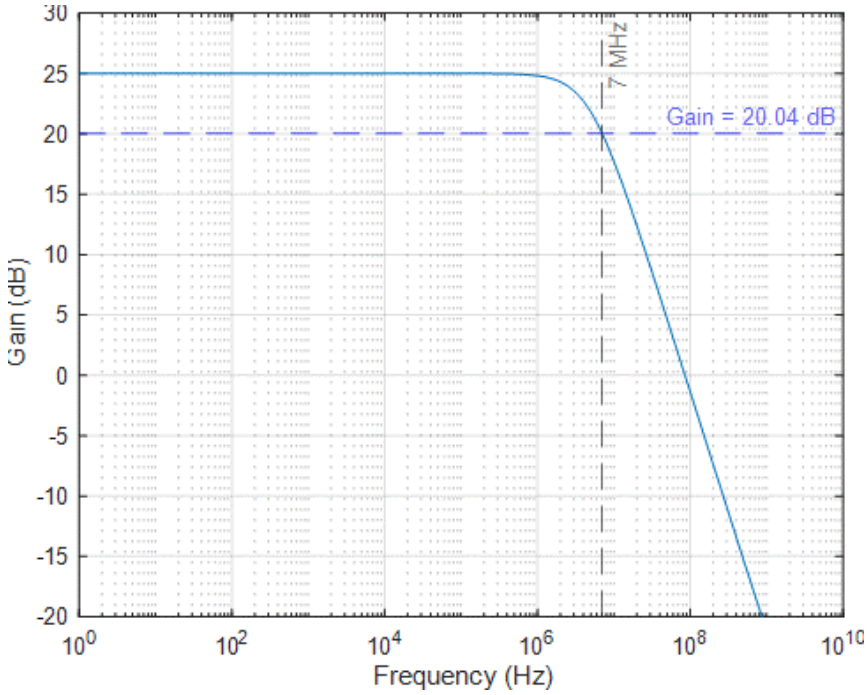

Figure 4 - 7 Resistive Feedback Common Source Amplifier Gain Frequency Response

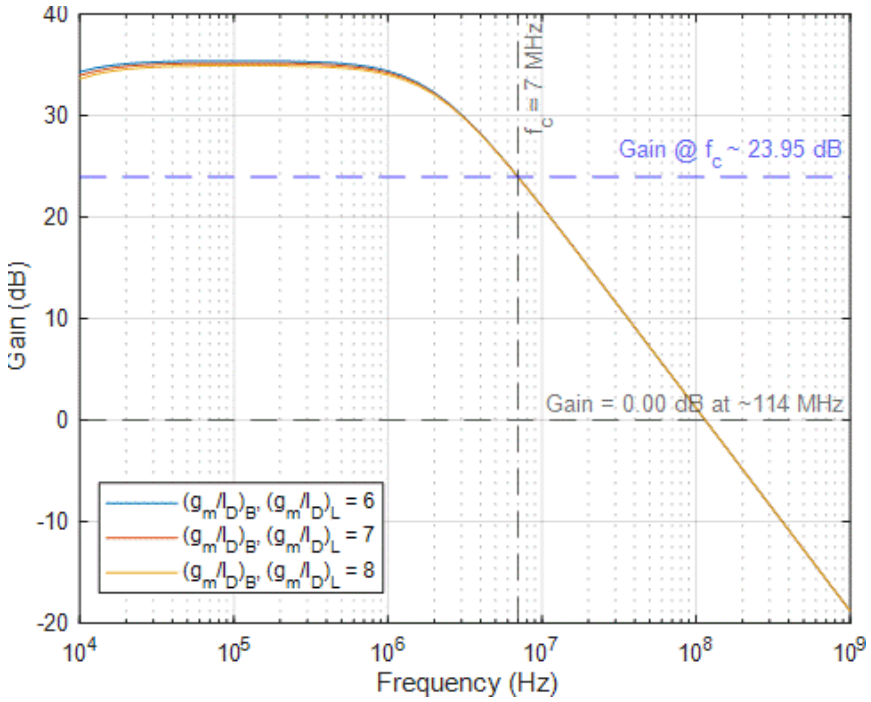

Figure 4 - 8 Gain Frequency Response of the Common Gate Stage (varying $(g_m/I_D)_I$ *at* $(g_m/I_D)_B = 10$ *and* $(g_m/I_D)_L = 10$*)*

Furthermore, in Figure 4 - 8, the gain response of the common gate amplifier is presented. As in the case of the common source amplifier, it fulfills the gain requirements set for the amplifier, having a low frequency gain greater than 30 dB, unity gain frequency about 114 MHz, and approximately 24 dB gain at 7 MHz. It should be noted that the observed dip at low frequencies in the gain response of the common gate amplifier is not inherent to the amplifier, but due to the high-pass filter formed by the ac coupling capacitor and amplifier's input impedance.

Furthermore, considering the frequency response of both amplifiers as shown in Figure 4 - 6, Figure 4 - 7 and Figure 4 - 8, the assumption that the load capacitance and output conductance constitute the dominant pole is justified, as no other poles are observed in the response, even pass the 0 dB point.

4.3 Transient Response

The transient behaviour of the resistive feedback common source amplifier at the design point $(g_m/I_D)_I = 22$ and $(g_m/I_D)_L = 6$ is presented in Figure 4 - 9.

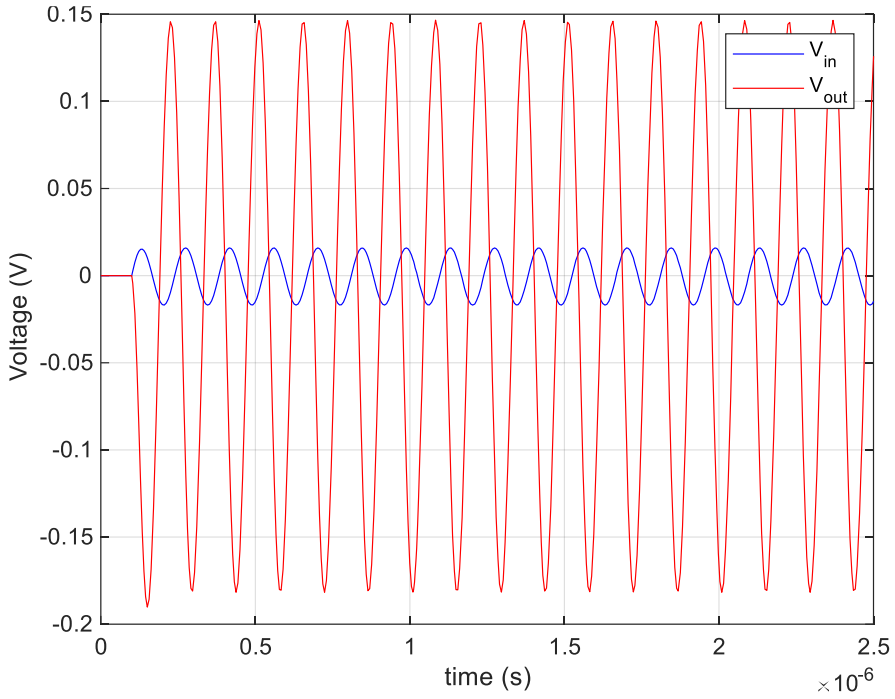

Figure 4 - 9 Resistive Feedback Common Source Amplifier Transient Response

Also, for the common gate amplifier, the transient response at the design point $(g_m/I_D)_I = 22$, $(g_m/I_D)_B = 6$ and $(g_m/I_D)_L = 6$ is shown in Figure 4 - 10.

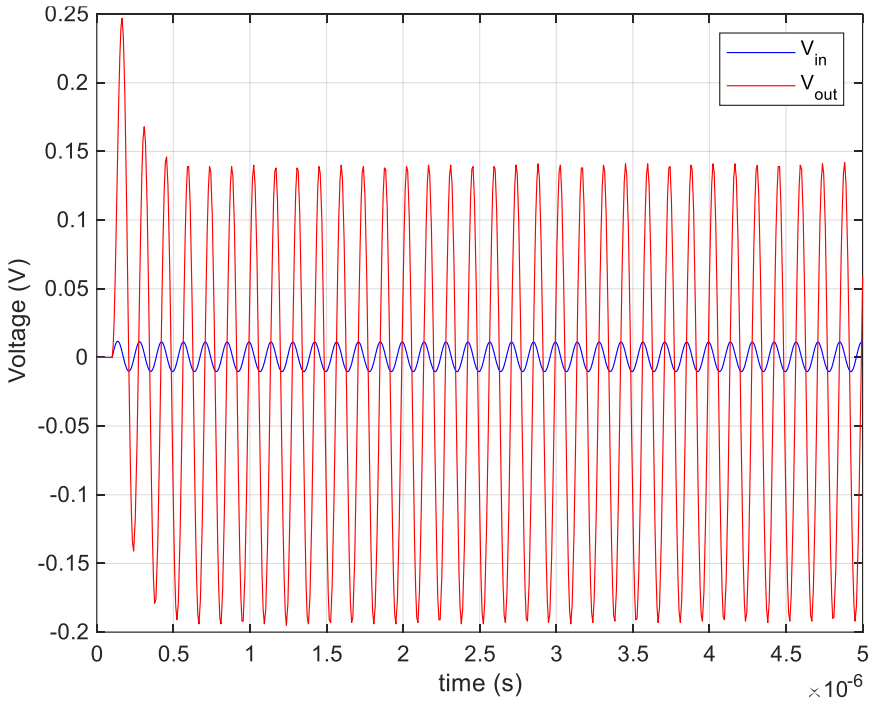

Figure 4 - 10 Common Gate Amplifier Transient Response

The input signal was at the centre frequency of the CMUT – 7 MHz and was in this case used to model the received ultrasound pulse. The response from both amplifiers shows they are able to amplify the signal level of the input signal.

4.4 Performance Summary

In Table 4 - 5, a summary of important parameters of Resistive Feedback Common Source (RS-CS) amplifier and the Common Gate (CG) amplifier is presented. The gm/ID design point of the common gate amplifier summarized in the table is $(g_m/I_D)_I = 22$, $(g_m/I_D)_B = 6$ and $(g_m/I_D)_L = 6$.

Table 4 - 5 Parameter Summary for RS-CS and CG Amplifiers

Parameter	*RF-CS Amplifier*	*CG Amplifier*
Noise Figure at f_c	6.98 dB	12.49 dB
Low Frequency Gain	25.00 dB	35.38 dB
Reference Current	57.20 µA	57.20 µA
Power Consumption	188.76 µW	188.76 µW
Unity Gain Frequency (f_{ug})	85.41 MHz	114.80 MHz
Gain at f_c	20.04 dB	23.90 dB
Phase Margin	60.45 °	N/A
Gain Margin	27.25 dB	N/A

5 Conclusion

This work presented the analysis and design of low-noise amplifiers (LNAs) specifically tailored for medical ultrasound imaging. Two amplifier topologies, namely the common source (including resistive feedback) and common gate configurations, were utilized. These amplifiers were implemented using the AMS-0.35µm CMOS process and were intended to operate in receive mode for the Dual-Frequency Hybrid Ultrasonic Transducer (DHUT).

In the DHUT's transmit/receive scheme, ultrasound echoes from bodily tissues are received using a Capacitive Micromachined Ultrasonic Transducer (CMUT). Therefore, the amplifiers were designed to sense signals from the CMUT. To facilitate the amplifier design, an existing analytical model for a collapsed CMUT array was adapted. This model allowed for an investigation of the CMUT's frequency response and determination of its center frequency, which proved valuable in the amplifier design process.

For amplifier design, the small signal model and noise characteristics were thoroughly analyzed to inform design parameter decisions. The design approach extensively utilized the g_m/I_D based design methodology for CMOS analog circuits. Various g_m/I_D combinations for the transistors in each amplifier were explored, with a focus on investigating noise performance as indicated by the noise figure.

The common source amplifier achieved a minimum noise figure of 4.52 dB, which increased to 6.98 dB when incorporating resistive feedback. On the other hand, the common gate amplifier achieved a minimum noise figure of 12.49 dB. At each g_m/I_D design point, additional performance metrics such as gain, unity gain frequency, and power consumption were evaluated. For the design points corresponding to the aforementioned noise figures, the resistive feedback common source amplifier exhibited a low-frequency gain of 25 dB, a gain of 20 dB at the center frequency (7 MHz), and an approximate unity gain frequency of 85 MHz with a 10 pF capacitive load. The common gate amplifier featured a low-frequency gain of approximately 35 dB, a gain of 24 dB at the center frequency, and operated with a unity gain frequency of 114 MHz with the same capacitive load. The power consumption of both amplifiers was approximately 189 µW.

5.1 Future Work

Further work requires conducting additional investigations into the harmonic distortion properties of the amplifiers. Additionally, it is necessary to generate layouts and perform post-layout simulations

for both amplifiers. Moreover, in the explored design space, the achieved minimum noise figures for both amplifiers exceeded the target specification of 3 dB. Therefore, an immediate extension to this work would involve exploring noise performance improvements by replacing the input transistor of each amplifier with a PMOS transistor.

Furthermore, it is worth considering the investigation of noise cancellation schemes for both amplifiers. Specifically, applying the feedforward noise cancellation scheme to the resistive feedback amplifier and implementing a single-ended to differential common-gate-common-source noise cancellation scheme for the common gate amplifier.

Another aspect to consider is the exploration and design of variable gain schemes for both amplifiers, enabling time gain compensation. In addition to the LNA, the transmit/receive switch and transmission driver circuit are essential components that form the entire analog interface for the Dual-Frequency Hybrid Ultrasonic Transducer, each of which could be designed and implemented as future projects.

References

[1] O. Mirea, C. Wulff, and T. Ytterdal, “Current-reuse Low-Power Single-Ended to Differential LNA for Medical Ultrasound Imaging,” in *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*, 2021.

[2] K. Naderi, E. H. T. Shad, M. Molinas, A. Heidari, and T. Ytterdal, “A Very Low SEF Neural Amplifier by Utilizing a High Swing Current-Reuse Amplifier,” *2020 35th Conference on Design of Circuits and Integrated Systems, DCIS 2020*, Nov. 2020, doi: 10.1109/DCIS51330.2020.9268627.

[3] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, “Wide-band CMOS low-noise amplifier exploiting thermal noise canceling,” *IEEE J Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004, doi: 10.1109/JSSC.2003.821786.

[4] Y. Tang *et al.*, “Wideband LNA with 1.9 dB noise figure in 0.18 µm CMOS for high frequency ultrasound imaging applications,” *14th IEEE International NEWCAS Conference, NEWCAS 2016*, Oct. 2016, doi: 10.1109/NEWCAS.2016.7604826.

[5] Y. Tang, Y. Feng, Q. Fan, C. Fang, J. Zou, and J. Chen, “A wideband complementary noise and distortion canceling LNA for high-frequency ultrasound imaging applications,” *Proceedings of the 2018 Texas Symposium on Wireless and Microwave Circuits and Systems, WMCS 2018*, pp. 1–4, Jun. 2018, doi: 10.1109/WMCAS.2018.8400635.

[6] Y. Tang *et al.*, “A Wideband Noise and Harmonic Distortion Canceling Low-Noise Amplifier for High-Frequency Ultrasound Transducers,” *Sensors 2021, Vol. 21, Page 8476*, vol. 21, no. 24, p. 8476, Dec. 2021, doi: 10.3390/S21248476.

[7] J. S. Chen, C. W. Lu, C. Hsia, and Y. H. Chen, “A low noise amplifier employing noise canceling technique for ultrasound system applications,” *Proceedings - 2012 International Symposium on Instrumentation and Measurement, Sensor Network and Automation, IMSNA 2012*, vol. 1, pp. 35–38, 2012, doi: 10.1109/MSNA.2012.6324511.

[8] J. DIao, S. Li, Y. Wu, F. Ye, J. Xu, and J. Ren, “Energy-Efficient Analog Frond-End Design for Ultrasound Imaging Applications,” *Midwest Symposium on Circuits and Systems*, vol. 2019-August, pp. 1171–1174, Aug. 2019, doi: 10.1109/MWSCAS.2019.8885304.

[9] J. H. Eriksrod and T. Ytterdal, “A 65nm CMOS front-end LNA for medical ultrasound imaging with feedback employing noise and distortion cancellation,” *2013 European Conference on Circuit Theory and Design, ECCTD 2013 - Proceedings*, 2013, doi: 10.1109/ECCTD.2013.6662292.

[10] A. Suna and S. Ozoguz, “A high linearity low power 130 nm CMOS LNA for medical ultrasound imaging,” *2019 26th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2019*, pp. 687–690, Nov. 2019, doi: 10.1109/ICECS46596.2019.8965090.

[11] S. Firouz, E. N. Aghdam, and R. Jafarnejad, “A Low Power, Low Noise, Single-Ended to Differential TIA for Ultrasound Imaging Probes,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 2, pp. 607–611, Feb. 2021, doi: 10.1109/TCSII.2020.3018223.

[12] F. Silveira, D. Flandre, and P. G. A. Jespers, “A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA,” *IEEE J Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep. 1996, doi: 10.1109/4.535416.

[13] P. G. A. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits*. Cambridge University Press, 2017. doi: 10.1017/9781108125840.

[14] H. Sehmbi and A. Perlas, “Basics of Ultrasound Imaging,” *Regional Nerve Blocks in Anesthesia and Pain Therapy*, pp. 33–52, 2022, doi: 10.1007/978-3-030-88727-8_2.

[15] H.-Y. Tang, “Interface Electronics for Ultrasonic Transducers,” 2016.

[16] E. Brunner, “Ultrasound System Considerations and their Impact on Front-End Components,” 2002.

[17] L. W. Schmerr, “Fundamentals of Ultrasonic Phased Arrays,” vol. 215, 2015, doi: 10.1007/978-3-319-07272-2.

[18] J. DIao, S. Li, Y. Wu, F. Ye, J. Xu, and J. Ren, “Energy-Efficient Analog Frond-End Design for Ultrasound Imaging Applications,” *Midwest Symposium on Circuits and Systems*, vol. 2019-August, pp. 1171–1174, Aug. 2019, doi: 10.1109/MWSCAS.2019.8885304.

[19] I. O. Wygant *et al.*, “Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging,” *IEEE Trans Ultrason Ferroelectr Freq Control*, vol. 55, no. 2, pp. 327–341, Feb. 2008, doi: 10.1109/TUFFC.2008.652.

[20] Q. H. Duong, Q. Le, C. W. Kim, and S. G. Lee, “A 95-dB linear low-power variable gain amplifier,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 8, pp. 1648–1657, 2006, doi: 10.1109/TCSI.2006.879058.

[21] E. Kang *et al.*, “A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes,” *IEEE J Solid-State Circuits*, vol. 55, no. 12, pp. 3157–3168, Dec. 2020, doi: 10.1109/JSSC.2020.3023618.

[22] Z. Yu *et al.*, “Front-end receiver electronics for a matrix transducer for 3-D transesophageal echocardiography,” *IEEE Trans Ultrason Ferroelectr Freq Control*, vol. 59, no. 7, pp. 1500–1512, 2012, doi: 10.1109/TUFFC.2012.2350.

[23] Y. Wang, M. Koen, and D. Ma, “Low-noise CMOS TGC amplifier with adaptive gain control for ultrasound imaging receivers,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 1, pp. 26–30, 2011, doi: 10.1109/TCSII.2010.2092822.

[24] M. E. Schafer and P. A. Lewin, “The Influence of Front-End Hardware on Digital Ultrasonic Imaging,” *IEEE Trans Sonics Ultrason*, vol. 31, no. 4, pp. 295–306, 1984, doi: 10.1109/T-SU.1984.31510.

[25] J. X. J. Zhang and K. Hoshino, “Implantable Sensors,” *Molecular Sensors and Nanodevices*, pp. 415–465, Jan. 2014, doi: 10.1016/B978-1-4557-7631-3.00007-7.

[26] H. Azhari, “Basics of Biomedical Ultrasound for Engineers,” *Basics of Biomedical Ultrasound for Engineers*, Apr. 2010, doi: 10.1002/9780470561478.

[27] L. Svilainis and G. Motiejunas, “Power amplifier for ultrasonic transducer excitation,” 2006, doi: 10.5755/J01.U.58.1.16970.

[28] S. Sherrit, H. D. Wiederick, and B. K. Mukherjee, “Accurate equivalent circuits for unloaded piezoelectric resonators,” *Proceedings of the IEEE Ultrasonics Symposium*, vol. 2, pp. 931–935, 1997, doi: 10.1109/ULTSYM.1997.661733.

[29] K. Brenner, A. S. Ergun, K. Firouzi, M. F. Rasmussen, Q. Stedman, and B. Khuri-Yakub, “Advances in Capacitive Micromachined Ultrasonic Transducers,” *Micromachines (Basel)*, vol. 10, no. 2, 2019, doi: 10.3390/MI10020152.

[30] A. S. Ergun, G. G. Yaralioglu, and B. T. Khuri-Yakub, “Capacitive Micromachined Ultrasonic Transducers: Theory and Technology,” *J Aerosp Eng*, vol. 16, no. 2, pp. 76–84, Apr. 2003, doi: 10.1061/(ASCE)0893-1321(2003)16:2(76).

[31] J. Joseph, B. Ma, and B. T. Khuri-Yakub, “Applications of Capacitive Micromachined Ultrasonic Transducers: A Comprehensive Review,” *IEEE Trans Ultrason Ferroelectr Freq Control*, vol. 69, no. 2, pp. 456–467, Feb. 2022, doi: 10.1109/TUFFC.2021.3112917.

[32] A. Stuart Savoia *et al.*, “A 120+ 120- Element Crisscross CMUT Probe’s with Real-Time Switchable Electronic and Fresnel Focusing Capabilities,” *IEEE International Ultrasonics Symposium, IUS*, vol. 2018-October, Dec. 2018, doi: 10.1109/ULTSYM.2018.8580084.

[33] T. Manh, L. Hoff, T. Eggen, T. F. Johansen, F. Lanteri, and J. F. Gelly, “Dual frequency hybrid ultrasonic transducers - Design and simulations,” *IEEE International Ultrasonics Symposium, IUS*, vol. 2016-November, Nov. 2016, doi: 10.1109/ULTSYM.2016.7728599.

[34] A. Stuart Savoia *et al.*, “Design, Fabrication and Characterization of a Hybrid Piezoelectric-CMUT Dual-Frequency Ultrasonic Transducer,” *IEEE International Ultrasonics Symposium, IUS*, vol. 2018-October, Dec. 2018, doi: 10.1109/ULTSYM.2018.8580125.

[35] W. M. Leach, “Fundamentals of Low-Noise Analog Circuit Design,” *Proceedings of the IEEE*, vol. 82, no. 10, pp. 1515–1538, 1994, doi: 10.1109/5.326411.

[36] J. Connelly, “Low noise electronic system design,” *Choice Reviews Online*, vol. 31, no. 05, pp. 31-2710-31–2710, Jan. 1993, doi: 10.5860/CHOICE.31-2710.

[37] B. Razavi, *Design of Analog CMOS Integrated Circuits. Second Edition*. 2017.

[38] J. B. Johnson, “Thermal agitation of electricity in conductors,” *Nature*, vol. 119, no. 2984, pp. 50–51, 1927, doi: 10.1038/119050C0.

[39] A. Van Der Ziel, “Thermal Noise in Field-Effect Transistors,” *Proceedings of the IRE*, vol. 50, no. 8, pp. 1808–1812, 1962, doi: 10.1109/JRPROC.1962.288221.

[40] H. F. Teng, S. L. Jang, and M. H. Juang, “A unified model for high-frequency current noise of MOSFETs,” *Solid State Electron*, vol. 47, no. 11, pp. 2043–2048, Nov. 2003, doi: 10.1016/S0038-1101(03)00248-X.

[41] H. T. FRIIS, “Noise Figures of Radio Receivers,” *Proceedings of the IRE*, vol. 32, no. 7, pp. 419–422, 1944, doi: 10.1109/JRPROC.1944.232049.

[42] B. Razavi, *RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*. 2011.

[43] A. S. Sedra and K. C. (Kenneth C. Smith, *Microelectronic circuits*, Seventh Edition. Oxford University Press, 2015. Accessed: Jun. 25, 2023. [Online]. Available: https://books.google.com/books/about/Microelectronic_Circuits.html?hl=no&id=idO-oQEACAAJ

[44] M. H. (Muhammad H. Rashid, *Microelectronic circuits : analysis and design*. Cengage Learning, 2011.

[45] T. C. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuits Design 2nd*. 2012.

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Appendices

MOSFET Parameter Extraction Setup

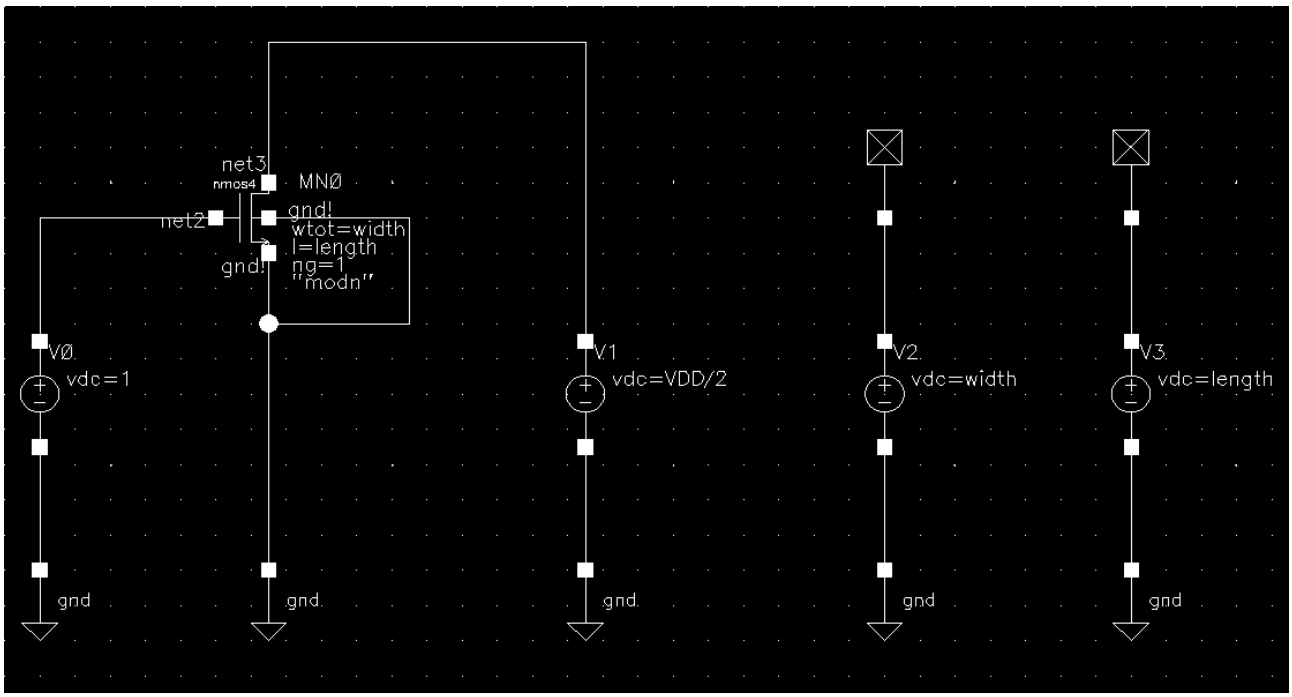

Figure A - 1 NMOS Parameter Extraction setup

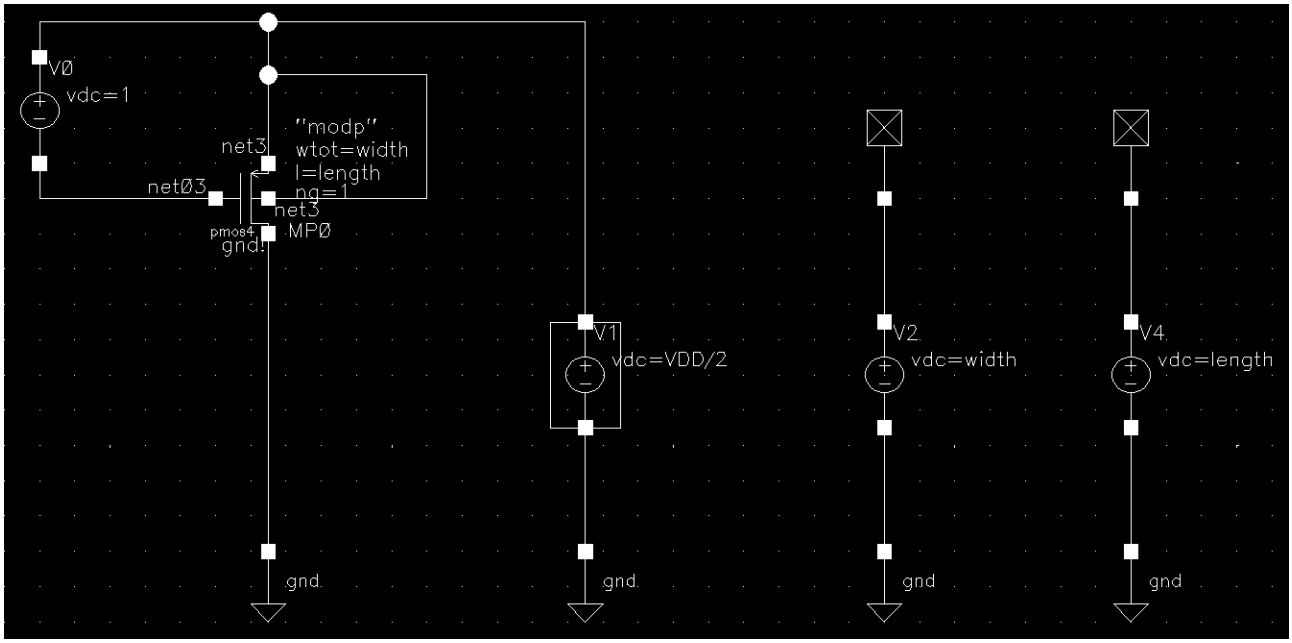

Figure A - 2 PMOS Parameter Extraction setup

Amplifiers Schematics

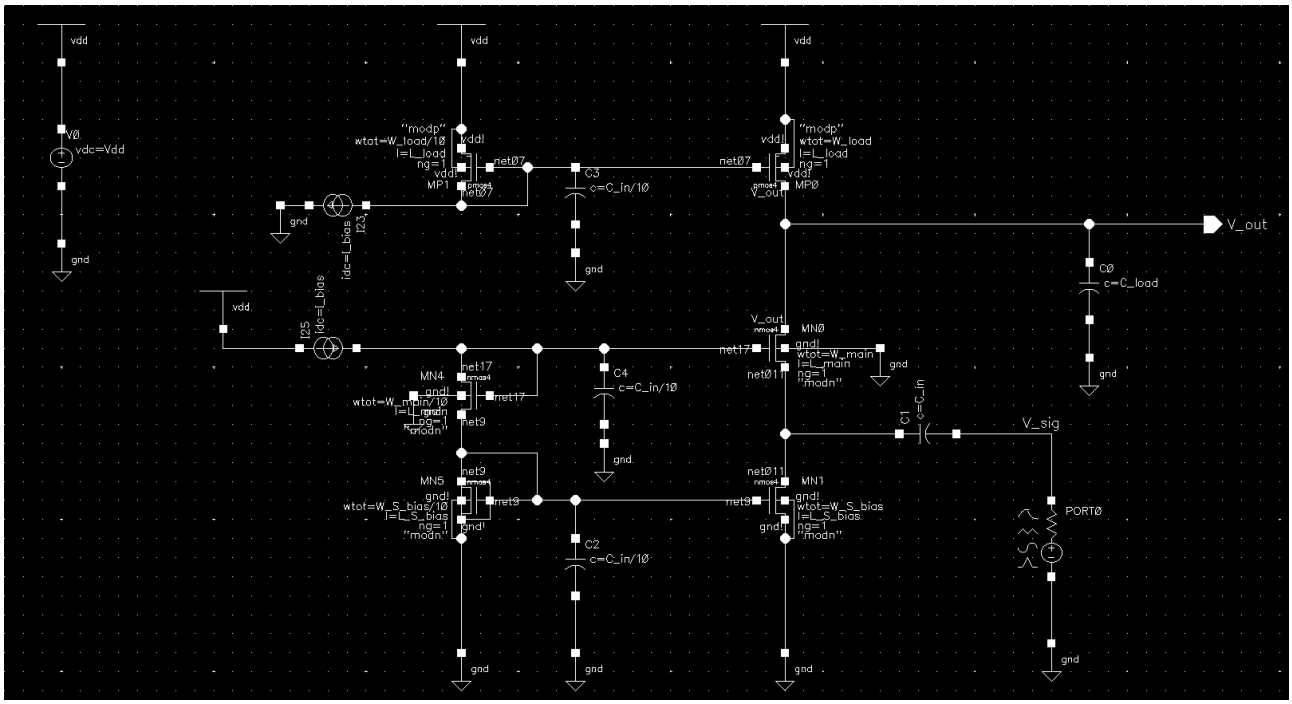

Figure A - 3 Common Gate Amplifier Schematic and Testbench

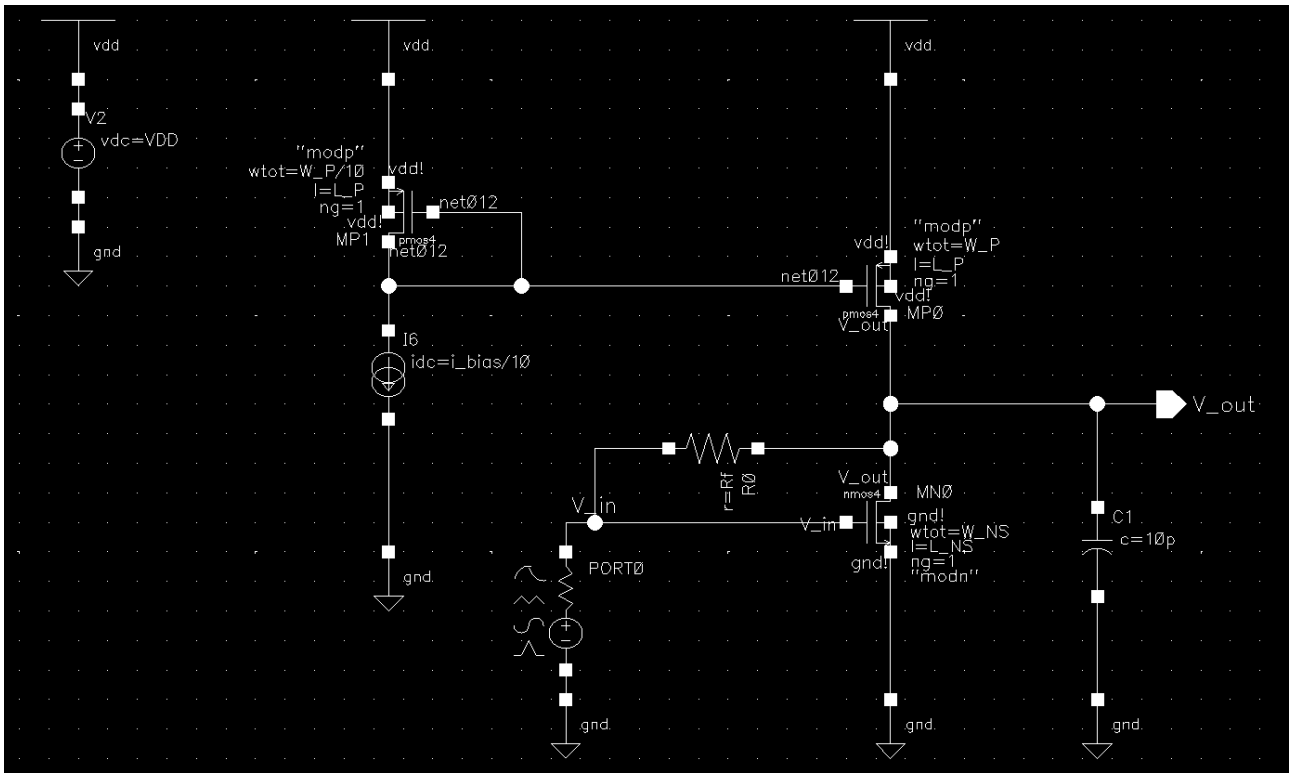

Figure A - 4 Common Source Amplifier Schematic and Testbench