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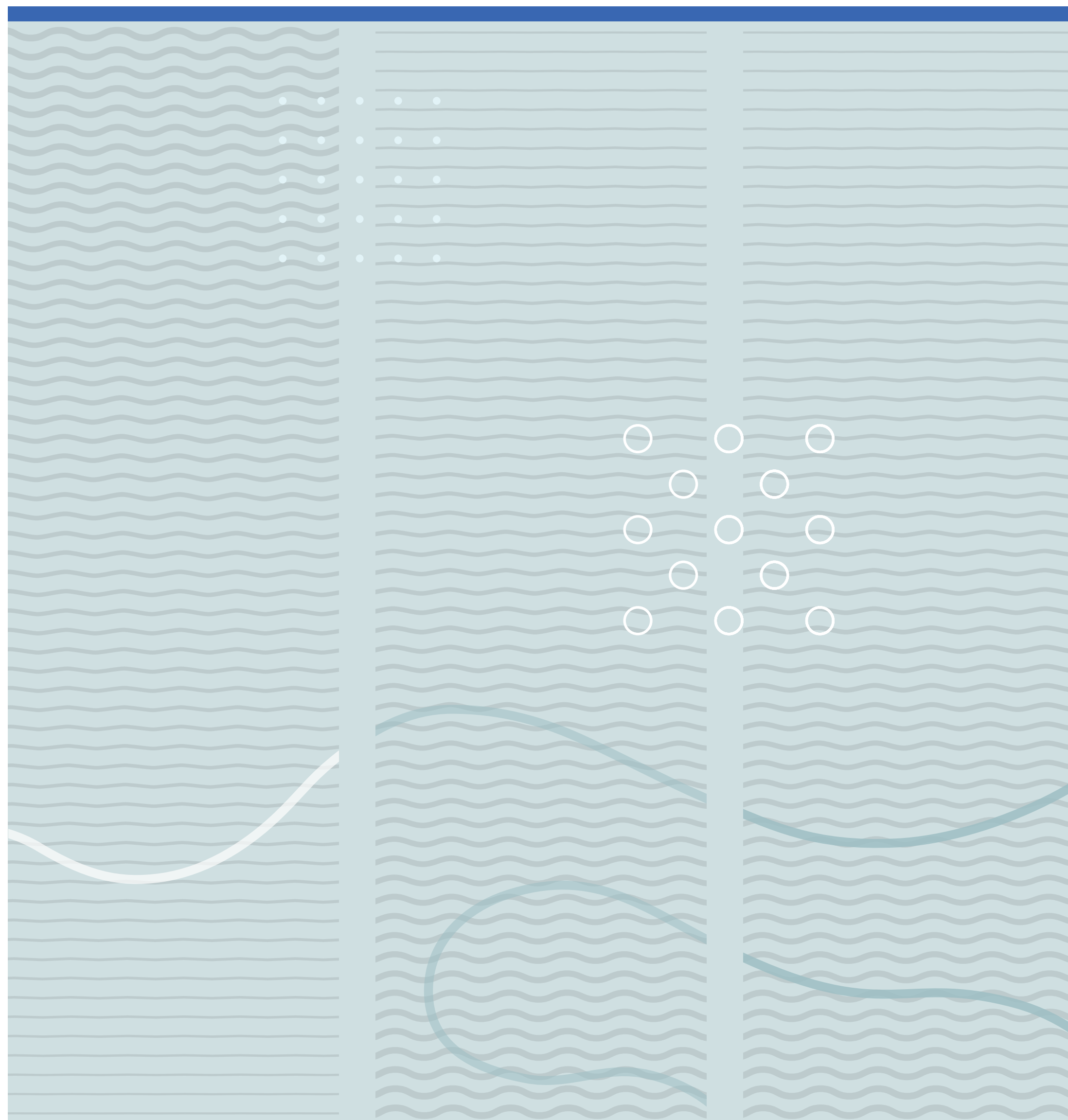
Phillip Papatzacos

Improved packaging techniques for LWIR microbolometers



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Improved packaging techniques for LWIR microbolometers

A PhD dissertation in
Applied micro- and nanosystems

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Dedication

I would like to dedicate this work to my family for making me who I am, my supervisors for teaching me what I know, and my wife for keeping me sane.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of Philosophiae Doctor (Ph.D.) from the Department of Microsystems, at the University of South-Eastern Norway (USN). This doctoral work has mainly been conducted at the Department of Microsystems (IMS), Faculty of Technology, Natural Sciences and Maritime Sciences, University of South-Eastern Norway (USN) in Borre, Norway. Experiments have also been carried out at Stanford University in Palo Alto, USA. The work has been done under the supervision of Professor Emeritus Per Øhlckers, Professor Knut E. Aasmundtveit, Associate Professor Hoang-Vu Nguyen, Associate Professor Avisek Roy, and Postdoctoral Fellow Eivind Bardalen at USN, and Professor Olav Solgaard at the University of Stanford.

This work was carried out with funding by the ECSEL Joint Undertaking (JU) project APPLAUSE under grant agreement No 826588. The JU receives support from the European Union's Horizon 2020 research and innovation program. The Research Council of Norway is also acknowledged for its support to APPLAUSE and the Norwegian Micro- and NanoFabrication Facility (NorFab, project number: 245963/F50). Part of this work was performed at the Stanford Nano Shared Facilities (SNSF), supported by the National Science Foundation under award ECCS-2026822.

Acknowledgments

I would first and foremost like to acknowledge my supervisors. They have answered my questions, read my writings, corrected my mistakes, and put up with my frustrations. Working under you has made me improve both as an academic and a human being.

I would also like to thank my colleagues, both domestic and abroad. I hope and suspect I'll retain many of the friends I have made at USN, Stanford University, Alto University, and IDEAS for many years to come.

There is also no way this work could have been completed without the skilled staff at USN. I would like to particularly acknowledge Zekija Ramic, Ole Henrik Gausland, and Thai Anh Tuan Nguyen for skillfully performing the thankless job of keeping the lab equipment functional. I would also like to acknowledge Kitty Lien for providing great food and even greater smiles, both of which never failed to improve my day.

Finally, I would like to acknowledge my wife, Ine Papatzacos. Thank you for taking part in my successes and helping me get through my failures. Thank you for inspiring me to work harder and for helping me relax. Thank you for listening to my ramblings and helping me make sense of my own mind. If there were no other indicators, the fact that you've helped proofread my articles and sat through my presentations, without any knowledge of the field, would still be conclusive proof of your love for me.

Abstract

A new generation of Infrared (IR) camera sensors, based on MicroBolometer Arrays (MBA) has been developed. This technology is lower cost and has no need for active cooling, unlike the previous generation. It, therefore, has the potential to bring thermal cameras to new application avenues, such as thermography for quality assurance and control, automated driver assistance systems in cars and unmanned aerial aircraft systems, as well as other surveillance, security, and safety applications. Packaging of these MBAs, like most Micro-Electro-Mechanical Systems (MEMS), is challenging because these devices are sensitive and have strict requirements when it comes to processing techniques, processing temperature, and vacuum operating level. Developing a realistic and scalable packaging process for these MBAs using existing techniques and improving them, is the main goal of this thesis.

A packaging process based on CMOS fabrication techniques and Solid Liquid InterDiffusion (SLID) bonding has been developed and is presented in detail. Detailed descriptions of the processes, including photolithography for patterning and electroplating for deposition of seal frames, DRIE for micromachining the cap wafer, and a justified bonding temperature profile are presented along with common characterization techniques.

The articles included in this thesis present techniques developed to improve this packaging through specific seal frame patterns and improved anti-reflective techniques. In “Squeeze-out and bond strength of patterned CuSn SLID seal-frames” from 2022, I demonstrate that patterning of seal frames may increase their shear strength by as much as 400%, and another pattern shows a 46% reduction in squeeze-out. The strongest of the seal frames, which contained 2x50 µm wide openings inside the bond, did not appear to reduce squeeze-out, which goes against the earlier findings in the article “Investigation of seal frame geometry on Sn squeeze-out in Cu-Sn SLID bonds” from 2021. The difference in findings can be explained by the improved analysis technique; For the first article, point measurements were made, while in the second the entire seal frame area was compared. For these reasons, the findings of the 2022 article are thought to be more reliable meaning that seal frames with openings inside the bond have an insignificant impact on squeeze-out.

In “Simulated effects of wet-etched induced surface roughness on IR transmission and reflection” I use COMSOL Multiphysics to estimate that roughness in silicon as a result of

wet-etching actually improves transmission for LWIR. I later apply this phenomenon of sub-wavelength structures that improve transmission, also referred to as moth-eye structures, to produce specific structures in "Moth-eye anti-reflection structures in silicon for Long Wave IR applications". In this article, an oxide mask and an alternating isotropic-anisotropic recipe is used to produce structures that increase transmission by 5%. Simulations show that with a few alterations to the recipe, the structures could be improved to further increase the transmission by a total of ~10%. I came to the idea of implementing moth-eye structures and defined their parameters through literature review and simulation myself, and the recipe was developed with the assistance of the research group at Ginzton Laboratories, Stanford, led by Prof. Solgaard.

These moth-eye structures are intended to be patterned inside the cavity on the cap wafer. This is necessary because ~30% of LWIR light is reflected at a single air-silicon interface and the anti-reflection measures on the inside of the package must be able to survive the bonding temperature of SLID (270°C), and traditional Anti-Reflective Coatings (ARC) are generally sensitive to temperature changes due to their multiple layers. In the article "Temperature Resistant Anti-Reflective Coating for LWIR imaging on Si-wafer", however, we present an ARC capable of maintaining its anti-reflective properties after being heat-cycled to 300°C. The ARC lowers reflection by 15% and was developed using a simple 2-layer structure composed of ZnS and YF_3 and deposition at 100°C.

Through the work described above, this thesis contributes to the state-of-the-art knowledge of electronic packaging by: 1) Further developing the technique of SLID bonding. 2) Investigating the impact of silicon processing on IR transmission. 3) Investigating and describing the fabrication of novel moth-eye structures. 3) Developing an ARC with hitherto unseen application areas.

Keywords: MEMS, bolometer, wafer-level packaging, Solid Liquid Interdiffusion bonding, Transient liquid phase bonding, Anti-reflective coating, Moth-eye structures

List of papers

Article 1

Papatzacos, P. H., Akram, M. N., Bardalen, E. & Øhlckers, P. (2020). Simulated effects of wet-etched induced surface roughness on IR transmission and reflection. 2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC). Tønsberg, Norway, 2020, pp. 1-4, doi: 10.1109/ESTC48849.2020.9229821.

My contribution: Assisted in formulating the idea. Constructed the simulation and imported the AFM data to construct the Si-air interface. Analyzed the results with the assistance of supervisors. Main author.

Article 2

Papatzacos P. H., Tiwary N., Hoivik N., Nguyen H. V., Roy A., Aasmundtveit K. E. (2021). Investigation of seal frame geometry on Sn squeeze-out in Cu-Sn SLID bonds. 2021 23rd European Microelectronics and Packaging Conference & Exhibition (EMPC). Gothenburg, Sweden, 2021, pp. 1-5, Doi: 10.23919/EMPC53418.2021.9584990

My Contribution: Assisted in formulating the idea. Manufactured and tested all samples. Analyzed results with the assistance of supervisors. Main author.

Article 3

Papatzacos P. H., Nguyen H. V., Roy A., Hoivik N., Broaddus P., Øhlckers P. (2022). Squeeze-out and bond strength of patterned Cu-Sn SLID seal-frames. Microelectronics Reliability, vol. 138, Article Nr. 114692, https://doi.org/10.1016/j.microrel.2022.114692

My contribution: Developed new seal frame geometries. Manufactured and tested all samples. Upgraded IR-imaging set-up at USN. Analyzed results with the assistance of supervisors. Main author.

Article 4

Papatzacos P. H., Akram, M. N., Hector, O., Lemarquis, F., Moreau, A., Lumeau, J., Øhlckers, P. (2022). Temperature Resistant Anti-Reflective Coating for LWIR imaging on Si-wafer.Accepted by Heliyon. To be published in Volume 9, Issue 5, in May 2023, https://doi.org/10.1016/j.heliyon.2023.e15888

My contribution: Assisted in formulating the idea. FTIR measurements and thermal cycling of all samples. Analyzed results. Communication with Institute Fresnel. Main author.

Article 5

Papatzacos P. H., Broaddus P., Solgaard, O., Akram, M. N., Øhlckers P. (2022). Moth-eye anti-reflection structures in silicon for Long Wave IR applications.
Submitted to Journal of Modern Optics

My contribution: Formulated the idea. Designed structures with assistance from the Ginzton Lab research group. Constructed and performed the simulations. Assisted in sample manufacturing. Performed FTIR testing. Main author.

Article 5 is unpublished and not included in online version

Abbreviations

Abbreviation	Term
AFM	Atomic Force Microscope
ARC	Anti-reflective Coating
BCB	BenzoCycloButene
CMOS	Complementary Metal Oxide Semiconductor
CTE	Coefficient of Thermal Expansion
DRIE	Deep Reactive Ion Etching
EDS	Energy Dispersive Spectroscopy
GOPHER	Generation Of PHotonic Elements by RIE
GRIN	Graded Refractive INdex
HMM	High Melting point Metal
IMC	InterMetallic Compound
IR	InfraRed
LMM	Low Melting point Metal
LWIR	Long Wave IR
MBA	MicroBolometer Array
ME	Moth Eye
MEMS	MicroElectroMechanical Systems
PR	Photoresist
RIE	Reactive Ion Etching
RMS	Root Mean Square
ROIC	Read Out Integrated Circuit
SEM	Scanning Electron Microscopy
SLID	Solid-Liquid InterDiffusion
VOx	Vanadium Oxide

Table of Contents

Dedication I

Preface III

Acknowledgments V

Abstract VII

List of papers IX

Abbreviations XI

1 Introduction: 1

2 MEMS 2

2.1 What are MEMS?: 2

2.2 What is electronic packaging? 2

2.3 Microbolometers: 4

3 SLID 7

3.1 What is SLID bonding? 7

3.2 Why SLID bonding? 9

3.2.1 Direct bonding 10

3.2.2 Anodic bonding 11

3.2.3 Adhesive bonding 11

3.2.4 Glass frit 12

3.2.5 Thermocompression bonding 13

3.2.6 Soldering 14

4 A packaging process from preparation to characterization: 18

4.1 Wafer preparation 18

4.1.1 Cleaning: 18

4.1.2 Sputtering of seed- and adhesion layer: 18

4.1.3 Backside Alignment Marks 20

4.2 Wafer patterning 20

4.2.1 Photolithography 20

4.2.2 Electroplating 21

4.3 Pre-bond 25

4.3.1 Etching of seed- and adhesion-layers 25

4.3.2 Cavity etching by DRIE: 25

4.3.3 Deposition of anti-reflection measures: 26
4.4 Bonding 26
4.5 Characterization 28
4.5.1 Optical microscopy, grinding, and polishing 28
4.5.2 SEM & EDS 28
4.5.3 IR-microscopy 29
4.5.4 Shear testing 29
4.6 Process summary: 30

5 Fresnel reflections 32

5.1 What are Fresnel reflections and why do we care about them? 32
5.2 What is an anti-reflective coating? 34
5.3 Limitations of ARCs 35

6 Moth-eye structures 36

6.1 What are moth-eye structures? 36
6.2 Advantages of moth-eye structures 37

7 Summary of articles 38

7.1 Article 2 & 3: Patterned seal-frames for SLID and their impact on Squeeze-out and bond strength: 38
7.1.1 Introduction 38
7.1.2 Article 2: Investigation of seal frame geometry on Sn squeeze-out in Cu-Sn SLID bonds 38
7.1.3 Article 3: Squeeze-out and bond strength of patterned Cu-Sn SLID seal-frames 39
7.2 Article 1 & 5: Structures in silicon to improve LWIR transmission 40
7.2.1 Article 1: Simulated effects of wet-etched induced surface roughness on IR transmission and reflection 40
7.2.2 Article 5: Moth-eye anti-reflection structures in silicon for Long Wave IR applications 40
7.3 Article 4: Temperature Resistant Anti-Reflective Coating for LWIR imaging on Si-wafer 41

8 Conclusion 43

8.1 Outlook 45
8.2 Concluding statement 46

9 Bibliography **47**
10 Publications **57**
10.1 Article 1: 57
10.2 Article 2: 63
10.3 Article 3: 69
10.4 Article 4: 75
10.5 Article 5: 85

1 Introduction:

This work presents a summary of the work done and knowledge gained during my time as a Ph.D. candidate. In the following pages, I will first introduce and explain the concept of MEMS, before I explain why the packaging of these devices is so difficult but important. I then introduce the MEMS device which this thesis is based on, namely the microbolometer.

Next, the concept of Solid Liquid InterDiffusion bonding is explained, followed by a detailed introduction and description of the other main techniques used for bonding devices at the wafer level. The chapter also includes explanations for why each of the other techniques are unsuited, or less optimal than SLID, for our application.

In the next chapter, the packaging process developed at USN is described in detail. The reason this is done so thoroughly is that a lot of the available time for this Ph.D. I spent developing, improving, and characterizing this process.

The following two chapters describe the problem and two approaches taken by the author, namely anti-reflective coatings and moth-eye structures, to solve some of the optical problems present in this use case.

The final chapters summarize the thesis and relate the information presented to the subsequent articles published by the author.

2 MEMS

2.1 What are MEMS?:

Micro Electro- Mechanical Systems (MEMS) is a genre of components with the common factor being that they are at the micrometer-scale and use mechanical and electrical techniques to sense or manipulate the world around them. These are the building blocks of modern society [1]. When you wake up in the morning, when you drive to work, and enjoy your spare time, MEMS surround you. Whether it's the components improving the flow of information to your house by optical fibers [2], the sensors in the car that measure your tire pressure and deploys your airbag [3, 4], , or the myriad of components in your phone, such as accelerometers, gyroscopes, cameras, and microphones [5] MEMS are all but omnipresent in today's society.

The advantages of MEMS are many, but the most obvious is arguably their size. Low size, which in turn means low weight, is in itself an advantage, but it also means the devices may be applied to previously inaccessible areas, ushering in concepts such as the internet of things [6], wearable- [7] and implantable devices [8], and even smart dust [9]. Decreased size also means shorter distances, and smaller areas needed to move, heat, or cool, which in turn means lower power consumption [10, 11]. The last advantage, which I will return to later, is that these more advanced devices, often end up costing less than their bulkier predecessors.

2.2 What is electronic packaging?

Electronic packaging is, as the name suggests, the method by which the electronics are packaged and protected from the environment. While this may seem simple, packaging is arguably one of the most important parts of electronics design and production, because it controls the system's electrical performance, cost, size, and reliability [1]. This is because the packaging not only provides protection from the environment - be it mechanical, electrical, or chemical - but also provides thermal management as well as physical and/or electrical contact with the rest of the system [1, 12]. The large variety in materials – like epoxies [13, 14], metals [15, 16], and glass [17, 18] - different techniques – like thermocompression [19], anodic bonding [17], molding [13, 14] etc. - and tools used - like lasers [20], wire bonders [21], simulation [22, 23], etc. - also make packaging a highly cross-disciplinary field.

Packaging of MEMS devices introduces even more considerations. These devices are generally fragile and need non-electrical feed-throughs – such as a transparent casing [24] - to interact with the environment [12]. They also often require a cavity within the package and special considerations during processing [25], both of which further complicate the design of a packaging process. Due to the large variation in MEMS, there are also few standardized packaging procedures, which means packaging must often be tailored to the device, increasing the costs even further [26].

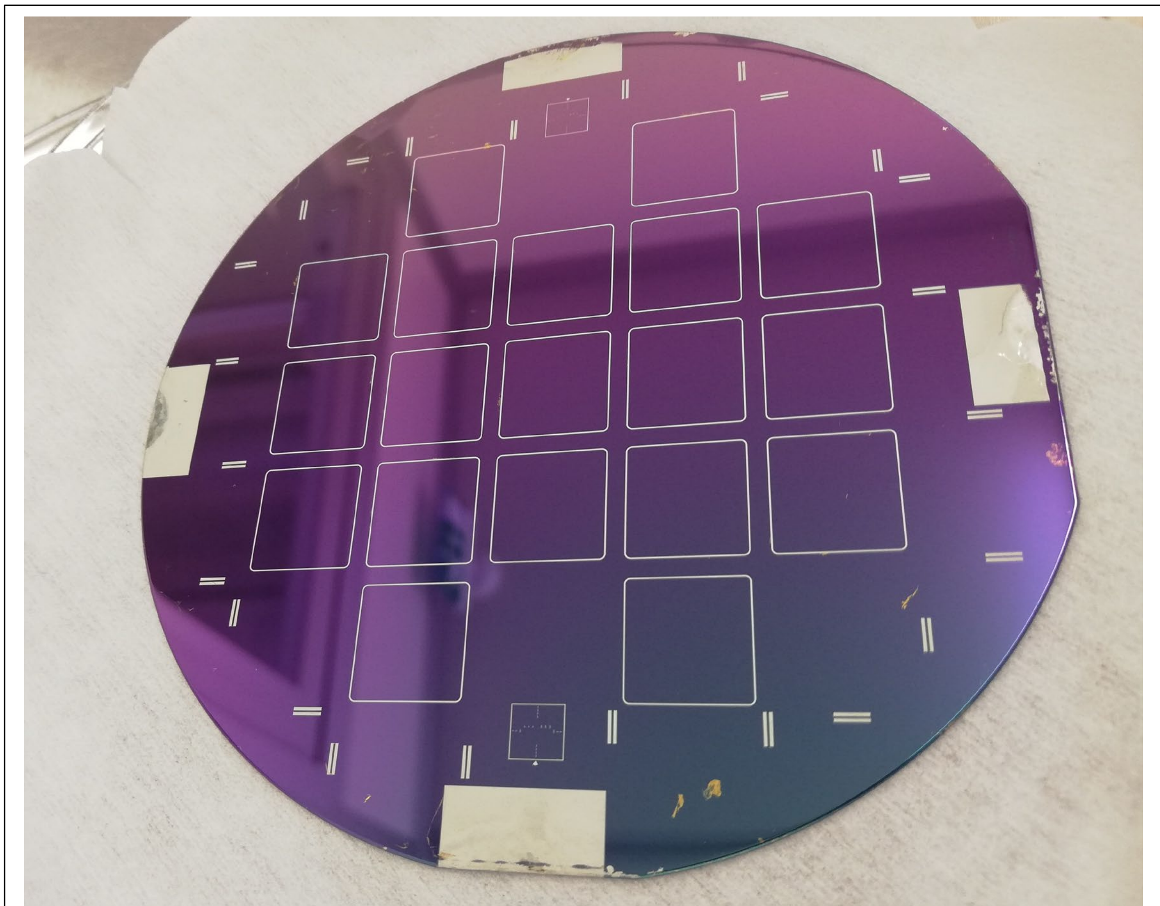

Figure 1: 100 mm diameter silicon wafer with electroplated Cu and Sn Seal frames, alignment marks, and connection points.

A central way of reducing the aforementioned cost is wafer-level packaging. Silicon, which is the main constituent of most MEMS, is generally produced and delivered in wafer form. The MEMS are then, in most cases, made by subjecting the entire wafer to each treatment simultaneously - be it doping, photolithography, or etching [1]. This allows for the manufacturing of several components in parallel, often at little to no extra cost, which is one of

the great advantages of micro- and nanotechnology because it allows for very high-volume manufacturing. Since the devices are at the micro-scale, the amount of material required is very little, which means a high production volume allows for advanced devices to be manufactured at low cost [3, 5, 10, 11].

When the MEMS device is finalized, they are conventionally separated into single devices and then packaged individually. The advantage of this so-called chip-level packaging – as opposed to wafer-level packaging – is that singularized chips can be tested. This means that only the chips that are known to work, commonly referred to as known-good die, are packaged [27]. It is also comparatively simple and easy to package a single chip. Wafer-level packaging, on the other hand, may drastically lower the cost of one of the priciest processes by performing it in parallel on the entire wafer provided the process has a high yield with few faulty chips [28, 29]. Hence the term - and attractiveness of - wafer-level packaging.

2.3 Microbolometers:

I have spoken of MEMS in the abstract, but a specific example – which happens to be the device the author has been working with in this thesis – is a microbolometer. A bolometer is accurately defined by Merriam-Webster's dictionary as "a very sensitive thermometer whose electrical resistance varies with temperature and which is used in the detection and measurement of feeble thermal radiation and is especially adapted to the study of infrared spectra" [30]. Microbolometers for thermal cameras are generally in the shape of a membrane on legs (see Figure 2) and made from a material with a high-temperature coefficient of resistance, usually amorphous silicon or vanadium oxide (VOx) [31-33].

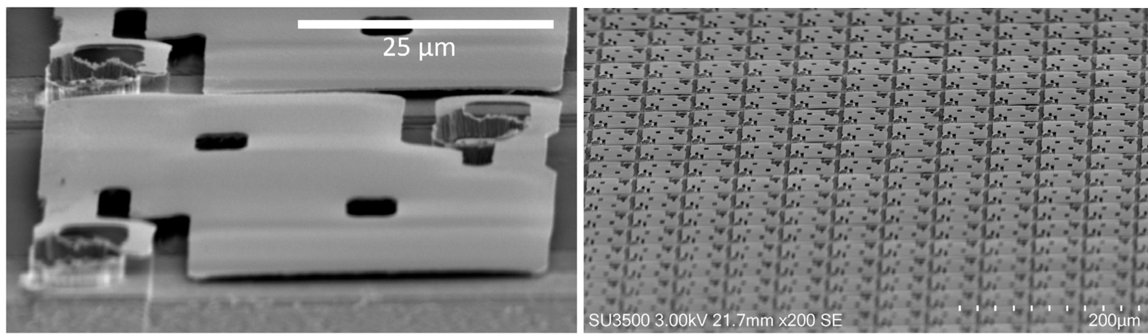

Figure 2: A single bolometer (left) and a bolometer array (right). Reproduced with permission from [33] (MPDI).

The microbolometers sense temperature by letting incoming IR radiation hit the membrane, which causes an increase in temperature, which in turn causes an increase in resistance [34]. This increase in resistance is then translated into an electrical signal. When placed in an array, each microbolometer functions as a pixel and the result is a thermal camera. These thermal cameras are promising because their competitor, the more sensitive photon IR detectors, are large, bulky, and require active cooling, often to cryogenic temperatures [31, 32]. This new generation of low-cost, uncooled microbolometer-based thermal cameras have the potential to open up new and exciting applications in areas like driver assistance[35, 36], medicine [37], and surveillance – both of machine condition and against trespassers [38, 39] - to mention a few (See Figure 3).

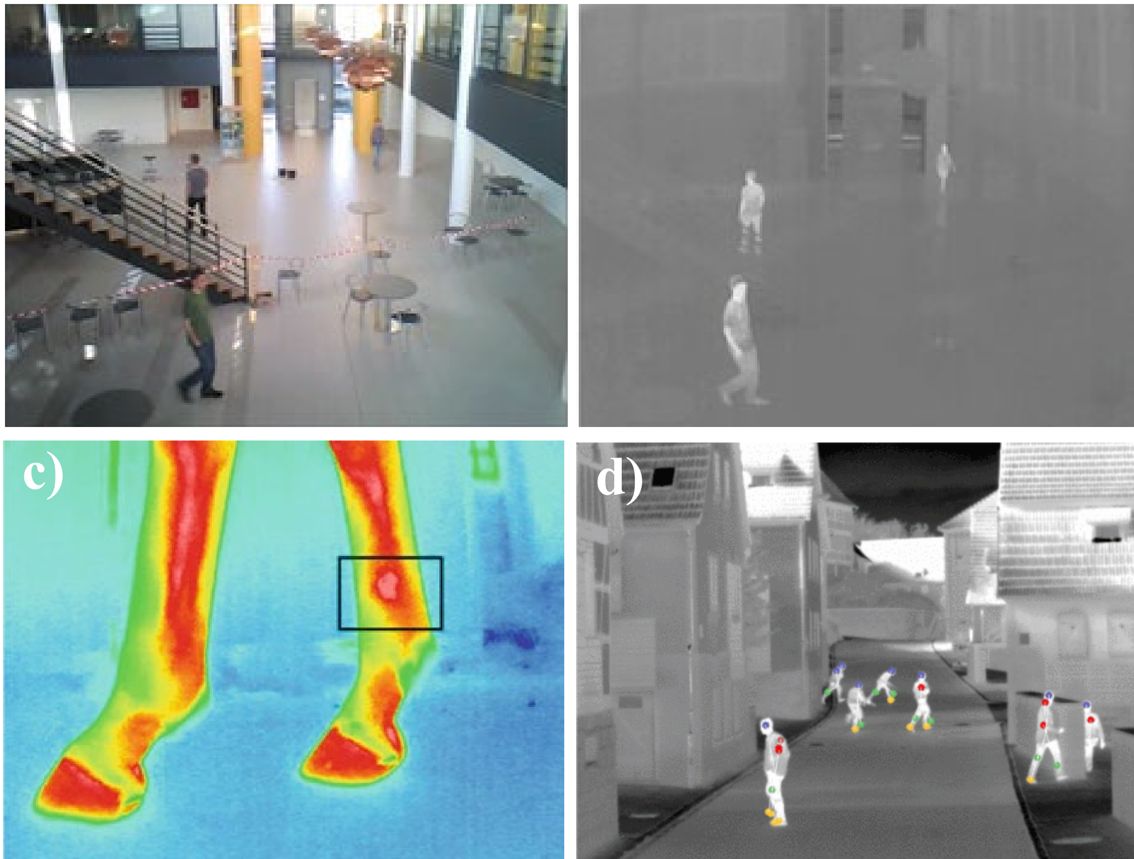

Figure 3: Image of the same scene using visible light- (a) and thermal camera (b). Thermal camera reveals inflammation in the leg of a horse (c). Machine learning system identifying pedestrians using a thermal camera (d). Images a-c from [38] and image d from [35] (all images reproduced with permission from SNCSC).

The main reason thermal cameras have not reached the wide adoption mentioned above is that price is still a limiting factor [40]. As mentioned in the electronic packaging section, the packaging of MEMS is often challenging and expensive, and microbolometers are no exception. For microbolometers to function well, the bolometers' thermal coupling to their surroundings needs to be limited. This is because the bolometer should ideally be affected by incoming radiation only [41]. A low internal pressure, therefore, translates to a camera with high sensitivity and low noise [34]. Developing a packaging process to encase the delicate bolometer in a way that can maintain this low-pressure environment for a long time, while letting the LWIR radiation in, was the motivation for this thesis.

3 SLID

3.1 What is SLID bonding?

Solid Liquid Interdiffusion (SLID) bonding is a technique wherein two surfaces are joined by using a low melting point metal (LMM) and a high melting point metal (HMM) and a bonding temperature between the two melting points. Bonding is achieved by pressing the two surfaces together using a moderate force and heating the joint above the melting point of the LMM. This causes the LMM to melt, which wets the two surfaces and accelerates the growth of InterMetallic Compounds (IMC). After some time, the LMM is fully consumed, leaving a solid bond consisting only of IMCs and the HMM, all of which have a melting point much higher than the LMM. The technique was first described by Leonard Bernstein in 1966 using the metal systems Ag-In, Au-In, and Cu-In [42], but in later years, Cu-Sn has become the most popular metal system to use for SLID, in part due to its low price and long history of use in the electronics industry. It also forms strong bonds and has a rather simple phase diagram, both of which increase its attractiveness in applications.

I have described an entire SLID process from preparation to characterization in Chapter 4, but what generally happens in a CuSn SLID bond, is that an alternating layer of Cu, Sn, and Cu (see Figure 4 a) is deposited and heated beyond the melting temperature of Sn, which is 232°C. As the temperature is rising, solid-state diffusion occurs and Cu and Sn start interdiffusing which results in the initial formation of the Cu_6Sn_5 phase (see Figure 4 b). When the melting point of Sn is reached, Sn liquefies and dissolves Cu at both surfaces (see Figure 4 d). Although bonding by solid-state diffusion is possible, solid-liquid interdiffusion is generally faster than its solid-state counterpart [43]. The presence of the liquid phase will also drastically reduce the

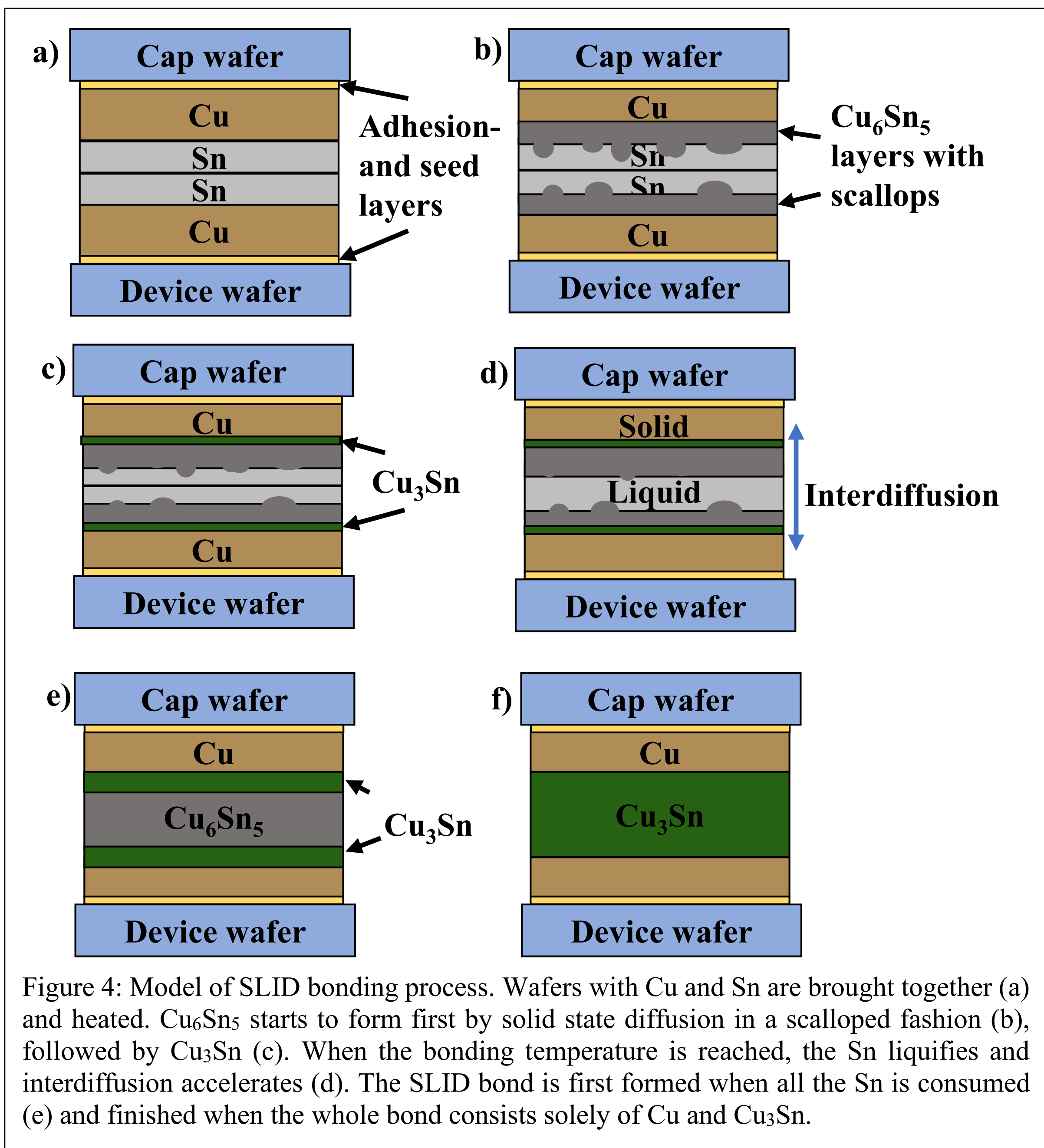

Figure 4: Model of SLID bonding process. Wafers with Cu and Sn are brought together (a) and heated. Cu_6Sn_5 starts to form first by solid state diffusion in a scalloped fashion (b), followed by Cu_3Sn (c). When the bonding temperature is reached, the Sn liquifies and interdiffusion accelerates (d). The SLID bond is first formed when all the Sn is consumed (e) and finished when the whole bond consists solely of Cu and Cu_3Sn.

demands for how flat the mating partners need to be. Cu will be allowed to continue to diffuse into Sn until all the Sn is consumed, which marks the earliest point at which the bond has been formed (see Figure 4 e).

Given enough time and Cu, the bond will continue to develop until all the Sn and Cu_6Sn_5 have been consumed into Cu_3Sn (see Figure 4 f). Wiel et al. make a convincing case for why a full conversion to Cu_3Sn is generally the target: “The Young’s modulus of Cu_6Sn_5 is 96GPa, which is lower than the Young’s modulus of Cu_3Sn of 106–123GPa. Moreover, Cu_6Sn_5 is "more brittle" than Cu_3Sn; the fracture toughness of Cu_6Sn_5 is 2.7MPa√m, whereas the fracture toughness of Cu_3Sn is 5.7MPa√m, which is more than two times higher. Moreover, Cu_6Sn_5 is almost as susceptible to corrosion as Cu, whereas Cu_3Sn is practically inert against corrosion. The melting temperature of Cu_6Sn_5 is 415°C, which is significantly lower than the melting point of Cu_3Sn. As a result, the thermal stability of the bond is negatively affected. This is an important drawback. Finally, a system comprised of surplus Cu in combination with Cu_6Sn_5 will tend to convert into a system with Cu_3Sn and thus would be a system with gradually changing material properties. The prediction of the reliability for these bonds would be extremely challenging.” [44]

3.2 Why SLID bonding?

Now that we have explained the concept of SLID, it is prudent to ask why this technique was chosen, considering the multitude of bonding options out there. The most common methods for wafer bonding are [29, 45]: Direct bonding (also known as fusion bonding), anodic bonding, glass frit bonding, thermocompressive bonding, bonding using adhesives, and soldering. In this chapter, we will briefly describe each technique and explain why SLID is the best choice for our application. The results are summarized in Table 1 at the end of the chapter.

3.2.1 Direct bonding

Direct bonding is a technique of joining two extremely flat surfaces with extremely low surface roughness together permanently using mostly Van der Waals forces and hydrogen bonds. The concept of joining two such extremely flat surfaces together was described by Galileo Galilei, but dates even further back [46]. This technique does not use an intermediate layer and is a common technique for joining silicon with a long history and high implementation in manufacturing [29, 46]. A common direct bonding process between two silicon wafers is shown in Figure 5 [46]. In it, we first see two mirror-polished wafers placed in a micro-cleanroom (a). They are then separated by spacers and cleaned thoroughly using deionized particle-free water (b). The application of micro-cleanrooms and thorough cleaning is usually necessary as even small particles or contaminations will cause large unbonded areas. For example, a particle of diameter 0.5 mm trapped between two 4” silicon wafers each with a thickness of 525 mm will yield an unbonded area of approximately 0.5 cm radius [47]. The wafers are then dried by spinning, possibly aided by IR radiation, before the spacers are removed. If the bonding is performed in air, the wafers usually float on a small air cushion at this point. Bonding is then usually initiated by a single pressure point. The bonding then self-propagates until the whole wafer is bonded.

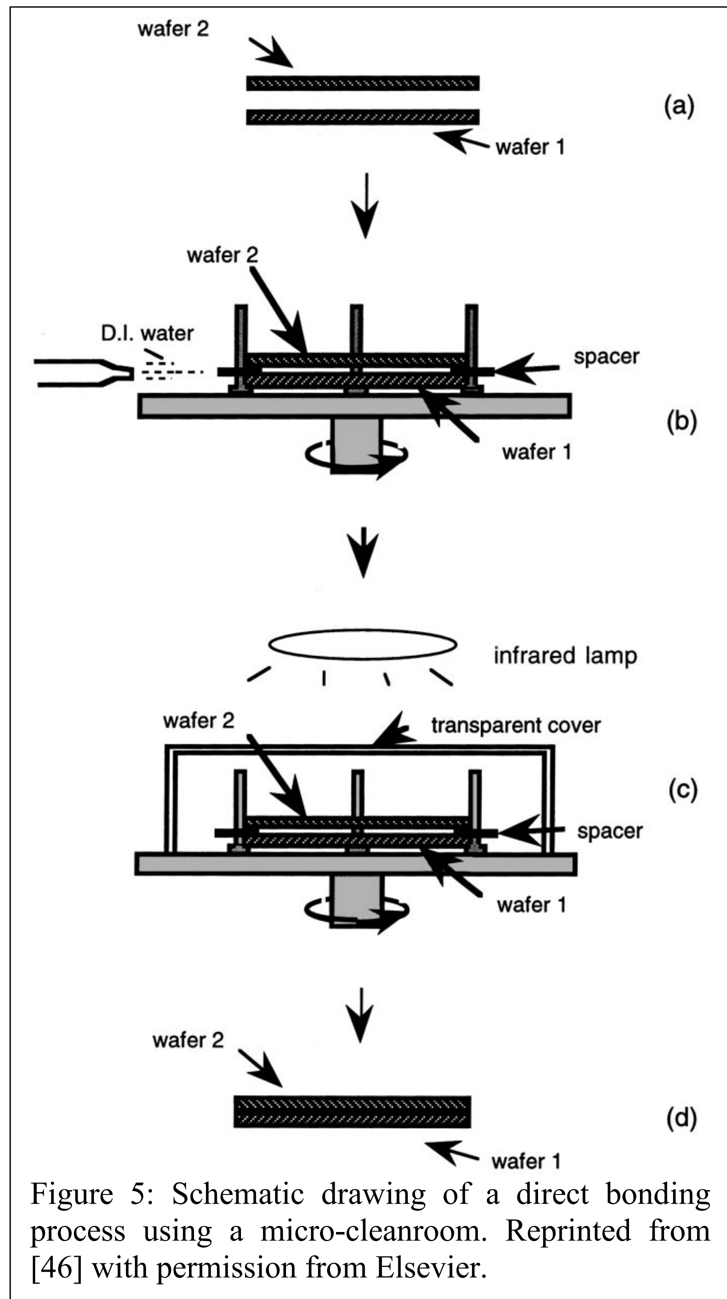

Figure 5: Schematic drawing of a direct bonding process using a micro-cleanroom. Reprinted from [46] with permission from Elsevier.

At this point, the bond is reversible, meaning the bond can be broken and reattached. This is because the bond strength is lower than the cohesive strength, which is the strength with which the bulk material holds itself together. To make the bond permanent, it is very common to heat it. Especially for silicon, this is an advantage because the heating converts the weak hydrogen bonds into strong covalent Si-O bonds [46]. This is commonly done in the 400°C-1000°C range for a couple of hours, but many techniques are being investigated to potentially lower both the time and temperature necessary to finalize the bond. Sayah et. al. for example managed to bond irreversibly in the 100-200°C range, by using a high bonding pressure (up to 50MPa) [48]. Ultimately, however, the technique is limited because it relies so heavily on flatness. This means that it has very strict limitations when it comes to processing, to avoid roughening of the surface, and high demands for cleaning, to avoid particulates. While it could be possible to develop a recipe with a bonding time, -temperature, and -pressure that our device and ROIC could handle, it is not feasible that a satisfactory cleaning and polishing process could be.

3.2.2 Anodic bonding

Anodic bonding is a bonding technique in which two wafers, most commonly Pyrex and silicon, are bonded together, without an intermediate layer. The bond is formed by heating the sodium-containing glass, e.g. Pyrex, until it is a sufficiently good conductor and then applying an electric field, which causes the charged sodium ions to move away from the bonding interfaces, creating large electrostatic forces [49, 50]. The technique creates strong hermetic bonds (10-15MPa) in a rather short time (15 min for a patterned 100mm wafer) and is a well-established wafer bonding technique first described as early as 1969 [50]. It is, however, limited by the required presence of sodium, high requirements for flatness (<0.05µm RMS), and the high processing temperatures and voltages, typically 300-500°C and 100-1500V [49]. These limitations mean it is not CMOS compatible, which in turn means it’s not suitable for our applications since the ROIC connected to the MBA is a CMOS device.

3.2.3 Adhesive bonding

Adhesive bonding simply means using an adhesive, generally consisting of a polymer, to bond wafers together [51]. It requires low bonding temperatures, has a very low sensitivity to surface topology, and it is compatible with most materials, including CMOS technology, but is also simple and low-cost. In a wafer bonding setting, the adhesive polymer is usually applied to one

or both wafers before they are brought together, and pressure is applied. The adhesive is then cured or hardened, most commonly using heat or ultraviolet light [51].

The reason this technique is not considered for our application is the fact that this technique does not provide seals that are sufficiently gas-tight. In fact: "Organic polymers such as fluorocarbons, epoxies, and silicones are a few orders of magnitude more permeable to gasses than glasses, ceramics or metals.". [52] Chowdhury et al. claimed in 2022 to be making "[…] vacuum-sealed insulated polymeric cavities on a silicon substrate […]" using benzocyclobutene (BCB), but present no evidence for their cavities being vacuum-sealed [53]. The reason for this might be found in Oberhammer et al. article from 2003 where they conclude that: "Helium leakage tests of cavities created by selective bonding have shown that BCB is not hermetic enough to provide sufficient gas tightness for MEMS applications with a strictly controlled atmosphere and does not sufficiently withstand moisture penetration for use in various MEMS and electronic applications" [52].

3.2.4 Glass frit

Glass frit is a technique that uses glass with a low melting point to bond two substrates. The glass comes in the form of a paste which is usually deposited by screen printing, consisting of glass particles, organic binders, and solvents [54]. Screen printing is a technique in which a stencil is placed above the wafer and then flooded with the paste. The stencil with the paste is then pressed onto the wafer with a squeegee, which then forces the paste into the open areas of the stencil (see Figure 6) [29].

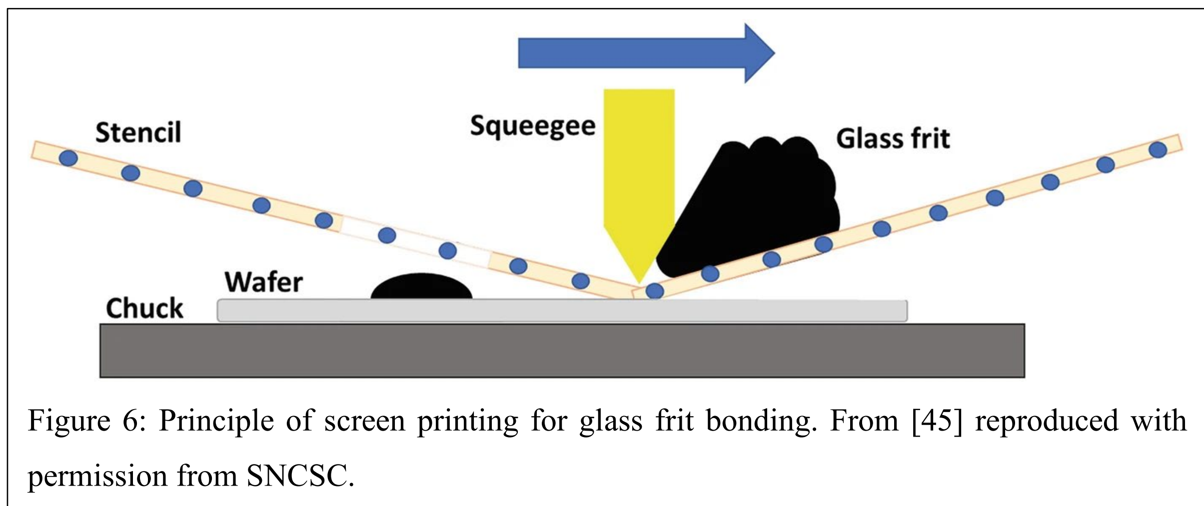

Figure 6: Principle of screen printing for glass frit bonding. From [45] reproduced with permission from SNCSC.

After the glass is deposited, but before bonding, an extra heating step is performed, usually referred to as pre-sintering. This heating is done to remove the binders and solvents in the paste and leaves pre-melted glass particles and is generally performed in the range of 320°C to 510°C [18, 54]. The wafers are then brought together with a moderate force and heated above the melting temperature of the glass, which is generally above 120°C [18, 54]. The result is a hermetic bond with the material properties of glass.

Glass frit is a technique that uses uncomplicated tools and common materials to create hermetic seals. The presence of a liquid state also means there are low requirements when it comes to surface roughness. The use of such uncomplicated tools as screen printing is, unfortunately, also one of its limitations, since it limits the width of structures to 150-300µm [29, 54]. The use of solvents also means it is also not particularly suited to vacuum packaging. While the bonds have excellent hermeticity, outgassing during the bonding means there is a limit to how low pressure one can achieve inside the package [55, 56].

3.2.5 Thermocompression bonding

Thermocompression bonding is the act of joining two mating partners, almost exclusively metals, by applying a sufficiently high heat and pressure. The bond is formed by solid-state diffusion, meaning there is no liquid phase, and the topology requirements are overcome by a high bond pressure [29]. For this reason, gold is preferred, since it has a low yield point, meaning it deforms easily [57]. Cu and Al are also common materials used in thermocompression bonding [45]. The advantages of the technique are that it is comparatively

simple, and the bond has all the advantages of the bulk metal, i.e. high strength, high-temperature resistance, and high hermeticity.

While the temperature necessary for this technique (300-450°C [45]) is CMOS compatible, the high pressures (10-15GPa [45]) would be challenging to accommodate for our application. To protect the micromachined cap and ROIC wafers, extra steps would be required, which increases complexity and manufacturing cost. Although some have reported bonding with as little as 200kPa [19], a surface roughness requirement of <1nm is stated in the article. At this point, it is arguable whether we are dealing with fusion bonding or if this is an edge case of thermocompression bonding. Regardless, the polishing steps required to achieve surface roughness this low, are not compatible with our process.

3.2.6 Soldering

There is evidence that humans have been using soldering as a technique to join metals far back as Egypt and ancient Mesopotamia [58]. It is the predominant joining technique in electronic packaging and is defined as a process that uses filler metal, also referred to as solder, with a melting temperature lower than 450°C [59]. Soldering is simple to do, makes strong bonds, has large tolerances when it comes to cleanliness, surface topography and temperatures, and can be done with a variety of materials [60]. All these factors have likely contributed to its long history of use and industrial dominance. In the last century, however, the fact that soldering can produce highly conductive bonds at relatively small pitches (>100µm [29]), and at CMOS-compatible temperatures, have been the main reasons for its wide adoption in the electronics industry.

Soldering is quite similar to SLID in many ways [29]. The most common metal system is Cu and Sn and the bonding temperatures are similar for similar reasons; the joining metal is supposed to melt, and the mating partners are not. They are, however, very different in some important ways.

If a bonded solder joint is reheated it will once again liquify. While this means that such bonds and devices can be more easily repaired, it also means that if we want to bond a device that has solder bonds already present, those bonds and seals will also melt, thus potentially destroying the device [42, 61].

Since soldering also uses Cu and Sn and heats the materials to similar temperatures as SLID, IMCs will form in a solder bond as they would in SLID. The difference, however, is that since the bond is heated for a shorter time and with a much higher amount of Sn, the bond will not completely solidify into IMCs as it would in a SLID process. As the size of these joints keeps shrinking to accommodate finer pitches it is expected that soldering will approach SLID in the future [61, 62] (see Figure 7).

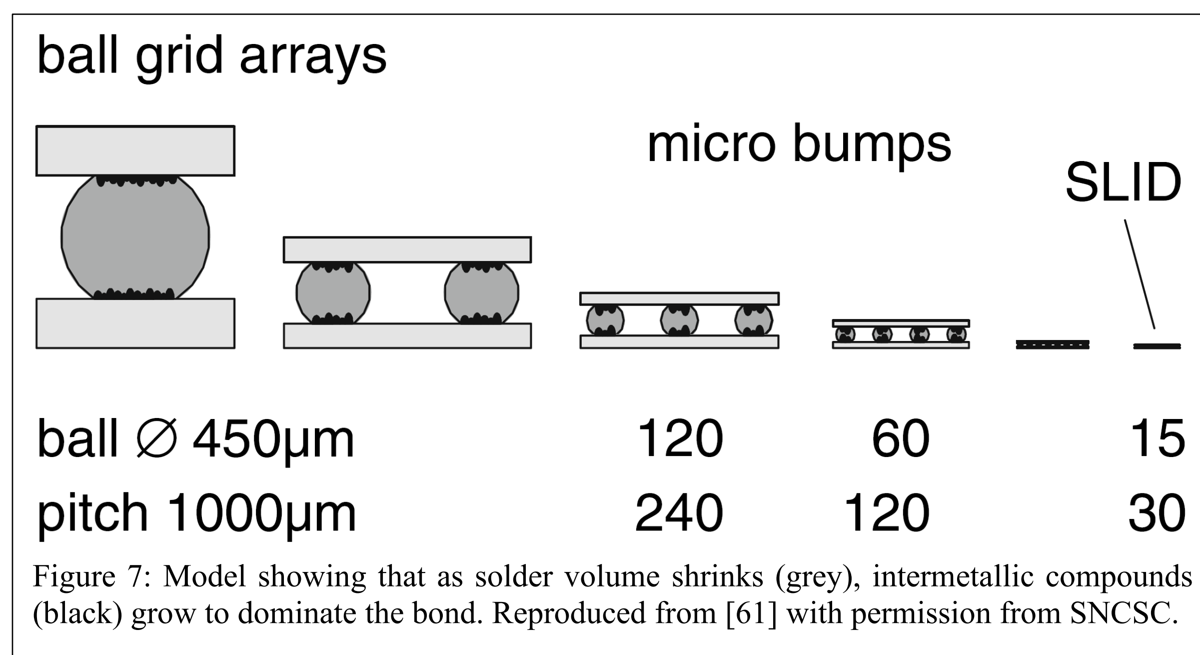

Figure 7: Model showing that as solder volume shrinks (grey), intermetallic compounds (black) grow to dominate the bond. Reproduced from [61] with permission from SNCSC.

Another important difference between soldering and SLID is the use of flux. The purpose of flux is to make sure the liquid solder flows to, and is in direct contact with, as much of the base material as possible. This is referred to as proper wetting, and it does this by removing contaminants and oxides, and stopping further oxides from forming [59, 63]. Because flux is a liquid, and it must be applied just before bonding, soldering is not optimal for our application. The delicate bolometers cannot survive wet processing. They will be protected for much of the other processes (similar to [64] where they've used a sacrificial layer of silicon dioxide which is removed by HF), but the bolometers must, understandably, be free and ready to operate before they are bonded. While wafer-level packaging [65] and high-quality vacuum packaging [66] have been achieved with flux-free soldering, these processes require specialized solders and sophisticated equipment, both of which increase the packaging cost [63].

Table 1: Overview of most common wafer-level bonding techniques with a brief description and explanation for exclusion.

Bonding technique	**Brief description**	**Exclusion criteria**
Direct bonding	Two very flat or plastic surfaces are placed together and bonded by Van der Waals forces and hydrogen bonds. Heating this bond creates bonds with the same properties as the bulk materials.	Very high requirements on surface flatness [47].
Anodic bonding	Sodium-containing glass is bonded to silicon by applying a high voltage to move charged sodium ions away from the bond interface, creating a strong electrostatic bond in a relatively short time, with no intermediate layer.	The presence of sodium, high temperatures, and high voltages are not compatible with CMOS devices [49].
Adhesive bonding	Substrates are “glued” together with a polymer which is then cured by heat or UV.	Not hermetic [52].
Glass frit	Glass with a low melting point is deposited as a paste with screen printing. The bond is then pre-heated to remove solvents before	Large bond frames [29, 54]. Not compatible with high vacuum packages, because of outgassing [55, 56].

	being brought to the glass melting point for bonding.	
Thermocompression	High pressure (10-15GPa) and temperature (300-450°C) is used to join two metal surfaces.	Requires high pressure [45] and/or low surface roughness [19].
Soldering	A filler metal with a melting temperature lower than 450°C is used as an intermediate layer to make conductive and hermetic bonds.	Flux is required for low-cost applications [59, 63]. The seal does not survive re-heating [42, 61].

4 A packaging process from preparation to characterization:

In this section, we will follow a silicon wafer from its arrival in our lab, all the way until a package is fully sealed, and the following characterization. This section describes in detail the full SLID process as it has been developed and refined at USN. It is a result of an extensive literature review by the Ph.D. candidate and extensive experimental work in cooperation with colleagues and lab engineers at USN.

4.1 Wafer preparation

4.1.1 Cleaning:

When the wafer arrives, it is generally clean and carefully packaged, which means it should be able to be moved into the cleanroom and used directly. A cleaning step is recommended regardless. At USN, cleaning generally consists of washing the wafer with acetone, followed by isopropanol, before rinsing the wafer with de-ionized water and dried with nitrogen.

When the wafer is thoroughly washed and dried, it is common to subject the wafer to a plasma cleaning step. This is especially common between processes, since the wafer will have been subjected to multiple sources of possible contaminants, in the form of moving around in the lab and using the machines therein. The plasma cleaner uses electrons and a magnetic field alternating at high frequencies to excite electrons inside the chamber, which creates charged ions [67]. The resulting substance is called plasma and is one of the four states of the universe, along with solid, liquid, and gas. The actual cleaning takes place when the aforementioned plasma is accelerated towards the specimen by a high voltage. This leads to heating, sputtering, and etching of the specimen, all of which contribute to the removal of unwanted contaminants [68]. An example of a plasma cleaning recipe at USN would be 10 minutes at 200 W of power and 100 sccm oxygen and 100 sccm argon with an Alpha Plasma Cleaner PPS.

4.1.2 Sputtering of seed- and adhesion layer:

Clean silicon and the material we want to use in the bonding process, namely Cu, does not stick well together. Silicon is also not a good starting point for electroplating, which is the method

we want to use for the deposition of Cu. This means that an adhesion and/or a seed layer is required.

Because these layers need to be thin, have good adhesion, and have low roughness, sputtering was chosen as the deposition process for these layers. This is a deposition technique that uses many of the same principles as the plasma cleaner described in the previous section. Plasma is generated and accelerated towards a crucible containing the material to be deposited, but because the energies are much higher in this case, the sputtering effect is more dominant. Sputtering means that atoms are knocked-lose from the target, and these atoms are then free to deposit on other surfaces, such as a nearby silicon wafer [69].

The main purpose of an adhesion layer is to keep the bond attached to the substrate. However, in most of the experimental observations made by the author, as well as in several of the articles where bond strength is studied, the place where the SLID bond fails is typically at the interface between the substrate and the adhesion layer [16, 70-73]. Since these articles all use the same adhesion layer, namely TiW, and the bond strengths for these samples are not atypical, two important inferences may be drawn from this: 1) A bond is only as strong as its weakest point and 2) proper deposition of an adhesion layer is important and difficult.

Achieving proper adhesion in the lab at USN also proved difficult. Early samples, if joined together at all, did not make it to the machine designed to test bond strength (see Chapter 4.5.4 shear testing). After several attempts at improving adhesion by lowering the deposition rate, pre-depositing the material intended to be sputtered on a dummy sample, cleaning the sample chamber, and booking the chamber for long periods of time to avoid other users, the decision was made to outsource the deposition of the adhesion and seed layer to external partners. Much higher bond strengths were achieved after this. The reason we could not achieve good adhesion at USN was not discovered, but the large amounts of users with varying degrees of competence, and the large number of materials available for use, remain likely sources of contamination.

If the intention is to deposit the metal system by electroplating, as is most common, a seed layer is also considered a necessity. The goal of this layer is to provide a conduction path for the current, which drives the electroplating process, as well as provide nucleation points for the metal growth [74]. While Cu and Au would both do this job adequately, Cu oxidizes quickly and continuously in ambient environments. Au is more expensive, but does not oxidize, and is,

therefore, more practical in an experimental setting. A recipe that provided good, if unreliable results at USN with an AJA 4050 sputterer, was: For TiW: 25 W power, and 9 sccm of Argon, resulting in a deposition rate of 0.14 Å/s until a thickness of 100 nm. For Au: 15 W power and 12 sccm of Argon, resulting in a deposition rate of 0.22 Å/s until 100 nm. Backside alignment marks

4.1.3 Backside Alignment Marks

The final step in wafer preparation is the patterning of the backside marks. This is done by a combination of photolithography and deep reactive ion etching (DRIE) and is only necessary to do on one of the wafers in the wafer pair. The point of these marks is to: 1) Use as guidelines to align the two wafers we intend to join before bonding them. 2) Use as guidelines when splitting the wafer into chips after the bonding has been performed. For these applications, the built-in microscope in both the wafer aligner and the dicing machine was unable to distinguish the etched markings from the surrounding untreated silicon as both showed the same level of surface roughness and the poor depth perception in the cameras. When swapping, to double-side polished silicon wafers, the contrast between treated and untreated silicon became much clearer and could be perceived in the built-in microscope. The process of photolithography and DRIE is further explained in the next section.

4.2 Wafer patterning

4.2.1 Photolithography

Photolithography is a technique for accurate patterning and realization of very small structures and is considered a cornerstone in a lot of MEMS production and development. The technique uses a chemical called photoresist (PR) which is coated on the specimen to be patterned and then exposed to UV light through a mask. Depending on the type of photoresist, either the exposed areas or the unexposed areas will be removed by a developing solution, leaving a 2D pattern in the resist, either identical to the mask or inverted [45].

The process of photolithography has quite a few variations depending on the application, but our recipe is as follows: After a thorough cleaning of the wafer, the wafer is coated in photoresist. We do this by placing the wafer on a spin coater and pouring the appropriate

photoresist in the middle of the wafer. The wafer is then spun according to a preprogrammed recipe, which results in the photoresist being evenly coated at a predictable thickness. Before electroplating, a two-step program of 2000 rpm and 2500 rpm at 30 s each with an acceleration rate of 1000 rpm/s^2 resulted in an even, 5.8 µm thick layer. The photoresist used for this work is AZ4562 which is a positive resist designed to be used in the 4.5 µm – 30 µm range and with optimized adhesion for compatibility with plating and wet etching processes (https://www.microchemicals.com/products/photoresists/az_4562.html). The tool used for the spin-on step was a Spin 150i Spinner.

4.2.2 Electroplating

The next step is to deposit a layer of Cu and Sn. Electroplating is the most scalable way to deposit layers of sufficient thickness (1-5µm) in the correct areas at the required pitches, which is why it is the most common approach. The process of electroplating is several centuries old and the general working principle is as follows: "Metal salts dissolved in an aqueous solution are reduced by a circuit current of electricity that is passed between two electrodes immersed in the solution. The negative electrode (cathode), has the metal plated onto it while the positive electrode (anode), dissolves into the solution (the electrolyte), replenishing the metal ions in solution." [75].

Electroplating of the Cu and the subsequent Sn layer is arguably the most challenging part of CuSn SLID bonding. Achieving two Cu surfaces with high uniformity and a low amount of impurities has been demonstrated to be very important factors. Several articles explicitly describe problems in achieving satisfactory electroplating results [76-78] or specifically name electroplating impurities as the root cause of voiding [79-81]. The most important parameters to achieve metal layers suitable for SLID bonding are current density/-distribution and the electroplating solution. Because Sn will melt and flow during the bonding process, Sn uniformity and distribution are not as crucial.

Part of what makes Cu plating difficult, is the number of parameters affecting the process and their interdependence. While current density can be easily calculated, the actual current distribution of the sample will vary with the pattern of the mask [82, 83]. The electroplating solution does not only contain different additives, some of which may be proprietary, but it will also deteriorate over time and use [76]. What current density is appropriate is also dependent

on what electroplating solution you use, and different baths with different circulation, anode-cathode-distance, -geometry, -orientation, and bath temperature are all likely to result in metal films with different characteristics when it comes to e.g. purity and topography.

Despite these issues, some factors seem common for successful bonds. Both 10mA/cm^2 [82-84] and 5mA/cm^2 [73, 80, 85] have been reported to create metal layers with satisfying uniformity for bonding. No exact uniformity requirement has been stated so far, but Suni et al. report 10% uniformity on a 6μm layer of Cu as causing unsuccessful bonds and 5% leading to successful ones [76]. Chang et al. report successful bonds with a height variation of less than 10% on a 4μm thick layer of Cu [86]. Kannojia et al. performed experiments with varying current densities and observed that a higher current density caused a much rougher surface, than lower current densities (50mA/cm^2 caused surface roughness of 300nm and peak-to-valley roughness of 2100nm. 5mA/cm^2 caused surface roughness of 60nm and peak-to-valley roughness of 400nm). This increased surface roughness reportedly caused voids as a result of the difference in the area available for diffusion at peaks compared to valleys [85]. An alternative approach is demonstrated by Menager et al., where extra Cu is deposited for the express purpose of polishing it until a satisfactory roughness is achieved [84]. Some surface roughness is considered advantageous to improve wetting according to Wenzel's equation [87], but high surface roughness means more Sn is required, which leads to more squeeze-out (see [16] for more details on squeeze-out). Poor uniformity also hinders the proper distribution of the bonding pressure.

The thickness requirements of the Cu layer can somewhat depend on how thick the final bond needs to be, but the ratio of Cu to Sn should be above 1.31 if the target is a full conversion into Cu_3Sn [23, 88]. A surplus of Cu is also recommended because: (i) Consuming all the Cu may jeopardize the adhesion between Cu and the seed and/or adhesion layer [23], (ii) to allow for process variations, and (iii) to improve the ductility of the overall bond, since pure Cu is more ductile than the IMCs [89]. A Cu thickness of approximately 3 μm was utilized for most of the SLID bonds made at USN.

The target thickness of Sn is highly dependent on the temperature profile of the bonding process. The thickness of Sn must exceed that which is consumed through solid-state diffusion during ramping to the target temperature. If there is no pure Sn left when the melting point is

reached, no liquid is formed, and the two surfaces will not be mated. A too-thick layer of Sn, on the other hand, will lead to unnecessarily long bonding times and squeeze-out of the excess Sn. Squeezed-out metal tends to form droplets extending past the intended bond area. These droplets have the potential to destroy MEMS devices and/or short-circuit electronics if the squeeze-out extends far enough. If the squeeze-out is not severe enough to affect the device immediately, the weakly adhered droplets may still get knocked loose, meaning the device may pass initial testing, but fail critically during operation [90].

The growth of the initial IMC, Cu_6Sn_5, is not planar, but scalloped, as seen in Figure 4 and 8 [91]. This means that the Cu_6Sn_5 may reach the other side and act as both a spacer and diffusion barrier to Sn islands as seen in Figure 8 b. Since there is a volume contraction as Cu and Sn convert to Cu_6Sn_5 of 10%, and a further 8% shrinkage as it converts from Cu_6Sn5 to Cu_3Sn [92], this means that these spacers and diffusion barriers may lead to voids if there is insufficient Sn for the IMCs to grow together [91, 93-95]. A 2 μm thick Sn layer was utilized at USN, which was thick enough to compensate for roughness and scalloping, and only resulted in moderate squeeze-out.

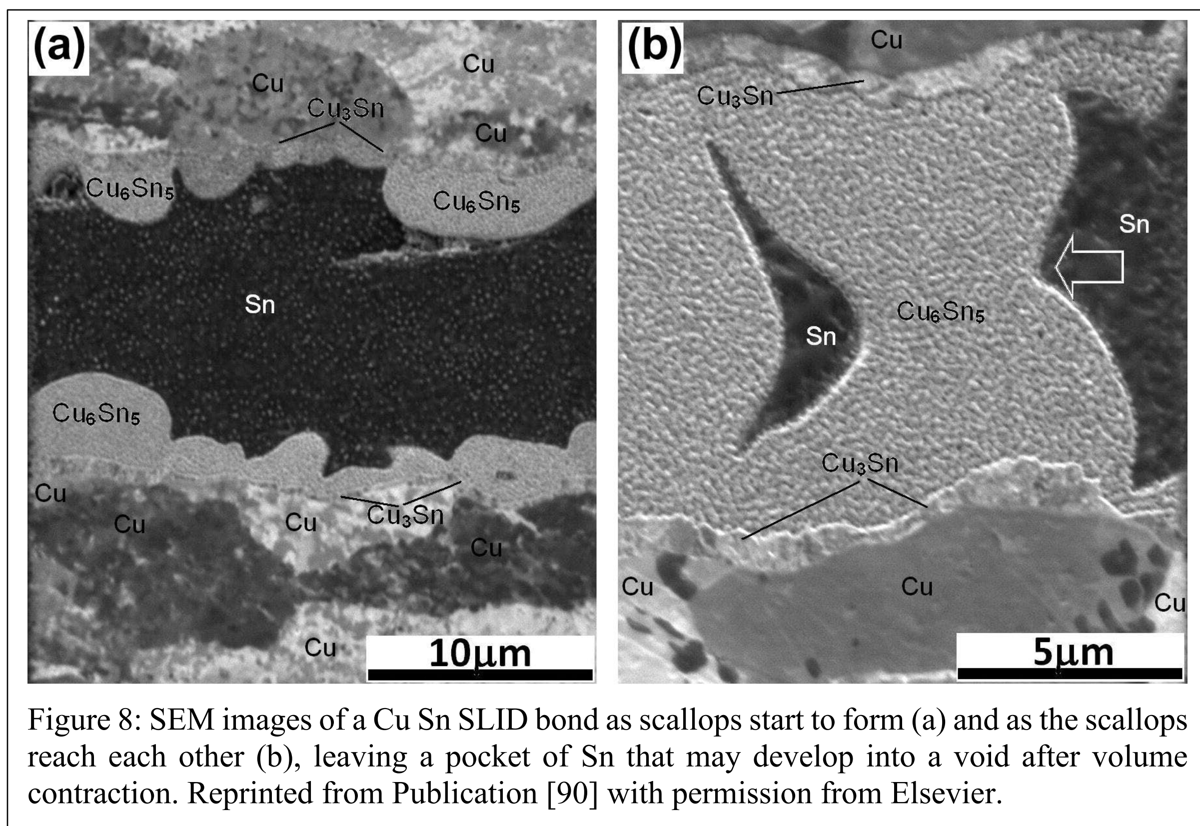

Figure 8: SEM images of a Cu Sn SLID bond as scallops start to form (a) and as the scallops reach each other (b), leaving a pocket of Sn that may develop into a void after volume contraction. Reprinted from Publication [90] with permission from Elsevier.

Several trials and considerations were made before a successful electroplating process was developed at USN for this project. Our final electroplating process was developed using a DMK Maroon 2100 acidic Cu-bath and a DMK Dekatinn 19 acidic Sn-bath and is as follows:

Firstly, care must be taken when designing the pattern to be electroplated. The pattern should be as symmetrical as possible to ensure even current distribution, and empty areas, referred to as current thieves, were employed in our design to improve this distribution. Openings must also be made in the photoresist for the connection of the wafer to the current source.

Secondly, care must be taken to prepare both the wafer and the electroplating solution. As mentioned, the solution decays with time and use, so a freshly prepared bath is preferred. Controlled circulation is also important, and the solution should be allowed to circulate for 0.5-1 hour to ensure it is filtered and stabilized. Briefly plating a dummy wafer at an elevated current is also a good idea if the equipment has not recently been used. This will remove the outer layer of the anode, which may be contaminated. Plasma cleaning the wafer is also advantageous as it will remove contaminants and activate the wafer prior to the deposition.

The wafer is then fastened properly in the holder, ensuring connection at all intended spots which should be equally distributed across the wafer to facilitate even current distribution. The program supply is then programmed with 5mA/cm^2 for 0.5 s forward and 15mA/cm^2 for 20 ms. The inclusion of pulsed electroplating and reverse electroplating was found to reduce the surface roughness. The wafer also needs to be rotated. This helps compensate for the remaining discrepancies in the current distribution. For our process, the wafer was rotated 90° for every ¼ of the total electroplating time which improved the uniformity of the electroplated Cu.

To evaluate the resulting bondline, a profilometer is recommended for point measurements due to its speed and simplicity of use. Since it provides limited data, a white light interferometer

should be considered when developing a recipe, since it requires more time, but will much more accurately analyze much larger areas (see Figure 9).

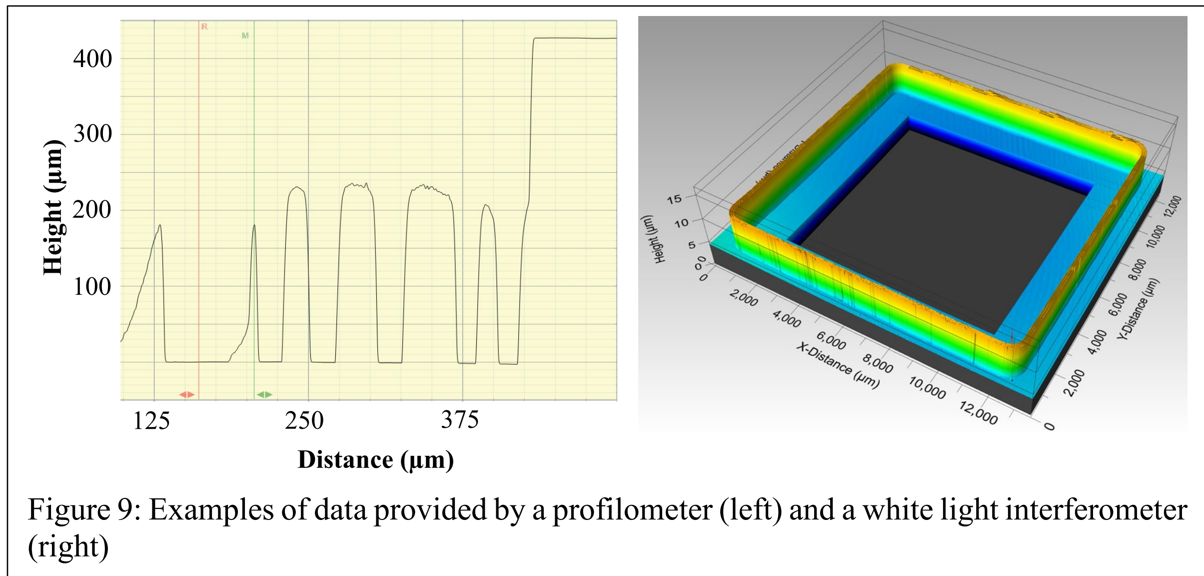

Figure 9: Examples of data provided by a profilometer (left) and a white light interferometer (right)

4.3 Pre-bond

4.3.1 Etching of seed- and adhesion-layers

Once the Cu and Sn bondlines have been electroplated, we can use these metals as a mask for the subsequent removal of the superfluous seed- and adhesion layers. For our process, these materials were deposited on the entire wafers, and leaving them there will hinder the subsequent cavity etching, but also increase squeeze-out because Sn adheres well to Au.

The gold is removed by a mixture of water (60-80%), potassium iodide (10-30%), and iodine (1-10%). The TiW is removed by a 30% hydrogen peroxide mixture at ~50°C.

4.3.2 Cavity etching by DRIE:

Reactive Ion Etching (RIE) is a technique that uses both physical and chemical processes to selectively remove material from a substrate. It uses a combination of the plasma techniques already described in the “cleaning” section and volatile gasses to remove material [96]. The most important feature, compared to wet-etching, is that this technique allows for very directional, also called anisotropic, etching. Deep RIE (DRIE) is an extension of this technique that includes at least two radio frequency generators, lower pressures, a wider temperature

range, and faster control of mass flow [96]. These additions lead to better process control and the capability to further tune the selectivity of the etching.

One such etching process, that happens to be used to etch the cavities in the cap wafer for our application, is the Bosch process. This process uses the fact that when C_4F_8 is used to etch, fluoropolymers are deposited on the sidewalls, which limits the etching in these directions [96]. The process used at USN alternately deposits the passivating gas C_4F_8 and the etching gas SF_6. The gases are exposed to a strong plasma which causes them to react and accelerate. These steps are then repeated in cycles until the desired depth is achieved. A typical process at USN process used a PlasmaPro 100 Cluster DRIE machine from Oxford Instruments and ran for 200 cycles for a total depth of 120 µm, each cycle lasting about 4 seconds.

4.3.3 Deposition of anti-reflection measures:

A sample with ARC was not bonded during this work, but the process is uncomplicated considering the cavity etching and anti-reflection measures are only necessary on the cap wafer, where the process requirements are much less strict due to the lack of devices and CMOS circuitry. For a thin film ARC as described in [97], a shadow mask could be placed on top of the wafer prior to sputtering, meaning the materials will only be deposited in the openings, i.e. inside the cavities.

The patterning of Moth-Eye structures, as described in Chapter 6 and article [98], is slightly more technical, but also feasible. Silicon dioxide must be grown on the wafer prior to Sn electroplating, since the increased temperatures required for the oxide to grow, will cause the metals to interdiffuse should they both be present. This also means the Cu oxide must be removed, prior to Sn electroplating. PR can be deposited inside the cavities by spray coating and the photoresist inside a cavity can be exposed by holographic lithography, meaning a laser source is split into multiple beams, making it easy to quickly pattern multiple circles at a distance [99].

4.4 Bonding

The wafers are now ready to be bonded. Firstly, the clean wafers must be aligned and placed so that the Cu and Sn seal frames, deposited on both wafers, face each other. This is done by using specific patterns on the face of the substrate wafer and aligning them with the alignment

marks on the back of the cap wafer. The alignment marks on the cap wafer were also used in the photolithography process prior to the deposition of the seal frames of the cap wafer, which is why they match up. Although some wafer bonders allow this aligning to be done inside the heating chamber, it is often necessary to align the wafers externally, clamp the wafers together, then transport them to the bonder, as is the case for the current setup at USN.

The properly aligned wafers will then be subjected to a so-called bonding profile, an example of which can be seen in Figure 10. This bonding profile describes what temperatures the wafer is subjected to, and for how long. It also includes information on when the bonding pressure is applied. Successful bonds at USN were performed with 5-15 MPa bonding pressure.

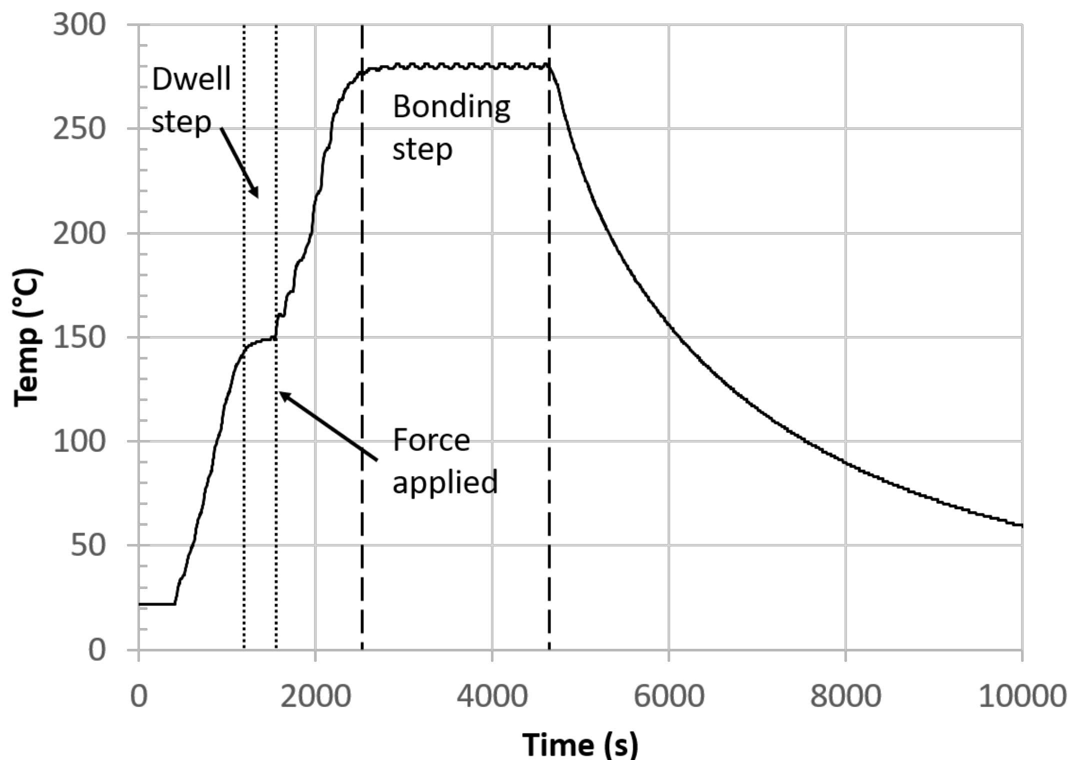

Figure 10: Temperature profile with dwell step, point of force application and bond step indicated. Reproduced with permission from [16].

In our bonding profile, we have included a dwell step. By leaving the bond for a time at an elevated temperature below the melting point of Sn, IMCs start to grow slowly, resulting in smaller scallops and decreased amount of pure Sn available when the melting point is reached, which reduces squeeze-out [23].

The entire bonding process is performed at 10^{-3} mbar, which will be the resulting pressure inside the seal frame. Once the bond profile is complete, the wafers are cooled to room temperature at a moderate rate. They are then ready to be singulated and characterized

4.5 Characterization

4.5.1 Optical microscopy, grinding, and polishing

The most common method of presenting SLID bonds is to look at a cross-section of the bond with a microscope. To look at the inside of the bond the bonds are usually subjected to a grinding process, to reach the cross-section of the bond we wish to investigate. To stop this grinding process from breaking or otherwise affecting the bond prior to characterization, it is common practice to mold the entire bond in a protective epoxy. After the molding and grinding, the surface of the cross-section will be very uneven and hard to resolve for a high-resolution microscope, so a polishing step is also generally employed.

When the sample is properly prepared, a lot of information can be deduced by employing an optical microscope. The different phases can be distinguished [100], and different types of voids can be identified, which in turn will provide information on whether an adequate bonding pressure, temperature profile, and electroplating quality has been achieved [101].

It is very important to note, that a single cross-section provides very limited information. Multiple cross-sections must be performed if conclusions are to be drawn about the entire bond based solely on these cross-sections. This technique is also destructive, meaning the bond is destroyed in the process of characterizing it.

4.5.2 SEM & EDS

Scanning Electron Microscopy (SEM) is a staple in MEMS characterization. The basic working principle of an SEM is to use reflected electrons instead of reflected light, to observe an object. Because electrons are heavier than photons, they also have a shorter wavelength, which in turn means they can resolve much smaller objects than is physically possible in optical microscopes due to the diffraction limit (0.3µm-0.1nm) [102]. This enhanced resolution can be used to more accurately identify and measure voids and the thicknesses of the different phases in a bond.

Because the SEM contains an electron gun, an energy-dispersive x-ray spectroscope (EDS or EDX) may be incorporated into the setup. This technique uses electrons to stimulate the sample to emit x-rays by exciting electrons from an inner shell, creating a vacancy in this shell, which will be filled by another electron. As an electron jumps from a higher shell to a lower one, energy will be released in the form of an x-ray. Because the amount and energy of these x-rays will be different depending on what shell the electron jumped from and to, as well as the atomic structure, these x-rays may be analyzed to give information on the elemental composition of a sample [102]. This information is useful in determining what phase is in the different layers of a sample. If the EDS finds Cu and Sn in the ratio 3:1, for example, we can conclude we are looking at Cu_3Sn.

It is important to note, that since we are, once again, only looking at a cross-section, all the limitations mentioned in the previous "optical microscopy" section, also apply here.

4.5.3 IR-microscopy

Because we are bonding silicon, which is transparent to IR-light, with Cu and Sn, which is not, it is possible to gain some insight into the bond without opening the package. By shining light from an IR source on one side of the wafer and mounting an IR camera with magnifying optics, the parts of the wafer with metal on it can easily be distinguished from the parts with bare silicon. This means that we can analyze the size and shape of the bond in 2 dimensions, with the sample perfectly intact [16]. These images will, however, provide limited information, considering we will only see a black-and-white view of the sample showing where there is or isn't metal.

4.5.4 Shear testing

Shear testing is also a staple for testing bonds. It is performed by immobilizing the bottom part of the sample, then using a metal tool to exert a sideways force on the top part of the die only. This force is then increased at a set rate until the sample breaks and the peak force is registered. Additional information may be found by analyzing the surfaces of the broken sample with a traditional and/or confocal microscope to identify at which interface, or interfaces, the fracture occurred [16]. This test requires the breaking of the bond and is therefore a destructive test.

The shear strength is also dependent on a lot of factors, such as bond geometry, bond composition, adhesion between bond layers, and the presence of voids. This can be considered an advantage since a high shear strength value indicates all these things have been tested simultaneously and are in order. The disadvantage, however, is that it is near impossible to discover the reason for poor shear test results, from shear testing alone. The large number of factors also means that there often is a large variation in shear strength values, meaning many test vehicles must be destroyed to achieve an accurate quantitative estimation of the shear strength.

4.6 Process summary:

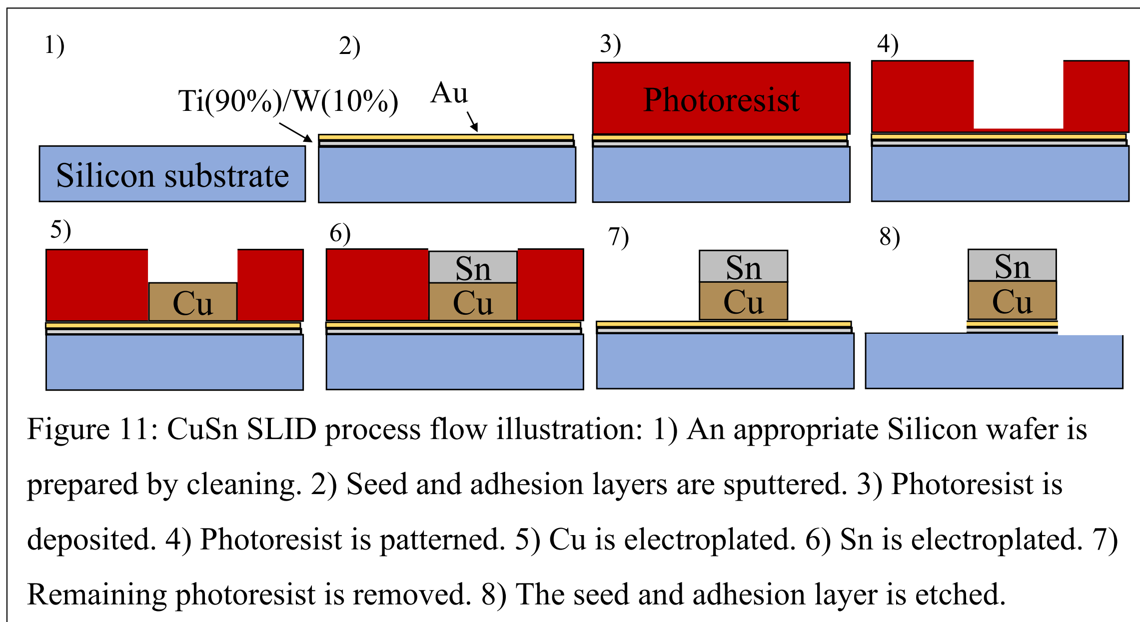

Figure 11: CuSn SLID process flow illustration: 1) An appropriate Silicon wafer is prepared by cleaning. 2) Seed and adhesion layers are sputtered. 3) Photoresist is deposited. 4) Photoresist is patterned. 5) Cu is electroplated. 6) Sn is electroplated. 7) Remaining photoresist is removed. 8) The seed and adhesion layer is etched.

The process described above is the result of an extensive literature review on CuSn SLID, trial and error by employees at USN, as well as improved instrumentation at the Department for Microsystems and is summarized in Figure 11. The process flow will have slight alterations, depending on whether it is a cap or device wafer. A cap wafer will have the etching of backside alignment mark described in Chapter 4.3.1 between step 2 & 3 in. It will also include the cavity etching step described in Chapter 4.3.2 and the deposition of anti-reflective measures as described in Chapter 4.3.3, both of which are performed after the process flow in Figure 11.

A device wafer would include a bolometer protection step before depositing the metals and a bolometer release step before bonding, i.e. before step 1 and after step 8 respectively in Figure 11. This is because a fully functional MBA is not able to survive wet processing and a support

material that may be later removed is therefore necessary. An example of this can be seen in [64] where a sacrificial layer of silicon dioxide, which is removed by hydrofluoric acid, is employed. The exact details of the bolometer in this application are the intellectual property of a partner company in the APPLAUSE project and may therefore not be disclosed.

While most of the details described in this chapter exist elsewhere in articles and books, I have not found a SLID process description that includes this level of detail – despite several fresh researchers, including myself 3 years ago, have expressed a need for it. By including these details, motivations and insights, I hope to preserve these process details for future generations of researchers who might also struggle to find good sources bridging the gap between basic working principles and detailed process descriptions.

5 Fresnel reflections

5.1 What are Fresnel reflections and why do we care about them?

We have previously described that we intend to package the microbolometer array - i.e. thermal camera image sensor – by placing a micromachined cap made from silicon on top of it and sealing it with SLID bonding. This means, that the infrared light will have to pass through this cap, in order to hit the sensor and generate a response (see Figure 12).

Absorption in a material is defined by:

$$A = (1 - r) * \frac{1-e^{-at}}{1-re^{-at}} \quad (1)$$

Where $r = \left(\frac{n-1}{n+1}\right)^2$, n is the refractive index of the material, a is the absorption coefficient and t is the thickness of the material in mm [103]. Refractive index and absorption coefficient values are not the same across all wavelengths, but for silicon, at a wavelength of 10 μm, these values are a=0.729 & n=3.4181 typically [104]. This means that for a cap with a thickness of 200 μm, there will be an absorption of ~12 % of the incoming light. Since this may be even further reduced by using high-purity silicon [105], this is considered acceptable. As we will see in the following paragraphs, this is not the case for reflection.

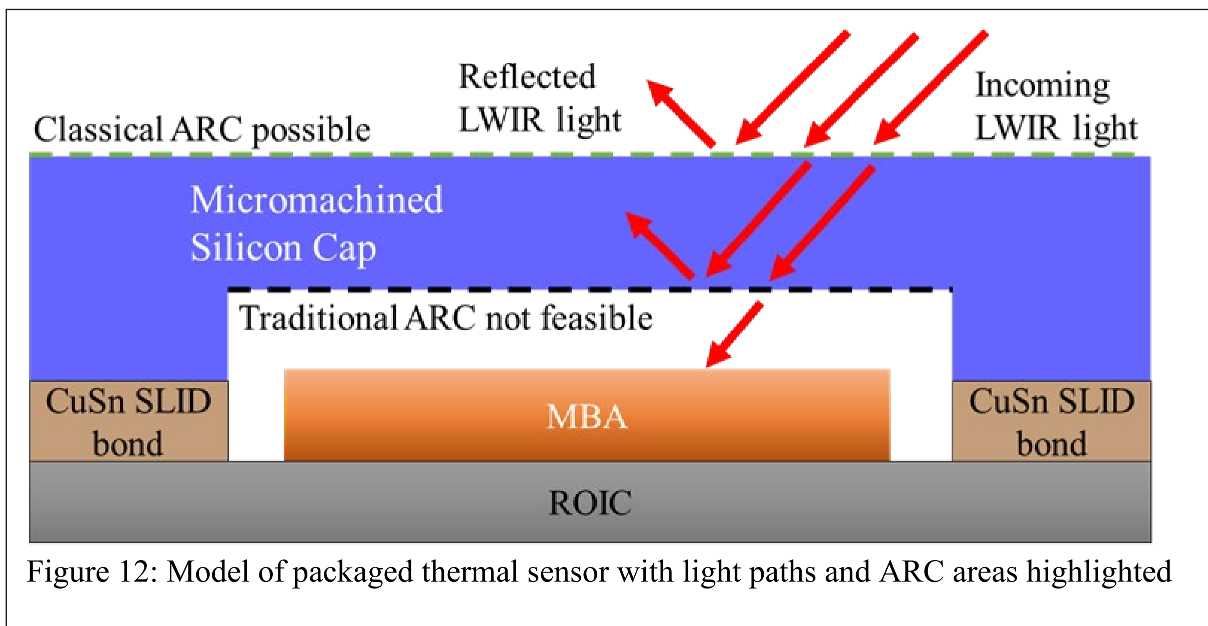

Figure 12: Model of packaged thermal sensor with light paths and ARC areas highlighted

In 1821 a French civil engineer and physicist named Jean-Augustin Fresnel presented a set of equations, one of which enabled easy calculation of the amount of reflected light that occurs at a boundary of two mediums with different refractive indices [106]. A simplified version of these equations that results in the fraction of reflected power for a single interface with plane waves R, is as follows:

$$R = \left|\frac{n_1 - n_2}{n_1 + n_2}\right|^2 \tag{2}$$

Where n_1 and n_2 are the refractive indices of the two media at either side of the interface. Inserting for air and silicon, this results in ~30%. Considering the silicon cap will have 2 such interfaces (see Figure 12), this is not acceptable. This is however a pretty common problem, and a common approach to solve it, is a so-called anti-reflective coating (ARC).

5.2 What is an anti-reflective coating?

An anti-reflective coating is a coating deposited on a surface to minimize reflections. As we can see from equation 2, the larger the difference in refractive index, the larger the fraction of reflected power. A typical ARC minimizes reflections, by making the transition between the two materials more gradual. It does this by having multiple layers, each with a gradual shift in refractive index from one medium towards the next [107]. This is often referred to as a Graded Refractive INdex (GRIN) (see Figure 13).

ARCs also utilize destructive interference to minimize reflections. By tuning the thickness of the ARC to be one-quarter of the wavelength, the reflections that occur at the ARC-substrate interface will cancel out the reflections that occur at the air-ARC interface, which will assist in lowering reflection [107, 108].

As mentioned previously, we would like a gradual change in the refractive index, to lower reflections. Unfortunately, finding materials with ideal refractive indices is not a trivial matter, especially considering we also have other material requirements such as adhesion, toxicity, price, and deposition methods available. Fortunately, Epstein demonstrated long ago that we can use Herpin's theorem to approximate a thin layer of an arbitrary refractive index, with a pair of high- and low-index layers with the same total thickness as a single ideal layer would be [109] (see Figure 13). This is the approach taken in [97].

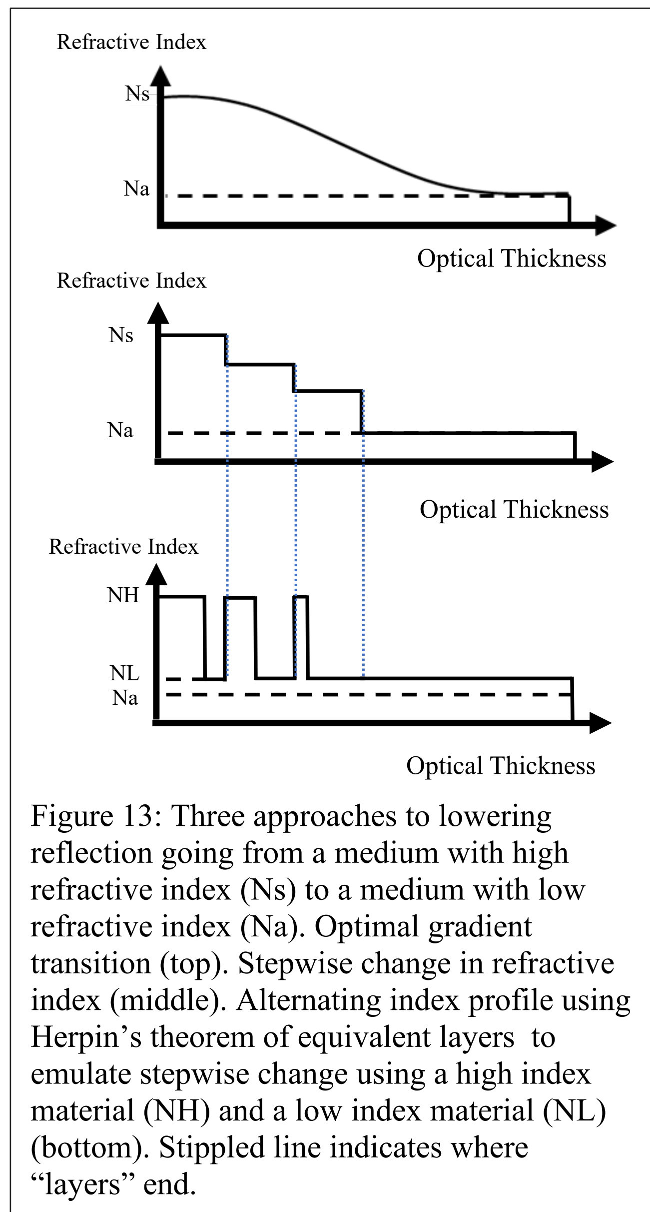

Figure 13: Three approaches to lowering reflection going from a medium with high refractive index (Ns) to a medium with low refractive index (Na). Optimal gradient transition (top). Stepwise change in refractive index (middle). Alternating index profile using Herpin's theorem of equivalent layers to emulate stepwise change using a high index material (NH) and a low index material (NL) (bottom). Stippled line indicates where "layers" end.

5.3 Limitations of ARCs

One important thing to note about these coatings is that they are generally multiple layers of different materials with different coefficients of thermal expansion (CTE) [99, 110]. Different CTEs mean that as the temperature changes, the materials increase or decrease in size at dissimilar rates. This often results in delamination, meaning the materials stop adhering to each other and the film stops working as intended and potentially fully disintegrates (see Figure 14) [97].

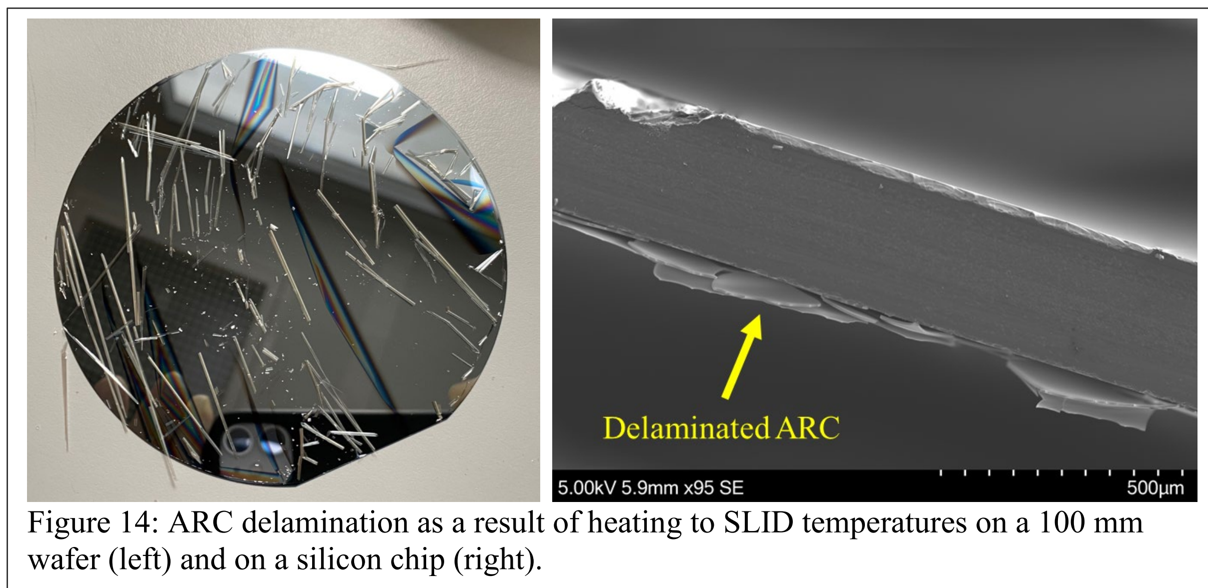

Figure 14: ARC delamination as a result of heating to SLID temperatures on a 100 mm wafer (left) and on a silicon chip (right).

Looking at Figure 14, it is clear we need anti-reflection on the inside of our cap. We also need to apply this anti-reflection measure prior to the SLID process, since we cannot access the inside after the package is sealed. Since the SLID process involves heating the package to 270°C, a traditional ARC will not suffice. In [97], included in this thesis, we present a novel ARC designed to survive these temperatures, but in the following section we will also see that a different approach, based on biomimetics, can provide the same anti-reflective properties by making specific patterns in the substrate materials.

6 Moth-eye structures

6.1 What are moth-eye structures?

Simulations were performed using the finite element simulation software COMSOL Multiphysics to see what impact the surface roughness that resulted from wet-etching a silicon wafer, would have on the transmission and reflection of incoming IR light [24]. Interestingly, when we increased the magnitude of the roughness of such a surface, the transmission actually increased, up to a point. While at the time, this seemed counterintuitive, we later found that nature has known about this effect for a long time.

Looking at Figure 15 we see that the eye of a moth is not smooth, but rather composed of millions of rods, smaller than the wavelength of light. These rods are an evolved trait that helps the moth survive at night. By increasing transmission, more light is directed to the inside of the moth's eye, helping it see better in the dark, but also reducing the amount of glare, making it harder for a potential predator to discover [107, 111].

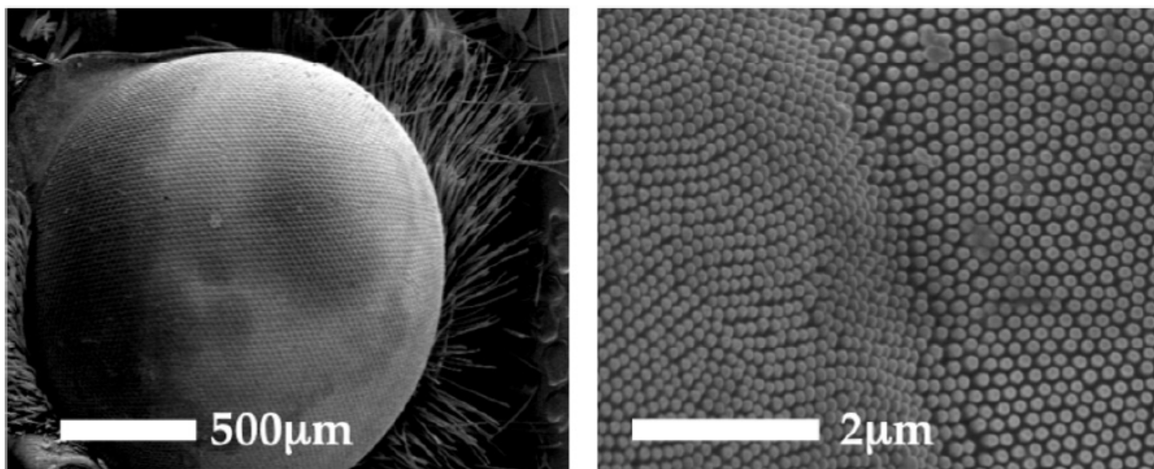

Figure 15: SEM images of the eye of the common gray moth (likely Anavitrinella pampinaria), showing sub-wavelength tissue protuberances and microscale lens-like structures. Reproduced from [111] with permission from Optica Publishing Group.

Physically, this technique works similarly to an ARC, but with some differences. Provided the structures are much smaller than the wavelength, the light behaves as if the structured layer is a homogenous material with its own refractive index [107, 111]. By creating structures that gradually increase the amount of the second material at the interface, the moth-eye structures

create a gradual transition from one medium to the other, which is equivalent to the GRIN we tried to emulate in the ARC section (see Figure 16).

6.2 Advantages of moth-eye structures

Two advantages of these moth-eye structures have already been hinted at in previous sections. The first advantage, which is also the reason for them being investigated for this use case, is that these structures are all one material. This means that we will experience none of the CTE mismatch issues we described for the ARCs, which in turn means they are much more temperature resilient [99, 107, 111]. The other advantage is that by tuning the size of the structures, they can be adapted to reduce reflection for any wavelength region [99, 107, 111].

A previously unmentioned advantage of moth-eye structures is that they outperform ARCs at higher angles of incidence [99, 107, 111]. They are also inherently more broadband, meaning they can lower reflection for a wider range of wavelengths than ARCs [99, 107, 111].

An important thing to note is that these structures may cause scattering of the incoming light if they are not tuned properly. This is especially important for visual applications considering this scattering may distort the image. This phenomenon can, however, be minimized by making the structures sufficiently small compared to the wavelength [99]. Design rules proposed by Hobbs et. al. are: 1) The structures should be 40% higher than the highest desired wavelength to achieve good anti-reflection and 2) The pitch of the structures should be smaller than 30% of the shortest desired wavelength to avoid free space diffraction losses, i.e. scattering [99].

Moth-eye structures show promise, but the field is still not mature. Article 5: Moth-eye anti-reflection structures in silicon for Long Wave IR applications, I present the first publication to describe structures in silicon for this wavelength range, and the structures explored are also not found in the literature. In the article, the design rules described above are explored through simulation and experimentation, and the fabrication process is described in detail, which was also lacking in the literature published to date.

7 Summary of articles

7.1 Article 2 & 3: Patterned seal-frames for SLID and their impact on Squeeze-out and bond strength:

7.1.1 Introduction

Two important factors in reducing voids in Cu-Sn SLID are the application of bonding pressure and Sn thickness. The bonding pressure improves the quality of the bonds by breaking the Sn oxide, and by compensating for any roughness in the bonding partners. Higher bond pressures yield stronger bonds with less voids [101]. A sufficiently thick Sn layer is required to ensure liquid Sn when the bond temperature is reached. This is because the growth of IMCs is scalloped, not planar [91]. These IMC scallops may act like spacers which could prevent the bond from developing evenly which may result in voids.

Since the Sn is in liquid phase for a period during the bonding, the bond force will cause some of the Sn to squeeze out past the intended bondline [90]. The amount of squeeze-out is related to the bond force magnitude and has the potential to short-circuit electronics or form weakly adhered droplets which may detach during operation, causing a critical failure after the product has reached the consumer [90].

Since higher bonding pressures yield stronger and more reliable bonds, but cause more squeeze-out, a balance must be struck. Our work attempts to shift this balance by presenting seal-frame geometries that accommodate this squeeze-out, potentially allowing for higher bond force.

7.1.2 Article 2: Investigation of seal frame geometry on Sn squeeze-out in Cu-Sn SLID bonds

In the conference article "Investigation of seal frame geometry on Sn squeeze-out in Cu-Sn SLID bonds", a single continuous 200µm wide bondline and a geometry consisting of 3x50µm wide bond rails with 25µm wide gaps are compared in terms of squeeze-out and shear-strength. Wafers are made with identical process parameters, but different seal-frame geometries and compared using non-destructive IR microscopy and die shear testing.

Point measurement comparisons made at a corner of both versions of dies show a 60% average reduction in squeeze-out. High shear strengths are measured in both geometries, with the patterned seal frames showing higher average strength, but a larger deviation (31±9MPa compared to 43±18MPa). From these values, we conclude that patterning the seal frames does not lead to a reduction in bond strength. The lack of significant difference in shear strength results is supported by simulations in COMSOL Multiphysics.

7.1.3 Article 3: Squeeze-out and bond strength of patterned Cu-Sn SLID seal-frames

This article extended the work in article 2 by studying more geometries and improving the characterization techniques. By upgrading the IR-microscopy stage, micrographs could now be taken with enough consistency for software to reliably stitch them together into a single image. ImageJ could then be used to quantify the size of the entire seal-frame area. 3 alternative designs, all of which include open spaces to accommodate squeeze-out, were compared to a contrinuous seal frame in this article. They are: 1) One mating partner with 3x50 µm wide rails and 25 µm gaps as seen in article 2. 2) Same geometry, but with 50 µmx200 µm square hatches added across the rails with a pitch of 75 µm. 3) Asymmetric samples with one 150 µm wide mating partner leaving 25 µm of open area at either side. For all geometries, the other mating partner is a continuous 200 µm wide seal frame. All were designed to have the same width when viewed from above, so any extra area would be due to Sn squeeze-out. After comparing multiple dies, no significant difference in squeeze-out could be observed for the geometries with rails or hatches. For the asymmetric samples, however, a 46% reduction in average squeeze-out could be observed.

The lack of squeeze-out reduction in the railed and hatched samples is attributed to poor filling of the internal gaps. This poor filling may be due to the scalloped growth of Cu_6Sn_5 and impurities deposited during electroplating, causing the liquid Sn to flow outside the bond. This also explains the reduction in squeeze-out seen in the asymmetric samples, since these samples have room designated for squeeze-out on the outside of the bond.

Shear strength results in this study are 80±18 MPa for the railed-, 57±13 MPa for the hatched-, 48±30 MPa for the asymmetric- and 17±7 MPa for the continuous samples. The significantly

higher shear strengths in the samples with gaps are attributed to the gaps stopping crack propagation, a phenomenon that is utilized in so-called “stop holes” or “defense holes” [112].

7.2 Article 1 & 5: Structures in silicon to improve LWIR transmission

7.2.1 Article 1: Simulated effects of wet-etched induced surface roughness on IR transmission and reflection

As described in this thesis, a promising approach to package the microbolometer is to use a silicon lid with a micromachined cavity and SLID bonding to encapsulate it and thus maintain its high vacuum requirements. One technique for creating the cavity in the lid considered early in the project, was wet-etching with KOH. Since this technique leaves some surface roughness, a COMSOL Multiphysics simulation was made to investigate the effects of this roughness on the incoming light.

A scan with an AFM was imported into COMSOL Multiphysics. This allowed us to replicate the surface, but also digitally manipulate it. To investigate the tolerances in surface roughness, the z-values in the measurements were multiplied by an increasing number, which proportionately increased peaks and valleys. Transmission and reflection of LWIR light with 8-12 µm wavelength passing through such a surface was then analyzed.

The simulations showed that wet-etch-induced surface roughness is not a concern when it comes to reflection and transmission. Instead, it is shown that a correct amount of RMS surface roughness (~500 nm) actually increases transmission as compared to a flat surface.

7.2.2 Article 5: Moth-eye anti-reflection structures in silicon for Long Wave IR applications

The results presented above seemed counterintuitive at first until we came upon the concept of moth-eye structures. These structures, which we describe in more detail in Chapter 6, ME structures lower reflections by gradually increasing the amount of silicon (see Figure 16), thus forming a Graded Refractive Index (GRIN) layer [111, 113]. These structures are very resilient to changes in temperature as opposed to ARCs [111, 113, 114]. This meant they were ideal for

application on the inside of the cavity of the silicon lid, which would otherwise reflect ~30% of the incoming light out of the package (see Chapter 5.1).

Moth-eye structures were fabricated using design rules outlined by Hobbs et. al. [99] and a variation of the Generation Of PHotonic Elements by RIE (GOPHER) process developed at Stanford University [115, 116]. Simulations of the structures were also performed using COMSOL Multiphysics. The structures demonstrated an approximately 5-percentage-point increase in the targeted 12-16 µm range, but all techniques and approaches are applicable to the 8-12 µm range more relevant for thermal imaging. A suggestion for an improved structure, which could be achieved with a few alterations to the recipe, was also presented and simulated. This structure shows promise of increasing transmissivity by another 5-percentage-points for a total of 10-percentage-point increase per side.

This approach of using well-established and scalable techniques, such as photolithography, isotropic and anisotropic etching, may, if refined to provide higher transmission as described, be applied to high-volume packaging of microbolometer-based thermal cameras. This process requires only a single photolithography mask and no alignment which reduces equipment requirements and processing steps.

7.3 Article 4: Temperature Resistant Anti-Reflective Coating for LWIR imaging on Si-wafer

As mentioned in Chapter 5.1, about 30% of the incoming light is reflected at a single air-silicon interface, which is why we need some form of anti-reflection measure on both sides of the silicon cap. A common approach to lower reflection that is efficient, cheap, and simple to implement in a manufacturing process is ARCs. Whatever coats the inside of the cap will, however, be required to survive the bonding temperatures of SLID, i.e. 270°C, and, as mentioned in Chapter 5.3, ARCs are considered sensitive to changes in temperature due to their multiple layers with different CTEs [99, 110].

In this article, we developed an ARC capable of retaining its anti-reflective properties and mechanical integrity up to 300°C for 1 hour. This was done by using a combination of fewer layers, a thin MgO adhesion layer, and a deposition temperature in-between room temperature and the bonding temperature (100°C). In the targeted LWIR range of 8-12µm, the ARC

demonstrated an average improvement of more than 15% for normal incidence and 13% for 30° incidence when compared to an uncoated wafer.

8 Conclusion

We have presented and described the importance, and challenges, of MEMS with a specific focus on packaging and the microbolometer. We have then described why SLID is the best currently available bonding method for this use case, followed by a thorough description of a packaging process, as developed at USN. This process was developed by the author, with the aid and assistance of colleagues.

Two of the attached articles by the author, describe an attempt to reduce the squeeze-out that occurs during SLID bonding. Employing seal frames with internal gaps is stated to result in a ~60% reduction in squeeze-out, without lowering the bond strength, in the conference article from 2021 [117].

In a later article, 3 seal frame geometries were investigated and compared with a traditional continuous seal frame[16]. In this study, no improvement in squeeze-out could be seen, except for the asymmetric samples which showed an average reduction of 46%. The difference in findings is due to a more thorough study of multiple dies with area measurements in the IR micrographs, rather than the point measurements used in the earlier article. The seal frames with internal gaps are, however, shown to have a higher strength than traditional continuous seal frames, with some geometries showing as much as 400% higher shear strength values.

The optical challenges have then been presented, followed by two potential approaches to solving these problems, namely ARCs and MEs. One of the articles included in this thesis documents the successful development of an ARC capable of surviving SLID bonding temperatures [97]. This is novel considering ARC are generally sensitive to changes in temperature as a result of their multi-layer nature. The ARC shows 15% increased transmission in the 8-12 µm LWIR range and the result is achieved by sputtering a 2-layer ZnS and YF_3 layer and deposition at 100°C. A thin layer of MgO (1-2nm) was also employed to improve adhesion and the resulting thin film can easily be selectively deposited in cavities with a shadow mask.

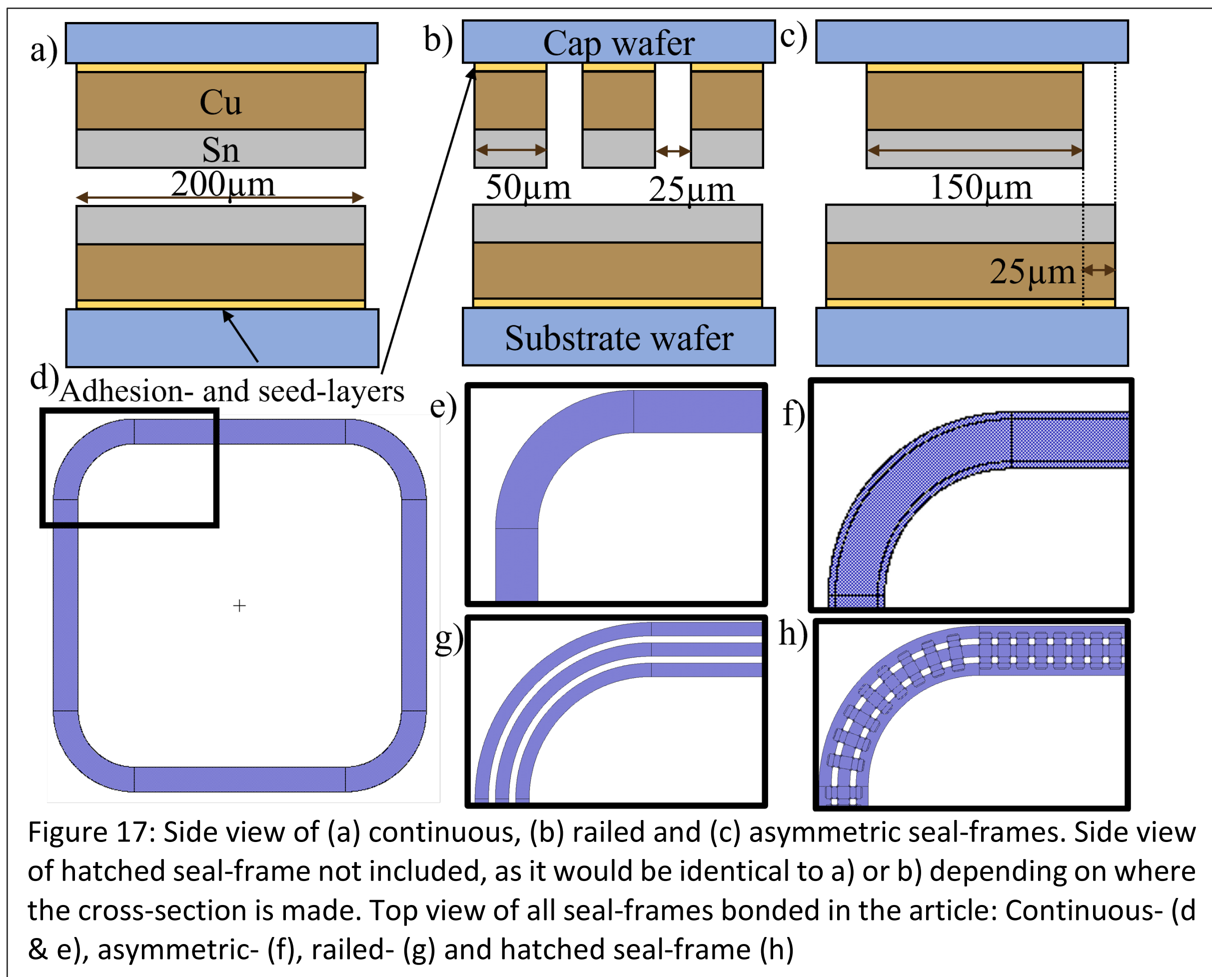

Figure 17: Side view of (a) continuous, (b) railed and (c) asymmetric seal-frames. Side view of hatched seal-frame not included, as it would be identical to a) or b) depending on where the cross-section is made. Top view of all seal-frames bonded in the article: Continuous- (d & e), asymmetric- (f), railed- (g) and hatched seal-frame (h)

The two remaining articles in this thesis relate to the ME phenomenon. The motivation of the simulation paper was to evaluate the potentially detrimental effects of surface roughness as a result of micromachining silicon, but the result was to demonstrate that specific surface structures aid in lowering reflection [24]. The final paper presents the results of an exchange and collaboration with Stanford University to manufacture such structures in silicon in a

scalable way to lower reflections in the LWIR region. This was achieved by patterning silicon oxide and using it as a hard mask which survived the following isotropic and anisotropic etching steps. By alternating these steps, we developed a recipe and presented the resulting structures. The structures showed a 5% increase in transmission for the 12-16 µm range it was designed for, but simulations suggest the structures will attain a 10% increase in the 8-12 µm range with few alterations to the recipe [98].

8.1 Outlook

The work in this thesis can be further investigated in the following ways:

- The simulation used to study the effects of wet-etched induced surface roughness on IR transmission and reflection was 2D. More accurate data would be obtained by using a 3D simulation. The simulation should also be experimentally verified.
- A mechanism for why patterning seal-frames didn't reduce squeeze-out is proposed, but not investigated. More advanced techniques like x-ray tomography could be used to investigate if impurities from electroplating, presenting as voids, and squeeze-out areas are correlated. Continuously observing a Cu-Sn stack during annealing under pressure with, for example, heat and pressure-resistant glass and video, could determine if areas with early scalloping and squeeze-out are correlated.
- The shear strength results vary from article to article. While this is common, more samples from more bonded wafers could be studied to better quantify how much higher shear strength is observed for patterned seal frames than continuous ones.
- While the temperature-resistant ARC has shown to survive the temperatures required for this application, it was not determined at which temperatures it no longer maintained its ARC properties. It was also not investigated how many such cycles the ARC could survive. This could be mapped out by a more in-depth heat-cycling study.
- It was shown that a 6-layer ARC could not survive the temperatures required for this application, unlike a 2-layer ARC with increased deposition temperature. It was not, however, investigated whether a 4-layer ARC with elevated deposition temperature could survive the heat-cycling. This could be investigated in future work
- The improved moth-eye structure we described showed great promise in simulations, but was not realized.

- Adding even more anisotropic-isotropic etch steps to the moth-eye recipe, could provide even lower reflection results. More simulations could be performed to establish a point of diminishing returns and a cost-benefit analysis could be made to establish a “perfect” GOPHER recipe for moth-eye structures.

8.2 Concluding statement

This thesis represents the work and insight gained by the author with collaboration and assistance of the colleagues listed within. It is a summation of the knowledge gained through research, review, experimentation, simulation and discussion. The motivation for the thesis is to develop and improve the packaging process of a microbolometer array, intended to be used in a thermal camera. My thesis achieves this in the following ways:

I have presented articles that provides insights on how patterning the mating partners may affect the final result when the bonding process involves a transient liquid phase. While the articles in question deal specifically with CuSn SLID – the most promising candidate for this appliacation – the findings are likely to be valid for other similar bond types, such as soldering. In these articles are also the beginnings of a complete packaging process compatible with microbolometer arrays. This process is described in more detail in this thesis.

Anti-reflective techniques have also been explored and presented in this thesis. Moth-eye structures show great promise to provide improved transmission in a resilient fashion at a range of wavelengths, but more research is required. I have contributed to the maturity of this field by exploring novel structures in a material and wavelength range previously unreported.

An Anti-Reflective Coating capable of withstanding 300°C have also been presented. Because these coatings are generally considered voulnerable to changes in temperature, this provides fresh insight to an established field of research, possibly paving the way for new application areas. My article describing this coating also presents multiple failed attemps. These provide insight on approaches not suited for this application, but also describes the thought process that brought us to the final successful ARC.

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10 Publications

10.1 Article 1:

Papatzacos, P. H., Akram, M. N., Bardalen, E. & Øhlckers, P. (2020). Simulated effects of wet-etched induced surface roughness on IR transmission and reflection. 2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC). Tønsberg, Norway, 2020, pp. 1-4, doi: 10.1109/ESTC48849.2020.9229821.

My contribution: Assisted in formulating the idea. Constructed the simulation and imported the AFM data to construct the Si-air interface. Analyzed the results with the assistance of supervisors. Main author.

Simulated effects of wet-etched induced surface roughness on IR transmission and reflection

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***Abstract*—We have constructed a finite element simulation where we investigate the effects of wet-etch-induced surface roughness on transmission and reflection of infrared light in the 8-12um band. A silicon wafer was wet-etched for 2 hours in a 10% KOH solution at 80°C, scanned in an atomic force microscope, and the surface profile was recreated in COMSOL. Simulated plane waves of light and varying angles of incidence were then allowed to pass through this surface and the resulting effects on the reflection and transmission were investigated. Roughness was then amplified to investigate the effects of increased surface roughness. For the wavelengths investigated, an increase in transmission of 8% could be seen up to an RMS surface roughness of 800nm followed by a decrease, while the angles investigated showed an RMS dependent increase in transmission between 20° and 40° for RMS surface roughness' above 1000nm.**

Keywords—Wet-etching, Finite element simulation, LWIR, Silicon, Packaging, Transmission, Reflection

I. INTRODUCTION

Thermal imaging cameras have potential applications in security, manufacturing, and in the automotive industry. Price is, however, a limiting factor in most of these applications, in large part due to the sensors' packaging requirement [1, 2]. The challenge is that optical sensors are often delicate and require protection from the environment. This is even more so the case for microbolometer (MB)-based infrared (IR) sensors, which often require a high vacuum (approximately 0.1-10µbar) to operate properly [3]. One attractive way to achieve these operating conditions at large scale is to use advances in wafer-level packaging and hermetically bond a silicon-wafer with micromachined cavities to wafers with Read-Out Integrated Circuits (ROIC) and MB arrays. Using a silicon lid to enclose such a sensor is promising both due to its relatively low absorption coefficient in the Long Wave-IR (LWIR) region, its mechanical strength, and due to the fact that a wide variety of techniques has been implemented in the treatment and processing of silicon.

A commonly used technique for micromachining cavities in silicon is wet-etching in KOH. This is, however, a process that leaves some amount of roughness at the etched surfaces [4]. The effects of surface roughness on optical transmission have previously been theoretically approximated by a number of works [5, 6]. These did not, however, take into account specifics such as slope, peak sharpness, and variations in depths of valleys and heights of hills, all of which impact how much the incoming light is scattered, transmitted, and reflected. Increasing and modifying roughness to achieve lower reflectivity is also of great interest to the solar cell industry [7-9], but for these applications, image quality is of no importance and is therefore not necessarily related to optical sensors. Knowing exactly what type and what amount of roughness the MBA can tolerate at the surfaces of the lid, will help determine which processes are required for the camera to operate properly, and which can be avoided to save cost.

In this work, we are investigating the optical effects of a silicon surface with etch-induced roughness in the Finite Element (FEM) multiphysics simulation software, COMSOL. A silicon wafer was wet-etched for 2 hours in a 10% KOH solution at 80°C, which resulted in a depth of 175µm±3µm. An area of 10µm x 10µm of this surface was scanned using an atomic force microscope (Park Systems Co. AFM XE-200) with a resolution of 256x256 pixels. Lines of this surface was integrated with 2D simulations of light with wavelengths between 8µm and 12µm and incidence angles varying from 0° to 60°. The rough-surfaces' effect on transmission and reflection was studied.

II. SIMULATION

The data from the AFM scan described in the introduction was exported as points and 10 of the lines were randomly selected for our 2D simulation. From these points, a cubic spline interpolation was applied and a 2D representation of the surface was digitally recreated for each line (see figure 1). One of the strengths of our simulation lies in this accurate representation of the surface. Similar simulations of surface

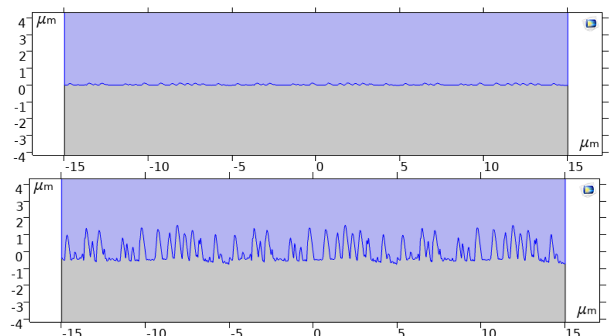

Fig. 1. Digitally recreated wet-etched silicon-air transition (top), and digitally manipulated silicon-air transition with RMS surface roughness of 580nm (bottom). Silicon in blue, vacuum in grey.

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roughness and geometry on optical performance use set geometries [10] or randomly generated roughness within set parameters [11]. By copying a real-life surface, we achieve a more accurate representation of its effects. We later deviate from this real-life approximation by increasing the roughness amplitude of this surface. How this affects our simulation is commented on in the discussion section.

We have in this simulation chosen to only simulate the silicon vacuum interface (see figure 2). Un-etched polished silicon has extremely low surface roughness [4], which means the air-silicon transition is of little interest and is removed to reduce computational requirements. A 30µm wide and 90µm high rectangle is constructed with Floquet periodic conditions on both sides. Perfectly Matched Layers (PMLs) are placed on top and bottom to absorb transmitted and reflected light and thereby avoid interference. In the middle, we place a parametric surface that will define the transition from silicon to vacuum. The vacuum domain has – by definition - a refractive index of 1 while we have used [12] as a reference for the refractive index of silicon in the 8-12µm wavelength range. The features on the etched surface limited the area we could accurately measure with the AFM in a single scan to 10µm by 10µm. For the simulation to make sense, however, we need a model significantly larger than our wavelength. Therefore, to span the entire 30µm transition, the measured line is repeated thrice.

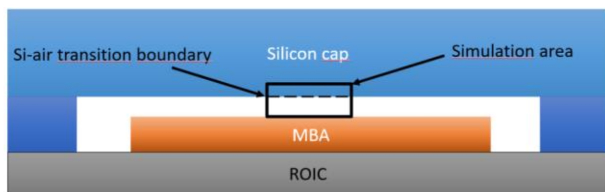

Fig. 2. Model of the entire MBA-sensor layout with simulation area highlighted

We then run 2 simulations for all 10 lines. In one simulation the angle of incidence is increased from 0°-60° in 2° increments, and in the other wavelength is increased from 8-12µm in 0.13µm increments. For every angle of incidence and wavelength, we also increase the roughness by multiplying the deviation from the zero-line – defined by our AFM scan - by an increasing integer. As a control, we run a wavelength sweep, and an angle of incidence sweep with the Si-vacuum transition perfectly flat. The results are then averaged across the 10 lines and plotted in a 3D surface diagram which is shown in the results section. The average amount of mesh elements was approximately 45 000 and the average run-time was approximately 5 hours and 15 minutes.

III. Results

A. *Wavelength sweep*

In figure 3 we can see that the results from the wavelength sweep with increasing roughness are fairly stable, with transmission coefficient ranging from 0.66-0.8. A clear trend we can observe, however, is that there is a clear increase from 0.7 to 0.78±0.02 at RMS surface roughness of approximately 500nm. This is interesting because it is still less than 1/10th of the minimum wavelength, which means it is unlikely to distort the image. The same peak can also be observed in the angle of incidence sweep below at 500nm at 0°.

B. *Angle of incidence sweep*

In figure 4 we see that as the angle of incidence increases, the transmission coefficient drops to zero at approximately 20° which corresponds to total internal reflection. An interesting observation we can make is that between 20° and beyond, an increase in RMS surface roughness actually increases our transmission coefficient. This makes intuitive

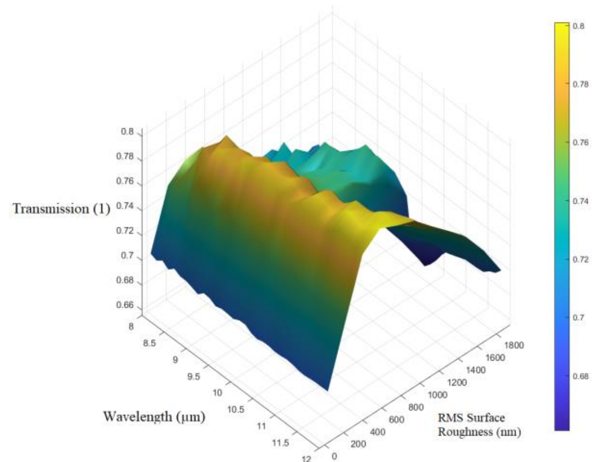

Fig. 3. Transmission coefficient as a result of increasing surface roughness and wavelength.

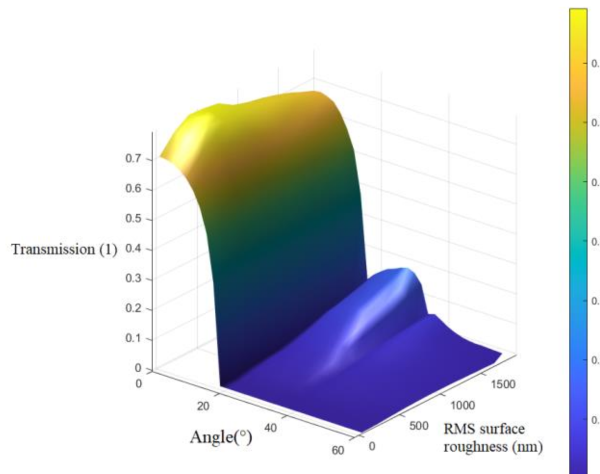

Fig. 4. Transmission coefficient as a result of increasing surface roughness and angle of incidence.

sense, considering that the increasingly sharp peaks will be more normal to light at increasing incidence angles, which aids transmission. It is worth mentioning, however, that the higher the surface roughness in this simulation, the less similar our transition is to the originally measured surface. This makes the simulated results more and more difficult to achieve in real-life.

IV. Discussion

A. Surface validity

When the etched sample is studied under the microscope, some specks could be observed, which is likely reaction products deposited on the surface after etching. To mitigate this, the surface was placed, with the etched face down, in an ultrasound bath with acetone for 30 minutes. This resulted in a surface of sufficiently smooth quality.

The RMS surface roughness of our sample is calculated to be just under 38 nanometers which is an order of magnitude larger than the results achieved in [4]. This could be explained by the fact that our measured sample was etched to a depth of 175µm and theirs only to 10µm, as well as the application of a more thorough cleaning step in [4].

It is also worth noting that our digitally reconstructed 30µm surface transition is in reality a 10µm scan repeated 3 times, which could potentially lead to inaccuracies in surface representation, especially at the transition between each repetition. To investigate this, we calculate the RMS surface roughness values for the 10µm line and compare it to the 30µm line and find a decrease of $9*10^{-13}$nm in the 30µm line, which we consider negligible.

In our simulation, we also increase the roughness, simply by multiplying the z-values in our measurements. While this proportionately increases peaks and valleys, it is unclear whether this relates to real-life cases of wet-etched silicon surfaces. Considering the shape remains intact, it is, however, not unlikely, at least up to a point. The simulation will regardless shed light on the impact of roughness for transmission and reflection for varying angles of incidence and wavelengths in the LWIR region.

B. Simulation validity

While simulation is never a substitute for the real thing, it can demonstrate or highlight problems in a manufacturing process early and cost-effectively, provided the simulation accurately reflects real life. One very important consideration that may affect this validity in FEM simulations like this one is mesh-element size. A general rule of thumb is to have mesh elements no bigger than a fifth of the wavelength. To air on the side of caution, we have chosen a maximum mesh size of 0.8µm which is a tenth of our minimum wavelength. We have also specified a small region surrounding our transition where the mesh size is defined to be a minimum 1.5pm, which is a third of the minimum measured deviation, and maximum 188nm, which is the maximum measured deviation. This is done to ensure that the transition is properly rendered.

Another step taken as a measure of validity is to add up the total of the simulated reflection, transmission, and absorption. In a valid simulation, these fractions should theoretically add up to unity. The plots are shown in figures 5 and 6 and we see that the simulation does this, especially at lower roughness' and angles.

A final step taken to validate our simulation is to compare our simulation of a smooth transition to an analytic estimation. For perfectly smooth surfaces the theoretical reflectance of the surface given by Fresnel's equation:

$$R_{analytic} = \left(\frac{n_1 Cos(\theta_i) - n_2 Cos(\theta_t)}{n_1 Cos(\theta_i) + n_2 Cos(\theta_t)}\right)^2 \quad (1)$$

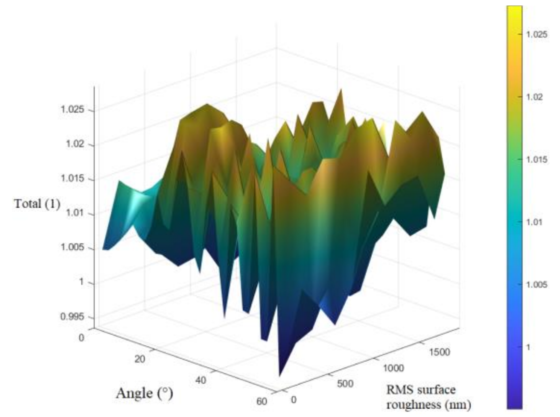

Fig. 5. Control showing the sum of transmission, reflection and absorption for roughness angle sweep

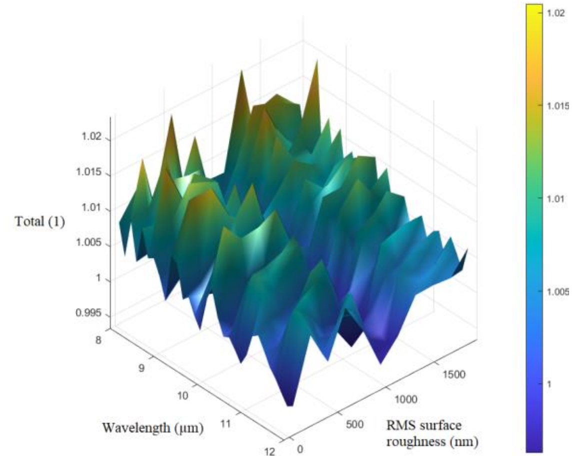

Fig. 6. Control plot showing the sum of transmission, reflection and absorption for roughness and wavelength sweep

Equation (1) may be rewritten as:

$$R_{analytic} = \left(\frac{n_1 Cos(\theta_i) - n_2\sqrt{1-\left(\frac{n_1}{n_2}\sin(\theta_i)\right)^2}}{n_1 Cos(\theta_i) + n_2\sqrt{1-\left(\frac{n_1}{n_2}\sin(\theta_i)\right)^2}}\right)^2 \quad (2)$$

Where n_1 and n_2 are the refractive indices of the two materials in the transition, and Θ_i and Θ_t is the angle of incidence and transmittance respectively. The analytic results from equation (2) are plotted with the simulated results in figure 7 and we see near-perfect overlap between the plots.

V. Conclusion and Outlook

We have constructed a simulation of LWIR light hitting a wet-etched silicon surface with more accuracy than previous works. We have also investigated how increasing RMS surface roughness affects a surface with this topography with regards to transmission and reflection. We can with confidence say that for LWIR light with wavelength 8-12µm, wet-etch induced roughness is not a concern when it comes to

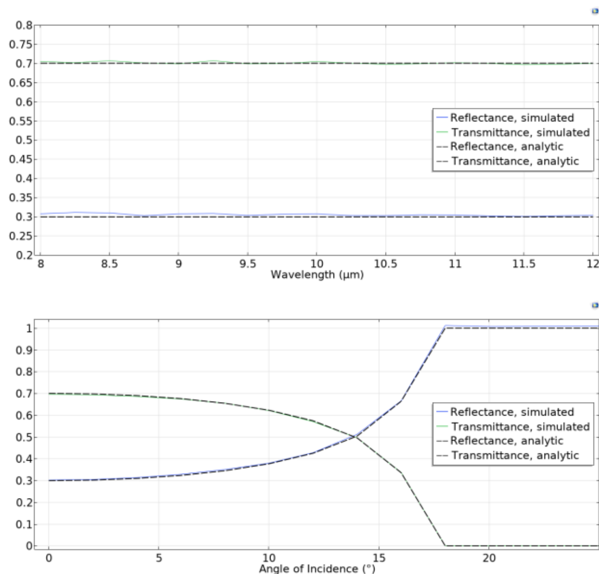

Fig. 7. Comparison of analytic and simulated results for reflectance and transmittance of a flat surface silicon-air transition. Data beyond 25° has been remover as the results are the same from 20° upwards

reflection and transmission, especially considering our high RMS values compared to other wet-etch analyses.

We have also reported that for angles between 20° and 40°, higher surface roughness may actually lead to lower reflection and higher transmission than a smoother surface. For wavelengths between 8µm and 12µm, we saw a peak in transmission at approximately 500nm surface roughness. This will be experimentally verified in further work and could lead to possible implementations as anti-reflective topographies in optical systems e.g. solar cells and thermal cameras.

Most importantly, however, we have constructed and demonstrated a simulation framework that may be used for a multitude of surfaces, wavelengths, incidence angles, and materials, with more accuracy than previous simulation work and with less physical requirements than experimentation. This simulation will also be expanded to make estimations with simple anti-reflective coatings, and the effect of surface roughness on converging light beams, to give insight into the roughness' effect on image quality.

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10.2 Article 2:

Papatzacos P. H., Tiwary N., Hoivik N., Nguyen H. V., Roy A., Aasmundtveit K. E. (2021). Investigation of seal frame geometry on Sn squeeze-out in Cu-Sn SLID bonds. 2021 23rd European Microelectronics and Packaging Conference & Exhibition (EMPC). Gothenburg, Sweden, 2021, pp. 1-5, Doi: 10.23919/EMPC53418.2021.9584990

My Contribution: Assisted in formulating the idea. Manufactured and tested all samples. Analyzed results with the assistance of supervisors. Main author.

Investigation of seal frame geometry on Sn squeeze-out in Cu-Sn SLID bonds

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Abstract— Cu-Sn SLID is an increasingly popular bonding technique with applications in such as hermetic sealing of microbolometers. A moderate bonding pressure is necessary to compensate for the surface roughness of the electroplated layers and to break the Sn oxide layer, thereby reducing the risk of voiding. However, such bonding pressures increase the risk for Sn squeeze-out during the bonding process, which has the potential to destroy MEMS or ROIC devices. To prevent this potential issue, an alternative bondline geometry consisting of 3x50µm wide bond rails and 25µm wide gaps was manufactured and compared to a continuous 200µm bondline by using non-destructive IR imaging, cross-sectional microscopy, and die-shear testing. High shear strength values of 31±9MPa and 43±18MPa were obtained for continuous and railed seal frames respectively. The Sn squeeze-out distance beyond the intended bondline was, on average, reduced by 60% when the railed geometry is employed. A reduction in peak squeeze-out distance from 188µm to 54µm was also observed.

Keywords—SLID, Cu-Sn, squeeze-out, MEMS packaging, seal frames, bondline.

I. Introduction

Cu–Sn Solid Liquid Interdiffusion (SLID) bonding is an attractive process for MicroElectroMechanical Systems (MEMS) packaging due to its high bond-strength, high hermeticity, and wafer-level compatibility [1]. SLID bonding is performed by placing a low melting point metal (LMM), in this case Sn, in-between two layers of high melting point metal (HMM), in this case Cu (see Fig. 1). Heating the system to above the melting point of the LMM results in melting of the LMM, dissolution of the HMM into the melt, followed by nucleation and isothermal solidification of InterMetallic Compounds (IMCs). The growth of IMCs then occurs via solid-state diffusion of HMM across IMCs and consumption of LMM [2]. When all the LMM is consumed, the result is a solid bond consisting of the HMM and IMCs, which both have a higher melting point than the LMM. For a Cu-Sn system, the most common target IMC is Cu_3Sn due to its high fracture toughness, high corrosion-resistance, high melting temperature, and thermodynamic stability [3].

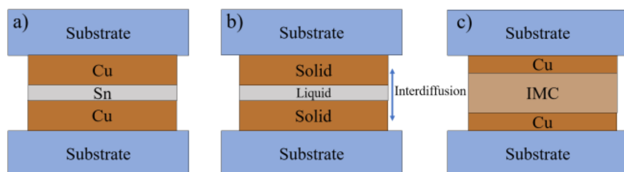


Figure 1: A simplified model of a Cu-Sn SLID bond before (a) during (b) and after (c) the bonding process is performed

A challenge in SLID bonding is finding a balance between bonding pressure, and the squeeze-out of the LMM. Because IMC formation starts at temperatures below the melting point of the LMM, a sufficiently thick layer will ensure pure LMM at the bonding interface when its melting point is reached during the bonding process. Without it, there will be no liquid phase, which is critical to compensate for surface roughness and avoid voids [4]. Moreover, a high enough bonding pressure is required to help reduce voiding by breaking the Sn-oxide layer and compensating for surface roughness[5].

A high bonding pressure tends to squeeze out LMM. Squeezed-out metal tends to form droplets extending past the intended bond area which and therefore has the potential to destroy MEMS devices and/or short-circuit electronics. Also, weakly adhered droplets may break off from the bond line after the package has reached the consumer, meaning the device may pass initial testing, but fail critically during operation [6].

A popular application of Cu-Sn SLID is hermetic sealing of microbolometers, accelerometers, and gyroscopes, which frequently require a vacuum to operate [7]. Packaging of these components is often done by electrodepositing a seal frame of Cu and Sn around the device on the substrate- and cap wafer aligning the two wafers and bonding them in a vacuum, resulting in a package that could potentially maintain this vacuum for over a century [8]. To reduce squeeze-out in unintended areas, earlier work [3, 8, 9] has demonstrated the use of one continuous seal frame bonded to a substrate with 3 smaller bondlines (see Fig. 2 b) to reduce squeeze-out in unintended areas. However, the earlier studies did not quantify the effect the bondline pattern had on squeeze-out and/or bond-strength. In this paper, we further investigate this type of bond geometry by quantifying the differences in terms of bond strength and squeeze-out between a 200µm wide continuous bondline and a bondline with a 3x50µm wide rails with 25µm gaps, as can be seen in Fig. 2 a and b respectively.

II. EXPERIMENTAL

A. *Seal frame stress simulations*

Simulations of the shear-force induced stresses in the two different bond-line geometries were performed in the Finite Element simulation software COMSOL Multiphysics. Because the ratio between the lateral dimensions and the height of the bond is very large, a 2D simulation of bondlines is chosen. Cross-sections of seal frames with identical geometries to the test vehicles seen in Fig. 2 were constructed, given the material properties of Cu_3Sn, and set to be the joint between two Si-chips. The Youngs modulus (E) and Poisson's ratio (ν) of Cu_3Sn were set to 108.3 GPa and 0.299 respectively [10]. The density (ρ) of Cu_3Sn was the default value available in COMSOL material library, i.e. 8900 kg/m^3. For silicon, E, ν and ρ were taken as 170 GPa, 0.28 and 2329 kg/m^3 respectively from COMSOL material library. The joint thickness is set to be 10µm while the Si chips are given the dimensions of 1000µm x 400µm each. The bottom silicon chips are given a fixed boundary condition and the top silicon chips are subjected to an identical shear force of 200 000N/m2. The schematic of the simulation model is presented in Fig. 3.

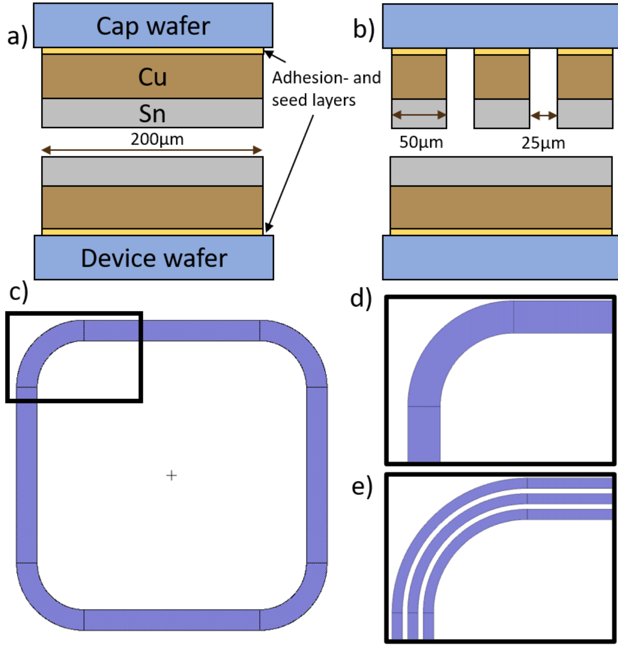


Figure 2: Model of bondlines used in this article. a) Cross-section of continuous bondline/seal frame. b) Cross-section of railed bondline/seal frame, c) top-down view of an entire seal frame with continuous bondline. d) sectional top view of continuous bondline and e) with railed bondline.

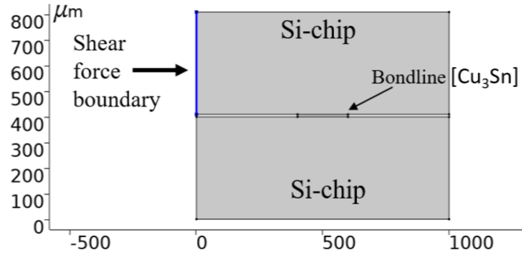


Figure 3: Schematic of FE simulation with continuous bondline.

B. *Sample preparation:*

Four 100mm oxidized Si wafers were sputtered with a 100nm TiW barrier/adhesion layer followed by a 100nm Au seed layer. Alignment marks and dicing marks were then etched on the backside of the wafers by a PlasmaPro 100 Cluster DRIE machine from Oxford Instruments using a patterned layer of photoresist as a mask.

The wafers were electroplated with 4µm Cu and 2µm Sn consecutively through a patterned layer of photoresist. The Cu plating was performed with a DMK Maroon 2100 acidic Cu-bath and a current density of 5mA/cm^2 and Sn plating was performed with a DMK Dekatinn 19 acidic Sn-bath and a current density of 10mA/cm^2. One set of test vehicles consisted of 2 wafers with continuous bondlines while the other set consisted of a continuous and a railed bondline.

After electroplating, the Au seed layer and TiW barrier/adhesion layer were removed by wet-etching by a Potassium Iodide and Hydrogen Peroxide solution respectively. The wafers were aligned using an EVG620 Mask Aligner and bonded in an EVG501 Wafer Bonding System at 280°C for 30 min (see Fig. 4). The temperature ramping rate is approximately 10°C/min and the whole process takes place under a 10^{-3}mbar vacuum. In these experiments, a bonding pressure of 15MPa was applied right after the dwell step and kept until the wafers were fully cooled.

The wafers are diced into individual dies using a Disco Automated Dicing Saw 3220.

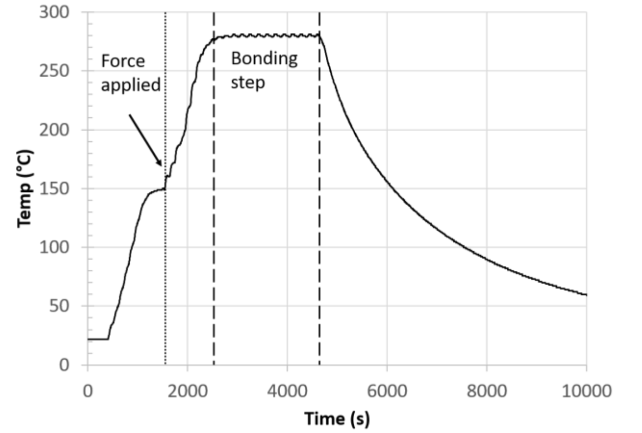


Figure 4: Bonding temperature profile exported from wafer bonder with the bond step and the point where pressure is applied indicated.

C. *Characterization:*

To prepare them for cross-sectional imaging, samples were molded in epoxy and subsequently grinded with SiC and polished with a solution 3µm diamond solution followed and finally with a 1µm solution. Imaging was performed by a Carl Zeiss Jena Neophot 32 optical microscope and a Hitachi SU 3500 SEM with an EDS module for material characterization.

All dies were inspected with a Pixelink PL-B74EF IR-Camera. Since the samples show a high degree of similarity, a single die from each wafer was chosen for complete mapping. The whole seal frame was photographed, and the resulting images were stitched together manually. A region was selected and the width of the bond frame was then measured at seven points for each die to quantify the amount of squeeze-out. The mechanical strength of the SLID bonded samples were measured by destructive die shear testing of 6 dies from each set of wafer-bonds. This was done by a Delvotec 5600 bond tester with a test speed of 100µm/s and a shear height of 60µm above the bottom die. The fracture surfaces were studied using a Leica DM3 XL optical microscope and a DEKTAK 150 profilometer.

III. RESULTS:

A. *Seal frame stress simulations:*

Fig. 5 shows resultant plots of the simulated von-mises and first principal stress on the seal frames.

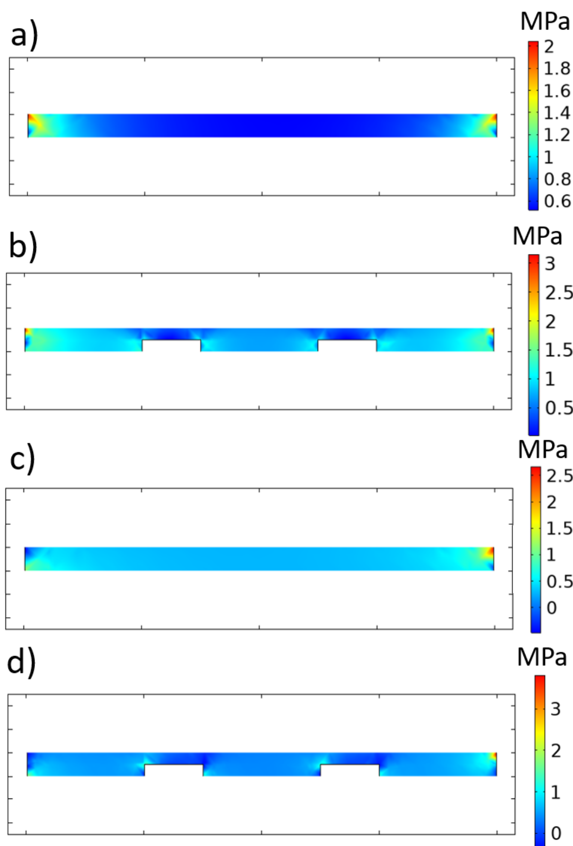


Figure 5: FE simulation results: Von-mises stress in (a) a continuous- and (b) a railed bondline. First principal stress in (c) a continuous- and (d) a railed bondline

The maximum first principal stresses are 2.67MPa and 3.81MPa for the continuous and railed bondline respectively. The peak von-mises stresses are 2.05MPa and 3.15MPa for the continuous and railed bondline respectively. These initial results indicate the two bondline geometries have similar mechanical rigidity, which means the difference in risk of crack initiation and propagation in the bondline is insignificant. Thus, the simulations suggest that the railed seal frames could offer room to accommodate excess Sn squeeze-out while maintaining similar bond integrity.

B. *Squeeze out analysis:*

From the infrared (IR) images and cross-sections, a clear difference in squeeze-out can be observed between the continuous and the railed samples (see Fig. 6-8). In the continuous samples, an uneven bondline is pervasive, indicating Sn has squeezed-out beyond the original bondline as can be seen in Fig. 6 b. For the railed samples, however, the bond frames are more uniform in width. Some metal was observed outside the bondline at selected areas in the railed

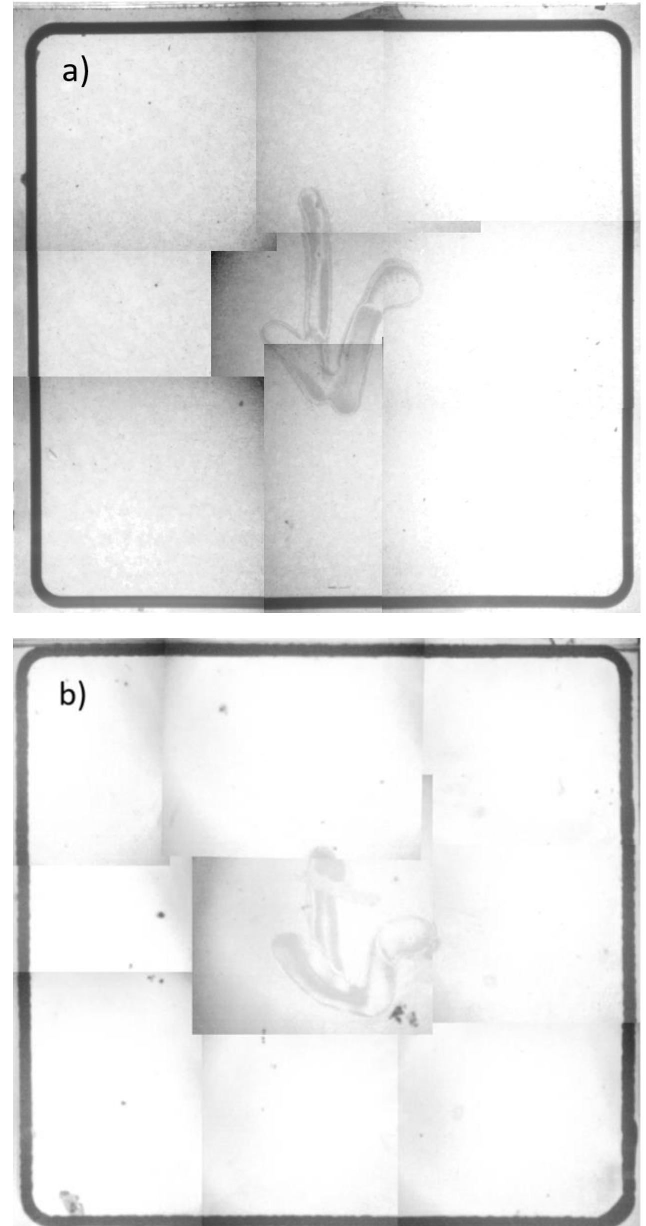
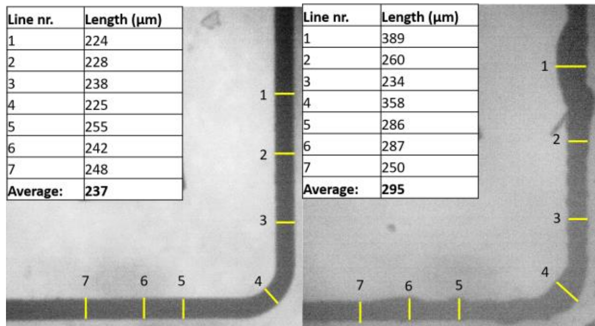


Figure 6: Stitched IR images of a full die with railed bond frame a) and continuous bond frame b).

samples (see the top line of the top image in Fig. 6 a). Upon further inspection after die-shear testing, however, this was found to be un-etched seed- and adhesion layer, not Sn squeeze-out.

Measurements of bond frame widths are shown in Fig. 7. Since the electrodeposited bondline is 200µm wide, any extension beyond this can be assumed to be Sn that has been squeezed-out during the bonding process. This means that there is a 60% reduction in average Sn squeeze-out distance, from 95µm to 36µm for the continuous samples and the railed samples respectively. It should also be noted that in one area, a width of 388µm is measured. Since the squeeze-out could be protruding at both or either side, this means that the squeeze-out extends a minimum of 94µm and potentially 188µm outside the intended bondline. On the other hand, the widest measurement in the sample with railed bondlines is 254 µm, which means a maximum potential squeeze-out of 54µm.



Line nr.	Length (µm)
1	224
2	228
3	238
4	225
5	255
6	242
7	248
Average:	**237**

Line nr.	Length (µm)
1	389
2	260
3	234
4	358
5	286
6	287
7	250
Average:	**295**

Figure 7: Close up of bondline corner with railed- (left) and continuous bondline (right) with location of width measurements indicated and inset showing measurement results.

The cross-sectional micrographs presented in Fig. 8 a and b also show that the rails work as intended. Sn has squeezed-out and filled the cavities between the rails, leading to less Sn squeeze-out in unwanted areas, such as inside the package. This leads to more Cu being consumed on the top wafer in these regions between the rails. SEM and EDX analysis show that all Sn has converted to IMCs with most of the squeeze-out, both in the cavities and on either side, consisting of only Cu_6Sn_5, instead of Cu_3Sn. The reason this has not converted to Cu_3Sn is because sufficient Cu was not able to diffuse to these areas in the given bonding time.

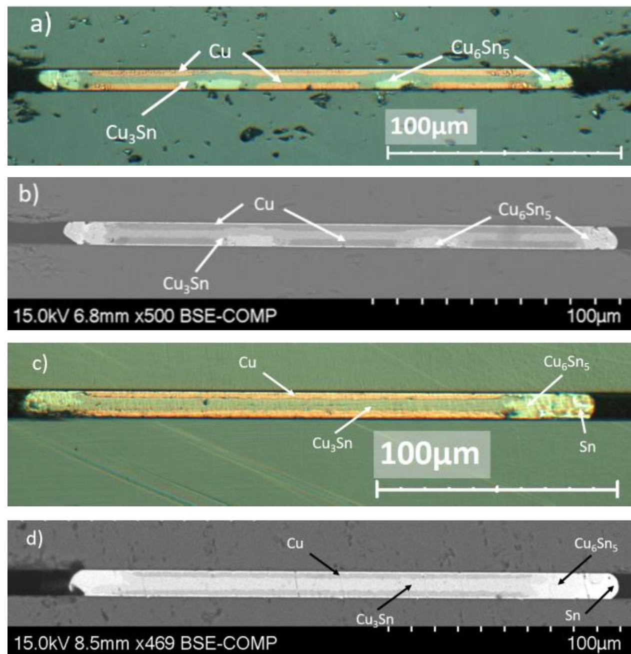


Figure 8: Cross-sectional micrographs of (a) a railed- and (c) a continuous bondline . SEM images of (b) a railed- and (d) a continuous bondline.

The cross-sectional micrographs of the continuous bond frames are shown in Fig. 8 c and d. These images show a higher degree of squeeze-out on either side and even pure Sn remaining at the far edges of the squeeze-out, which is due to the same reasons mentioned in the previous paragraph.

All micrographs show good alignment, further indicating that any width increase in bondline is likely due to Sn squeeze-out.

C. *Die shear testing*

The die shear testing results are presented in Fig. 9. An average die shear strength of 31±9MPa for the continuous bond frames and 43±18MPa for the railed bond frames is found. This is higher than the MIL-STD-883E standard of 12MPa and higher than other values presented in the literature for Cu-Sn SLID (13-20MPa) [9, 11, 12].

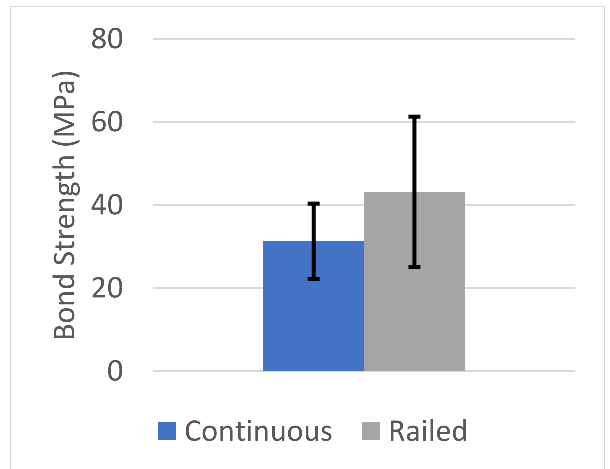


Figure 9: Comparison of average die shear strength for samples with continuous and railed bondlines.

The visual inspection and profilometer measurements of fracture surfaces showed failures at the interface of silicon and TiW adhesion layer, at the original bond interface, and fracturing of the silicon cap wafer. No clear pattern of which failure mechanism is most dominant could be distinguished.

IV. Discussion

Full IR-image results for a single die and squeeze-out measurements at seven locations per wafer pair have been presented. It is clear from these images that the squeeze-out amount and -distance is reduced by patterning the seal-frames with rails. A representative was selected in each of the sample sets and point measurements provided insight into the average and peak squeeze-out distance. In the future, area measurements and comparisons of an entire seal frame could

provide more accurate quantification of the squeeze-out reduction that the railed seal-frames provide.

There is a large difference in the average die shear-strength values of the two sample sets. When considering the standard deviation, the uncertainty in our measurements is higher than this difference. This suggests that parameters other than bondline geometry, such as adhesion layer strength and interface voids as a result of impurities from electroplating, could have a larger effect on the final bond strength. The comparable bond strength for the two samples is also supported by our simulation.

The simulation did not account for the Sn solidifying in the gaps of the railed bondline (see Fig. 5 and 8). These IMCs are not bonded to the other side, since the seed- and adhesion-layer has been etched away at these areas, but could potentially help distribute some of the stresses built up next to these areas during shear-testing.

Finally, while this study is on the Cu-Sn SLID system, this bondline geometry should provide the same benefits to other SLID systems, especially those using Sn as the LMM, for example, Au-Sn and Ni-Sn.

V. Conclusion

An alternative seal-frame geometry with potential applications in hermetic sealing of MEMS has been demonstrated. The seal-frame design was comprised of 3 rails with 50µm width and 25µm gaps on one mating partner, and a continuous 200µm wide seal-frame on the other. When compared to a conventional bondline with a continuous 200µm wide bond frame on both sides, a 60% reduction in average squeeze-out distance is observed for the railed sample. Peak squeeze-out distance was also reduced from 188µm to 54µm outside the intended bondline when the railed seal-frame is employed.

A high average bond-strength (31±9MPa) was measured for the continuous samples, with the railed samples showing a higher average bond strength, but with a larger deviation (43±18MPa). From these initial results, we conclude that the two bondlines have comparable bond strength. This conclusion is backed up by our simulation results.

Furthermore, since identical parameters were used for all samples, this squeeze-out improvement comes with no extra steps or increased complexity in the fabrication process.

More experiments are underway to further quantify the effect railed bondlines, have on squeeze-out and bond strength. Studies will also be conducted to investigate the impact these bondlines have on the hermeticity of the final package. Finally, these types of studies will also be conducted on other bondline geometries.

Acknowledgments

This work was carried out with funding by the ECSEL Joint Undertaking (JU) project APPLAUSE under grant agreement No 826588. The JU receives support from the European Union's Horizon 2020 research and innovation program. The Research Council of Norway is also acknowledged for its support to APPLAUSE and the Norwegian Micro- and NanoFabrication Facility (NorFab, project number: 245963/F50).

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10.3 Article 3:

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My contribution: Developed new seal frame geometries. Manufactured and tested all samples. Upgraded IR-imaging set-up at USN. Analyzed results with the assistance of supervisors. Main author.

Squeeze-out and bond strength of patterned Cu-Sn SLID seal-frames

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Abstract

Control of Sn squeeze-out due to the presence of liquid phase and bond pressure is important in Cu-Sn SLID bonding. This work studies the impacts of seal-frame design for limiting this squeeze-out. Three alternative seal-frame geometries are evaluated and compared to a traditional continuous seal-frame with respect to squeeze-out and shear strength. The alternative designs include open spaces to accommodate squeeze-out and are: 1) One mating partner with 3x50 µm wide rails and 25 µm gaps. 2) Previous geometry with 50 µmx200 µm square hatches added across the rails with a pitch of 75 µm. 3) One 150 µm wide mating partner leaving 25 µm of open area at either side. For all geometries, the other mating partner is a continuous 200 µm wide seal-frame. A 46% reduction in squeeze out could be seen in the bond with asymmetric bonding partners, but no significant reduction was measured for the geometry with rails and the geometry with hatches. The hatched, railed and asymmetric seal-frames displayed shear strengths of 57±13 MPa, 80±18 MPa, and 48±30 MPa respectively, which was significantly higher than that of the traditional continuous bonds which only measured 17±7 MPa. Fracture surface analysis showed no correlation between fracture modes and differences in shear strengths.

1. Introduction

Cu-Sn Solid Liquid Interdiffusion (SLID) is a bonding technique based on the intermetallic (IMC) formation between Cu and Sn. Due to advantages such as low-cost, high hermeticity, wafer-level suitability, high bond strength, and CMOS compatible bonding temperature [1], it is especially well suited for hermetic sealing of MEMS like infrared (IR)-microbolometers.

Void formation in seal-frames is a concern when performing SLID bonding. Voids lower bond strength, but also lowers hermeticity, conductivity, and reliability [1, 2].

Two important factors in reducing voids in Cu-Sn SLID is the application of bonding pressure and Sn thickness. The bonding pressure improves the quality of the bonds by breaking the Sn oxide, and by compensating for any roughness in the bonding partners. Higher bond pressures yield stronger bonds with less voids [2]. A sufficiently thick Sn layer is required to ensure liquid Sn when the bond temperature is reached. This is due to InterMetallic Compound (IMC) formation starting at room temperature, but also because the growth of IMCs is scalloped, not planar [3]. These IMC scallops act like spacers which may prevent the bond from developing evenly which may result in voids [3].

Since the Sn is in liquid phase for a period during the bonding, the bond force will cause some of the Sn to squeeze out past the intended bondline [4, 5]. The amount of squeeze-out is related to the bond force magnitude and has the potential to short-circuit electronics or form weakly adhered droplets which may detach during operation, causing a critical failure after the product has reached the consumer [4].

Since higher bonding pressure yield stronger and more reliable bonds, but cause more squeeze-out, a balance must be struck. Our work attempts to shift this balance by presenting seal-frame geometries that accommodate this squeeze-out, allowing for higher bond force. Three geometries are presented and

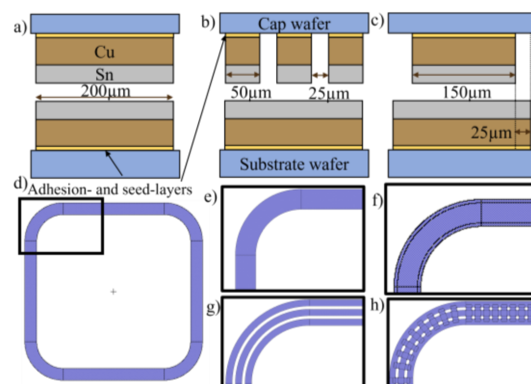

Fig. 1: Side view of (a) continuous, (b) railed and (c) asymmetric seal-frames. Side view of hatched seal-frame not included, since it will be identical to a) or b) depending on where the cross-section is made. Top view of all seal-frames bonded in this article: Continuous- (d & e), asymmetric- (f), railed- (g) and hatched seal-frame (h)

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compared to a traditional 200 µm wide continuous seal-frame (see fig. 1) with respect to squeeze-out amount and bond strength.

The seal-frame geometry with three 50 µm wide parallel rails is based on previous work [4-6]. This geometry has previously shown potential to reduce void formation by allowing Sn to fill the gaps between the rails (see fig 1 b & g). The next seal-frame utilizes this same geometry, but ads 50 µm by 200 µm cross-hatches with a 75 µm pitch (see fig 1 h). The goal of these cross-hatches is to increase the bonded surface area and thus increase the shear force the final bond will withstand, while still leaving some room for squeeze out.

The last geometry is a 150 µm seal-frame center-aligned on the 200 µm bondline (see fig 1 c & f). This leaves a bonded area identical to that of the railed geometry, but with the openings on either side, meaning the squeeze-out could have an easier time finding them.

This paper presents the results of a study on the impact of these geometries on the squeeze-out and bond strength of the seal-frames.

2. Experimental

2.1. Sample preparation

100 mm Si wafer pairs with a thickness of 500 µm were thermally oxidized before an adhesion-layer of 100 nm TiW and a seed-layer of 100 nm Au were deposited by sputtering. Backside alignment marks were then produced on the wafers by photolithography and a PlasmaPro 100 Cluster DRIE machine from Oxford Instruments. Arrays of seal-frames with different geometries are then patterned on separate wafers using photolithography. The seal-frames were then patterned on the wafers by another photolithographic process. This photoresist served as a mask in the subsequent electroplating process.

For the electroplating, a DMK Maroon 2100 acidic Cu-bath and a current density of 5 mA/cm^2 were used for Cu, while a DMK Dekatinn 19 acidic Sn-bath and a current density of 10 mA/cm^2 were used for Sn. To promote even deposition, pulsed reverse plating was used, and the wafers were rotated 90 ° at approximately one-quarter of the plating time. Metal growth was measured at multiple locations during and after electroplating by a DEKTAK 150 profilometer. The wafers were all plated with approximately 4 µm Cu and 2 µm Sn. After the electroplating is completed, the excess TiW and Au is etched by a Hydrogen Peroxide- and a Potassium Iodide solution respectively using the plated Cu and Sn as a mask.

Wafer pairs are then aligned in an EVG620 Mask Aligner and loaded into an EVG501 Wafer Bonding System. The temperature profile seen in fig. 2 is then applied. Details on the temperature profile are

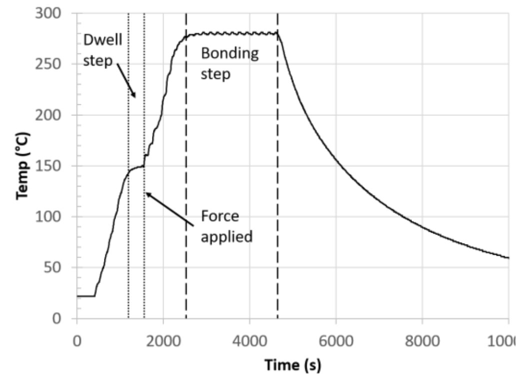

Fig. 2: Temperature profile with indicated dwell step, point of force application and bond step (taken with permission from [6])

presentent in our previous work [6]. While the seal-frame arrays are patterned on separate wafers, the fabrication process and bonding parameters, such as temperature profile and bonding pressure, are identical. Finally, the wafer pairs are cut into individual dies using a Disco Automated Dicing Saw 3220.

2.2 Squeeze out analysis

Because silicon is transparent to IR and metal is not, the seal-frames of the dies can be inspected non-destructively by IR-microscopy, in our case a Pixelink PL-B74EF IR-Camera with an Optem 70XL Zoom Lens. ImageJ software is used to extract and analyze the seal-frame area. The calculated area of an idealized seal-frame with no squeeze-out and perfect alignment is then subtracted from the measured area and the resulting difference is the area caused by squeeze-out and/or misalignment.

Two dies from each wafer pair were also molded in epoxy and subjected to a grinding and polishing protocol using SiC paper and diamond suspension solutions. This was done to observe cross-sections of the bonds and measure misalignment. Optical microscopy was performed with a Carl Zeiss Jena Neophot 32.

2.3 Shear strength testing and fracture analysis

Five dies from each wafer pair were subjected to die shear tests using a Nordson Dage 4000Plus bond tester. Test speed was 100 µm/s and the shear height was 60 µm above the substrates. The tests were performed with a shear tool slightly wider than the dies, capable of rotation to ensure parallelity between the tool surface and die edge.

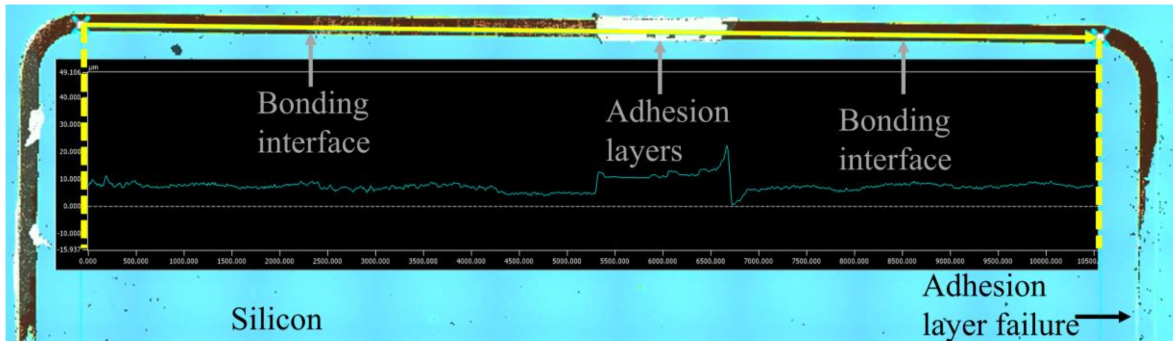

Fig. 3. Confocal microscopy image of half a die with various fracture surfaces indicated. Inset shows measured height difference at fracture surfaces along the scan line (solid yellow).

After die shear testing, 2 fractured dies of each type is selected at random and scanned in a Keyence VK-X250/260K 3D Laser Scanning Confocal Microscope. During the scans, 3 failure modes are detected along the bondlines: 1) Failure at the Silicon-Adhesion layer interface, 2) Failure at the original bonding interface, and 3) Fracture in the silicon bulk (see fig 3.). The area fraction of each failure mode is calculated using measured height area compared to the measured total area of each seal-frame.

3. Results

3.1. Misalignment measurements

If the two bonding partners are misaligned, the seal-frames will appear wider when viewed by the IR-microscope from above. Cross-sections of the seal-frames are therefore analysed to measure the misalignment in the x and y direction. Some cross-sections are presented in fig. 4. and the measured misalignment is presented in table 1.

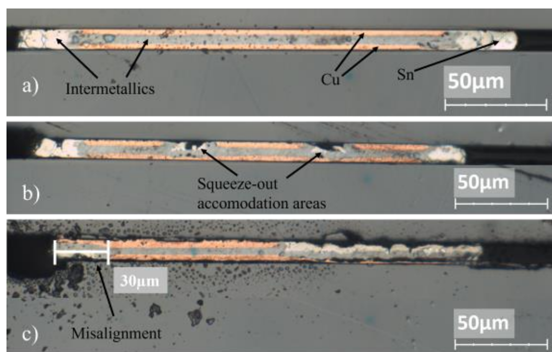

Fig. 4: Cross-sectional micrographs of a) continuous, b) railed, c) hatched and d) asymmetric samples. Note the unfilled areas in b) and measured misalignment in c).

3.2. Sn Squeeze-out analysis

Optical micrographs of cross-sections and representative IR-micrographs of the seal-frames are presented in fig. 4 and fig. 5 respectively. The continuous seal-frames display even seal-frames and some areas with more squeeze out. Point measurements in the IR-images and cross-sections both indicate squeeze-out of about 20-30 µm along the bond on either side, with a few areas showing more (see insets in fig. 5a).

For the hatched samples, even seal-frames are observed, but wavy lines with the distance between peaks corresponding to the pitch of the cross-hatches, are present throughout the frame (see inset in fig. 5 b).

Table 1: Misalignment for geometries in each direction

Geometry & direction	Misalignment (µm)
Continuous (Y)	3
Continuous (X)	1
Railed (Y)	2
Railed (X)	3
Hatched (Y)	4
Hatched (X)	1
Asymmetric (Y)	30
Asymmetric (X)	8

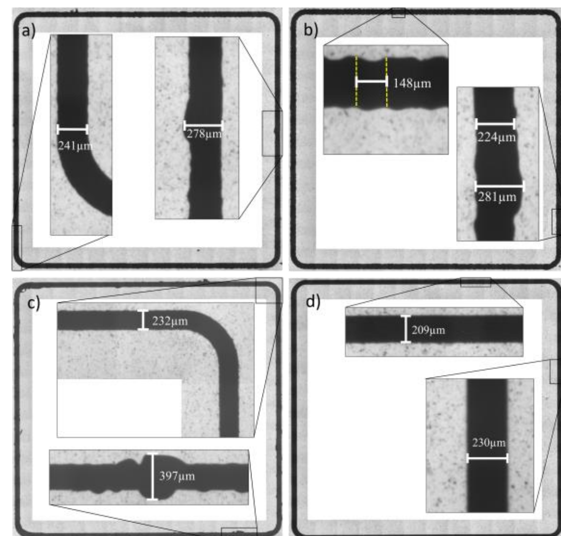

Fig.5: Representative IR-images with insets and point measurements of a (a) continuous, (b) hatched, (c) railed and (d) asymmetric seal-frame.

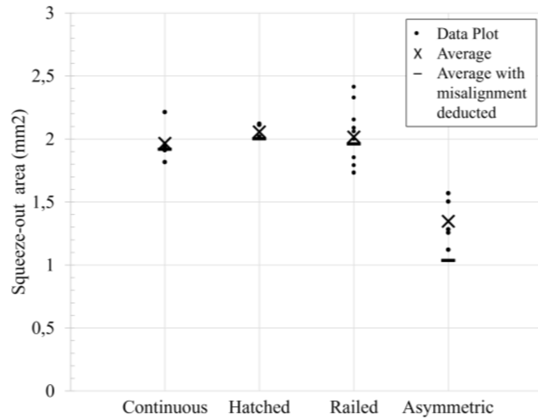

Fig. 6. Area comparison of all 4 geometries

The railed samples show a large degree of variation, with some areas showing thick blobs protruding from the seal-frame. The cross-sections also show that the area between the rails are not filled completely.

For the asymmetric samples, we observe no apparent squeeze out in the bondlines. However, both the cross-sections and the IR-images show a large amount of misalignment.

The compiled data for the area measurements of the seal-frames are presented in fig. 6. The extra area due to squeeze-out and misalignment for the continuous, hatched, railed and asymmetric seal-frames are 1,96 mm^2, 2,06 mm^2, 2,02 mm^2, and 1,35 mm^2, respectively. These results show an insignificant difference in Sn squeeze-out when employing railed or hatched geometries, compared to traditional continuous seal-frames. The asymmetric seal-frames display a smaller seal-frame area, with a reduction of 31%.

To consider the area added by misalignment, the misalignment in the x and y direction from table 1 was used to calculate and subtract the extra area. As can also be seen from fig. 6 this does not change the differences between the area of the seal-frames significantly, except for the asymmetric samples. After controlling for misalignment, the asymmetric samples demonstrate a 46% reduction in extra area.

3.3. Shear strength measurement

The results of the shear strength tests are presented in fig. 7. The average shear strength of the continuous, hatched, railed and asymmetric seal-frames are 17±7 MPa, 57±13 MPa, 80±18 MPa, and 48±30 MPa respectively.

3.4 Fracture Surface Analysis

The fracture surface analysis results are presented in table 2. No correlation could be established between fracture surface fraction and bond strength.

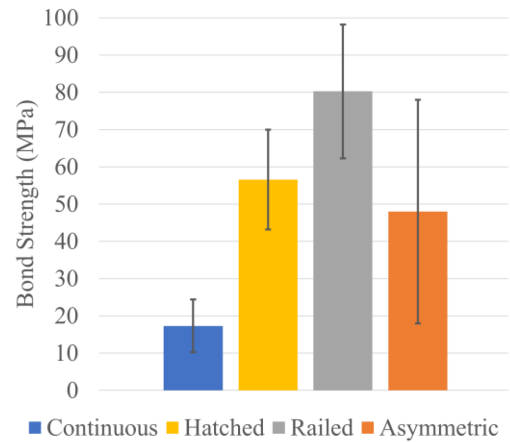

Fig. 7. Shear strength results for all 4 geometries bonded in this article

The sample with the highest recorded shear strength, Railed 2, has fracture surfaces very typical to the rest of the samples. The samples with highest amount of failure at adhesion level, Railed 1 and Hatched 2, show average shear strength values. The sample with the most fractures are at the bonding interface, Continuous 1, demonstrates low shear strength. Samples with fractures in the silicon, Continuous 2, Hatched 1, and Asymmetric 1, demonstrate low and average shear strength.

Table 2: Fracture surface fraction and bond strength

Seal-frame pattern	Adhesion layer failure (%)	Bond interface fracture (%)	Silicon fracture (%)	Bond strength (MPa)
Continuous 1	68	32	0	24.3
Continuous 2	85	6	9	7.6
Railed 1	92	8	0	67.1
Railed 2	86	14	0	110.7
Hatched 1	88	9	3	58.9
Hatched 2	93	7	0	52.7
Asymmetric 1	85	14	1	29.1
Asymmetric 2	84	16	0	17.0

4. Discussion

Area measurements and calculations for more than 20 dies have been presented and indicate insignificant decrease in squeeze-out when applying railed- or hatched seal-frames, compared to a traditional continuous one. The asymmetric samples show a decrease of 46% after accounting for misalignment. The cross-sections and IR-images are in good agreement.

In our previous work, there was a clear decrease in squeeze-out for samples with railed geometry when compared to the samples with continuous seal-frames

[6]. It is likely that some of the differences in results stem from the quantification method. Previously, only point measurements were made in a representative image, while in this study, the area of multiple dies was characterized and compared.

An additional contribution to the difference between findings could be that in the earlier study it appeared from the cross-sectional micrographs in that the areas between the rails were completely filled, while in this work they do not (see fig. 4). It is possible that impurities such as S, Cl, O, and C, are deposited during the electroplating process [1], which could hinder the Sn from flowing in these areas of the bond. Some of the liquid Sn could then be forced to flow outside of the bond, thus causing the blobs seen in the IR-images (see fig. 5c). Also, since the IMCs do not grow isometrically, but in scallops [3], the solidified IMCs could prevent the Sn from flowing in the designated areas, which would also cause blobs.

This is supported by the fact that no decrease is seen in the hatched samples, which also have squeeze-out areas inside the bond. The asymmetric bonds, on the other hand, have the designated squeeze-out areas on the outside of the frame. This means that only two areas where the Sn is able to flow are intended to accommodate squeeze-out.

It is worth noting that the asymmetric bonds do not trap the Sn inside the seal-frame, meaning the squeeze-out could get knocked loose during the lifetime of the device. The squeezed-out Sn in the asymmetric samples does, however, adhere to at least two sides, which decreases the likelihood of this issue.

In our previous study [6], railed and continuous samples were also shear tested. Higher average measured shear strength was obtained for the railed samples, compared to continuous ones. The large uncertainty in the measurements, however, meant we could not conclude they were more than similar in bond strength. Those results were obtained using an older shear testing machine without parallelity compensation and a shear head narrower than the die, meaning the current results are more trustworthy. Although the results cannot be directly compared, for the reasons stated above, they do display the same trend, which reinforces the findings of this paper.

There is now evidence that samples with intentional openings in the middle of the seal-frames show higher shear strength than continuous frames. While this may seem counterintuitive, similar techniques of “stop holes” or “defense holes” has been demonstrated in the literature. Miyagawa et. al. [7] for example introduced defense holes in a plate and saw an increase in the number of fatigue cycles the plate could withstand. They further propose a mechanism where these holes or gaps reduce the crack-tip stress concentration, thus retarding or arresting the crack propagation. This mechanism is supported by the fact that as the gaps inside the bond decrease from railed- to hatched- to continuous geometry, the shear strength decreases.

5. Conclusion

Three alternative seal-frame geometries have been presented and compared to a traditional continuous seal-frame with respect to squeeze-out and bond strength. No reduction in seal-frame area could be observed in samples with railed or hatched seal-frames, indicating that there is no meaningful reduction in squeeze-out. Samples with asymmetric bonds, however, showed a reduction of 46%.

An increase in shear strength is observed for all samples compared to the continuous bond. It is proposed that the intentional openings in the bondline acts as defence holes. This mechanisms fits well with the observed reduction in shear strength as the amount of gaps in the bondline decreases.

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10.4 Article 4:

Papatzacos P. H., Akram, M. N., Hector, O., Lemarquis, F., Moreau, A., Lumeau, J., Øhlckers, P. (2022). Temperature Resistant Anti-Reflective Coating for LWIR imaging on Si-wafer. Accepted by Heliyon. To be published in Volume 9, Issue 5, in May 2023, https://doi.org/10.1016/j.heliyon.2023.e15888

My contribution: Assisted in formulating the idea. FTIR measurements and thermal cycling of all samples. Analyzed results. Communication with Institute Fresnel. Main author.

Temperature Resistant Anti-Reflective Coating for LWIR imaging on Si-wafer

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ABSTRACT:

A micromachined Si lid, sealed by CuSn SLID bonding is a promising approach for hermetic sealing of microbolometers for use in low-cost IR cameras. However, since ~30% of long-wave infrared light is reflected at an uncoated single Si-air interface, anti-reflective treatments are required. Traditional anti-reflective coatings are inapplicable since CuSn SLID bonding requires heating to about 270°C and these multi-layer coatings fail due to differing coefficients of thermal expansion (CTEs). For this purpose, an anti-reflective coating that maintains its anti-reflective properties after being heat-cycled to 300°C has been developed. This coating was developed using a simple 2-layer structure composed of ZnS and YF_3 and deposition at 100°C. The development process has also been described in this paper. The final sample with a one-sided coating shows a 15% average increase in transmission in the 8-12µm wavelength range compared to an uncoated wafer. The coating shows a maximum of 17% increase at 8µm, decreasing to 15% at 12µm. At 30° incidence, the coating has an average of 14% increase in transmission, with a similar trend of starting at 15% improvement and falling to ~12%.

Keywords: LWIR ARC, temperature resistant, ZnS, YF3, SLID

1 INTRODUCTION

Infrared (IR) microbolometers have been developed which, when placed in an array, result in a thermal camera with low cost and no need for active cooling. These MicroBolometer Arrays (MBAs) therefore have the potential to bring thermal cameras to new application avenues, such as thermography for quality assurance and control, automated driver assistance systems in cars and unmanned aerial aircraft systems, as well as other surveillance, security, and safety applications [1].

Packaging of these MBAs, like most Micro-Electro-Mechanical Systems (MEMS), is challenging because these devices are sensitive and have strict requirements when it comes to processing techniques, processing temperature, and vacuum operating level [1]. One promising approach for encapsulating these MBAs is to use micromachined silicon as a cap and seal the package using CuSn Solid Liquid Interdiffusion bonding (SLID) (see figure 1). Silicon is chosen due to its relatively high transparency in the Long Wave InfraRed (LWIR) region and its long history of wide implementation in large-scale production. CuSn SLID is chosen as the bonding technique due to its low cost, high hermeticity, and wafer-level compatibility.

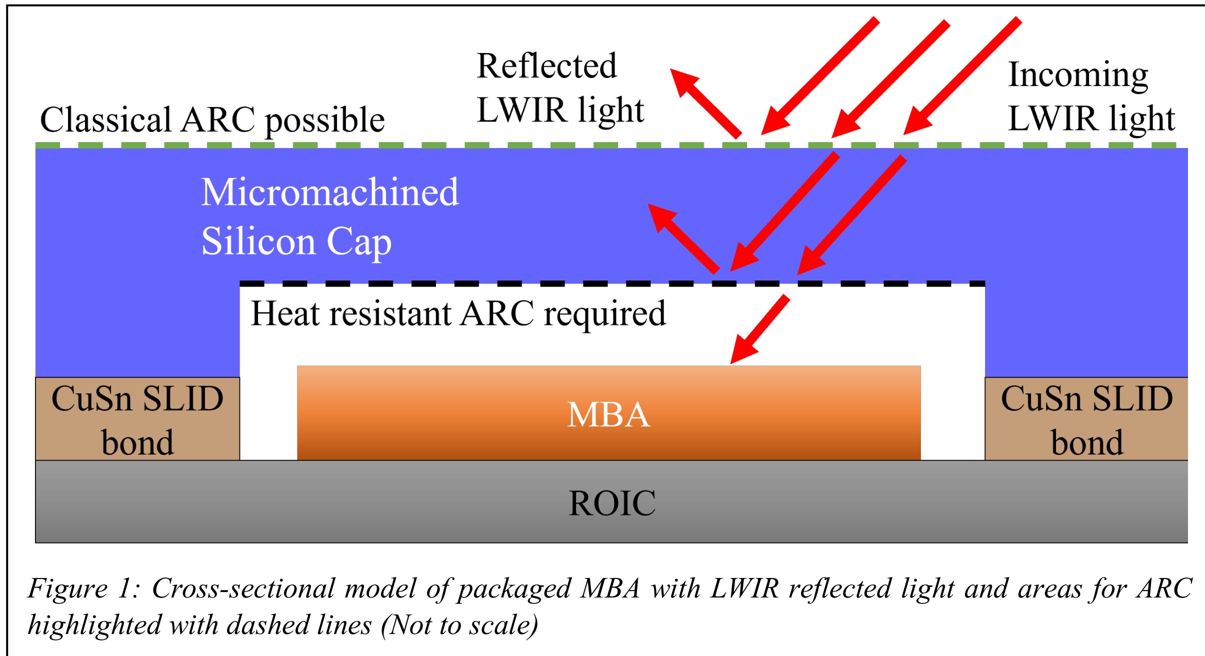


Figure 1: Cross-sectional model of packaged MBA with LWIR reflected light and areas for ARC highlighted with dashed lines (Not to scale)

CuSn SLID is a bonding technique in which Cu and Sn is deposited on the mating partners and heated to about 270°C. At this temperature, the Sn melts and interdiffuses with the Cu, forming first the intermetallic (IMC) Cu_6Sn_5 and then Cu_3Sn. After a time, all the Sn is consumed, and the final bond consists of Cu and Cu_3Sn, both of which are highly hermetic and have a melting point far higher than that of Sn (Approximately 670°C and 1000°C for Cu_3Sn and Cu respectively) [2].

Although silicon has low absorption in the LWIR range [3], Fresnel reflections remains an issue. According to Fresnel's equations, ~30% of the light will be reflected at a single Air-Si interface at normal incidences due to the large difference between the refractive indices of air and Si [4]. Since the light must traverse two such interfaces (see figure 1), some anti-reflective measures need to be taken. A common approach is to use an Anti-Reflective Coating (ARC). However, since a typical design requires 5-25 layers [5, 6], all with potentially different coefficients of thermal expansion (CTE), these coatings are sensitive to changes in temperature. In this article, we have developed an ARC capable of retaining its anti-reflective properties and mechanical integrity up to 300°C, which is a critical requirement for the coating to be used inside a package sealed hermetically using CuSn SLID, as shown in figure 1. This has been done by using a combination of fewer layers and a deposition temperature in-between room temperature and the bonding temperature.

2 DESIGN

To perform this design, we used a classical thin-film approach based on matrix formalism to calculate a simple multilayer structure that would allow for the minimizing of the reflection coefficient in the 8-12μm range for

Table 1: Composition of anti-reflective coatings

Batch 1	**Layer nr.**	**Material**	**Refr. Index**	**Thickness (nm)**	**Batch 2-4:**	**Material**	**Refr. Index**	**Thickness (nm)**
	1	ZnS	2.257	1026		ZnS	2.257	1180
	2	YF_3	1.363	1723		YF_3	1.363	1908
	3	ZnS	2.257	151				
	4	YF_3	1.363	969				
	5	ZnS	2.257	2102				
	6	YF_3	1.363	1749				
Total				**7719**				**3088**

angles of incidence ranging from 0° to 30°. ZnS and YF_3 were chosen as high and low refractive index materials respectively because they are classical infrared materials that both exhibit low absorption in the LWIR range. Two different structures were designed. First, a 6-layer anti-reflection was developed. Then, in order to limit the total stack thickness, the number of interfaces, and the bending caused by the stress and temperature dependence, the stack was eventually limited to a simple 2-layer design with formula 1.04 H, 1.04 L where H represents a ZnS quarter wave layer and L a YF_3 quarter wave layer, both at 10 µm. The refractive index at 10 µm wavelength of the ZnS and YF_3 layers are equal to 2.257 and 1.363 respectively [7]. The thicknesses of the layers are equal to 1183 nm and 1935 nm respectively (see table 1). This solution represents a compromise between minimizing

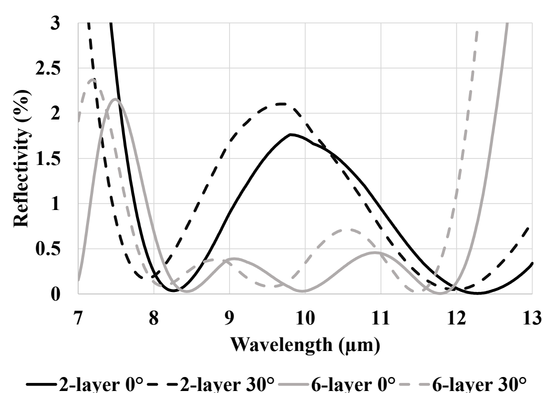


Figure 2: Simulated results of the designed coatings at 0° and 30° from Optilayer.

the total thickness and minimizing the residual reflection of the final ARC.

To verify the efficiency of the coatings, simulations were performed using the Optilayer software and the results for normal incidence and 30° incidence are presented in figure 2 below. We can see that the 2-layer coating theoretically reduces reflection to under 2% for a single air-Si interface, which is a great improvement compared to the original ~30%. Also, the 6-layer design has better overall performances than the 2-layer design, but sharper reflectance fluctuations at boundaries of the considered spectral region.

3 EXPERIMENTAL

The ARC was fabricated using a Bühler/Leybold Optics SYRUSpro 710 machine. ZnS layers were obtained from pure flakes placed in a Cu crucible while YF_3 layers were obtained from pure granules that were preliminarily melted into a Mo liner. A focused electron beam (e-beam) was used to heat the material with a typical current of a few tens of mAmp for both materials. Specific e-beam patterns were developed in order to secure uniform evaporation of the material. 100 mm diameter, 550 µm thick silicon substrates were placed about 600 mm from the crucible on a rotating calotte to achieve layers with good uniformity over the substrate aperture. Depositions were carried out at an initial pressure of about 10^{-6} mbar. Both materials were deposited at a rate of 0.3-0.5 nm/sec. The deposition rates of the layers were controlled with a quartz crystal microbalance while the thickness was optically monitored with a Bühler OMS 5000. Due to the limited spectral range of the optical monitoring system, the layers were monitored at 870 nm, i.e. far from the operating wavelength of the antireflection coating meaning that the dispersion curve of the used materials must be well known over a broad spectral range. To verify that the thicknesses had been properly controlled, the transmission spectra were measured in the visible/near IR region using a Perkin Elmer Lambda 1050 spectrophotometer after deposition, which showed very good agreement between theory and experiment.

The wafers with intact ARC were separated into multiple samples using a Disco Automated Dicing Saw 3220. Heating of the samples was done in a Gravimetric Furnace LG, LAC.

To measure the efficiency of the final ARC, a Nicolet iS50 FTIR Spectrometer was used to measure a wafer coated with the ARC. These results were then compared to an identical scan on an uncoated wafer from the same batch. Measurements were made at 0° incidence and 30° incidence using a 3D-printed mount. Cross-sections of the coatings after dicing were taken by a Hitachi SU 3500 SEM.

4 PROCESS OPTIMIZATION

The initial batch of ARC-coated wafers was composed of 6 layers (see table 1). While this batch showed great promise to lower reflection as can be seen in the Optilayer simulations in figure 2, it disintegrated quickly after heating to 300°C (see figure 4 & 5). This is likely the result of the stress induced in the layers by the CTE-mismatch between the Si wafer and the layers, which results in delamination [8]. These results lead to the 2-layer approach described below.

Few layers make the coating less susceptible to CTE-induced stress, but it is also known that ZnS has poor adhesion to Silicon. A 1-2 nm thick layer of MgO was therefore applied beneath ZnS for all designs and adhesion was confirmed by a scotch tape test.

Another important optimization turned out to be the choice of the deposition temperature of the ZnS and YF_3 layers. It was found that if a too-low temperature is used during the deposition of the ZnS and YF_3 layers, i.e. below 50°C, delamination of the layers was observed when the sample was heated up to 300°C (see Figures 3 & 5).

To overcome this challenge ZnS and YF_3 were deposited at approximately 175°C. This temperature was chosen as experience suggests that a higher temperature would cause deposition issues due to a too-large decrease in deposition rate, as suggested by Cox et. al. [9].

This run resulted in a coating that cracked and delaminated when the samples were brought back to ambient temperature and pressure (see figure 4). The reason for this cracking is, in all likelihood, the same as that for the

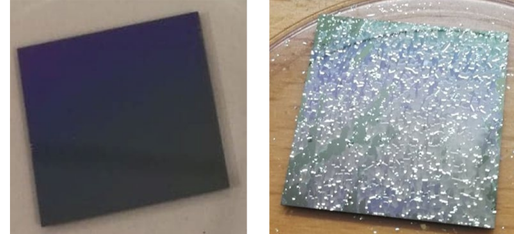


Figure 3: ARC deposited at room temperature before (left) and after (right) subjected to 300°C. Note the delamination in the heated sample.

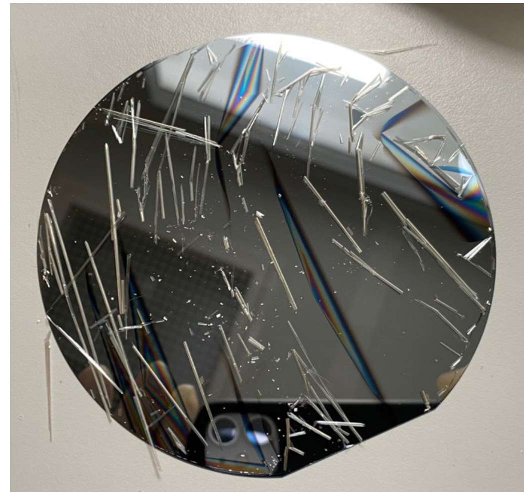
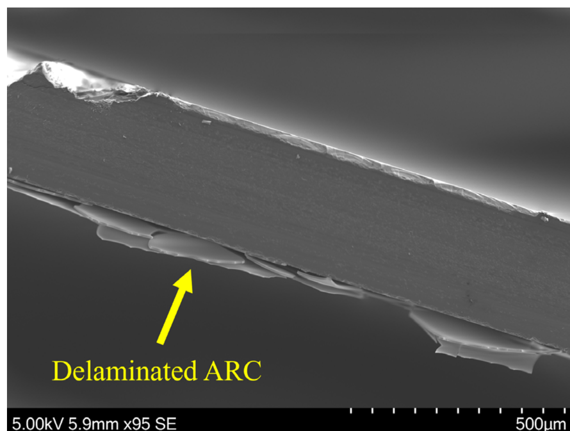


Figure 4: Example of ARC delamination at room temperature as a result of deposition at 175°C



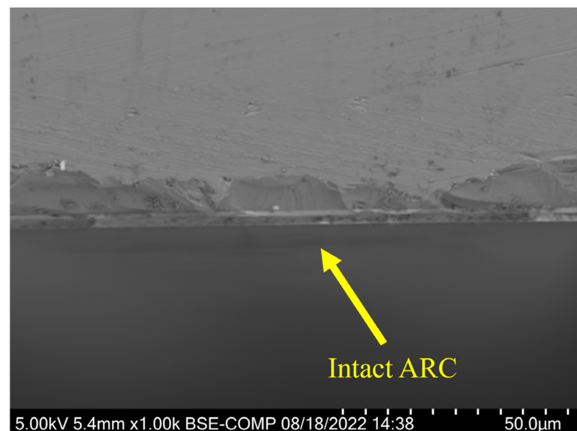


Figure 5: SEM micrographs of a diced silicon wafer cross-section with a delaminated ARC (left) and the ARC that remained intact after heating (right)

delamination seen in the first batch mentioned above.

Finally, an intermediate temperature of 100°C was chosen. After deposition, this sample showed no cracking or delamination. The sample was then heated for 1 hour at 300°C, which did not affect the spectral properties or the mechanical stability of the coating (See figure 5).

RESULTS:

The transmission spectra of the wafers are presented in figures 6, 7, 8, and 9. For the wafers coated on one side, we see a 17% increase in transmission at 8µm, with a steady decrease to about 10% at 12µm. Below 8µm there is still an overall increase in transmission, although quite uneven. Above 12µm we see that the decrease in transmission improvement described in figure 6 continues. At 17.5µm wavelength, the coated wafer crosses over to having increasingly lower transmission than an uncoated wafer as the coating was not designed for such a large spectral range. Measurements was also made at 30° incidence. As can be seen from figure 8, these measurements also have a higher transmission at 8µm wavelength and decreases as the wavelength increases. The difference between the normal incidence and 30° measurements is that the angled measurements show a slightly lower improvement, starting at 15%, ending at 12% with an average of 14% increase in transmission.

At 15µm wavelength, some dips and spikes can be seen in figure 7, 8 and 9. These arise because CO_2 has an absorption peak at 14.9µm wavelength [10]. This means that when the chamber is opened and closed by the operator, to go from background measurement to measurement of the sample, slight variations in the CO_2 concentration will cause a dip, or a spike, as seen in the aforementioned figures.

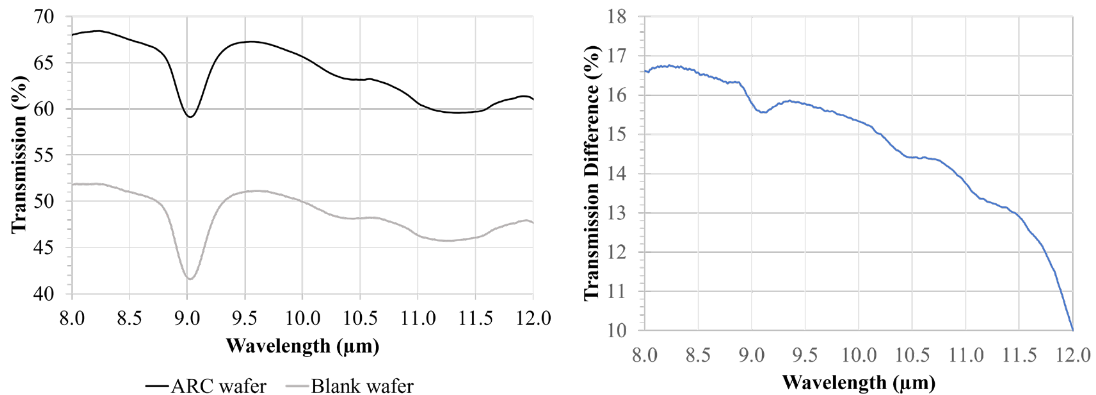


Figure 6: FTIR measurements (left) and comparison (right) of a wafer with the final optimized ARC and without ARC in the intended wavelength range of 8-12µm

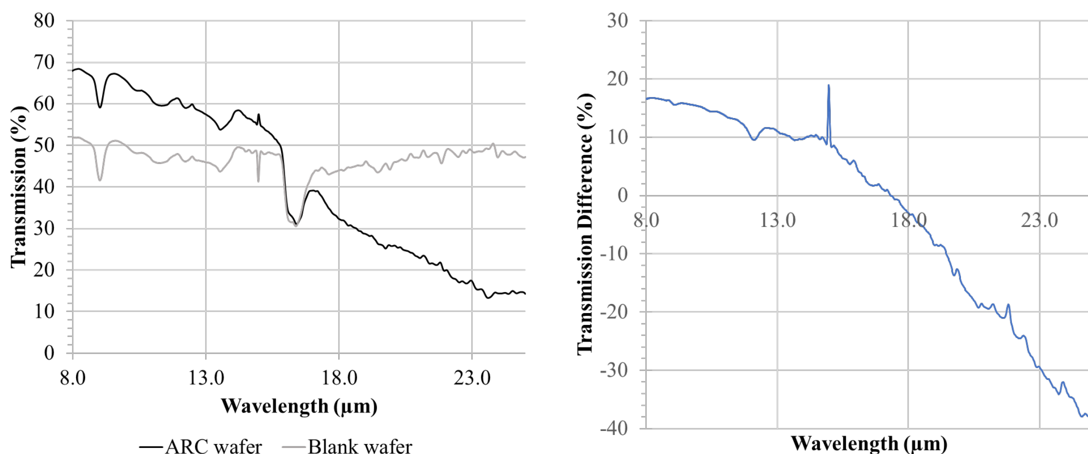


Figure 7: FTIR measurements (left) and comparison (right) of a wafer with the final optimized ARC and without ARC in the 8-25µm wavelength range.

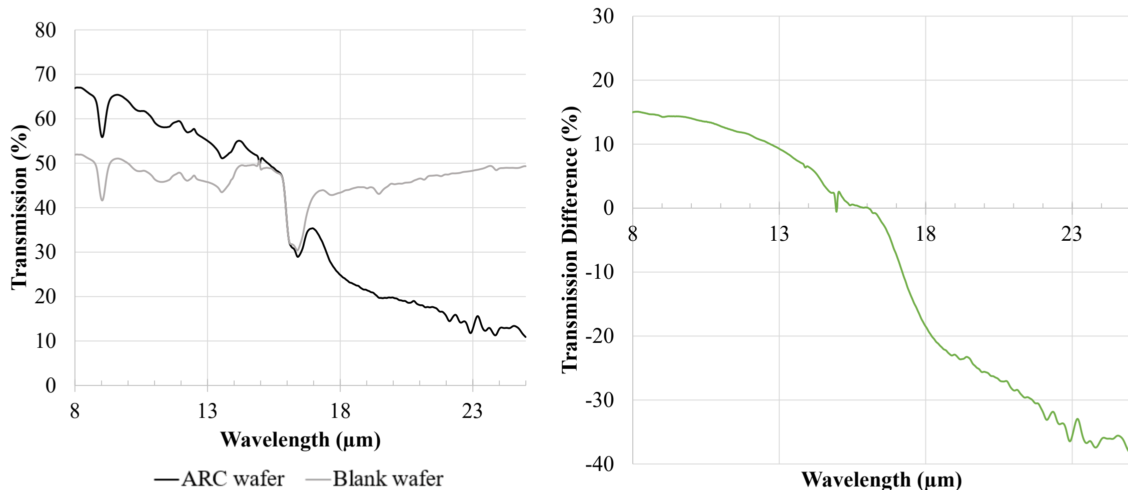


Figure 8 FTIR measurements made at 30° incidence (left) and comparison (right) of a wafer with the final optimized ARC and without ARC in the 8-25µm wavelength range.

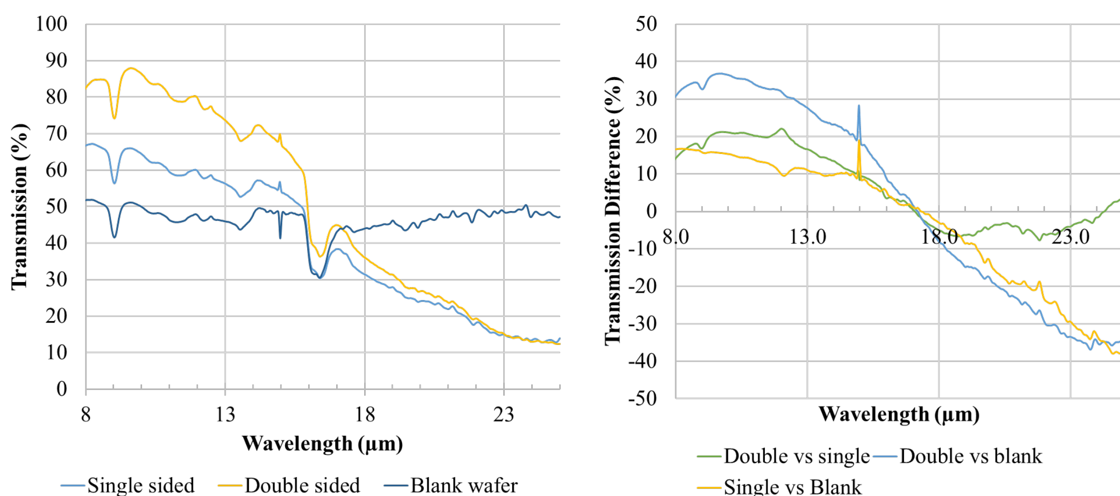


Figure 9: FTIR measurements (left) and comparison (right) of a wafer with the final optimized ARC on one side, both sides, and without ARC in the 8-25µm wavelength range.

SEM images of the final coating revealed no delamination after heating, meaning the ARC also maintained good adhesion and mechanical integrity (see figure 5).

As an additional test, a wafer had both sides covered with the successful ARC. These wafers were also run through heat cycling and measured in the FTIR. The results in figure 9 show that coating the wafer on both sides provides an additional 15% increase in transmission. It is clear when comparing the graphs showing the difference between coatings in figure 9, that in the 8-12µm range, the difference between an uncoated and single-side coated wafer, is very similar to the difference between a single side and a double-side coated wafer.

5 Discussion

A detailed process description for an effective heat-resistant ARC coating has been presented, along with three unsuccessful ones. The successful ARC was compared to a blank wafer using an FTIR spectrometer in transmission mode. It should be noted that the FTIR spectrometer measurements include losses due to scattering, reflection from the uncoated side of the wafer, and absorption in the silicon and coating. These factors explain

the difference between the results seen in the thin-film simulations and the experimental results. In a final package, thinner silicon with lower absorption may be used, and both sides of the silicon will be coated, resulting in higher transmission than presented here. Moreover, high resistivity Si wafer can be used which has lower intrinsic absorption as compared to the wafers used in this study, especially at 9 µm wavelength [11].

While a wafer with coating on both sides is demonstrated, only one side will need heat-resistant coating in the final product. This is because the coating on the outside of the final package can be done as the final step of the processing, which means it will not have the same stringent temperature requirements. This means more traditional coating with more layers and higher transmission may be selected and deposited at room temperature on the outside of the cap wafer.

Another consideration is that we have deposited the coatings on flat wafers. If the coating is to be used as shown in figure 1 the coating will need to be deposited in a cavity, on a micromachined surface. Fortunately, the deposition method used, i.e. e-beam, is compatible with using a shadow mask, as long as the mask material has a CTE similar to silicon. Simulations have also shown that the roughness in the cavity as a result of micromachining, i.e. wet- or direct ion etching, will not negatively impact the transmission [12].

6 CONCLUSION

In this article, a detailed process description and development of an AR coating able to maintain its anti-reflective properties up to 300°C for 1 hour have been presented. This is beyond the requirements for a CuSn SLID bonding process, which is usually done at about 270°C for 30 minutes [13]. In the targeted LWIR range of 8-12µm, the ARC demonstrated an average improvement of more than 15% for normal incidence and 13% for 30° incidence when compared to an uncoated wafer. This was achieved by using only two layers, a MgO adhesion layer, and deposition at 100°C. Three unsuccessful attempts for making such a coating have also been presented. These coatings consisted of more layers and were deposited at room temperature or 175°C, which caused them to delaminate upon temperature cycling to 300°C.

This coating may be directly employed in MBA-based thermal cameras, but the techniques and considerations made here also have potential applications where a thermal camera must go through high temperatures before or during operation, such as in space and subsea.

7 ACKNOWLEDGMENTS

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10.5 Article 5:

Papatzacos P. H., Broaddus P., Solgaard, O., Akram, M. N., Øhlckers P. (2022). Moth-eye anti-reflection structures in silicon for Long Wave IR applications.
Submitted to Journal of Modern OpticsInfrared Physics and Technology

My contribution: Formulated the idea. Designed structures with assistance from the Ginzton Lab research group. Constructed and performed the simulations. Assisted in sample manufacturing. Performed FTIR testing. Main author.

Article 5 is unpublished and not included in online version

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Improved packaging techniques for LWIR microbolometers

Dissertation for the degree of PhD

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Phillip Papatzacos

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