FACULTY OF TECHNOLOGY
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Solid Liquid Inter-diffusion wafer-level bonding for MEMS packaging

Doctoral Thesis

Thi Thuy Luu

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Solid Liquid Interdiffusion wafer-level bonding for MEMS packaging

Thesis submitted for the degree of Philosophiae Doctor

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Department of Micro- and Nanosystem Technology (IMST)
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Horten, 2015

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Abstract

The trend of micro-electronic-mechanical-systems (MEMS) packaging requires cost-effective and high performance packaging techniques. The objective of this study is to develop solid-liquid-interdiffusion (SLID) wafer-level bonding, a promised cost effective and high performance bonding technique for MEMS packaging. Two techniques were addressed: Cu-Sn SLID and Au-In SLID bonding.

The main contributions are:

- Fully characterization of intermetallic formation during the Cu-Sn bonding process
- Development of a numerical simulation model for IMCs thickness development during a Cu-Sn and Au-In bonding process, which could be used as a tool for process design and optimization
- Development of an in-house process for Cu-Sn and Au-In SLID wafer-level bonding
- Fabrication and testing of Cu-Sn and Au-In SLID wafer-level bonding, perform mechanical integrity test at high temperature
- Propose new methods for fracture characterization
- Investigation of voids formation during the Cu-Sn SLID bonding process

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of Philosophiae Doctor from the Department of Micro and Nanosystems Technology (IMST), at Buskerud and Vestfold University College (HBV).

This doctoral work has been conducted at the Department of Micro and Nano Systems Technology (IMST), Faculty of Technology and Maritime Science, Buskerud and Vestfold University College (HBV) in Horten, Norway and in collaboration with Sensonor As. (Horten, Norway) under the supervision of Professor Nils Høivik and Professor Knut E. Aasmundtveit.

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I would like to thank the staffs at Sensonor AS, Dr. Adriana Lapadatu, Stian Martinsen and Jannicke Ødegaard and Dr. Gjermund Kittilsland who have been involved in my PhD work. Special thanks to Dr. Adriana Lapadatu for her valuable discussion and advice, and Stian Martinsen and Jannicke Ødegaard for their contribution on the fabrication and characterization processes.

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List of publications

The thesis includes the following articles

1. **Optimization of Cu-Sn wafer-level bonding based upon intermetallic characterization**, Thi Thuy Luu, Ani Duan, Kaiying Wang, Knut E. Aasmundtveit, Nils Høivik, *4th Electronics Systems-Integration Technology Conference (ESTC)*, 2012.

   My contribution: design, experiment, characterization, estimation, modelling, manuscript preparing.
2. **Optimized of Cu-Sn wafer-level bonding using intermetallic phases characterization,** Thi Thuy Luu, Ani Duan, Knut E. Aasmundtveit, Nils Høivik, *Journal of Electronic Materials*, Vol 42(12) 2013, pp. 3582-3592.

   My contribution: design, experiment, characterization, estimation, modelling, manuscript preparing.
3. **Cu-Sn SLID wafer-level bonding optimization,** Thi Thuy Luu, Ani Duan, Kaiying Wang, Knut E. Aasmundtveit, Nils Høivik, *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd, 28-31 May 2013, Las Vegas, NV*, pp. 1531-1537.

   My contribution: design, fabrication, characterization, analysis, manuscript preparing.
4. **Wafer-level hermetical Cu-Sn micro-joints with high mechanical strength and low Sn flow,** Ani Duan, Thi Thuy Luu, Kaiying Wang, Knut E. Aasmundtveit, Nils Høivik, *submitted to Journal of Micromechanics and Microengineering.*.

   My contribution: a part of mask design and experiment, description of modelling part and take part of manuscript preparing.
5. **High-temperature mechanical integrity of Cu-Sn SLID wafer-level bonds,** Thi Thuy Luu, Nils Hoivik, Kaiying Wang, Knut E. Aasmundtveit, Astrid-Sofie Vardoy, *manuscript accepted to be published on Metallurgical and Materials transaction A.*

   My contribution: design, fabrication, characterization, analysis, testing, manuscript preparing.

6. **Characterization of wafer-level Au-In bonded samples at elevated temperatures**, Thi Thuy Luu, Nils Hoivik, Kaiying Wang, Knut E. Aasmundtveit, Astrid-Sofie Vardoy, *Metallurgical and Materials Transactions A June 2015, Volume 46, Issue 6, pp 2637-2645.*
   My contribution: design, fabrication, characterization, analysis, testing, manuscript preparing.

In addition, I have contribution to the following articles:

7. **High-Temperature shear strength solid-liquid interdiffusion (SLID) bonding: Cu-Sn, Au-Sn and Au-In,** Knut E. Aasmundtveit, Thi Thuy Luu, Astrid-Sofie Vardoy, Torleif A. Tollefsen, Kaiying Wang, Nils Høivik, *5th Electronics Systems-Integration Technology Conference (ESTC)*, 2014.
8. **Void Formation in Cu–Sn Solid-Liquid Interdiffusion (SLID) bonding,** Knut E. Aasmundtveit, Thi Thuy Luu, Nils Hoivik, Kaiying Wang, *accepted to be presented at the 20th European Microelectronics and Packaging Conference 2015*.
9. **Characterization of Cu-Sn SLID interconnects for harsh environment applications,** A. Campos-Zatarain, D. Flynn, K. E. Aasmundtveit, N. Hoivik, K. Wang, H. Liu, **T. T. Luu**, M. Mirgkizoudi and R. W. Kay, *Design, Test, Integration & Packaging of MEMS/MOEMS, DTIP 2014.*
10. **Wafer level vacuum encapsulation for uncooled microbolometers**, Andriana Lapadatu, Stian Martinsen, Gjermund Kittilsland, Astrid-Sofie B. Vardøy, Thi Thuy Luu, Nils Høivik, *WaferBond'13*.
11. **Solid-Liquid Interdiffusion (SLID) bonding — Intermetallic bonding for high temperature applications**, Knut E. Aasmundtveit, Torleif A. Torllefsen, Thi Thuy Luu, Ani Duan, Kaiying Wang, Nils Høivik, *19th European Microelectronics and Packaging Conference, EMPC 2013, Grenoble; France; 9 September 2013 through 12 September 2013.*
12. **Au-Sn fluxless SLID bonding: Effect of bonding temperature for stability at high temperature, above 400 ^{o}C,** Knut E. Aasmundtveit, Thi-Thuy Luu, Hoang-Vu Nguyen, R. Johanessen, Nils Hoivik and Kaiying Wang, *Electronic Systems-Integration Technology Conference (ESTC), 2010 3rd*.
13. **Thermosonic bonding for ultrasound transducer: Low-temperature metallurgical bonding**, Knut E. Aasmundtveit, Thi-Thuy Luu, Trym Eggen,

Charles E. Baumgartner, Nils Hoivik, Kaiying Wang, Hoang-Vu Nguyen and Kristin Imenes, *Electronic Systems-Integration Technology Conference (ESTC), 2010 3rd*.

14. **Gold to gold thermosonic bonding: Characterization of bonding parameters**, Thi-Thuy Luu, Hoang-Vu Nguyen, Andreas Larsson, Nils Hoivik and Knut E. Aasmundtveit, *IMAPS Nordic 2010 Conference.*

Abbreviations

SLID: Solid liquid interdiffusion

IMC: Intermetallic compound

MEMS: Micro-electro-mechanical systems

BCB: Benzocyclobutene

RF: Radio frequency

SEM: Scanning electron microscope

EDS: Energy dispersive spectrum

IC: Integrated circuit

HT: High-temperature

3D: Three dimension

UBM: Under-bump metallization

TLP: Transient liquid phase

IR: Infrared

PID: Proportional-integral-derivative

DUT: Device under test

1 Introduction

1.1 MEMS

Microelectromechanical systems (MEMS) are integrated systems that combine electrical, mechanical and other interact-components. Being the first to combine moving mechanical structure and electronic components at micro-scale, MEMS is considered a breakthrough technology and has become a distinctive research field with remarkable progress [1] on advanced sensing systems, implantable biomedical sensors, and microactuators [2]. Nowadays, MEMS has been commercialized in numerous applications such as automotive, consumer mobile products, biotechnology, medical, and optical products [3]. According to prediction (Yole Development France report 2013 [4, 5]), the MEMS market has an annual growth of ~15 % and could reach $ 22.5 billion in 2018. Although MEMS has been developed for many applications, the most critical issue of MEMS commercialization is packaging.

1.2 MEMS packaging requirements and challenges

According to the industry reports, the packaging/assembly and testing still account for 35-60 % of the final cost of the devices [4, 6-11]. The reason is that MEMS packaging is much more complex than integrated circuit (IC) packaging and usually requires interactions with the environment [12, 13]. Since MEMS have been implemented for various applications, the packaging requirements depend on the end-applications. For example, optical MEMS devices need optical communication with the environment; implant medical devices need bio-compatible materials; RF-MEMS need the electrical interconnection. In general, the requirements and challenges of MEMS packaging include:

- MEMS devices usually contain fragile structures, such as membrane, resonator, accelerometer, etc. Therefore, the packaging of MEMS requires more mechanical support during the fabrication and packaging process.
- MEMS devices, such as mechanical resonator structures, microbolometer needs a vacuum environment for high performance and long-term reliability. Therefore, hermetic sealing is required to perform an internal vacuum environment for the devices and protect devices from the external environment. In addition, the outgassing during the bonding and fabrication process must be controlled.
- The processing of MEMS fabrication includes many steps; the packaging must be compatible with the devices manufacturing process.
- MEMS devices include many different materials, and the thermal stress during the packaging process must be controlled to improve the performance of the devices.

1.3 Wafer-level packaging of MEMS devices

The trend in MEMS manufacturing is to increase production volume, reduce cost and size, and improve the performance [8]. This trend has raised new challenges for MEMS packaging: hermetic sealing to improve the performance of MEMS devices, high production volume packaging and lowering cost. Wafer-level packaging is an important approach that meets the new demands of MEMS packaging due to these advantages:

- High production volume is enabled by using 8'' wafers
- Low cost: (since all the dies are packaged parallel, the processing cost per product is reduced).
- Miniature size: wafer-level packaging reduces the space between the dies, thus reduces the size of the devices.

1.3.1 Wafer-level bonding techniques for MEMS packaging

Wafer-level bonding is an important process of MEMS packaging. Over the years, there are many different wafer-level bonding techniques have been developed for MEMS packaging. An overview of these bonding techniques is shown in Figure 1.1; and the

comparison of different bonding techniques is shown in Table 1.1. In this thesis, the focus is on solid liquid interdiffusion bonding (SLID).

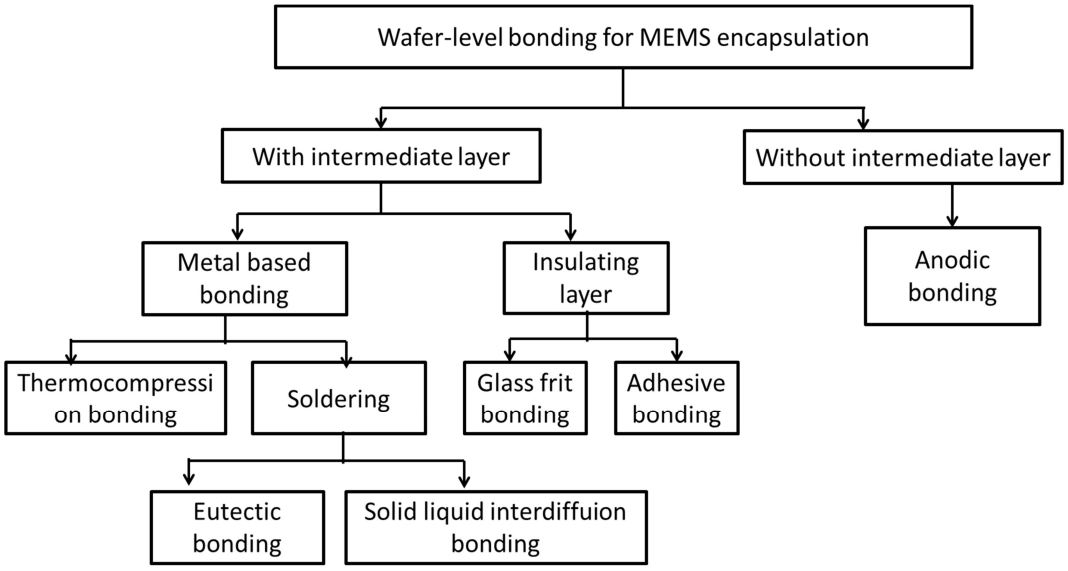


Figure 1.1: Overview of wafer-level bonding techniques used to package MEMS devices

Table 1.1: Comparison of different wafer-level bonding techniques

Bonding technique	**Advantages**	**Disadvantages**
Anodic	Mature technique, hermetic high bond strength, low CTE miss-match, narrow bond frame	High temperature (~500^{o}C), electronic charged (400-1000 V), flat surface requirement
Direct metal (thermocompression)	Hermetic, high bond strength	High temperature and force, flat surface requirement
Soldering	Hermetic, self-alignment, low process temperature	Solder flow possibility, flux medium bond strength, low temperature stability
Solid liquid interdiffusion (SLID)	**Low process temperature, high bond strength, hermetic, high temperature stability**	**Complex process, in research stage**
Glass-frit	Mature technique, hermetic, high bond strength	Large bond frame (> 200 µm), high temperature (>450^{o}C), complex process
Adhesive	Very low temperature (150-200 ^{o}C), low cost, flexible	Low bond strength, non-hermetic

1.3.2 Anodic bonding

Anodic bonding is a mature bonding technique, usually used for silicon to glass bonding. The bonding is performed by applying high voltage (400-1000 V) at elevated temperature (300-500^{o}C) [14]. Anodic bonding produces uniform, high strength, hermetic and long term reliability bonding suitable for MEMS encapsulation [15, 16]. This bonding technique has been well established for many applications, such as resonator, pressure sensor and microfluidic devices [17-25]. Several commercial applications of anodic bonding are shown in Figure 1.2.

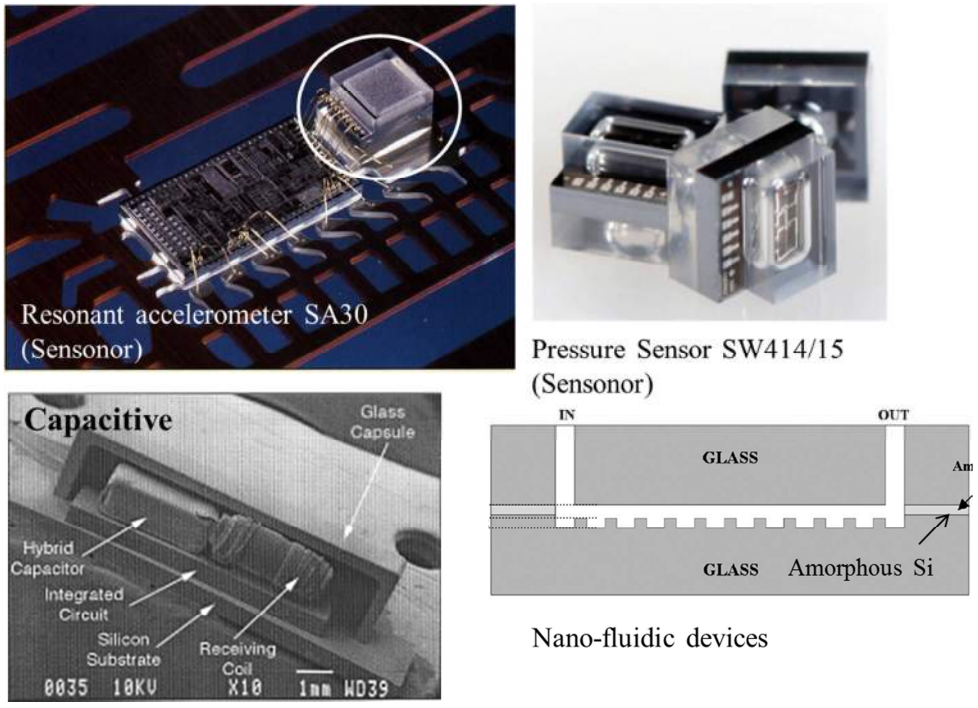


Figure 1.2: Applications of anodic bonding for hermetic sealing of MEMS devices and encapsulation of nano-fluidic devices [18, 22, 25, 26].

1.3.3 Glass-frit bonding

Glass-frit bonding uses special glass as an intermediate bonding layer. This glass must have low melting temperature that could reflow at temperature 400-450 ^{o}C [27-29]. The glass is deposited on the wafers using screen printing method. During the bonding process, the glass is heated and melts. The liquid glass flows and wets the wafer surface to form the bonding at atomic level. During the cooling process, glass-frit re-solidifies and forms a reliable hermetic and strong mechanical bond [29-32]. An illustration of the bonding process is shown in Figure 1.3. Glass-frit bonding is a mature technique for

MEMS encapsulation and has been well established for many commercial products. Several applications of glass-frit bonding are shown in Figure 1.4. However, the main disadvantage of glass-frit bonding is the large sealing area [33] which increases the final product size.

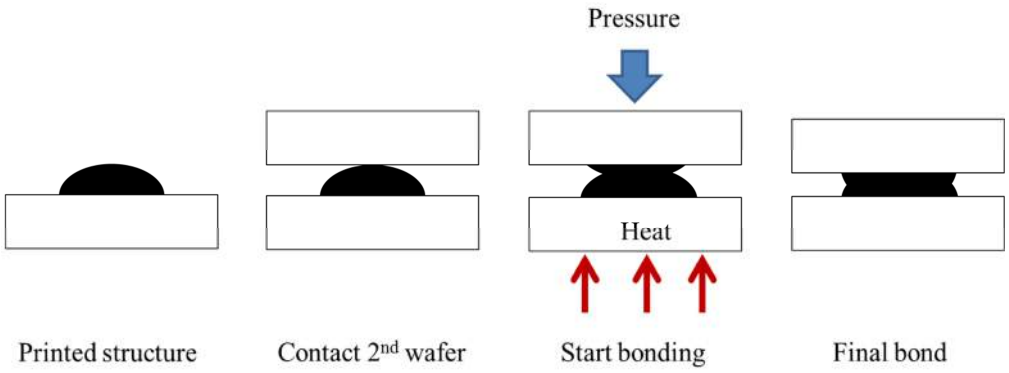


Figure 1.3: An illustration of glass-frit bonding process.

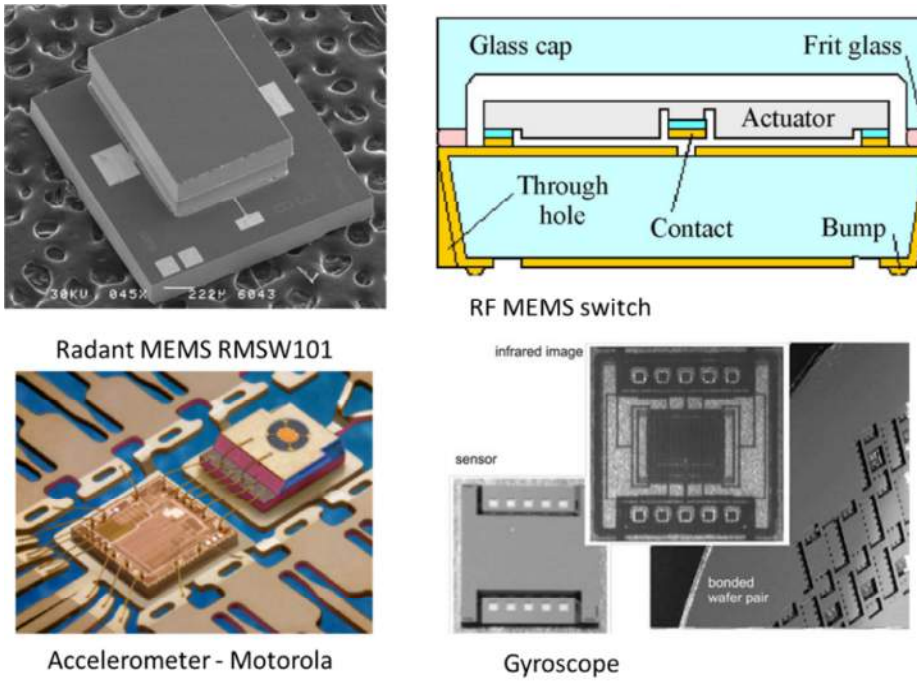


Figure 1.4: Glass-frit bonding applications for MEMS encapsulation [34-37].

1.3.4 Adhesive bonding

Adhesive bonding uses polymer as an intermediate bonding layer. During the bonding process, the polymer is in liquid or semi-liquid form. Due to pressure, the polymer wets the wafer's surface and forms intimate bonding. Afterwards, the polymer is hardened

by thermal or UV curing. The most important advantages of adhesive bonding are the low temperature process and the low cost [38-43]. However, the resulting bonding is not hermetic and has low mechanical strength. This bonding technique has been developed for microfluidic and bio-MEMS devices fabrication, MEMS devices encapsulation and served as temporary bonding for film and devices transfer [44-48]. Figure 1.5 shows an application of adhesive wafer-bonding for RF MEMS devices encapsulation.

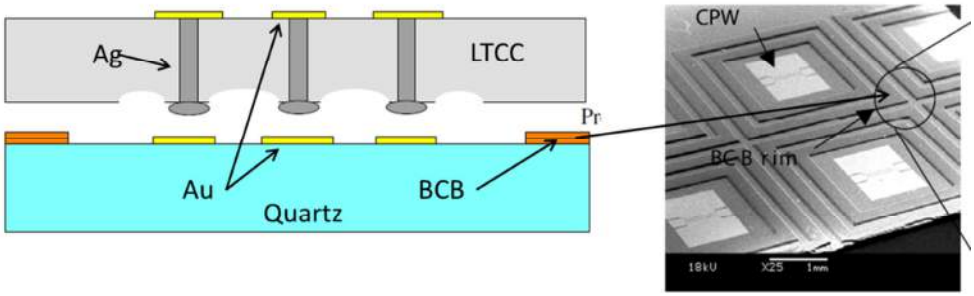


Figure 1.5: Application of BCB adhesive bonding for RF-MEMS encapsulation [45].

1.3.5 Metal diffusion bonding (thermocompression)

Direct metal bonding uses metal as intermediate layer. The most common metal diffusion bonding techniques are Au-Au, Cu-Cu and Al-Al [49-59]. The metal bonding performs a hermetic and high strength bond. In addition, compared to glass-frit bonding, the metal bonding can shrink the bonding area by reducing the frame width and thus reduce the final product size by about 50 % [33]. However, the planarity and oxidation are critical for the bond performance. Chemical treatment prior to bonding is needed in order to remove the oxidation layer on the metal surface if non-inert metal is used. In addition, the process temperature is relatively high. The bonding temperature could be lowered by surface activation with plasma or ultrasonic; but the activation process can damage sensitive devices. The technique is used for hermetic sealing of MEMS devices and 3D integration. Figure 1.6 shows several applications of metal diffusion bonding for MEMS devices encapsulation.

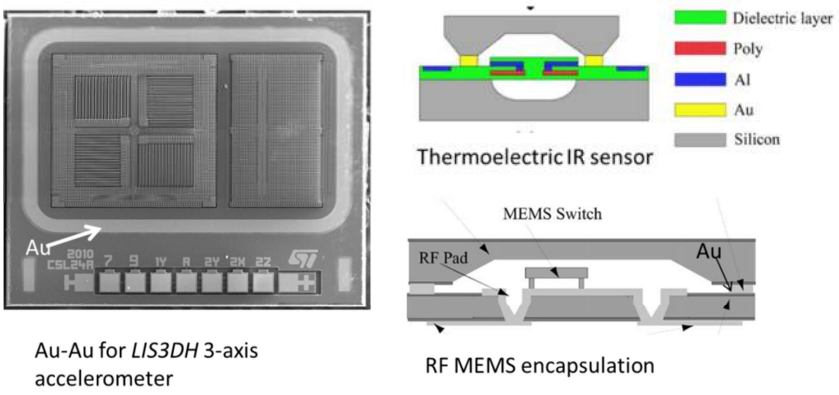


Figure 1.6: Metal thermocompression bonding for MEMS encapsulation [33, 54, 56]

1.3.6 Soldering using standard solder

Soldering uses standard solder alloys as an intermediate layer. Normally, a metal layer is needed to serve as under-bump metallization (UBM) to improve the adhesion of solder to wafers. An illustration of the soldering process is shown in Figure 1.7. The solder is deposited on the wafers by electroplating, printing or injection molded transferring process [60-66]. The bonding temperature is above the melting point of solder alloy. During the bonding process, the solder alloy reflows and wets the metal layer. During the cooling process, the solder solidifies and forms a solid bond. Solder alloys react with the UBM to form IMCs during the reflow and the bonding process.

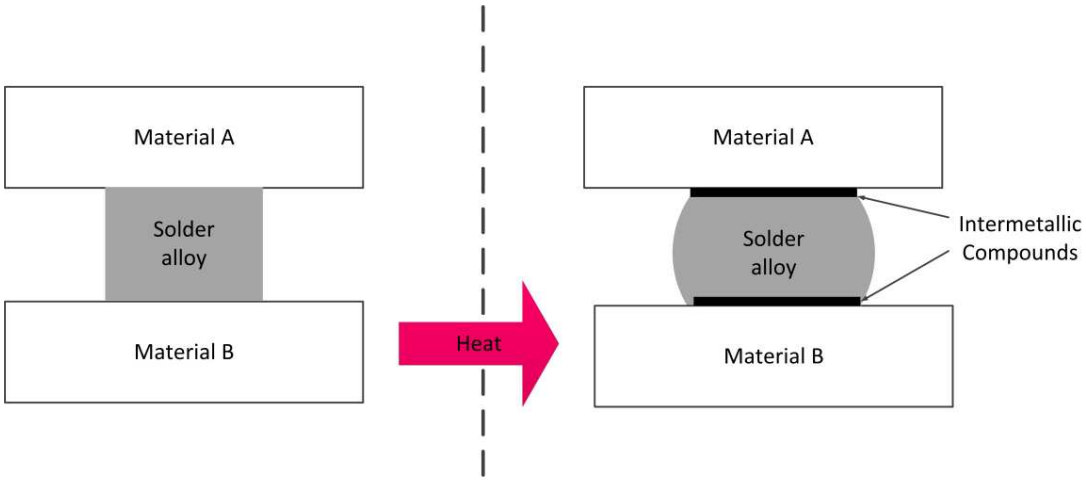


Figure 1.7: Illustration of solder bonding process

Solder has been widely used in electronic packaging as interconnections [67-69]. For MEMS packaging, soldering is mainly used in order to provide the electrical connection

for the devices[70, 71], to package the devices that have different planarity [72] or to enable low temperature packaging [72-74]. The technique is of interest for MEMS packaging due to the low temperature process and being hermetic. However, soldering has low temperature stability, low mechanical strength, and crack or voids formation [68, 75-77]. Therefore, the application of soldering for MEMS encapsulation is limited.

Figure 1.8 shows one application of Sn-Pb solder for interconnections and optical microarray encapsulation. One of the critical requirements of soldering is the use of flux (cleaning agent) prior to bonding. The residual of impurities from flux could cause void formation or crack that affect the bond performance.

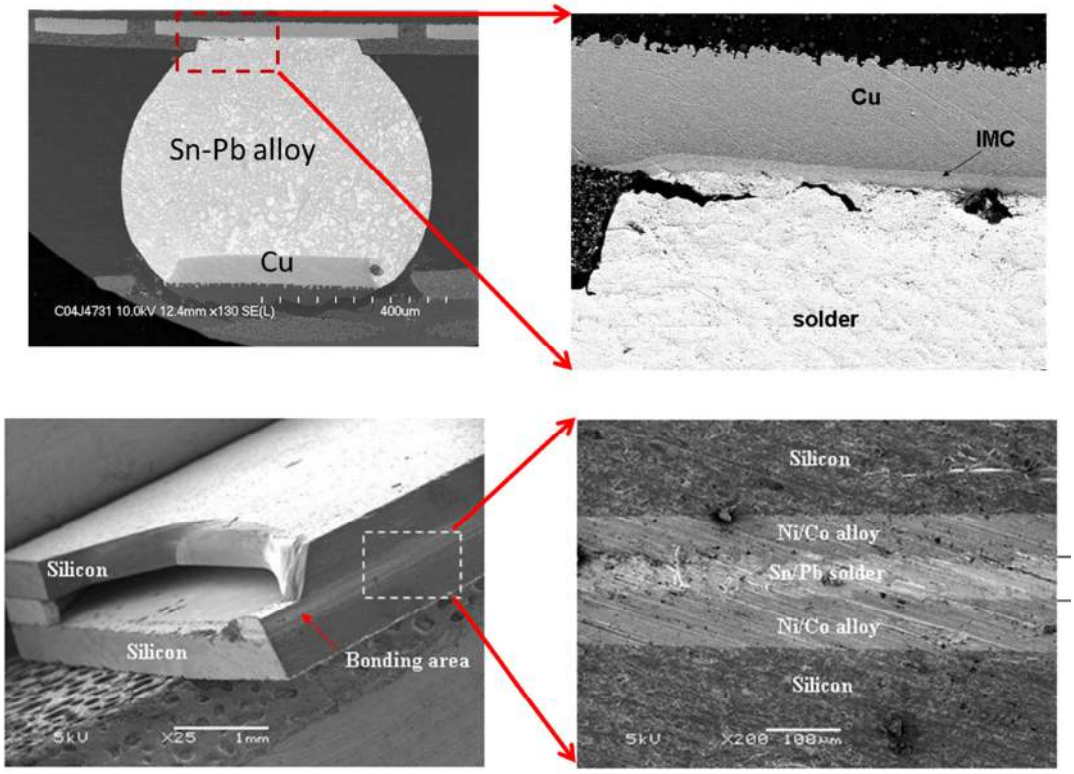


Figure 1.8: Solder application for interconnection and optical microarray encapsulation [74, 78].

1.3.7 Solid liquid interdiffusion bonding

Solid liquid interdiffusion (SLID) bonding, also called transient liquid phase bonding (TLP) or off-eutectic bonding or isothermal solidification bonding, is based on rapid formation of intermetallic compounds (IMCs) between two metal components, one

metal with high melting temperature (Au, Cu, Ni, Ag) and the other with low melting temperature (In, Sn). The bonding process is performed at low temperatures, just above the lowest melting point. At the bonding temperature, the low melting component melts and IMCs solidify isothermally. The reaction is brought to thermal equilibrium and the resulting bond-line consists of only the high-melting component and IMCs with elevated melting temperatures. An illustration of IMCs formation during SLID bonding process and binary phase diagram of metal systems with two used metal components is shown in Figure 1.9.

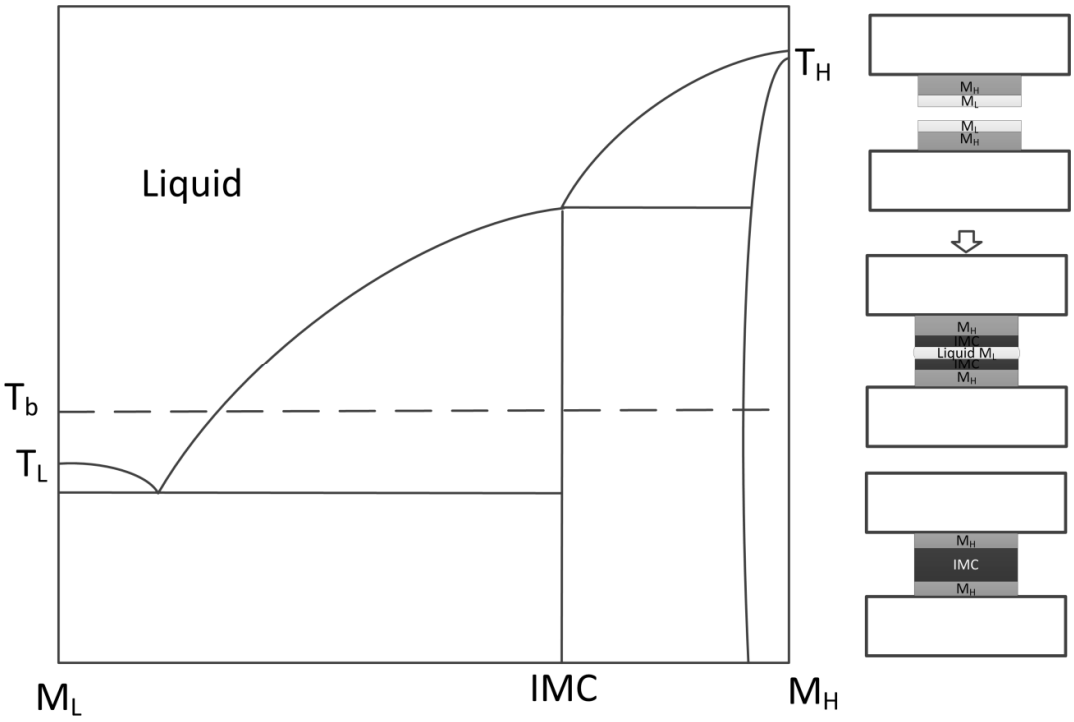
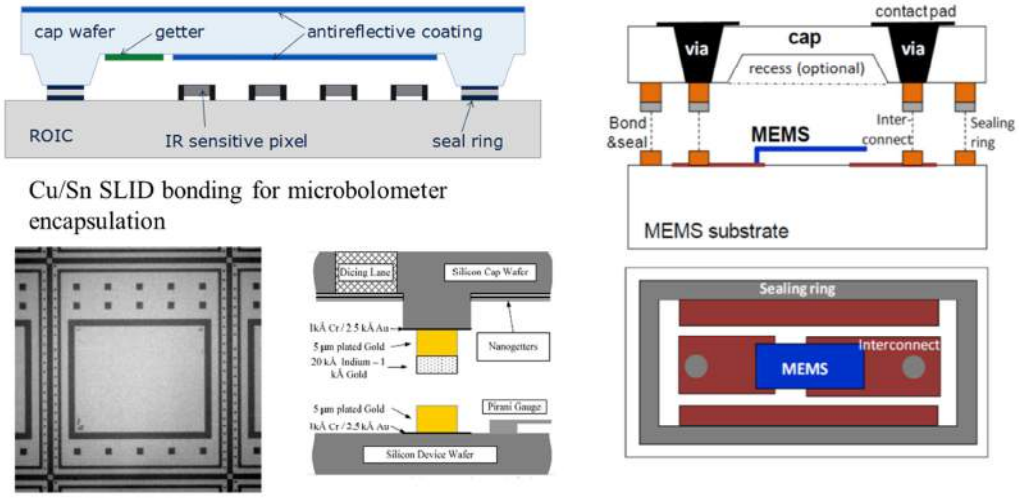


Figure 1.9: Illustration of SLID bonding systems. Schematic phase diagram shows binary equilibrium of metal systems with high-melting (T_H) and low-melting (T_L) components, and IMC with high melting point. The process temperature T_b is above T_L. The insert shows a schematic of a typical layer structure for SLID bonding and bonding process [79].

SLID bonding has received much attention from industry and research activities due to several advantages:

- High temperature stability: the final bond-line with IMCs and high-melting metal has high temperature stability that allows repeating processing without bond melting.
- Moderate process temperature: compared to metal diffusion bonding, glass-frit bonding and anodic bonding, SLID has lower process temperature. This allows reducing thermal stress introduced during the bonding process and bonding of devices that are sensitive to temperature.
- High bond performance: metals are used as intermediate layers, which enable high bond strength and hermeticity.
- Low cost: metals are deposited by an electroplating process, which enables low cost processing. In addition, flux-less is enabled by using symmetric bonding [79] which removes the need of using flux

With these advantages, SLID bonding is becoming an attractive technique for MEMS packaging. Many research activities have demonstrated SLID bonding for different applications. Figure 1.10 shows several potential applications of SLID bonding for MEMS encapsulation.



Au/In SLID bonding for image sensor module and Pirani Gauge encapsulation

Cu/Sn bonding for RF MEMS encapsulation and interconnect

Figure 1.10: SLID bonding applications [71, 80-82]

Table 1.2: Comparison of different SLID bonding techniques (refers to [83, 84])

Materials	Bonding Temperature(^{o}C)	Re-melting Temperature (^{o}C)	References
Cu-Sn (*)	**260-300**	**676**	[79, 85-87]
Au/Sn	280-350	500	[88, 89]
Au-In (*)	**160-200**	**>495**	[80, 90, 91]
Ag/Sn	250	600	[92, 93]
Ni/Sn	300	794	[94]
Ag/In	180-200	880	[95, 96]
Cu/In	260-360	>600	[97]

The use of different SLID bond materials has been demonstrated for MEMS packaging. A comparison of these materials is shown in Table 1.2. For all SLID techniques, the final bond has a much higher re-melting temperature compared to the bonding temperature. In this study, two bonding techniques; Cu-Sn SLID bonding and Au-In SLID bonding are presented.

1.4 Hermetic sealing of MEMS devices

1.4.1 Hermetic sealing

A particular requirement of MEMS packaging is hermetic sealing. The main objective of hermetic sealing is to define an internal environment with accepted vacuum level for MEMS structure in order to improve the performance and lifetime of devices.

A typical wafer-level packaging process for MEMS hermetic encapsulation is shown in Figure 1.11. MEMS devices are fabricated on a device-wafer. The other wafer is served as cap-wafer. Cavity is performed on the cap-wafer to create an internal space for MEMS devices. The sealing material is deposited on both cap and substrate wafers. In order to perform an internal vacuum inside the cavity, the wafers are bonded in vacuum environment. After bonding, the sealing frame protects the device from the external environment.

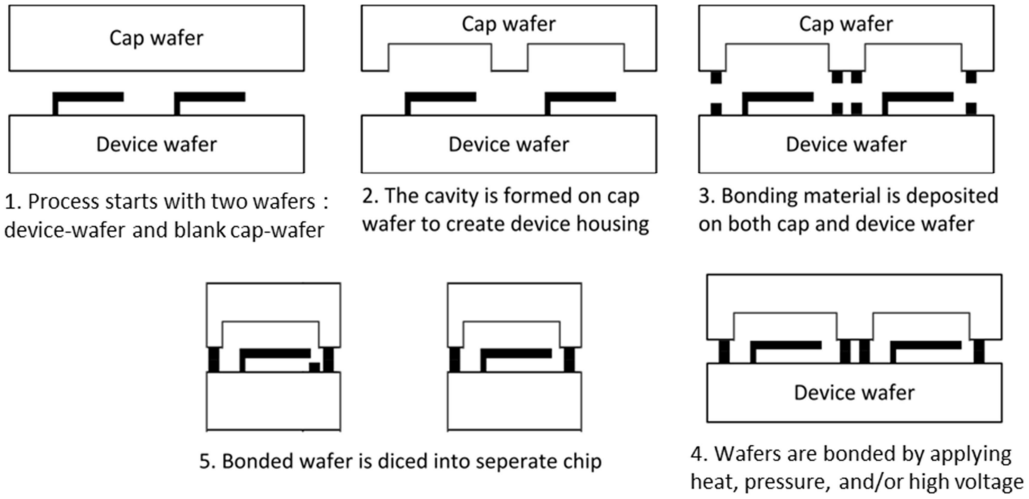


Figure 1.11: Illustration of a typical wafer-level packaging process for MEMS encapsulation.

1.4.2 Material requirements for hermetic sealing

To perform a hermetic sealing, the bonding material must be hermetic in order to protect devices from gas and water diffusion into the package. Hermetic property of material is evaluated by permeability rate. The permeability rate of a material is the diffusion rate of gas atoms through the material.

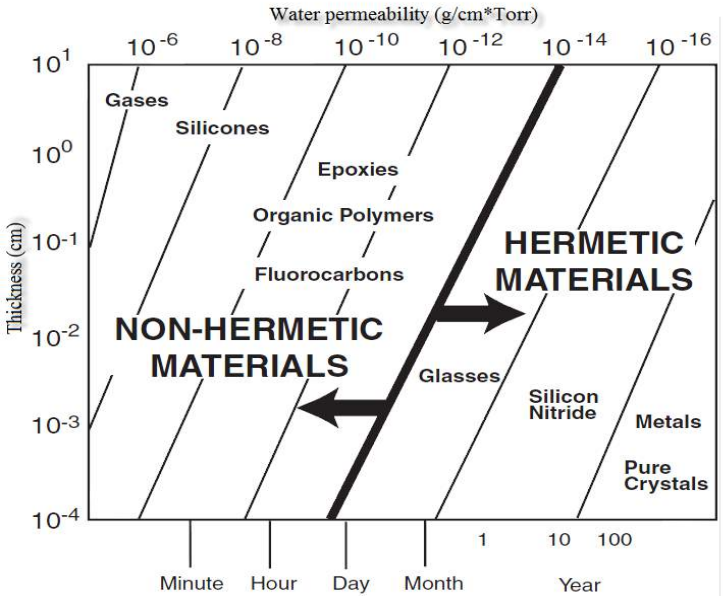


Figure 1.12: The permeability of materials as function of thickness. The highlighted line indicates the boundary between hermetic and non-hermetic materials [59, 98]

Figure 1.12 shows the permeability rate of different materials. The materials that have less than one day sealing capability (permeability is larger than 10^{-14} g/cm*Torr) are defined as non-hermetic materials. The material that could be used for hermetic sealing includes glasses, silicon nitride and metals.

1.4.3 Vacuum level requirement of MEMS devices

Hermetic sealing is critical to almost all MEMS devices, such as pressure sensor, motion sensor and microbolometer. For the devices that contains moveable structures; such as accelerometer, gyroscope and resonator; an internal vacuum environment eliminates the gas damping effect and improves the performance of devices [99-101].

Table 1.3: Vacuum level requirement of different MEMS devices

Application	**Vacuum level**	**Packaging technology**	**Reference**
Pressure sensor	< 1 bar	Glass frit	[102-105]
		Anodic	
		Silicon fusion	
Accelerometer	10^{-1}→ 1 bar	Metal eutectic	[19, 33, 106-108]
		Metal thermocompression	
		Glass frit	
		Anodic bonding	
High quality factor resonator	10^{-2}→ 10^{-1} bar	Silicon fusion	[30, 109]
		Metal with getter	
		Glass frit with getter	
Gyroscope	10^{-3}→ 10^{-2} bar	Metal eutectic	[33, 110]
		Metal thermocompression	
		Glass frit	
Resonator magnetic field sensor	10^{-3} → 10^{-2} bar	Glass frit	[111, 112]
		Silicon fusion bonding	
Microbolometer	< 10^{-4} bar	SLID	[56, 113, 114]
IR sensor		Thin film evaporation	
		Metal thermocompression	

For infrared microbolometer, vacuum environment minimizes the thermal conduction and convection and improves the thermal stability of the devices [56, 82]. For pressure

sensor, an internal vacuum environment is needed in order to perform a reference for pressure measurement. The requirement of vacuum level for different MEMS devices is shown in table 1.3.

2 Methodology

2.1 Cu-Sn SLID bonding

Cu-Sn solid liquid interdiffusion (SLID) bonding is based on rapid intermetallic compounds (IMCs) formation between Cu and Sn. The bonding process is performed at temperatures 250-300 ^{o}C [79, 82, 85, 115-118], which is above the melting point of Sn (232 ^{o}C). At the bonding temperature, Sn melts; Cu diffuses into Sn and reacts with Sn to form IMCs. The resulting final bond-line consists of Cu and IMCs with elevated temperature stability.

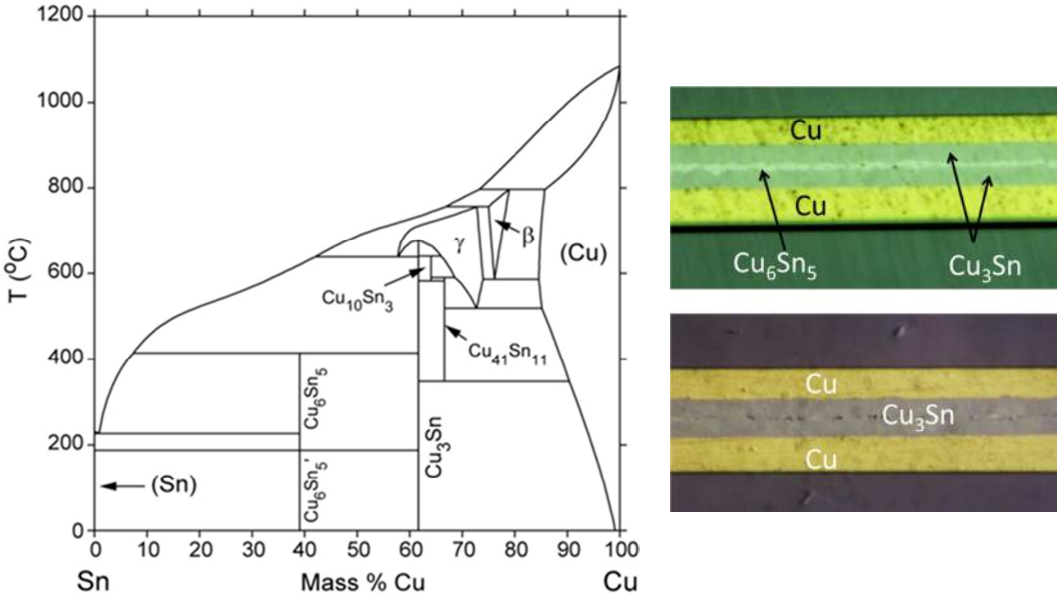


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Figure 2.1: Equilibrium phase diagram of Cu-Sn binary systems and cross-section micrograph of Cu-Sn bonded samples.

Figure 2.1 shows equilibrium phase diagram Cu-Sn binary systems and cross section micrograph of final Cu-Sn bonded samples. The two IMCs that form during Cu-Sn

bonding process are Cu_3Sn and Cu_6Sn_5 with the temperature stability up to 676^{o}C and 415^{o}C respectively. The final bond consists of IMCs and an excess Cu layer to isolate the IMCs layer from adhesion layer and to ensure that the final bond has high temperature stability. Cu-Sn is becoming an attractive technique for MEMS packaging due to low cost and high performance (high bond strength, reliable hermeticity, high temperature stability and long term reliability). In addition, compares to other SLID bonding processes, the phase diagram is simpler and thus the formation of IMCs during bonding process is easier to predict and describe. Cu-Sn SLID bonding with high bond strength, reliable hermeticity has been demonstrated for MEMS packaging, interconnection and 3D integration [82, 85, 115, 119, 120].

In the scope of this thesis, Cu-Sn SLID wafer-level bonding has been demonstrated for hermetic encapsulation of MEMS devices. The high temperature mechanical integrity has also been proven however further reliability testing is required to prove the method for high temperature applications. IMCs formation during the Cu-Sn bonding process was fully investigated. The development of IMCs during bonding process was modeled as a function of initial Sn thickness and temperature profile. This modeling is a powerful tool for process design and optimization. Actual bonding experiments were demonstrated for hermetic encapsulation and high temperature applications.

2.2 Au-In SLID bonding

Au-In SLID bonding is based on the intermetallic compounds formation of Au and In. Due to the low melting point of In (156 ^{o}C), the bonding process could be performed at low temperatures (< 200 ^{o}C) [90, 91, 121-123]. This is of interest for many applications since lower bonding temperature reduces thermal stress in the package, and also facilitates bonding of temperature sensitive devices [81]. Another advantage is that an Au rich phase could be formed during processing and thus increases the maximum re-melting temperature of the final bond. Figure 2.2 shows the binary phase diagram of binary Au-In systems, presents a complex system with more than 10 different equilibrium phases. The Au-rich IMCs could have temperature stability up to 500 ^{o}C.

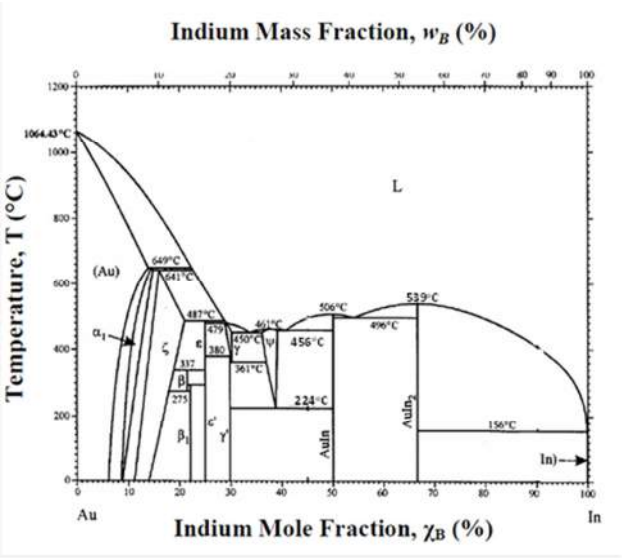

Figure 2.2: Equilibrium phase diagram of Au-In binary systems.

A typical cross-section micrograph of an Au-In bonded sample is shown in Figure 2.3. For Au-In, an initial In surplus thickness design is considered in order to tolerate the rapid formation of $AuIn_2$ which occurs even at room temperature. Therefore, different from "standard" SLID requirement, there is no Au surplus in the final bond-line. The formation of IMCs bonding is more difficult to predict due to complex phase diagram. Therefore, for this actual bonded sample, the final bond-line consists of four different IMCs, which is non-equilibrium.

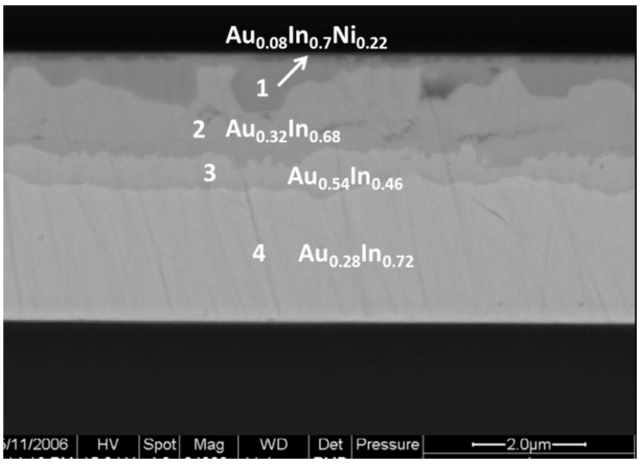

Figure 2.3: Cross-section micrograph of Au-In bonded samples with four IMCs present [91].

In this thesis, initial Au-In bonding is being demonstrated. The formation of $AuIn_2$ during bonding process was modeled as a function of initial In thickness and

temperature profile. The mechanical integrity of Au-In bonded samples at high temperature was investigated.

2.3 Intermetallic formation during SLID bonding process

Intermetallic formation is one of the critical issues of SLID bonding. The principle of SLID bonding is based on the IMCs solidification at the bonding temperature, when the low melting component (M_L) melts. In order to obtain successful bonding, there must be pure M_L available at the surface when the melting temperature of M_L (T_L) is reached. However, in a SLID bonding process, the temperature is raised following a defined temperature profile. The IMCs are formed during the ramping process, even at a temperature below T_L, and M_L is consumed into IMCs. The challenge is predicting how much M_L remains at the melting point T_L which does not only depend on the initial M_L thickness, but also the temperature profile or the amount of M_L that has been consumed to form the IMCs. Therefore, the formation of IMCs during bonding process must be well understood. In order to optimize the bonding process, there is a need of a simulation model for IMCs development during the SLID bonding process which can predict remaining M_L thickness.

2.3.1 IMCs growth kinetic coefficients

The general mechanism of IMCs formation during SLID annealing process is itself well understood [124]. The formation rate of IMCs depends on both the diffusion rate and actual chemical reaction kinetics. By assuming simplification to one-dimension diffusion model, the kinetics model of IMCs growth thickness can be expressed by:

$$y_t{}^2 - y_0{}^2 = k_0 e^{\frac{-Q}{RT}} t^{2n} \qquad \textbf{Eq 2. 1}$$

Where y_t is IMCs thickness, y_0 is initial IMCs thickness, t is annealing time at temperature T, k_0 is diffusion coefficient, Q is activation energy, R is the gas constant and n is an empirical coefficient; n = ½ corresponds to a direct solution of Fick's law, the introduction of the empirical coefficient n opens for modeling an experimentally observed time-dependent that deviates from a purely-diffusion controlled one.

The kinetics coefficients of IMCs growth thickness can be estimated by annealing the sample at different temperatures and times. Further information is presented in our articles [124, 125]. The estimated kinetics coefficients of IMCs during Cu-Sn and Au-In annealing process are shown in Table 2.1 and Table 2.2. Note that for Cu-Sn systems, different values of *n* were obtained. This indicates that the IMCs formation is controlled by the combination between diffusion and chemical reaction mechanisms. At low temperatures, the chemical reaction rate is low and slowing down the growth of IMCs, a lower value of *n* was obtained. At high temperature, the chemical reaction rate is fast and the effect of the chemical reaction is eliminated. Therefore, the diffusion mechanism dominates and $n = ½$ was obtained.

Table 2.1: Kinetics coefficients of Cu_3Sn growth thickness and the amount of Sn that reacts with Cu to form IMCs [124]

	Cu_3Sn	**Reacted Sn**
Diffusion coefficient k_0 [$\mu m^2/min^{2n}$]	7.9×10^6	2.8×10^4
Activation energy *Q* [kJ/mol. K]	78	52
Empirical exponent *n*	0.5 for T>=232°C	0.45 for T>=180°C
	0.4 for T<232°C	0.3 for T<180°C

Table 2.2: Kinetics coefficients of $AuIn_2$ thickness growth, adapted from Zhang [121]

	k_0 (cm^2/s)	**Q (eV)**	**n**
T>150°C	6.43×10^{-6}	0.46	0.5
T<150°C	1.20×10^{-8}	0.23	0.5

2.3.2 Modeling of IMCs development during bonding process

The objective of bonding process modeling is to build a mathematical tool used for bonding process design and optimization. The simulation model for IMCs development during the SLID bonding process was built based on the kinetics coefficients shown in Table 2.1 and Table 2.2, using a numerical method. For any given time *t* with assuming given IMCs thickness y_t and temperature T_t; with further assuming initial zero thickness ($y_0 = 0$), the required time that the sample has to be annealed at T_t in order to obtain IMCs y_t could be estimated by:

$$t_{est} = \left(\frac{y_t^2}{k_0 e^{\frac{-Q}{RT_t}}} \right)^{\frac{1}{2n_t}} \quad \textbf{Eq 2. 2}$$

For a small time period from *t* to *t+dt*, we can assume that the temperature is kept at constant *dt*. Using the extrapolation method, the IMCs or reacted Sn thickness at *t+dt* could be estimated by:

$$y_{t+dt} = \sqrt{k_0 e^{\frac{-Q}{RT_t}} (t_{est} + dt)^{2n_t}} \quad \textbf{Eq 2. 3}$$

An example of the simulation result of IMCs development during Cu-Sn bonding process is shown in Figure 2.4, where the IMCs thickness (Cu_3Sn and Cu_6Sn_5) and the remaining Sn thickness are described as a function of bond temperature profile and initial Sn thickness. With this simulation, we can predict the critical parameters of the bonding process:

- Remaining Sn thickness when the melting point of Sn is reached
- When all Sn is consumed into IMCs
- When the final $Cu/Cu_3Sn/Cu$ bond-line is achieved

For Cu-Sn SLID bonding, to obtain a successful bonding, it is important to ensure that there is remaining pure Sn at the bond interface when the melting point of Sn is reached. In addition, the objective is to achieve final $Cu/Cu_3Sn/Cu$ bond-line that is thermodynamic stable since no IMCs will be further formed during operation process. Therefore, the model is a powerful tool for the initial design and optimization of Cu-Sn bonding process.

In a Cu-Sn system, both Cu_3Sn and Cu_6Sn_5 coexist for a given time. However, in Au-In system, the first IMC that forms during the bonding process is $AuIn_2$ and this IMC would be stable if there is excess In [126-129]. Other IMCs would be formed after $AuIn_2$ if there is excess Au. In addition, the formation of IMCs during the Au-In bonding process is more complex to understand due to complex phase diagram. Therefore, it is more complicated to achieve the most desired final bond structure. In the modeling, only $AuIn_2$ is taken into account. Figure 2.5 shows the simulation interface for IMCs growth during Au-In bonding process.

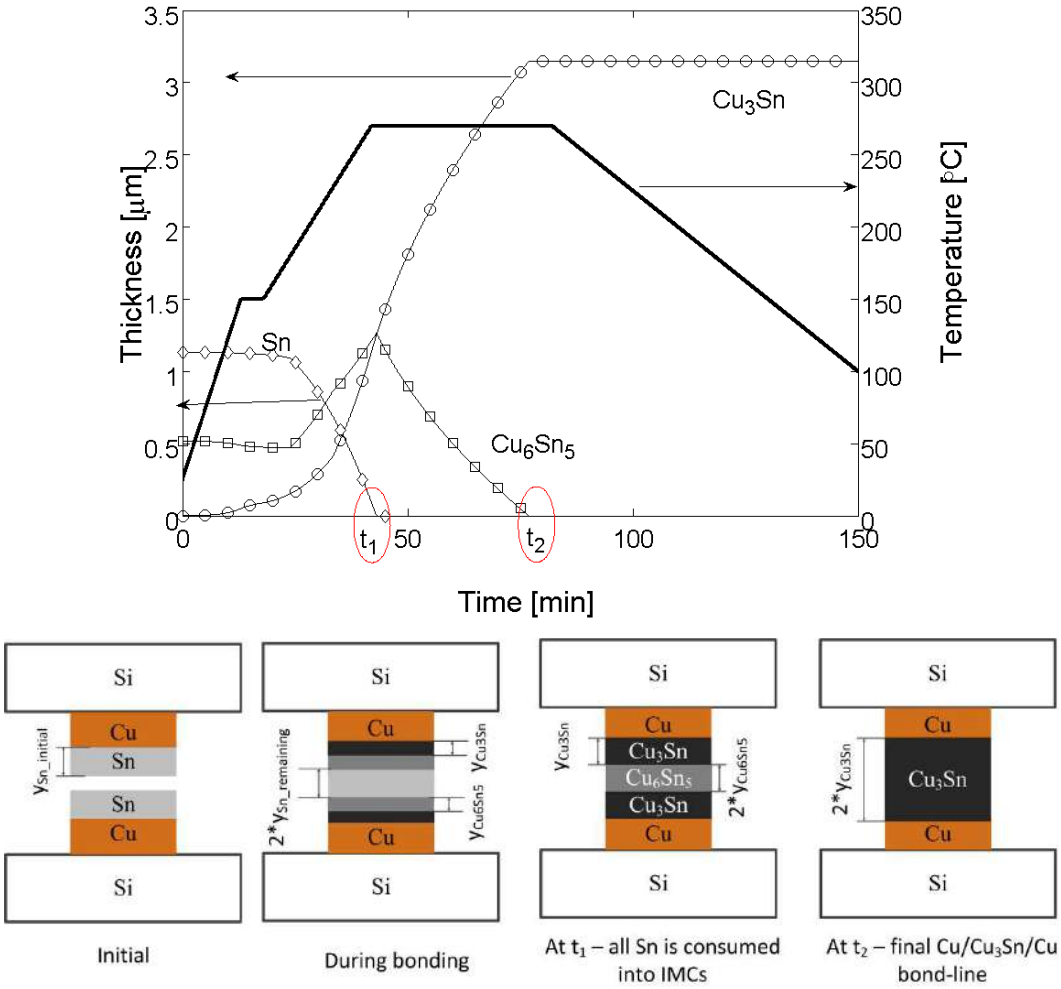

Figure 2.4: Simulation of IMCs development of Cu-Sn SLID bonding process. IMCs and Sn thickness are described as functions of temperature profile and initial Sn thickness. At t_1, all Sn is consumed into IMCs. At t_2, the final Cu/Cu_3Sn/Cu bond-line is achieved. The modeling is published in article 1 [124].

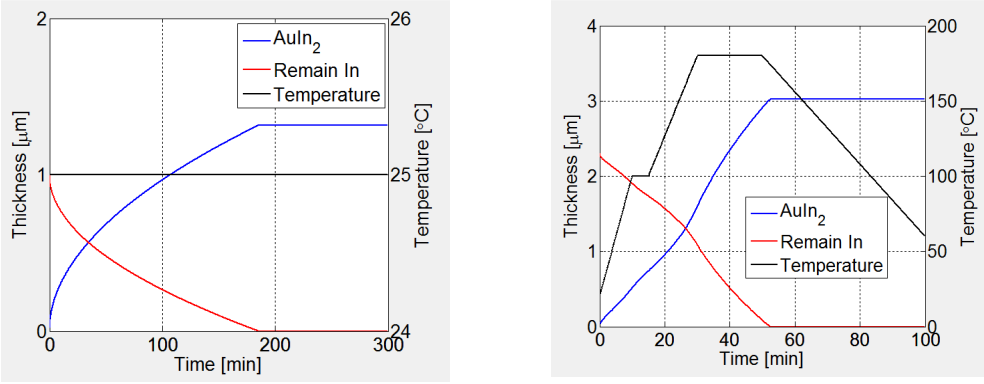

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Figure 2.5: a)$AuIn_2$ thickness development at room temperature storage and b) $AuIn_2$ thickness development during bonding process. Note that, in this simulation, only $AuIn_2$ growth is taken into account. When $AuIn_2$ reaches the maximum thickness, the reaction may continue and other Au-rich phases are formed. The modeling is not published.

2.4 Design rules for SLID wafer-level bonding

2.4.1 Material selection

Two material systems that have been investigated in this thesis work are Cu-Sn and Au-In SLID. In the section below, the advantages and disadvantages of each material system will be presented.

Using a symmetric Cu-Sn SLID bonding enables a flux-less bonding. This technique is suitable for hermetic encapsulation and packaging of devices, which operate at high temperature. The most important advantage of Cu-Sn SLID is low cost compared to other SLID bonding techniques, such as Au-In, Au/Sn. Both metals used are low cost and can be deposited by using an electroplating process. In addition, the IMCs formation during bonding process is simple compared to other SLID systems, such as Ag/In, Au/Sn and Au-In, with only two equilibrium phases: Cu_3Sn and Cu_6Sn_5. Therefore, the bonding process is easily controlled. However, the limitation of this bonding technique is thick metal layer requirements (compared to thermocompression). Normally, the thickness of the final bond-line is up to above 10 µm.

Au-In SLID bonding is addressed to MEMS hermetic encapsulation. The most important advantage of this technique is the low bond temperature. Au-In can perform a strong and hermetic bonding at temperatures below 200 ^{o}C. Low process temperature reduces the thermal stress that occurs during bonding process and addressed to the packaging of temperature sensitive devices. Another advantage of Au-In bonding is that the strong and hermetic bond can be performed by using thin Au-In layer thicknesses. The successful bonding can be obtained with 1µm Au. However, the cost of this bonding technique is high. The two metals used are relatively expensive. In addition, Indium is sensitive to oxidation and requires deposition in an inert atmosphere.

2.4.2 Metal thickness design

2.4.2.1 Cu-Sn design principle

Requirements for Cu-Sn SLID bond structure design:

- Symmetric bond structure is used in order to enable flux-less bonding [87]. In a symmetric structure, Sn is deposited on both wafers.

- The initial Sn thickness must be above the critical Sn thickness to ensure there is Sn remaining on the surface when the melting point of Sn is reached. The critical Sn thickness depends on temperature profile and could be estimated by using IMCs modeling.
- For Cu-Sn SLID bonding, the desired final bond-line is Cu/Cu_3Sn/Cu. Therefore, the Cu-Sn thickness ratio must be larger than 1.32, the ratio of Cu-Sn thickness for full conversion to Cu_3Sn is estimated by:

$$\frac{y_{Cu}}{y_{Sn}} = \frac{m_{Cu(Cu_3Sn)}}{m_{Sn(Cu_3Sn)}} \frac{\rho_{Sn}}{\rho_{Cu}} = 1.32 \qquad \textbf{Eq 2. 4}$$

Here y_{Cu} and y_{Sn} are required Cu and Sn thickness, $m_{Cu(Cu_3Sn)}$ and $m_{Sn(Cu_3Sn)}$ are Cu and Sn mass in Cu_3Sn, ρ_{Cu} and ρ_{Cu} are Cu and Sn mass density.

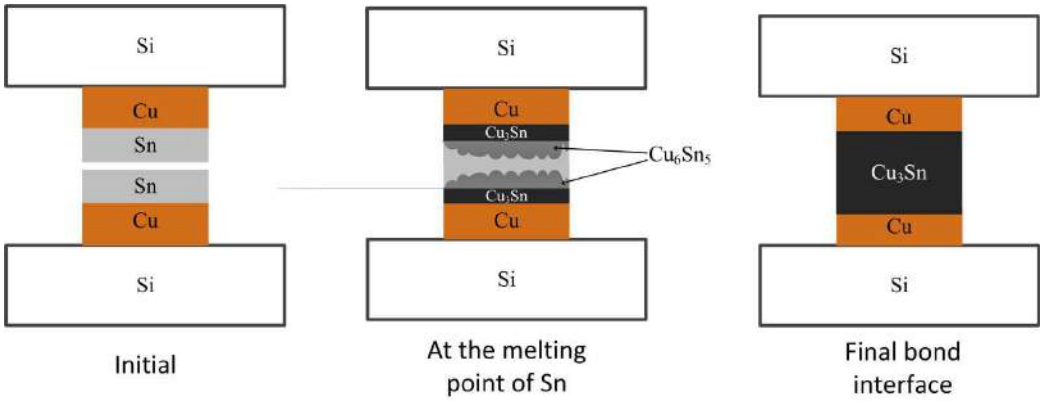


Figure 2.6: Requirements of Cu-Sn SLID bond structure design.

2.4.2.2 Au-In design principle

The requirements of Au-In SLID bond structure design are presented in Figure 2.7. Different from Cu-Sn bonding, In is only deposited on one wafer and the final bond only consists of IMCs.

- For Au-In, the most critical challenge is rapid formation of $AuIn_2$, which may consume all In into IMC and cause fail bonding, even at room temperature storage. There are two solutions to tolerate the formation of $AuIn_2$: 1) use Ti as diffusion barrier between Au and In to eliminates the formation of $AuIn_2$ at room temperature [121]; 2) design Au-In thickness with surplus In to ensure there is In remaining on the surface prior to bonding. This contradicts to “standard” SLID

requirement with surplus high melting component. In this work, solution 2 is selected. Therefore the In/Au initial thickness ratio must be larger than 3.1 – is the In/Au thickness for full conversion to $AuIn_2$ and estimated by:

$$\frac{y_{In}}{y} = \frac{m_{In(AuIn_2)}}{m_{Au(AuIn_2)}}\frac{\rho_{Au}}{\rho_{In}} = 3.1 \qquad \textbf{Eq 2. 5}$$

Here y_{In} and y_{Au} are In and Au thickness, $m_{In(AuIn_2)}$ and $m_{Au(AuIn_2)}$ are In and Au mass in $AuIn_2$, ρ_{In} and ρ_{Au} are In and Au mass density.

With In/Au thickness ration larger than 3.1, In surplus $AuIn_2$ formation. Therefore, even all Au reacts with In to form $AuIn_2$, there is pure In available prior to the bonding.

- There should be pure In available on the surface when the melting point of In is reached.
- The overall In/Au thickness ratio depends on the targeted final bond interface. For examples, for the targeted IMC is Au_xIn_y, the required In/Au thickness is estimated by:

$$\frac{y_{In}}{y_{Au}} = \frac{m_{In(Au_xIn_y)}}{m_{Au(Au_xIn_y)}}\frac{\rho_{Au}}{\rho_{In}} \qquad \textbf{Eq 2. 6}$$

Here y_{In} and y_{Au} are In and Au thickness, $m_{In(Au_xIn_y)}$ and $m_{Au(Au_xIn_y)}$ are In and Au mass in Au_xIn_y, ρ_{In} and ρ_{Au} are In and Au mass density. Table 2.3 shows the required In/Au thickness ratio for different targeted IMCs.

Table 2.3: Required Au-In thickness ratio for different targeted IMCs

Phase	m_{In}/m_{Au}	y_{In}/y_{Au}
$AuIn_2$	54/46	3.1
AuIn	37/63	1.34
γ (Au_7In_3)	20/80	0.66
ε	15.5/84.5	0.49
β_1	14/86	0.43
ζ	8/92	0.23
α_1	5/95	0.14

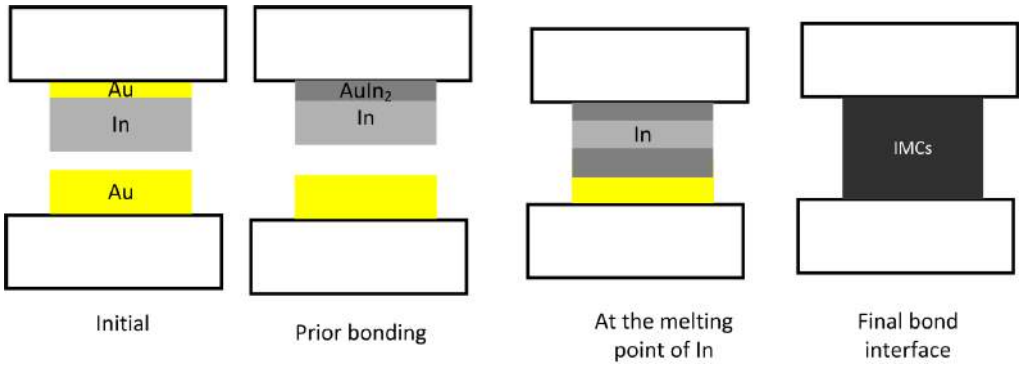


Figure 2. 7: Design principle for Au-In SLID bonding

2.4.3 Metal deposition

Two metal deposition methods were used in this thesis: electroplating and thermal evaporation.

For Cu-Sn bonding, thick metal thickness is required. Therefore the electroplating method is selected. Photoresist AZ4562 was used as the mask and Au was used as the seed layer for the electroplating process. In order to avoid Cu oxidation, the Sn is electroplated immediately after Cu electroplating. The Cu-Sn wafer fabrication process is shown in Figure 2.8.

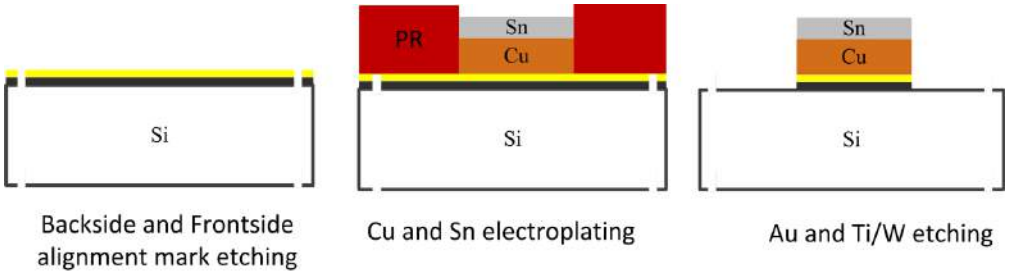


Figure 2. 8: Cu-Sn wafer fabrication process

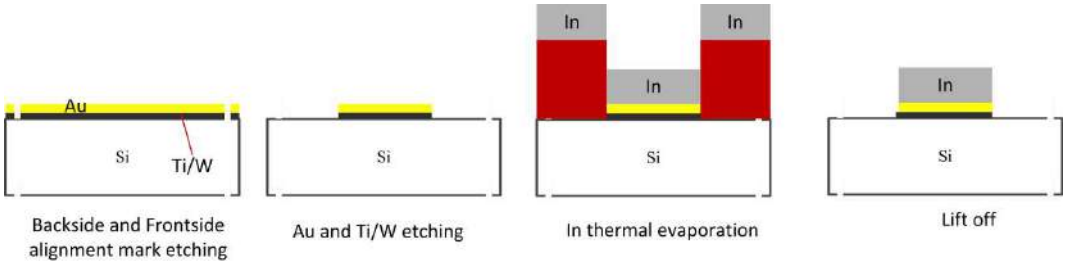


Figure 2. 9: Au-In wafer fabrication process

For Au-In bonding, the thickness of In layer is thin, thermal evaporation method was selected for metal deposition. The Au-In wafer fabrication process is shown in Figure 2.9. Photoresist was used as mask for In thermal evaporation. After evaporation, photoresist was removed by lift-off process.

2.4.4 Bonding process

For both Cu-Sn and Au-In bonding, a two-steps bond temperature profile was selected in order to reduce squeeze out of Sn and In. A description of the two-steps bond temperature profile is shown in Figure 2.10. The temperature is raised to the contact temperature T_c where the wafers are brought into contact and bond pressure is applied. The contact temperature is below the the melting point of low melting component T_m. Wafers are kept at T_c for several minutes and then raised to the bonding temperature T_b that is above T_m. When the bonding process is finished, the temperature is ramped down and bond pressure is released.

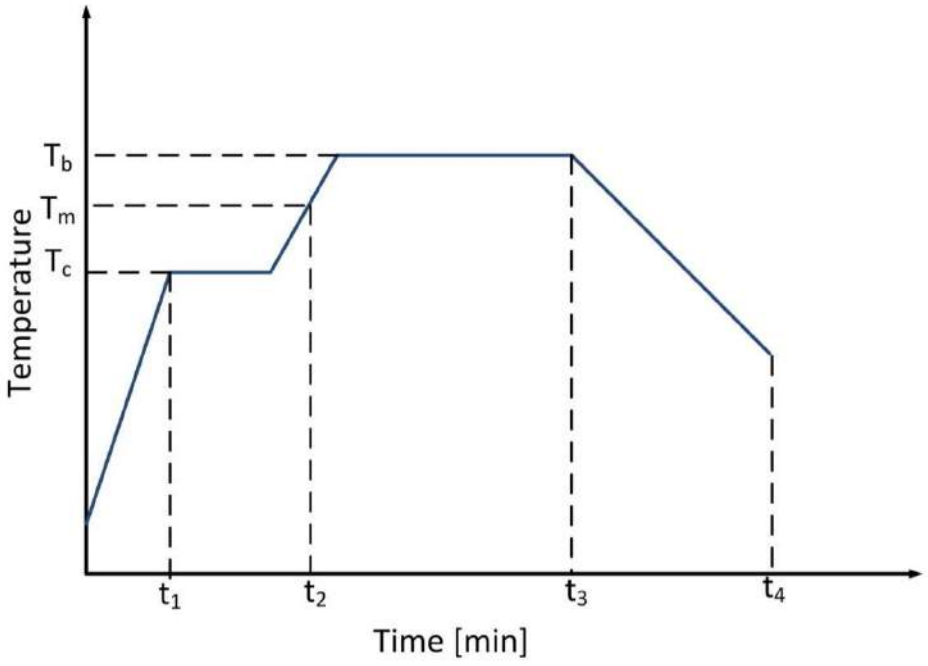


Figure 2.10: Typical two steps SLID bonding profile. In a two steps bond profile, the temperature is ramped up to the contact temperature T_c that is below the melting point of low melting component T_m. At contact temperature, the wafers are brought into contact and bond pressure is applied. Wafers are kept at T_c for several minutes. Then, the temperature is ramped up to bonding temperature T_b which is above the melting point of the low melting component.

2.5 Characterization of bond performance

2.5.1 Cross-section investigation

Cross-section characterization is a common method to investigate the microstructure of bonded samples, the voids formation during bonding process and the material changes. In this study, the cross-section of the SLID bonded samples is investigated by using optical microscope, SEM and EDS. Optical microscope is used for general observation of the bond interface. With a well-prepared cross-section, voids formation could be observed by optical microscopy. SEM and EDS were used for further investigation of the intermetallic composition. The cross-section of the samples was prepared by using mechanical polishing and ion milling methods.

2.5.1.1 Mechanical grinding/polishing

Mechanical grinding/polishing is the traditional method to prepare cross-sections. The sample is molded in Struers EpoFix and cured at room temperature for 8-9 hours. The molded sample is grinded using SiC paper. One of the challenges of mechanical polishing is that the sample is damaged by mechanical force. In order to avoid this mechanical effect, the sample is hold carefully and grinded slightly during polishing process. Three grinding steps are used using different SiC paper with different roughness. Finally, sample is polished using diamond powder (Ø3 µm and Ø1 µm). Figure 2.11 shows the typical cross-section micrograph of a Cu-Sn bonded sample, which is prepared by mechanical polishing. The final Cu/Cu_3Sn/Cu bond-line is clearly observed. However, the contaminants from mechanical grinding/polishing process can fill the voids and holes. Therefore, as shown in Figure 2.11, for typical mechanical grinded/polished samples, the voids could not be observed.

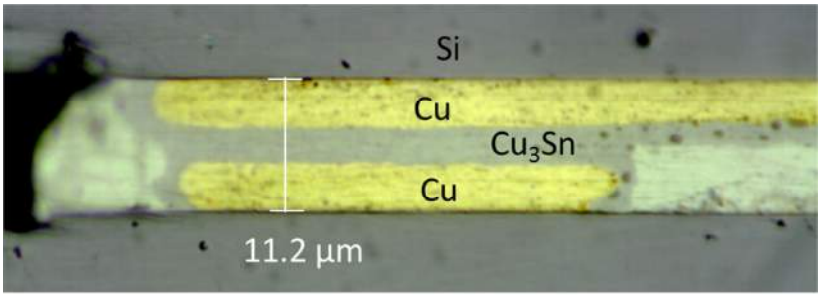


Figure 2.11: Cross-section of a Cu-Sn bonded sample prepared by mechanical polishing. Three different layers: Cu, Cu_3Sn and Cu are clearly observed. Sample is bonded by Sensonor As.

2.5.1.2 Ion milling

In addition to mechanical polishing method, Hitachi Ion miller IM4000 was used for preparing cross-section. A visible picture of the equipment is shown in Figure 2.12. There are two different ion milling modes: flat milling and cross-section milling. The Argon ion gun is used to remove material. On the specimen stage, we can adjust the eccentricity distant (distant from the center of the sample to the center of the ion beam) and angle of the sample. On the control panel, we can set up and adjust Ar gas flow, milling time, accelerated voltage, discharged voltage and milling mode.

Figure 2. 12: Hitachi Ion miller IM4000.

Flat ion milling

Flat milling is used to further polish the cross section of samples prepared by mechanical grinding/polishing. An illustration of flat milling mode is shown in Figure 2.13. During the milling process, the samples holder iterates around the rotation center with specimen iteration angle $\pm\varphi$ (the angle of the movement from the center of specimen) and specimen iteration speed ω (the number of movements per min). The ion gun bombards the samples surface and removes the material on the surface. The milled area is dependent on the ion beam irradiation angle (θ) and the amount of eccentricity. The milling rate is dependent on the acceleration voltage (V) and gas flow (R).

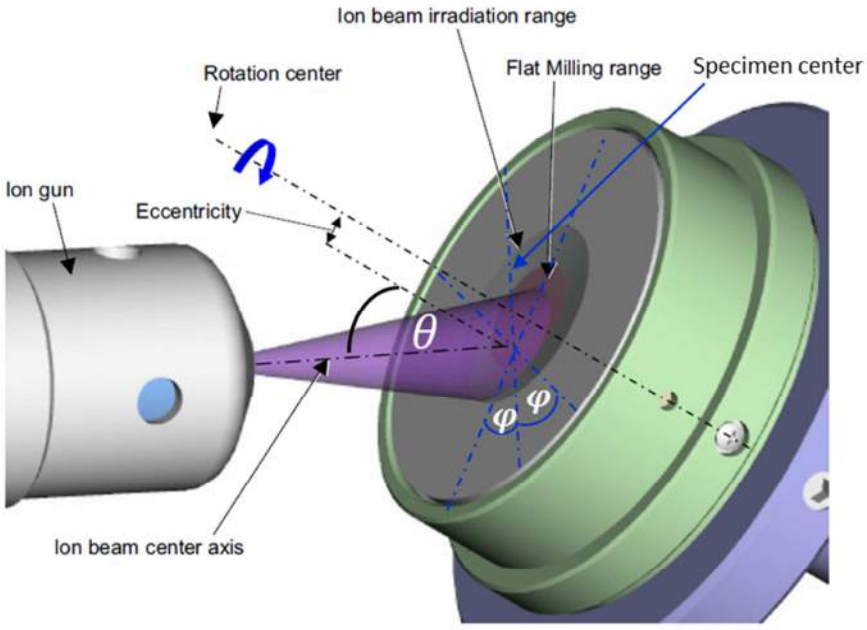


Figure 2.13: Schematic of flat mode milling configuration [130].

Flat milling mode F4 [130] (specimen iteration speed ω = 15 reciprocations/min and specimen angle $\varphi = \pm 60^{o}$) was selected. Two steps milling was used. The parameters of each step are shown in Table 2.4. The first milling step, a small ion beam irradiation angle (θ=60^{o}) and high-accelerated voltage (6 kV) were used in order to remove the material and contaminants on the surface. The second milling step, a large ion beam irradiation angle and lower accelerated voltage were used in order to polish and achieve uniformity of the flat surface. The micrograph of a cross-section sample after flat milling is shown in Figure 2.14. Different from typical mechanical grinded/polished samples, the voids are clearly observed for the flat milled samples.

Table 2.4: Parameters of two steps flat milling for samples polishing.

	Mode	**Voltage**	***θ***	**Gas flow**	**time**
Step 1	F4	6 kV	60^{o}	0.09 cm^{3}/min	5 min
Step 2	F4	4 kV	80^{o}	0.09 cm^{3}/min	20 min

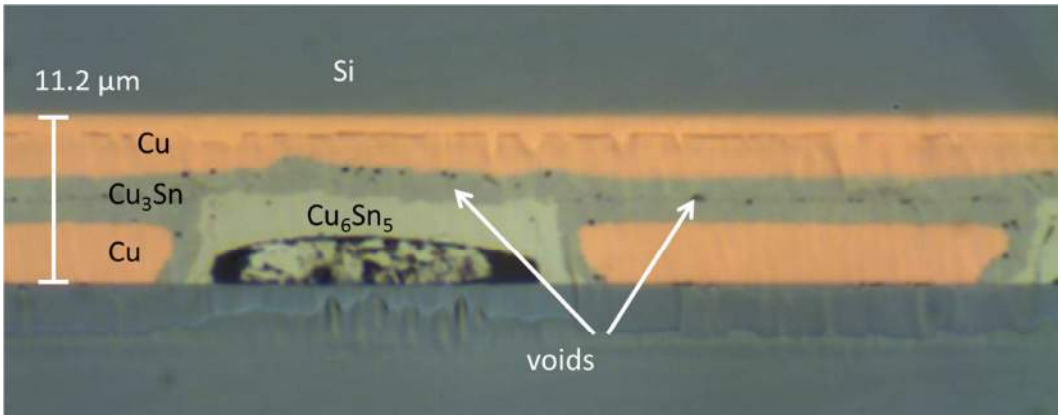


Figure 2.14: Cross-section of Cu-Sn bonded sample prepared by mechanical polishing and further polished by flat ion milling. Different material layers (Cu, Cu_3Sn, Cu_6Sn_5) and the interface between these layers are clearly observed. The voids in the bond interface are clearly observed after flat milling. The sample is bonded by Sensonor As.

Cross section milling

The Cross-section milling mode is used to prepare cross-section samples directly from diced sample. Illustration of cross-section milling mode configuration is shown on Figure 2.15. The sample is mounted to the sample holder. A hard metal plate was used as blocking plate. During the milling process, the holder rotates around the center with swing speed ω (the number of swings per minute) and swing angle$\pm\varphi$. The ion gun bombards the samples and removes the material layer by layer.

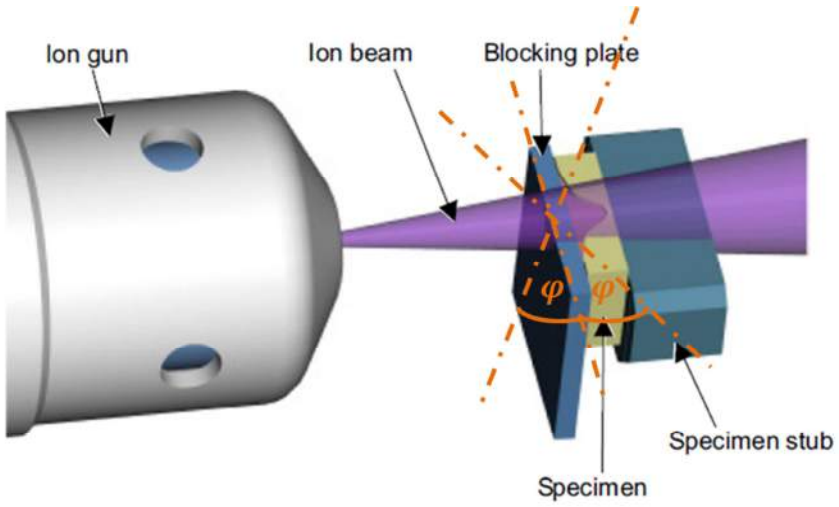


Figure 2.15: Schematic of cross-section milling mode configuration [130]

In this study, the cross-section milling mode C6 (swing speed ω = 23 reciprocation/min and swing angle $\varphi = \pm 40^{o}$) was used. The milling parameters are shown in Table 2.5.

Note that for as-deposited sample, a thin glass plate (200 µm) was attached on the metal surface in order to protect the soft metal layers. The cross-section of a cross-section milled sample is shown in Figure 2.16. Different material layers and layer interface are clearly visible. The voids that introduce in the bond interface are also clearly observed.

Table 2.5: Parameters for cross-section milling of as-deposition sample and bonded sample

	Mode	Voltage	Gas flow	Time
As-deposited sample	C6	6 kV	0.09 cm^3/min	2 h
Bonded sample	C6	6 kV	0.09 cm^3/min	3 h

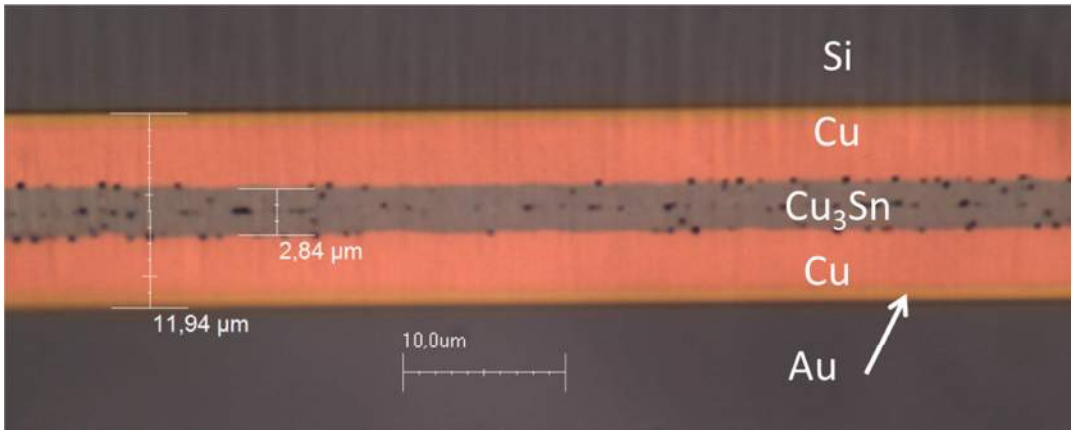


Figure 2.16: Cross-section of a Cu-Sn bonded sample which is prepared by cross-section milling. Different material layer (Au, Cu, Cu_3Sn) and the interface between these layer are apparently visible. Voids are clearly observed.

Compared to the mechanical grinding/polishing method, ion milling has several advantages:

- The mechanical effect is eliminated
- Micrograph of the cross-section is clear, even voids and grain structure could be observed

2.5.2 Bond strength testing

Bond strength is considered as an important property of the packaging. This property gives general information about the mechanical integrity of the systems and the potential weakness. Bond strength measurement is also performed for quality control inspection of the industrial process [131, 132].In this study, shear testing was used for bond strength testing.

Shear testing is a common method to characterize the bond strength of a bonded sample. This is a fast, robust, simple and cost-effective test method. The important parameters of shear testing are: test height (the height of the shear tool from substrate), test speed (the speed of shear tool movement), sample alignment and the tested temperature. In this study, we used NordsonDage 4000Plus shear-tester for the shear test.

2.5.2.1 Test vehicles design for shear testing

The test vehicles design for shear test is shown in Figure 2.17. Chip size is 1.8 x 3.4 mm^2 and substrate size is 6 x 6 mm^2. Each substrate and die contains two bond pads with pad size is 0.8 x 1.0 mm^2.

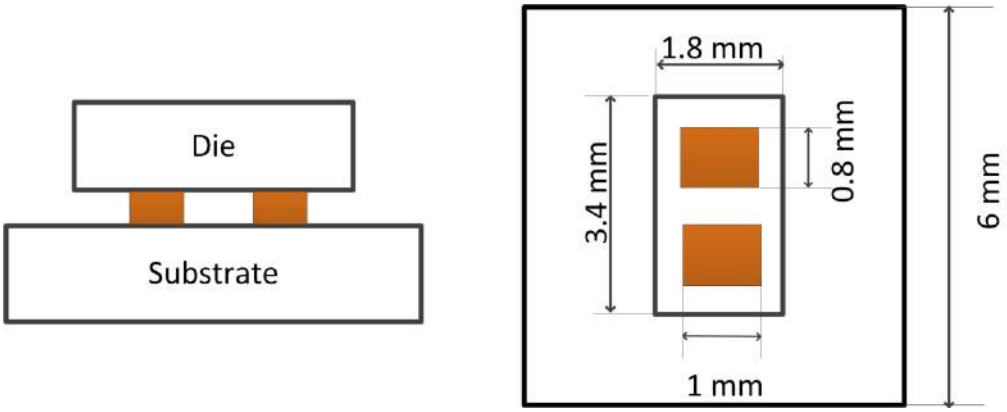


Figure 2.17: Test vehicles design foe shear strength measurement at elevated temperature.

2.5.2.2 Shear testing configuration

The test configuration of the shear tester is shown in Figure 2.18. A customized-holder is used to align the sample and prevent the rotation of the sample during shear test. The samples holder is attached to a hot plate. The temperature of the hot plate is controlled by a proportional-integral-derivative (PID) controller. A test height of 75 µm and a shear speed of 10 µm/s were used. The shear strength of the bond is calculated by:

$$\tau_S = \frac{F_S}{A} \qquad \textbf{Eq 2. 7}$$

Where F_S is the recorded shear force when the fracture occurs and A is bonded area.

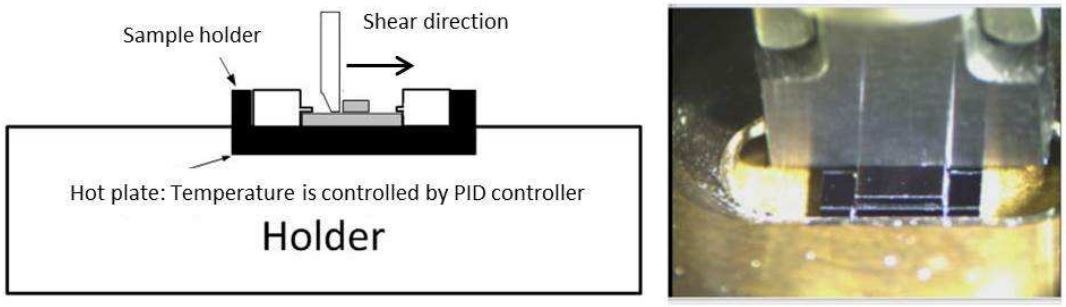


Figure 2.18: Illustration of shear test configuration. The bonded sample is attached and clamped to the hot plate, using a customized sample holder. The holder will reduce any misalignment of the die and prevent the rotation of the tested die during shear process. A PID controller controls the temperature of the hot plate. The entire temperature range was calibrated to ensure that the actual measured temperature on hot plate matches the indicated temperature on PID controller.

2.5.2.3 Temperature calibration

The calibration of the hot plate temperature was carried out in order to examine the PID indicator temperature. Different temperatures from room temperature to 300 ^{o}C were set up by PID. The actual hot plate temperature was measured by a thermometer. Figure 2.19 shows the measured temperature as a function of PID indicator temperature, showing that the actual temperature is linear dependent on indicator temperature. There is a slight difference between set up temperature and measured temperature. However, in our case, the difference is at acceptable level.

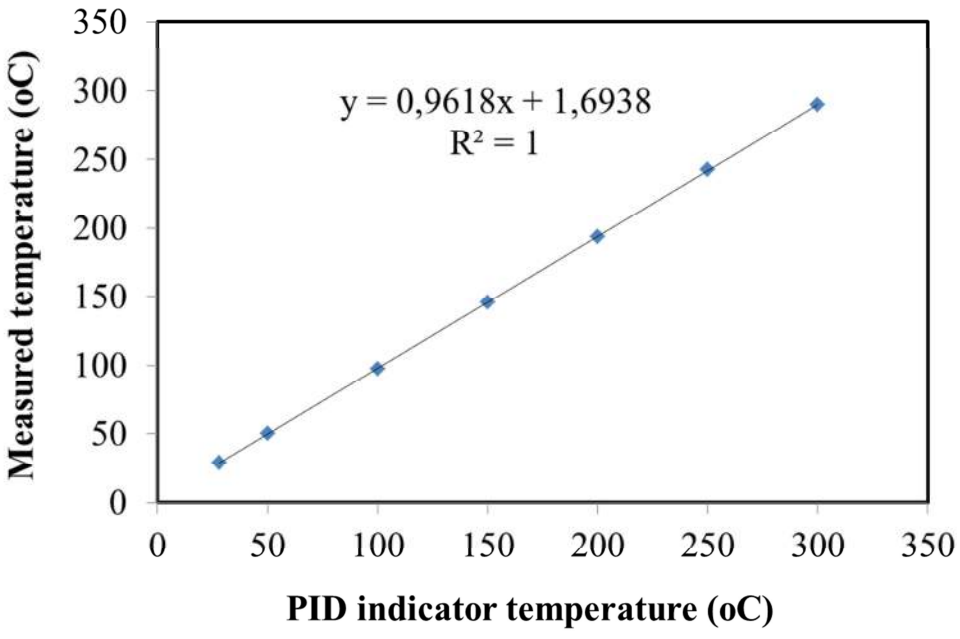


Figure 2. 19: The measured temperature as a function of PID indicator temperature.

2.5.2.4 Calibration of shear testing

With this shear test equipment, we can shear the bonded samples at elevated temperature. The temperature of the hot plate is controlled by a PID controller. One of the concerns is the actual temperature of the device under the test (DUT). The shear tool itself is not heated (only the stage is heated) and upon contacting the DUT, it will act as a heat sink and reduce temperature on the DUT. Thus, we conducted the following experiment where we positioned a thermocouple on a dummy Si chip during a shear test procedure at 300 ^{o}C to measure any temperature drop. Note that, the measured temperature is 290 ^{o}C, slightly lower than set up temperature.

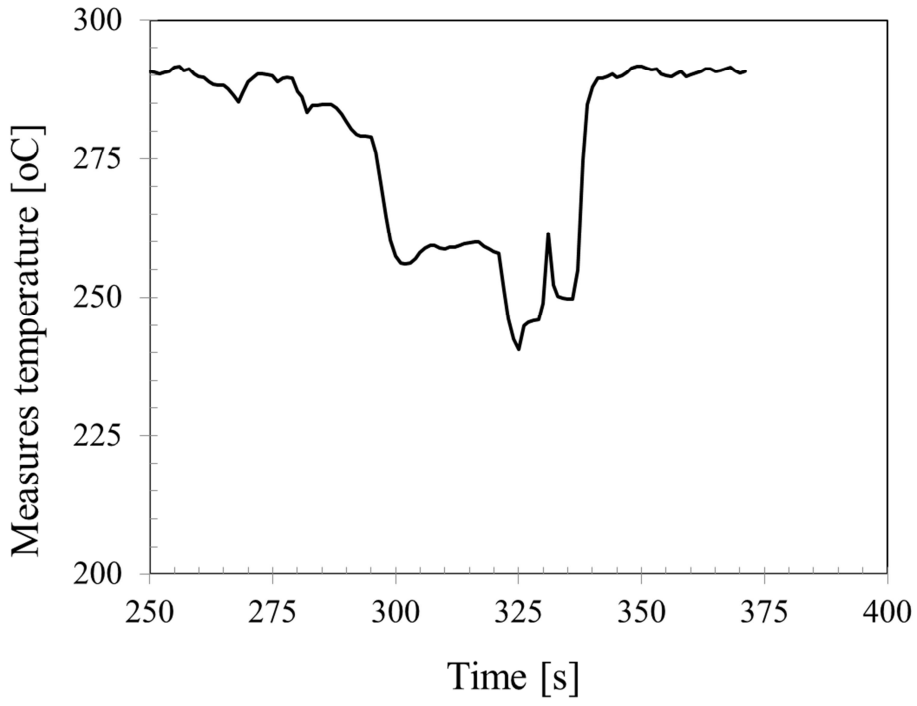


Figure 2.20: Measured temperature on the top of a dummy die during shear testing at 300^{o}C. The measured temperature is 290 ^{o}C. When the shear tool touches the die, the temperature drops down because the tool is a heat sink. When the fracture occurs; the temperature at the top die reduced to 250 ^{o}C. After the test is complete, the temperature quickly increases to 290 ^{o}C.

Figure 2.20 shows the measured temperature on the top of Si die during a shear test procedure. As evident, when the shear tool touches the die, and moves, the temperature is reduced. Depending on the duration of contact, when a fracture occurs, the temperature on the top die from this experiment can be estimated to drop about 50 ^{o}C. Our bonded samples are symmetric; therefore we can estimate that the minimum temperature on any Cu-Sn bond interface would be at least 275^{o}C for a test temperature

of 300 ^{o}C. Further characterization of temperature at the DUT was not carried out, as we view the results satisfactory to and the test setup repeatable since it will be identical for all temperatures.

2.5.3 Fractography

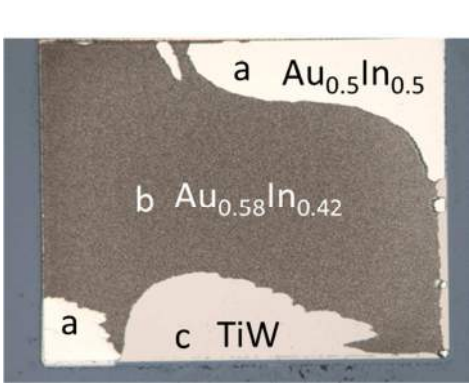
Fractography is the investigation of the sheared fracture surfaces. This is an effective method to determine the fracture mode of the sheared sample and the weakest material or interface of the bonded sample. In this study, optical microscope, interferometer, SEM and EDS were used for fracture characterization.

An example of a fractography analysis of an Au-In sheared sample is shown in Figure 2.21. The optical microscopy picture and EDS analysis shown in Figure 2.21a indicates that there are three different fracture surfaces. The height profile in Figure 2.21b indicates that these surfaces have different height, and each surface is planar. We can extract the area fraction of these fracture surfaces by using bearing ratio analysis.

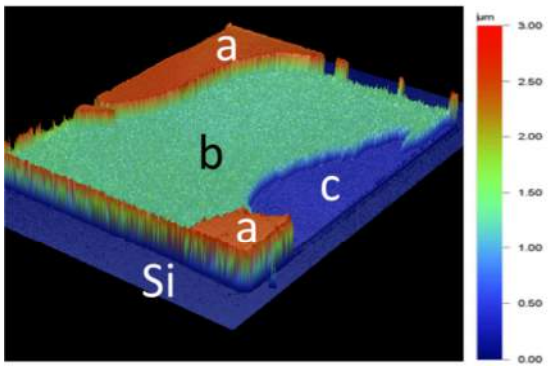
The filter bearing ratio analysis calculates the bearing ratio t_p, the ratio of the bearing area to the total surface area. The bearing area is the area of the surface cut by a plane at a particular height [133]. The bearing curve shows t_p in relation with the profile level. For this particular sample, the total bond pad area is 66.5 %. The fraction of each fracture surface area could be estimated by:

$$fr_* = \frac{Br_*}{Br_{total}} \qquad \textbf{Eq 2. 8}$$

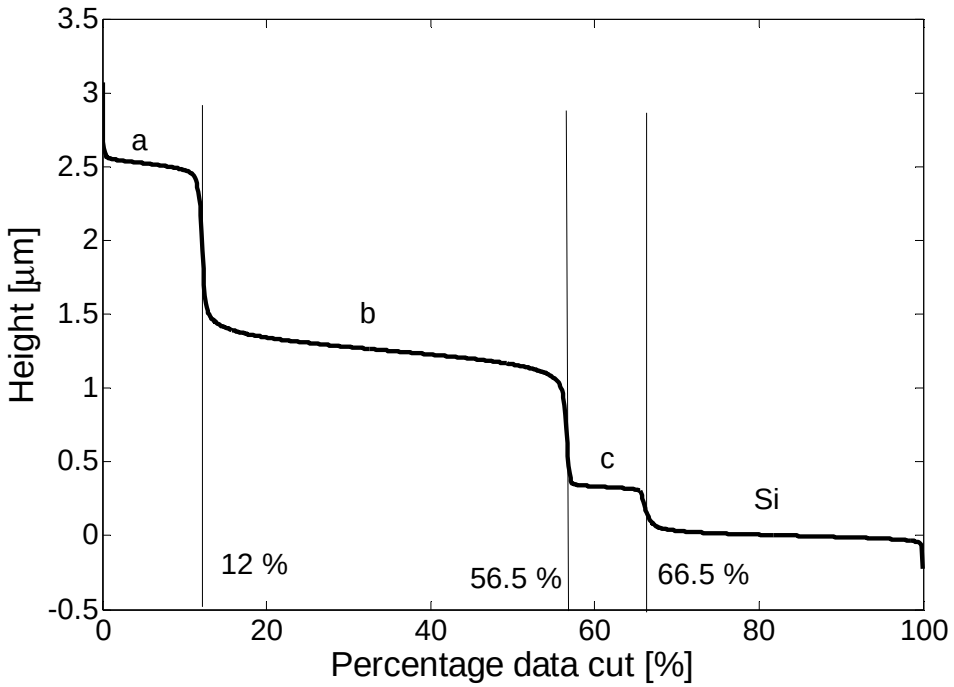
Where Br_* is the bearing ratio of surface *, Br_{total} is total bearing ratio of the pad. For this particular case, the area fraction of surface a, b and c are 18.8 %, 66.2 % and 15 % respectively.



a. Microscope picture and SEM analysis



b. Height profile



c. Bearing ration analysis

Figure 2.21: Fractography of an Au-In sheared sample a. microscope picture and SEM analysis, b. height profile and c. bearing ratio analysis

The bearing ratio only takes into account the measureable data. In the case the fracture surface contains the regions that the height could not be measured by interferometer, the bearing ratio must be calibrated. One example of this fracture surface is shown in Figure 2.22. The fracture surface contains four different fracture modes a, b, c and d; where the height of surface d could not be measured by interferometer. The area fraction of this surface (d) over total area is 20 %. The calibrated bearing ratio (*Br_calibrated*) is estimated by:

$$Br_{Calibrated} = Br * (1 - 0.2) \quad \text{Eq 2. 9}$$

For this particular sample, the bearing ratio given by interferometry, calibrated bearing ratio and area fraction of different fracture surfaces are shown on Table 2.6.

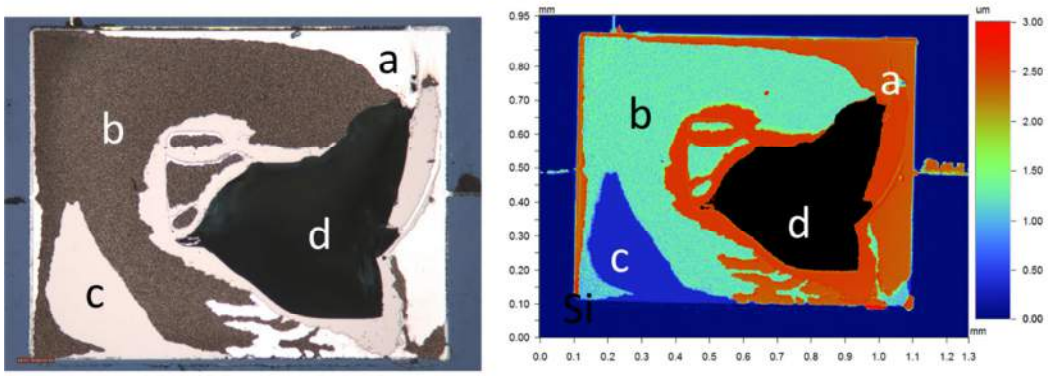


Figure 2.22: Fractography which contains four different fracture surfaces a, b, c, and d; where the height of surface d could not be measured by interferometer.

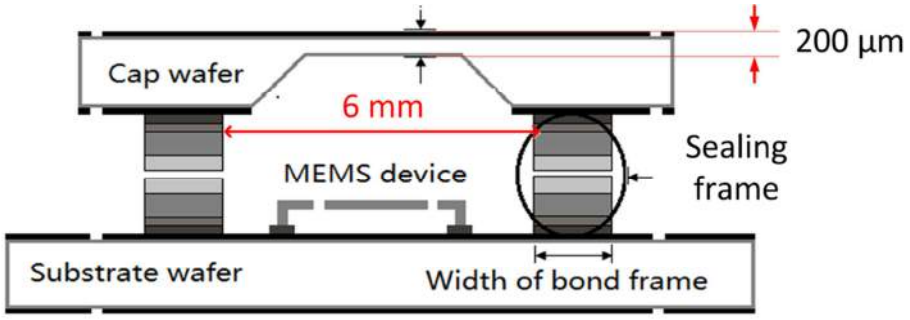
Table 2.6: Calibrated bearing ratio and are fraction of different fracture surfaces shown in Figure 2.15.

Area	a	b	c	d	total
Bearing ratio Br (%)	23.5	31.5	7.5	--	62.5
Calibrated Br (%)	18,8	25,2	6	20	70
Fraction fr (%)	26.9	36	8.6	28.5	

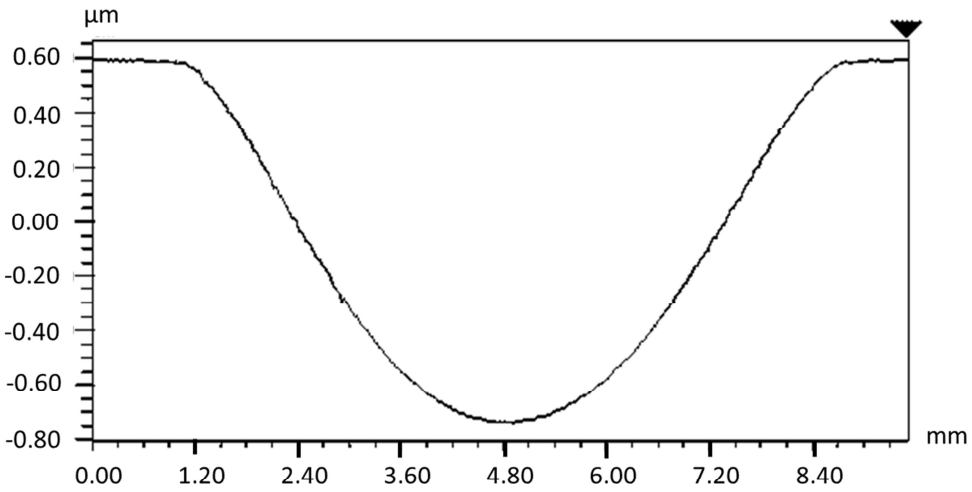
2.5.4 Bonding yield investigation

For SLID wafer-level bonding, due to the non-uniformity of the metal deposition process, one may introduce several un-bonded areas on the wafers where the metal layer thickness is thinner than in other areas of the wafer [89, 118]. Therefore, in addition to shear test, bonding yield is one of the used methods in order to evaluate the performance of wafer-level bonding. In this study, dicing yield (the percentage of dies that remains after dicing) and sealing yield (the percentage of the dies that vacuum remains inside the cavity after bonding) were used for evaluation of the performance of the bonding. While the shear test gives information about the mechanical integrity of the bonded samples, the bonding yield gives general information about the bond performance on the whole bonded wafers. The dicing yield could be observed after wafer dicing.

In order to investigate the sealing yield, the membrane deflection method is used to examine if the vacuum remains inside the cavity after bonding. The test structure for sealing yield verification is shown in Figure 2.23a. The membrane is performed on cap wafer using silicon etching. The thickness of membrane is 200 µm. The dimension of membrane is ~6 x 6 mm^2.



a. Test vehicles design for hermetic test.



c. Membrane deflection after bonding

Figure 2.23: Test structure design for hermetic verification by membrane deflection method and typical membrane deflection profile of a sealed sample.

The wafers are bonded in a vacuum environment. If the wafer is hermetically sealed, the vacuum remains inside the cavity when the bonded wafers are exposed to the atmosphere. Due to the differential of external and internal pressures inside the cavity, the membrane is deflected. For a square membrane, the differential pressure could be estimated by [134]:

$$P_{diff} = C_1 \frac{y w_0}{a^2}\sigma + C_2 \frac{y w_0^3}{a^4}\frac{E}{1-\nu} + C_3 \frac{E}{1-\nu^2}\frac{y^3 w_0}{a^4} \qquad \textbf{Eq 2. 10}$$

Where $w_0$is the maximum deflection at the center of membrane, a is half of membrane length, $\sigma$is residual stress, E is Young's modulus, $\nu$is Poisson ratio of the membrane material, y is membrane thickness. $C_1 = 3.4057$, $C_2 = 1.84$ and $C_3 = 4.129$ are coefficients, which are dependent on geometry. With small deflection w_0 and zero residual stress, the differential pressure could be estimated by

$$P_{diff} = 4.129 \frac{E}{1-\nu^2} \frac{y^3 w_0}{a^4} \quad \textbf{Eq 2. 11}$$

Typical membrane deflection of a hermetic sealing cavity is shown in Figure 2.23b. The deflection of membrane was measured by interferometer.

For our case, <100> silicon membrane, E =130 GPA, $\nu = 0.278$, y = 200 µm, a = 3 mm. Therefore:

$$P_{diff}\ (bar) = 0.6 \times w_0\ (\mu m) \quad \textbf{Eq 2. 12}$$

For this particular sample, the maximum deflection of membrane is 1.4 µm, then P_{diff} = 0.84 bar and the pressure inside the cavity is 0.16 bar. In our case, the accuracy of the pressure measurement could be limited for several reasons: the membrane thickness is uncertain and the residual stress is un-known. Therefore, in order to determine the accurate pressure for a hermeticity test, this method is not good enough. However, the measurement can determine if there is a difference of pressure inside the cavity and outside the cavity, and initially evaluate if the die is sealed or not.

3 Summary of articles

3.1 Article I, II

Article I:

Thi-Thuy Luu, Ani Duan, Kaiying Wang, Knut E. Aasmundtveit and Nils Hoivik, *"Optimization of Cu-Sn wafer-level bonding based upon intermetallic characterization"*, 4th Electronic System-Integration Technology Conference (ESTC 2012), September 17-20, 2012, Amsterdam, Netherland.

Article II: this article is extended from article 1

Thi-Thuy Luu, Ani Duan, Knut E. Aasmundtveit and Nils Hoivik, "Optimized Cu/Sn wafer-level bonding using intermetallic phase characterization", Journal of Electronic Materials 2013, Vol 42(12), 2013, pp. 3582-3592.

My contribution: literature review, design, experiment, characterization, estimation of kinetics coefficients, numerical modeling, and manuscript preparation

For Cu-Sn SLID bonding, the formation of IMCs during bonding process is one of the critical issues to the bond performance. The successful bonding is only obtained if there remains pure Sn at the melting point of Sn (T_m). However, in a Cu-Sn bonding process, the temperature is raised following a defined temperature profile. The IMCs are formed during the ramping process, even below the T_m and an amount of Sn would be consumed into IMCs. The challenge is to predict how much Sn remains at T_m which does not only depend on the initial Sn thickness, but the amount of Sn that has been consumed to form IMCs. Therefore, there is a need of a simulation model for IMCs

development during Cu-Sn bonding process, which can predict how much Sn, remains at the melting point of Sn. The motivation of this work is to implement a numerical simulation model for IMCs development during Cu-Sn bonding process. With this simulation model, we can predict the critical parameters of the bond temperature profile: the Sn thickness that remains at the melting point of Sn, the time that all Sn are consumed to form IMCs and the time that final $Cu/Cu_3Sn/Cu$ bond-line is obtained.

Main results:

In order to simulate the IMCs thickness growth during Cu-Sn SLID bonding process, the formation of IMCs during Cu-Sn annealing process was fully characterized. It is well known that the two IMCs that form during Cu-Sn annealing process are Cu_3Sn and Cu_6Sn_5. In this study, the initial characterization focuses on growth kinetics model of Cu_3Sn growth thickness and the amount of Sn thickness that is consumed into IMCs. The as-electroplated Cu-Sn samples were annealed at different temperatures (150 ^oC to 300 ^oC) and annealing times (0 min to 320 min). The kinetics coefficients are then extracted from the measured IMCs thicknesses of the annealed samples.

Based upon the estimated kinetics coefficients, a numerical simulation model for IMCs thickness development during Cu-Sn bonding process was implemented, using MATLAB. With this simulation, the IMCs thickness (Cu_3Sn and Cu_6Sn_5) and the remaining Sn thickness on the surface are described as functions of initial Sn thickness and bond temperature profile. The actual bonding experiments were carried out in order to evaluate the simulation model. According to our characterization, the measured IMCs thicknesses match the simulated thicknesses. This verifies the accuracy of simulation model, and the model could be used as a tool for process design and optimization.

According to the simulation model, for an initial Sn thickness of 1.5 µm, successful bonding could be obtained by using two steps temperature profile. In this two steps temperature profile, the temperature is ramped to contact temperature (150 ^oC) where the wafers are brought into contact and kept at 150 ^oC for 5 min. The temperature is then ramped to bond temperature 270 ^oC. To achieve final $Cu/Cu_3Sn/Cu$ bond interface, the bonding time should be longer than 30 min.

3.2 Article III

Thi-Thuy Luu, Ani Duan, Kaiying Wang, Knut E. Aasmundtveit and Nils Hoivik, *"Cu/Sn SLID wafer-level bonding optimization"*, proceeding of Electronic Components and Technology Conference (ECTC), 2013 63rd, May 28-31 2013, pp. 1531-1537.

My contribution: mask design, fabrication, characterization and analysis of experiment result.

The objectives of this study is to further investigate the effect of different bonding parameters, include initial Sn thickness, bond pressure and bond temperature profile to Cu-Sn SLID bond performance. Bond performance was evaluated by bonding yield (dicing yield: the percentage of dies that remains after dicing; sealing yield: the percentage of dies that vacuum remains inside after bonding).

Main results:

The experimental results confirm that: high bonding yield is achieved if there is pure Sn at the bond surface when the melting point of Sn is reached. For our actual bonding, a Sn thickness of 1.5 μm should be used in order to minimize the squeeze-out of Sn, and tolerate the non-uniformity during Cu/Sn plating process. A moderate bond pressure will give high bond yield. With bond pressure of 1.5 MPa, bond temperature of 270oC and initial Sn thickness of 1.5 μm - dicing yield of 100% and sealing yield of 80 % waere obtained.

3.3 Article IV

Ani Duan, Thi Thuy Luu, Kaiying Wang, Knut E. Aasmundtveit and Nils Hoivik, *"Wafer-level hermetical Cu-Sn micro-joints with high mechanical strength and low Sn flow"*, submitted to Journal of Micromechanics and Microengineering.

My contribution: modelling of IMCs development during bonding process, part of mask design and characterization, process optimization, description of modeling part in manuscript.

The objective of this work is to demonstrate Cu-Sn SLID wafer-level bonding for MEMS hermetic encapsulation. For hermetic encapsulation, shrinkage of sealing frame width is one of the important issues. With small sealing frame width, the size of the final product could be reduced and the volume of production could be improved. However, one of the concerns is how much we can shrink the frame width; since with a small frame width, the performance of the bonded samples could be affected. In this study, we investigated the effect of Cu-Sn sealing frame with on bond performance. In addition, the effect of the bond pressure and the temperature profile were further investigated. The bond performance was evaluated by bond yield and bond strength.

Main results:

We demonstrated Cu-Sn SLID wafer-level bonding with high yield and less Sn squeeze-out for MEMS encapsulation. The minimum frame width we could achieve is 80 µm. To obtain high bond performance, a bond pressure higher than 1.5 MPa should be used. A two-steps temperature profile (described in chapter 2) can reduces the squeeze-out of Sn.

3.4 Article V

Thi Thuy Luu, Nils Hoivik, Kaiying Wang, Knut E. Aasmundtveit and Astrid-Sofie Vardoy, *"Cu-Sn SLID wafer-level bonding for high temperature application"*, manuscript accepted to be published on Metallurgical and Materials Transactions A.

My contribution: literature review, mask design, assembly, characterization and test, analysis, and manuscript preparation.

For the applications that require operating at high temperature, long-term reliability will be challenged due to the increase of thermal stress, material corrosion and other effects. Therefore, it is important that the materials used in a bond-line have a high melting point as well as a high mechanical integrity at high temperatures. Furthermore, the bond-line should have high thermal conductivity to reduce any thermal stress in the bond stack, and be thermodynamically stable to reduce any corrosion from diffusion at high temperature. Cu-Sn SLID wafer-level bonding is a promising set of materials suitable for these applications, as it enables low cost metallization, flux-free bonding,

high mechanical strength and hermeticity. The objective of this study is to demonstrate Cu-Sn SLID wafer-level bonding for high temperature applications. The mechanical integrity of Cu-Sn SLID bonded samples at elevated temperatures up to 300 ^{o}C was investigated.

Main results:

Cu-Sn SLID wafer-level bonding results in a high yield bonding and high mechanical integrity at high temperatures. The resulting bond strength show relatively small variation in strength as a function of temperature, corresponding very well to the phase diagram predicting the present phase (Cu_3Sn) in the bond-line to be stable to temperatures above 676 ^{o}C. The average measures shear strength is 45 MPa from room temperature up to 300 ^{o}C, exceeding the MIL-STD by far. The average shear strength does not vary significantly across the different regions of the bonded wafers. However, at the regions with initially thinner Sn there is larger scatter in the measured shear strength. It is believed that small un-bonded regions within the test die where the Sn layer was at its thinnest cause this variation.

Interferometry of the fractured surfaces show brittle and well-defined planar surfaces, either between Ti/W adhesion layer to SiO_2, between Cu and Cu_3Sn, or at the original bonding interfaces. The two dominating fracture modes are in the adhesion layer and the original bond interface. This verifies that the material systems have potential for giving even higher bond strength than our measured strength.

This work provides experimental evidence for the stability of Cu-Sn SLID bonding at high temperature, a stability that has long been predicted from the phase diagrams. This strongly confirms the applicability of Cu-Sn SLID bonding for high temperature applications.

3.5 Article VI

Thi Thuy Luu, Nils Hoivik, Kaiying Wang, Knut E. Aasmundtveit and Astrid-Sofie Vardoy, *"Characterization of wafer-level Au-In bonded samples at elevated temperatures"*, Metallurgical and Materials Transactions AJune 2015, Volume 46, Issue 6, pp 2637-2645.

My contribution: design, assembly, characterization and test, part of shear test experiment, analysis, modeling, and manuscript preparation.

The motivation of this study is to demonstrate Au-In SLID bonding for high temperature applications. High temperature applications are defined by the applications that require operation at, or exposure to high temperatures above 125 ^{o}C. For these applications, the main requirements to the bonding material are that the bond-line has a high melting point and that the shear strength remains high at elevated temperatures. In order to achieve high shear strength at elevated temperatures, it is important to minimize the thermally induced stresses in the bond stack; this is typically done by reducing the bonding temperature, having a low CTE mismatch between the utilized materials, and by having a good thermal conductivity. One of the advantages that make Au-In bonding interested for high temperature applications is the low temperature process. The bonding could be assembled at 180 ^{o}C, which is lower than other SLID bonding. In this study, the mechanical integrity of Au-In SLID bonded samples at different temperatures was investigated.

Main results:

Au-In SLID wafer-level bonding with a proper design of the metal thicknesses for Au and In results in a very high bonding yield and a high resulting shear strength: in the 30 MPa range. The shear strength is stable when the temperature is increased from room temperature to 200 ^{o}C, and *increases* to ~40 MPa when the temperature is increased to 300 ^{o}C. This verifies experimentally that Au-In SLID bonding, performed at temperatures right above the melting temperature of In (156 ^{o}C) is indeed very suitable for high-temperature applications. Phase diagram predictions call for stability to 450 ^{o}C, and we demonstrated high strength up to our highest testing temperature of 300 ^{o}C.

The bond-line consists of the intermetallic phases AuIn and γ`, as found by cross-section microscopy and EDS. Interferometry of the fractured, sheared samples reveals that at temperatures up to 200 ^{o}C, the samples fracture at well-defined planar surfaces: either at the adhesion layer to intermetallic interfaces, or at the position of the original bond interface. At 300 ^{o}C, the nature of the fracture changes to a ductile fracture, explained by a phase transition to the ψ-phase and an annealing effect of the original bond

interface. The higher overall bond strength at 300 ^{o}C results from this improved strength of the initial bond interface.

The shear strength of devices has been investigated. With a proper design of the metal thicknesses for Au and In, a very high bonding yield was achieved. The final bond-line has both AuIn and γ` phases present as verified by cross section microscopy and EDS analysis. Furthermore, the die shear strength of the bonded samples was measured as function of temperature, from RT to 300 ^{o}C. The increasing trend of shear strength from RT to 300^{o}C confirms that Au-In bonding is a promising technique for high-temperature applications.

4 Voids characterization

4.1 Voids formation

Voids formation during bonding process is one of the important issues of Cu-Sn SLID bonding which can affect the bond performance. The voids formation during Cu-Sn bonding process has been reported by many research and industry groups [36, 45, 76, 78, 89, 115, 117, 135-151] and can be classified in three voids scenarios as shown in Figure 4.1: a) bond interface voids, which distribute at the original bond interface, b) Cu/Cu_3Sn voids, also call sporadic voids and distribute as a continuous layer at Cu/Cu_3Sn interface and c) Kirkendall voids which distribute across the Cu_3Sn layer. In this section, different mechanisms of void formation will be presented and discussed.

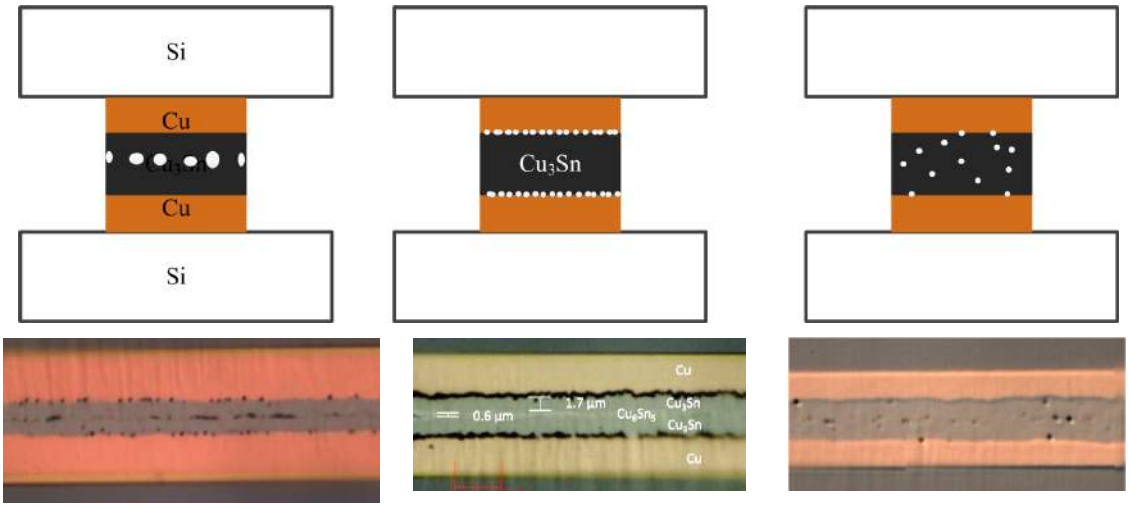


Figure 4. 1: Three different types of voids that can form during Cu-Sn SLID bonding process a) bond interface voids, b) Cu/Cu_3Sn voids and c) Kirkendall voids.

4.1.1 Bond interface voids

4.1.1.1 Bond interface voids formation mechanism

There are several mechanisms behind the formation of bond interface voids: lack of wetting at the bond interface, growth of Cu_6Sn_5 scallops, non-uniformity of electroplating process and non-uniform initial Cu-Sn thickness [143, 152-155].

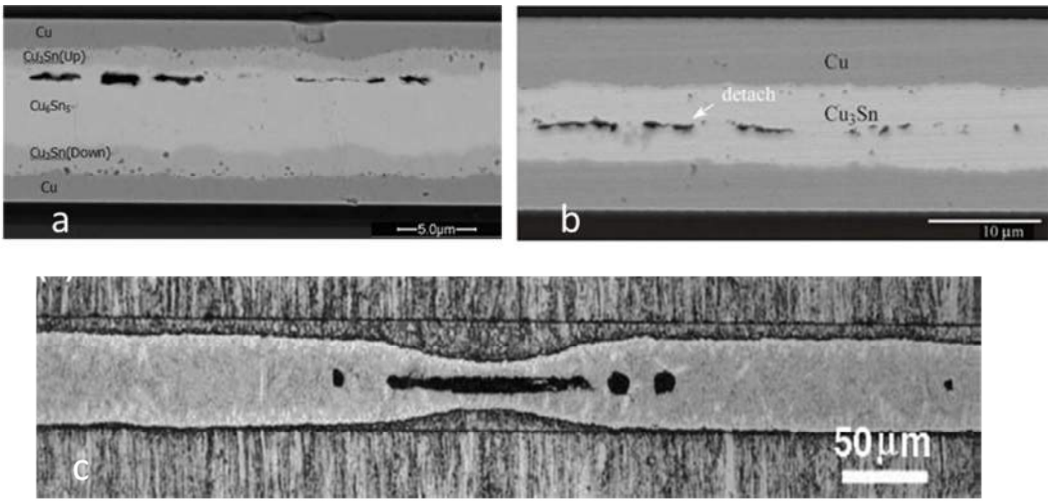


Figure 4. 2: Cross-section of Cu-Sn SLID bonded samples. Interface voids are formed due to a) lack of wetting at original bond interface [152], b) non-uniformity of electroplating process [155] and c) the growth of Cu_6Sn_5 scallops during bond process [153].

Lack of wetting at the original bond interface

Lack of wetting at the bond interface is caused by contaminations, Sn and Cu oxidation when Cu to Cu-Sn bonding is used [116, 152]. The oxidation issue can be solved by using a Cu_3Sn layer as protection layer to prevent Cu from oxidation or symmetric Cu/Sn bonding [87, 156]. In this study, symmetric Cu-Sn bonding is used. Therefore, lack of wetting at the original bond interface is not an issue for voiding.

Non-uniformity of electroplating process

For Cu-Sn SLID wafer-level bonding, the Cu-Sn layers are prepared by electroplating process. According to our experience, there is always a degree of non-uniformity during electroplating process. This causes a 2-10 % variation of Cu and Sn thickness. At the regions of the wafers where Cu layer is thinnest, Sn may not contact together during bonding process and cause un-bonded area [118, 155].

Growth of Cu_6Sn_5 scallops

During Cu-Sn SLID bonding process, the temperature is increased following a defined temperature. During the ramping process, the Cu_6Sn_5 scallops grow and Sn is converted into solid IMCs. Defined T_m is the melting point of Sn. Defined critical Sn thickness ($y_{critical}$) is the minimum thickness to ensure that there is pure Sn at the original bond interface when T_m reached. If the initial Sn thickness is thinner than $y_{critical}$, Cu_6Sn_5 scallops will reached the Sn surface before T_m is reached, and acts as spacers and cause interface voids. This is further described in article 1 and 2.

4.1.1.2 Prevent interface voids

Pretreatment of wafers prior bonding

As described, one of the reasons of interface voids is the growth of Cu_6Sn_5 scallops which occurs even at room temperature. In order to prevent interface voids, one of the solutions is to prevent the growth of Cu_6Sn_5 scallops.

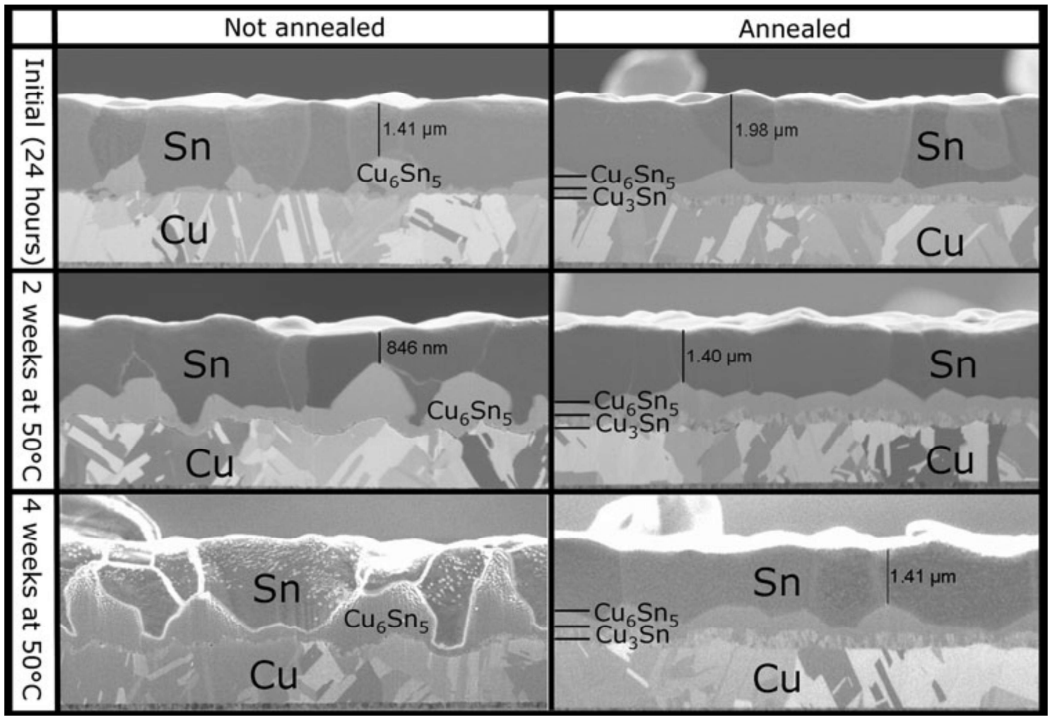


Figure 4. 3: IMC development during annealing process at 50 °C of as-plated Cu-Sn sample and shorted pre-annealed Cu-Sn sample, showing that short annealing at 200 °C in 1 minute can flatten IMC layer [157].

Annealing of electroplated Cu/Sn sample at temperatures 125-200 ^{o}C can produces a thin and uniform Cu_6Sn_5 layer; this leads to subsequent growth of a planar IMCs instead of scallops [148, 157]. Therefore, pre-annealing electroplated Cu-Sn sample is one of solutions to slow-down the formation of Cu_6Sn_5 scallops, and prevents interface voids formation.

Optimize initial Cu-Sn thickness and bonding process

Optimize bond temperature profile is one solution to prevent interface voids formation. There are two issues should be taken into account:

- A two-steps bonding profile should be used [158]. In a two-steps bond temperature profile, the wafers are brought into contact at a temperature of 150-200 ^{o}C and kept at this temperature for several minutes. This temperature soak is served as pre-treatment of the wafers and prevent the growth of Cu_6Sn_5 scallops.
- There must be pure Sn available at the surface when the melting point of Sn is reached, in order to perform a good wetting at the interface and compensate the non-uniformity of electroplated Cu thickness over the wafer.

Bond temperature can be optimized by using the simulation model described in this thesis of IMCs development during the Cu-Sn bonding process. More information about this approach is presented in chapter 2 and article 1, 2.

4.1.2 Cu/Cu_3Sn voids

4.1.2.1 Cu/Cu_3Sn voids formation

Cu/Cu_3Sn voids are usually observed in Cu-Sn soldering and have been frequently reported in earlier studies [78, 135, 136, 138]. Different mechanisms of these voids formation correlates to impurities and stress-strain have been proposed [136, 139, 146, 149, 150, 159]:

- Vacancy injection mechanism: during the Cu-Sn bonding or annealing process, the reactive of Cu and Sn occurs at Cu/Cu_3Sn and Sn/Cu_6Sn_5 interfaces and leaves vacancies at these interfaces. Theoretically, the vacancies would be injected by Cu and Sn diffused atomics. The impurities can block the vacancies injection process and voids later form [135, 139, 160, 161].

- Strain mechanism: Cu, Sn, Cu_6Sn_5 and Cu_3Sn have different elasticity and crystalline structure. During Cu-Sn annealing process, the difference of elasticity causes the strain at Cu/Cu_3Sn interface. The strain distributes at Cu grain boundary and induces voids formation [149].

The effects of Cu grain structure, organic impurities and Cu oxidation on this type of voids formation are experimentally confirmed [78, 135, 139, 146, 150, 159, 162, 163]. These studies demonstrated that: small Cu grain size, organic impurities and single crystalline Cu texture can cause higher voids level at Cu/Cu_3Sn interface. The possible reasons are:

- For small Cu grain size, more Cu diffuses into IMCs through grain boundary and more vacancies are formed at Cu/Cu_3Sn interface.
- In a polycrystalline texture, the Cu has random orientations; therefore Cu diffuses into Sn trough many different orientations and reduces voids level.
- During the Cu-Sn bonding process, the reaction between Cu and Sn mostly occurs at Cu/Cu_3Sn and Cu_3Sn/Cu_6Sn_5 interface and results vacancies at these interfaces. Impurities from electroplating process and cleaning chemical [161, 164] or Cu oxidation can block the vacancies injection at Cu/Cu_3Sn interface and voids later form.

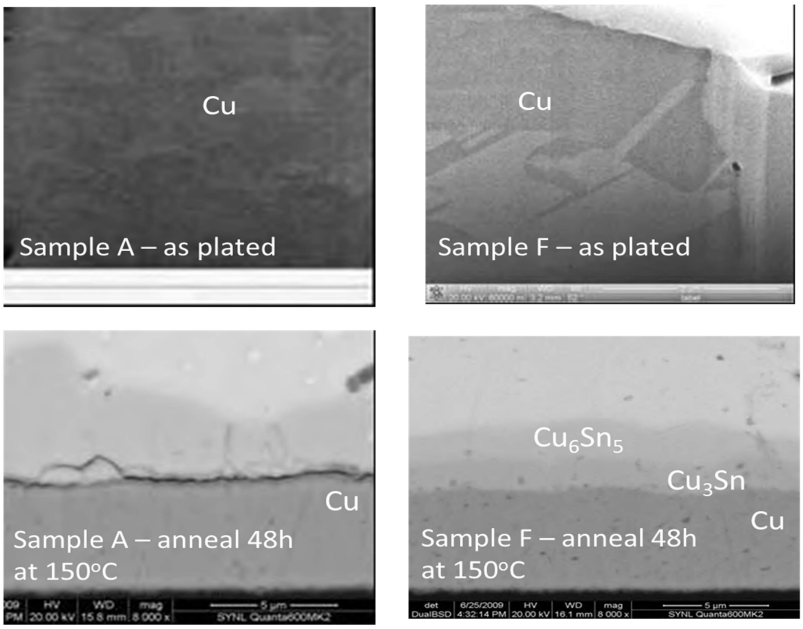


Figure 4. 4: Cu/Cu_3Sn voids formation due to small Cu grain size. For sample A, the grain size is small, voids form at Cu/Cu_3Sn interface after annealing [162].

Even Cu/Cu_3Sn voids do not cause any degradation of the Cu-Sn solder joint reliability [138, 165], these voids can reduce the contact area of solder joint and therefore increase the resistant of solder interconnects. In addition, this type of voids also reduces significantly the shear strength of solder ball [162]. Figure 4.4 shows two different as-plated Cu samples with different grain sizes [162]. The shear test on these two samples shows that: sample "A" has much lower shear strength compared to sample "F"; and the fracture for sample "A" occurs at Cu/Cu_3Sn voids interface.

4.1.2.2 Prevent Cu/Cu_3Sn voids

To prevent the voids formation at Cu/Cu_3Sn interface, the most effective solution is to control electroplating parameters, such as current density, additive and the bath ages [139, 162]. By controlling these parameters, Cu grain size and texture and the impurities level can be controlled [139, 162]. To achieve large Cu grain size and polycrystalline texture, a current density above 10 mA/cm^2 and combination of different additives should be used [139]. To reduce the impurities level, the electroplating bath age must be well controlled.

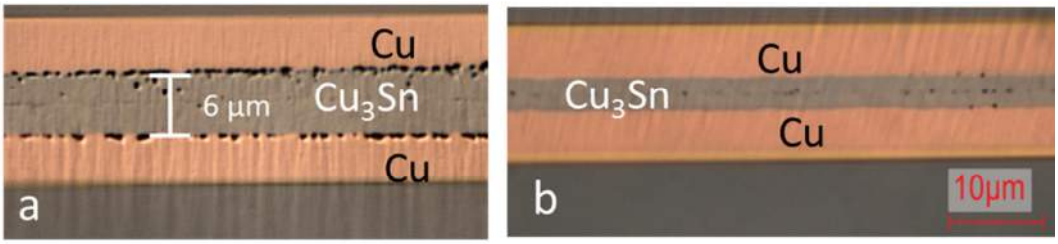


Figure 4. 5: Cross-section of two different bonded samples. A Cu electroplating current density of 10 mA/cm^2 was used. For sample a) an old electroplating bath was used, Sn was not electroplated immediately after Cu. For sample b) a new electroplating bath with fresh prepared electroplating solution was used, Sn was electroplated immediately after Cu.

In our work, we used a current density of 10 mA/cm^2 and commercial additive DMK - Glanzzusatz Maron. In addition, Sn was electroplated immediately after Cu to avoid Cu oxidation. For the bonded sample given in Figure 4.5a, an old electroplating bath was used and Sn was not electroplated immediately after Cu. For the bonded sample given in Figure 4.5b, new electroplating bath (fresh prepared electroplating solution bath) was used and Sn was electroplated immediately after Cu. There are two possible reasons that may cause voids at sample in Figure 4.5: old electroplating bath may produce more impurities in Cu; and Cu surface is oxidized before Sn electroplating.

Another option to reduce voids formation is to anneal Cu at high temperature before electroplating of Sn. Annealing Cu at 650^{o}C or 350^{o}C for 2h can increase Cu grain size and gasify certain impurities inside Cu [139, 146, 159]. This produces high purity, large Cu grain structure and subsequently reduces voids level Cu/Cu_3Sn interface. In our case, we do not use this solution due to several reasons:

- In our electroplating, we used a current density 10 mA/cm^2 and commercial Cu electroplated additive. This can produce Cu with high purity large grain size.
- Annealing Cu before Sn electroplating introduces one more fabrication step.
- For MEMS packaging and encapsulation, the devices can be damaged due to high temperature annealing.

4.1.3 Kirkendall voids

The Kirkendall voids are formed due to the difference between the intrinsic diffusivities of Cu and Sn in Cu_3Sn, which is typical for any multiphase diffusion systems [166]. In the Cu-Sn diffusion system, the diffusion rate of Cu into Cu_3Sn is much faster than the diffusion rate of Sn [167]. This imbalanced interdiffusion leaves atomic-level vacancies at Cu_3Sn side. Voiding is formed from the accumulation of excess vacancies.

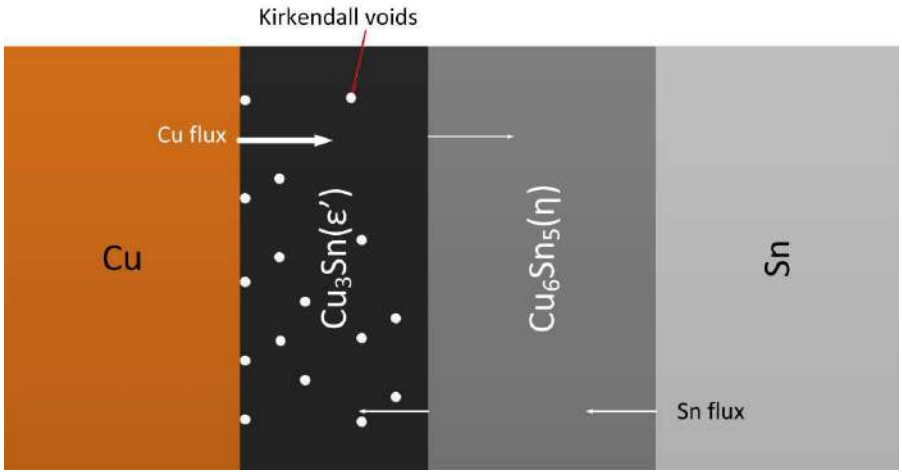


Figure 4. 6: An illustration of Kirkendall voids formation due to the difference between the intrinsic diffusivities of Cu and Sn in Cu3Sn.

An illustration of Kirkendall voids formation mechanism is shown in Figure 4.6. Similar to Cu/Cu_3Sn voids, the Kirkendall voids are correlated to the impurities level in Cu and Cu grain size. Small Cu grain size and high impurities introduce much higher voids level.

4.2 Voids characterization

Figure 4.7 shows the cross sections of two different Cu-Sn bonded samples. With samples shown in Figure 4.7 b, two types of voids are presented: Kirkendall voids and interface voids. For these two actual samples, we clearly observe that voids area increases with the increasing of Cu_3Sn thickness. In this study, the correlation between voids and Cu_3Sn thickness is investigated. To eliminate the effect of the length of sample and Cu thickness, the void area was described as voids fraction (area per unit length).

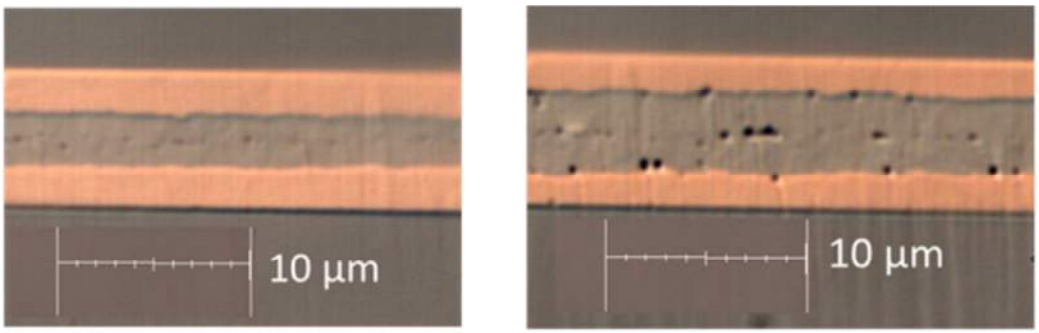


Figure 4. 7: Cross section of the bonded samples which is prepared by process A. The samples were electroplated and bonded by Sensonor As. The thickness of Cu_3Sn layer is not uniform.

To estimate void fraction and Cu_3Sn thickness, image processing software "ImageJ" was used for samples analysis. The analysis process is described in Figure 4.8. The original cross-section of the bonded sample is shown in Figure 4.8a. The original image was split into three different colors: red, green and blue. The blue one is used for voids area estimation, the red one is used for IMCs thickness estimation. By adjusting color threshold of the blue, voids are presented, as shown in Figure 4.8b. These voids are considered as particles. The software can count the number of particles and measure the area of each particle and total area. The voids fraction (voids area per unit length) is estimated by:

$$f_{void} = \frac{A_{void}}{L} \qquad \textbf{Eq 4. 1}$$

Here, f_{void} is voids area fraction per unit length, A_{void} is total voids area and L is the length of sample.

By adjusting color threshold of the red, the Cu layers and Cu_3Sn layer are presented as shown in Figure 4.8c. The area of Cu_3Sn layer can be measured by software. Cu_3Sn thickness is estimated by:

$$y_{IMC} = \frac{A_{IMC}}{L} \qquad \textbf{Eq 4. 2}$$

Here y_{IMC} is average Cu_3Sn thickness, A_{IMC} is Cu_3Sn area and L is length.

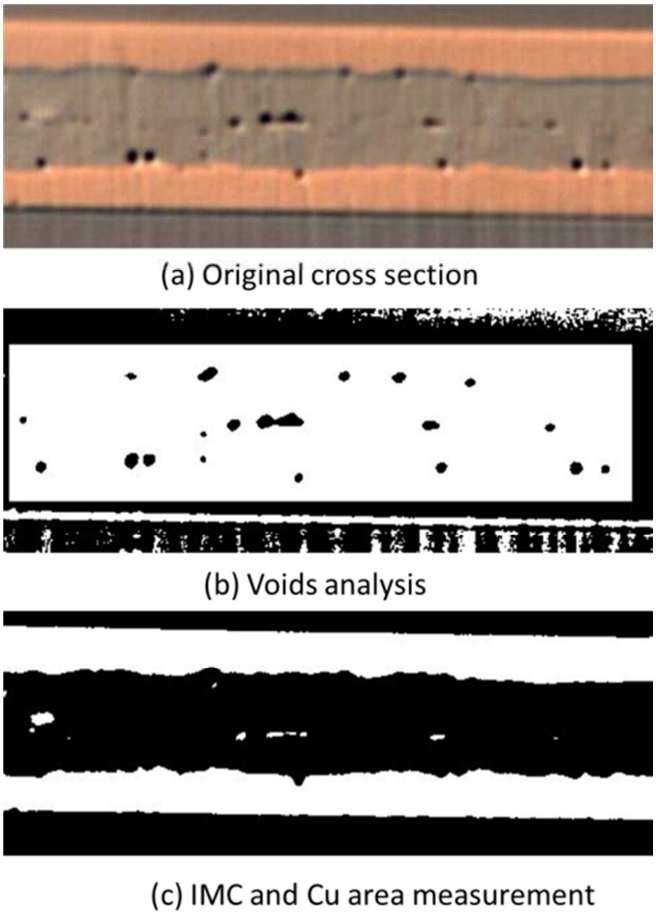


Figure 4. 8: Voids analysis using image processing software: a) original cross-section of the bonded samples, the original picture was split into three different colors – green, blue and red; b) cross-section picture after adjusting the color threshold of the blue, voids present as particles, software can count and measure the volume of these particles; c) cross-section picture after adjusting the color threshold of the red; Cu_3Sn layer present as center dark layer, software can measure the area of this layer.

4.3 Analysis of voids formed in wafer-level bonded samples

4.3.1 Voids analysis results

Figure 4.9 describes the voids area fraction of different Cu-Sn SLID wafer-level bonded samples as function of Cu_3Sn thickness. Two different wafer-level bonded samples were prepared: A) samples prepared by industry partner Sensonor AS, B) samples prepared by our work. Voids area fraction increases with the increasing of Cu_3Sn thickness.

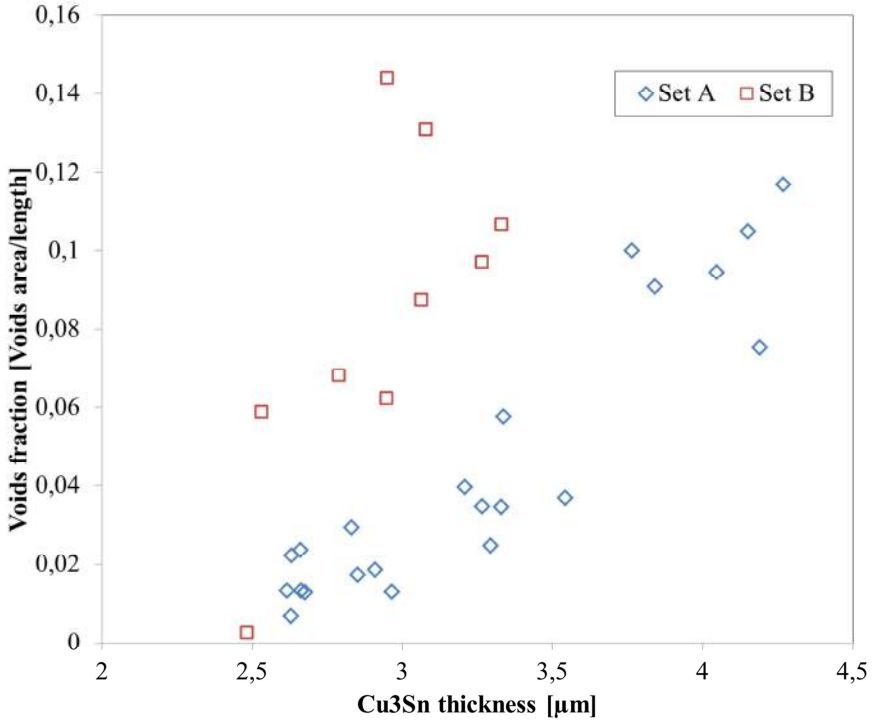


Figure 4. 9: Voids area fraction of Cu-Sn SLID wafer-level bonded samples as functions of Cu_3Sn thickness. A: bonded samples prepared by industry partner Sensonor AS. B: bonded samples prepared by our work.

4.3.2 Voids development during further annealing of bonded samples

To investigate the effect of voids to the bond performance, further annealing of bonded samples were carried out. Figure 4.10 shows the cross-sections of as-bonded sample and further annealed sample. For this sample, we obtain a low voids area fraction of 0.01. The voids area does not change during the annealing process; but Cu grain size has changed after annealing. This experimentally confirms that: there is not further diffusion

of Cu into Cu_3Sn; final $Cu/Cu_3Sn/Cu$ bond-line has high temperature stability up to 370 ^oC and annealing Cu at 370 ^oC.

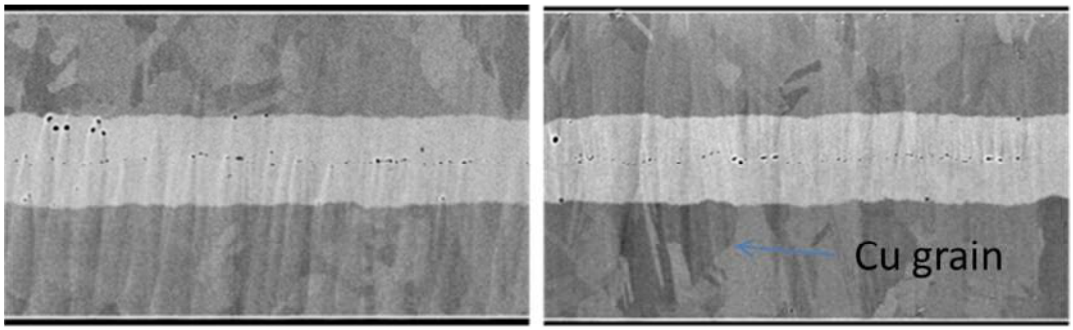


Figure 4. 10: Further annealing of Cu-Sn bonded samples. Samples were prepared by process A. SEM cross-section is taken by Sensonor As.

4.3.3 Discussion

In our bonding experiment, the electroplating process was controlled and we can prevent the formation of sporadic voids at Cu/Cu3Sn layer. Only bond interface and Kirkendall voids were observed. The area fractions of these types of voids as functions of Cu_3Sn thickness are shown in Figure 4.11. Bond interface voids area fraction seems not to be depended on Cu_3Sn thickness and does not have significant change with Cu_3Sn thickness. The Kirkendall voids area fraction increases monotonically with Cu_3Sn thickness.

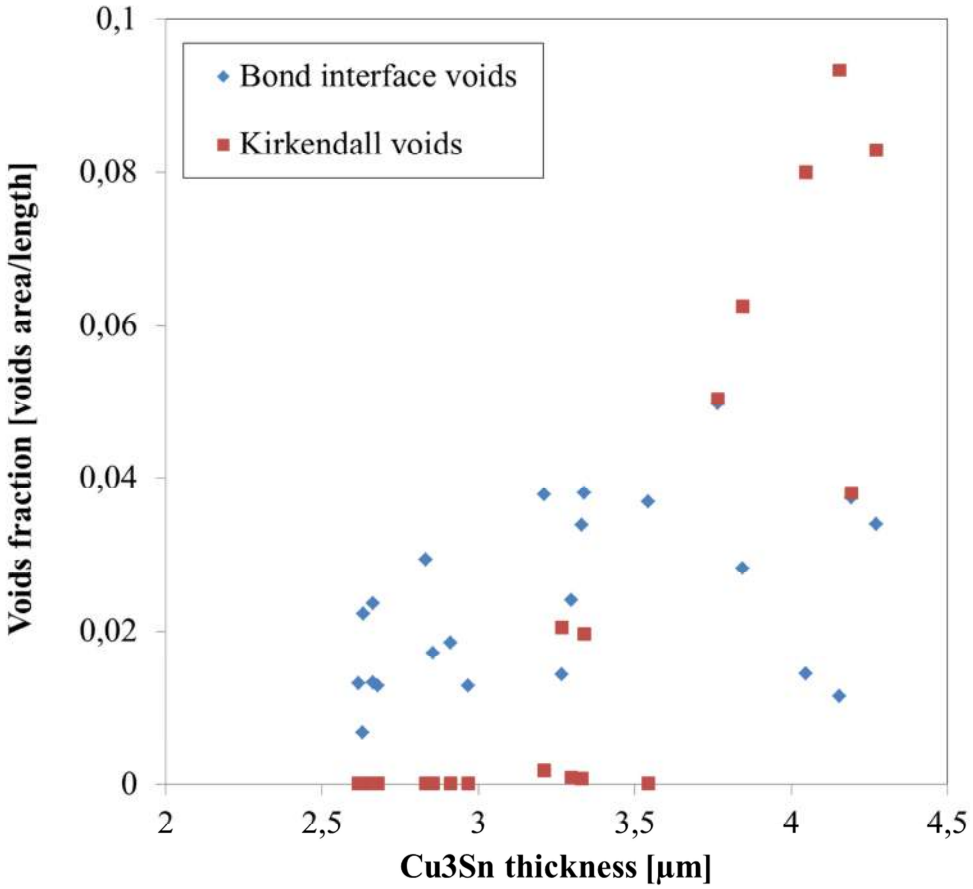


Figure 4. 11: Bond interface and Kirkendall voids area fractions as functions of Cu_3Sn thickness, bonded samples set A.

According to earlier work [78, 146, 168], with a constant annealing temperature, the Kirkendall voids area fraction and Cu_3Sn thickness have parabolic correlation with annealing time. Therefore, Kirkendall voids area fraction should have a linearly correlation with Cu_3Sn thickness. A linear fitting of voids area fraction and Cu_3Sn thickness correlation is shown in Figure 4.12. For samples set A and set C, the voids area fractions and Cu_3Sn thickness have linear correlation. This linear trend is caused by Kirkendall voids. For sample set B, the initial Sn thickness is thinner than set A and cannot compensate the non-uniformity of electroplating process. This introduces voids that come from un-bonded area and the voids area fraction does not have linear correlation with Cu_3Sn thickness.

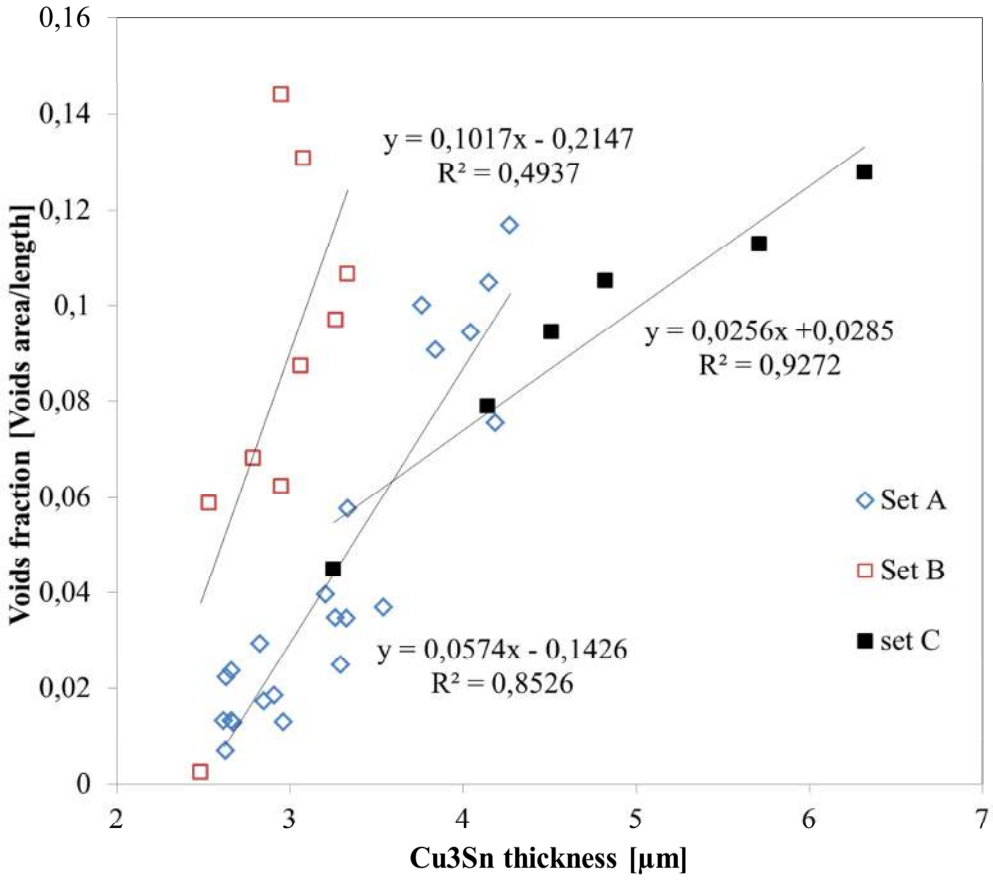


Figure 4. 12: Voids fraction as function of Cu_3Sn thickness A. Bonded sample from industry partner (Sensonor As). B. Bonded sample from our work. C. from literature (G. Lim [168]).

Another mechanism that could be driving factor of voids formation is the volume change of metallization during bonding process. The reaction between Cu and Sn induces a volumetric change due to the differences in mass densities of Cu, Sn and IMCs. The volume change can cause a voids area fraction ~0.1*t_{Cu3Sn} [$\mu m^2/\mu m$]. During the bonding process, the bond pressure is applied. This may reduce the effect of volumetric change. Therefore, in our bonding, the voids area fraction/Cu_3Sn thickness ratio is ~0.05 (set A), much smaller than 0.1.

4.4 Conclusion

In this session, the voids formation during Cu-Sn SLID wafer-level bonding process was presented. Even there are different voids scenarios: interface voids, Cu/Cu_3Sn voids and Kirkendall voids, the voids level have strong correlation with Cu grain structure and

impurities. By controlling Cu electroplating process, we can eliminate Cu/Cu_3Sn voids and obtain Cu-Sn SLID wafer-level bonded samples with low voids area fraction.

For this work, voids are formed due to Kirkendall effect and the growth of Cu_6Sn_5 scallops. The linear correlation between Kirkendall voids area fraction and Cu_3Sn thickness was experimentally verified. With a final $Cu/Cu_3Sn/Cu$ bond-line, the voids area does not change during further annealing of bonded samples. This confirmed that low voids area fraction does not cause degradation of the bond performance.

5 Summary and outlook

5.1 Summary

This thesis presented solid liquid interdiffusion (SLID) wafer-level bonding for MEMS packaging. Two techniques, Cu-Sn SLID bonding and Au-In SLID bonding, have been investigated.

5.1.1 IMCs develoment during Cu-Sn SLID bonding process

The formation of IMCs which takes place during the Cu-Sn SLID wafer-level bonding process was successfully characterized. Thermal kinetics models of the Cu_3Sn thickness and the amount of Sn that is converted into IMCs were estimated. We experimentally verified that the growth of IMCs during Cu/Sn annealing process follows Arrhenius equation $y^2 = k_0 e^{\frac{-Q}{RT}} t^{2n}$. One of the major findings of our study is that the empirical coefficient *n* depends on temperature. Above the melting point of Sn, *n* is equal to 1/2, as expected from the analytical solution of the diffusion equation, corresponding to a diffusion-controlled process. For temperatures below the melting point of Sn, a value of *n* below 1/2 is obtained, indicating that slower chemical reaction limits the IMC growth rate. Based on this knowledge of IMC formation during the annealing process, a MATLAB model was created to simulate the IMCs development during the bonding process. Using this simulation model, we can predict the parameters that are important for bonding temperature profile optimization: unreacted remaining Sn thickness on each wafer at the contact temperature and bonding temperature, and required bonding times to achieve $Cu/Cu_3Sn/Cu_6Sn_5/Cu_3Sn/Cu$ and $Cu/Cu_3Sn/Cu$ final bond-lines. Experiments show that the simulation model accurately predicts the IMCs formation during the bonding process. The experimental and simulation results show that an effective solution to reduce the bonding time is to leave the final bond-line as

$Cu/Cu_3Sn/Cu_6Sn_5/Cu_3Sn/Cu$, with further annealing performed outside the wafer bonder to convert all the Cu_6Sn_5 into Cu_3Sn.

5.1.2 Effect of bond pressure and temperature profile to Cu-Sn SLID bond performance

We have demonstrated Cu-Sn SLID wafer-level bonding for fabricating micro-joints with high mechanical strength. The effect of bond temperature profile, bond pressure and Cu/Sn frame width to the bond performance was investigated. The main findings of this work are:

- To achieve high bond strength, a high bond pressure above 1.5 MPa should be used. For this work, with bond pressure 1.5 MPa, we can obtain a bond-strength of 74 MPa, a dicing yield 100 % and a sealing yield of 80 %.
- A two-steps temperature profile can reduce effectively Sn squeeze out.
- In this work, the minimum frame-width we can obtain is 80 µm.

5.1.3 High-temperature mechanical integrity of Cu-Sn SLID bonds

Cu–Sn SLID wafer-level bonding results in a high bonding yield and a high mechanical integrity; also well above the melting point of Sn. The average measured shear strength is 42 MPa, exceeding the MIL-STD by far. For shear tests performed at temperatures from room temperature up to 300 ^oC, no significant change in shear test is observed, thus verifying the high-temperature stability predicted for Cu–Sn SLID bonding.

These high shear-strengths are obtained although there was non-uniformity in the electroplating process that resulted in larger scattering of the shear strength at several regions of the bonded wafer pair. The non-uniformity also caused voids and un-bonded areas at the original bond interfaces, and led to this being one of two dominating fracture surfaces. The other dominating fracture surface was adhesive fracture at Ti-W adhesion layer to SiO_2. The fracture at these interfaces provides evidence that the mechanical integrity of Cu–Sn SLID bonded samples is stable up to 300 ^oC and stronger than the adhesion layer. Further improvement of the bond strength may be obtained by improving the adhesion layers and the uniformity of the electroplated layer thicknesses.

5.1.4 Void formation during Cu-Sn SLID wafer-level bonding

In this session, the voids formation during Cu-Sn SLID wafer-level bonding process was presented. Even there are different voids scenarios: bond interface voids, Cu/Cu3Sn voids and Kirkendall voids, the voids level has strong correlation with Cu grain structure and impurities. By controlling Cu electroplating process, we can prevent Cu/Cu3Sn voids and obtain Cu-Sn SLID wafer-level bonded samples with low voids area fraction.

For this work, voids are formed due to Kirkendall effect and the growth of Cu_6Sn_5 scallops. The linear correlation between Kirkendall voids area fraction and Cu_3Sn thickness was experimentally verified. With a final $Cu/Cu_3Sn/Cu$ bond-line, the voids area does not change during further annealing of bonded samples. This confirmed that low voids area fraction does not cause degradation of the bond performance.

5.1.5 Au-In SLID wafer-level bonding

Au-In SLID wafer-level bonding at 180 ^oC, with a proper design of the metal thicknesses for Au and In, results in a very high bonding yield and a high resulting shear strength: in the 30 MPa range. The shear strength is constant when the shear test temperature is increased from room temperature to 200 ^oC, and *increases* to ~40 MPa when the shear test temperature is increased to 300 ^oC. This verifies experimentally that Au-In SLID bonding performed at temperatures right above the melting temperature of In 156 ^oC is indeed very suitable for high-temperature applications. Phase diagram predictions call for stability to 450 ^oC, and this work demonstrated high strength up to our highest testing temperature of 300 ^oC.

The bond-line consists of the intermetallic phases AuIn and $\gamma`(Au_7In_3)$, as found by cross-section microscopy and EDS. Interferometry of the fractured, sheared samples reveals that at temperatures up to 200 ^oC, the samples fracture at well-defined planar surfaces: either at the adhesion layer to intermetallic interfaces, or at the position of the original bond interface. At 300 ^oC, the nature of the fracture changes to a ductile

fracture, explained by a phase transition to the ψ-phase (Au_6In_4) and an annealing effect as the IMC-to-IMC phase boundary sweeps across the original bond interface. The higher overall bond strength at 300 ^oC results from this improved strength of the initial bond interface.

5.2 Outlook

In summary, this PhD work has demonstrated Cu-Sn and Au-In SLID wafer-level bonding with high yield and performance. The research carried out in this PhD raise several topics for future studies:

- Even we have developed the model for IMCs development during Cu-Sn bonding process and obtained high bond performance, there is still room for improving the performance. Further improvement of bonding process in term of uniformity of electroplating process and adhesion layer.
- The Cu-Sn and Au-In SLID wafer-level bonding has proved high-temperature mechanical integrity. The next step is to carry out the reliability tests, such as high-temperature aging and thermal cycling to further verity the mechanical performance of the bonds at high-temperature.
- In this work, the Cu-Sn and Au-In SLID bonding were used to bond Si to Si wafers. Using the techniques to bond other substrate materials, such as glass, SiC should be carried out. Bonding with different materials would open room for more application.
- Initial work on Au-In SLID wafer-level bonding was demonstrated in this work. The bond design principles were described. One of the interesting topics is to optimize bonding process. Different Au/In thickness ratio could be used in order to find out which will give optimal mechanical integrity.
- A study of hermeticity should be carried out

5.3 Contributions of PhD candidate

During the PhD work, the PhD candidate has been working with two different bonding techniques: Cu-Sn and Au-In SLID wafer-level bonding for MEMS packaging and encapsulation. The main contributions of this work are:

- SLID bonding is well-known process, but a simulation model for the IMCs development during bonding process is not available. This work built up such a model. This modelling provides a fully understanding about the development of IMCs during the SLID bonding process and could be used as a tool for process design and optimization.
- Mechanical integrity at temperature surpassing the melting temperature of the low-melting metal component of SLID bonding has long been predicted, but experimental verification is scarce. In this study, the mechanical integrity of Cu–Sn and Au-In SLID bonding was experimentally confirmed at high temperature. This provides an evidence of these bonding techniques suitable for packaging of the devices that need to operate or expose to high temperatures.
- Through this work, a new method of fracture characterization was proposed. By using interferometry, we can define accurately where the fracture occurs in the bond interface. Compared to traditional fracture characterization (using optical microscopy, SEM and EDS), this method provide a fast and effective characterization.
- An overview of voids formation during Cu-Sn SLID bonding was presented. Voids formation during Cu-Sn annealing process and soldering has been investigated by previous work, but the mechanism of voids formation is not fully understood. In this work provides an overview of different voids formation mechanisms in a SLID bonding process. The work also provides the evidence that micro voids may not affect the performance and reliability of the bonding.

In addition of the contribution to the scientific, the work has been done in this thesis also facilitates further research activities in SLID bonding at Buskerud and Vestfold University College and also the cooperation with other research partner, such as Herriot Watt University, SINTEF ICT and Sensonor AS.

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Papers not available in this file due to publisher's restrictions:

I:

Thi-Thuy Luu, Ani Duan, Kaiying Wang, Knut E. Aasmundtveit and Nils Hoivik, *"Optimization of Cu/Sn wafer-level bonding based upon intermetallic characterization",* 4th Electronic System-Integration Technology Conference (ESTC 2012), September 17-20, 2012, Amsterdam, Netherland.

II:

Thi-Thuy Luu, Ani Duan, Knut E. Aasmundtveit and Nils Hoivik, *"Optimized Cu/Sn wafer-level bonding using intermetallic phase characterization",* Journal of Electronic Materials 2013, Vol 42(12), 2013, pp. 3582-3592

III:

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IV:

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V:

Thi Thuy Luu, Nils Hoivik, Kaiying Wang, Knut E. Aasmundtveit and Astrid-Sofie B. Vardøy, *"Cu/Sn SLID wafer-level bonding for high temperature application"*, manuscript accepted to be published on Metallurgical and Materials Transactions A

VI:

Thi Thuy Luu, Nils Hoivik, Kaiying Wang, Knut E. Aasmundtveit and Astrid-Sofie Vardoy, *"Characterization of wafer-level Au-In bonded samples at elevated temperatures"*, Metallurgical and Materials Transactions AJune 2015, Volume 46, Issue 6, pp 2637-2645

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