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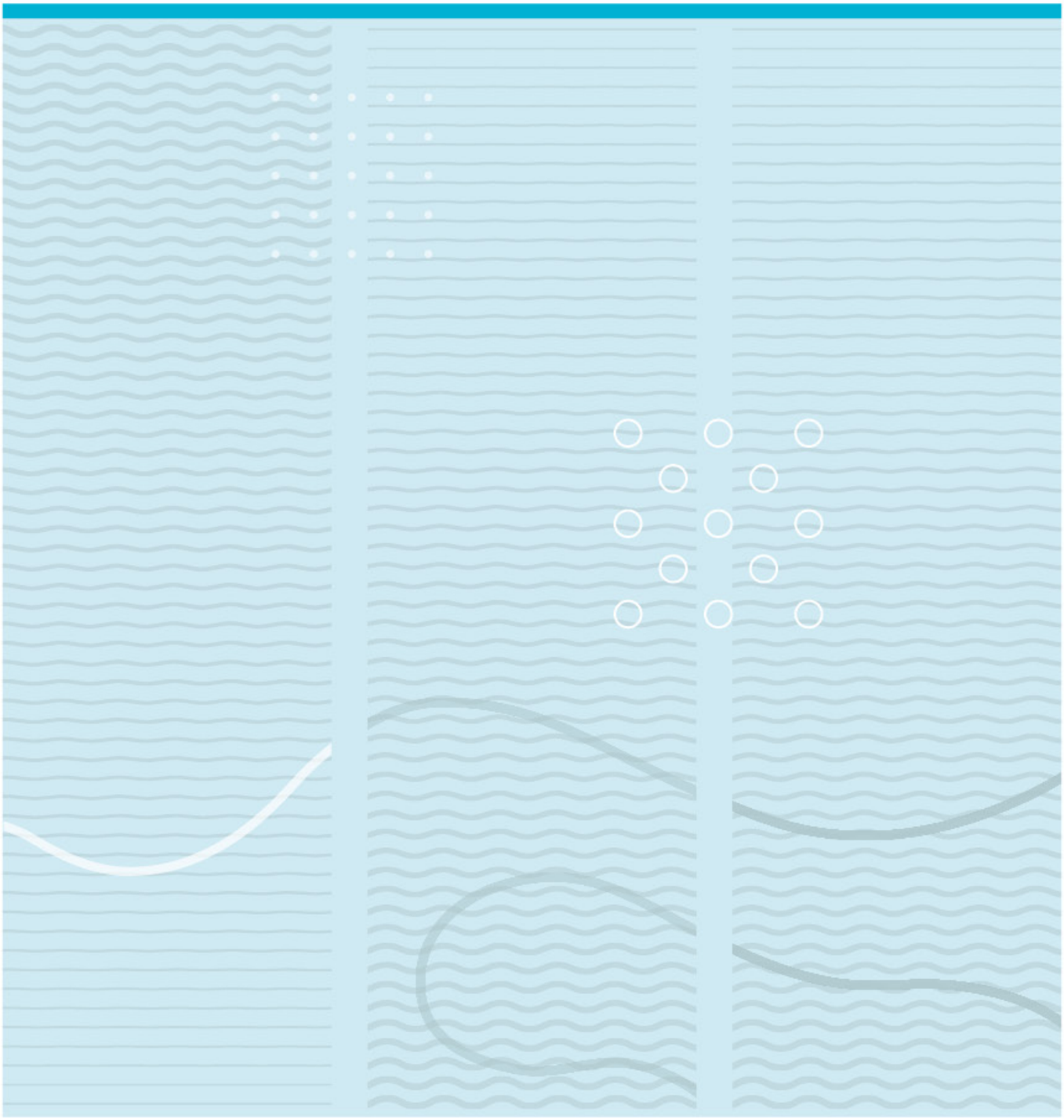
Design and Fabrication of on-chip heating for Electric Substitution Radiometer

Design and Integrate Heating Resistors on backside of the Photodiode



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i. Abstract

This thesis describes the design, simulations, and fabrication of heating resistors by the photolithography process, and finally integration of a selected resistor through a bonding procedure to the backside of a photodiode. TiW (90/10%) is used for resistor lines and Au is used for resistor pads. The fabricated resistors are integrated into an electric substitution radiometer (ESR) equipped with a predictable quantum efficient detector (PQED) to assemble a dual-mode detector module (DMD).

This research project is part of the European research project chipS·CALe [1], which is in close collaboration with Justervesenet, Norway's metrology institute. The goal of this research is to develop high-precision optical power measurement techniques using silicon photodiodes.

After describing the process of the integration of the heating resistor onto the backside of the photodiode, the assembly of the dual-mode detector module will be explained. This is where a mix of wire bonding techniques and silver conductive epoxy were used to make a connection between the bottom printed circuit board (PCB) and the top PCB (attached to photodiode with resistor).

ii. Acknowledgement

Foremost, I would like to thank my supervisor Eivind Bardalen for his supervision during my research and writing of the thesis.

Furthermore, my thanks go to Jarle Gran, Marit Ulset Nordsveen at Justervesenet and Per Øhlckers at the University of South-Eastern Norway for the weekly meetings with enlightening presentations, discussions, and the opportunity of doing this project with them. I have learned a lot, I also enjoyed working with them.
I would also like to thank Zekija Ramic for her guidance in the cleanroom.

To conclude, I would like to send my thanks to my parents and my friends: Hoi Yi Siu and Olivia FitzGerald, and all the rest who are not mentioned in here. Without your support it would not be possible to reach this point, and I wish you all the best in your endeavours.

<Borre, August 13st 2021>
<Hamed Jalalian Javadpour>

iii. List of Abbreviations

Au = Gold

CR = Cryogenic radiometer

DI Water = Deionized water

DMD = Dual mode detector

DRIE = Deep reactive ion etching

ESR = Electrical substitution radiometer

FEM = Finite element method

IC = integrated circuits

InGaAs = Indium gallium arsenide

LED = Light-emitting diode

MEMS = Micro electromechanical systems

PCB = Printed circuit board

PQED = Predictable quantum efficient detector

SiO_2 = Silicon dioxide

UV Light = Ultraviolet light

TCR = Thermal coefficient of resistance

TiW = Titanium tungsten

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1 Introduction

1.1 Motivation

Optical radiation surrounds the world where light sources play an important role in life on this planet. Using features of natural sources of light, including the sun, stars, and moon, as well as artificial light sources such as lamps and LED, allows us to improve our quality of life. Measuring light power, and its effects on material properties which can be applied to different applications in health and science, relies heavily on the precision of light spectrum measurement [2]. In response to current measurement accuracy requirements, there is a need to find cost-efficient and precise solutions to measuring optical power. The use of photodiodes as an electric substitution radiometer is one method. The power is determined in the ESR mode using a temperature sensor to measure the temperature increase, ΔT.

In order to determine the relationship between optical power and heat absorption by the photodiode, a known amount of electric power ($I \cdot V$) is supplied to the photodiode and its corresponding absorption level is recorded. **Figure 1.** depicts the mentioned steps [3].

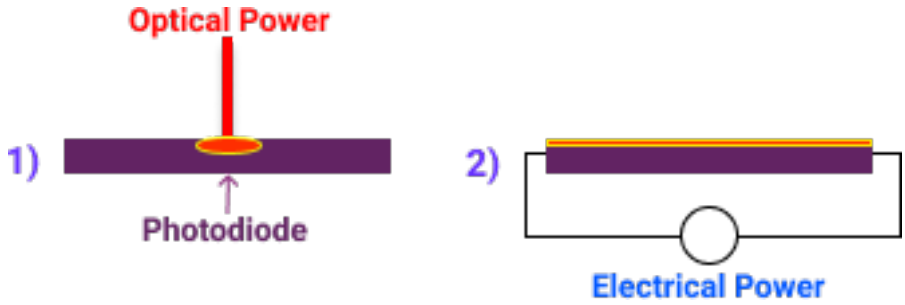


Figure 1. Illustrates optical heating mode (1), using laser beam, vs electrical heating mode (2). Where in electrical heating mode, the photodiode is heated electrically by applying a forward bias.

By comparing the corresponding temperature increase in each step, a precise determination of the optical power may subsequently be determined. Also, photodetectors can be calibrated using this technique.

In a previous study [4], applying a forward bias has been used to electrically heat the photodiode. However, as **Figure 1** depicts, power is dissipated differently by electrical

than with optical heating, and this method limits theoretical performance and causes for the edges of the photodiode to become heated.

One way of improvement could be expected through the design and integration of a heating resistor on the backside of the photodiode to heat the photodiode [3]. **Figure 2** visualizes the concept.

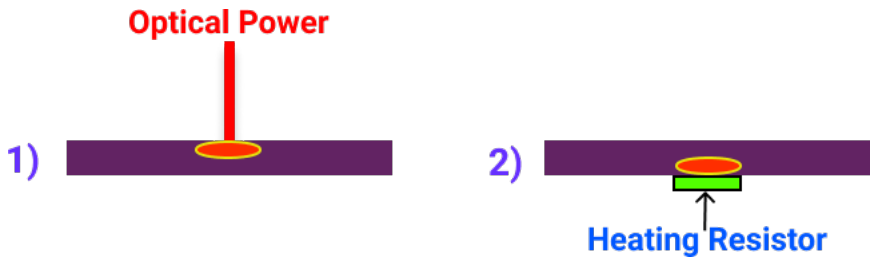


Figure 2. Demonstrates optical heating mode (1) vs electrical heating mode (2). Where in electrical heating mode, the photodiode is heated electrically through a bonded heating resistor on backside of photodiode.

In this master project, to generate electrical heating, the heating resistors are fabricated by the photolithography process and integrated through bonding procedure to the backside of the photodiode. It will also make it possible to use an alternative type of photodiode, such as Indium gallium arsenide (InGaAs). The master project is being carried out in partnership with Justervesenet, Norway's metrology institute. The fabricated resistors are integrated into an electric substitution radiometer (ESR) equipped with a predictable quantum efficient detector (PQED) to assemble a dual-mode detector module for the European research project chipS·CALe [1]. The goal of this research is to develop high-precision optical power measurement techniques using silicon photodiodes.

1.2 Thesis Objective

The aim of this thesis is to provide an overview of design, simulations, and fabrication of heating resistors by the photolithography process. The following are the objectives:

1. Fabrication of heating resistors with suitable resistance.
2. Develop a thinning process for thinning the chips to 100 µm.
3. Thermal simulations in COMSOL to ensure good performance.

1.3 Thesis Structure

Chapter 2 of this thesis describes the relevant theoretical background for this work.

Chapter 3 shows the materials and methods that were used to fabricate the heating resistors, finite element method simulations, and the assembly of the dual mode detector module.

In chapter 4, results are presented.

Chapter 5 presents a discussion based on findings, results, and fabrication procedure.

Chapter 6 presents the conclusion.

2 Theoretical Background

2.1 Microfabrication

Microfabrication is also known as micromachining, or micromanufacturing is the process of fabricating device with a dimension feature in micrometer range. It involves thin films deposition and finally, pattern transferring and metal etching through photolithography procedure. In the deposition techniques from gas phase, two main types can be differentiated - physical vapor deposition (PVD) and chemical vapor deposition (CVD) [5].

Micro electromechanical systems (MEMS) is a manufacturing technique that combines mechanical and electrical components to build tiny integrated devices or systems. MEMS, which combines silicon-based microelectronics with micromachining technology, has been recognized as one of the most promising technologies for the 21st century. It has the potential to change both industrial and consumer products [6].

2.1.1 Physical Vapor Deposition

Nowadays, sputtering and evaporation, which are both instances of PVD, are used to deposit different types of thin films during ICs (integrated circuits) and micro machines fabrication. One of the oldest thin film deposition techniques is thermal evaporation. The working principle of thermal evaporation is based on vaporizing of a metal target onto a substrate in a vacuum chamber, by applying a strong current which is passed through a tungsten filament target holder.

In sputtering technique, usually argon, a plasma gas is used to eject atoms from a metal target source and bombard the surface of the substrate with highly energised particles. Sputtering is preferable over thermal evaporation in many applications because it allows for a greater variety of materials to be used, better substrate adhesion, and a deposition rate of one atomic layer per second which allows metal films to be deposited in nanometer range with a good control and better substrate adhesion. On the other hand, the deposition rate of thermal evaporation is a thousand atomic layers per second [5]. In this thesis, sputtering technique is used for thin films deposition of TiW and Au on silicon oxide wafer (SiO_2).

2.1.2 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is used to coat a wide range of materials, such as solid thin film on substrate surfaces. The coating process includes a precursor gas or gases which are delivered into a chamber that is loaded by one or more heated targets. Chemical reactions occur at or near hot surfaces (typically temperature is above 300 ºC) which leads to deposition of thin film on the surface. Intermolecular collisions occur in diffusive convective transport to the substrate, as a result, mass and heat transfer modeling of deposition rates are substantially more difficult than in PVD. CVD includes different processes such as plasma enhanced CVD (PECVD) which has some advantage over other techniques mentioned. For instance, it operates in lower substrate temperatures, better film adhesion can be achieved, and it also has a good step coverage [5, 7].

2.1.3 Photolithography

Photolithography, by far the most widely used form of lithography, transfers mask patterns on deposited thin films over silicon wafer. It includes several steps and starts by dispensing photoresist, an ultraviolet radiation sensitive polymer by a spinner machine on the surface of a silicon wafer. The thickness of the photoresist layer depends on the spinning duration, spinning speed, and photoresist viscosity. Pattern transfer is commonly done by ultraviolet light (UV light) exposed through a mask. The mask is made of mylar, optically qualified glass, or quartz with a metal pattern absorber. The exposure of UV light on the mask affects properties of the parts of the photoresist that are exposed to light, whereas those parts that are covered by the mask remain intact. The positive tone of the photoresist will become stronger, while the negative tone of the photoresist will become weaker due to exposure to UV light. To remove unwanted parts of the photoresist (sacrificial layer), a water-based solution, (which is called developer), is used. Before almost all of the photoresists are removed, the next step is etching of the unwanted film by a solvent to create the pattern that is already transferred by the mask onto the wafer [5].

2.2 Optical Metrology

Optical metrology is the science and technique of using light to establish measurement standards. These measurements can be used to determine the qualities of light and light sources, including the dimensions, distances, and temperatures of objects [8] [9].

In the study of visible radiation, a key measurement technique of optical power utilized by national metrology institutes around the world is the electrical substitution radiometer, operating at cryogenic temperatures [10].

2.2.1 Electric Substitution Radiometer

The working principle of ESR is based on measurements of temperature increase of the detector by a temperature sensor, during applying either optical radiation or electrical heating modes in relation to a heat sink with a constant temperature [11].

A bolometer quantifies temperature increase by a temperature sensor as a result of electromagnetic radiation. For an optical or an electrical signal, the operating principle of an electrical substitution radiometer and bolometer is assumed in the same way. The comparative approach presented in **Figure 3** can be used to calibrate photodetectors [12].

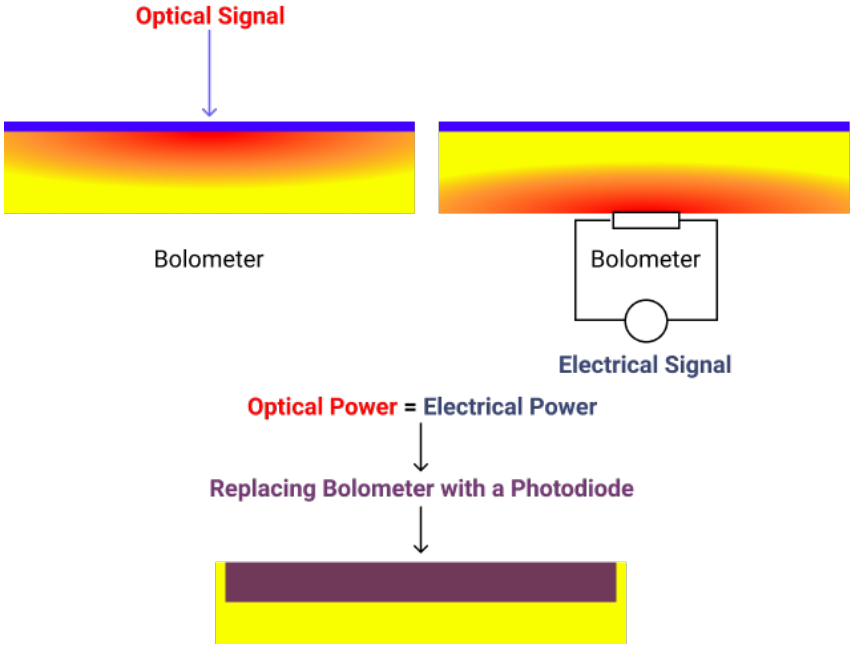


Figure 3. Calibration of photodetectors by replacing the bolometer with a photodiode.

2.2.2 Cryogenic Radiometer

The Cryogenic radiometer (CR) is an ESR-based radiometer that operating at extremely low temperatures (cryogenic temperatures). The National Institute of Standards and Technology (NIST) developed a precise cryogenic radiometer which has a relative standard uncertainty of around 210 ppm to serve as a primary standard for optical power measurements at an optical power level of 0.8 mW. **Figure 4** illustrates structural details of a NIST precise cryogenic radiometer [13].

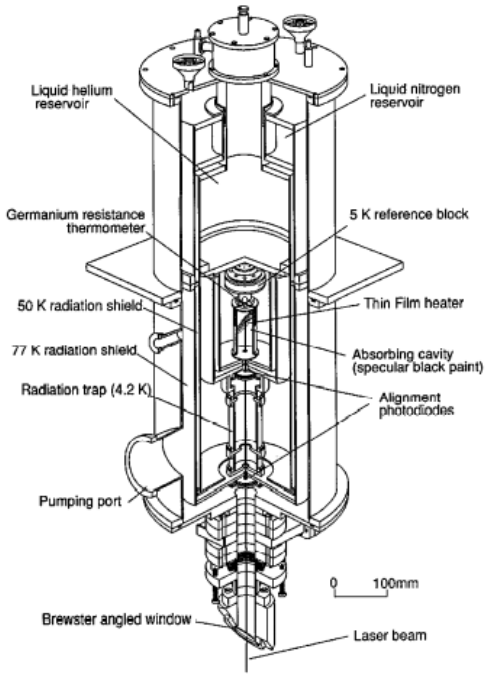


Figure 4. Cryogenic radiometer having a high precision from NIST. Adapted from [13].

The device's copper cavity absorbs incoming beam and is designed to enhance the beam absorption. On the cavity, an electrical heater is used to yield the same temperature rise as optical power, applied on the cavity. The generated heat through optical and electrical heating modes leads through a weak thermal link to a reference block with a fixed temperature. The magnitude of optical power is determined by comparing temperature rise in electrical and optical modes [13]. Apart from measurement precision, CR requires a complex setup, and it is not a cost-efficient solution for optical measurements [1].

2.2.3 PQED

The predictable quantum efficient detector (PQED) is an induced junction silicon photodiode with a high efficiency. It consists of low doping p-type Si crystal surface, covered by a coated layer of silicon dioxide (SiO_2). Low-doping leads to reduction of reflectance and losses in carrier charge. Simultaneously, the positive surface charge of the SiO_2 layer generates an inversion layer in the Si substrate, leading in a p–n junction [14]. In a real case, all photodiodes have reflection loss which implies that some of the incoming photons are reflected from the surface. On the other hands, dust particles on the surface may also absorb or disperse the photons [4].

Figure 5 illustrates the cross section of PQED and its architecture.

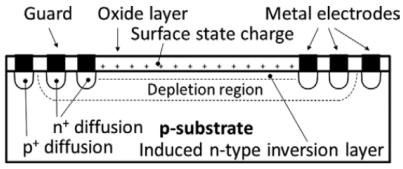


Figure 5. Illustrates cross section of internal construction of the PQED's induced junction photodiode. Adapted from [15].

2.3 Chip.Scale

The accurate and simplified measurement of the light spectrum is highly important for the photonics industry, health, and science. Currently, the uncertainty of the measurement of optical power is limited by the spectral responsivity of silicon detectors, proficient operators, and costs. In response to the current needs of the measurement-accuracy of optical power, there is a need to develop techniques using silicon photodiodes, therefore chipS·CALe intends to develop an "NMI-on-a-chip" for the first time with improved technology to enhance and simplify optical power measurements, followed by new metrology which allows predicting responsivity of photodetectors in a wide-spectrum range by measuring only one wavelength [1].

2.3.1 DMD

The dual mode detector (DMD) is a self-calibrating device that can accurately measure optical power. The integration of PQED and CR into a single module makes it possible to measure increasing of temperature by a temperature sensor during optical and electrical heating modes. The DMD have two induced junction silicon photodiodes that are stacked in a trap structure to reduce reflection loss. In electrical heating mode, the photodiode is heated electrically either by applying a forward bias which previously was done in [4]. Whereas in a new DMD design which will be explained in more details, the electrical heating is generated through integration of a heating resistor on backside of the photodiode to produce the same amount of heat as in optical heating mode. Therefore, estimation of unknown optical power can be done by comparing the temperature rise generated by known electrical power with optical heating mode [16].

The DMD's latest design is optimized to minimize the non-equivalence between optical and electrical heating modes to lower than 100 ppm at room temperature. This can be achieved by design of a new PCB with four-leg compared to previous design which had one-leg structure. The optimization in new design leads to a better heat transfer through new four-leg PCB tracks and by bonding of the fabricated resistor chips on backside of the photodiode to electrically heat the photodiode instead of previous method which has been done by applying a forward bias. The absorbed heat by photodiode that is induced by optical power or electrical power, conducts to 4 bonded diced pieces of Au coated wafer, where leads to centre of bottom PCB tracks. A temperature sensor is soldered in the middle of the bottom PCB tracks to record temperature differences and compare it with top reference temperature sensor which is operate at ambient temperature. The bottom PCB is bonded via epoxy over an aerogel spacer to provide a high thermal resistance to the copper reference heat sink which will be kept at a fixed temperature during measurement experiment. Figure 6 illustrates the new design of DMD with different parts. [16].

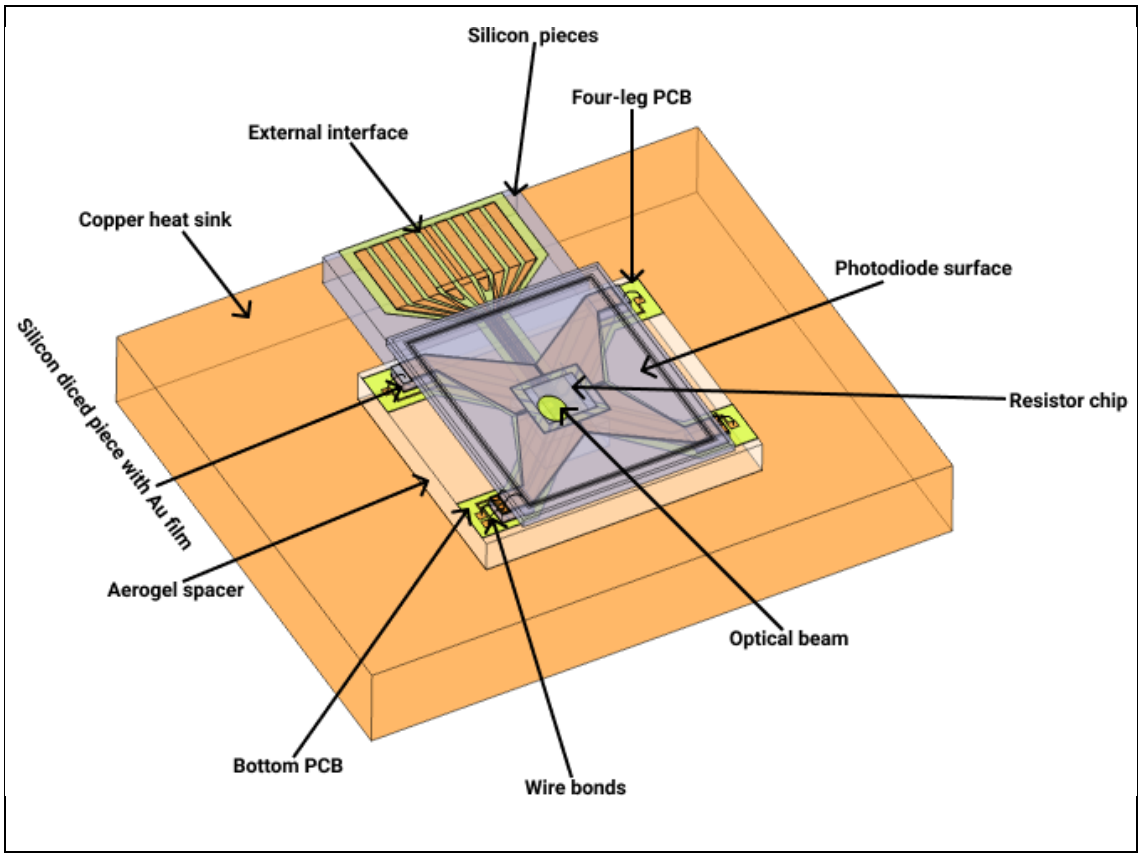


Figure 6. The Dual Mode Detector Module.

2.4 Resistors

The resistor is a widely used passive component. Its main purpose is to restrict the current flow. The resistor's value is measured in ohms and is known as resistance [17]. Ohm's law is expressed as:

$$R = \frac{V}{I} \qquad (2.1)$$

Resistors are applied in a variety of applications for different purposes such as generate heat, regulate electric current, and adjust time constants.

"Heater resistors are a special type of power resistors whose main purpose is to convert electrical energy into heat" [17].

When a current passes through a resistor, it dissipates power. Heat is produced as a result of the dissipation of energy. The power is a function of the applied voltage V and the current I and can be calculated using Ohm's power law:

$$P = V \cdot I \qquad (2.2)$$

P stands for power in watts.

The material's capacity to resist the electric current flow is known as electrical resistivity ρ and expressed in Ohm-meters (Ω·m). Materials with a high resistance do not conduct electric charges well. It is the equivalent to reciprocal of electrical conductivity which quantify the materials conduction degree [17]:

$$\rho = \frac{1}{\sigma} \qquad (2.3)$$

The concepts "resistance" and "resistivity" are not equal. Resistance is indeed an object property, whereas resistivity is a material property [17]. It is expressed in ohms. A wire's resistance is determined by three factors: resistivity, length, and diameter.

The following is the formula for calculating wire resistance:

$$R = \rho \frac{l}{A} \qquad (2.4)$$

Where R is the resistance (Ω), ρ material resistivity (Ωm), l length (m), and A cross-sectional area (m^2).

The length and area relationship states that the longer the wire, the greater the resistance. The larger the surface area, the lower the resistance. The resistance can be calculated by replacing ρ with conductivity:

$$R = \frac{l}{\sigma A} \qquad (2.5)$$

2.5 Thermal Physics

The study of heat and temperature is known as thermal physics. Heat is described as a form of energy transfer between two objects that flows from a warmer to a colder object due to temperature differences [18].

Any natural transfer of energy from one medium to another, induced by a temperature difference between the mediums, is known as heat. Three categories include conduction, convection, and radiation are classified as heat transfer based on the mechanism involved [19].

2.5.1 Thermal Conduction in Solids

Electrons, electromagnetic waves, or other excitations can all be used to transfer heat energy through solids. Electrical carriers transmit most of the heat in metals. The major heat transporter in insulators is lattice waves or phonons [20].

The term "thermal conductivity" is used to describe the ability of a material to conduct heat:

$$k = -\frac{Q}{\Delta T} \qquad (2.6)$$

where absolute temperature is denoted by T, and Q is flow rate or heat flux.

2.5.2 Thermal Radiation

At non-zero temperatures, all matter emits electromagnetic radiation. Thermal radiation is the term for this. Since most of the emission occurs in infrared range of electromagnetic

spectrum and is beyond visible range of human eyes, one may not noticed this effect on items at room temperature [21].

The Stefan-Boltzmann law defines the relationship between an object's temperature, surface area, and the rate at which heat is emitted or absorbed from the surface.

$$P = \varepsilon\sigma A(T^4 - T_0{}^4) \qquad (2.7)$$

In this equation, P is net heat flow rate emitted or absorbed, ε is surface emissivity of material that either emits or absorbs thermal radiation. The emissivity ranging between a minimum value of 0 and a maximum value of 1. σ is Stefan's constant, 5.670×10^{-8} W/m^2K^4, A is the surface area m^2, T is object absolute temperature in K that emits or absorbs the thermal radiation, and $T0$ is absolute ambient temperature or environment temperature in K.

3 Materials and Methods

This chapter covers the design, simulations, material selection, sputtering, photolithography fabrication of heating resistors, integration of a selected resistor via a bonding technique to the backside of the photodiode, and lastly the assembly of the dual-mode detector module. The fabrication of heating resistors and assembly of the dual-mode detector module were done in laboratory and clean room facilities at the University of South-Eastern Norway, Department of Microsystems. **Figure 7** shows how this research was carried out in a step-by-step manner.

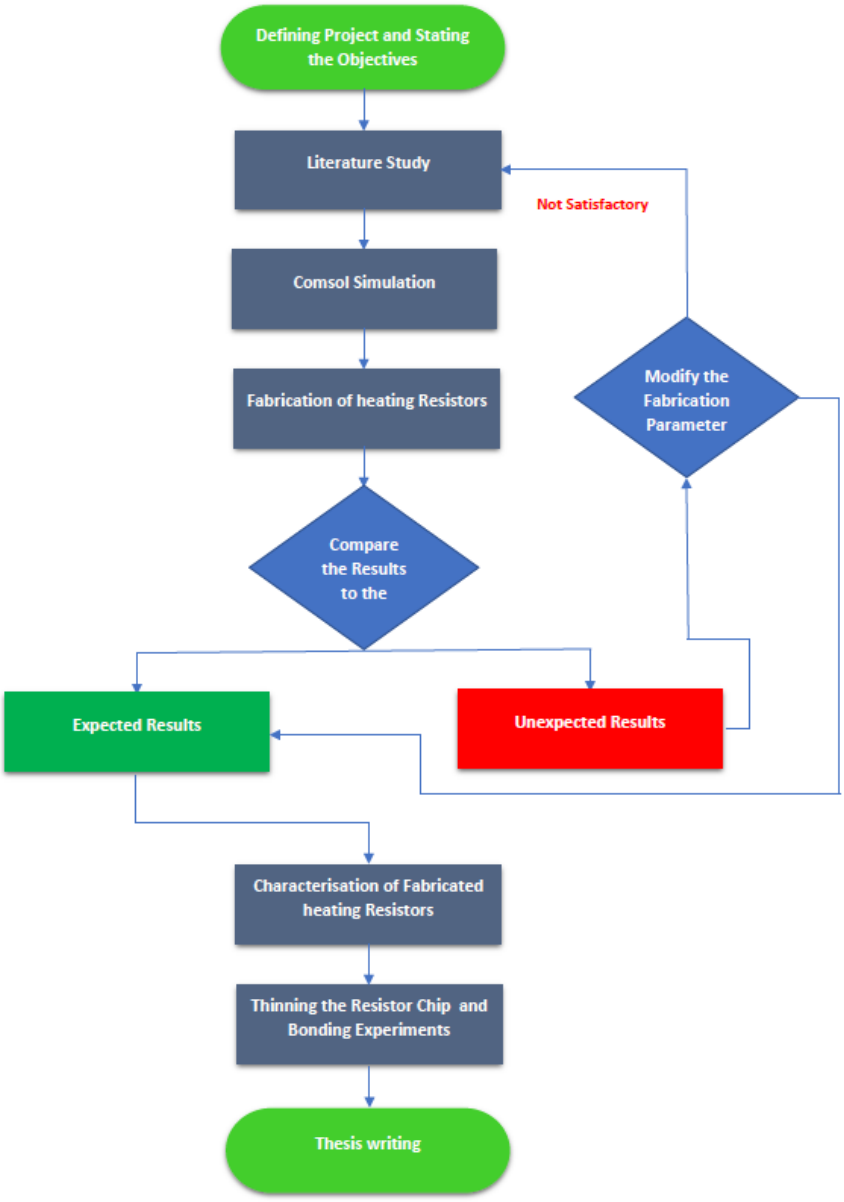


Figure 7. Workflow Diagram for this project.

3.1 Material Selection for Resistor Layer and Pad Layer

The fabrication of resistors through photolithography steps requires the materials that are suitable for deposition on silicon wafers in terms of adhesion and having high resistivity. Checking material properties helps to find suitable materials for the resistor layers. Materials like chromium, titanium, titanium tungsten (TiW) have high binding robustness with oxygen, as a result, they have very good adhesion to SiO_2 wafers, therefore, it bonds easily with them. Additionally, Au and titanium react to form a strong bond. [22]. By comparing the electrical resistivity of chromium and titanium showed in Table I, it can be seen that titanium is a fitting candidate to use as a resistor layer due to higher resistivity. Furthermore, a thin titanium layer enables for the fabrication of heating resistors on a tiny structure. For resistor pads, Au was selected because of its high conductivity and ability to make interconnections via wire bonding technique to the top PCB. Due to safety reasons in our clean room, using hydrofluoric acid (HF) to etch titanium is avoided, therefore instead of pure titanium, TiW (90/10%) was utilized.

Table I. Resistivity and conductivity of titanium, tungsten, and chromium at 20°C. Adapted from [23].

Material	Resistivity ρ (Ω•m) at 20 °C	Conductivity σ (S/m) at 20 °C
Titanium	5.56×10^{-7}	1.798×10^{6}
Tungsten	5.49×10^{-8}	1.82×10^{7}
Chromium	1.96×10^{-7}	5.10×10^{6}

3.2 Design and Simulation of Heating Resistors

The Finite Element Method (FEM) simulation was performed by COMSOL Multiphysics 5.6 to design the heating resistor structure, calculate resistance value and verify the thermal performance through the heat transfer module.

3.2.1 Resistor Structure

The resistor chip have a width of 3 mm x 3 mm, enclosing 2.56 mm, 2.5 mm, and 2.4 mm diameter circular resistor lines. They have circular shape to replicate optical beam and generate similar heating profile. In the designing process, 3 x 3 mm resistor chip width is designed to keep it small enough, and also to provide a sufficient wire bonding pad spaces. Three different lines spaces between resistor line and bonding pads; 20 μm, 50 μm, and 100 μm were considered to minimize risk of having problems during pattern transferal, due to photolithography masks and the capacity to develop wafers according to existing cleanroom equipment. Figures below show three mentioned resistor designs with lines spaces of 20 μm, 50 μm, and 100 μm respectively. The gray color in the following figures refer to the resistor lines with selected TiW as material and the yellow area indicates Au layer that is used as bonding pads as well as covering layer to reduce emissivity effect of blank SiO_2 area on the surface of resistor chip.

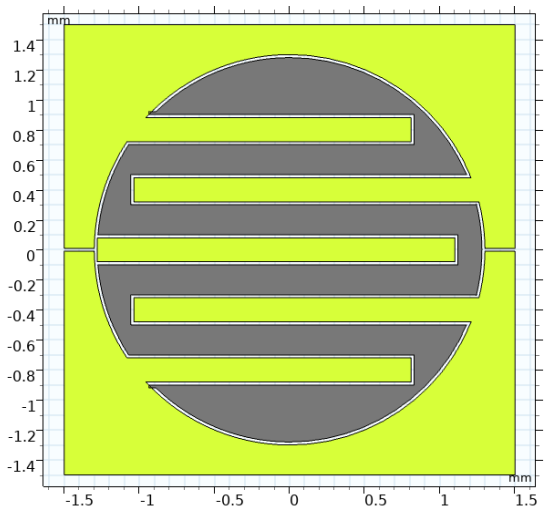


Figure 8. Resistor chip, enclosing 2.56 mm circular resistor with line spaces of 20 µm.

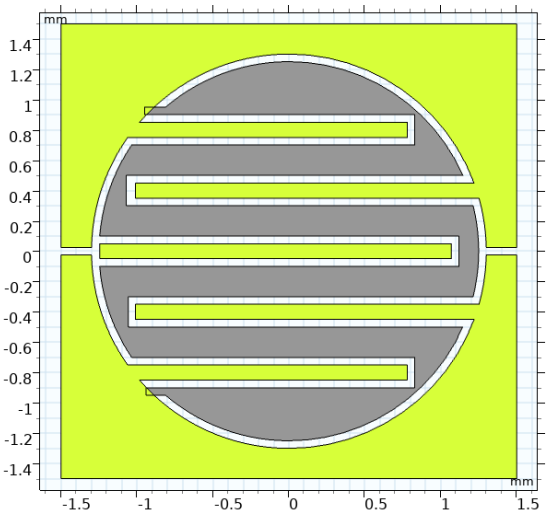


Figure 9. Resistor chip, enclosing 2.5 mm circular resistor with line spaces of 50 µm.

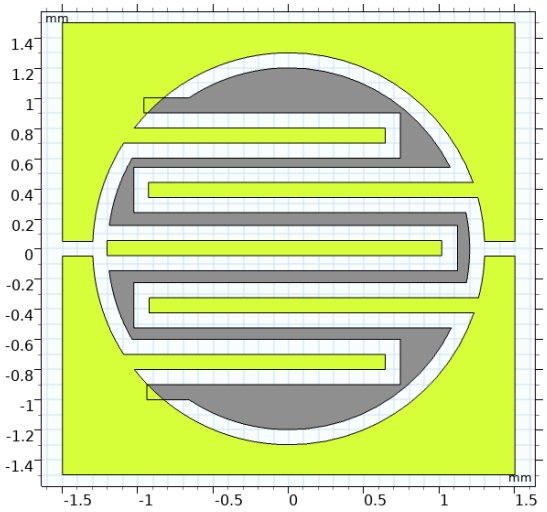


Figure 10. Resistor chip, enclosing 2.4 mm circular resistor with line spaces of 100 µm.

3.2.2 Motivation for Thinning the Resistor Chips

The reasons why thinning the resistor chip is important in this work are:
First it should be bonded on backside of the photodiode, where another PCB (bottom PCB) is located close to the photodiode. This increases the risk of short connection between resistor chip and the PCB. Secondly, the rate of heat transfer is inversely proportional to the thickness of the resistor chip [24].

3.2.3 Electrical Resistance Calculation

To find electrical resistance of mentioned structures in COMSOL, the electrical conductivity of TiW is needed. According to previous research [25] the electrical resistivity of TiW films, based on chemical composition for this case, TiW (90/10%) can be estimated to approximately 100 μOhm cm. The simulations of the resistance value of resistors can be performed using COMSOL. To do this, 1 V was applied to one resistor pad (Terminal 2) and for the other pad (Terminal 1), the value was set to 0. After that, the thickness of resistor layout should be increased to 50 nm.

3.2.4 Thermal Simulation

To study heating profile differences between optical and electrical heating modes, two heat transfer phenomena were simulated. Radiative heat transfer from top surface of the photodiode and resistor chip surface as well as conductive heat transfer for both optical and electrical heating mode. The simulations were performed by creating a simplified version of the DMD module in COMSOL. The model consists of geometries for the photodiode, silicon chip, epoxy layers, heating resistor, and 4 silicon legs. First, heat transfer mechanism in solids physics which allows to study conduction, convection, and radiation was added in COMSOL. Next, resistor lines were selected as electrical boundary heat source with 1 mW applied power. Then a cylinder shape equal to thickness of resistor chip (53 μm) was added on top of the photodiode surface which was used as optical boundary heat source with the same power was used in electrical boundary heat source. Then two studies were added, one assigned to electrical heating mode the other one assigned to optical heating mode. Next, surface radiation was estimated in COMSOL using equation (2.7) to account for heat radiation from top surface of the photodiode, back surface of the photodiode which is covered by aluminum, and the resistor chip surface. Finally, a fixed temperature of 293.15 K was set to the bottom of legs.

By performing these simulation and probing conducted heat between silicon and epoxy legs the difference between two heating modes can be estimated. This will be called non-equivalence between optical and electrical heating modes based on radiative heat flux and normal conducted heat flux and defined as following:

$$\gamma = \frac{Rfo - Rfe}{Rfo} \qquad (3.1)$$

Where γ the non-equivalence, R_{fo} is radiative heat flux in optical heating mode, R_{fe} is radiative heat flux in electrical heating mode. Similarly, the non-equivalence between conductive heat flux in optical and electrical heating modes can be calculated.

In this work, resistor chip thickness, epoxy thickness (see **Figure 11**), and resistor chip emissivity are considered as variables to study the non-equivalence in part per million (ppm), between electrical heating mode and optical heating mode. The emissivity values of epoxy, silicon surface of the photodiode, and aluminum backside of photodiode were set to 0.45, 1, and 0.8 respectively. However, there is no information about TiW's emissivity but the estimated value by [16] was considered and 0.1 was selected for initial emissivity simulation value of TiW and increased to a max value of 1.

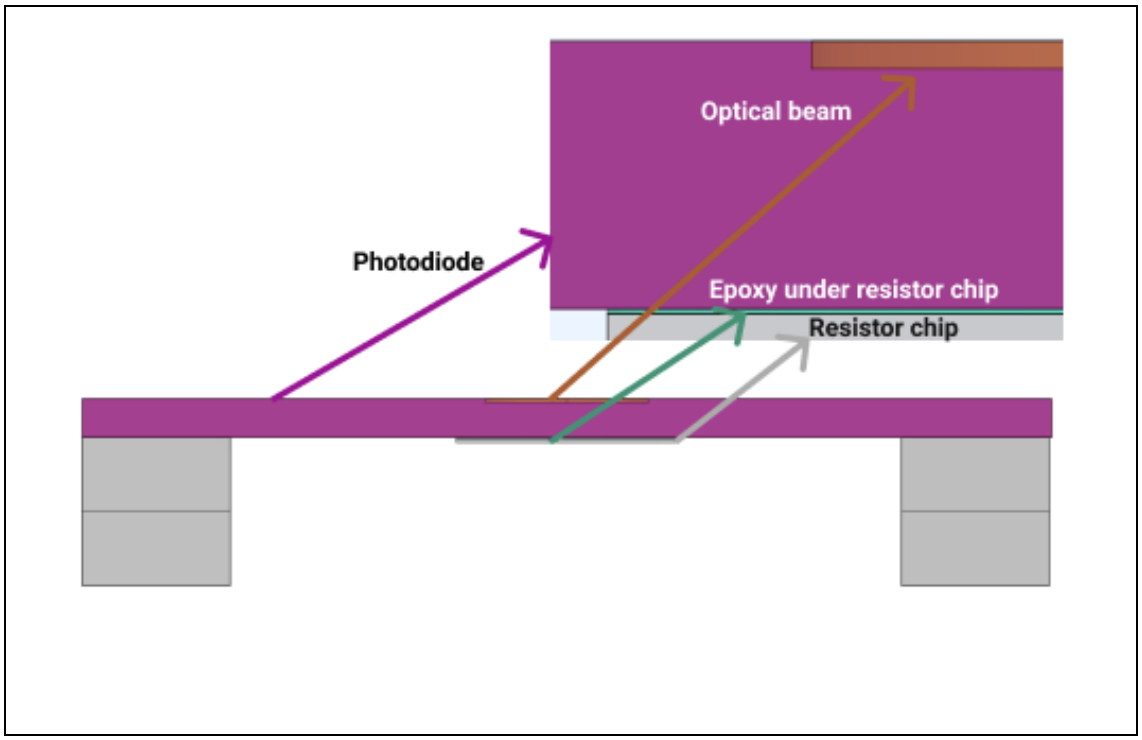


Figure 11. Illustrates resistor chip thickness and epoxy thickness in COMSOL model.

Figure 12 shows the simulation model with different parts that was created in COMSOL.

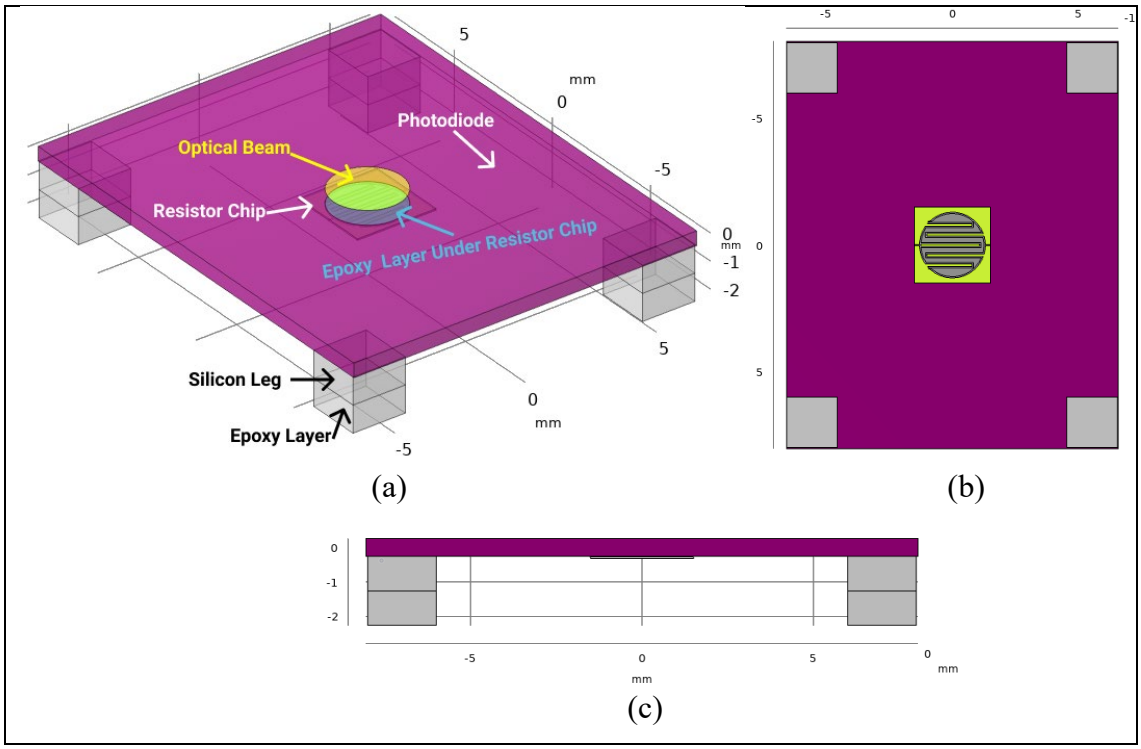


Figure 12: (a) Shows transparent side view of simulated model in COMSOL with details. (b) Shows bottom view of model with resistor chip. (c) Shows transparent cross-section of simulated model.

3.3 Fabrication Process of TiW Thin Film Resistors

Figure 13 Illustrates the fabrication steps in this section.

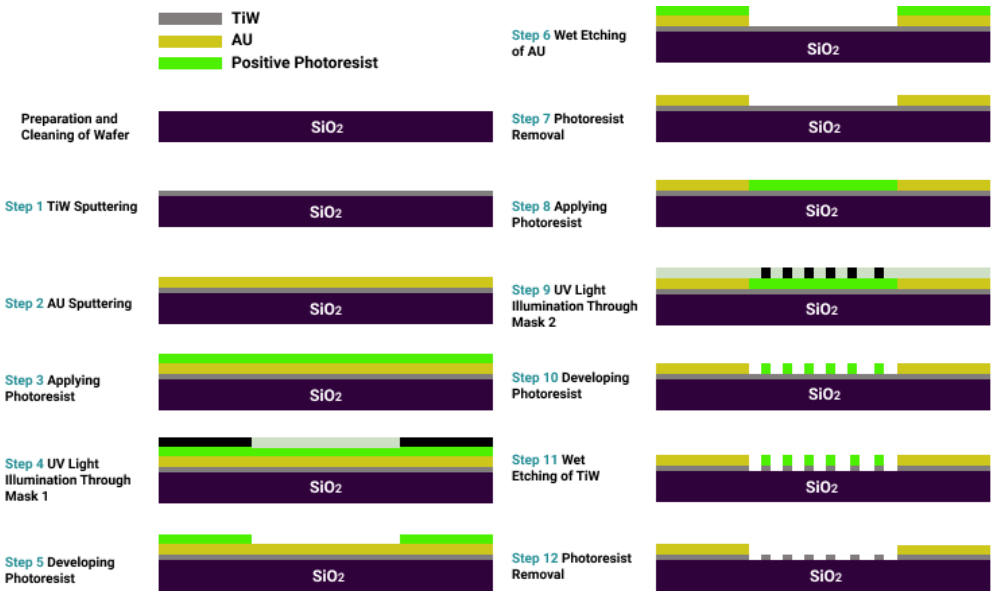


Figure 13. Illustrates the fabrication procedure of TiW resistors through PVD by sputtering technique and photolithography.

3.3.1 Wafer Cleaning

The wet and dry cleaning procedure were done before the sputtering process to remove contaminants which might degrade adhesion of TiW film on the wafer.

The wet cleaning procedure was started by fixing the wafer into a dipper (wafer holder) and immerse into acetone. Next, isopropanol was sprayed over the surface of wafer. Then, it was rinsed in deionized water (DI-water) bath. After that, the wafer was placed on a paper to be dried, and nitrogen was used to remove visible drops of DI-water. Finally, the wafer was placed on a hot plate with a temperature of 115°C and kept for 5 minutes to dry remained water on the wafer.

The dry cleaning procedure was started by placing wafer into Alpha-Plasma's vacuum chamber for 4 minutes. The cleaning parameters were used are shown in Table II.

Table II. Parameters were used to clean the wafer by plasma cleaner.

Gas	Gas flow rate	Power
ARGON	90 cm^3/s	250 W
OXYGEN	10 cm^3/s	250 W

3.3.2 Sputtering Deposition of TiW and Au

A cleaned wafer was loaded into AJA International sputter machine. Next, the target materials were selected to Ti (90%) / W (10%) via deposition controller panel. After that, the deposition parameters were set by a computer attached to the sputtering machine on its provided software. Finally, by reaching 15 nm thickness of the deposited TiW, sputtering process was stopped, and target changed to Au to deposit 300 nm over TiW film. The second wafer had similar procedure except the thickness of deposited TiW, which was 50 nm. The details of sputtering parameters for both wafers are shown in Table III and Table IV.

Table III. Sputtering deposition parameters were used for Wafer 1.

Target	Pressure	Gas	Rate	Power	Thickness
TiW	6.5 Pa	9 Pa	0.23 (Å/S)	40 W	15 nm
Gold	6.5 Pa	9 Pa	0.31 (Å/S)	20 W	300 nm

Table IV. Sputtering deposition parameters were used for Wafer 2.

Target	Pressure	Gas	Rate	Power	Thickness
TiW	6.5 Pa	9 Pa	0.23 (Å/S)	40 W	50 nm
Gold	6.5 Pa	9 Pa	0.30 (Å/S)	20 W	300 nm

3.3.3 Cleaning Process of Film Deposited wafers

The deposited SiO_2 wafers were cleaned before starting the photolithography process. The cleaning procedure was started by spraying isopropanol over the surface of wafer. Next, it was rinsed in DI-water bath. Then, the wafer was placed on a paper, and nitrogen was used to dry and remove visible drops of DI-water. Finally, the wafer was placed on a hot plate with the temperature of 115°C, for 5 minutes to make sure the remained DI-water on the wafer is removed.

3.3.4 Photolithography Procedure for Au layer

The photolithography process for Au layer was started by placing the wafer in the center of SPIN 150, a spinner machine which is used to spread photoresist on surface of wafer. Next, S1813 positive photoresist was poured on the center of the wafer.
The wafer spun for 60 seconds totally, in each step the wafer spun for 30 seconds. The programs details were used are shown in Table V.

Table V. SPIN 150 programs details.

Step	**1**	**Step**	**2**
Time	30s	Time	30s
Speed	1300rpm	Speed	2000rpm
Acceleration	1000rpm/s	Acceleration	1000rpm/s

After that, the wafer was placed on a hot plate and soft-baked for 5 minutes at 115°C. After soft baking, the wafer placed on the wafer carrier to cool down to room temperature. The resistors pad layer mask 1 (made of mylar) shown in **Figure 14.** was fixed on a glass plate and placed into EVG 620 machine which is used to align the mask with the wafer using mask markers and expose UV light through the mask. Finally, UV light illuminated through the mask for 25 seconds, and the mask pattern was transferred on the wafer.

Figure 14. Mask 1 which was used for transferring Au pattern and later will be used as resistor pads layer.

The wafer placed on wafer carrier for around 3 minutes. Next, MF-319 developer was used to develop the photoresist. The wafer was loaded on dipper and placed into the

developer for 26 seconds. Then, it was immersed in inside DI-water bath to remove sacrificial layer of photoresist. Next, the wafer was dried by nitrogen.
The Dektak 150 profilometer was used to measure thickness of the photoresist on the wafers. After measuring the thickness of photoresist after soft baking, the wafer was hard baked for 1 minute and thickness of photoresist was measured again.

For etching Au layer, a mixture of **KI**, **I_2,** and **H_20** with the composition percentages is shown in Table VI was used.

Table VI. Composition percentages of Au etcher.

Name	%
H_20	60 - 80
KI	10 - 30
I_2	1 - 10

The chemical reaction for the Au etcher is shown in R1-1.

$$KI + I_2 + H_2O \rightarrow HI + KIO_3 \quad \text{(R1-1)}$$

The wafer was placed into the solution and shaked. Next, was inspected and some of the Au was not etched, therefore was placed again into the solution for 30 seconds more. Then, the wafer was cleaned by Di-water to remove etched gold particles. After that, the thickness of gold and the thickness of gold + thickness of photoresist were measured. The photoresist completely removed with acetone and isopropanol was used to clean the wafer. The visible remaining water dried by nitrogen and placed on a hot plate for 5 minutes to dry the remained Di-water on the wafer. The resistors gold pads were developed here. In the following, the etching procedure of TiW (resistors layer) will be discussed.

3.3.5 Photolithography procedure Tiw layer

The same spinning process as in the previous step was used for TiW layer. After that, the wafer was placed on a hot plate and soft-baked for 3 minutes at 115°C. After soft baking, the wafer placed on the wafer carrier to cool down to room temperature. The resistors

lines layer mask 2 (made of mylar) shown in **Figure 15** was fixed on a glass plate and placed in EVG 620 machine.

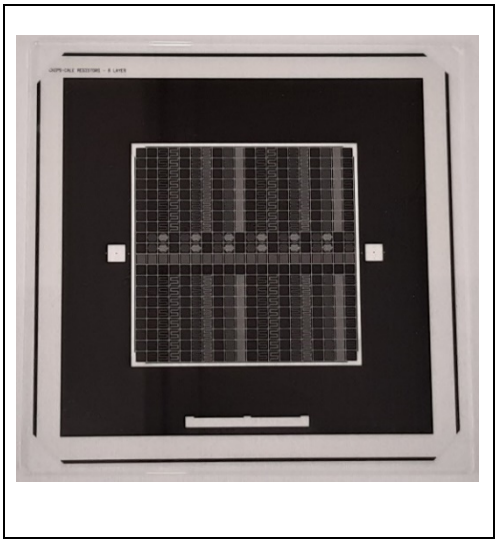


Figure 15. Mask 2 which was used for transferring TiW pattern and later will be used as resistors lines layer.

The overlay alignment accuracy is crucial here to align the alignment mark of Mask 2 with Mask 1.

After developing the wafer with similar process as before, the wafer 1 hard-baked for 1 minute and the wafer 2 hard-baked for 3 minutes. Then, thickness of photoresist on wafer 1 and wafer 2 after hard-baking was measured.

Next, H_2O_2 30% (Hydrogen peroxide) warmed to the temperature of 52 °C and the wafer was placed into it for 2 minutes to etch TiW.

The wafer was cleaned by DI-water to remove the etched TiW particles Afterward, the photoresist completely removed with acetone, and isopropanol was used to clean the wafer. The visible remaining water dried by nitrogen and placed on a heater for 5 minutes to dry the wafer. Unfortunately, after investigation of wafer 1, the TiW layer was completely etched.

The wafer 2 was diced into two parts to have a better control on TiW etching and prevent loss of the whole wafer, in case of extra TiW etching.

Here the resistors TiW lines on wafer 2 were developed. Then the thickness of the TiW layer was measured.

3.4 Dicing the Resistors

The dicing of resistor chips were performed by Disco DAD 3220, an automatic dicing saw with advance water flow rate controller [26]. The dicing saw start point, and dicing saw alignments were done by Semi-auto mode. 3.12 mm dicing distance was use for each resistor chip.

3.5 Thinning the resistor

In this experiment, for thinning the resistor chips, a MultiPrep system grinding / polishing device by Allied company was used (see **Figure 16).**
In the following, steps will be discussed in detail.

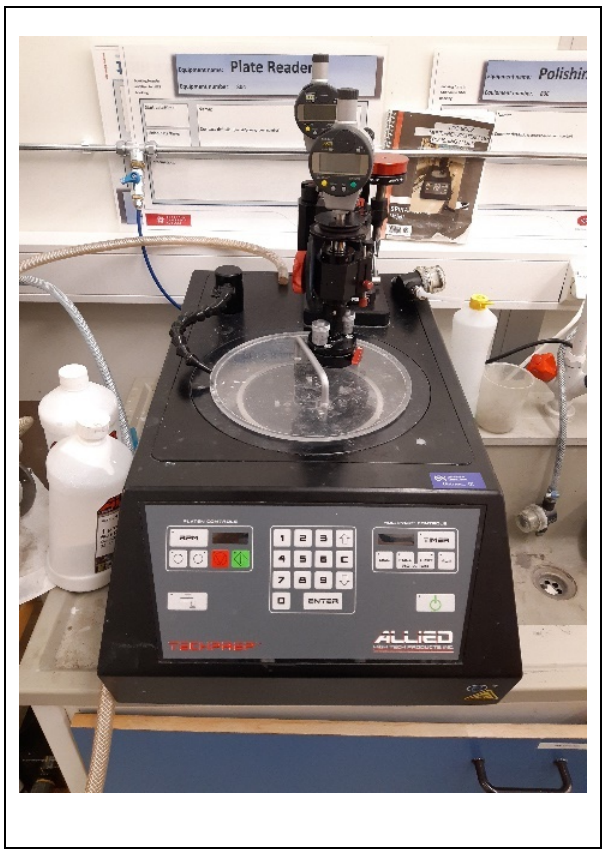


Figure 16. Shows the MultiPrep system grinding / polishing that was used to thin the resistor chips.

3.5.1 Grinding Steps

First, polishing fixture was placed on a heater with a temperature of 80°C to be warmed. Next, mounting paste wax was melted over the surface of polishing fixture and diced resistor chip from top side was placed on wax dispensed area and around the chip was

covered by wax. Then, the polishing fixture was taken from heater and left to cool down to room temperature.

Figure 17. Shows the resistor chip fixed on polishing fixture using mounting paste wax.

After that, polishing fixture was placed on a HEIDENHAIN thickness gauge plate to measure the thickness of chip + melted wax under the chip. A silicon carbide paper 400 (P-800) with adhesive side was fixed on griding plate and polishing fixture was loaded to grinding machine and grinded with 100 RPM speed in 75 seconds to reach to 70 µm thickness. Finally, the polishing fixture was unloaded and placed on the heater to melt the wax and separate the resistor chip.

3.5.2 Resistor Chip Cleaning

The thinned resistor chip should be cleaned to completely remove melted paste wax and be ready for bonding. The cleaning was performed by gently immersing the thinned resistor chip in acetone. Next, it was placed into Branson ultrasonic cleaning bath for 5 minutes. Finally, it was immersed in isopropanol to be ready for bonding procedure.

3.6 Dual Mode Detector Module Assembly Procedure

In the following the packaging of DMD will be explained.

3.6.1 Die Bonding

Die bonding is referred to attaching a die (chip) to its package or substrate during manufacturing process, using epoxy, solder, thermal compression, solid liquid interdiffusion techniques. In die bonding process, the die is picked and attached into an epoxy dispensed location or eutectic solder location. It provides a high level of precision, often 1 to 3 μm, which is far higher than other packaging techniques. [27].

3.6.2 Die Bonding of Resistor Chip to the Photodiode

The bonding process was started by picking a 13.1 mm width and 16.1 mm length photodiode using a FinePlacer Pico flip-chip bonder. Next, Stycast 1266 epoxy dispensed on top PCB legs. Then, the photodiode was aligned with top PCB and gently bonded by 1 N force over the top PCB and left for 24 hours to be cured.

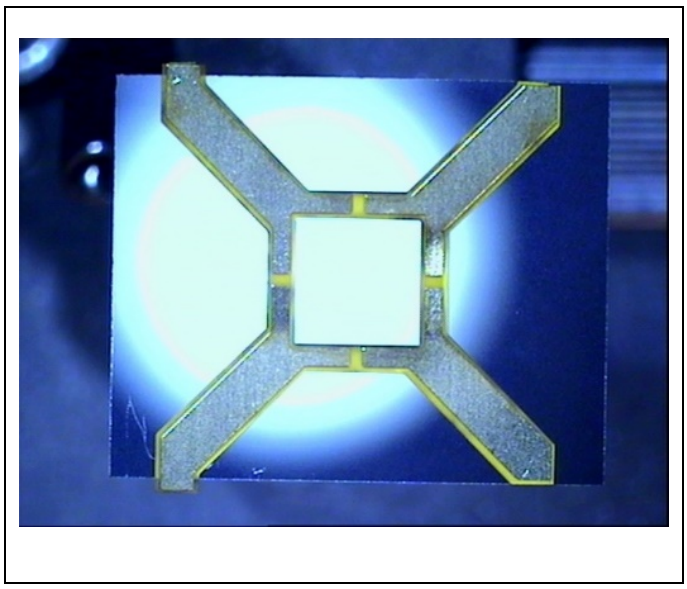


Figure 18. Shows the top PCB bonded to backside of the photodiode.

The thinned resistor chip is picked by flip-chip bonder. Next, small amount of Stycast 1266 epoxy was dispensed on backside of the photodiode.

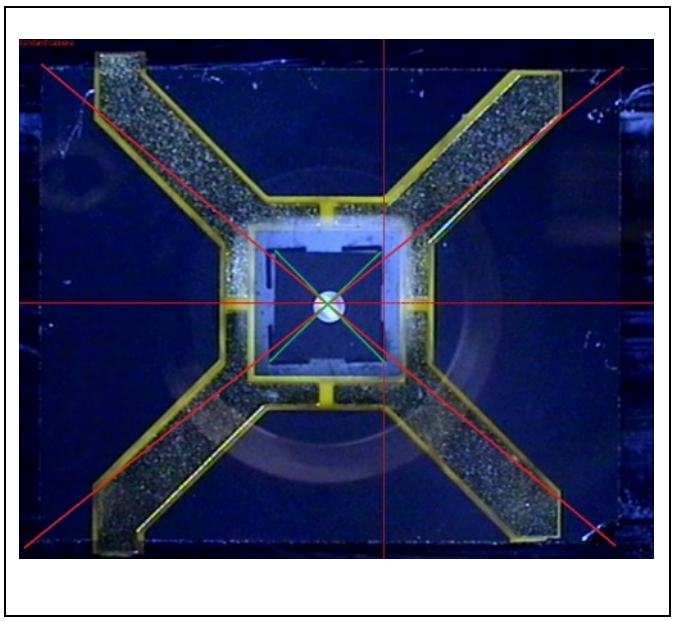


Figure 19. Shows picked resistor chip while was aligning in center of the photodiode and top PCB with the help of marking lines.

Finally, the resistor chip was aligned and bonded on the epoxy dispensed location on backside of the photodiode by applying 1 N force first, and then 5 N force to make sure the epoxy is squeezed enough. Finally, the bonded chip on the photodiode left for 24 hours to be cured.

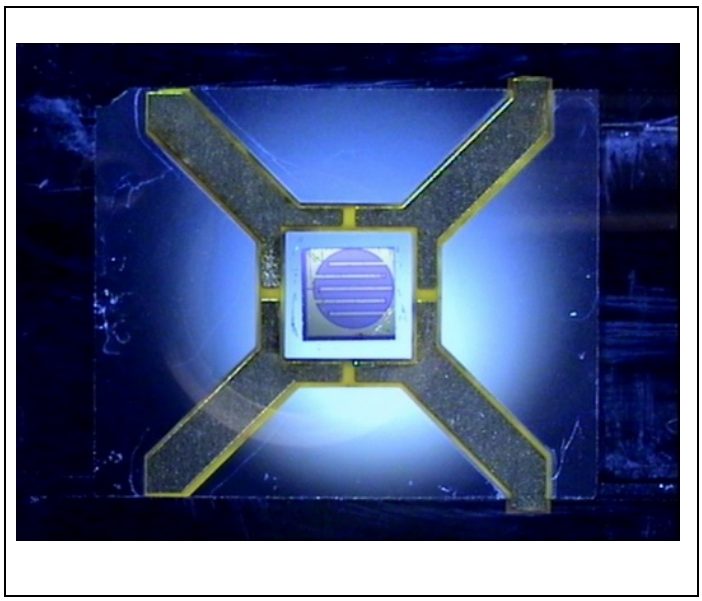


Figure 20. Shows the bonded resistor chip and backside of the photodiode.

3.6.3 Wire bonding of Resistor Chip to Top PCB

The resistor's pads were wire bonded via Al wires to the PCB using TPT Wedge Wire bonder (HB12). A capillary with thickness of 25 μm was used to connect resistor pads to the PCB.

3.6.4 Soldering Temperature Sensors and External Connection Interface Bottom PCB

Two Semitec 103FT1005A5P1 temperature sensors with dimensions of 1 mm x and 0.5 mm x 0.15 mm were soldered on bottom PCB.
One is in the bottom center of PCB and the other one which is used as reference temperature was soldered on top of bottom PCB. Finally, the PCB pads were soldered to an external connection interface by soldering wires.

3.6.5 Flatting the Aerogel

To flat the aerogel spacer surfaces which was cut by scalpel. Similar technique that was used to thin the resistor chips was done. However, as the aerogel is sensitive to acetone and isopropanol, instead of using mounting paste wax, it was fixed by Kapton tape and thinned to 1.8mm.

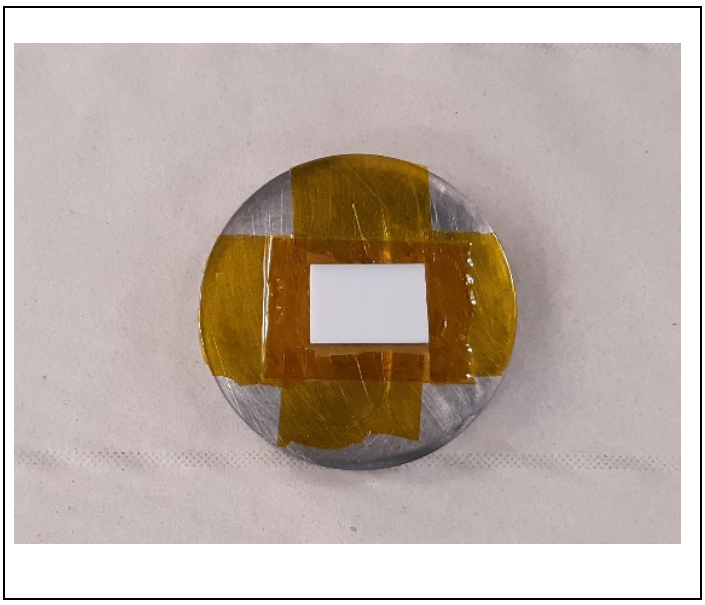


Figure 21. Shows the aerogel fixed on polishing fixture using kapton tape.

Finally, a hole was made by drilling on center of aerogel, to open enough space for keeping bottom temperature sensor, soldered on bottom PCB.

3.6.6 Die bonding of Bottom PCB to Aerogel and Copper Plate

The aerogel was picked by flip-chip bonder and Stycast 1266 epoxy was applied on bottom PCB legs. Next, the aerogel is aligned by the PCB legs and gently placed by applying 5 N force over the PCB and left for 24 hours to be cured.

The aerogel was picked by flip-chip bonder and Stycast 1266 epoxy was applied on a copper plate. Next, the aerogel is aligned by the copper plate and gently placed by applying 5 N force. Then, a very small amount of super glue was applied on the corners of aerogel to fix it on the copper plate. Here the bonded aerogel and PCB was bonded to copper plate. Finally, some pieces of silicon wafer were glued to copper plate and tail of bottom PCB to fix its position and create a same level of height (see **Figure 22**).

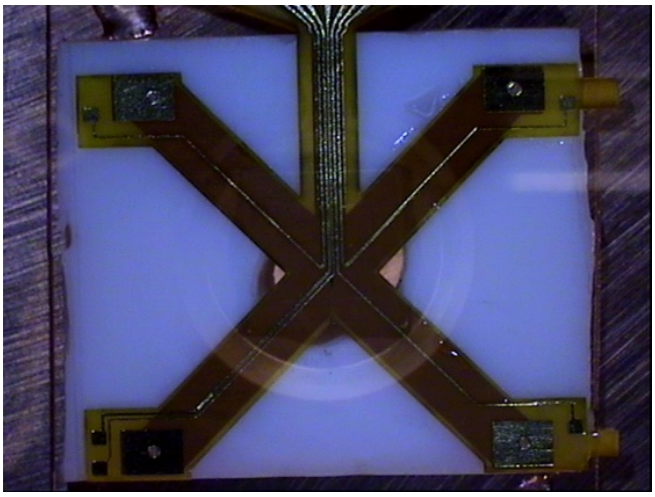
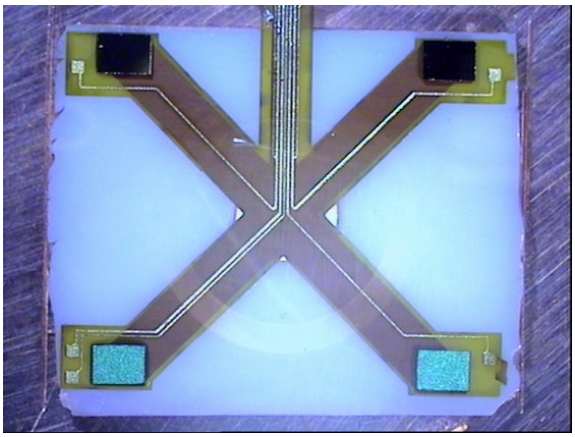


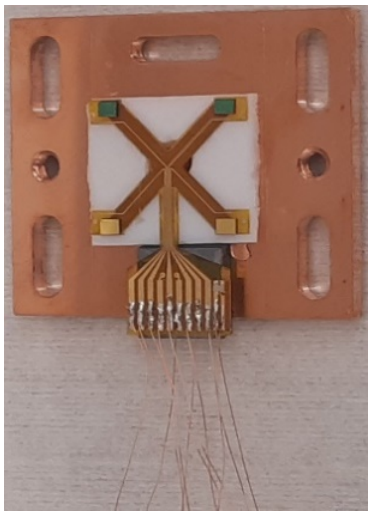
Figure 22. Shows bonded bottom PCB to aerogel and copper plate.

To make connections between backside of the photodiode (negative side) to the bottom PCB via wire bonding, 4 diced pieces of silicon (2x1 mm) which had Au layer were selected and bonded by dispensing Stycast 1266 epoxy over 4 rectangular shape bottom PCB connection pads.

Two pieces of the diced wafer were bonded on Au side and the other two pieces were bonded on silicon side and left to be cured for 24 hours.



(a)



(b)

Figure 23: (a) Shows 4 diced pieces of wafer which had Au layer bonded on bottom PCB. (b) Shows completed bottom part of DMD.

The Epo-Tek EJ2189 LV silver conductive epoxy was dispensed over the two Au side and the other two pieces with silicon side. The photodiode with bonded top PCB and the resistor chip was picked by flip-chip bonder and placed by 5 N force over bottom PCB with epoxy squeezed area and left to be cured for 24 hours.

3.6.7 Wire bonding of the Photodiode to Bottom PCB

The photodiode pads were wire bonded via gold wires to the bottom PCB using Delvotec 5610 Wire Bonder (Ball). Capillary with thickness of 17.5 µm was used to connect the photodiode pads to the bottom PCB.

3.7 Characterization

3.7.1 Adhesion Test of Coated Thin Films

Adhesion test was done to check adhesion of deposited thin films on the wafer. To check adhesion quality, the tape test was done by sticking a piece of Kapton tape on both coated wafers. Next, the tape was peeled away [28].

3.7.2 Resistance Measurements of Tiw Resistors

The resistance measurements were performed using a Lakeshore Cryogenic Probe station equipped to KEITHLEY 2100 digital multimeter. The selected resistor chips for resistance measurements are marked with corresponding numbers in Figure 24.

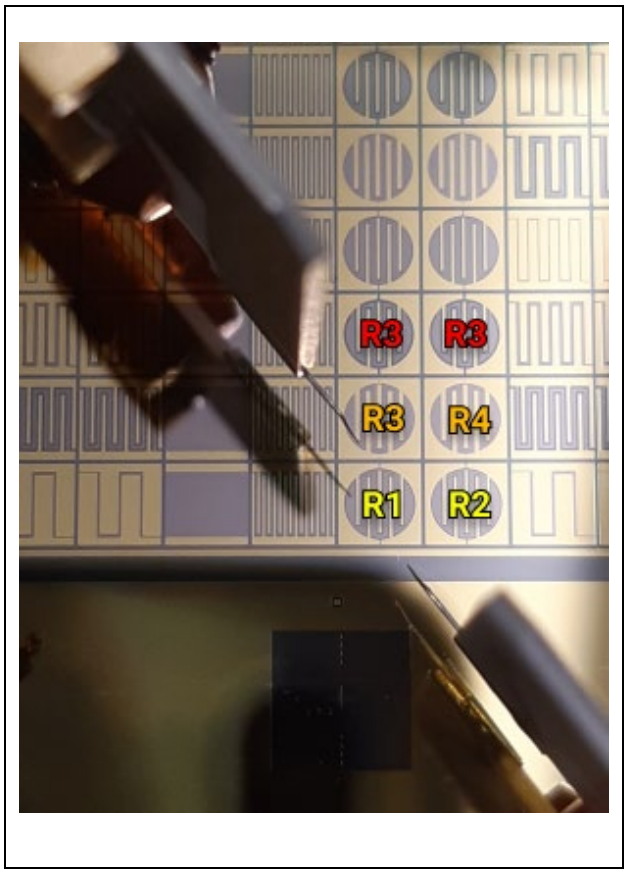
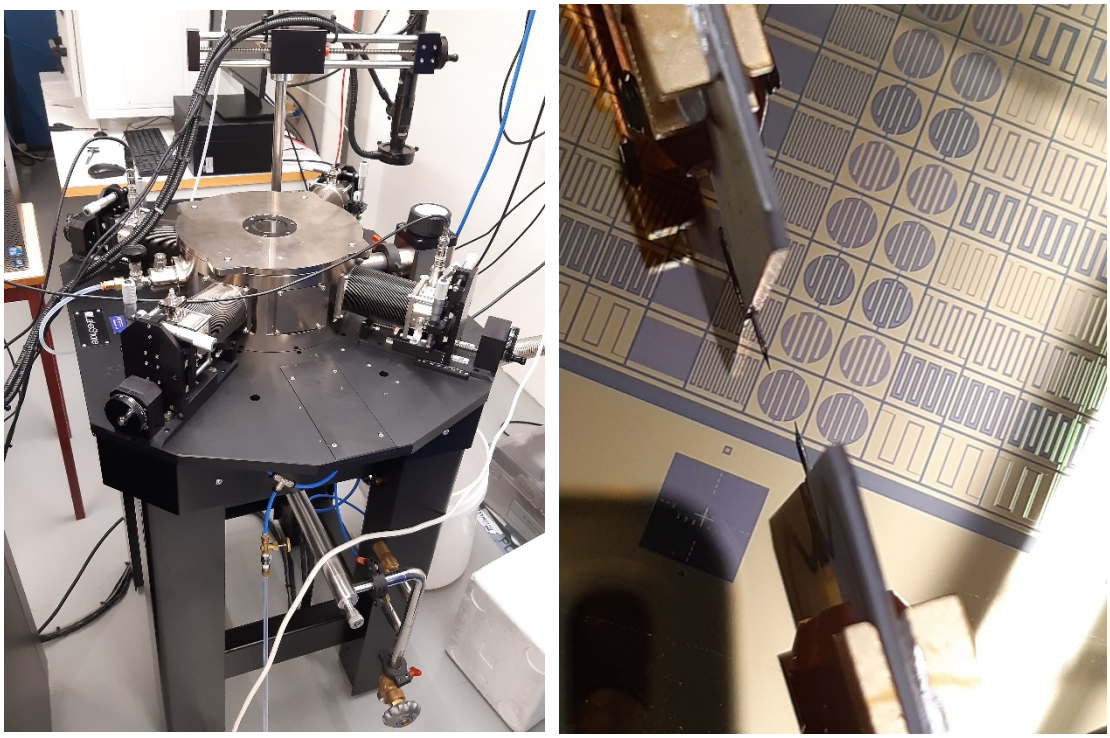


Figure 24. Resistor chips were selected to measure the resistance values.

Two of the probe station's needles were touched the resistor pads to read resistance value in kΩ.



(a) (b)

Figure 25: (a) Shows Lakeshore cryogenic probe station that was used to measure resistance value of resistors. (b) Shows a fixed diced wafer and device needles touching the gold pads of resistor chip during measurements of resistance value.

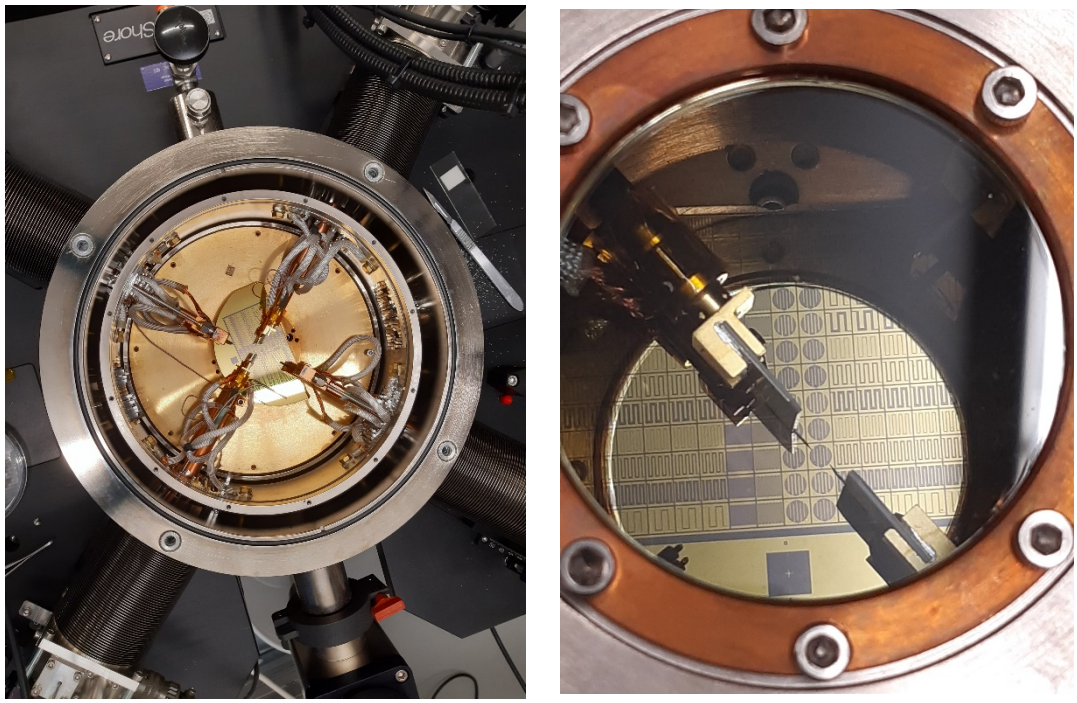
3.7.3 Temperature Coefficient of Resistance Measurement

The TCR measurements were performed with the same equipment was used as in resistance measurement step . Two of the probe station's needles were touched the resistor pads in to read resistance value in 3 steps. First the resistance value was read at 296 °K. Next, sample stage of device was heated to 320 °K to read the resistance value change. Finally, the sample stage was heated to 340 °K and the resistance value was read. The temperature coefficient of resistance (TCR) which denotes as α, is estimated using following formula:

$$\alpha = \frac{R_2 - R_1}{R_1(T_2 - T_1)} * 10^6 \qquad (3.2)$$

Where TCR is in parts per million per degree Kelvin (ppm/°K) or part per million degree Celsius (ppm/°C), R1 is resistance value at room Temperature in ohms, R2 is resistance

value at operating temperature in ohms, T1 is room temperature, and T2 is operating temperature.



(a) (b)

Figure 26: (a) shows the Lakeshore cryogenic probe station used to measure resistance value of resistors during heating. (b) Shows fixed diced wafer on stage and device needles touching the gold pads of resistor chip during measurements of resistance value.

4 Results

The results, characterization, and findings of the manufactured TiW resistors are presented in this section.

Characterisation of SiO_2 Wafer after Sputtering Deposition of TiW and Au Films

Figure 27 shows deposited SiO_2 wafer right after finishing the sputtering process of TiW and Au films.

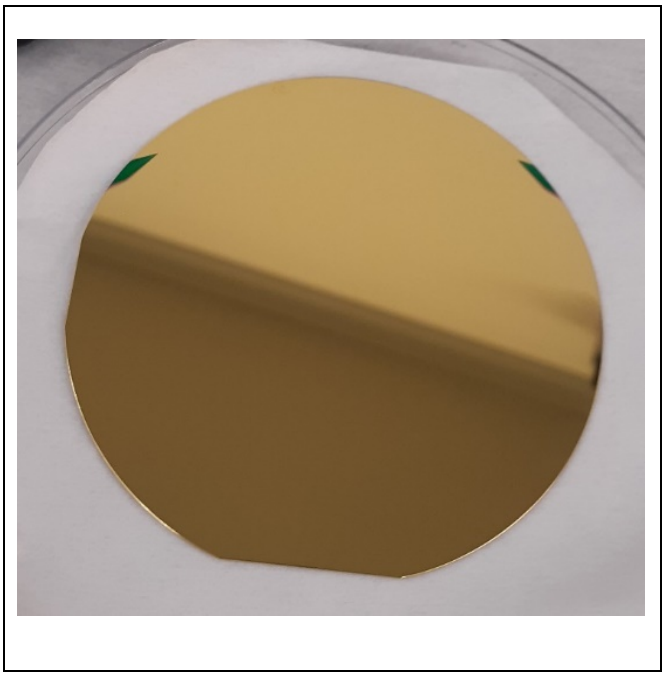
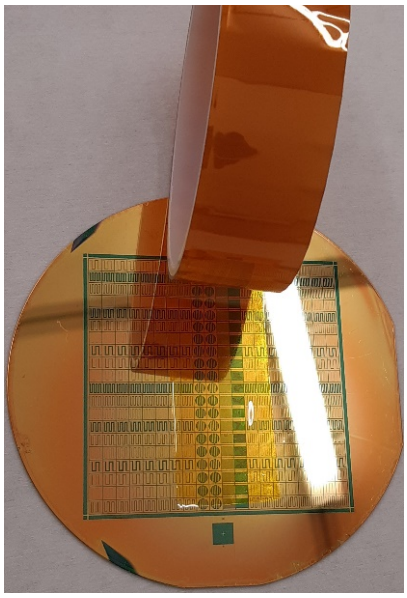
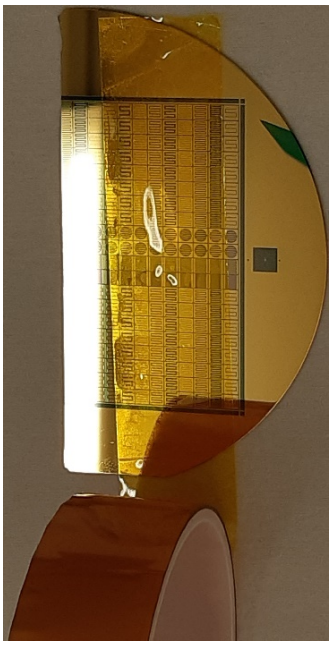
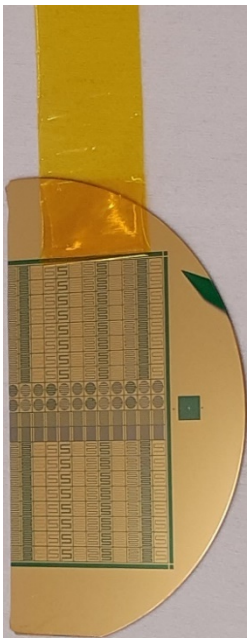


Figure 27. Sputtering deposited SiO_2 wafer by TiW and Au targets.

4.1.1 Adhesion Test Result

The scotch tape test results of wafer 1 and wafer 2 illustrate in **Table VII** respectively.

Table VII. Adhesion test of deposited wafers using scotch tape test.

Sticking the Kapton tape on wafer 1	Peeling the Kapton tape off from wafer 1
	
Sticking the Kapton tape on wafer 2	Peeling the Kapton tape off from wafer 2
	

4.1.2 Wafer after Etching of Au and TiW Layer

The resistors gold pads on wafer 1 developed is shown on **Figure 28.** However, TiW layer (resistors lines) etched away during etching procedure (see **Figure 29**).

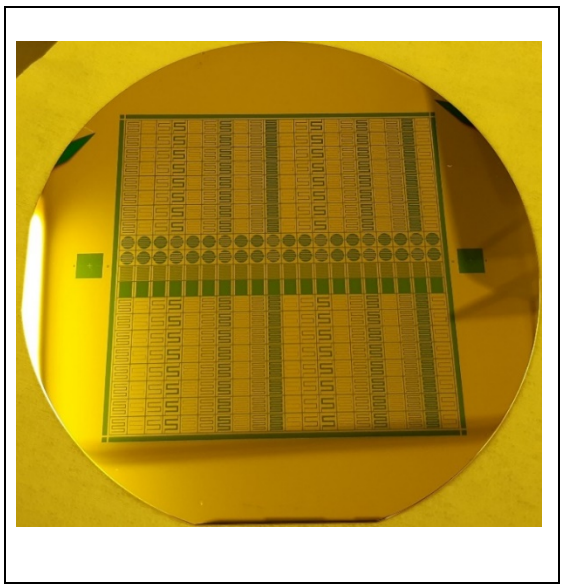


Figure 28. Au layer (resistors gold pads) on wafer 1 was developed after etching process.

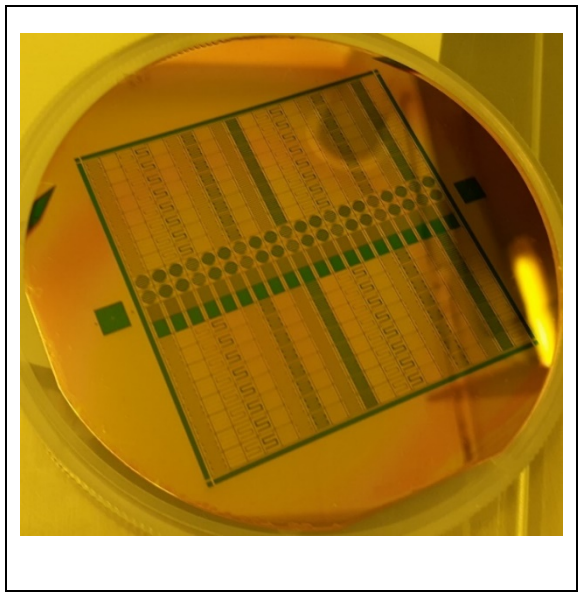


Figure 29. TiW layer (resistor lines layer) on wafer 1 etched away during etching process.

The deposited TiW resistors successfully developed on wafer 2 show on **Figure 30**.

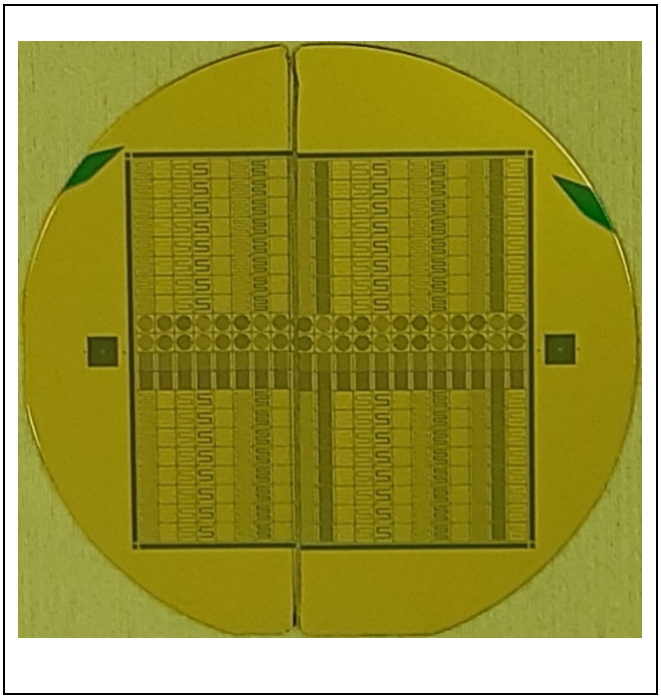


Figure 30. Fabricated resistors on wafer 2 that both TiW and Au masks patterns successfully transferred.

4.1.3 Mesured Thicknesses

4.1.3.1 Au and Photoresist Thickness after Soft-Bake and Hard-Bake

The graphs illustrate thicknesses of photoresist on wafer 1 and wafer 2 which are showed in **Figure 31** and **Figure 32**.

The overall thickness measurement results for photoresist after soft-bake, photoresist after hard-bake, and Au is summarized in **Table VIII**.

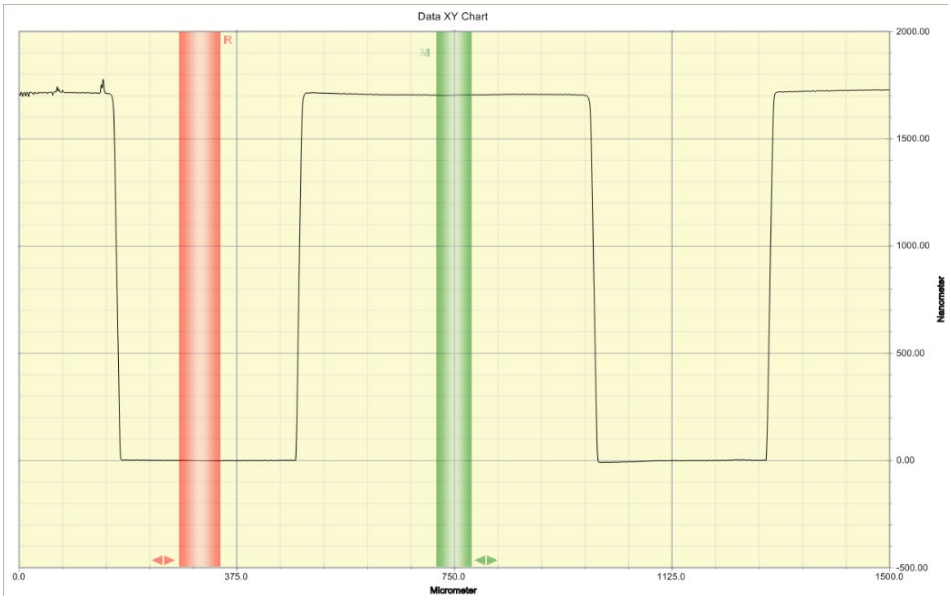


Figure 31. Thickness of photoresist on wafer 1 after soft baking.

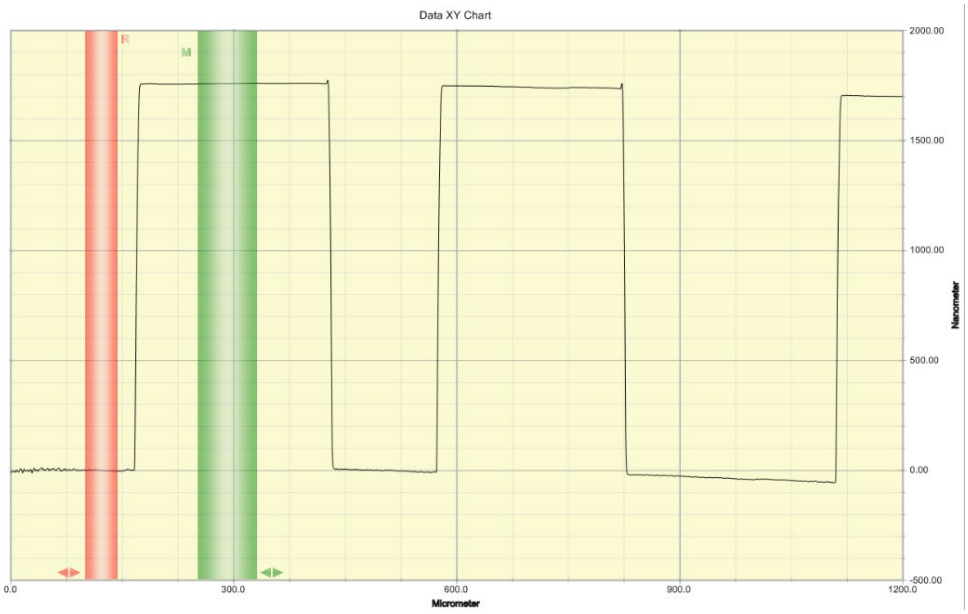


Figure 32. Thickness of photoresist on wafer 2 after soft baking.

Table VIII. Summarize of thickness measurements for Au and photoresist after soft-bake and hard-bake.

Thickness of photoresist on wafer 1 after soft baking	1703 nm
Thickness of photoresist on wafer 2 after soft baking	1759 nm
Thickness of photoresist on wafer 1 after 1 minute hard baking	1724 nm
Thickness of photoresist on wafer 2 after 1 minute hard baking	1793 nm
Thickness of photoresist + Au on Wafer 1	2142 nm
Thickness of photoresist + Au on Wafer 2	2215 nm
Thickness of Au on Wafer 1	422 nm
Thickness of Au on Wafer 2	423 nm 455 nm 449 nm
Thickness of photoresist on wafer 1 after soft baking (Mask 2)	1931 nm
Thickness of photoresist on wafer 2 after soft baking (Mask 2)	1747 nm
Thickness of photoresist on wafer 1 after 1 minute hard baking (Mask 2)	2241 nm
Thickness of photoresist on wafer 2 after 3 minutes hard baking (Mask 2)	1851 nm

4.1.3.2 TiW Layer (Resistors Lines)

The thickness of TiW on wafer 2 was measured in different location from middle of wafer to bottom of wafer. **Figure 33** shows average thickness measurement on middle of wafer, whereas **Figure 35** shows average thickness measurement on bottom of wafer. **Figure 33** and **Figure 35** show point thickness measurement on middle and bottom location of wafer 2 from left to right respectively.

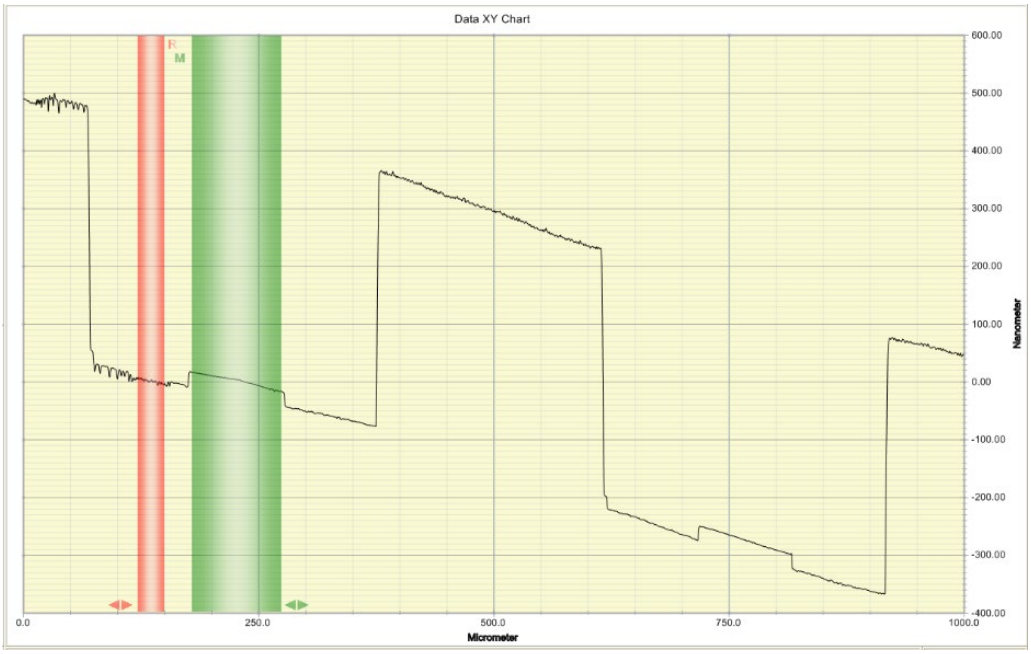


Figure 33. Shows average thickness measurement of TiW on middle of wafer 2.

Analytical Results					
Function	R Pos	R Width	M Pos	M Width	Result
ASH	133.9 um	1.0 um	235....	1.0 um	0.00 nm
ASH	149.1 um	19.1 um	235....	1.0 um	0.21 nm
ASH	149.1 um	19.1 um	215....	26.9 um	3.04 nm
ASH	149.1 um	19.1 um	198....	26.9 um	7.84 nm
ASH	149.1 um	19.1 um	185....	26.9 um	11.48 nm
ASH	149.1 um	19.1 um	241....	26.9 um	-8.49 nm
ASH	149.1 um	19.1 um	216....	26.9 um	2.50 nm
ASH	149.1 um	19.1 um	248....	26.9 um	-11.65 nm
ASH	149.1 um	19.1 um	180....	26.9 um	12.75 nm
ASH	149.1 um	19.1 um	215....	0.1 um	6.91 nm
ASH	149.1 um	19.1 um	233....	0.1 um	1.44 nm
ASH	149.1 um	19.1 um	258....	0.1 um	-10.57 nm
ASH	149.1 um	19.1 um	207....	0.1 um	9.38 nm
ASH	149.1 um	19.1 um	190....	0.1 um	13.96 nm
ASH	150.8 um	28.6 um	184....	78.7 um	2.48 nm
ASH	150.8 um	28.6 um	179....	95.0 um	0.73 nm
ASH	150.8 um	28.6 um	179....	95.0 um	0.73 nm

Figure 34. shows point measured thicknesses of TiW on middle part of wafer from left to right.

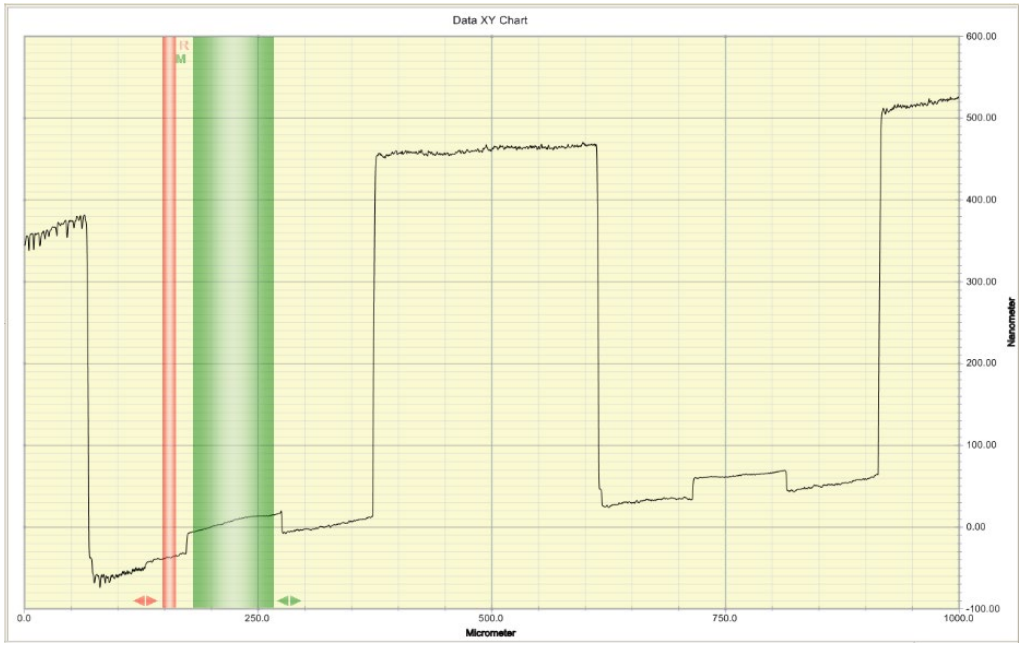


Figure 35. shows average thickness measurement of TiW on bottom of wafer 2.

Analytical Results

Function	R Pos	R Width	M Pos	M Width	Result
ASH	153.6 um	1.0 um	223....	1.0 um	45.35 nm
ASH	153.6 um	1.0 um	236....	1.0 um	49.13 nm
ASH	153.6 um	1.0 um	248....	1.0 um	50.63 nm
ASH	163.0 um	14.8 um	180....	87.0 um	43.58 nm
ASH	163.0 um	14.8 um	183....	15.6 um	34.05 nm
ASH	163.0 um	14.8 um	217....	15.6 um	45.39 nm
ASH	163.0 um	14.8 um	244....	15.6 um	50.39 nm
ASH	163.0 um	14.8 um	254....	15.6 um	51.17 nm

Figure 36. shows point measured thicknesses of TiW on bottom part of wafer from left to right.

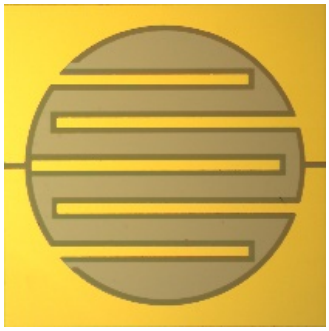
4.2 Characterization of TiW Resistors

The fabricated resistors by photolithography show in following, with the measured and simulated resistance values.

4.2.1 Fabricated Resistors images with Measured Resistance values

The COMSOL simulated and measured resistance values for three structures with different line spaces are shown in **Table IX**.

Table IX. Fabricated resistors images with measured and simulated resistance details.

Fabricated resistor with 20 µm line spaces	Fabricated resistor with 50 µm line spaces	Fabricated resistor with 100 µm line spaces
		
COMSOL simulated resistance value for 50 nm TiW thickness: 1961.6 KΩ	COMSOL simulated resistance value for 50 nm TiW thickness: 2046.2 KΩ	COMSOL simulated resistance value for 50 nm TiW thickness: 3792.4 KΩ
Measured resistance value: **R1**: 2.149 KΩ, **R2**: 1.811 KΩ	Measured resistance value: **R3**: 1.4882 KΩ, **R4**: 1.4036 KΩ	Measured resistance value: **R5**: 11.233 KΩ, **R6**: 10.321 KΩ

The resistance value of resistors is varied within the wafer location which resistance is reduced for the chips closer to the edge of the wafer. Based on the measured resistance value of resistor chips in **Table IX** , two resistor chips with 20 and 50 µm line spaces between resistor lines and pads are fairly similar to the COMSOL simulated value. However, for the chips with 100 µm line spaces it is significantly higher.

4.2.2 Temperature Coefficient of Resistance

Figure 37 shows measured resistance value of resistor chips by heating from 296 °K to 320 °K and finally 340 °K. The results show that, the resistance value of the resistor chips, were dropping in each heating cycle to 200 ohms. The estimated TCR are shown on **Table X**.

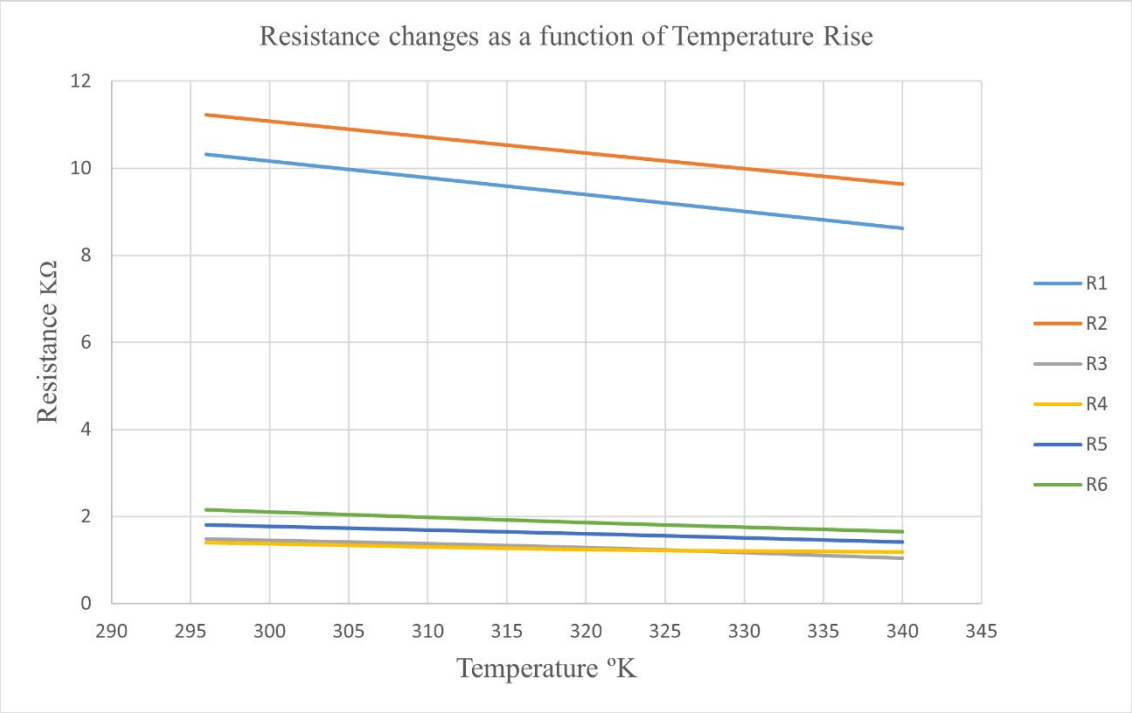


Figure 37. Resistance changes during measurement of TCR.

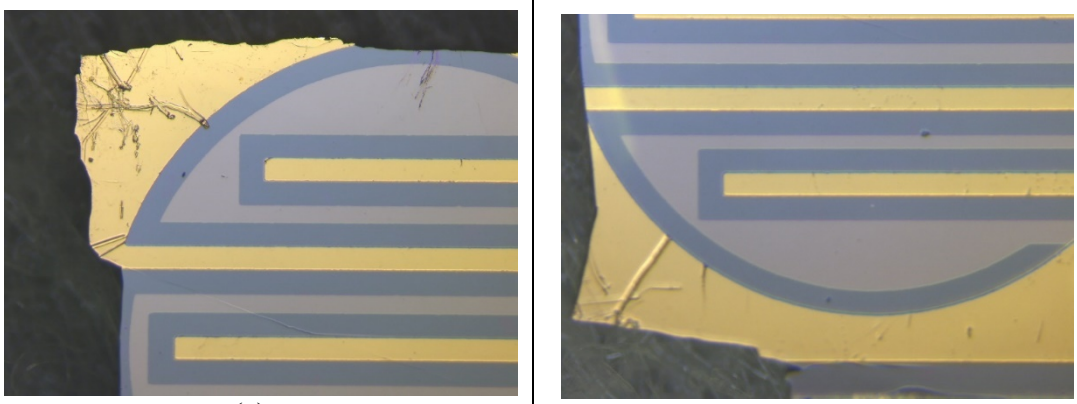
Table X. Estimated TCR values for 6 resistor chips.

Resistor Number	Resistance at room Temperature (R1)	Room Temperature (T1)	Resistance at Operating Temperature (R2)	Operating Temperature (T2)	TCR
1	10.321 kΩ	296 °K	8.6252 kΩ	340 °K	-3734 ppm/°K
2	11.233 kΩ	296 °K	9.6387 kΩ	340 °K	-3225 ppm/°K
3	1.4882 kΩ	296 °K	1.0412 kΩ	340 °K	-6826 ppm/°K
4	1.4036 kΩ	296 °K	1.1845 kΩ	340 °K	-3547 ppm/°K
5	1.811 kΩ	296 °K	1.4178 kΩ	340 °K	-4934 ppm/°K
6	2.149 kΩ	296 °K	1.652 kΩ	340 °K	-5256 ppm/°K

The estimated TCR value for TiW shows a negative value which is not usual for metals that typically have a positive value. TCR value of TiW alloy was experimentally measured by [29] shows a negative value which confirmed by this thesis work calculated value. However, the TCR estimated value in this work for 90% titanium and 10% tungsten is approximately -250 ppm/°K. Whereas the average estimated value in this thesis works is -4587 ppm/°K.

4.2.3 Thickness Measurements of Thinned Resistor Chip

The maximum achieved thickness by grinding machine on thinning experiment was down to 36 µm. Despite being gentle with the thinned chip after separation from polishing fixture, during cleaning procedure of the chip in ultrasonic cleaning bath which was immersed into acetone, the chip was broken. The broken resistor top and bottom sides images illustrate on **Figure 38.**



(a) (b)

Figure 38: (a) Shows damaged resistor chip top side during thinning procedure. (b) Shows bottom side of the damaged resistor chip.

Figure 39 shows thickness of a 39 kΩ resistor which thinned successfully to 53 µm. **Figure 40** shows the broken resistor chip that thinned to 36 µm.

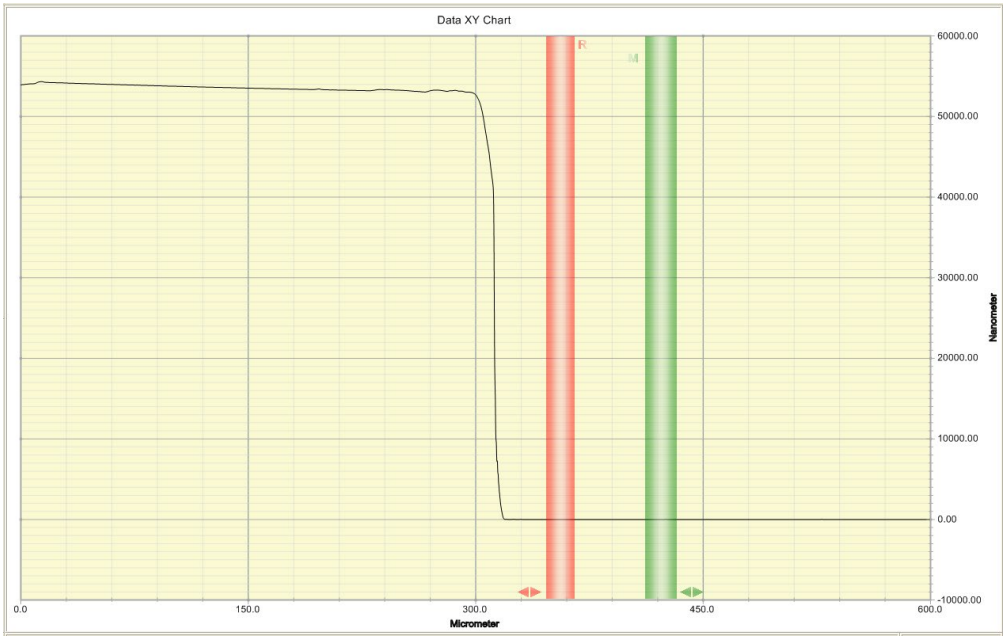


Figure 39. Thickness of thinned 39 kΩ resistor chip.

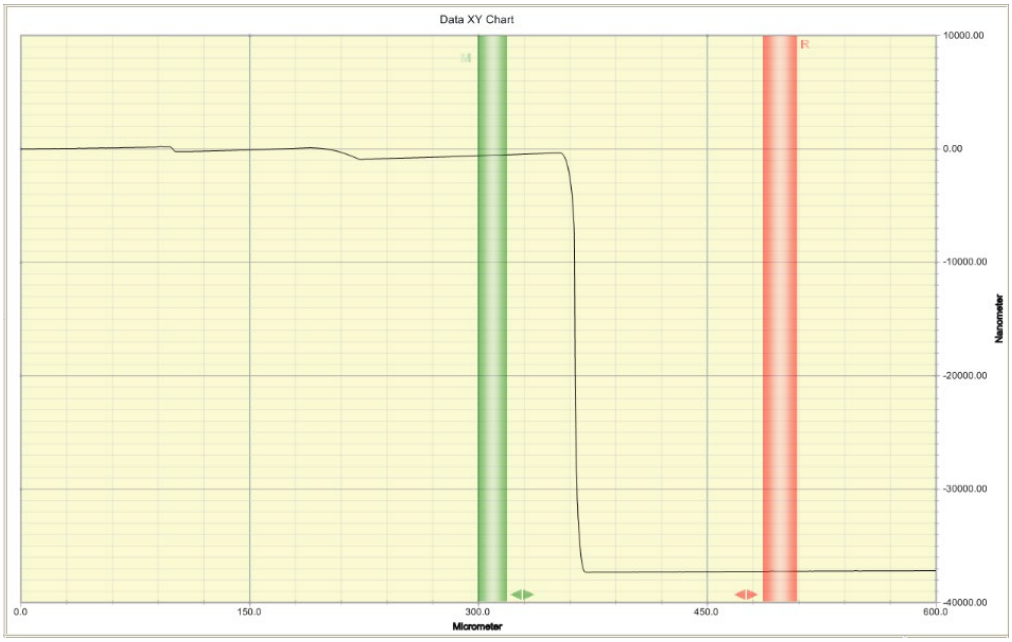


Figure 40. Thickness of broken thinned resistor chip.

4.3 Wire Bonding

4.3.1 Wire Bonding of Resistor Chip to Top PCB

Figure 41 shows wire bonding which was performed to make connections between two resistor pads and top PCB.

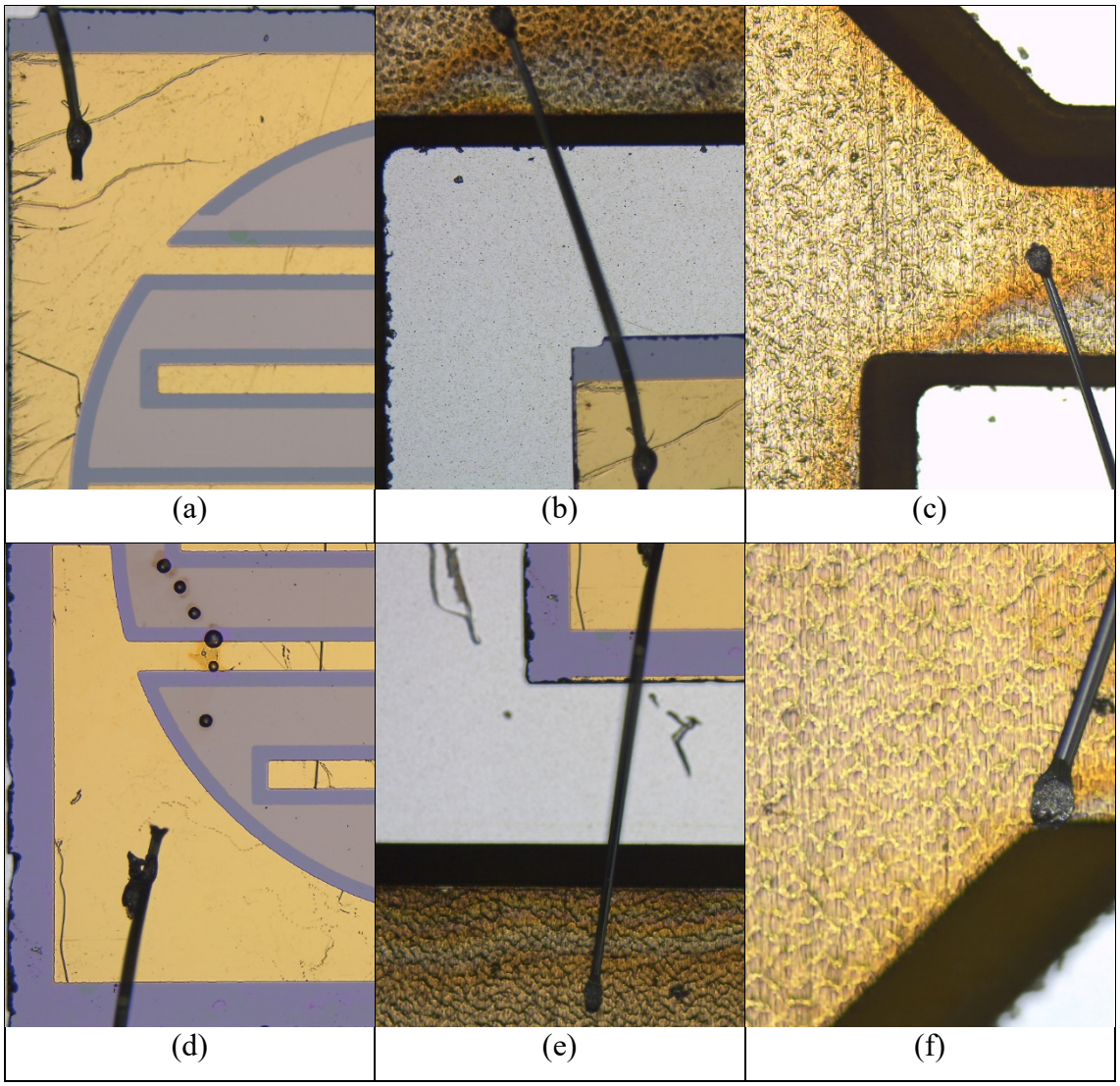
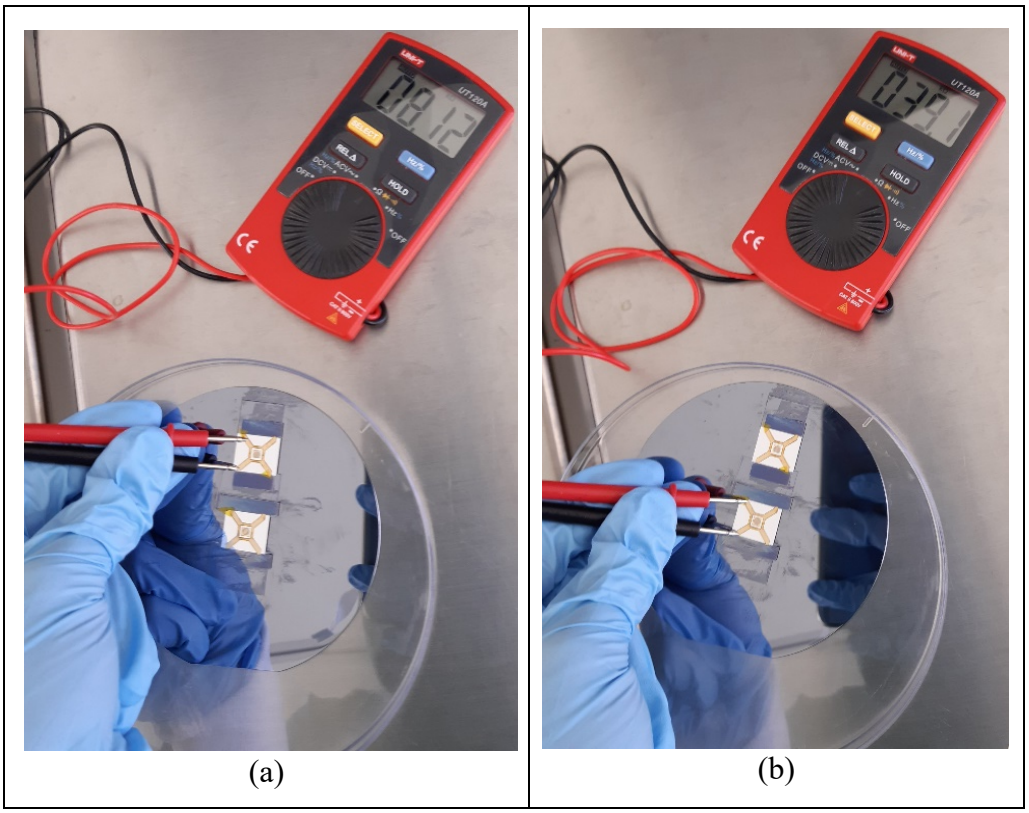


Figure 41: (a) Shows top resistor pad wire bonded using wedge bonding. (b) Shows top resistor pad and PCB wire bonding connection. (c) Show wire bonding to top leg of PCB. (d) Shows bottom resistor pad wire bonded using wedge bonding. (b) Shows bottom resistor pad and PCB wire bonding connection. (c) Show wire bonding to bottom leg of PCB.

4.3.2 Conductivity and Resistance Test after Wire Bonding of Resistor to the Top PCB

After performing wire bonding of resistor to the top PCB, the conductivity test was performed to check the connection between resistor pads to the PCB as well as to check the resistance to make sure the thinned resistor chip is not damaged during bonding procedure (see **Figure 42**).



(a) (b)

Figure 42:. (a) Shows conductivity and resistance check of sample 1 after wire bonding. (b) The same check for sample 2.

4.3.3 Wire Bonding of the Photodiode to Bottom PCB

Figure 43 shows the photodiode positive and negative contact wire bonding connections to the bottom PCB.

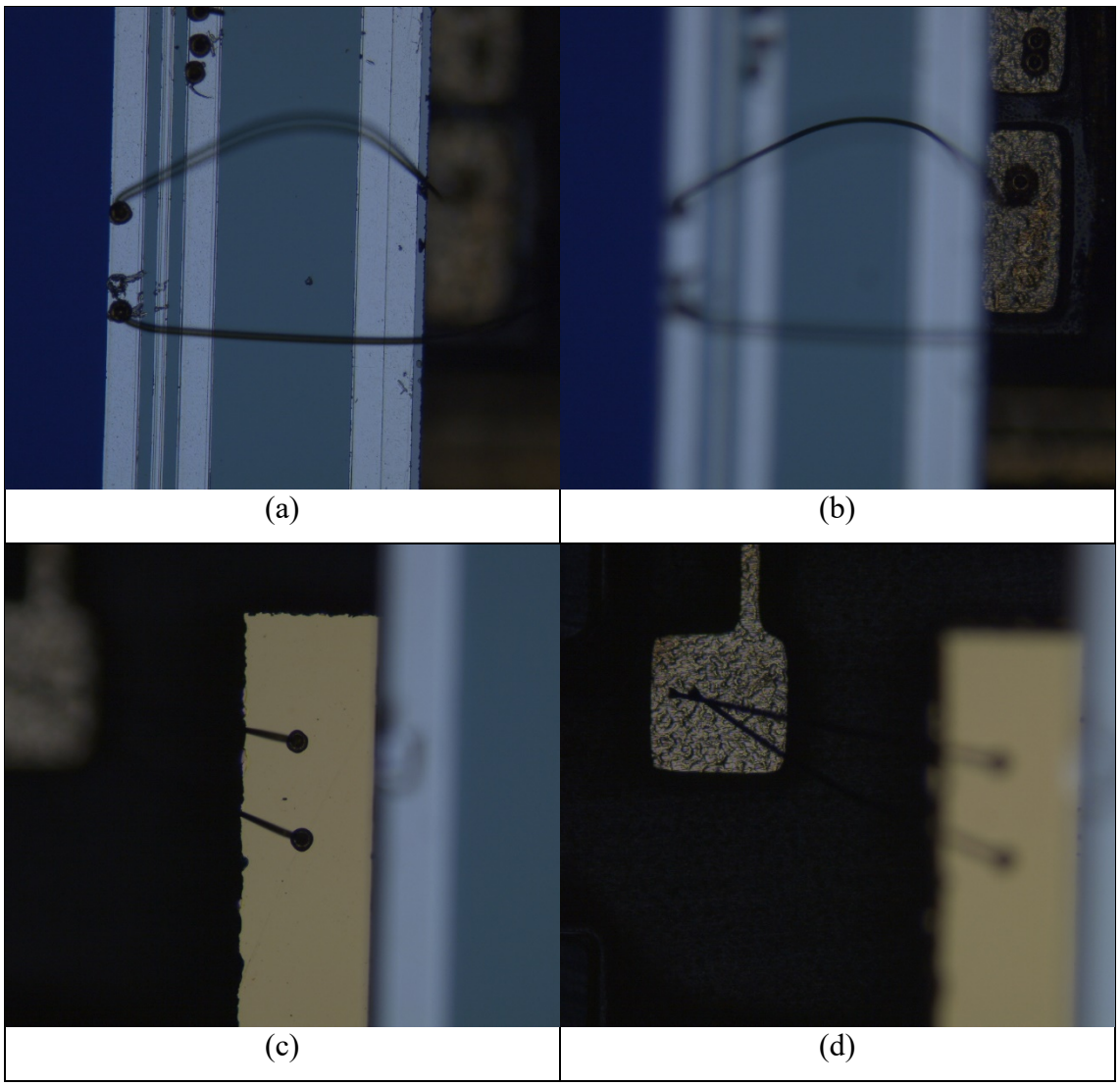


Figure 43: (a) Shows the photodiode positive contact wire bonded. (b) Shows wire bonding connection of positive contact to the bottom PCB. (a) Shows the photodiode negative contact wire bonded. (b) Shows wire bonding connection of negative contact to the bottom PCB.

4.4 Thermal Simulations

The result of thermal simulation for finding non-equivalence between optical and electrical heating modes as a function of epoxy thickness, resistor chip thickness, and TiW emissivity are shown on figures below.

Figure 44 Shows the simulated non-equivalence between optical heating and electrical that done by increasing epoxy thickness from 5µm to 100 µm. As it can be seen, the non-equivalence value will be increased.

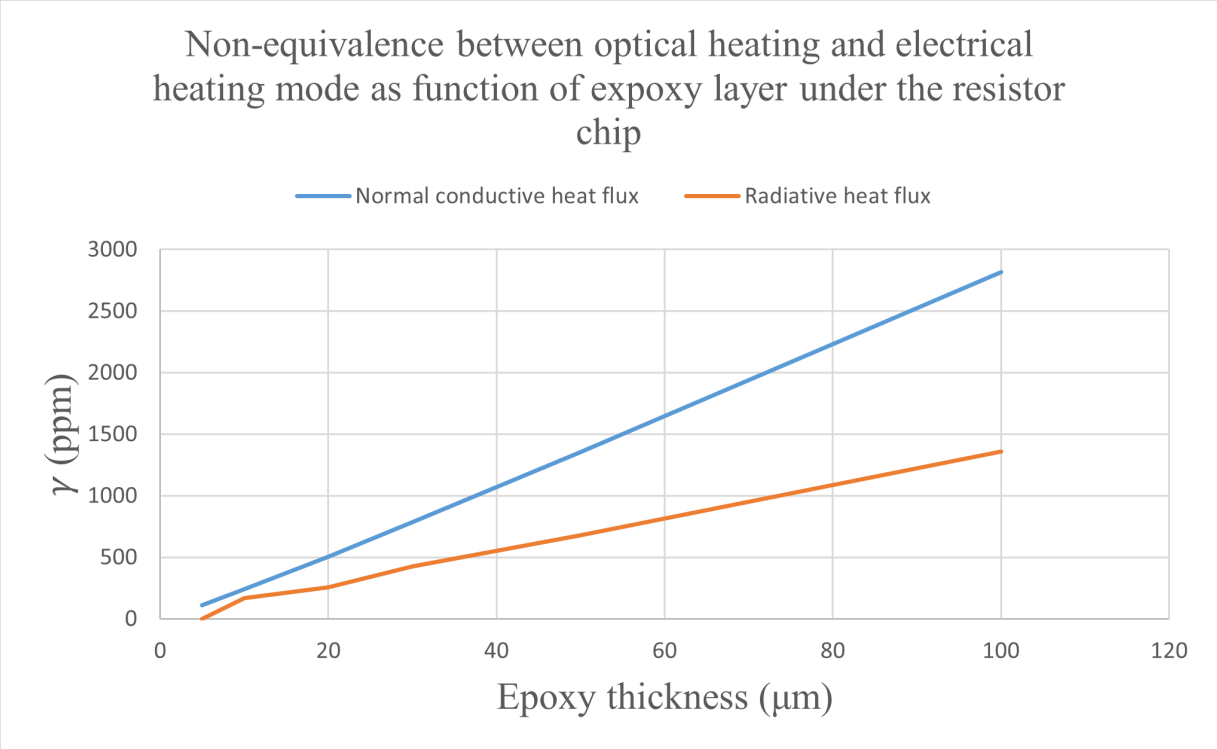


Figure 44. Non-equivalence between optical heating and electrical heating mode as function of epoxy layer under the resistor chip.

Figure 45 Shows the simulated non-equivalence between optical heating and electrical that done by increasing the emissivity of TiW from 0.1 to 1. **Figure 46** Shows the simulated non-equivalence between optical heating and electrical that done by increasing the thickness of resistor chip from 20 µm to 100 µm. These results were not expected as the non-equivalence values as function of emissivity and resistor chip thickness have around 240 ppm and 300 ppm differences at the beginning and increasing to 450 ppm and 350 ppm respectively. However, it is likely that the reason for this is the epoxy cylinder diameter which leads to generation of a different temperature gradient than optical beam.

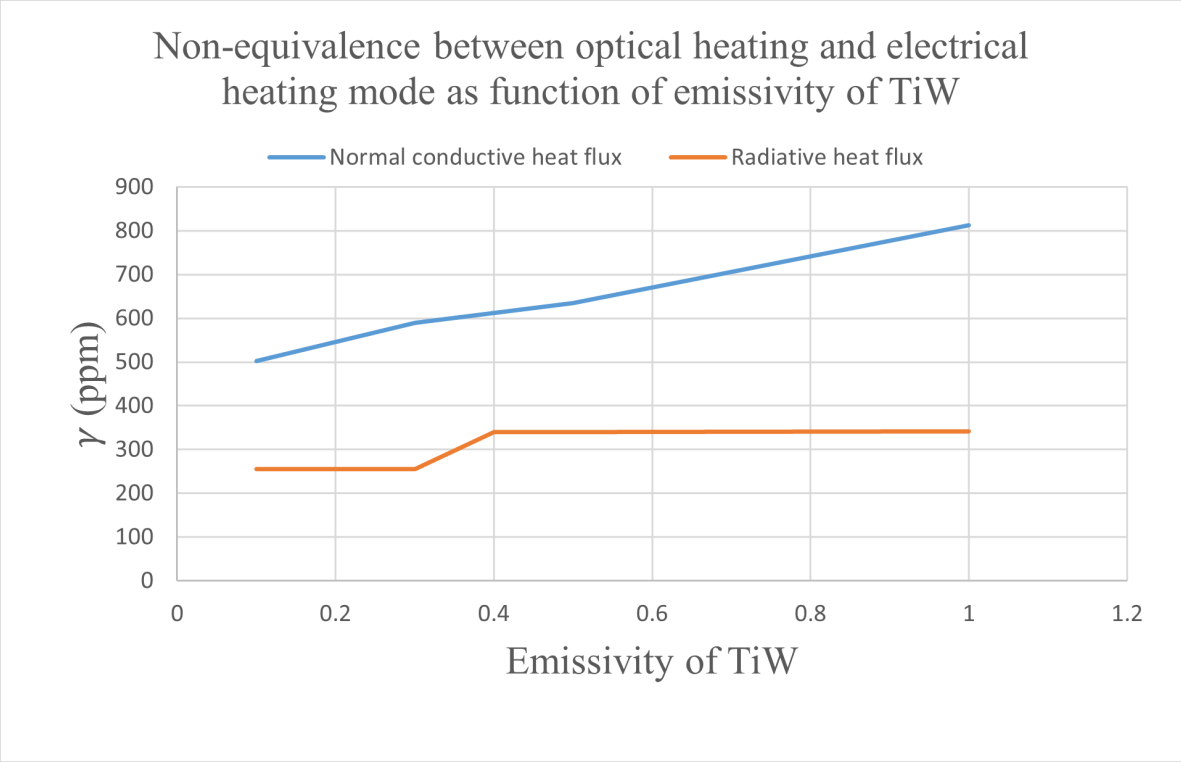


Figure 45. Non-equivalence between optical heating and electrical heating mode as function of emissivity of TiW.

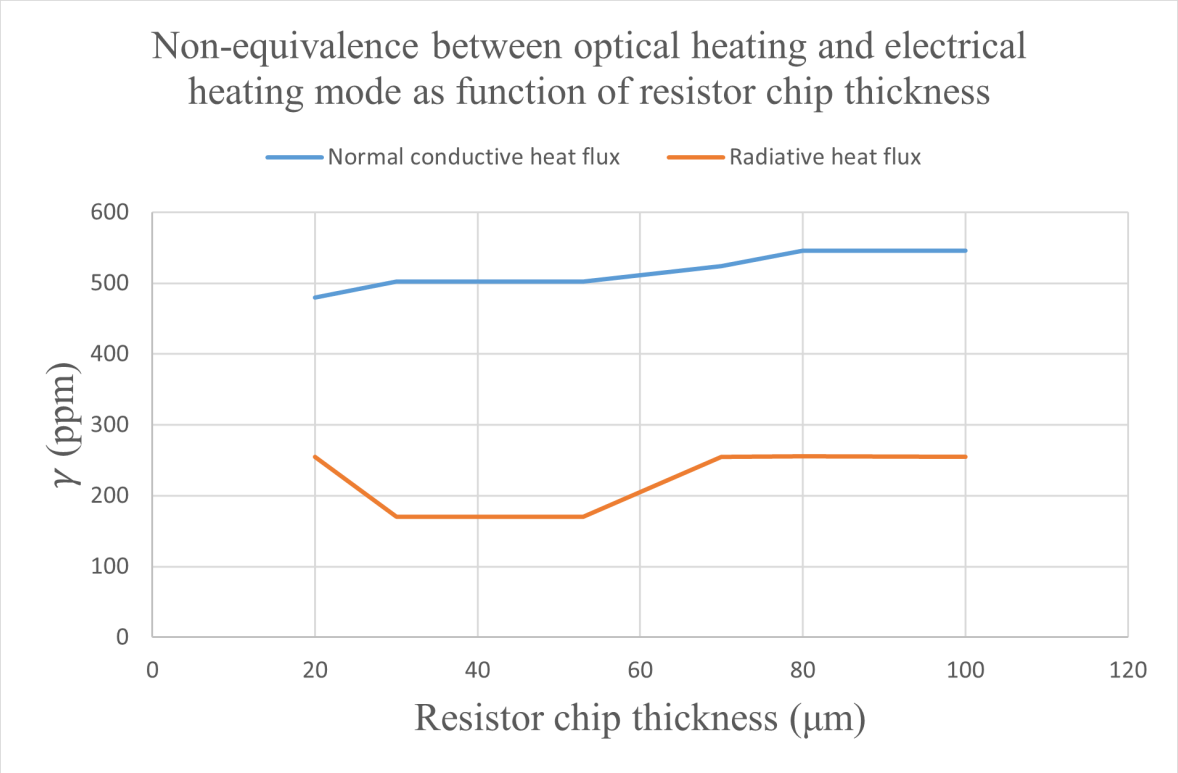
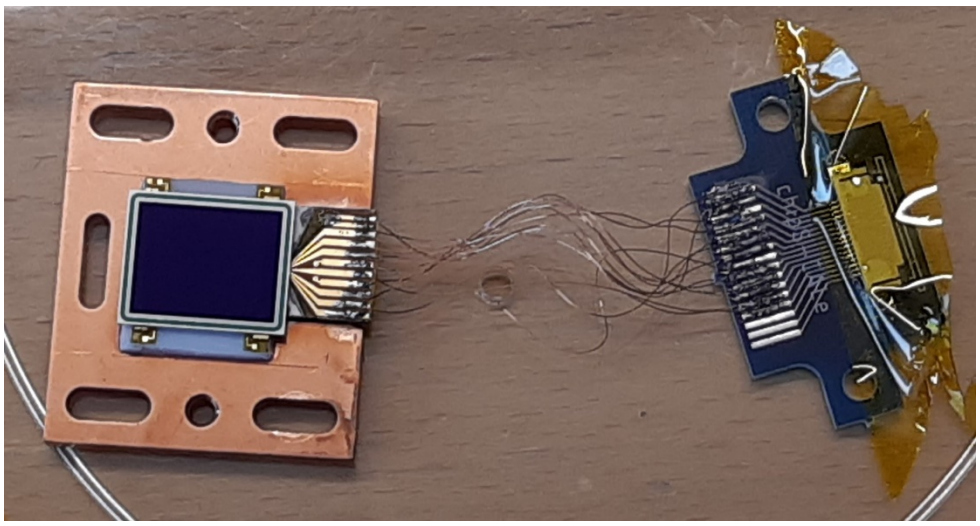


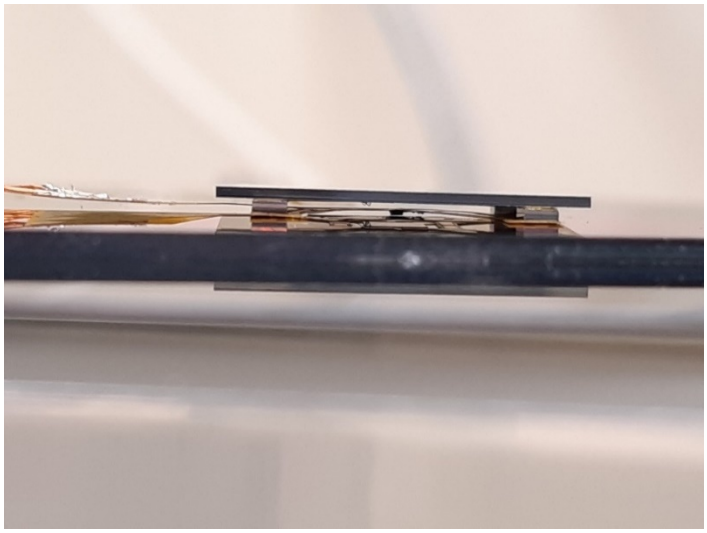
Figure 46. Non-equivalence between optical heating and electrical heating mode as function of resistor chip thickness.

4.5 Dual Mode Detector Module

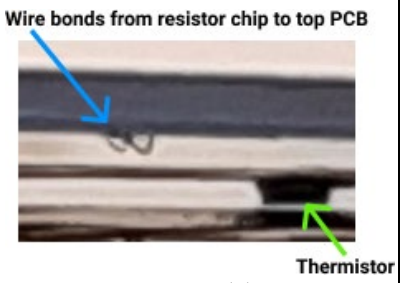
The completed DMD module images show on **Figure 47**, where a mix of wire bonding techniques and silver conductive epoxy adhesive were used to make the connection between top and bottom PCB to the resistor and the photodiode.



(a)



(b)



(c)

Figure 47: (a) Shows completed image of DMD module. (b) shows cross-section image of module. (c) illustrates soldered temperature sensor to bottom PCB as well as wire bonding from bonded resistor chip to backside of the photodiode to top PCB.

5 Discussion

The objectives of project have been met. The resistor application in this work is to generate on-chip heat and at the time of starting the project, the commercially available resistor product with gold pads had a resistance value of 1 kΩ. The amount of heat is generated by resistors can be related to power ohm law (2.2). A resistor with higher resistance value can produce more heat. Regarding the packaging of a SMD resistor, the thickness, and the amount of generated heat for such resistor which is much lower compared to the current fabricated ones that ranging from 1 kΩ to 39 kΩ. The acceptable range values agreed was more than 1 kΩ. One benefit of the fabrication of resistor through photolithography is that the possibility of thin the fabricated resistor chip which doesn't have a packaging and makes it more suitable to integrate on backside of the photodiode.

The adhesion results show very good adhesion on both wafers according to **Table VII**. This can be due to sputtering deposition parameters were used as well as wafer cleaning procedure which was done before thin film deposition. During the etching of the TiW film on wafer 1 with 15 nm deposited TiW, the film completely etched away. This was because of thin layer of TiW with small structure that made it hard to see the etching progress while it was immersed into hydrogen peroxide. This probably could be prevented by carefully immerse the wafer in hydrogen peroxide for couple of seconds for instance 5 second and investigate the wafer to see the etching progress step by step.

The two simulated values of resistor chips have fairly similar resistance as measured ones in the experiment. Which indicates the selected bulk resistivity value of TiW, used for COMSOL simulations can be a realistic value. However, there is a resistance variation within the wafer. This could be due to dishing of soft metals (non-uniform thickness) during sputtering or different etching rate during etching process of TiW. The thickness of TiW on wafer 2 was measured by the Dektak 150 profilometer to confirm thickness variations from middle part of wafer shows in **Figure 33** and from bottom of wafer shows in **Figure 35**. It was seen the middle part of the wafer for TiW layer has point thicknesses from 1 to 13 nm, whereas bottom side of wafer has point thicknesses between 34 and 50 nm.

Thermal simulation in COMSOL based on **Figure 44** shows the epoxy thickness has as a significant contribution to non-equivalence. Where the non-equivalence value is increasing by increasing epoxy thickness from 5 μm to 100 μm.
During COMSOL simulation it was observed that the diameter of epoxy cylinder under resistor chip has significant effect on conducting the generate heat. Which by decreasing the radius of epoxy cylinder to less than 1.5 mm, the non-equivalence will increase. It is likely it affects the unexpected results of non-equivalence as a function of emissivity and chip thickness.

The TCR measurements showed a high negative value which confirms the possibility of using the resistor structure as a NTC thermistor. One benefit of this, is the possibly of eliminating the middle temperature sensor and use the bonded resistor chip on backside of the photodiode simultaneously as a heater and a temperature sensor.

The thinning experiment in this thesis demonstrates that if the fabricated wafer thinned by deep reactive ion etching (DRIE) technique, the dicing of resistor chips would be very challenging comparing to grinding technique which was used to thin diced resistor chips individually.

The most challenging problem during the epoxy bonding of resistor chip and top and bottom PCBs was controlling the amount of epoxy which was needed to apply and prevent to squeeze out and spread to unnecessary locations like photodiode surface, as well as bonding pads which makes the wire bonding process on gold pads very hard or impossible. Moreover, the amount of epoxy applied under the PCBs should be enough to fix them on surface. During wire bonding of a test sample, the bonded PCB was pulled after the first wire bond that was made on a contact pad of the PCB.

The wire bonding experiment first was performed by ball bonding technique, initial ball “Flame-Off- Process” was successfully done on resistor gold pads. However, on the PCB pads it was very challenging without a succeed. This can be due to contamination by exceeded epoxy during bonding of top PCB on backside of the photodiode or the PCB surface. Also, as can be seen on **Figure 41** (c) and (f) on the surface of top PCB, there is steps which indicates that is not very flat. Whereas wedge bonding with aluminium wire

was done without this problem to create interconnection between resistor pads and bottom PCB.

The completed DMD module was sent to Justervesenet to be tested and extract the non-equivalence value in a real case scenario. Based on previous study of module in [4] and results achieved so far, it is expected that the module in room temperature, have a non-equivalence bellower than 100 ppm [16].

6 Conclusion

In conclusion, the intended heating resistors fabricated with an acceptable range. From 1 KΩ to 39 KΩ in a 3x3 mm dimension which indicates the selected TiW (90/10%) film was a suitable candidate for fabrication of thin film resistors in a small structure. Thinning procedure showed the possibility of thin the resistor chips down to 53 μm with wire bonding ability. The fabricated resistors were bonded to the backside of the photodiode and successfully assembled in the dual mode detector module (DMD). The completed DMD module was sent to Justervesenet to perform measurements.

The TCR measurements of resistors, showed a high negative value which is beneficial for use as a heater, that leads to provide the power for a longer time compares to the ones with lower TCR [30]. Moreover, a high negative value makes it possible to use the resistor structure as a NTC thermistor. The advantage of this, is the possibly of using the resistor chip as a heater and a temperature sensor at the same time in DMD module.

The performed COMSOL thermal simulation indicates that the thickness and covered area of epoxy layer under resistor chip has enormous effect on heating profile.

7 Future work

- Measurement TiW layer emissivity on resistor chip.
- Estimation of TCR in cryogenic temperatures.
- Find a solution to integrate the resistor chip inside the photodiode structure.
- Assess the possibility of design vias interconnection or flip-chip interconnection between the resistor chip and the PCBs.

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Appendix

7.1 Dimension Measurements

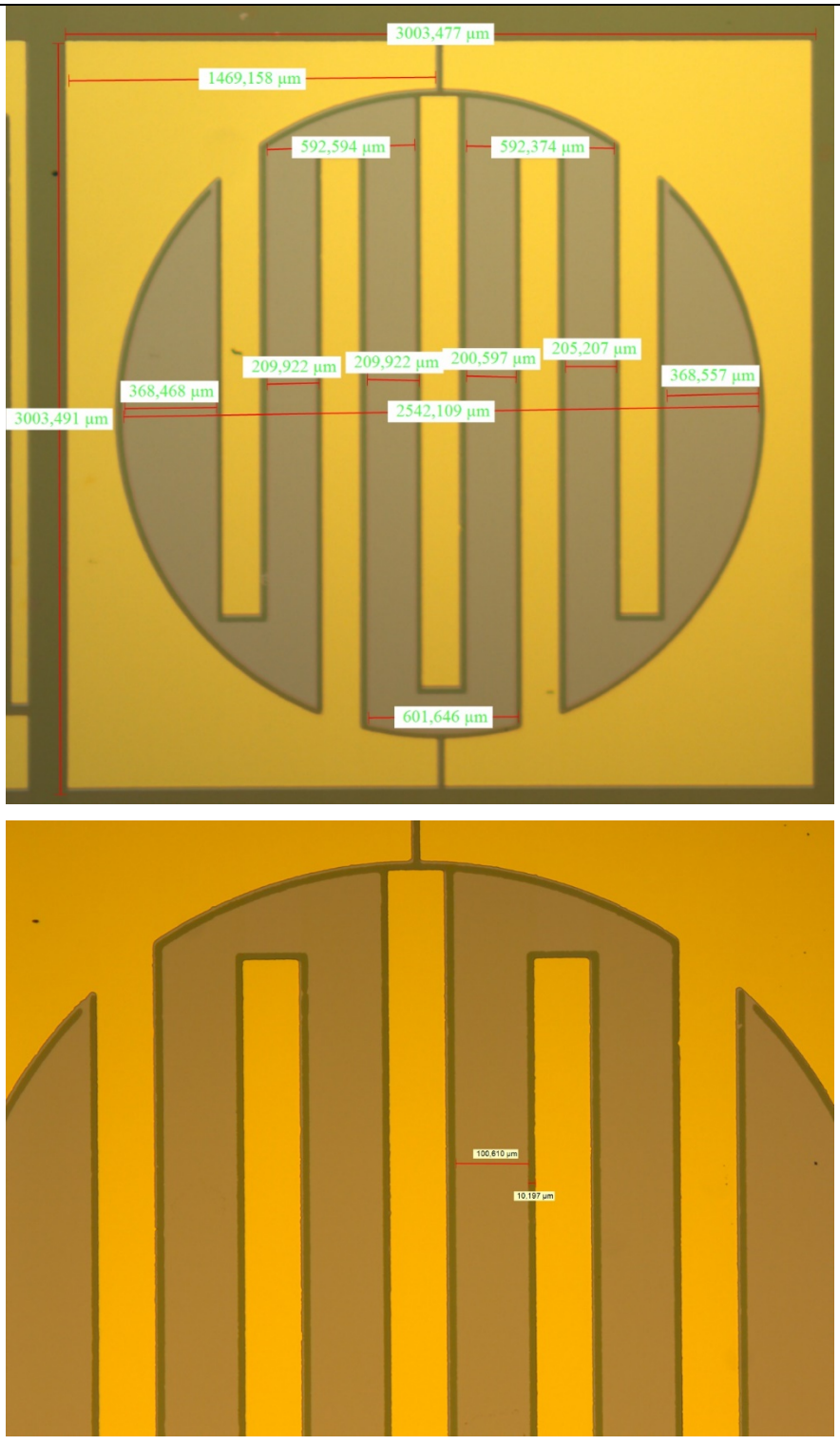

Figure 48 Dimension measurements of fabricated resistor with 20 µm line spaces using an optical microscope.

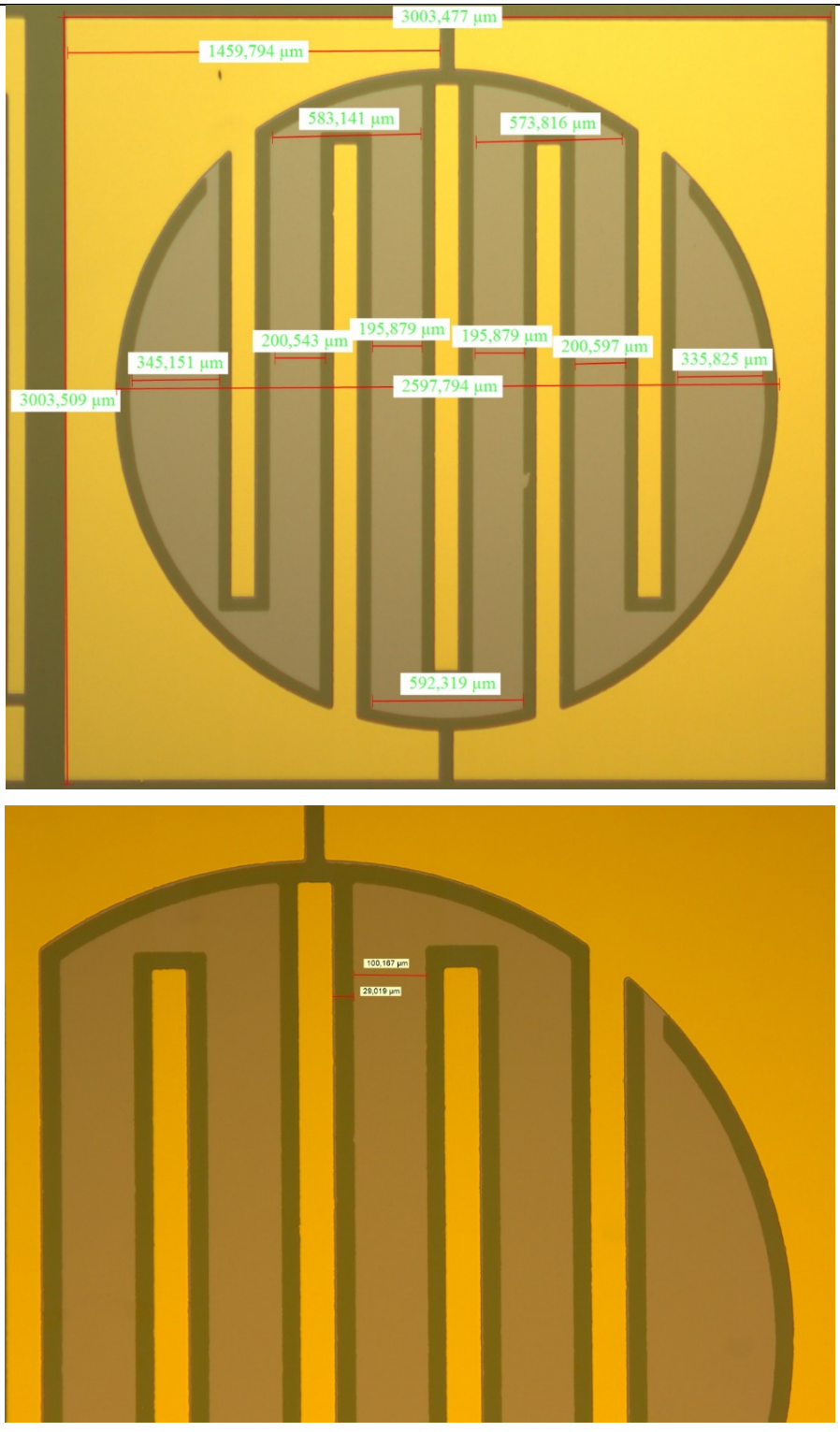

Figure 49 Dimension measurements of fabricated resistor with 50 µm line spaces using an optical microscope.

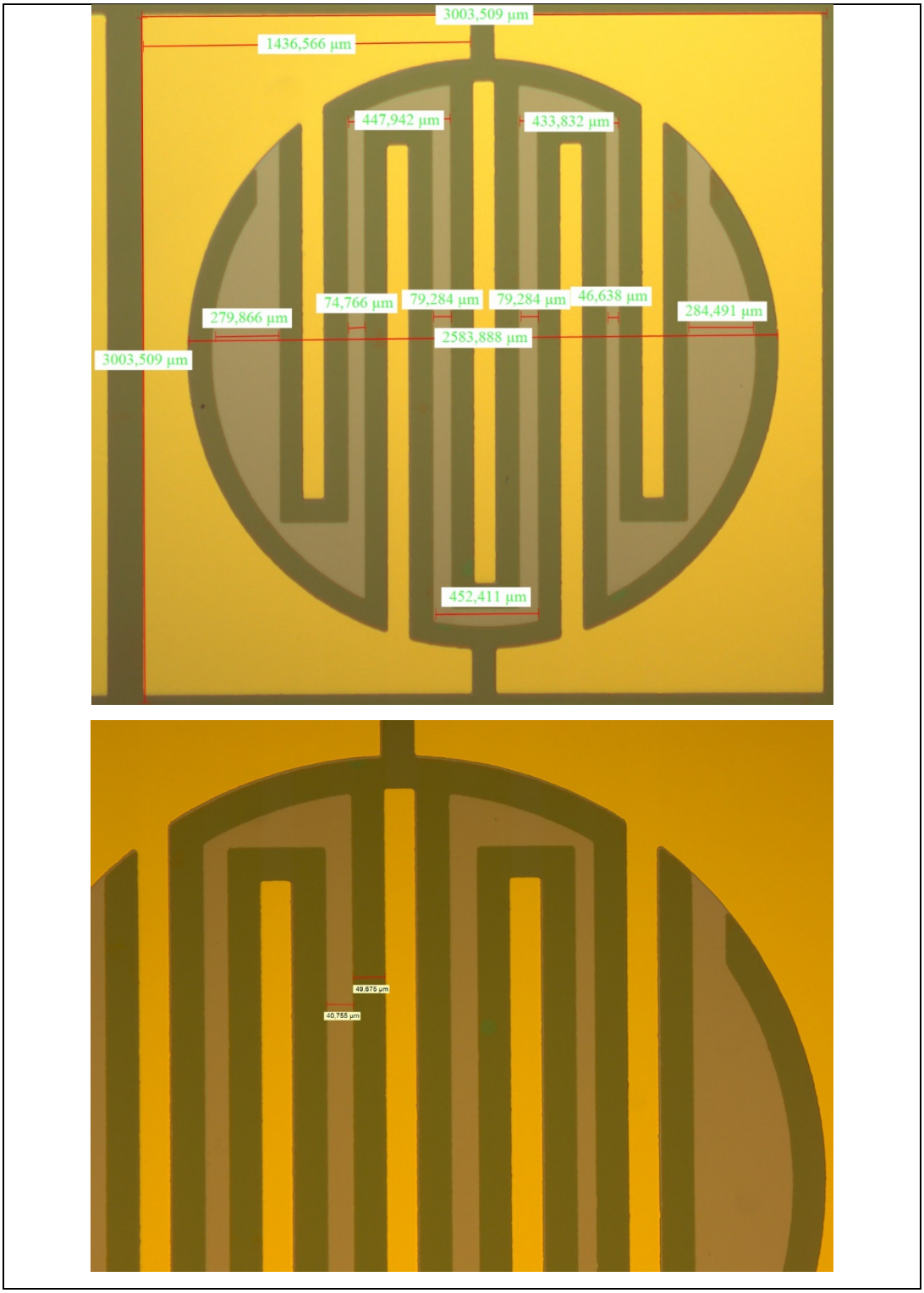

Figure 50 Dimension measurements of fabricated resistor with 100 µm line spaces using an optical microscope.