Carbon Nanotubes Directly Integrated in CMOS by Local Synthesis – Towards a Wafer-Level Process

Aasmundtveit, Knut; Roy, Avisek; Ta, Bao Quoc
Institutt for mikrosystemer- Universitetet i Sørøst-Norge

Accepted version of article in
2018 IEEE 13th Nanotechnology Materials and Devices Conference (NMDC)

Publisher's version: Aasmundtveit, K. E., Roy, A., & Ta, B. Q. (2018). Carbon Nanotubes Directly Integrated in CMOS by Local Synthesis-Towards a Wafer-Level Process. I *2018 IEEE 13th Nanotechnology Materials and Devices Conference (NMDC)* (s. 1-5). IEEE.

DOI: 10.1109/NMDC.2018.8605926

© 2018 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

Carbon Nanotubes Directly Integrated in CMOS by Local Synthesis – Towards a Wafer-Level Process

Knut E. Aasmundtveit*, Avisek Roy and Bao Q. Ta

IMS-Department of Microsystems, University of South-Eastern Norway, 3184 Borre, Norway

* Email address: kaa@usn.no, Phone: + 47 - 3100 9319

Abstract

Integrating nanomaterials in electronic circuitry and in microsystems is highly desired for fully exploiting the functionality of nanomaterials such as Carbon Nanotubes (CNTs), utilizing the signal processing of micro/ nano-electronics such as CMOS. An example device is a CNT-based gas sensor, where the extreme surface-to-volume ratio of CNTs provides ultra-high sensitivity, and direct integration with CMOS enables a device rendering processed, amplified and calibrated signals in a single, low-cost device. The CNTs should be synthesized on-chip directly into electric circuits. One challenge to overcome is the contradiction between temperature requirements for CNT growth (800-1000 °C) and CMOS compatibility (< 300 °C).

We can achieve local CNT growth temperatures while keeping the main part of the chip at CMOS compatible temperatures by designing resistive micro-heaters. Synthesized CNTs are directed towards an electrode for desired contact by applying a voltage that gives a guiding electric field. All process parameters are controlled electrically, enabling a wafer-level process compatible with high-volume, low-cost manufacturing.

This paper shows results from CNT integration in test vehicles manufactured in MEMS processes (using silicon microheaters), as well as our status towards realizing CNT integration in a purpose-designed CMOS chip (optionally using the chip's metal or polysilicon layers for microheaters).

Key words: Micro/ nano system integration, Carbon Nanotubes, Nanoscale assembly, Gas sensors.

Introduction

Carbon nanotubes (CNTs) have unique electronic, mechanical, thermal and optoelectronic properties, as well as a huge surface-to-volume ratio. They are used as constituent of advanced composites, e.g. for their mechanical strength. Their unique properties can be exploited for smart devices, such as ultrasensitive gas sensors, optoelectronic devices, field-emission based devices [1-5], and transistors, where CNTs may be the electron channel enabling transistor miniaturization beyond the limit predicted for Si processing [6]. For successful use of these nanostructures as functional materials, it is essential to integrate them into microsystems, with micro/ nanoelectronics [7], where they make part of the electronic circuits. The goal is to have a single manufacturing platform combining CMOS, MEMS and CNTs. Thus, a single chip can encompass sensing, processing and actuating functionality, and high-volume production can assure cost levels acceptable for the market.

On-chip CNT synthesis is hampered by conflicting thermal requirements: CNT synthesis processes are normally at high temperatures (700-1000 °C), using techniques such as arc discharge, chemical vapour deposition (CVD) and laser ablation, whereas CMOS compatibility typically requires that the temperature during post-processing should not exceed 300 °C, to avoid excessive dopant diffusion that will eliminate *pn*-junctions. CNTs may alternatively be manufactured in bulk, and subsequently integrated into CMOS/MEMS microsystems, but techniques for patterning, nanomaterial manipulation and bonding at nano-scale are not compatible with low-cost, high-volume production [8]. Integration schemes such as solution processing (dispersed CNTs) [9, 10] or dielectrophoresis [11] give little possibility for achieving single-nanotube connections or a well-aligned array of nanotubes for good electrical contact to electrodes.

On-chip synthesis of CNTs was demonstrated by Englander *et al* [12] and Christensen *et al* [13] in

2003, using resistive heating of purpose-made microstructures to synthesize CNTs locally, at the desired locations. These Si structures are suspended for thermal isolation. When heated by a current, large thermal gradients can be created so the hotspot of the microheater reaches CNT growth temperatures while the bulk of the chip is kept at ambient temperature. Carbon nanotubes grow at the hot regions upon introduction of a carbon-containing gas, and the direction of CNT growth is guided by an electric field, controlled by the voltage applied to the microstructures. Thus, CNTs can be directly integrated as part of closed circuits, and the number of CNTs closing a connection can be monitored through electrical measurements during the experiment. Similar approaches have been shown using metallic growth structures [14].

This paper presents the work of our group over the last decade, aiming towards a wafer-level, room-temperature, low-cost CMOS / MEMS - compatible process for direct integration of CNTs into CMOS and other Si microsystems. We have demonstrated that the synthesis process, as outlined above, can be controlled through electrical measurements only [15], allowing for implementation in an automated industrial setting, and scalable to wafer-level manufacturing. Using low-cost consumables and rapid processing at ambient temperature ensures the low cost crucially important for such a process to be industrially feasible. Until now, our test vehicles for growing CNTs are made in MEMS processes, which are well suited for design and fabrication of dedicated microstructures for microheaters. MEMS processes share many similarities with CMOS processes, and can therefore be used as relevant demonstrators for CNT-to-CMOS integration. However, dedicated CMOS processes are not intended for fabricating mechanical structures as a microheater, hence the implementation in CMOS will bring new challenges, which we will detail in this paper. We have currently designed a dedicated CMOS chip for CNT integration. Post-processing of this CMOS chip is required for CNT integration, this work is ongoing.

Our goal is to define processes needed to enable CNT integration to be a standard part of a CNT-CMOS process for advanced, smart systems. Gas sensing for monitoring the aging process of food is an example where cheap and sensitive devices are necessary at the consumer level. This paper also demonstrates the potential of our process to implement such a compact and ultra-sensitive sensor. In this integrated device, CNTs can be used in their virgin state or they can be functionalized to increase the sensitivity and selectivity towards specific gases and analytes.

CNT growth structures, designed in MEMS processes

Test vehicles for CNT local synthesis were designed and fabricated in the PolyMUMPS (polysilicon structures) and SOIMUMPS (single crystal Si structures) processes. Polysilicon structures simulate a process that integrates CNTs in CMOS at low cost. Single crystal structures using SOI gives the additional possibility to design a hole in the chip. This allows for transmission imaging of CNTs using S(T)EM, revealing far more details than standard SEM (scanning electron microscopy).

The geometry of the microheaters is designed, using FEM simulations, to give the required temperature gradients when passing a specified current. That current must be sufficiently small to avoid resistive heating in other circuitry than were intended. The validity of the temperature simulations has been confirmed through four-point resistive measurements on dedicated structures, and through the use of temperature-sensitive paint as an independent control.

Figure 1 shows an example of such a microstructure: A resistive microheater with a wider central part for uniform temperature distribution and a meandering part to account for thermal expansion, and a secondary microbridge to which CNTs are guided by the applied electric field.

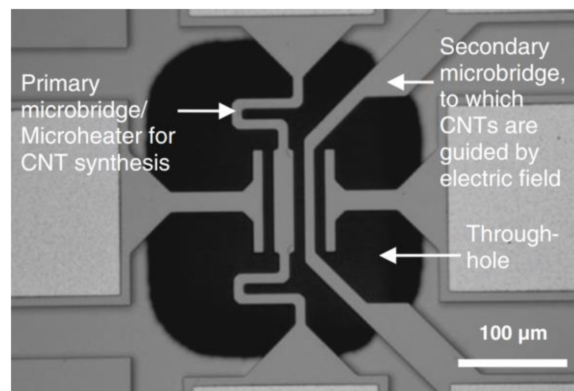

Figure 1: Micrograph of SOI microstructure for localized CNT growth.

As catalyst for CNT growth, a 1-3 nm Fe layer is deposited on the Si microheaters by thermal evaporation, forming nanoparticles upon thermal annealing (performed by passing a current) [16]. The current is adjusted to the value needed to obtain the specified CNT growth temperature, a flow of C_2H_2 and Ar is introduced, and an electric field is applied between the two microstructures. Figure 2 shows a sketch of this CNT growth process. The current between the two microstructures is continuously monitored for observing when CNTs close the circuit between the two structures.

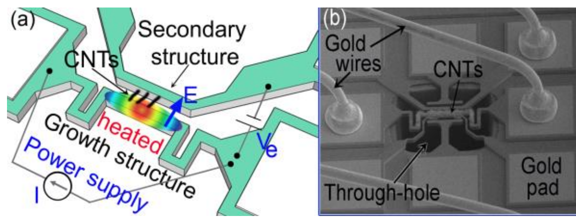

Figure 2: (a) Sketch of the CNT growth process. (b) Micrograph showing electrical connections.

CNT growth, MEMS growth structures

Figure 3 shows the current between the two Si microstructures, monitored during the synthesis process. The current increases stepwise when CNTs connect the two structures to form a closed electrical circuit. When connection(s) are broken, the current decreases stepwise. The connections are somewhat fragile before the situation stabilizes, as seen in Figure 3.

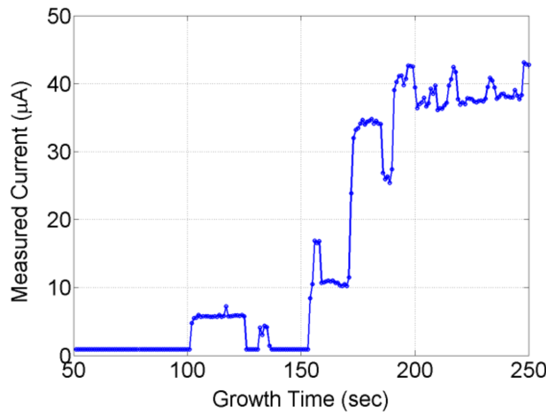

Figure 3: Current flowing in CNT connections during the synthesis process.

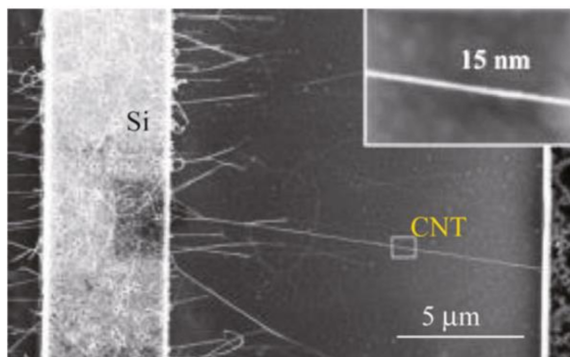

Figure 4: CNTs grown on heated microstructure.

Figure 4 shows a microheater after CNT growth, with a large number of CNTs. Most CNTs are curled and disordered, located on the microheater itself, but a number of CNTs are straight and actually close the gap between the two microstructures, as expected from the current-time measurement shown in Figure 3. Only the CNTs closing the gap will become part of an electric circuit, and contribute to the measured signal in a sensor device. A thorough study of chips with a thousand of CNTs shows that the thinner CNTs ($d <$ 5-10 nm) are straight and aligned to the electric field, whereas CNTs with higher diameters tend to be more disordered, as shown in Figure 5 [17]. These observations are supported by an electrostatic and thermodynamic model.

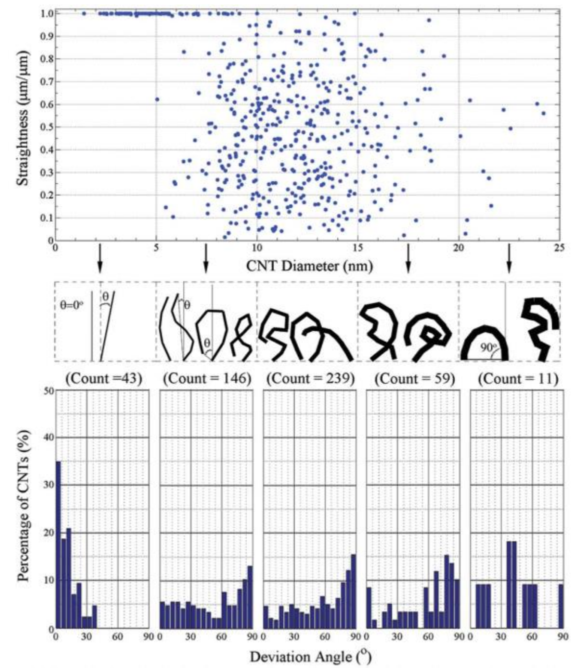

Figure 5: Distribution of CNT "straightness" (ratio of vector length and arc length between the two ends of each CNT), and angular direction.

This diameter-dependence on field alignment effectively ensures that only the thin, straight CNTs become part of the Si-CNT based device. This is an important observation, since the local growth process, effectively growing CNTs at very different temperatures at different positions of the microheaters, is not likely to produce as well-ordered CNTs as a bulk process with possibilities of subsequent refining may do.

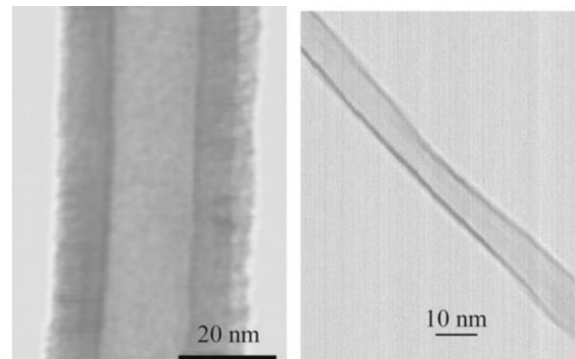

Figure 6: Detailed view of individual CNTs, transmission image in S(T)EM.

Figure 6 shows high-magnification transmission images of individual CNTs, with

diameters 40 nm and ~ 8 nm, respectively. The CNTs appear as multi-walled CNT (MWCNT).

Measured IV-curves show that some Si-CNT-Si systems are highly non-linear, whereas others have a near-ohmic behaviour [16]. We found this characteristic to depend on the Si doping level at the position of CNT attachment. CNTs can grow from different depth locations at the primary microbridge, and connect to different locations at the secondary microbridge. We assume our CNTs to be multi-walled (as suggested by their diameters), hence metallic. Connecting to highly doped Si, an ohmic behaviour is expected. For lower doping levels at the junction, a Schottky-type metal-to-semiconductor junction is expected. Both cases (as shown in Figure 7) were successfully modelled as electrical circuits with a number of parallel couplings of two diodes connected back-to-back in series with a resistance [16].

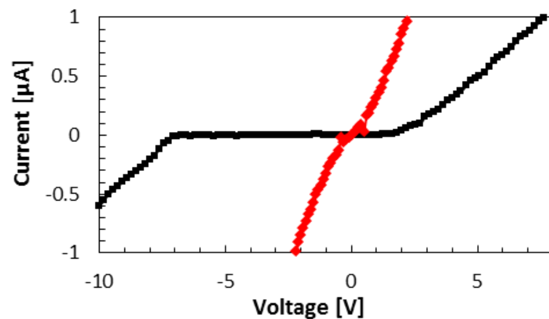

Figure 7: IV-curves for Si-CNT-Si systems, showing examples of near-ohmic and non-linear (Schottky-like) behaviour.

The fabricated Si-CNT-Si systems were subjected to gas sensing tests. We demonstrated that near-ohmic Si-CNT-Si systems can detect NH_3 gas at a concentration of 200 ppm [7]. We also demonstrated that Schottky-like Si-CNT-Si systems can be used for detection of CO_2 gas with a sensitivity of ~1 µV/ppm [18].

There are several methods to deposit functional materials on carbon nanotubes. Functionalization is needed to enhance the sensitivity and selectivity to various gases. Common methods for functionalization of CNTs involve doping CNTs via ion implantation or chemical modification [19] and attaching functional materials to CNTs via solution treatment and sonication [20]. However, fabrication processes of these methods require several post-processing steps, such as photolithography and lift-off. Solution treatment and sonication for attaching metal nanoparticles to the CNT surface would break the free-standing CNTs between the Si electrodes. Therefore, these methods are not well suited for functionalizing suspended CNTs.

In order to demonstrate the possibility to functionalize our CNTs, thermal evaporation of Palladium (Pd) [21] and atomic layer deposition (ALD) of metal oxides (ZnO, TiO_2 and Co_3O_4) [22] were done on a system with CNTs directly integrated. The Pd deposition thickness using the evaporation technique was around 1.6 nm, the result is shown in Figure 8. The thickness of the deposited metal oxides using ALD method varied from 2 nm to 30 nm.

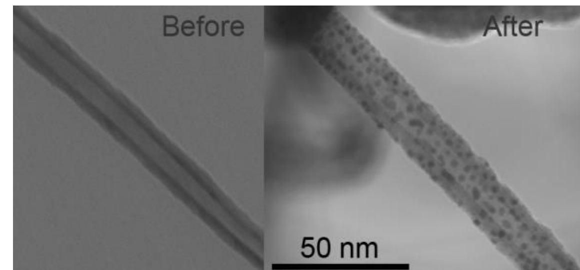

Figure 8: (Left) A CNT before thermal evaporation of Pd. (Right) a CNT covered with Pd nanoparticles after thermal evaporation. Transmission images in S(T)EM [23].

CNT growth structures in CMOS

Whereas CNT integration in MEMS can be interesting in itself, the main motivation for the MEMS-based CNT growth structures are as demonstrators for the feasibility of CNT-to-CMOS integration. The material (silicon) for MEMS and CMOS devices is the same, the typical overall dimensions are similar, and many of the basic fabrication processes are common. Very much of the knowledge obtained in MEMS-based CNT growth structures, is directly transferrable to CMOS-based structures, in particular when it comes to optimization of the CNT growth process. However, the MEMS and CMOS processes differ greatly in the ability to make free-standing structures such as micro-heaters. Since an integrated CMOS-MEMS process is not yet readily available, we look into how to integrate CNTs in a regular CMOS process.

For implementation directly in CMOS, fabrication of suspended microheaters implies post-processing (etching), which is ongoing work in our laboratory. The etching mask for post-processing can be designed in the CMOS chip, by using one of the CMOS layers as etching mask. Alternatively, non-suspended microheaters can be fabricated without the need of post-processing, at the cost of much higher thermal conductance from the hotspot, implying a higher applied power is needed, and the risk of overheating the CMOS circuitry increases.

Two different materials in the CMOS process can be used for microheaters: The semiconducting layer (polysilicon), or the conducting layers (typically Al, but Cu is also used in CMOS). Using polysilicon for microheaters will resemble our MEMS devices, but the layer thickness is much smaller in CMOS, implying a redesign of the

geometries. Aluminium cannot, however, be used directly as a microheater, since the melting temperature is below the desired CNT growth temperature. Also, the electrical and thermal resistivity is too low, requiring extreme dimensions of a microbridge for obtaining the required electrical and thermal performance. Such extreme dimensions will not satisfy mechanical requirements (for avoiding buckling and stiction of the microbridge).Alloying Al with a suitable metal to form intermetallic compounds (IMCs) is a potential solution to this, since IMCs typically have significantly higher melting temperatures and higher resistivities (electrical and thermal) than the pure metals they consist of. We have found Al-Ni IMCs to be promising candidates, since these have suitable material parameters, and since Ni deposition can be performed by a number of well-established techniques including electroplating. Using Al-Ni IMCs for microbridges implies two post-processing steps: Ni deposition and annealing for alloying with Al. By using electroplating as the Ni deposition method, the use of mask for metallization may be avoided, as the selected area for deposition can be controlled by selecting electrical circuits. The annealing can be performed resistively, in the same manner as heating is performed for CNT CVD.

High CNT synthesis temperature (~ 900 °C) is a vital challenge for directly growing CNTs in CMOS structures. Unlike MEMS, CMOS process have strict temperature limitation during any post processing as the circuits area should be kept in a temperature lower than 300 °C. The high thermal gradient needed to maintain the temperature requirements is also easier to achieve in MEMS due to the available established processes for fabricating suspended microstructures. In CMOS, we intend to partially suspend the microheaters to meet the requirements for both thermal gradient and mechanical stability of the heaters. Our thermomechanical simulations have shown positive results for the Al-Ni and polysilicon microheaters [24]. A cross-sectional sketch of the micro-heaters is illustrated in Figure 9, where the dielectric layer beneath the Al-Ni and polysilicon layers have limited etching to partially suspend the heaters.

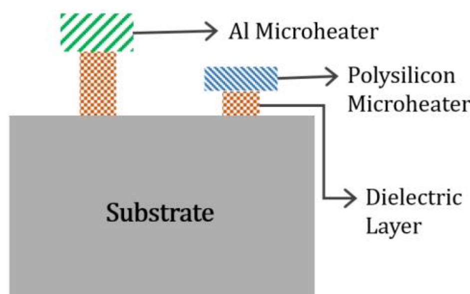

Figure 9: Cross-sectional sketch of partially suspended microheaters.

We have designed several microheaters with the Al & polysilicon layers of a standard AMS 350 nm CMOS process. CMOS chips including these microheaters have been fabricated using the same CMOS process [25]. Required post processing of the chips are currently ongoing. The fabricated polysilicon CMOS microheaters are less than 10 µm in length & 1 µm in width; whereas the silicon MEMS microheaters were around 160 µm in length & 5 µm in width. Reduced length & width (surface area) of the polysilicon microheaters mean lower heat conduction to the dielectric layer. In case of metal CMOS microheaters, the length and width is around 200 µm & 1 µm respectively. Due to low electrical resistivity of Al-Ni IMCs compared to polysilicon, length of the metal heaters needed to be extended significantly to achieve sufficient heater resistance - required for efficient joule heating.

Conclusion

The process of direct integration of CNTs in Si microsystems by local CVD synthesis holds great promise to give nano-functionality to CMOS devices. We have demonstrated and optimized the process using MEMS test vehicles, showing its ability to form electric circuits that includes thin, well-aligned CNTs. We also demonstrate the ability of such a circuit to act as a gas sensor, as well as demonstrating functionalization. We are currently in the process of demonstrating direct integration of CNTs in a purpose-made CMOS chip.

The process is controlled solely by electrical parameters, and is scalable to wafer-level. We see this as candidate for a standardized process for CNT/ CMOS integrated devices, opening vast possibilities in combining nanomaterial functionality with CMOS electronic circuitry.

Acknowledgements

The Research Council of Norway is acknowledged for grants to support the NORFAB infrastructure.

References

[1] T. Kawano, H. C. Chiamori, M. Suter, Q. Zhou, B. D. Sosnowchik, and L. Lin, "An electrothermal carbon nanotube gas sensor," *Nano Letters,* vol. 7, pp. 3686-3690, Dec 2007.

[2] C. B. Jacobs, M. J. Peairs, and B. J. Venton, "Review: Carbon nanotube based electrochemical sensors for biomolecules," *Analytica Chimica Acta,* vol. 662, pp. 105-127, 2010.

[3] P. Avouris, M. Freitag, and V. Perebeinos, "Carbon-nanotube photonics and optoelectronics," *Nature Photonics,* vol. 2, pp. 341-350, Jun 2008.

[4] T. Zhang, S. Mubeen, N. V. Myung, and M. A. Deshusses, "Recent progress in carbon nanotube-based gas sensors," *Nanotechnology,* vol. 19, Aug 20 2008.

[5] J. E. Morris and K. Iniewski, Eds., *Nanoelectronic Device Applications Handbook*. CRC Press, Taylor & Francis, 2013, p.^pp. Pages.

[6] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," *Applied Physics Letters,* vol. 73, pp. 2447-2449, Oct 26 1998.

[7] K. E. Aasmundtveit, B. Q. Ta, L. W. Lin, E. Halvorsen, and N. Hoivik, "Direct integration of carbon nanotubes in Si microstructures," *Journal of Micromechanics and Microengineering,* vol. 22, Jul 2012.

[8] K. E. Aasmundtveit, B. Q. Ta, N. Hoivik, and E. Halvorsen, "Electrical Control on Synthesis Conditions for Locally Grown CNTs on Polysilicon Microstructures," in *Nanoelectronic Device Applications Handbook*, J. E. Morris and K. Iniewski, Eds., ed: CRC Press, Taylor & Francis, 2013.

[9] G. Qingqing, E. Albert, B. Fabel, A. Abdellah, P. Lugli, M. B. Chan-Park*, et al.*, "Solution-processable random carbon nanotube networks for thin-film transistors," in *Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on*, 2011, pp. 378-381.

[10] M. T. Humayun, R. Divan, Y. Z. Liu, L. Gundel, P. A. Solomon, and I. Paprotny, "Novel chemoresistive CH4 sensor with 10 ppm sensitivity based on multiwalled carbon nanotubes functionalized with SnO2 nanocrystals," *Journal of Vacuum Science & Technology A,* vol. 34, Jan 2016.

[11] M. A. Cullinan and M. L. Culpepper, "Design and fabrication of single chirality carbon nanotube-based sensors," in *Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on*, 2011, pp. 26-29.

[12] O. Englander, D. Christensen, and L. Lin, "Local synthesis of silicon nanowires and carbon nanotubes on microbridges," *Applied Physics Letters,* vol. 82, pp. 4797-4799, Jun 2003.

[13] D. Christensen, O. Englander, K. Jongbaeg, and L. Lin, "Room temperature local synthesis of carbon nanotubes," in *Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE Conference on*, 2003, pp. 581-584 vol. 2.

[14] S. Dittmer, O. A. Nerushev, and E. E. B. Campbell, "Low ambient temperature CVD growth of carbon nanotubes," *Applied Physics a-Materials Science & Processing,* vol. 84, pp. 243-246, Aug 2006.

[15] B. Q. Ta, N. Hoivik, E. Halvorsen, and K. E. Aasmundtveit, "Electrical control of synthesis conditions for locally grown CNTs on polysilicon microstructure," in *Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on*, 2011, pp. 374-377.

[16] T. B. Haugen, B. Q. Ta, E. Halvorsen, N. Hoivik, and K. E. Aasmundtveit, "Integration of Carbon Nanotubes in Microsystems: Local Growth and Electrical Properties of Contacts," *Materials,* vol. 6, pp. 3094-3107, Aug 2013.

[17] B. Q. Ta, E. Halvorsen, N. Hoivik, and K. E. Aasmundtveit, "Diameter dependency for the electric-field-assisted growth of carbon nanotubes," *Applied Physics Letters,* vol. 103, Sep 16 2013.

[18] H. Q. Nguyen, B. Q. Ta, N. Hoivik, E. Halvorsen, and K. E. Aasmundtveit, "Carbon nanotube based gas sensor for expiration detection of perishable food," in *Nanotechnology (IEEE-NANO), 2013 13th IEEE Conference on*, 2013, pp. 675-678.

[19] J. J. Adjizian, R. Leghrib, A. A. Koos, I. Suarez-Martinez, A. Crossley, P. Wagner*, et al.*, "Boron- and nitrogen-doped multi-wall carbon nanotubes for gas detection," *Carbon,* vol. 66, pp. 662-673, Jan 2014.

[20] E. H. Espinosa, R. Ionescu, B. Chambon, G. Bedis, E. Sotter, C. Bittencourt*, et al.*, "Hybrid metal oxide and multiwall carbon nanotube films for low temperature gas sensing," *Sensors and Actuators B-Chemical,* vol. 127, pp. 137-142, Oct 2007.

[21] B. Q. Ta, A. V. Ngo, H. Q. Nguyen, N. Hoivik, E. Halvorsen, and K. E. Aasmundtveit, "Deposition of palladium on suspended and locally grown carbon nanotubes using thermal evaporation," in *Nanotechnology (IEEE-NANO), 2013 13th IEEE Conference on*, 2013, pp. 1176-1179.

[22] K. E. Aasmundtveit, B. Q. Ta, A. V. Ngo, O. Nilsen, and N. Hoivik, "Functionalization of suspended carbon nanotubes in silicon microsystems by Atomic Layer Deposition (ALD)," in *14th IEEE International Conference on Nanotechnology*, 2014, pp. 659-662.

[23] B. Q. Ta, A. V. Ngo, Q. H. Nguyen, N. Hoivik, E. Halvorsen, and K. E. Aasmundtveit, "Deposition of Pd on Suspended and Locally Grown CNTs using Thermal Evaporation," presented at the IEEE Nano 2013, Beijing, China, 2013.

[24] A. Roy, F. Ender, M. Azadmehr, B. Q. Ta, and K. E. Aasmundtveit, "Design considerations of CMOS micro-heaters to directly synthesize carbon nanotubes for gas sensing applications," in *2017 IEEE 17th International Conference on Nanotechnology (IEEE-NANO)*, 2017, pp. 828-833.

[25] A. Roy, M. Azadmehr, P. Häfliger, B. Q. Ta, and K. E. Aasmundtveit, "Direct Synthesis of Carbon Nanotubes in CMOS – Layout of Micro-heaters," in *IEEE 18th International Conference on Nanotechnology (IEEE-NANO), 2018*, Accepted for publication, 2018.