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Analysis of an Approximated Model for the Depletion Region Width of Planar Junctionless Transistors

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Abstract: In this paper, we investigate the accuracy of the approximated analytical model currently utilized, by many researchers, to describe the depletion region width in planar junctionless transistors (PJLT). The proposed analysis was supported by numerical simulations performed in COMSOL Multiphysics software. By comparing the numerical results and the approximated analytical model of the depletion region width, we calculated that the model introduces a maximum RMS error equal to 90% of the donor concentration in the substrate. The maximum error is achieved when the gate voltage approaches the threshold voltage (V_{th}) or when it approaches the flat band voltage (V_{FB}) of the transistor. From these results, we concluded that this model cannot be used to determine accurately the flat-band and the threshold voltage of the transistor, although it represents a straightforward method to estimate the depletion region width in PJLT. By using the approximated analytical model, we extracted an analytical formula, which describes the electron concentration at the ideal boundary of the depletion region. This formula approximates the numerical data extracted from COMSOL with a relative error lower than 1%. The proposed formula is in our opinion, as useful as the formula of the approximated analytical model because it allows for estimating the position of the depletion region also when the drain and source terminals are not grounded. We concluded that the analytical formula proposed at the end of this work could be useful to determine the position of the depletion region boundary in numerical simulations and in graphical representations provided by COMSOL Multiphysics software.

Keywords: junctionless transistor; depletion region; electron concentration; COMSOL

1. Introduction

The concept of junctionless transistor (JLT) was introduced by Lilienfeld in 1925 [1]. The main characteristic of the Lilienfeld device was the absence of any p-n junction in the physical structure of the transistor. By controlling the voltage at the gate of this semiconductor device, Lilienfeld was able to deplete the carriers in a localized region of the substrate, called depletion region. In this manner, it was possible to control the resistivity of the device and the electrical current through the transistor. Although the idea and the operation of this device were verified through analytical formulas, the technology of that time did not allow him to realize a working device [2], which required the fabrication of a nanometric substrate layer. Only in 2010 at the Tyndall National Institute was the first junctionless transistor [2] successfully manufactured; J.P. Colinge et al. fabricated a 10 nm thick and 1 μm long highly doped (10^{19} cm^{-3}) junctionless nanowire transistor. The advantages of

a junction-free structure are numerous such as the absence of doping concentration gradients [3], which are difficult to be precisely controlled in the nanometric regime, the absence of junction leakages, simple fabrication process, and lower fabrication cost (no implantation for source and drain) [4]. In addition, junctionless technology can provide greater performance with respect to conventional transistors, such as reduced short-channel effects (effective channel length not reduced by p-n junctions) [5] and less degradation of carrier mobility (current flows in the bulk of the substrate) [6]. Junctionless transistors can be realized in different shapes and dimensions. Most often, they are characterized by a three-dimensional (3D) structure (ex: nanowire, finFET (fin field effect transistor) [7], GAA (gate all around) [8], etc.), which allows an improved control on the channel of the transistor. On the other hand, the implementation of two-dimensional (2D) or planar solutions have been recently investigated by numerous researchers because they are simple and easy to fabricate [9–12]. During the last decade, numerous implementations of junctionless transistors were proposed such as single gate [10,11], double gate [13], thin-film [12], tunnel-FET [14], just to mention a few. These structures are characterized by different geometries; however, their operation is based on the same working principle, which consists of varying the dimensions of the depletion region in order to control the flow of the current through the transistor. Due to the significant role of the depletion region in the operation of a JLT, numerous researchers have tried to extract an analytical formula, which relates the width of this region to the applied gate voltage. Unfortunately, the Poisson equation, which has to be solved to determine that such relation does not provide a closed form for an analytical solution [15]. In order to provide an analytical formula, which describes the operation of a JLT, some researchers have proposed introducing a few simplistic assumptions. Among the others, the complete depletion assumption is the most significant hypothesis that allows for extracting an approximated analytical formula for the depletion region width [12,16–19]. Although this approximated model have been mentioned and utilized in numerous scientific articles, its accuracy was never formally analyzed, at least to the best knowledge of the authors. For this reason, we decided to investigate on this issue, by analyzing and simulating a single gate PJLT using COMSOL Multiphysics software [20]. The paper is organized as follows. Section 2 introduces the working principle of a planar junctionless transistor, Section 3 describes the approximated model used to estimate the depletion region width of a PJLT, and Section 4 reports a detailed analysis of the approximated analytical model performed by using COMSOL Multiphysics software (version 5.4, COMSOL Inc). Finally, this paper ends with Section 5, which summarizes the main points of this paper and future works.

2. Single Gate Planar Junctionless Transistors

2.1. Physical Structure of PJLT

The physical structure of a planar junctionless transistor is shown in Figure 1a [11,21].

A PJLT is typically realized on a fully depleted silicon on insulator (FD-SOI) wafer [22], which is characterized by three layers: a handle substrate (silicon), an insulating layer often referred to as buried oxide or BOX since it is made of silicon dioxide and a thin silicon layer also known as device layer (silicon). In order to realize PJLT on FD-SOI wafers, the device layer is usually highly doped and characterized by a thickness in the range of tens to hundreds of nanometers. The device layer can be uniformly doped with acceptor or donor atoms. For this reason, we have to distinguish two categories of PJLT: p-type PJLT and n-type PJLT. The particular case of an n-type PJLT is represented in Figure 1. The handle substrate does not require to be doped unless the designer decides to use it as a second gate terminal or back gate. In this paper, we focus on a single gate PJLT; therefore, we will neglect the back gate terminal. The physical structure of a single gate PJLT resembles a MOSFET (metal oxide semiconductor field effect transistor); however, in PJLT, there are no p-n junctions. Although the operation of a PJLT is possible with a uniformly doped device layer, better performance is achieved by realizing highly doped drain and source wells. These minimize the parasitic resistances between the channel of the transistor (conductive part of the device layer between the wells) and the actual source

and drain metallizations. In particular, if the device layer is n-doped, then the source and drain wells must be heavily doped with donors (n⁺⁺). On the other hand, if the device layer is p-doped, then the source and the drain wells must be heavily doped with acceptors (p⁺⁺). These wells are represented with black regions in Figure 1a. Finally, a very thin insulating layer separates the gate terminal of the PJLT and the device layer beneath.

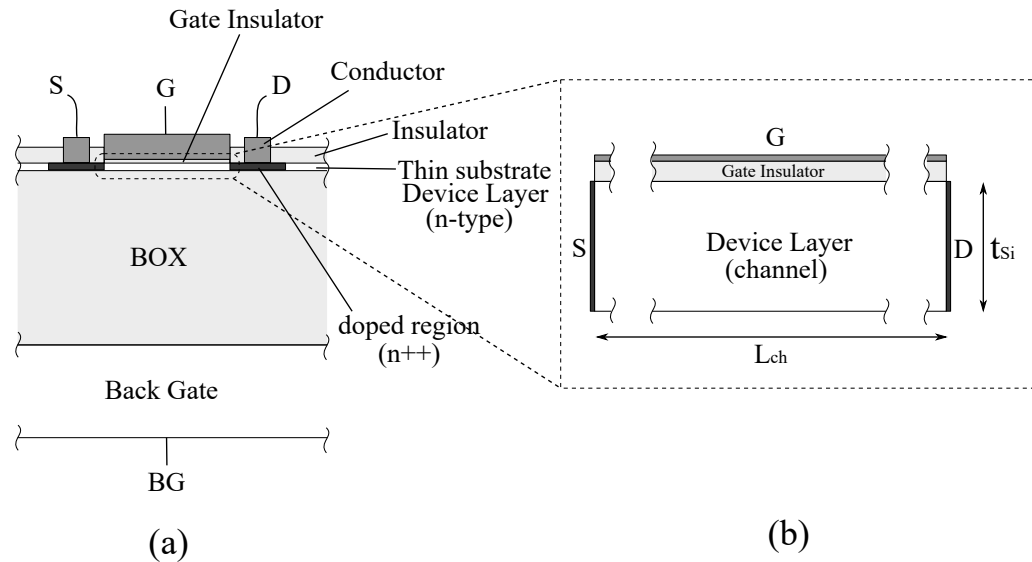


Figure 1. N-type PJLT physical structure; (a) complete structure on FDSOI wafer; (b) simplified model of the JLT physical structure.

2.2. Working Principle of Single Gate PJLT

Current literature describes PJLT as gated resistors [2] in which the amount of electrical current through the device is controlled by the gate voltage [3]. In order to clarify this definition, we will consider a simplified model of the single gate PJLT shown in Figure 1b. An electrical current, typically known as drain current, flows through the channel of the transistor, only when a voltage difference is applied between the drain and the source terminals. For the case shown in Figure 1b, the channel is fully enhanced (completely conductive), hence the amplitude of the drain current is only limited by the electrical resistance of the device layer. This resistance depends on the device layer resistivity ρ_{Si} and the geometrical dimensions of the channel such as channel width W_{ch} , channel length L_{ch} and channel thickness t_{Si} ($R_{ch} = \rho_{Si}L_{ch} / (W_{ch}t_{Si})$). However, if we vary opportunely the gate voltage of this transistor, we can affect the carrier distribution inside the device layer modifying the effective dimensions of the channel, thus varying the resistance and the electrical current through the transistor. In order to exploit the effects that the gate voltage provides on the channel of the transistor, we analyzed an n-type PJLT in capacitor configuration as shown in Figure 2.

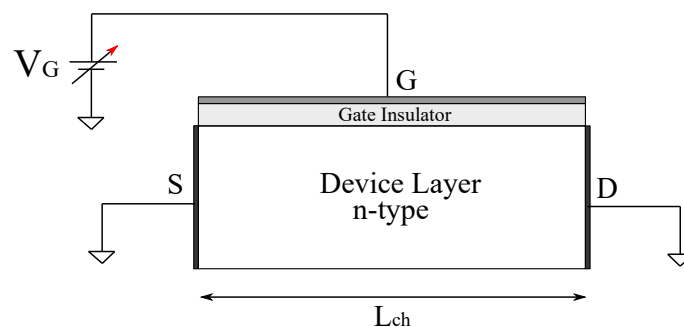


Figure 2. N-type PJLT capacitor.

In this scenario, the device layer acts as the second electrode of the PJLT capacitor and for this reason has been grounded through the source and drain terminals. Next, by reducing the gate voltage to negative values, the electrons under the gate insulator will be repelled and moved away from their initial position. In this region, the atoms will be depleted of carriers; hence, a non-conductive region known as a depletion region will start to be created as shown in Figure 3a.

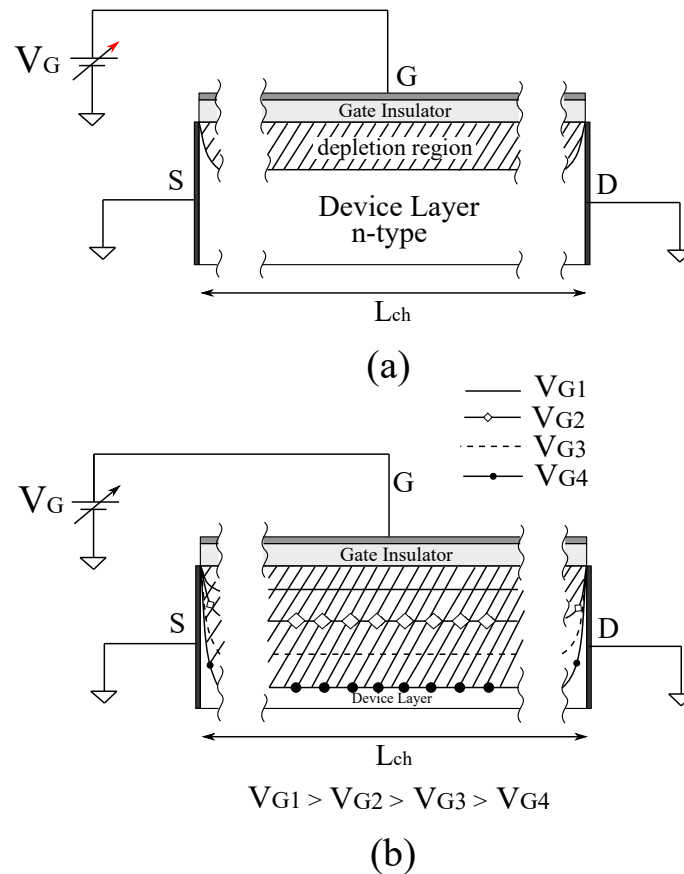


Figure 3. N-type PJLT working principle. (a) state of the PJLT for a generic value of gate voltage; (b) depletion region for different values of gate voltage.

The presence of a depletion region in the device layer reduces the dimensions of the conductive channel of the transistor, increasing the electrical resistance between drain and source terminals. We can observe that, if the channel length is sufficiently long, the depletion region is uniform in the middle of the substrate. However, as soon as we get closer to the drain and source terminals, the depletion region starts to curve due to the electric potentials V_D and V_S . Figure 3b shows that, if the gate voltage becomes sufficiently negative, then the channel of the transistor will be fully depleted of carriers and there will not be any conductive path between the drain and the source terminals. When this event occurs, the transistor is said to be turned off.

Finally, a detailed analysis conducted in Section 3 shows that the gate voltage at which the PJLT can be considered fully conductive or turned on is equal to the flat band voltage of the transistor $V_{G,ON} = V_{FB}$. On the other hand, the gate voltage value at which the transistor can be considered turned off is usually referred to as threshold voltage $V_{G,OFF} = V_{th}$.

3. An Approximated Model for the Depletion Region

The relation between gate voltage and the dimension of the depletion region can be extracted by solving the Poisson equation, shown in Equation (1) (for n-type PJLT), inside the device layer:

$$\frac{d^2\phi(x)}{d^2x} = -\frac{\rho(x)}{\epsilon_{Si}} = -\frac{q(p_n(x) - n_n(x) + N_D^+)}{\epsilon_{Si}}, \tag{1}$$

where $\phi(x), \rho(s), n_n(x), N_D^+$ and $p_n(x)$ are the distribution of the electric potential, the distribution of the charge density, the distribution of the concentration of electrons, the distribution of the concentration of the positive ions, and the distribution of the hole concentration, respectively, all evaluated along the symmetric axis of the transistor. Furthermore, ϵ_{Si} is the dielectric constant of the silicon substrate and q is the elementary charge $\simeq +1.6 \times 10^{-19}C$. Unfortunately, this equation cannot be solved analytically because $n_n(x)$ and $p_n(x)$ depend on the electric potential $\phi(x)$ as shown in Equation (2) (Complete derivation in Appendix A):

$$\frac{d^2\phi(x)}{d^2x} = -\frac{q\left(\frac{n_i^2}{N_D}e^{-\frac{\phi(x)}{V_t}} - N_D e^{\frac{\phi(x)}{V_t}} + N_D^+\right)}{\epsilon_{Si}}. \tag{2}$$

In order to find an analytic solution to this problem, we have to take advantage of a few assumptions. First of all, we assume that the minority carrier concentration is negligible ($p_n(x) \simeq 0$) during the whole operation of the the PJLT. Next, we assume complete ionization ($N_D^+ = N_D$). Finally, we need to utilize the hypothesis of complete depletion ($n_n(x) \simeq 0 \quad \forall x \in [0, X_{dep}]$, where $x = 0$ is situated at the interface SiO_2 /substrate, and X_{dep} corresponds to the position of the depletion region boundary). In this case, the equation simplifies as shown in Equation (3):

$$\frac{d^2\phi(x)}{d^2x} \simeq -\frac{qN_D}{\epsilon_{Si}}, \quad \forall x \in [0, X_{dep}]. \tag{3}$$

From this approximated form of the Poisson equation, we can finally obtain the target formula, shown in Equation (4):

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{ox}} + \sqrt{\left(\frac{\epsilon_{Si}}{C_{ox}}\right)^2 - \frac{2\epsilon_{Si}}{qN_D} (V_G - V_{FB})}. \tag{4}$$

A similar formula can be found for a p-type PJLT as shown in Equation (5):

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{ox}} + \sqrt{\left(\frac{\epsilon_{Si}}{C_{ox}}\right)^2 + \frac{2\epsilon_{Si}}{qN_A} (V_G - V_{FB})}, \tag{5}$$

where C_{ox} is the capacitance per unit area of the oxide used to implement the thin gate insulating layer, N_D is the donor concentration used to dope the device layer in n-type PJLT, N_A is the acceptor concentration used to dope the device layer in p-type PJLT, V_G is the gate voltage, and V_{FB} is the flat band voltage. These analytical formulas provide numerous amounts of information about the operation of the transistor. For the case of an n-type PJLT, the depletion region exists only for $V_G < V_{FB}$, while, for the p-type PJLT, the depletion region exists only for $V_G > V_{FB}$. In both cases, at $V_G = V_{FB}$, the depletion region is practically negligible, and the channel can be considered fully conductive. This is the reason why V_{FB} represents the voltage at which the transistor is considered turned on. There is a third situation that can occur during the operation of PJLT when $V_G > V_{FB}$ (for n-type PJLT); however, in this paper, we restrict the analysis to the range $[V_{th}, V_{FB}]$, which simplifies the description of the transistor operation. The formulas for threshold voltage V_{th} can be derived from Equation (4) or Equation (5) by assuming $X_{dep} = t_{Si}$. The on and off gate voltage values of an n-type PJLT are shown in Equation (6):

$$\begin{cases} V_{G-ON} = V_{FB} \\ V_{G-OFF} = V_{th} = V_{FB} + \frac{qN_D}{2\epsilon_{Si}} \left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - \left(t_{Si} + \frac{\epsilon_{Si}}{C_{OX}}\right)^2 \right]. \end{cases} \tag{6}$$

Similar formulas are valid for the p-type PJLT, which are shown in Equation (7):

$$\begin{cases} V_{G-ON} = V_{FB} \\ V_{G-OFF} = V_{th} = V_{FB} - \frac{qN_A}{2\epsilon_{Si}} \left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - \left(t_{Si} + \frac{\epsilon_{Si}}{C_{OX}} \right)^2 \right]. \end{cases} \quad (7)$$

More details about the difference between the operation of an n-type and a p-type PJLT can be extracted by analyzing the plots of the formulas in Equations (4) and (5), shown in Figure 4.

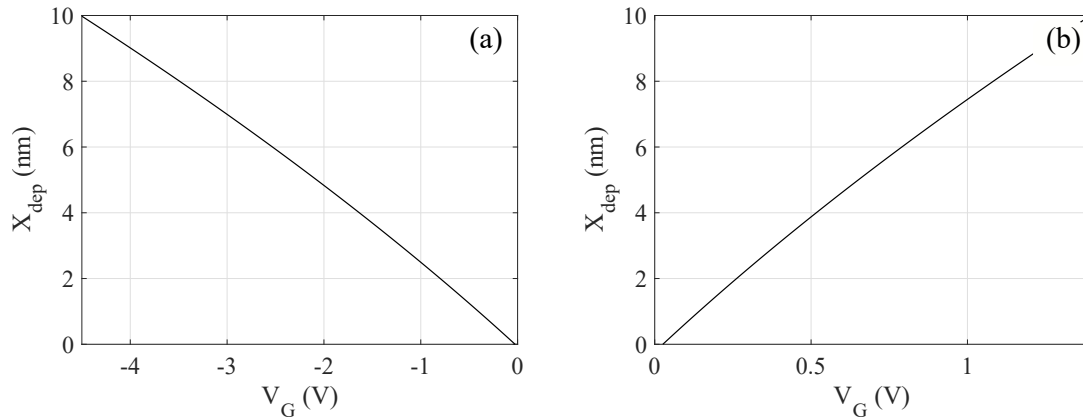


Figure 4. Analytical depletion width as a function of the gate voltage computed with the data in Table 1. (a) N-type PJLT; (b) P-type PJLT.

These graphs were extracted by using the parameters shown in Table 1.

Table 1. Depletion PJLT parameters

Parameter	n-Type PJLT	p-Type PJLT
	Value	
Materials		
Device layer	Si/n-type	Si/p-type
insulating gate layer	<i>SiO₂</i>	
Gate electrode	N-type Poly-Si	P-type Poly-Si
Material proprieties		
Device layer Doping concentration (atoms/cm ³)	$N_D = 10^{19}$	$N_A = 3.05 \times 10^{18}$
Intrinsic carrier concentration : n_i (atoms/cm ³)	5.4×10^9 at 293.15 K	
Dielectric constant device layer : ϵ_{Si} (F/cm)	$11.7\epsilon_0$	
Dielectric constant insulator : ϵ_{ox} (F/cm)	$3.9\epsilon_0$ (<i>SiO₂</i>)	
Dimensions		
Channel length : L_{ch} (nm)	500	
Device layer thickness : t_{Si} (nm)	10	
Gate oxide thickness : t_{ox} (nm)	8	
Derived Parameters		
Electron affinity: $q\chi$ (eV)	4.05	
Energy band gap: E_g (eV)	1.13	
Bulk potential : $q\Phi_{n,p} = k_B T \ln(N_{D,A}/n_i)$ (eV)	0.539	0.509
Oxide capacitance per unit area : $C_{ox} = \epsilon_{ox}/t_{ox}$ (F/cm ²)	4.32×10^{-7}	
Gate work function: $q\Phi_M$ (eV)	4.05 (PolySi/n-type)	5.15 (PolySi/p-type)
Flat Band Voltage : V_{FB} (V)	−0.026	0.026

The n-type PJLT associated with the plot shown in Figure 4a is characterized by a device layer made of n-doped silicon, a gate insulating layer made of silicon dioxide, and a gate electrode made of n-type poly-silicon. On the other hand, the p-type PJLT associated with the plot shown in Figure 4b is characterized by a device layer made of p-doped silicon, a gate insulating layer made of silicon dioxide and a gate electrode made of p-type poly-silicon.

The doping concentration and the thickness of the device layer in the n-type PJLT are similar to the one used by Colinge in [2], and they ensured that the channel of the transistor can be fully depleted by applying a precise value of gate voltage V_{th} . A different criterion was used to decide the doping concentration and the thickness of the device layer for the p-type PJLT. In this case, we set these two parameters in order to obtain a unipolar gate voltage range characterized by a flatband voltage of approximately 0 V. This choice allows for using both transistors in analog and digital circuits characterized by single power supply. The channel length of the transistor was chosen to be sufficiently long so that the drain and source electric potentials would not affect the carrier distribution in the middle of the channel. In this way, we can study the dependency of the depletion region width due to the only effect of the gate electric potential. Next, the dielectric constants in Table 1 were found in [23]. The thickness of the gate insulating layer t_{ox} was set in order to provide a sufficiently high dielectric strength. In fact, this insulator layer has to withstand the electric field created by the gate electrode when its potential sweeps within the range $[V_{FB}, V_{th}]$.

By using the parameters listed in Table 1, we calculated the threshold voltage for both the n-type ($V_{th} = -4.51$ V) and p-type ($V_{th} = 1.39$ V) PJLT. This means that, in order to turn on and turn off these transistors, the gate voltage has to vary within the range $[-0.026$ V, -4.51 V] and $[0.026$ V, 1.39 V] for the n-type and p-type PJLT, respectively. In the n-type PJLT, the depletion region increases if the gate voltage becomes more negative than the electrical potential of the device layer, while, in the p-type PJLT, the depletion region width increases when the gate voltage becomes more positive than the electrical potential of the device layer. This is due to the fact that the depletion region in n-type PJLT expands if negative electrical charges accumulate at the gate electrode, so that the free electrons beneath the insulating gate layer are repelled. On the other hand, in p-type PJLT, the depletion region expands only if positive electrical charges accumulate at the gate electrode. This ensures that the holes beneath the gate insulating layer are repelled. Figure 4 shows that the operating range of the p-type PJLT is smaller than the one for the n-type. This situation occurs because these two ranges are proportional to the doping concentration in the substrate of these two devices, as shown in Equations (6) and (7).

4. Analysis and Simulations of the Approximated Model

The design and the analysis of the PJLT performed until this point are based on the main assumption of complete depletion. This assumption is often utilized in many scientific articles [17,24–32] to provide a simple analytical formula for the depletion region width in PJLT. This formula represents an approximated model of the depletion region width. Therefore, we decided to investigate about the accuracy and the source of errors of this model. A qualitative representation of the main parameters characterizing an n-type PJLT is shown in Figure 5

First of all, we observe that although the holes are attracted by the negative electric potential applied at the gate electrode, their concentration is assumed to be negligible during the whole operation of the PJLT ($p_n(x) \simeq 0$). Once reached the equilibrium state shown in Figure 5a, the depletion region is ideally emptied of electrons ($n_n(x) \simeq 0$), but filled by positive ions of impurities (complete ionization $N_D^+ \simeq N_D$). The distribution of carriers, ions and charge density characterizing this ideal situation are shown in Figure 5b–d. These plots show that the assumption of complete depletion impose a step profile (red lines) for the electron distribution inside the device layer. Figure 5d shows a localized positive charge distribution inside the depletion region generated by the uncovered ions of impurities. From a physical point of view, a step profile such as the one represented by red lines in Figure 5c,d is not possible because these physical quantities lack of continuity. A more realistic profile for the charge and electron distributions are represented by the green profiles (smooth profile).

Unfortunately, the real profiles of these two quantities do not allow for define a precise boundary for the depletion region, which to be identified must be approximated by using a simple model. In order to verify our previous qualitative analysis, we performed a few simulations of a 2D n-type PJLT by using COMSOL Multiphysics software. The geometrical dimensions of the simulated structure are shown in Figure 6.

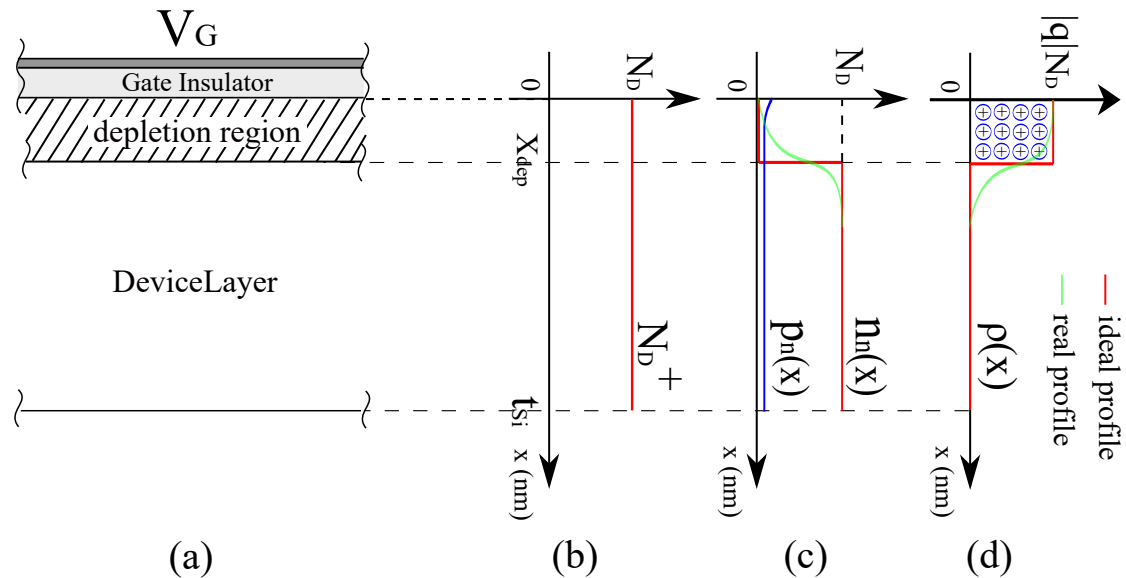


Figure 5. Profiles of the main parameters characterizing the depletion region in an n-type PJLT. (a) PJLT in capacitor configuration with source and drain sufficiently far from each other to consider the depletion region boundary uniform in the middle of the device layer; (b) impurity ions distribution inside the device layer (complete ionization); (c) carrier distribution inside the device layer (blue line = hole distribution, green line = real electron distribution, red line = ideal electron distribution); (d) charge density inside the device layer (green line = real charge density distribution, red line = ideal charge density distribution).

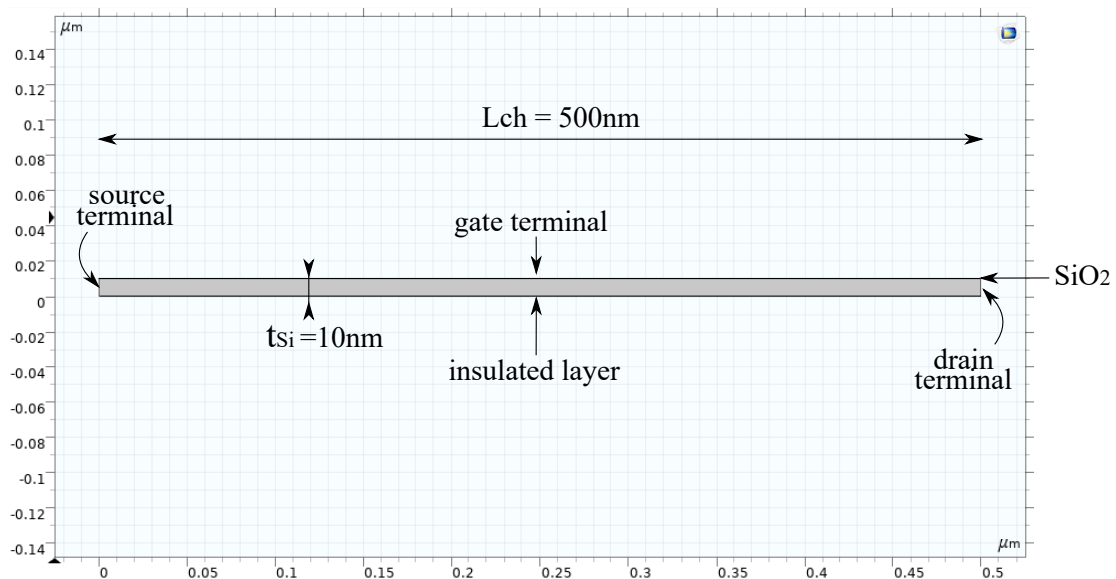


Figure 6. Geometrical dimensions of the simulated n-type PJLT.

The first simulation aimed to extract the "real" distribution of the electron concentration inside and outside the depletion region of the PJLT. By using the simulation results, we compared the real and the ideal electron concentration profile. Simulation results are shown in Figure 7.

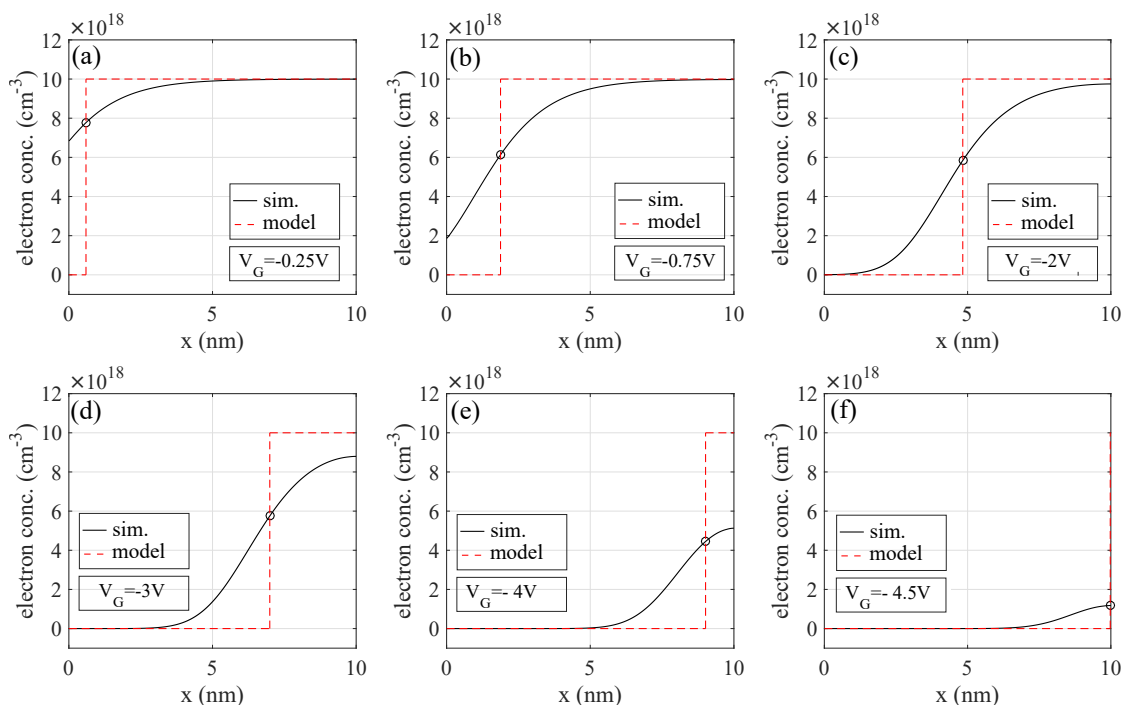


Figure 7. Comparison between the ideal and the simulated electron concentration inside the device layer, for different values of gate voltage. The parameter of the simulated structure are shown in Table 1. The PJLT was electrically connected as shown in Figure 3. $x = 0$ is placed at the interface SiO_2 /substrate. (a) Profiles for $V_G = -0.25$ V. (b) Profiles for $V_G = -0.75$ V. (c) Profiles for $V_G = -2$ V. (d) Profiles for $V_G = -3$ V. (e) Profiles for $V_G = -4$ V. (f) Profiles for $V_G = -4.5$ V.

Simulation results show an evident difference between the ideal electron concentration profiles representing the approximated analytical model and the simulated profiles. The main result from the analysis of these plots is that the electron concentration, inside the depletion region, is not zero and it can also reach significant values. This means that the formulas of the electric field and the electric potential distribution derived by using the hypothesis of complete depletion are affected by a certain amount of error, which may not be negligible. A qualitative analysis of the previous plots suggests that the greatest error of the analytical model occurs when the voltage approaches to V_{FB} and V_{th} . In fact, if we analyze Figure 7a, we observe that the electron concentration in what is supposed to be the ideal depletion region is actually almost equal to the maximum value N_D . Therefore, it is quite far from being completely depleted as the approximated analytical model claims. On the other hand, we observe in Figure 7e that the profile of the electron concentration inside the depletion region is similar to the ideal profile for values of V_G , but they are not equal yet. In this case ($V_G \simeq V_{th}$) the main source of error is due to the fact that the electron concentration outside the depletion region becomes so small that this region cannot be considered a good conductor as assumed by the analytical model. This was an important assumption, which allowed us to set zero electric field and zero electric potential at the boundary of the depletion region (see Appendix A). In conclusion, the main source of error of the approximated model consists in considering the term $n_n(x) = 0 \quad \forall x \in [0, X_{dep}]$ and $n_n(x) = N_D \quad \forall x \in [X_{dep}, t_{Si}]$.

Similar observations could be extracted by analyzing the charge distribution inside the device layer, shown in Figure 8.

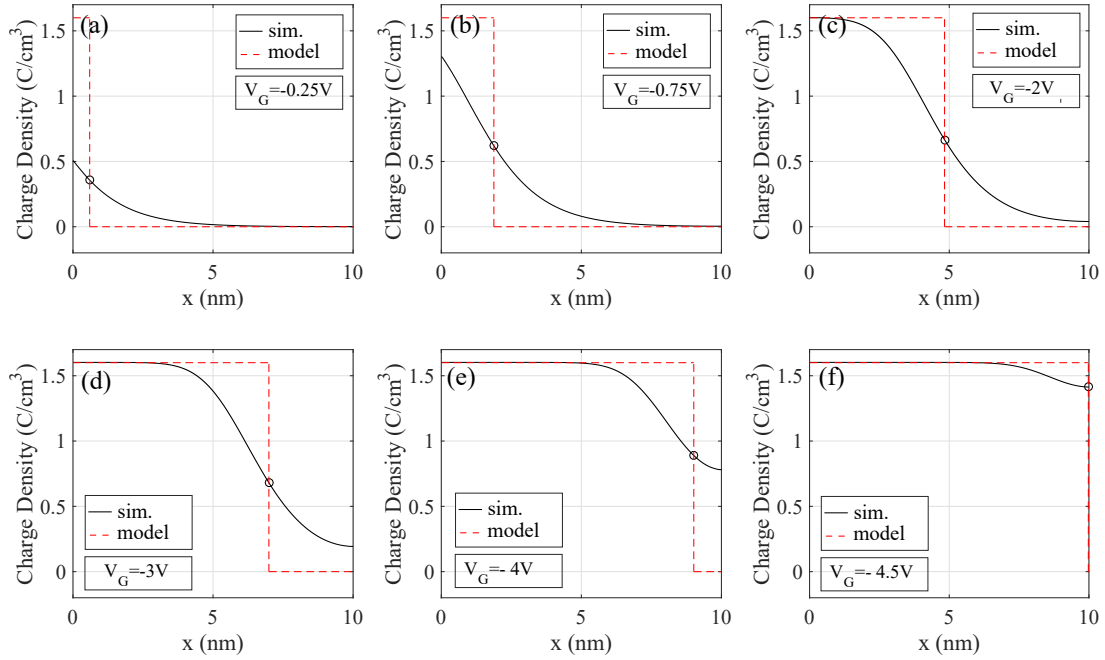


Figure 8. Comparison between the ideal and the simulated charge density inside the device layer, for different values of gate voltage. The parameters of the simulated structure are shown in Table 1. The PJLT was electrically connected as shown in Figure 3. $x = 0$ is place at the interface SiO_2 /substrate. (a) Profiles for $V_G = -0.25$ V. (b) Profiles for $V_G = -0.75$ V. (c) Profiles for $V_G = -2$ V. (d) Profiles for $V_G = -3$ V. (e) Profiles for $V_G = -4$ V. (f) Profiles for $V_G = -4.5$ V.

In order to quantify the error of the analytical model, we calculated the RMS error normalized with respect to N_D for the concentration of the electrons inside (ϵ_{RMSi}) and outside (ϵ_{RMSo}) the depletion region by using the formulas in Equations (8) and (9).

$$\epsilon_{RMSi} = \frac{1}{N_D} \sqrt{\frac{1}{X_{dep}} \int_0^{X_{dep}} n_n^2(x) dx} \quad x \in [0, X_{dep}] \tag{8}$$

$$\epsilon_{RMSo} = \frac{1}{N_D} \sqrt{\frac{1}{t_{Si} - X_{dep}} \int_{X_{dep}}^{t_{Si}} [N_D - n_n(x)]^2 dx} \quad x \in [X_{dep}, t_{Si}] \tag{9}$$

These RMS errors are plotted for different values of gate voltage and shown in Figure 9.

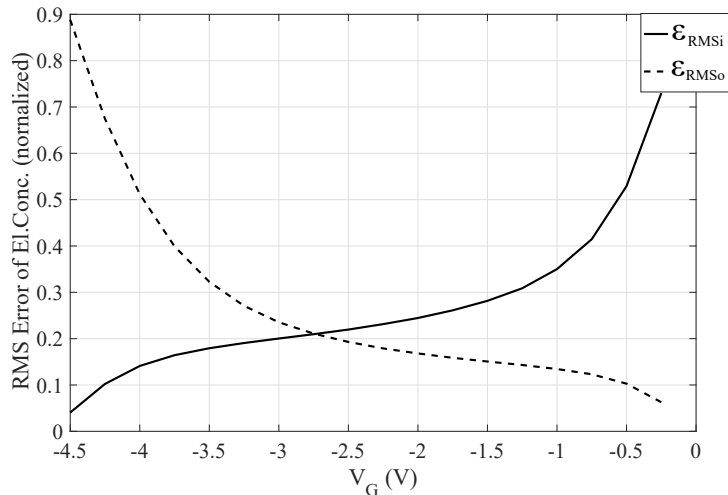


Figure 9. RMS error between the ideal and the simulated electron concentration profile inside (ϵ_{RMSi}) and outside (ϵ_{RMSo}) the depletion region, normalized in respect to N_D .

The previous plot shows that the error due to the approximation of complete depletion (ϵ_{RMSi}) and the error due to the approximation of conductive device layer (ϵ_{RMSo}) increase as soon as the gate voltage approaches V_{FB} and V_{th} , respectively. The maximum RMS error is approximately 90% of N_D , when the gate voltage approaches the threshold and the flat band voltage of the transistor.

Once the error introduced by the approximated model is quantified, we continued our analysis trying to extract a physical interpretation of this model. Figure 7 shows that the simulated charge density and electron concentration at the ideal boundary of the depletion region vary depending on the gate voltage applied. This trend is summarized in Figure 10.

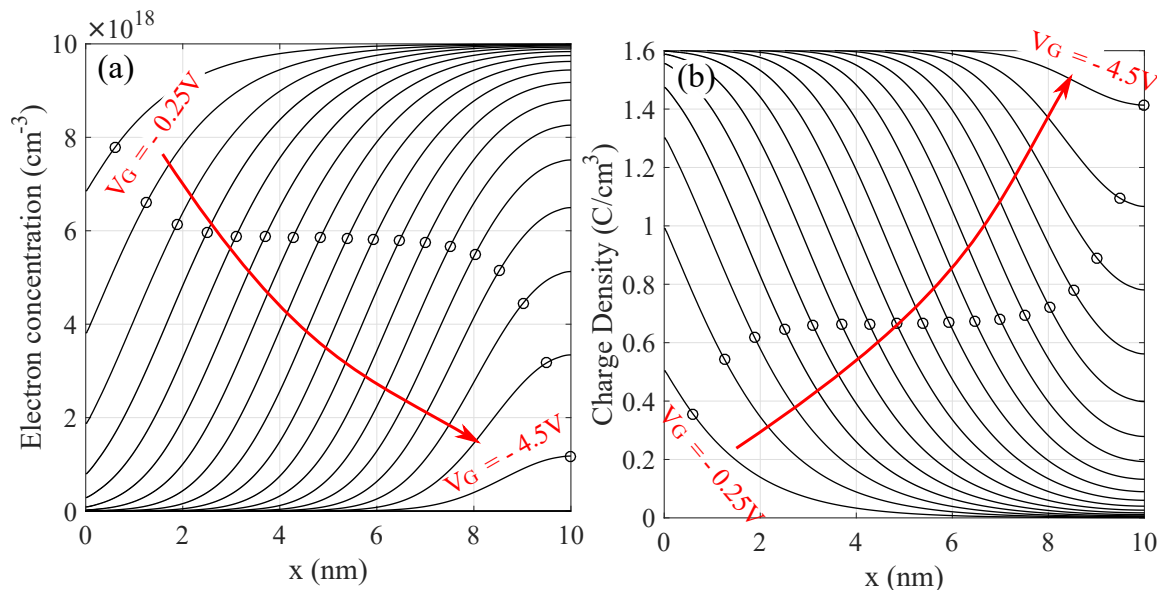


Figure 10. (a) electron concentration profiles for different values of gate voltage; (b) charge density profiles for different values of gate voltage. The circles represent the value of electron concentration and charge density at the ideal boundary of the depletion region. The gate voltage was swept in the range $[-0.25V, -4.5V]$ with a step of $0.25V$.

The circles on each curve represent the electron concentration or the charge density at the ideal boundary of the depletion region, which was calculated by using Equation (4). Figure 10a shows that the electron concentration at the ideal boundary of the depletion region is not constant or equal to half of its maximum value, as common sense would suggest. Instead, the electron concentration at the boundary of the depletion region increases as the gate voltage approaches V_{FB} and decreases as the gate voltage approaches V_{th} . Between these two values, there is a voltage range in which the electron concentration at the ideal boundary of the depletion region is almost constant and approximately equal to $0.58 \times 10^{19} \text{ cm}^{-3}$. A similar observation can be made in Figure 10b for the charge density at the ideal boundary of the depletion region. Finally, we can conclude that the approximated analytical model describes the boundary of the depletion region, as a locus of points characterized by an electron concentration, which depends on the applied gate voltage. This dependency is a consequence of the fact that the profiles of the electron concentration and charge density diverge from the ideal profiles, when the voltage approaches to V_{FB} and V_{th} .

During our analysis, we observed that a definition of the depletion region boundary in terms of electron concentration has one major advantage with respect to the definition based on spatial position described by Equation (4). The definition based on electron concentration can be used to determine the boundary of the depletion region also for the cases where the drain and source terminals are not grounded. In fact, in this case, the boundary of the depletion region is bent due to the variation of electric potential along the channel and this phenomenon is not taken into account by Equation (4). For this reason, we tried to extract an analytical formula, which describes the dependency of the electron concentration (and charge density) at the boundary of the depletion region with respect to

the applied gate voltage. First of all, we joined the circles in Figure 10 with straight lines as shown in Figure 11a,b. Then, we approximated these curves with polynomial functions. We observed that the relative error between the curves in Figure 11a,b and their polynomial approximation drop to a few percentage points when the order of the polynomial function approaches the eighth order as shown in Figure 11c,d.

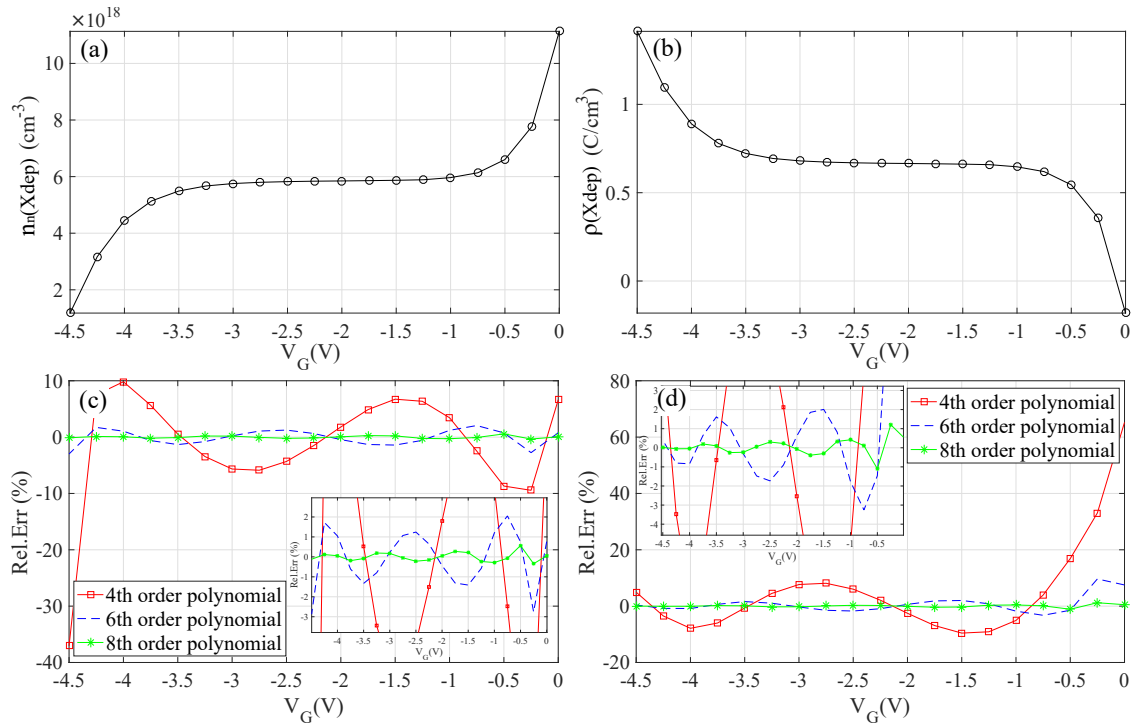


Figure 11. (a) electron concentration at the boundary of the ideal depletion region for different values of gate voltage; (b) charge density at the boundary of the ideal depletion region for different values of gate voltage; (c) relative error between the data in (a) and polynomial approximations of fourth, sixth, and eighth order; (d) relative error between the data in (b) and polynomial approximations of fourth, sixth, and eighth order. The gate voltage was swept in the range $[-0.25V, -4.5V]$ with a step of $0.25V$.

The analysis of the plots in Figure 11c,d shows that a good approximation of the data in Figure 11a,b is obtained by using a polynomial function of the eighth order, which provides a relative error of less than 1%. The eighth order polynomial formulas for $n_n(X_{dep})$ and $\rho(X_{dep})$ are shown in Equations (10) and (11):

$$n_n(X_{dep})_{8th} = [1.1127 + 2.0256V_G + 3.5541V_G^2 + 3.5545V_G^3 + 2.1561V_G^4 + 0.8023V_G^5 + 0.1782V_G^6 + 0.0216V_G^7 + 0.0011V_G^8] \times 10^{19}, \tag{10}$$

$$\rho(X_{dep})_{8th} = -0.1806 - 3.2454V_G - 5.6943V_G^2 - 5.6949V_G^3 - 3.4544V_G^4 - 1.2855V_G^5 - 0.2854V_G^6 - 0.0346V_G^7 - 0.0017V_G^8. \tag{11}$$

We can use these two equations for detecting the boundary of the depletion region for any value of gate voltage. Furthermore, these formulas can be used to provide a graphical representation of the depletion region boundary from the numerical results obtained in COMSOL Multiphysics. This includes also the cases where the drain is not grounded as shown in Figure 12.

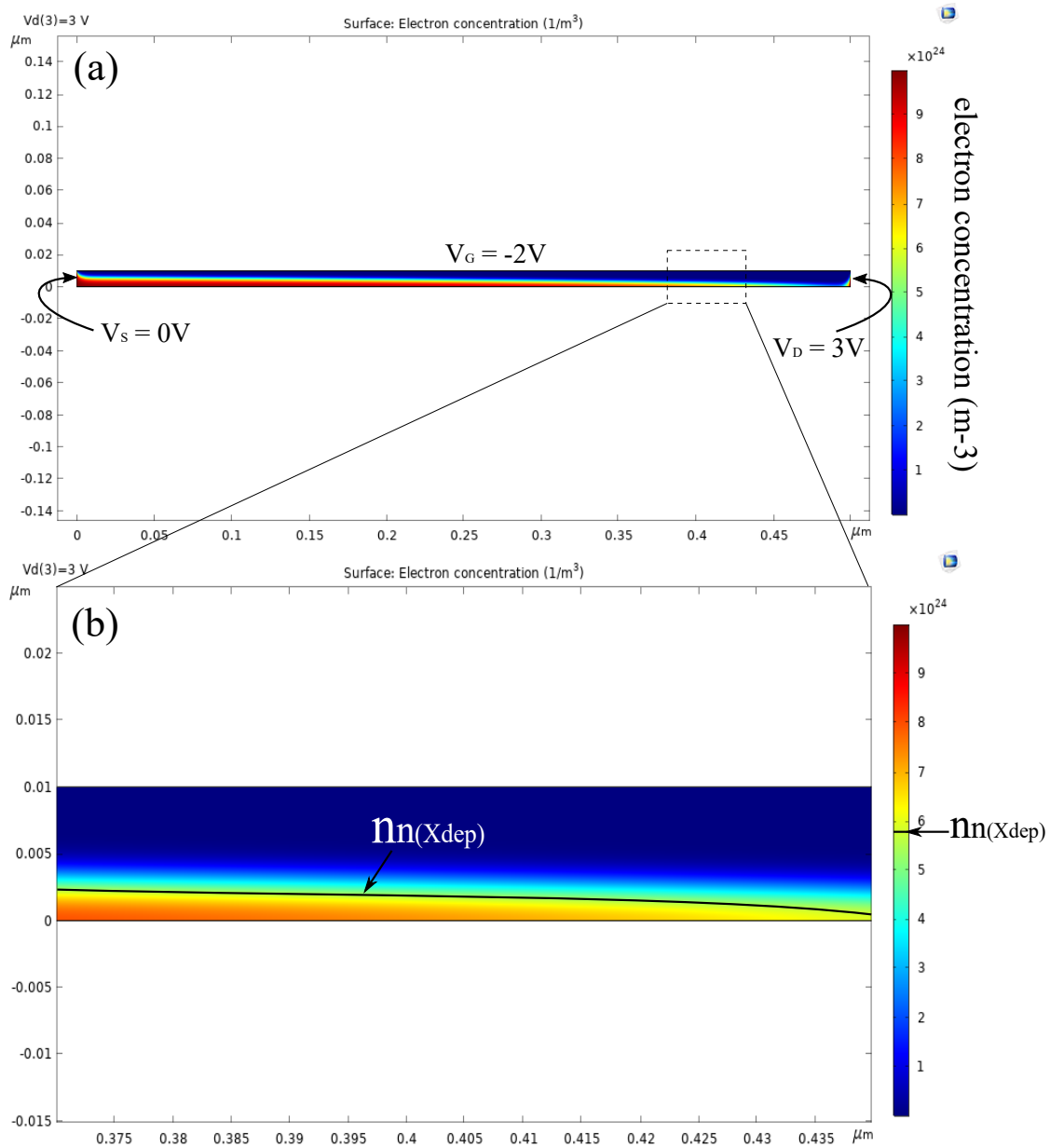


Figure 12. Electron concentration generated by COMSOL Multiphysics. $V_G = -2\text{ V}$ and $V_D = 3\text{ V}$. The black line represents the boundary of the depletion region. (a) whole PJLT; (b) zoom on a specific area of the PJLT.

Finally, we wanted to compare the approximated analytical model with another one derived by our own “common sense”. The “common sense” model is based on the assumption that the electron concentration at the boundary of the depletion region can be assumed to be half of the donor concentration inside the device layer. This represents the most intuitive model of the depletion region width. The electron concentrations at the depletion region boundary defined by the common sense threshold are circled and shown in Figure 13a.

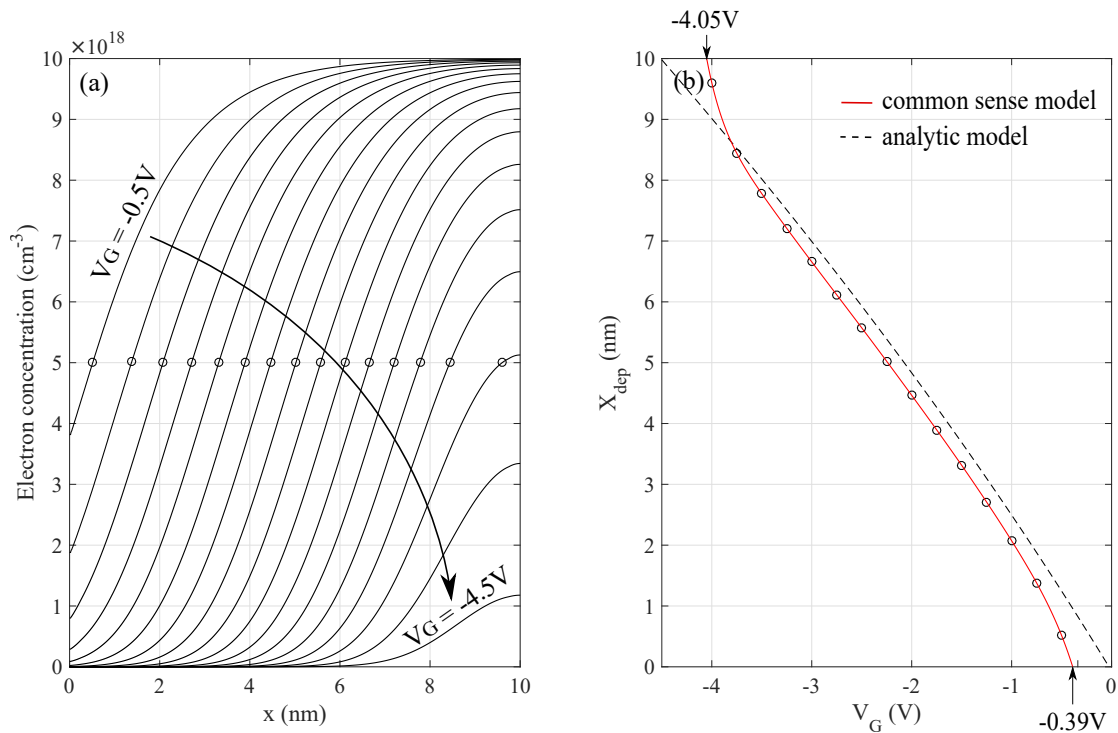


Figure 13. Comparison between the “common sense” model and the approximated analytic model. (a) detection of the electron concentration at the boundary of the depletion region defined by the “common sense” model for different values of gate voltage; (b) comparison between the depletion region estimated by the “common sense” model and the depletion region estimated by using the approximated analytic model described in Equation (4). The gate voltage was swept in the range $[-0.25, -4.5]$ with a step of 0.25V.

By using the x -coordinates of the "circles" drawn in Figure 13a and the voltages associated with the curves over which each circle lay, we can draw the red continuous line shown in Figure 13b. This curve represents the depletion region width model derived by using common sense. In the same plot, we drew a dashed line, which represents the analytic model that we investigated in this paper. First of all, we notice that the analytic model and the “common sense” model estimate two different values of depletion region width, when the same gate voltage is applied to the transistor. The two curves seem to follow a similar trend in the middle range of the gate voltage, although they are separated by an offset value. The “common sense” model predicts that the transistor should turn off when $V_G = -4.05$ V, and it should turn on when $V_G = -0.39$ V. These values are quite different than the OFF and ON voltage predicted by the approximated analytic model ($V_{th} \simeq -4.5$ V and $V_{FB} = -0.026$ V). Finally, by comparing the electron concentration profiles at the on and off voltages of these two models (Figure 13a and Figure 10a), we find out that the approximated analytic model is the one that provides an electron concentration profile, which resembles better the ideal profile. In fact, if we compare the electron concentration profiles extracted at the off voltage of these two models, then we can observe that the electron concentration profile predicted by the "common sense model" (curve in Figure 13a for $V_G \simeq -4$ V) is much larger than the one predicted by the approximated analytical model (curve in Figure 10a for $V_G \simeq -4.5$ V). This means that the substrate of the transistor is more conductive at the off voltage predicted by the “common sense” model, thus the off state of the transistor is better approximated if we estimate the depletion region width by using the approximated analytical model. A similar consideration can be done when we analyze the electron concentration profiles at the on voltages associated with the two models. We conclude that the “common sense” model is less accurate than the analytic model, when the transistor approaches the on and off state. However, the “common sense” model still represents a good approximation when the gate voltage is far from the on and off voltage values.

5. Conclusions

In this paper, we analyzed and quantified the error introduced by the approximated model, which is widely used to describe the depletion region width of junctionless transistors. The analysis was supported by numerical simulations performed in COMSOL Multiphysics software. Simulation results of an N-type PJLT showed that the analytical model is affected by a significant error when the gate voltage approaches the threshold voltage or when it approaches the flat-band voltage of the transistor. In these two extreme cases, the RMS error of the electron concentration profile inside and outside the depletion region was calculated to be approximately 90% of the donor concentration inside the substrate of the transistor. This proves that the approximated analytical model does not provide an accurate formula to calculate the values of the flat-band and threshold voltages of the transistor. Furthermore, we found out that the approximated analytical model of the depletion region width defines the depletion region boundary characterized by a value of electron concentration, which depends on the applied gate voltage. This dependency was analytically extracted by using an eighth order polynomial function. Finally, we proved that this polynomial formula is as useful as the initial analytical model because it can be utilized to determine the position of the depletion region boundary in numerical simulations, when the drain and source terminals are not grounded.

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Appendix A. Depletion Region Width Analytical Formula

The purpose of this appendix is to clarify the procedure utilized to derive the analytical model of the depletion region width in a PJLT. The structure analyzed in this paper is an n-type PJLT connected in capacitor configuration as shown in Figure A1.

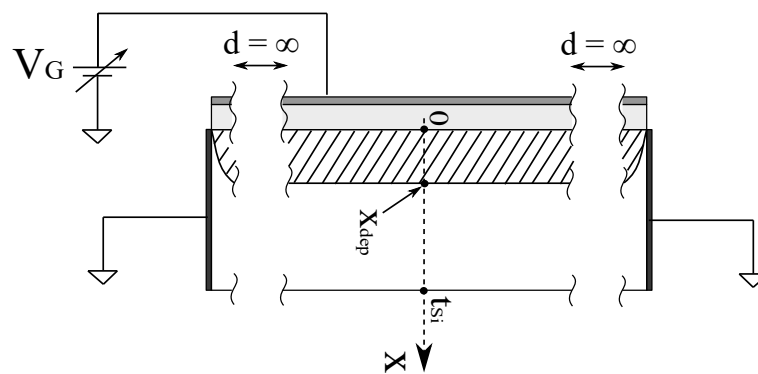


Figure A1. N-type PJLT ideal physical structure.

In this analysis, we assume that the PJLT device layer has been uniformly doped, which means that $N_D(x) = constant = N_D$. In addition, we assume that the drain and source terminals are sufficiently far from each other that the depletion region in the middle of the device layer can be considered flat or uniform. By using the previous assumptions, we can extract an analytical formula for the depletion region width by solving the Poisson equation, shown in Equation (A1):

$$\frac{d^2\phi(x)}{d^2x} = -\frac{\rho(x)}{\epsilon_{Si}} = -\frac{q(p_n(x) - n_n(x) + N_D^+(x))}{\epsilon_{Si}} \quad \forall x \in [0, X_{Xdep}], \tag{A1}$$

where: $\phi(x)$, $\rho(s)$, $n_n(x)$, $N_D^+(x)$ and $p_n(x)$ are the distribution of the electric potential, the distribution of the charge density, the distribution of the concentration of electrons, the distribution of the positive ion concentration due to the impurities in the substrate, and the distribution of the hole concentration, respectively, all evaluated along the symmetric axis of the transistor inside its depletion region. Furthermore, ϵ_{Si} is the dielectric constant of the silicon substrate and q is the elementary charge $\simeq +1.6 \times 10^{-19}C$. The concentrations $n_n(x)$ and $p_n(x)$ can be rewritten by using the Shockley Equations as shown in Equations (A2) and (A3):

$$n_n(x) = n_i e^{\frac{E_F - E_{Fi} + q\phi(x)}{k_B T}} = N_D e^{\frac{+q\phi(x)}{k_B T}} = N_D e^{\frac{+\phi(x)}{V_t}}, \quad (\text{A2})$$

$$p_n(x) = \frac{n_i^2}{n_n(x)} = \frac{n_i^2}{N_D} e^{-\frac{\phi(x)}{V_t}}, \quad (\text{A3})$$

where : E_F is the Fermi level of the doped semiconductor, E_{Fi} is the intrinsic Fermi level, n_i is the intrinsic concentration of electrons, and $V_t = k_B T/q$ is the thermal voltage. Unfortunately, by substituting Equation (A2) and (A3) in Equation (A1), we find that the Poisson equation cannot provide an analytical solution. Nevertheless, a common method to overcome this problem consists of using the hypothesis of complete depletion ($n_n(x) \simeq 0$ if $x \in [0, X_{dep}]$ and $n_n(x) \simeq N_D$ if $x \in [X_{dep}, t_{Si}]$), along with the hypothesis of complete ionization ($N_D^+ = N_D$) and negligible concentration of the minority carriers ($p_n(x) = 0$) during the whole operation of the transistor. In this case, the equation simplifies as shown in Equation (A4):

$$\frac{d^2\phi(x)}{dx^2} \simeq -\frac{qN_D}{\epsilon_{Si}}, \quad \forall x \in [0, X_{dep}]. \quad (\text{A4})$$

Finally, this approximated form of the Poisson equation can be analytically solved. From the Poisson Equation, we can extract Equation (A5), by using the known relation $-\nabla\Phi(x) = \vec{E}$:

$$\frac{dE_x(x)}{dx} = \frac{qN_D}{\epsilon_{Si}}. \quad (\text{A5})$$

Next, by integrating Equation (A5) once, we can find the general solution for the electric field inside the device layer shown in Equation (A6):

$$E_x(x) = \frac{qN_D}{\epsilon_{Si}}x + c_1. \quad (\text{A6})$$

By integrating Equation (A6) once more, we obtain the general solution for the electrical potential inside the device layer as shown in Equation (A7):

$$\phi(x) = -\frac{qN_D}{2\epsilon_{Si}}x^2 - c_1x + c_2, \quad (\text{A7})$$

where: c_1 and c_2 are arbitrary constants. To find the value of these two arbitrary constants, we need to define two boundary conditions. The first one can be found by evaluating the electric potential at the interface between the device layer and the thin gate insulating layer. This interface corresponds to the potential at $x = 0$. The electrical potential in this point is usually known as surface potential ϕ_s , which can be expressed as shown in Equation (A8):

$$\phi_s = V_G - V_{FB} - V_{OX}, \quad (\text{A8})$$

where: V_G is the electric potential at the gate terminal and V_{OX} is the drop voltage across the thin gate insulating layer. A useful formula of V_{OX} is shown in Equation (A9). This one can be calculated by integrating the electric field across the oxide, which separates the metal from the device layer:

$$V_{OX} = -\frac{qN_D}{C_{ox}} X_{dep}. \tag{A9}$$

On the other hand, the flat band voltage can be calculated by using the formula in Equation (A10) for an n-type PJLT and the formula in Equation (A11) for a p-type PJLT:

$$V_{FB,n} = q\Phi_M - q\Phi_{sn} = q\Phi_M - (q\chi + Eg/2 - q\Phi_n), \tag{A10}$$

$$V_{FB,p} = q\Phi_M - q\Phi_{sp} = q\Phi_M - (q\chi + Eg/2 + q\Phi_p), \tag{A11}$$

where: $q\Phi_M$ is the gate work function, $q\chi$ is the electron affinity, E_g is the energy band gap, and $q\Phi_{n,p}$ is the bulk potential that is defined as $k_B T \ln(N_{D,A}/n_i)$, k_B is the Boltzmann constant, and T is the temperature.

A second boundary condition can be found by introducing an additional approximation, which consists of assuming that the device layer behaves like an ideal conductor. If we consider the doping of the device layer sufficiently high to mimic the behavior of an ideal conductor, then we can assume that the electric field created by the gate electrode becomes zero ($E_x(X_{dep}) = 0$) at the boundary of the depletion region. In addition, the electric potential at the boundary of the depletion region is also zero because the device layer has been electrically grounded through the drain and the source terminal ($\phi(X_{dep}) = 0$). By using $\phi(x = 0) = \phi_s$ and $E(x = X_{dep}) = 0$, we can solve the system of equations shown in Equation (A12) [12]:

$$\begin{cases} E_x(x) = \frac{qN_D}{\epsilon_{Si}} x + c_1, \\ \phi(x) = -\frac{qN_D}{2\epsilon_{Si}} x^2 - c_1 x + c_2, \\ E(X_{dep}) = 0, \\ \phi(0) = \phi_s. \end{cases} \tag{A12}$$

The particular solutions of the system are shown in Equation (A13):

$$\begin{cases} E_x(x) = \frac{qN_D}{\epsilon_{Si}} (x - X_{dep}), \\ \phi(x) = \phi_s + \frac{qN_D}{\epsilon_{Si}} X_{dep} x - \frac{qN_D}{2\epsilon_{Si}} x^2, \end{cases} \tag{A13}$$

where the arbitrary constants were found to be : $c_1 = -\frac{qN_D}{\epsilon_{Si}} X_{dep}$ and $c_2 = \phi_s$. Finally, by evaluating the electric potential in $x = X_{dep}$ at which $\phi(X_{dep}) = 0$ and by using Equations (A8) and (A9) in Equation (A13), we can find the formula of the depletion region width shown in Equation (A14):

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{OX}} + \sqrt{\left(\frac{\epsilon_{Si}}{C_{OX}}\right)^2 - \frac{2\epsilon_{Si}}{qN_D} (V_G - V_{FB})}. \tag{A14}$$

A similar procedure can be used to derive the formula of the depletion region for a p-type PJLT. The formula for this case is shown in Equation (A15):

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{OX}} + \sqrt{\left(\frac{\epsilon_{Si}}{C_{OX}}\right)^2 + \frac{2\epsilon_{Si}}{qN_A} (V_G - V_{FB})}. \tag{A15}$$

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