Interleaved high gain DC-DC converter for integrating solar PV source to DC bus.

B.Sri Revathi[a]
PrabhakarMahalingam[a]
FranciscoGonzalez-Longatt[b]

[a]School of Electrical Engineering, Vellore Institute of Technology, Chennai Campus, Chennai, India

[b]Department of Electrical Engineering, Information Technology and Cybernetics, University of South Eastern Norway, Norway

Solar Energy, 188, 924-934.
DOI: http://dx.doi.org10.1016/j.solener.2019.06.072

Interleaved High Gain DC-DC Converter for Integrating Solar PV Source to DC Bus

B. Sri Revathi [1], Prabhakar Mahalingam [1*], Francisco Gonzalez-Longatt [2]
[1] School of Electrical Engineering, Vellore Institute of Technology, Chennai Campus, Chennai, India.
[2] Centre for Renewable Energy Systems Technology – CREST, Loughborough University, United Kingdom.
[*] Corresponding Author: prabhakar.m@vit.ac.in

Abstract: In this paper, a novel non-isolated DC-DC converter topology is proposed for solar photovoltaic (PV) application. The proposed converter is constructed from an interleaved boost converter (IBC) to reduce the input current ripple. Voltage gain is extended by (i) using voltage lift technique, (ii) replacing the conventional inductors of the IBC by coupled inductors with appropriate turns ratio and (iii) connecting a voltage multiplier cell (VMC) across the secondary windings of the coupled inductor (CI). As the voltage gain is extended mainly at the secondary side of the CIs, the switches are subjected to low voltage stress which is only 12.63 % of the output voltage. The converter yields a high voltage conversion ratio of 15.83. Experimental results obtained from a 24 V/380 V, 225 W prototype converter operating at 91.6 % efficiency serves as a proof of the presented concept which has been employed to achieve high voltage conversion ratio (15.83) with low input current ripple (20 %).

Keywords: Solar PV; renewable energy; DC-DC power converters; power electronics; power conversion.

1. Introduction

The ever-increasing electrical energy demand and the need to reduce carbon dioxide gas emission during the energy conversion process is forcing electrical energy planners to opt for renewable energy sources (RES). Among the available RES such as solar, wind and fuel cell (FC), solar energy is a promising source of electrical energy conversion [1]. Generally, the voltage output from PV panels is low; many panels need to be connected in series and/or parallel to meet the output voltage and power levels. However, due to partial shading conditions and low voltage output due to module mismatch or fault condition, an intermediate high gain DC-DC converter must be used as an interface between the PV source and the load [2].

In recent times, the concept of DC microgrids (μG) has been introduced to utilise RES and supplement the existing main grid efficiently; especially at remote localities [3]. μGs are attractive as electrification solution because of their ability to (i) easily incorporate RES, (ii) operate in grid-connected and standalone mode and (iii) the possibility of exporting power to the main grid or receiving it during heavy demand [3], [4]. Fig. 1 shows the illustrative block diagram of a DC-μG operating in standalone mode [5]. Conventional AC loads and variable frequency drives (VFDs)

are supplied through an inverter (DC-AC) while native DC loads, like LED lamps and electric vehicles (EV), are directly fed from the DC bus.

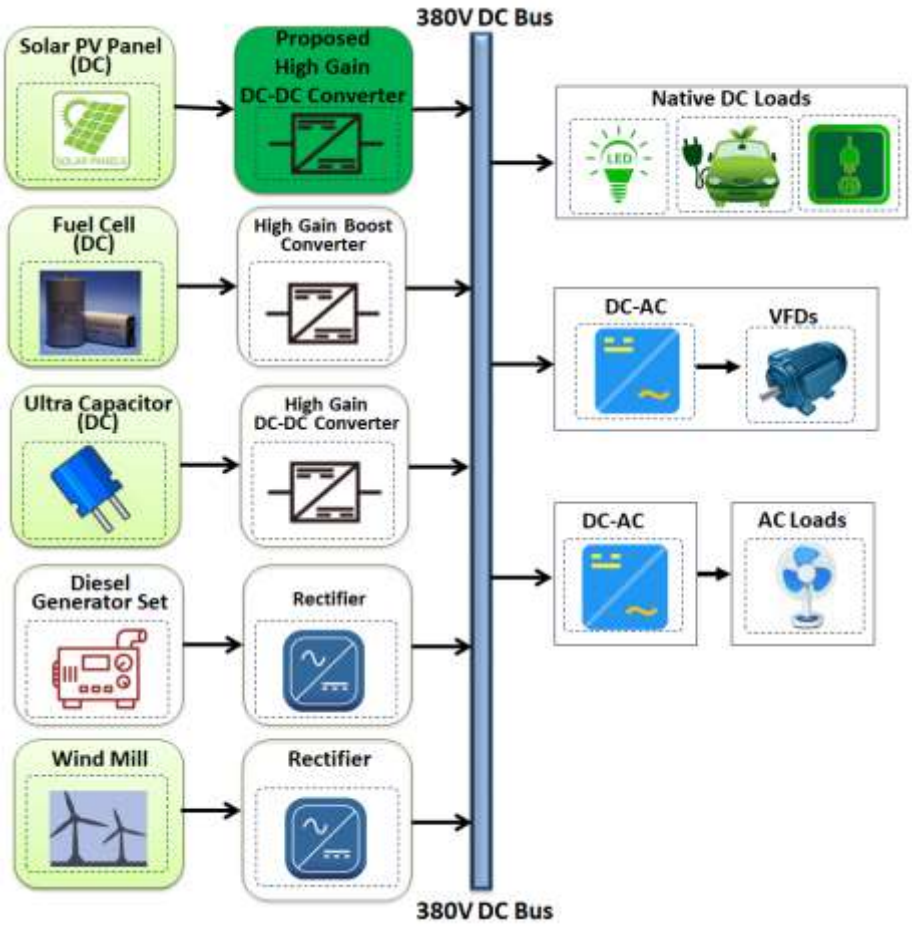


Fig.1. An illustrative block diagram of a DC microgrid operating in standalone mode [5].

The efficient operation of a DC-μG largely depends on the intermediate high step-up converter [6], [7]. During high step-up operation, a conventional boost converter (CBC) suffers from severe limitations like diode reverse recovery issue, and objectionably higher losses across the components used [8]. Non-isolated high gain DC-DC converter topologies easily overcome these drawbacks [8]-[12].

In [13], voltage multiplier cells (VMC) are employed in conjunction with a CBC to enhance the voltage gain and minimise the voltage stress across the power devices. In VMC based converters, many cells are required to achieve steep step-up ratios. Consequently, incremental power dissipation across additional components reduces the overall power conversion efficiency.

Quadratic boost converters (QBC) are obtained by judiciously cascading the well-known CBC structure; the output obtained from first CBC structure supplies the next CBC structure.

Consequently, the voltage gain of QBC is square of the voltage gain obtained from CBC. Unfortunately, the voltage stress experienced by the switch is same as the output voltage. therefore, when high voltage gain values are required, the switch stress is extremely high. Resultantly, the additional power dissipation across the switch due to the incremental voltage stress dissuades users from employing the QBC for practical applications which require voltage conversion ratios higher than 10.

The power handling capability of CBC and other derived converters is enhanced using an interleaved structure [14]-[17]. Since the total input current is shared between the interleaved phases, current stress on the semiconductor switch is reduced. Moreover, by appropriately phase-shifting the switches employed in each interleaved phase, the input current is smooth and free from ripples. However, the voltage gain of the IBC structure is constrained by the operating duty ratio of the switches and difficulties associated with extreme duty ratios.

To enhance the voltage gain of IBC and converters derived from interleaved structure, coupled inductors (CIs) are used instead of discrete inductors [18]-[23]. In CI based converters, voltage gain requirement is easily met by suitably adjusting the turns ratio of the CIs.

In [18], [19], voltage conversion ratio is extended by using diode-capacitor multiplier (DCM) cells. Though DCM based converters provide good voltage gain, the power handling capability of the power converter is restricted by the number of DCM cells. When the number of DCM cells is increased, the power dissipation across the additional components also increase. Consequently, the operating efficiency of the converter reduces. In [20], the super-lift technique is employed to achieve higher voltage conversion ratio. Though the converter yields a voltage gain of about 13, turns ratio of the CI is very high; the turns ratio value is 7. The magnetic element (CI) may be heavy and bulky when higher turns ratio value is adopted; the converter size may also increase.

In [21]-[23], CI based topologies with soft-switching capabilities are presented. The converter presented in [21] uses two CIs and yields a voltage gain of about 6.67 only. The converters presented in [22] and [23] offer a voltage gain of 10. Nevertheless, in the converter presented in [22], the switch is operated at a slightly higher duty ratio of D=0.7. The converter presented in [23] employs a CI with a marginally higher turns ratio of 4.

In this paper, a novel non-isolated DC-DC (niDC-DC) converter topology is proposed. The main novel contribution of the proposed paper is achieving a high voltage gain of about 15.83 by employing various gain extension techniques and judiciously connecting them. Consequently, the added advantageous features are (i) the higher voltage gain is achieved by operating the switches at a nominal duty ratio of D=0.5, (ii) the switches are subjected to very low voltage stress levels and (iii) ripple free input current is obtained by operating the interleaved phases. The structure of this paper is as follows: Section 1 provides a detailed introduction to the proposed concept. The structure of the proposed topology and its operating principle along with characteristic waveforms are described in Section 2. In Section 3, the design details and performance analysis of the

proposed converter are described. Experimental results obtained from a prototype converter are elaborated in Section 4 to substantiate the converter's performance. Salient features which are benchmarked with few state-of-the-art converters are detailed in Section 5 while the concluding remarks are presented in Section 6.

2. Proposed Converter and its Operating Principle

2.1. Circuit Description

Fig. 2 is used to illustrate the circuit topology of the proposed niDC-DC power converter. The proposed power converter consists of two main Stages. Stage 1 consists of a two-phase IBC with a voltage lift capacitor C_{Lift}, lift diode D_{Lift} and the primary windings of CIs namely L_{1P} and L_{2P}. Stage 2 consists of the gain extension network formed by the secondary windings (L_{1S}, L_{2S}) and one VMC comprising of DM1, DM2, CM1 and CM2. Diode D_0 and capacitor C_0 serve as the boost rectifier diode and output filter capacitor respectively.

2.2. Operating Principle

The operating principle is explained in four Modes and by considering the following valid assumptions: (i) all semiconductor devices and passive components are ideal and (ii) primary windings of the CIs, L_{1P} and L_{2P} are previously charged.

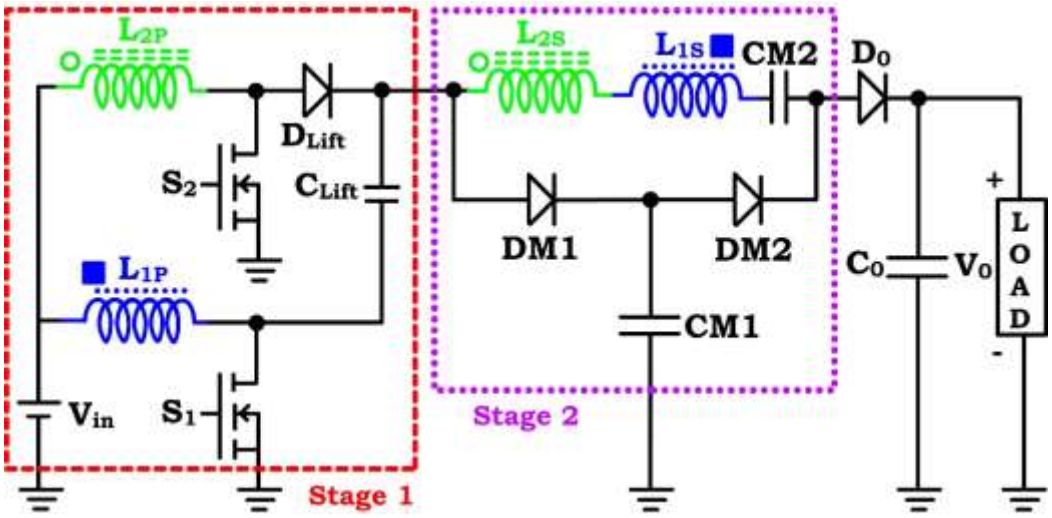


Fig.2. Power circuit diagram of the proposed non-isolated high step-up DC-DC converter with low input current ripple.

Mode 1: ($t_0 - t_1$)

At time $t = t_0$, switch S_1 is turned ON, and S_2 is switched OFF. Current through primary inductor L_{1P} raises linearly, and energy is stored across L_{1P}. As S_2 is OFF, stored energy in L_{2P} is transferred to C_{Lift} through D_{Lift}. In Stage 2, diode DM1 is forward biased and stored energy in the secondary windings L_{1S} and L_{2S} are transferred to CM1. As CM1 continues to charge, multiplier

diode DM2 remains in reverse bias condition. Mode 1 ends when the current through L_{2P} reaches zero and turns OFF D_{Lift}; while in Stage 2, CM1 is completely charged and reverse biases the multiplier diode DM1.

Current through the primary inductors L_{1P}, L_{2P}, C_{lift} and switch S_1 $\left(i_{L_{1P}}, i_{L_{2P}}, i_{C_{Lift}} \text{ and } i_{S_1}\right)$ is governed by (1) and (2).

$$i_{L_{1P}}(t) + i_{C_{Lift}}(t) = i_{S_1}(t) \tag{1}$$

$$i_{L_{2P}}(t) = i_{C_{Lift}}(t) + i_{DM1}(t) + i_{L_{2S}}(t) \tag{2}$$

Mode 2: ($t_1 - t_2$)

In Mode 2, the switches remain in their respective states similar to Mode 1. Inductor L_{1P} continues to store energy and current through L_{1P} continues to increase linearly. Voltage lift capacitor C_{Lift} begins to discharge and transfer its stored energy to Stage 2. In Stage 2, as CM1 is completely charged, the voltage developed across CM1 forward biases DM2. Resultantly, the energy stored in CM1 is transferred to the load through output diode D_0. Current through DM2 and inductor L_{2P} is given by (3) and (4).

$$i_{L_{1P}}(t) = i_{S_1}(t) + i_{C_{Lift}}(t) \tag{3}$$

$$i_{CM1}(t) = i_{DM2}(t) \tag{4}$$

As CM1 continues to discharge, its potential keeps reducing. At the end of Mode 2, the potential across CM1 is just not enough to sustain DM2 in the ON state. Thus, DM2 turns OFF at time $t=t_2$ (end of Mode 2).

Mode 3: ($t_2 - t_3$)

Mode 3 commences at time $t=t_2$ when switch S_1 is turned OFF, and S_2 is switched ON. As S_1 is turned OFF, the energy stored in L_{1P} begins to get transferred to C_{Lift} and CM1 (through diode DM1). Consequently, the current through L_{1P} begins to decrease linearly. As S_2 is ON, inductor L_{2P} starts to charge linearly towards the supply voltage and current through L_{2P} raises linearly. As S_2 is conducting, voltage lift diode D_{Lift} is reverse biased. As CM1 is slightly discharged during the previous mode and L_{1P} begins to transfer its stored energy, DM1 is forward biased and helps in transferring the stored energy across CM1 (charging CM1). As CM1 is charging, DM2 remains in reverse biased state. Mode 3 comes to an end at time $t=t_3$ when CM1 is ultimately charged, and the potential built up across CM1 is sufficient enough to turn OFF DM1. The equations that govern Mode 3 are given by (5) and (6).

$$i_{L_{1P}}(t) = i_{C_{Lift}}(t) \tag{5}$$

$$i_{L_{2P}}(t) = i_{S_2}(t) \tag{6}$$

Mode 4: ($t_3 - t_4$)

During Mode 4, switches are retained in their respective states as in Mode 3. At time $t=t_3$, L_{1P} is completely discharged. However, the energy stored across C_{Lift} is transferred to Stage 2 through the continuity provided by L_{1P} and the elements located in Stage 2. (The continuity is indicated as a dark grey line in Fig. 3(d))). The primary winding of coupled inductor L_{2P} continues to store energy since S2 remains ON. In Stage 2, multiplier capacitor CM1 transfers its stored energy to the load through DM2 (similar to Mode 2). Mode 4 ends at $t = t_4$ when CM1 is discharged and reverse biases DM2. During Mode 4, the governing equation is expressed as (7).

$$i_{L_{2P}}(t) = i_{S_2}(t) \tag{7}$$

Turning ON S_1 again marks the beginning of next switching cycle. Figs. 3(a)-(d) show the equivalent circuits in various modes while Fig. 4 shows the waveforms pertaining to key parameters of the presented converter.

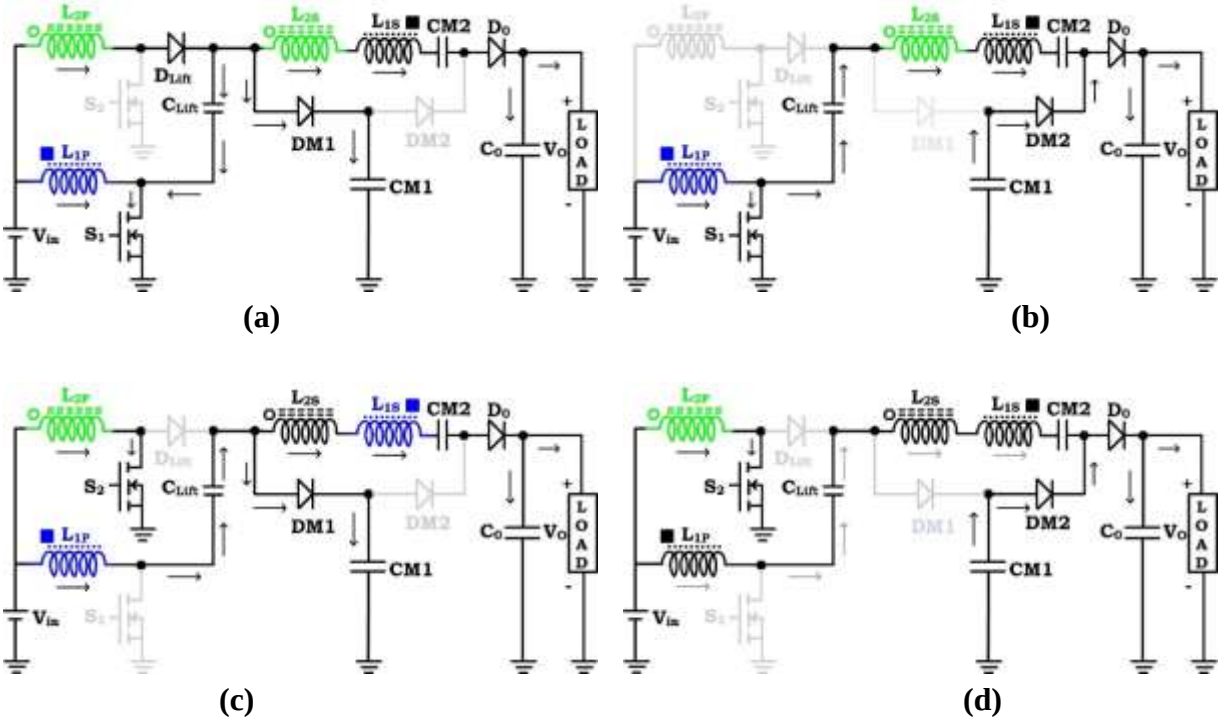


Fig.3. Equivalent circuit of the proposed niDC-DC converter during (a) Mode 1, (b) Mode2, (c) Mode 3 and (d) Mode 4.

3. Steady-state analysis and design details

3.1 Voltage Gain

Stage 1 of the proposed converter operates precisely similar to an IBC. Due to C_{Lift}, the voltage induced in L_{1P} gets added up with the voltage developed across L_{2P} and C_{Lift}. Therefore, at the end of one switching cycle, the voltage across C_{Lift} (Stage 1) is given by (8).

$$V_{Stage\ 1} = V_{C_{Lift}} = \frac{2}{1-D} V_{in} \quad (8),$$

where D is the duty ratio of the switches S_1 and S_2.

During Mode 2, S_1 is ON, and S_2 is OFF. Stored energy in inductors L_{1P} and L_{2P} and the multiplier cell elements contribute to the load voltage. The output voltage is expressed as

$$V_0 = V_{C_{Lift}} - V_{L_{2S}} + V_{L_{1S}} + V_{CM2} \quad (9).$$

At the end of Mode 3, the voltage across multiplier capacitor CM1 is same as output voltage V_0. Consequently, the left side terminal of L_{2S} is at a potential of V_0. As output diode D_0 conducts, the voltage at one plate (right side plate) of multiplier capacitor CM2 is held at V_0.

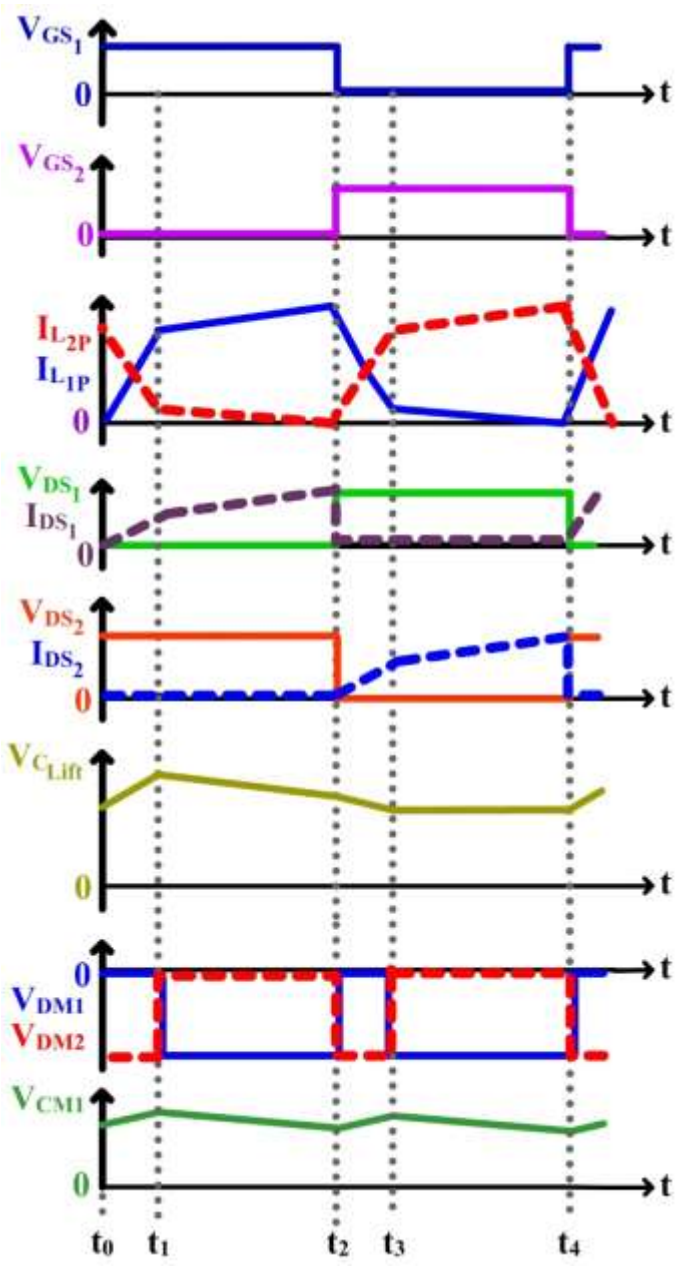


Fig.4. Characteristic waveforms showing the key parameters of the proposed niDC-DC converter for one switching cycle.

Equating the two potential using the loop formed by L_{2S}, L_{1S} and CM2, the voltage developed across multiplier capacitor CM2 (Stage 2) is derived as

$$V_{Stage\ 2} = V_{CM2} = V_{L_{2S}} + V_{L_{1S}} \quad (10).$$

By substituting the voltage induced across the secondary windings,

$$V_{Stage\ 2} = V_{CM2} = \frac{2N}{1-D} V_{in} \quad (11),$$

where N is the turns ratio of the CIs.

Substituting (10) in (9), the output voltage is given by

$$V_0 = V_{C_{Lift}} + 2V_{L_{1S}} \quad (12).$$

Recognising that the voltage induced across the secondary winding L_{1S} is turns ratio (N) times the voltage obtained from a classical boost converter, the expression for output voltage is obtained. Alternatively, using (8) and (11), the voltage gain (M) of the proposed converter is derived as

$$M = \frac{V_0}{V_{in}} = \frac{2+2N}{1-D} \quad (13).$$

Equation (13) provides the expression for ideal voltage conversion ratio. By considering k as the average coupling coefficient value of the two CIs, the realistic voltage gain is

$$M = \frac{V_0}{V_{in}} = \frac{2+2Nk}{1-D} \quad (14).$$

Fig. 5 shows the voltage gain plot obtained from (14) considering ideal coupling (k=1), and for various values of N. The proposed niDC-DC converter is intended for a DC-μG which operates at a standard DC voltage of 380 V from a 24 V DC input. The required voltage gain is about 15.833 based on the input-output voltage specifications. In the proposed niDC-DC converter, to meet the voltage gain requirement, either the turns ratio or the duty ratio can be varied. However, when the switches operate at extreme duty ratios, the power loss across the semiconductor devices is very high [8]. Hence, in the proposed niDC-DC converter, turns ratio N is adjusted to achieve the required high voltage gain of about 15.833 at a moderate duty ratio of D=0.5.

For a particular turns ratio value, when k varies, the voltage gain also varies. Considering the wide variations in k and D, the changes in voltage gain values are negligible as depicted in Fig. 6. Therefore, even though CIs with actual coupling coefficients less than 1 are practically employed, the required voltage conversion ratio value is expected to be obtained under test condition. In the proposed niDC-DC converter, CIs are designed carefully, and the value of k is experimentally determined to be 0.95 which is very close to the ideal value.

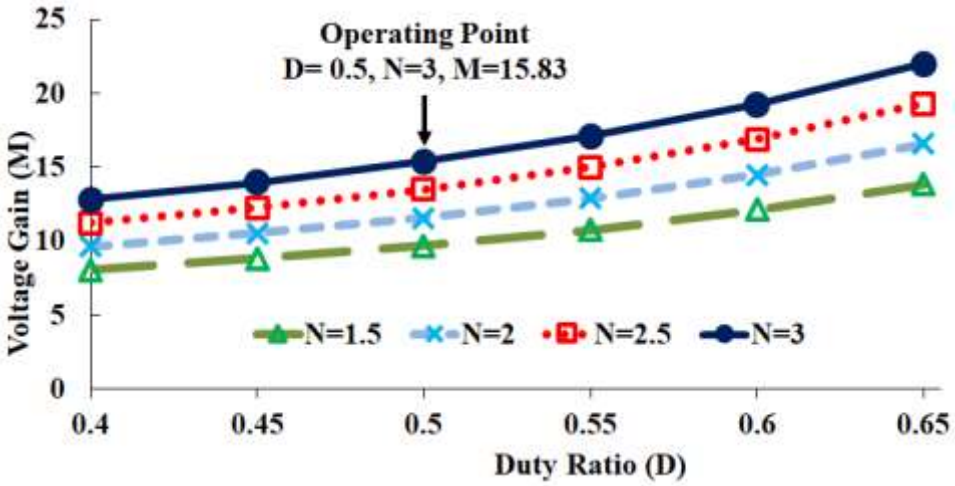


Fig.5. Plot of voltage gain (*M*) of the proposed niDC-DC converter for various values of *D* and *N* when *k*=1.

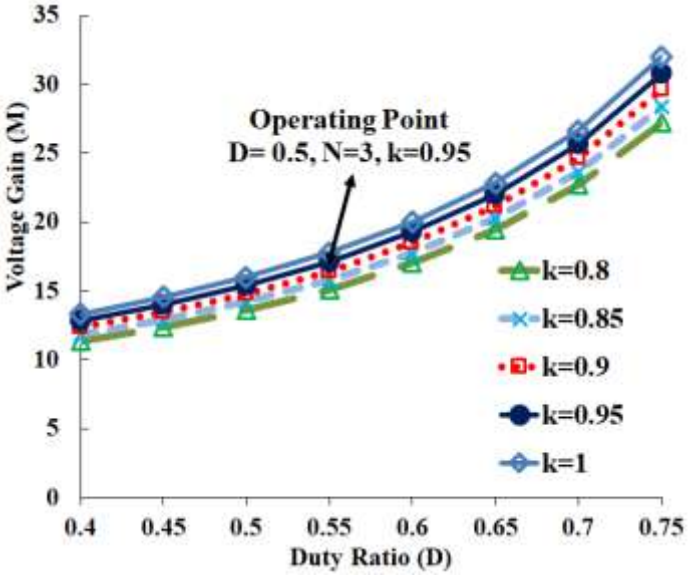


Fig.6. Plot depicting the change in voltage gain of the proposed niDC-DC converter when *D* and *k* are varied while maintaining *N* = 3.

3.2. Voltage Stress on Semiconductor Devices

In the proposed niDC-DC converter, the switches S_1 and S_2 are located in Stage 1. Since Stage 1 operates similar to an IBC, the voltage stress on S1 and S_2 is given by

$$V_{S_1} = V_{S_2} = \frac{1}{1-D} V_{in} = \frac{V_0}{2+2Nk} \quad (15).$$

The voltage stress on S_1 and S_2 is only a fraction of the voltage at the output. Consequently, switches with low voltage rating are used to minimise the conduction losses. The potential difference across D_{Lift} is given by

$$V_{D_{Lift}} = \frac{2}{1-D} V_{in} = \frac{V_0}{1+Nk} \quad (16).$$

The voltage stress on multiplier diodes DM1 and DM2 is obtained by considering the reverse voltage developed across their anode and cathode terminals when DM1 is OFF. Thus, voltage stress on the multiplier diodes is derived as

$$V_{DM1} = V_0 - V_{C_{Lift}} = \frac{2Nk}{1-D} V_{in} \quad (17).$$

$$V_{DM2} = V_0 = \frac{2+2Nk}{1-D} V_{in} \quad (18).$$

3.3. Current Stress on Semiconductor Devices

Stage 1 of the proposed niDC-DC converter is similar to an IBC. Therefore, the input current is shared by the two switches used in Stage 1. The RMS value of currents flowing through the switches S_1 and S_2 are given by

$$I_{S_1} = I_{S_2} = \frac{I_{in}}{2} \quad (19).$$

Though the overall structure of Stage 1 is slightly asymmetrical due to the employment of voltage lift technique using C_{Lift}, the overall performance of the converter remains largely unaltered. The RMS value of current stress on D_{Lift} will be same as the current through S_2. Thus,

$$I_{D_{Lift}} = I_{S_2} = \frac{I_{in}}{2} \quad (20).$$

Since the multiplier diodes, *DM1* and *DM2* are located in Stage 2, they are subjected to a slightly reduced current stress given by

$$I_{DM1} = \frac{1-D}{2} I_{in} \quad (21).$$

$$I_{DM2} = \frac{1-D}{2+2nk} I_{in} \quad (22).$$

The output diode D_0 is rated to carry a current which is equal to output current I_0. Hence, the current stress of diode D_0 is given by

$$I_{D_0} = I_0 \quad (23).$$

3.4. Design of Primary Inductors and Turns Ratio

The primary inductors L_{1P} and L_{2P} store energy when the switches are turned ON and then transfer the stored energy thereby contributing to the required voltage gain. Further, the current ripple at the input is based on the design of magnetic elements. Thus, L_{1P} and L_{2P} are designed based on (24).

$$L_{1P} = L_{2P} = \frac{V_{in} D}{2 f_s \Delta i_{in}} \tag{24}$$

where f_s is the switching frequency and 'Δi_{in}' represents the input current ripple.

The turns ratio (N) of CIs is obtained based on the values of the voltage gain (M) and primary inductances. The voltage stress on the semiconductor devices is also dependent on the chosen value of N as observed through (15)-(18). Hence, to reduce the voltage stress, the value of N is carefully calculated using (25).

$$N = \frac{M(1-D)-2}{2k} \tag{25}$$

Output capacitor value C_0 is determined from duty ratio D, output current I_0, output voltage ripple Δv_0 and the switching frequency f as

$$C_0 = \frac{DI_0}{f \Delta v_0} \tag{26}.$$

4. Experimental Results and Discussion

This section is dedicated for verifying the performance of the proposed niDC-DC converter and its concept. A hardware prototype is fabricated and tested, the parameters and specifications of the implemented prototype are shown in Table 1. PIC18F45k20 microcontroller is programmed suitably to obtain two gate pulses at the required duty ratio of D=0.5, the switching frequency f_s = 50 kHz and 180° phase-shift. The two gate pulses are optically isolated using TLP250 and then applied as an input to IR25600 gate driver IC. The driver IC is configured to provide two low side outputs. The outputs obtained from the gate driver IC are applied to the gate terminals of S_1 and S_2. Tektronix 4-channel digital storage oscilloscope (DSO – TPS2024B) is used along with standard accessories like high voltage and current probes to obtain the required output waveforms. Table 2 shows the list of components used to construct the prototype version of the proposed niDC-DC converter.

Fig. 7(a) shows a screen capture of the waveforms obtained from the digital storage oscilloscope (DSO), the signals corresponding to the input voltage, gate pulses and the output voltage. When the switches S_1 and S_2 are switched at a 50 kHz frequency, operated with D=0.5, and phase-shifted by 180°, an output voltage of 380 V is obtained from the 24 V input. The voltage conversion ratio matches with the expected value of 15.833. The results obtained from the real niDC-DC converter implementation allow validating the adapted gain extension technique.

Table 1 Specifications of the proposed converter

Parameters	Value
Input voltage, (V_{in})	18 V-24 V
Output voltage, (V_0)	380 V
Output power, (P_0)	225 W
Switching frequency, (f_s)	50 kHz
Turns ratio (N)	3.0
Primary inductors (L_{1P}, L_{2P})	60 μH
Secondary inductors (L_{1S}, L_{2S})	540 μH
Coupling coefficient (k)	0.95
Input ripple current (Δi_{in})	2.00 A

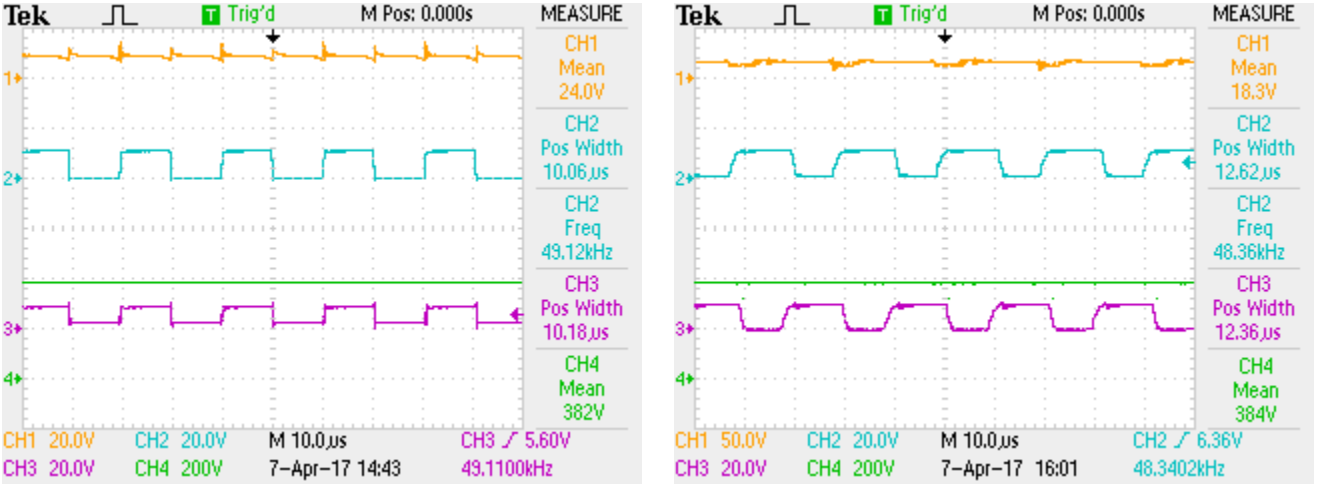
Table 2 Details of the components employed in the proposed converter

Element	Part number	Ratings
S_1, S_2	PSMN6R5-80PS	80 V, 100 A, 6.9 mΩ
D_{Lift}	MBR1660	600 V, 16 A, 0.75 V
DM1, DM2, D_0	MUR460	600 V, 4 A, 1.05 V
C_{Lift}	ECQ-E2106JF	10 μF, 250 V, polyester
CM1	ECW-FD2W475J	4.7 μF, 450 V, polypropylene
CM2	UVR2E100MPD1TD	12 μF, 250 V, electrolytic
C_0	MCKSK400M470I30S	47 μF, 400 V, electrolytic

To verify the voltage gain capability of the proposed niDC-DC converter and its deployment for solar PV applications (wherein the input voltage varies due to variable solar irradiation levels), experiments are conducted when the input voltage is 18 V. Fig. 7(b) shows the waveforms (obtained during experimentation) representing input voltage, gate pulses and output voltage when the input voltage is 18 V. The switches are operated at D=0.63 to meet the required 380 V output. The proposed niDC-DC converter delivers the expected output voltage at the designed power level when the input voltage fluctuates from 18 V to 24 V. Therefore, the proposed converter is an appropriate choice for connecting the PV source to the 380 V DC bus.

To comprehend and verify the gain extension mechanism used in the proposed converter, voltage waveforms at key points are captured and presented in Fig. 8. The voltage gain increment due to voltage lift technique and VMC network connected across the secondary winding of the CIs is validated. Voltage lift capacitor C_{Lift} is located at Stage 1. The voltage developed across the plates of C_{Lift} equal to that of the output from a classical boost converter (CBC) or an interleaved boost converter (IBC). Therefore, when S_1 and S_2 are operated at D=0.5, the voltage across C_{Lift} is close to 48V. Due to voltage lift technique, the voltage obtained from Stage 1 (potential difference between the top plate of C_{Lift} and ground) is twice that of a CBC. The

experimental value of voltage developed across Stage 1 is very close to four times the input voltage magnitude as predicted through (8). In Stage 2, further gain enhancement occurs, and the practical magnitude of load voltage matches with the predicted value of 380 V. Thus, the progressive increment in voltage gain is verified through experiment.



(a) **(b)**

Fig.7. Experimental waveforms obtained from the oscilloscope to demonstrate the voltage conversion ratio when the input voltage is (a) 24 V and (b) 18 V; waveforms represent input voltage (CH1), gate pulses to S_1 and S_2 (CH2, CH3) and output voltage (CH4).

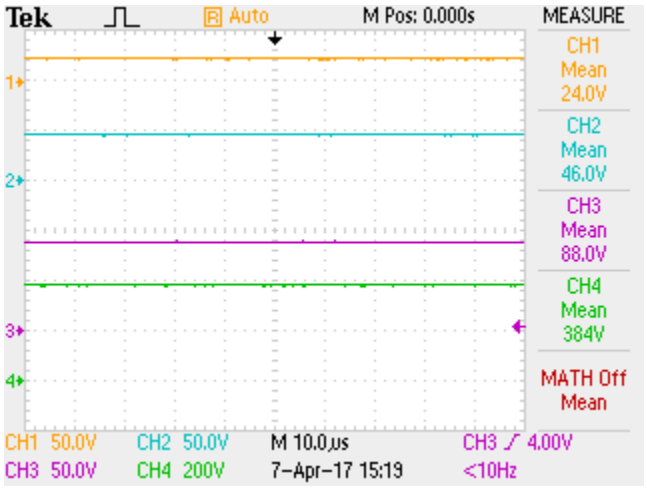
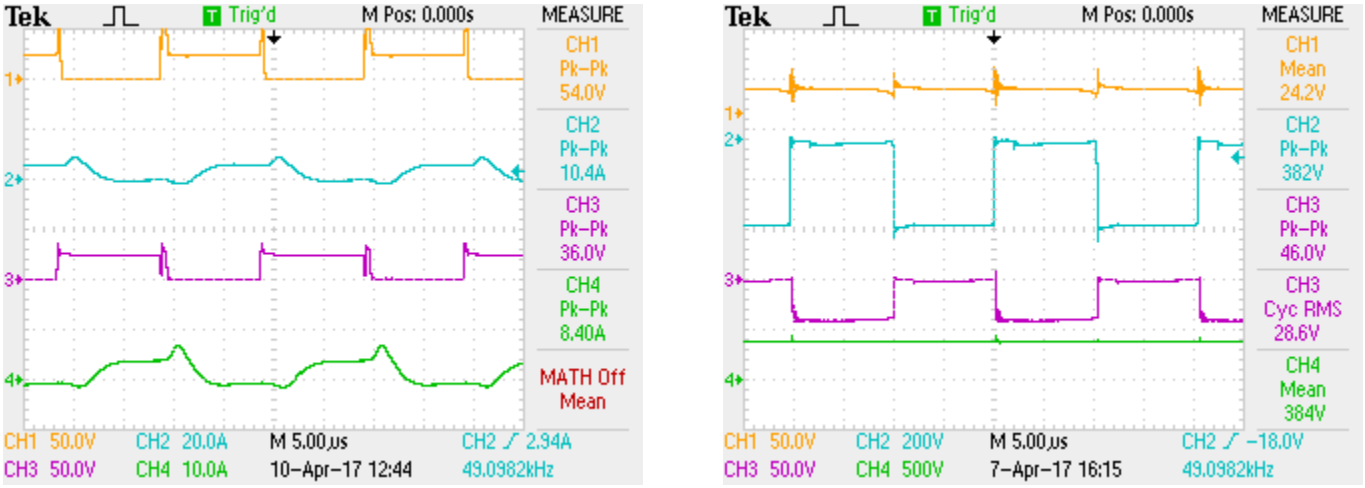


Fig.8. Experimental waveforms showing gain extension at various stages; input voltage (CH1), the voltage across the plates of C_{Lift} (CH2), the voltage across Stage 1 (CH3) and output voltage (CH4).

The practical waveforms of voltage and current stress on S_1 and S_2 are depicted in Fig. 9(a). The switches operate complimentary with one another and help to charge and discharge the primary winding of coupled inductors. Consequently, the CIs contribute to higher voltage gain at the output. The energy stored in the leakage

inductance of the CIs are recycled within the VMC network which is connected across the secondary windings. Resultantly, voltage spikes across the switches are suppressed. As the switches are employed in Stage 1, the voltage stress on the switches is only 48 V for a 380 V output. The magnitude of switch voltage stress works out to only 12.63 % of the output voltage and is in accordance with the theoretical value predicted using (15).



(a) **(b)**

Fig.9. (a) Practical oscilloscope waveforms showing the voltage and current stress experienced by switches; the voltage across S_1 (CH1), the current through S_2 (CH2), the voltage across S_2 (CH3) and current through S_1 (CH4), (b) Oscilloscope waveforms obtained from the experimental setup showing the voltage stress experienced by diodes compared with output voltage; the input voltage (CH1), the voltage across DM2 (CH2), voltage stress on D_{Lift} (CH3) and the output voltage V_0 (CH4).

The practical waveforms of the voltage at the input port, voltage stress across diodes D_{Lift} and DM2 are compared with the output voltage as shown in Fig. 9(b). The diodes operate complimentary with one another resulting in charging and discharging the multiplier capacitors. Thereby, the multiplier capacitors contribute to enhancing the voltage gain at the output. As the voltage lift diode D_{Lift} is placed in Stage 1, the voltage stress across it is 96 V for a 24 V input. However, the multiplier diode DM2 experiences voltage stress which is equal to output voltage V_0.

Fig. 10 shows the behaviour of current measured through the primary windings L_{1P}, L_{2P}, input terminal and the output port. As an interleaved structure is used and the switches are phase-shifted by 180°, the current flowing through the primary inductors of CIs are complimentary in nature. This confirms the fact that when one inductor charges, the other discharges. The mean value of current magnitudes is slightly different because of the asymmetrical structure. The asymmetry is due to the introduction of C_{Lift} which aids to enhance the voltage gain without affecting the overall performance of the presented converter.

The magnitude of input current shows that the total current at the input is shared by the two CIs. Resultantly, the inductors need to be rated to carry a lesser current as compared with other classical (non-interleaved) high gain converters. Though current through L_{1P} and L_{2P} individually seem discontinuous, the total input current is continuous. Moreover, the input ripple current magnitude is reduced by operating the interleaved legs at D= 0.5 with 180° phase-shift. Thus, an interleaved structure at the input side not only helps in reducing the current ripple but also aids in using smaller sized magnetic elements.

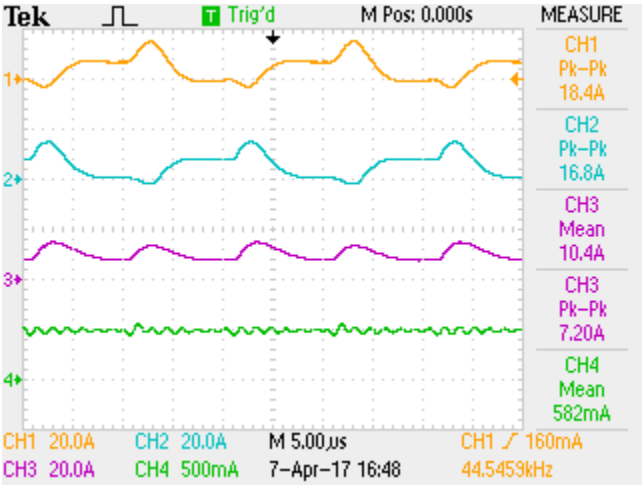


Fig.10. Practical waveforms showing current through the primary winding of CIs L_{1P} (CH1) and L_{2P} (CH2), input current (CH3) and output current (CH4).

Fig. 11 shows the oscilloscope waveforms used to compute the converter efficiency when it operates at full load condition. Using the practical values displayed in the oscillogram, the efficiency is computed to be 91.6 % at full load condition. The efficiency values under simulated and practical conditions match very closely with each other. Under the experimental condition, the losses occurring in the semiconductor devices and stray resistance of the CIs account for about 8.4 % of the total power. However, during simulated condition, losses due to the stray resistance of the CIs are absent which results in marginal incremental efficiency under simulated condition.

The loss occurring across the elements employed in the niDC-DC converter is computed using (27)-(29).

$$P_{switch\_loss} = I^2_{switch\_RMS} \times R_{switch\_ON} + P_{switch\_ON} + P_{switch\_OFF} \quad (27)$$

$$P_{diode\_loss} = V_{diode\_ON} \times I_{diode\_Avg} + I^2_{diode\_RMS} \times R_{diode} \quad (28)$$

$$P_{CI\_loss} = I^2_{py} \times R_{py} + I^2_{sy} \times R_{sy} + P_{iron} \quad (29)$$

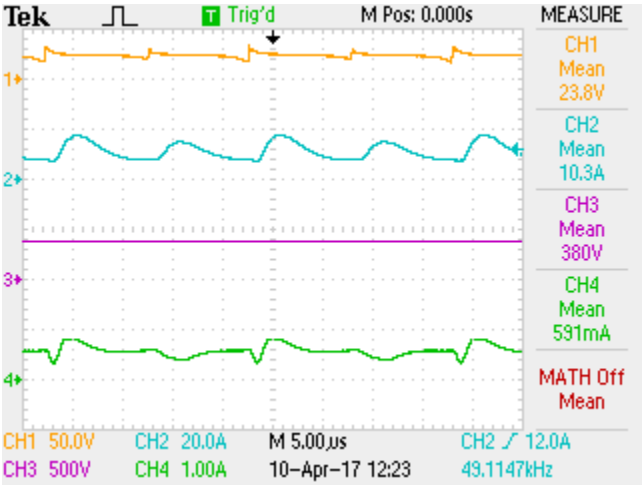


Fig.11. Waveforms obtained from the experimental setup to compute the efficiency of the proposed converter under full-load condition; input voltage (CH1), input current (CH2) output voltage (CH3) and output current (CH4).

Parameters like V_{diode_ON}, R_{switch_ON}, R_{diode} and P_{iron} are obtained from the manufacturers' datasheet, and the loss across individual components are computed. Fig 12 shows the loss distribution profile of the proposed niDC-DC converter under full load condition. As the voltage rating of switches is reduced due to the gain extension technique employed, the conduction losses on the switches are minimum (about 13.6 % of total loss). The loss occurring across the four diodes are about 23.2 % of the total loss. Higher voltage rating and forward voltage drop result in higher loss across diodes. The power loss occurring across the CIs is mainly due to the stray resistance of the windings and the loss of the magnetic core. As the CIs are designed to carry the full load current, the stray resistive loss is higher and is reflected as the significant loss contributor (31.6 % of total loss). By careful choice of magnetic core and placement of windings, the loss due to CIs may be brought down. The loss due to electrical series resistance (ESR) of capacitors, the stray resistance of the tracks used in the printed circuit board (PCB) and conducting wires are minimum and account for 1.5 % of the total losses.

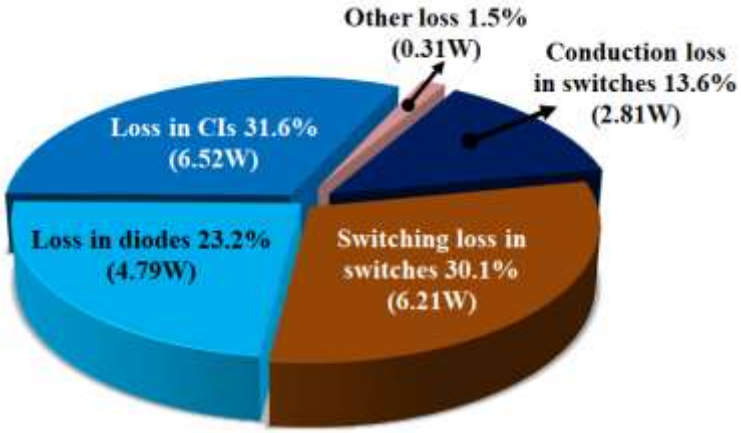


Fig.12. Loss distribution profile of the proposed niDC-DC converter.

Fig. 13 shows the efficiency curve of the proposed converter under simulated and practical conditions. The efficiency values under simulation and experimentation are very close to each other; the difference in the values is mainly due to the stray resistance of passive elements and leakage loss occurring across the CIs.

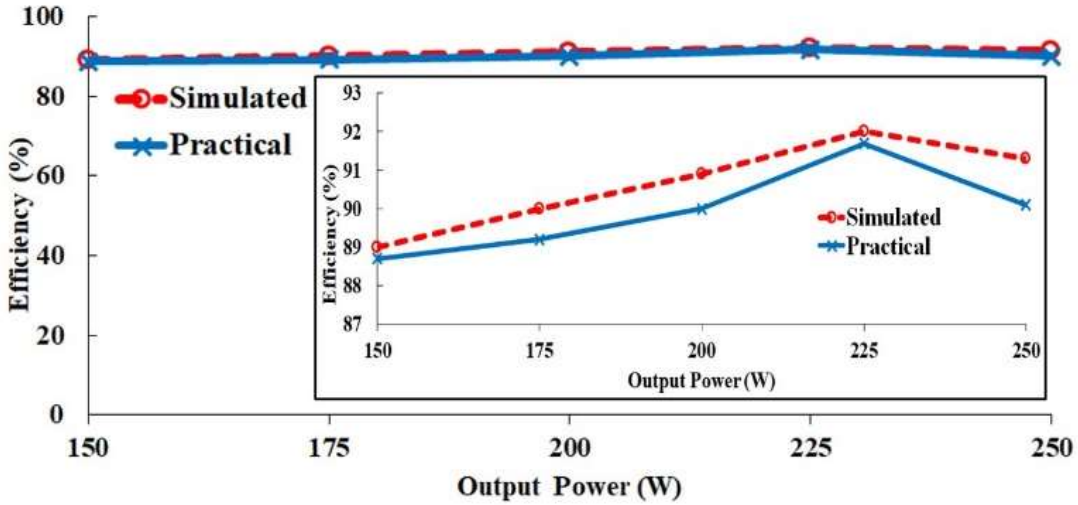


Fig.13. Efficiency curve of the proposed niDC-DC converter under simulated and practical conditions. Inset shows the magnified view of the curve.

Fig. 14 shows the photograph of the experimented converter. The magnetic elements have been accommodated in the PCB. To observe the current through the primary windings, provisions are provided which are shown as small wire loops (red colour). The overall dimension (length×width×height) of the converter is 200 mm×115 mm×45 mm.

Fig.14. Photograph showing the top-view of the implemented niDC-DC converter.

5. Comparison of the proposed niDC-DC converter with some state-of-the art converters

Some salient features of the proposed niDC-DC converter are compared with basic CBC and the QBC presented in [new ref]. Table 3 shows the main attributes that are compared.

Table 3. Comparison between the proposed converter and some basic boost derived converters.

Attributes	**CBC**	**QBC in [new Ref]**	**Proposed niDC-DC converter**
Voltage gain expression	$\frac{1}{1-D}$	$\frac{1}{(1-D)^2}$	$\frac{2+2Nk}{1-D}$
Voltage gain (M) at D=0.5	2	4	15.83
Voltage stress on switch (V_{switch}) expressed as % of V_0	100	100	12.63
No. of switches	1	1	2
Component count (CC)	4	8	12
M/CC	0.5	0.5	1.3191
M/V_{switch}	0.02	0.04	1.2533

In comparison with the CBC and QBC, the proposed converter offers a higher voltage gain at a nominal duty ratio of D=0.5. Further, due to the gain extension technique that is implemented, the switches employed in the proposed niDC-DC converter are subjected to the least voltage stress. Consequently, the ratio of voltage gain to component count (M/CC) translates to be the highest. The fact that the proposed converter offers the highest voltage gain with least voltage stress on the switches is reflected through the highest M/V_{switch} value for the proposed niDC-DC converter; the M/V_{switch} values for CBC and QBC are negligible.

To appreciate the beneficial features of the proposed niDC-DC converter, three CI based high-gain converters are chosen and compared with the proposed converter. Table 4 shows the primary attributes that are considered for comparison and the source of information.

5.1. Voltage Gain (M)

Among the three converters considered for comparison presented in [21]-[23], the proposed niDC-DC converter provides the highest voltage gain of 15.83. Usage of CI, voltage lift technique and VMCs results in higher voltage gain at a moderate duty ratio of *D*=0.5. The converters in [21]-[23] use use CI with appropriate turns ratio. Consequently, the voltage conversion ratio of those converters is moderate when compared with the proposed niDC-DC converter which uses CI and other hybrid gain extension techniques. Fig. 15 provides a graphical comparison of voltage gain values that are obtained in the four converters considered for comparison.

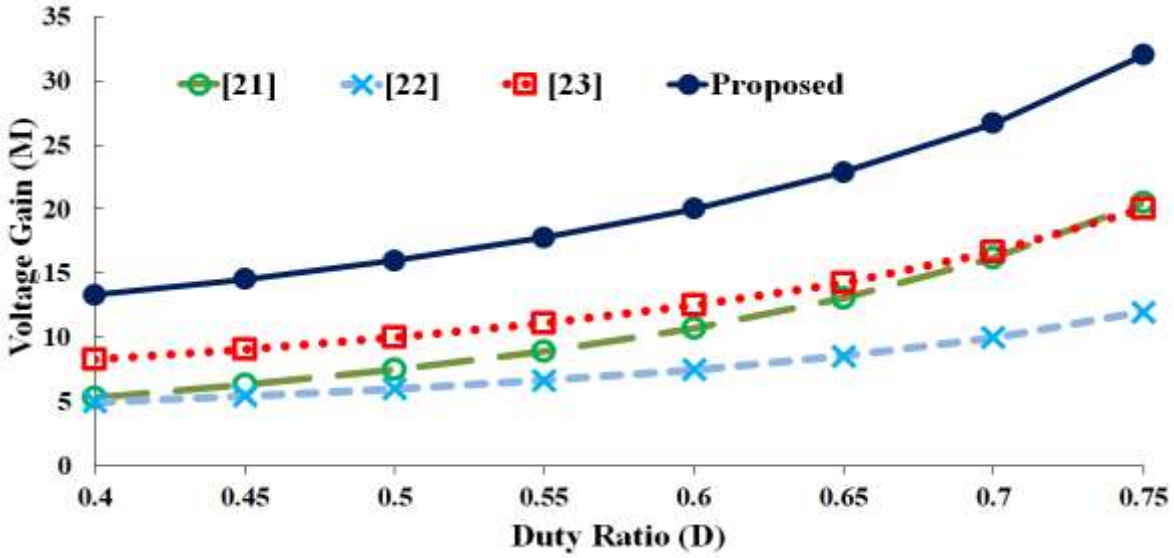


Fig.15. Plot showing the voltage gain of the converters compared in Table 4.

5.2. Number of CIs and their Turns Ratio

Converter presented in [21] uses only one CI with two secondary windings. The turns ratio of the secondary windings is maintained at 1.5 and 4 to achieve the required voltage conversion ratio. In [23], one CI with a turns ratio of 4 was used to obtain a voltage gain of 10. In [22] and the proposed converter, two CIs are used. In [22], the turns ratio is kept at 0.5, and duty ratio iss adjusted to 0.67 to meet the voltage gain requirement. In the proposed converter, since an interleaved structure is used, duty ratio iss fixed at 0.5 to minimise the input current ripple, and CIs with a turns ratio of 3 are used to achieve a higher voltage gain of 15.83.

5.3. Voltage Stress on Semiconductor Devices and Component Count

Converter presented in [21] and [23] uses eight components. Twelve components are used in the proposed niDC-DC converter and the one presented in [22]. In [22], active clamping technique is used to achieve soft-switching. Resultantly, two additional switches are required. The voltage stress on the main switches used in [22] is higher as the gain extension is mainly achieved by adjusting the duty ratio of the switches. In [21], as the turns ratio of the CIs were adjusted to obtain the required voltage gain, the voltage stress on the switch is slightly reduced compared to [22]. A buffer capacitor along with CI is used to extend the voltage gain of the converter presented in [23]. Hybrid combinations of CI, voltage lift technique, use of VMC at the secondary side of the CIs are used as gain extension mechanisms in the proposed niDC-DC converter. Further, the duty ratio of the switches is maintained at D=0.5 to reduce current ripple at the input side. Therefore, the voltage stress impressed across the switches in the proposed converter is considerably reduced compared to the other converters considered for comparison. Considering the highest voltage gain achieved with the lowest voltage stress on the switches, the proposed niDC-DC converter is an excellent choice for integrating the PV source.

5.4. Ratio of Voltage Gain to Component Count (M/CC)

To appreciate the high voltage gain capability of the proposed niDC-DC converter, the ratio of voltage gain (M) versus component count (CC) is considered as an index. The M/CC value is the highest for the proposed converter; employing 12 components is justified considering the higher M/CC value. Other converters that are compared yield lower voltage gain values only. Consequently, the M/CC value is lower for the other state-of-the art converters considered for comparison.

5.5. Ratio of Voltage Gain to Voltage Stress on the Switch (M/V_{switch})

Voltage stress impressed across the switch employed in a converter plays an important role in determining the operating efficiency. To obtain a fair idea on the voltage stress magnitude of all the converters that are compared, the ratio of voltage gain to voltage stress on the switch (expressed as a % of V_0) is obtained and indicated as M/V_{switch}. The M/V_{switch} value of the proposed niDC-DC converter (1.2533) is much higher than the other three converters. In fact, the M/Vswitch value is about 2.5 times higher than the second highest value which is 0.5 for the converter presented in [23]. The low M/Vswitch value obtained for converters presented in [21] and [22] clearly indicate the fact that the switches used are subjected to considerably higher voltage stress levels as compared to their respective voltage gain magnitudes. Thus, the proposed niDC-DC converter possesses the advantage of yielding higher voltage gain while its switches are subjected to very low stress level.

Table 4. Performance comparison between the proposed converter and some CI based high gain converters.

Attributes	**Converters presented in references**			
	[21] Zhangyong Chen	**[22]** Musbahu	**[23]** Moumita	**Proposed niDC-DC converter**
Input voltage, V_{in} (V)	30	12-14	25-50	24
Output voltage, V_0 (V)	200	120	450	380
Voltage gain, M	6.67	10	10	15.83
Power rating, P_0 (W)	100	500	400	200
Duty ratio, D	0.47	0.7	0.5	0.5
No. of CIs	1 CI (2 secondary windings)	2	1	2
Turns ratio, N	1.5 and 4	0.5	4	3
Gain extension method	Turns ratio of CI	Turns ratio of CI	CI with buffer capacitor	CI, voltage lift capacitor, and VMC
Voltage stress on switch, V_{switch} (% of V_0)	28	33.33	20	12.63
No. of switches	1	4	1	2
Component count, CC	8	12	8	12
Voltage gain / Component count, M/CC	0.83375	0.833	1.25	1.3191
Voltage gain / Switch stress, M/V_{switch}	0.2382	0.3	0.5	1.2533

6. Conclusion

A novel non-isolated DC-DC (niDC-DC) converter topology was proposed in this paper. The niDC-DC converter was developed from a two-phase IBC consisting of one CI in each phase, a voltage lift capacitor C_{Lift} and one VMC network connected across the secondary windings. The laboratory test results obtained from the prototype of niDC-DC converter confirmed that the converter delivered power of 225 W to the load at 91.6 % full load efficiency. The niDC-DC converter yielded a voltage gain of 15.83 when operated at a duty cycle of D=0.5 while maintaining the turns ratio of CIs at N=3. Since the proposed converter used the interleaved technique with uniform phase-shift between the interleaved legs, the current ripple content at the input side was reduced. In addition, the switches were subjected to only about 12.63 % of the output voltage. The reduction in

voltage stress magnitude was achieved by using hybrid combinations of voltage extension mechanisms like voltage lift technique, two coupled inductors each with a turns ratio of 3 and one VMC. Some of the salient features of the described converter are (i) high voltage gain, (ii) low input current ripple due to interleaved technique, (iii) reduced switch stress and (iv) compact in size. The salient features of this converter prove to be a good option for stepping up the voltage from the PV source and connecting it to a common 380 V DC bus of a microgrid.

7. References

[1] Firas Obeidat (2018). A comprehensive review of future photovoltaic systems. *Solar Energy*, vol. 163, pp.545-551.

[2] Sinan Ozlu and Ibrahim Dincer (2015). Development and analysis of a solar and wind energy based multigeneration system. *Solar Energy*, vol. 122, pp. 1279-1295.

[3] Hassan Fathabadi (2017). Novel standalone hybrid solar/wind/fuel cell power generation system for remote areas. *Solar Energy*, vol. 146, pp. 30-43.

[4] N.W.A Lidula, A.D. Rajapakse (2011). Microgrids research: a review of experimental microgrids and test systems. *Renewable and Sustainable Energy Reviews*, vol. 15, pp. 186_202.

[5] B. Sri Revathi, M. Prabhakar and Francisco Gonzalez-Longatt (2018). High-gain–high-power (HGHP) DC-DC converter for DC microgrid applications: Design and testing, *International Transactions on Electrical Energy Systems*, vol. 28, no. 2, https://doi.org/10.1002/etep.2487.

[6] T. Arunkumari and V. Indragandhi (2017). An overview of high voltage conversion ratio DC-DC converter configurations used in DC micro-grid architectures, *Renewable and Sustainable Energy Reviews*, vol. 77, pp. 670-687.

[7] B. Sri Revathi and M. Prabhakar (2016). Non-isolated high gain DC-DC converter topologies for PV applications – A comprehensive review, *Renewable and Sustainable Energy Reviews*, vol. 66, pp. 920-933.

[8] Mojtaba Forouzesh, Yam P. Siwakoti, Saman A. Gorji, Frede Blaabjerg and Brad Lehman (2017). Step-Up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies and applications, *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143-9178.

[9] Huawu Liu, Haibing Hu, Hongfei Wu, Yan Xing, and Issa Batarseh (2016). Overview of coupled-inductor high step-up boost converters, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 689-704.

[10] Nilanjan Tewari and V.T. Sreedevi (2018). A novel single switch dc-dc converter with high voltage gain capability for solar PV based power generation systems, *Solar Energy*, vol. 171, pp. 466-477.

[11] V. Fernão Pires, Daniel Foito, F.R.B. Baptista, J. Fernando Silva (2016). A photovoltaic generator system with a DC/DC converter based on an integrated Boost-Cuk topology, *Solar Energy*, vol. 136, pp. 1-9.

[12] Asim Amir, Hang Seng Che, Aamir Amir, Ahmad El Khateb, Nasrudin Abd Rahim (2018). Transformerless high gain boost and buck-boost DC-DC converters based on extendable switched capacitor (SC) cell for stand-alone photovoltaic system, *Solar Energy*, vol. 171, pp. 212-222.

[13] R. Girish Ganesan and M. Prabhakar (2013). Non-Isolated High Step-Up Interleaved Boost Converter, *International Journal of Power Electronics*, vol. 6, no. 3, pp. 288-303.

[14] Wuhua Li, Weichen Li, Xin Xiang, Yihua Hu and Xianging He (2014). High step-up interleaved converter with built-in transformer voltage multiplier cells for sustainable energy applications, *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2829-2836.

[15] Tohid Nouri, Naser Vosoughi, Seyed Hossein Hosseini and Mehran Sabahi (2017). Novel interleaved nonisolated ultrahigh-step-up DC–DC converter with ZVS performance, *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3650-3561.

[16] Tohid Nouri, Syed Hossein Hosseini, Ebrahim Babaei and Jaber Ebrahimi (2015). Interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell, *IET Power Electronics*, vol. 8, no. 2, pp. 175-189.

[17] Kuo-Ching Tseng, Chi-Chih Huang (2014). High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system, *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1311-1319.

[18] Antônio Alisson Alencar Freitas, Fernando Lessa Tofoli, Edilson Mineiro Sá Júnior, Sergio Daher and Fernando Luiz Marcelo Antunes (2015). High-voltage gain DC-DC boost converter with coupled inductors for photovoltaic systems, *IET Power Electronics*, vol. 8, no. 10, pp. 1885-1892.

[19] Boris Axelrod, Yuval Beck, and Yefim Berkovich, Y (2015). High step-up DC–DC converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier steady state and dynamics, *IET Power Electronics*, vol. 8, no. 8, pp. 1420-1428.

[20] Hamid Bahrami, Hossein Iman-Eini, Babak Kazemi, Alireza Taheri (2015). Modified step-up boost converter with coupled-inductor and super-lift techniques, *IET Power Electronics*, vol. 8, no. 6, pp. 898-905.

[21] Zhangyong Chen, Qun Zhou, Jianping Xu (2015). Coupled-inductor boost integrated flyback converter with high-voltage gain and ripple-free input current, *IET Power Electronics*, vol. 8, no. 2, pp. 213-220.

[22] Musbahu Muhammad, Matthew Armstrong, and Mohammed A. Elgendy (2016). A nonisolated interleaved boost converter for high-voltage gain applications, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 352-362.

[23] Moumita Das, and Vivek Agarwal (2016). Design and analysis of a high-efficiency DC–DC converter with soft switching capability for renewable energy applications requiring high voltage gain, *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2936-2944.