

PAPER • OPEN ACCESS

## Comparative performance of voltage multipliers for MEMS vibration-based energy harvesters

To cite this article: Binh Duc Truong *et al* 2018 *J. Phys.: Conf. Ser.* **1052** 012118

View the [article online](#) for updates and enhancements.

### Related content

- [Electrostatic vibration energy harvester using an electret-charged mems transducer with an unstable auto-synchronous conditioning circuit](#)  
Armine Karami, Philippe Basset and Dimitri Galayko
- [Characterization of the capacitance variation of electrostatic vibration energy harvesters biased following rectangular charge-voltage diagrams](#)  
Armine Karami, Dimitri Galayko and Philippe Basset
- [Maximizing Output Power in a Cantilevered Piezoelectric Vibration Energy Harvester by Electrode Design](#)  
Sijun Du, Yu Jia and Ashwin Seshia



**IOP | ebooks™**

Bringing you innovative digital publishing with leading voices to create your essential collection of books in STEM research.

Start exploring the collection - download the first chapter of every title for free.

# Comparative performance of voltage multipliers for MEMS vibration-based energy harvesters

**Binh Duc Truong, Cuong Phu Le and Einar Halvorsen**

Department of Microsystems, University College of Southeast Norway, Campus Vestfold,  
Raveien 215, 3184 Borre, Norway.

E-mail: [Einar.Halvorsen@usn.no](mailto:Einar.Halvorsen@usn.no)

**Abstract.** This paper investigates by numerical simulation the performance of an electrostatic vibration energy harvester when it is electrically configured in two different diode-capacitor multiplier topologies. The complete lumped-model of an overlap-varying generator along with power electronic interface circuit is constructed for analysis using a circuit simulator. Parasitic capacitance of the transducers and nonideal diode traits such as leakage current and junction capacitance are incorporated. We find that both configurations are able to efficiently operate with a ratio of capacitance variation much lower than 2, which overcomes a challenging obstacle of MEMS-based devices. Other advantages and disadvantages of the two topologies are compared and discussed.

## 1. Introduction

There are circumstances in which sensing devices are positioned in inaccessible places such as the moving parts of machinery and vehicles, or where cabling is expensive or even impossible [1, 2]. In this scenario, energy harvesting can enable or lower the cost of an application by providing a means to implement battery-less systems [3]. Many environmental energy sources can be exploited these purposes, for instance temperature gradient or mechanical vibrations [4]. This paper focuses on vibrational energy harvesters with electrostatic transduction.

The first report of a MEMS-based electrostatic generator that includes integrated electronics was presented in [5]. Since then, several studies on power electronic interface circuit for capacitive transducers in which the harvester is commonly coupled to AC-DC and/or DC-DC converters, have been published [6–8]. Complexity of control circuitry and power consumption are the main concerns of those architectures. Furthermore, in the majority of cases, those converters cannot start up below a certain input voltage [9] which is can be higher than a typical output voltage generated by the microharvesters [10]. Therefore, a processing circuit that scales up the voltage making it suitable for the following converters is sometimes required. Based on the ancient "doubler of electricity" invented by Bennet in the late 18th century, de Queiroz *et al.* proposed a promising electronic version adapted to MEMS devices [11]. The circuit consists of two variable capacitors, three diodes/switches and one fixed capacitor where the harvested energy is stored. When the voltage across the storage capacitor reaches a certain maximum value, the accumulated charge is then dumped into a battery by using a simple buck converter [12]. An attempt to increase charging current for the doubler circuit was reported in [13]. The main disadvantage of such a configuration is its inability to operate efficiently with



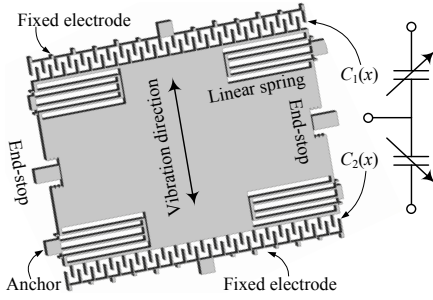


Figure 1: Overlap-varying electrostatic energy harvester (EH).

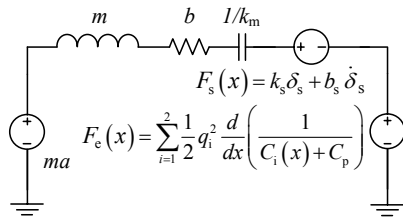


Figure 2: Equivalent circuit for mechanical domain.

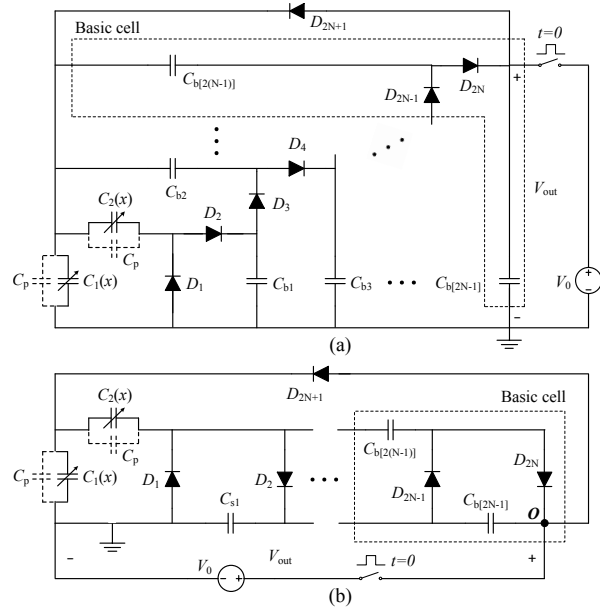


Figure 3: EH electrically configured as (a) Parallel-Series (PS) and (b) Cockcroft-Walton (CW) voltage multipliers.

transducers that have ratio of capacitance variation  $\eta$  lower than 2. This challenge is difficult to overcome in practice since MEMS harvesters tend to suffer from parasitic capacitances and the variable capacitance is small due to limitation of microfabrication processes and device size.

Recent work by Lefeuvre *et al.* [14] introduced a self-biased topology for electrostatic vibration energy harvesters. Based on theoretical analysis in the electrical domain using a rectangular Q-V cycle, the authors suggested that this circuit configuration can operate with  $\eta < 2$ . With an N-stage voltage multiplier, the ideal minimum required ratio of capacitance variation is  $\eta_{min}^{ideal} = \frac{N+1}{N}$  [15]. In the same manner, this paper presents and compares two alternative electrical configurations: (i) A parallel-series multiplier adapted from the Greinacher voltage doubler [16] and (ii) a variation of Cockcroft-Walton multiplier [17]. Dynamic performances of both topologies are analyzed using circuit simulations.

## 2. Energy harvester model and voltage multiplier configurations

A sketch of the in-plane overlap-varying energy harvester is shown in Figure 1. The proof mass is suspended by linear, folded springs with total stiffness  $k_m$ . The transducer capacitances as functions of the proof mass displacement  $x$  are  $C_{1/2}(x) = C_0(1 \pm x/x_0)$ , where  $C_0$  and  $x_0$  are the nominal capacitance and the nominal overlap respectively. The maximum displacement  $X_{max}$  is defined by rigid end-stops. The movable mass is subject to the fictitious force  $ma$ , the electrostatic force  $F_e$  and the impact force  $F_s$  from the end-stops. The equivalent circuit for the mechanical domain is presented in Figure 2, where  $b$  is the damping coefficient,  $q_{1/2}$  are the charges on the two transducers,  $C_p$  is the parasitic capacitance and  $\delta_s$  is the relative displacement of the mass and the end-stops during contact at high input acceleration.

Two ordinary anti-phase transducers are electrically configured as N-stage voltage multiplier as shown in Figure 3. The Parallel-Series (PS) configuration was first proposed and thoroughly analyzed in [18], showing its superior performance over the circuit presented in [14]. The Cockcroft-Walton (CW) topology is generalized from 2-stage CW generator introduced in [19]. The voltage source  $V_0$  in series with a switch is used to pre-charge the capacitors to initiate

Table 1: Model parameters

Parameters	Value
Proof mass, $m$	0.79 mg
Spring stiffness, $k_m$	3.60 N/m
Thin-film air damping, $b$	3.48e-5 Ns/m
Nominal overlap, $x_0$	80 $\mu\text{m}$
Nominal capacitance, $C_0$	15 pF
Parasitic capacitance, $C_p$	7.5 pF
Contact stiffness, $k_s$	3.361 MN/m
Impact damping, $b_s$	0.435 Ns/m
Maximum displacement, $X_{\text{max}}$	$\approx 31 \mu\text{m}$
Relative contact displacement, $\delta_s$	$\delta_s =  x  - X_{\text{max}}$
Multiplying capacitor, $C_{b[j]}$	$C_b = 1 \text{ nF}$

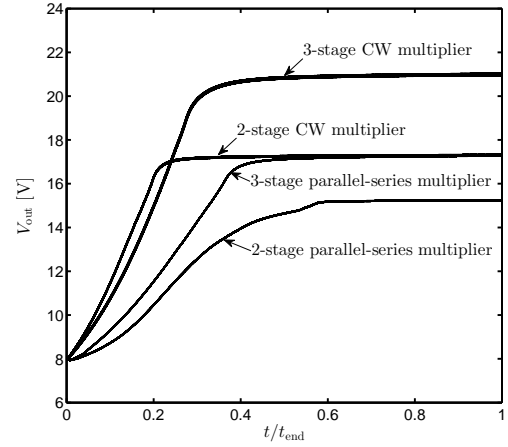


Figure 4: Time evolution of output voltage.

operation of the multiplier circuits in the simulations. How to secure such a pre-charge in a complete system is not addressed here. Output of the PS multiplier is the voltage across  $C_{b[2N-1]}$  while that of the CW circuit is the potential between the node  $O$  and ground. The dynamic model of the Schottky diode BAS716 is used for SPICE simulations incorporating junction capacitance and losses due to leakage current. All fixed capacitances  $C_{b[j]}$  are chosen equal for simplicity.

In order to investigate the potential merits of these two configurations, the transducers are designed so that the capacitance variation ratio is

$$\eta = \frac{C_{\text{max}} + C_p}{C_{\text{min}} + C_p} = 1.7 \quad (1)$$

where the minimum and maximum capacitances are  $C_{\text{min}} = 9.19 \text{ pF}$  and  $C_{\text{max}} = 20.81 \text{ pF}$ . The parameters are summarized in Table 1.

### 3. Simulation results

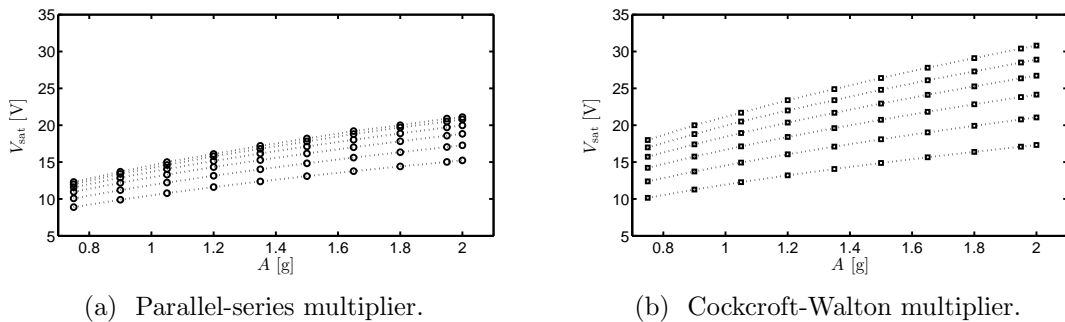


Figure 5: Saturation voltage of the two configurations versus input acceleration amplitudes.

Figure 4 shows time evolution of the output voltage  $V_{\text{out}}$  for both PS and CW topologies with number of stages  $N = 2$  and 3, initial bias  $V_0 = 8 \text{ V}$ , input acceleration amplitude  $A = 2 \text{ g}$  and drive frequency  $f = f_0 = 1/2\pi\sqrt{k_m/m}$ . As long as  $V_0$  is sufficient for operation of the circuits,  $V_{\text{out}}$  initially increases. After several transient cycles, a saturated output voltage is observed for all cases. It can be explained by an increase of electromechanical coupling.

Figure 5a and 5b present the saturation voltage  $V_{\text{sat}}$  of the two multiplier configurations over a range of acceleration amplitude  $A \in [0.75 \text{ g}, 2 \text{ g}]$  for several numbers of stages  $N \in \{2, \dots, 7\}$ . The simulation results show that both voltage multipliers give higher  $V_{\text{sat}}$  with increase of  $N$  and  $A$ . However, the CW multiplier performs better than the PS multiplier. In addition, it is worth mentioning that  $V_{\text{sat}}$  is independent on  $V_0$ . Therefore, the lowest possible value of pre-charging voltage is desirable. In particular, with  $N = 2$ , the minimum required initial bias for PS and CW multipliers are  $(V_0)_{\text{min}}^{\text{PS}} = 5.5 \text{ V}$  and  $(V_0)_{\text{min}}^{\text{CW}} = 4 \text{ V}$  respectively making the CW multiplier somewhat more attractive.

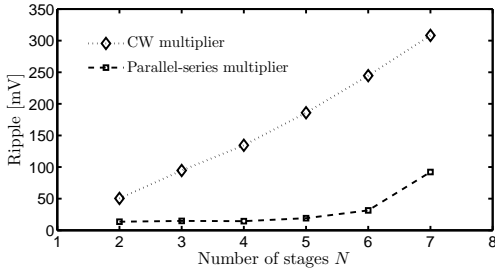


Figure 6: Comparison of ripple voltage between the two topologies.

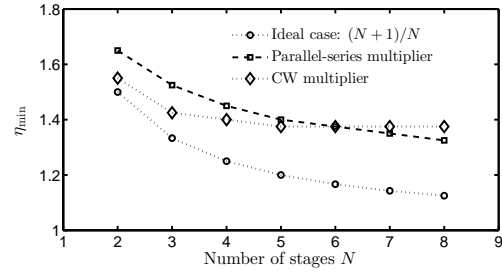


Figure 7: Minimum required capacitance variation ratio versus number of stages.

Due to the charge and discharge of capacitors, the output is distorted and shows some ripple superimposed on the DC saturation voltage. Figure 6 depicts peak-to-peak ripple of the two multipliers versus the number of stages  $N$  for  $A = 2 \text{ g}$  and  $f = f_0$ . The comparison shows a potential advantage of the PS multiplier over the CW configuration if ripple is a concern.

To explore the benefits of  $N$ -stage multipliers, we choose to adjust  $X_{\text{max}}$  as a way to modify  $\eta$  while the other parameters in Table 1 are kept unchanged. Figure 7 reveals variations of the minimum required ratio of capacitance variation  $\eta_{\text{min}}$  when the number of stages  $N$  increases. When electrical losses are taken into account,  $\eta_{\text{min}}$  is a little higher than the threshold corresponding to the ideal case. A general trend for the PS topology is the continued decrease of  $\eta_{\text{min}}$  when adding more stages. However, for the CW configuration, this statement is only the case with  $N \leq 5$ . Higher  $N$  results in almost unchanged  $\eta_{\text{min}}$ . As a consequence, the  $\eta_{\text{min}}$ -curve of PS multiplier crosses that of CW circuit at  $N = 6$ . Hence, the PS multiplier can be advantageous when  $N \geq 7$ .

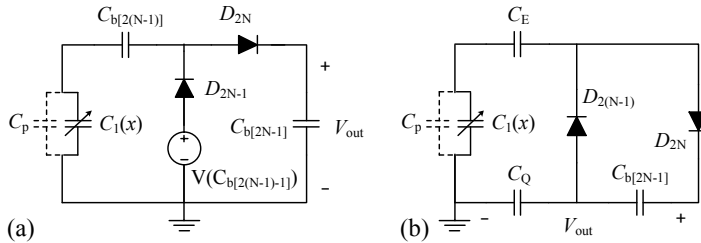


Figure 8: Equivalents for the final stages of (a) PS and (b) CW multipliers.

To explain the behavior for increasing  $N$ , we consider simplified operation of the two topologies at the final stage as shown in Figure 8, which directly affect the output performance of the harvesting system. For the PS multiplier, the voltage across capacitor  $C_{b[2(N-1)-1]}$  can effectively be represented by a DC voltage source  $V(C_{b[2(N-1)-1]})$ . Meanwhile, two series connected capacitors of CW multiplier ( $C_2(x), C_{b2}, C_{b4}, \dots, C_{b[2(N-1)]}$ ) and

$(C_{b1}, C_{b3}, C_{b5}, \dots, C_{b[2N-3]})$  are presented by two equivalent capacitors  $C_E$  and  $C_Q$  respectively, where

$$C_E = \frac{C_b(C_2(x) + C_p)}{C_b + (N-1)(C_2(x) + C_p)}, C_Q = \frac{N-1}{C_b}. \quad (2)$$

The harvested energy of the PS topology is always stored in a capacitor whose capacitance is independent on  $N$ . For the CW topology, in contrary, capacitance of the equivalent storage capacitor can be treated as a function of  $N$ , i.e.,  $C_{out} = (C_Q^{-1} + C_{b[2N-1]}^{-1})^{-1} = \frac{C_b}{N}$ . Increase of  $N$  reduces  $C_Q$ , and therefore  $C_{out}$ . Hence, the voltage ripple of the latter significantly increases with  $N$  while that of the former is only changed negligibly.

Our simulations also show that increase of  $V(C_{b[2(N-1)-1]})$  allows  $\eta_{min}$  of the PS multiplier to be reduced by increasing  $N$ . In this case,  $C_{b[2(N-1)]}$  is not affected by  $N$  and is still satisfies the condition that it is relatively much larger than the transducer capacitance for operation of the circuit. While for the CW multiplier, the more stages, the smaller  $C_E$  and  $C_Q$  are obtained. Therefore  $\eta_{min}$  cannot decrease further at high  $N$ .

#### 4. Conclusion

This paper presented a study of the performance of MEMS capacitive energy harvester when electrically configured as voltage multipliers. Two topologies were investigated and compared. Both are able to operate with the capacitance variation ratio  $\eta$  lower than 2 which is the threshold for operation of the Bennet's voltage doubler. The CW multiplier has the advantages of higher saturation voltage and lower required initial bias. However, the PS multiplier gives smaller ripple at the output. In addition, even though the minimum required capacitance ratio  $\eta_{min}$  of both configurations can be reduced by adding more stages, the PS topology benefits more from a high number of stages.

#### Acknowledgment

This work was supported by the Research Council of Norway through Grant no. 229716/E20.

#### References

- [1] Wang L and Yan Y 2014 *Measurement Science and Technology* **25** 115101
- [2] Ngigi R W, Pislaru C, Ball A and Gu F *Journal of Physics: Conference Series* **364** 012016
- [3] Ferrari M, Ferrari V, Guizzetti M and Marioli D 2009 *Smart Materials and Structures* **18** 085023
- [4] Vullers R, van Schaijk R, Doms I, Hoof C V and Mertens R 2009 *Solid-State Electronics* **53** 684 – 693
- [5] Roundy S 2003 Ph.D. thesis University of California at Berkeley Berkeley CA
- [6] Yen B C and Lang J H 2006 *IEEE Transactions on Circuits and Systems—Part I: Regular Papers* **53** 288–295
- [7] Torres E O and Rincon-Mora G A 2010 *IEEE Journal of Solid-State Circuits* **45** 483–496
- [8] Kempitiya A, Borca-Tasciuc D A and Hella M M 2013 *IEEE Transactions on Industrial Electronics* **60** 5639–5647
- [9] Damaschke J M 1996 *Applied Power Electronics Conference and Exposition* pp 856–860 vol.2
- [10] Hudak N S and Amatucci G G 2008 *Journal of Applied Physics* **103** 101301
- [11] de Queiroz A C M and Domingues M 2011 *IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)* pp 1–4
- [12] de Queiroz A C M and Domingues M 2011 *IEEE Transactions on Circuits and Systems II: Express Briefs* **58** 797–801
- [13] Dragunov V and Dorzhiev V 2013 *Journal of Physics: Conference Series* **476** 012115
- [14] Lefeuvre E, Riskey S, Wei J, Woytasik M and Parrain F *Journal of Physics: Conference Series* **557** 012052
- [15] de Queiroz A C M 2016 *2016 IEEE International Symposium on Circuits and Systems (ISCAS)* pp 650–653
- [16] Hauschild W and Lemke E 2014 *High-Voltage Test and Measuring Techniques* 1st ed (Springer-Verlag Berlin Heidelberg)
- [17] Cockcroft J D and Walton E T S 1932 *Proceedings of the Royal Society of London A: Mathematical, Physical and Engineering Sciences* **136** 619–630
- [18] Truong B D, Le C P and Halvorsen E *arXiv:1709.08759*
- [19] Truong B D, Le C P and Halvorsen E *arXiv:1709.08754*