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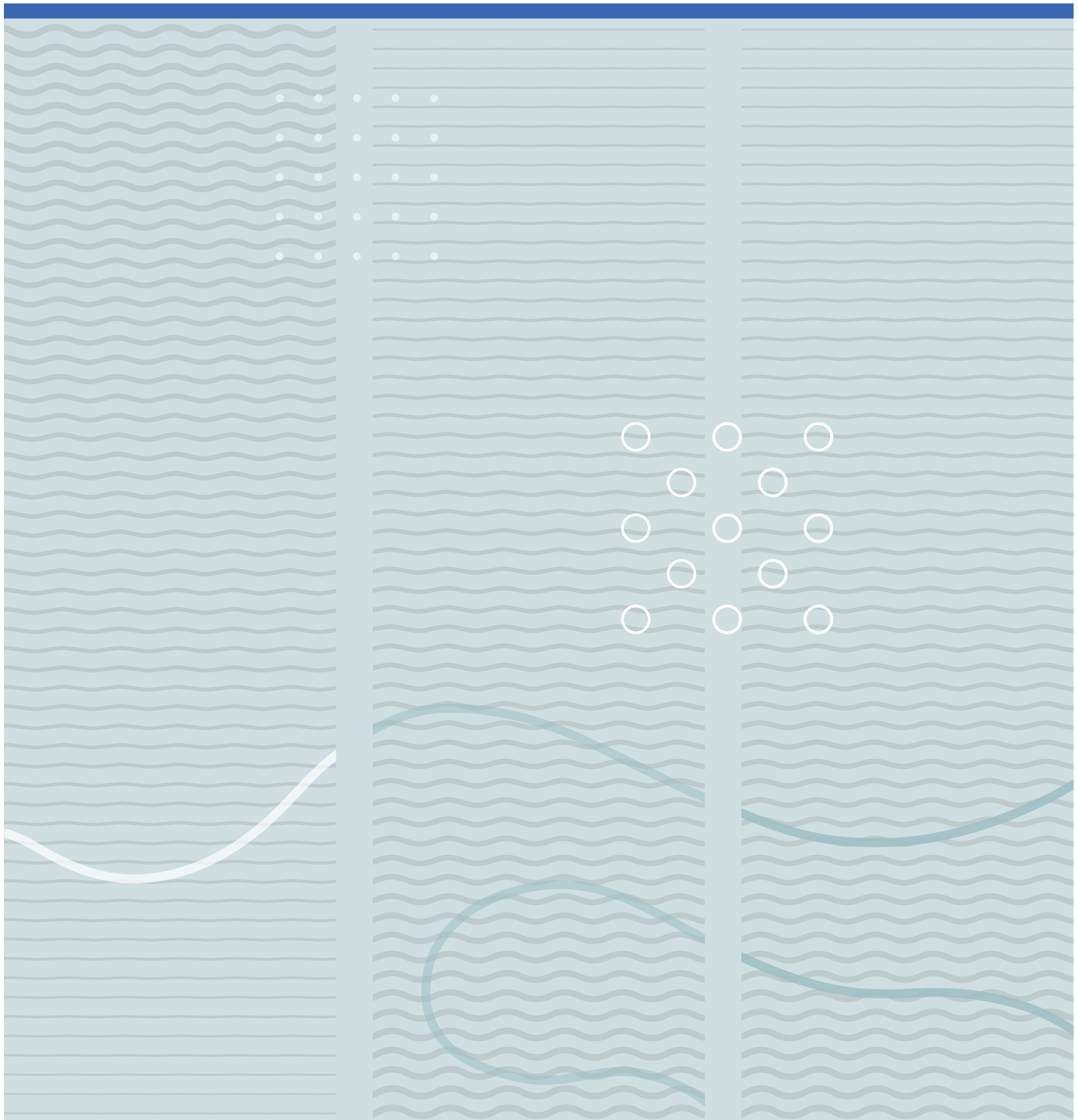
Doctoral dissertation no. 5
2018

Eivind Bardalen

# Reliable Packaging and Development of Photodiode Module for Operation at 4 K



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# Reliable Packaging and Development of Photodiode Module for Operation at 4 K

A PhD dissertation in
**Applied Micro- and Nanosystems**

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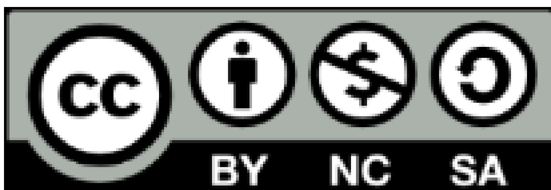
Faculty of Technology, Natural Sciences and Maritime Sciences
**University of South-Eastern Norway**
Borre, 2018

**Doctoral dissertations at the University of South-Eastern Norway no. 5**

ISSN: 2535-5244 (print)
ISSN: 2535-5252(online)
ISBN: 978-82-7860-318-5 (print)
ISBN: 978-82-7860-317-8 (online)

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Print: University of South-Eastern Norway

# Preface

This doctoral thesis is submitted in partial fulfilment of the requirements for the degree of Philosophiae Doctor at the Faculty of Technology and Maritime Science, University College of Southeast Norway (HSN), Norway.

The work was carried out from 2014 to 2017 at the University College of Southeast Norway, Institute for Microsystems, under the supervision of Per Øhlckers and Muhammad Nadeem Akram, HSN and Helge Malmbekk, Justervesenet.

The background for the work are the European Research Projects Q-WAVE and QuADC. The work has been done in cooperation with groups at Justervesenet, Physikalisch-Technische Bundesanstalt (PTB) and National Physical Laboratory (NPL) in Norway, Germany and the UK, respectively.

The work was mainly funded by a PhD scholarship from University College of Southeast Norway funded by the Norwegian Ministry of Education and Research. In addition, Norwegian PhD Network on Nanotechnology for Microsystems (NanoNetwork) funded part of the research work.

This work was also partly carried out with funding by the European Union within the EMRP JRP SIB59 QWAVE and EMPIR JRP 15SIB04 QuADC. The EMRP and EMPIR are jointly funded by the EMRP participating countries within EURAMET and the European Union.

I am thankful for the support of colleagues at HSN, especially for lab assistance from Thai Anh Tuan Nguyen, Zekija Ramic, Thomas Martinsen, Hoang Vu Nguyen and Ragnar Dahl Johansen.

# Abstract

AC voltage standards based on pulse-driven Josephson junction arrays, operated at 4 K, enable quantum-accurate generation of arbitrary voltage waveforms. These devices are operated by biasing the arrays with high-frequency current pulses. Utilizing an optically controlled current source, consisting of a modulated laser source and optical fiber-coupled photodiodes, operated at 4 K, rather than an electrical link, is expected to have several advantages in terms of performance.

The PhD-project has focused on the development of an optoelectronic module for realizing this concept. Packaging techniques and characterization of the module was investigated. In particular, designs and materials for reducing thermal stress at 4 K were considered.

A packaging technique for assembling multiple optical fiber-coupled high-speed photodiodes on silicon substrates was demonstrated. The assembly was shown to have sufficient precision and to be robust against thermal stress. Finite element simulations of the thermomechanical stresses were performed in order to validate the robustness claim.

The frequency response of commercial InGaAs/InP photodiodes up to 14 GHz, as well as DC-response, was measured at room temperature and at 4 K. It was shown that the effect of low temperature did not negatively affect the frequency response.

The thesis also includes a review of devices, packaging techniques and materials for cryogenic optoelectronics. In addition, initial work on semiconductor simulations of photodiodes at low temperature is discussed.

# Abbreviations

| | |
|---|---|
| AC | Alternating current |
| BIPM | International Bureau of Weights and Measures |
| CTE | Coefficient of Thermal Expansion |
| CPW | Coplanar Waveguides |
| DC | Direct Current |
| DMTA | Dynamical Mechanical Thermal Analysis |
| FEM | Finite Element Method |
| FR | Flame Retardant |
| HSN | University College of Southeast Norway |
| JAWS | Josephson Arbitrary Waveform Synthesizer |
| JJA | Josephson Junction Array |
| MSM | Metal-Semiconductor-Metal |
| NMI | National Metrology Institutes |
| NPL | National Physical Laboratory |
| PCB | Printed circuit Board |
| PPG | Pulse Pattern Generator |
| PTB | Physikalisch-Technische Bundesanstalt |
| RF | Radio Frequency |
| RSFQ/SFQ | Rapid Single Flux Quantum |
| VNA | Vector Network Analyzer |

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# List of papers

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*Journal papers*

1 E. Bardalen, M. N. Akram, H. Malmbekk, and P. Ohlckers, "Review of Devices, Packaging, and Materials for Cryogenic Optoelectronics," *Journal of Microelectronics and Electronic Packaging,* vol. 12, pp. 189-204, 2015.

2 E. Bardalen, B. Karlsen, H. Malmbekk, O. Kieler, M. N. Akram, and P. Ohlckers, "Packaging, and Demonstration of Optical-Fiber-Coupled Photodiode Array for Operation at 4 K," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. PP, pp. 1-7, 2017.

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*Conference Papers*

5 E. Bardalen, T. A. T. Nguyen, H. Malmbekk, O. Kieler, M. N. Akram, and P. Ohlckers, "Packaging of fiber-coupled optoelectronic module for cryogenic voltage standards," in Electronic System-Integration Technology Conference (ESTC), 2016 6$^{th}$, 2016, pp. 1-4. Published IEEE Xplore, December 5$^{th}$, 2016. INSPEC Accession Number:16520013 DOI: 10.1109/ESTC.2016.7764502

*The work has also been presented at the following workshop and conferences:*

6 Eivind Bardalen, Muhammad Nadeem Akram, Helge Malmbekk, and Per Ohlckers: "Fiber-coupled Optoelectronic Module for AC Josephson Voltage Standards" Presentation at MME2016, 27$^{th}$ Micromechanics and Microsystems Europe workshop, Cork, Ireland, 28-30$^{th}$ August 2016

7 Eivind Bardalen, Muhammad Nadeem Akram, Helge Malmbekk, and Per Ohlckers: "Packaging of Fiber-coupled Module for Josephson Junction Array

Voltage Standards", Proceedings of CPEM 2016, Ottawa, Canada, July 10-15, 2016.

8 Eivind Bardalen, Muhammad Nadeem Akram, Helge Malmbekk, and Per Ohlckers: "Fiber-coupled Optoelectronic Module for AC Josephson Voltage Standards" Presentation at MME2016, 27th Micromechanics and Microsystems Europe workshop, Cork, Ireland, 28-30th August 2016

9 Eivind Bardalen, Per Ohlckers, Muhammad Nadeem Akram and Helge Malmbekk: "Packaging and Interconnection Techniques for Cryogenic Superconducting Optoelectronic Devices" Proceedings of the 22nd World MicroMachine Summit 2016, Tokyo, Japan, May 24 – 27, 2016

10 Eivind Bardalen, Bjoernar Karlsen, Per Ohlckers, M. Nadeem Akram, Helge Malmbekk, Oliver Kieler: "Packaging and demonstration of optical-fiber coupled photodiode array for operation at 4 K" Proceedings of the 23nd World Smart Systems & MicroMachine Summit 2017, Barcelona, Spain, May 15 – 17, 2017.

# 1 Introduction

## 1.1 Motivation

Metrology is the science of measurements. As advances are made in technology and sciences, there follows an ever increasing need for techniques and instruments that are able to perform measurements with higher speed, sensitivity, resolution and accuracy. Instruments such as voltmeters, clocks and weighing scales must be calibrated against a known reference. Ideally, any such instrument is linked to a *primary standard* through a chain of references. The primary standard must have the highest quality and follow specifications set by International Bureau of Weights and Measures (BIPM). Typically, they are maintained and operated by national metrology institutes (NMIs).

The primary standard ideally provides a reference that remains the same, independent of its age and environmental factors such as temperature, humidity and air pressure. In order to fulfill this goal, several primary standards have been redefined in terms of quantum properties during the last decades. A famous example is the definition of time, and conversely, frequency: "*The second is the duration of 9 192 631 770 periods of the radiation corresponding to the transition between the two hyperfine levels of the ground state of the Cesium 133 atom*" [1]. This redefinition was made possible by the invention of the atomic clock [2]. In contrast, the definition of the kilogram, which is the prototype platinum–iridium cylinder located in Paris, France [1], remains not defined by quantum properties.

The DC volt was redefined in 1992 by the Josephson standard, which exploits superconducting effects in the Josephson junction, and successfully replaced less accurate standards such as Weston cells [3]. These systems are based on Josephson junction arrays (JJA), a superconducting device, which are typically operated at 4.2 K.

Since then, effort has been put into extending the principle to AC voltages. The European research projects "A quantum standard for sampled electrical measurements " (Q-WAVE) [4], followed by "Waveform metrology based on spectrally pure Josephson voltages"

(QuADC) [5], aims to develop the Josephson Arbitrary Waveform Synthesizer (JAWS), in order to enable quantum-accurate measurements of alternating voltage waveforms. Justervesenet, the national metrology institute of Norway, and University College of Southeast Norway (HSN), are partners in this project, which includes NMIs in major European countries. The main task of Justervesenet and HSN is to develop a photodiode module capable of operating as a high-speed current source at 4 K. The module is intended to replace the coaxial high-speed electrical link between a pulse-pattern generator and the superconducting JJA chip. Several challenges are associated with this development, including developing packaging compatible with cryogenic environments, as well as testing and characterization of the devices.

The PhD-project focuses on the development of photodiode modules for pulse operation of Josephson arrays. In its final version, the optoelectronic drive system may consist of a variety of optical and optoelectronic elements, such as photodiodes, lenses, optical fibers, as well as laser sources and optical modulators. A successful implementation of the optoelectronic system requires careful consideration of individual elements, as well as the collective behavior of the system.

The goal of the PhD.-project was to investigate, design and characterize an optoelectronic module, with the goal of implementing it in the JAWS system.

## 1.2 Thesis structure

In sections 1.3-1.7, the intention is to provide an overview of the basic theory that is necessary to understand the devices and systems in the scope of the PhD.-project. The state of the art technological background is first discussed, including AC Josephson voltage standards and optoelectronic control of superconducting electronics. In addition, some theoretical and practical challenges associated with the design and operation of the optical module are discussed.

In chapter 2, the development and investigation of packaging techniques for photodiode modules are described. In chapter 3, the optical and electrical characterization of photodiode modules is described. A discussion of each paper in a wider context is given

in chapter 4, while the conclusions reached and summary of papers are given in chapter 5 and 6, respectively.

## 1.3 The Josephson Voltage Standard

### 1.3.1 DC Josephson voltage standard

The SI system contains seven units: ampere, kelvin, second, meter, kilogram, candela and mol. These can be used to represent any physical quantity. The unit for electric potential, volt, can be derived from these units:

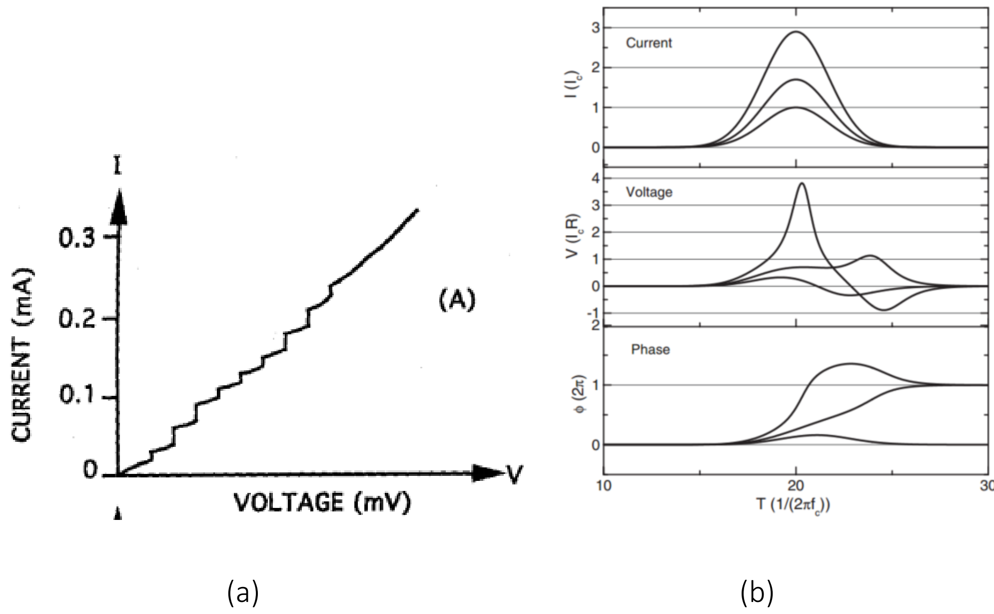
$$V = \frac{J}{C} = \frac{kg \cdot m^2/s^2}{A \cdot \ s} = \frac{kg \cdot m^2}{A \cdot s^3} \tag{1}$$

Since 1990, the practical realization of the volt has been defined by the Josephson effect [3]. This effect occurs in Josephson junctions, which are two superconductor layers separated by a thin slice of a non-superconducting material. Brian Josephson first derived the equations that predicted superconducting tunneling flow in these junctions [6], which showed that there is a unique relationship between the voltage $V(t)$ across the junction and the superconducting tunneling current $I(t)$:

$$V(t) = \frac{\hbar}{2e}\frac{d\phi}{dt}, \tag{2}$$

$$I(t) = I_c \sin\big(\phi(t)\big), \tag{3}$$

where $I_c$ is the *critical current* of the junction, $\phi$ is the *phase difference* between the two superconductors, while $\hbar$ and $e$ are Planck's reduced constant $(h/2\pi)$ and the elementary charge, respectively. From equations (2) and (3), it can be seen that in the absence of a voltage, a constant tunneling current may be present through the junction. This is the so-called DC Josephson effect.




(a) (b)

Figure 1: (a) Voltage steps in an overdamped Josephson junction array biased by a constant microwave signal. The voltage steps are given by eq. (5). Reproduced from [3]. (b) Simulation of Gaussian current pulses through a Josephson junction. Top panel: Current pulses. Middle panel: Instantaneous voltage. Bottom panel: Integral of voltage expressed as phase. Reproduced from [7].

On the other hand, if a constant voltage is applied on the Josephson junction, a sinusoidal supercurrent oscillating between $+I_c$ and $-I_c$ will be generated: $I(t) = I_c \sin(2\pi f t)$. It is then easy to show that the frequency of the current is directly proportional to the applied voltage:

$$f = \frac{2e}{h} V \tag{4}$$

In eq. (4), the *Josephson constant* $K_{J-90} = \frac{2e}{h}$ appears. Its inverse, $\Phi_0 = \frac{h}{2e} = 2.07 \cdot 10^{-15}\ Wb$, is known as the *magnetic flux quantum*.

Conversely, if a microwave frequency is applied on the Josephson junction, it is possible to generate precise voltage plateaus in the I-V diagram that appear as multiples ($n = 0,1,2,3,\dots$) of $\Phi_0$ [8]. By integrating hundreds to tens of thousands of Josephson junctions in a series array on a single integrated chip, it is possible to generate voltages up to several volts by applying a microwave frequency to the array. For *N* junctions, the step heights of the voltages are given by:

$$V_n = \Phi_0 \cdot f \cdot n \cdot N \quad (5)$$

This equation forms the basis of the Josephson voltage standards: The step number *n* is selected by applying a DC biasing current in combination with the microwave signal. The appearance of such steps depends heavily on the design and fabrication of the Josephson junctions. Several types of Josephson junction have been developed using various materials and barrier thicknesses for the non-superconducting layer, which result in variations in the critical current, junction capacitance and resistance (see e.g. [9]). For *overdamped* Josephson junctions, a single-valued voltage step may be selected by controlling the bias current, as seen in Figure 1 (a).

### 1.3.2 AC Josephson standards

Today, high accuracy measurements of AC voltages are still largely performed using *thermal voltage converters* (TVC) [10]. These devices compare the heat generated from the AC source with a known DC source to determine the root-mean-square of the AC voltage. While this is a well-established technology, TVC measurements do not have a basis in quantum properties. In addition, they carry no information about harmonic content or phase.

Recent developments in digital metrology have increased the demand for AC voltage measurements: This demand especially "*consists in direct traceability for analog-to-digital (ADC) and digital-to-analogue converters (DAC) dealing with arbitrary waveforms in the DC to 10 MHz range" [4].*

Developing methods for synthesizing AC voltages based on Josephson junction technology would bring these desired improvements. From eq. (5) it can be seen that in order to generate a time-varying output voltage $V_n$, *N* and *f* may be modulated. In fact, two different techniques have been developed based on changing *N* and *f,* respectively.

### 1.3.3 Programmable Josephson Voltage Standard

In the *Programmable Josephson Voltage Standard (PJVS)*, the voltage is modulated by operating JJAs with different lengths in parallel [3]. The number of junctions in each array is such that the voltages follow a binary system: ($1V_1$, $2\ V_1$, $4\ V_1$, $8\ V_1$, $16\ V_1$…). Thus, a time-dependent voltage such as a sine wave is generated by controlling the bias current through each segment, and thereby the number of junctions operated at a given quantum step:

$$V(t) = \Phi_0 \cdot f \cdot n \cdot N(t) \tag{6}$$

High peak-to-peak voltages, up to 20 V [11], may be synthesized using this technique. However, as it is a step-wise approximation, the output has limited accuracy and contains significant higher-order harmonics.

### 1.3.4 Pulse driven Josephson Array/Josephson Arbitrary Waveform Synthesizer

The second technique is based on modulating the frequency of the microwave signal. However, directly modulating the frequency of a sine wave is not preferable, as the voltage steps collapse rapidly as the frequency is decreased [3]. Instead, a signal consisting of short current pulses with a repetition frequency $f$ is used. This technique, named the *pulse driven Josephson array*, was first proposed and demonstrated by Benz and Hamilton in 1996 [12]. From equations (2) and (3), it is easy to show that the time-averaged voltage generated by a single electrical pulse is proportional to $\Phi_0$. Incidentally, a class of superconducting electronics, single flux quantum (SFQ) electronics, is based on this principle (see e.g. [13]). Assuming the time between each pulse is $T = \frac{1}{f}$, the time-averaged voltage in a series array of N junctions is:

$$< V > = N\frac{1}{T}\int_0^T V(t)dt \ = Nf\int_0^{2\pi \cdot n} \frac{\hbar}{2e} d\phi = N\Phi_0 nf \tag{7}$$

The step number $n$ depends on the peak current and the width of the input current pulse, as shown in Figure 1 (b). The *Josephson Arbitrary Waveform Synthesizer (JAWS)*,

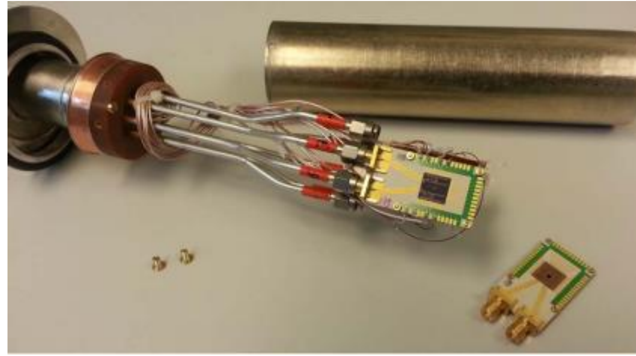


Figure 2: Photograph of the cold-head of an 8-channel cryoprobe at Physikalisch-Technische Bundesanstalt (PTB). Two arrays are arranged on each chip, and four chips are operated in total. The input signal is connected with coaxial cables from a room-temperature pulse pattern generator. Reproduced from [14].

which appears to have first been coined in 2000 [15], is an extension of this principle: Any desired waveform is encoded in a pulse train with varying pulse repetition frequency $f(t)$. A common technique for converting the analogue waveform to a digital code is so-called *Delta-Sigma modulation [16].* The programmed code is generated as an electrical signal by a pulse-pattern generator (PPG) and transmitted to the JJA located at 4 K. Bipolar voltage waveforms may be generated by using a combination of positive and negative pulses.

A major challenge with the pulse-drive technique is the generation of sufficiently high voltages. As the voltage generated by a 10 Gbps signal by a single junction is only around 20 µV ($\Phi_0 \approx 2.07\, \mu V/GHz$)), an array must contain several thousand junctions to generate voltages of a few hundred mV. However, increasing the number of junctions leads to attenuation of the input microwave signal [17], which limits the maximum number of junctions in an array. Nonetheless, today, improvements in chip fabrication and system design of the JAWS technology have advanced to the stage where very pure sine waves with voltages up to 1-2 $V_{rms}$ at frequencies around 1 kHz have been demonstrated [14, 18, 19]. Essential to these results is to operate multiple JJAs in parallel and connecting the output voltage in series. Figure 2 shows an example of this setup, demonstrated by PTB. In [14, 18], each array is driven by a separate PPG channel

connected with coaxial cables to the chip-carrier PCB, while in [19], on-chip power dividers were used to split the PPG output channels between two arrays.

## 1.4 Optoelectronic control of superconducting Josephson electronics

Using an optoelectronic link instead of electrical coaxial cables between room-temperature equipment and superconducting Josephson junction devices have been demonstrated in several applications. Such a link usually consists of a modulated laser source linked by an optical fiber to a cooled photodetector. There are several motivations for doing this:

- The JJA is isolated from the signal generator. This allows for simpler operation of the arrays as a common noise problem is avoided [20].
- Bipolar voltages may be generated by operating the JJA with a pair of photodiodes which produce positive and negative current pulses [7].
- Single mode optical fibers have high bandwidths, up to 100 GHz, and are immune to electromagnetic interference [21].
- Optical fibers have a lower thermal load than coaxial electrical cables [21].

The feasibility of this approach, in terms of optoelectronic performance, depends on pulse parameters, such as shape, width and amplitude. The necessary peak amplitude of the current pulses is related to the critical current $I_C$ of the Josephson junctions, as appears in equation (3). In [7], as shown in Figure 1 (b), it can be seen that the peak current should exceed $I_C$ in order to generate the quantized voltage.

Optoelectronic control of Josephson-type superconducting electronics and JJAs have been demonstrated by several groups, and was first demonstrated for SFQ circuits in the 1990s, (e.g. [21, 22]). Later, the prospect of using photodiodes to control JJAs was demonstrated [7, 23, 24]. In these demonstrations, the critical currents of the Josephson junctions were typically well below 1 mA. In contrast, Josephson junctions with critical currents in the range 1-12 mA are used in state-of-the-art JJA chips (see e.g. [14, 18]).

## 1.5 High-speed photodetectors

Today, high-speed photodetectors are used extensively in e.g. fiber optic networks, as well as in sensor applications. A wide range of photodetector designs exists, with different characteristics in terms of sensitivity, bandwidth, saturation and noise levels. The bandwidths of photodetectors are limited by carrier transit time, RC time constant, diffusion current, carrier trapping at heterojunctions and packaging [25].

In particular, *PIN-photodiodes* are commonly used in commercial high-speed applications. Their structure consist of P- and N-doped semiconductor layers separated by an undoped, intrinsic (I) layer, as shown in Figure 3. In thermal equilibrium, an electric field is present between the N- and P-doped layers. The basic working mechanism of PIN-photodiodes is to generate free electrons and holes by absorbing the optical input, which subsequently are drifted away by the electric field. In PIN-photodiodes, the purpose of the intrinsic layer is:

- The quantum efficiency is increased as the absorption length is increased
- The bandwidth is increased as most carriers are generated within the intrinsic layer, and are therefore rapidly transported away by the electric field.

Depending on the semiconductor material, the photodiode may be designed to operate at different wavelengths of light. GaAs and $In_{0.53}Ga_{0.47}As$ are typically used as the absorbing material in high-speed photodetectors, typically operating at up to 850 nm and 1700 nm, respectively. These wavelengths correspond to dips in the absorption spectra of silica optical fibers at 850 nm, 1310 nm and 1550 nm [26]. In fiber-optic networks, 1550 nm has become more or less the standard wavelength, with widely available commercial components such as laser and optical modulators.

InGaAs PIN-photodiodes are fabricated on InP-substrates, and are therefore often referred to as InGaAs/InP photodiodes. They are heterostructures, as one or both of the doped regions consist of InP, which has a higher bandgap than InGaAs. Therefore, most absorption takes place in the InGaAs-region, which reduces the diffusion of carriers from outside the intrinsic layer.

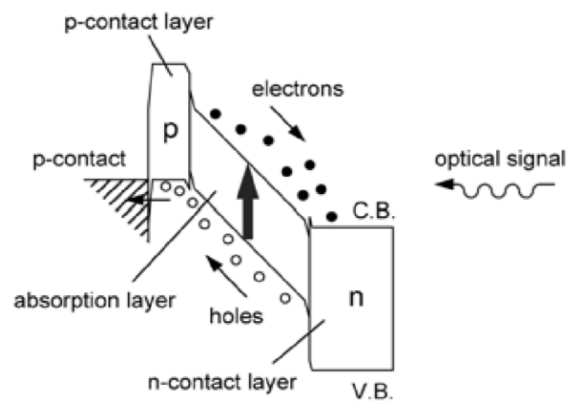



Figure 3: General band structure of a PIN-photodiode. Reproduced from [27].

### 1.5.1 Low-temperature operation of photodiodes

There have been several demonstrations of photodiodes operating at cryogenic temperatures: An InGaAs PIN-photodiode tested at 4 K was shown to have improved high-speed performance compared to room temperature in [22]. In [28], an InGaAs/InP photodiode with graded bandgap layers was tested and shown to have a bandwidth over 20 GHz at both room temperature and at 9 K.

Some other types of photodiodes have also been demonstrated for control of superconducting electronics: A structure similar to PIN-photodiodes, InGaAs/InP *uni-travelling carrier* (UTC)-photodiode [29] was demonstrated for a 40 Gbps input signal in [30]. Similarly, a UTC-photodiode module cooled to 4 K was also used successfully to operate a JAWS in [20]. Additionally, Metal-Semiconductor-Metal (MSM)-photodiodes have been demonstrated as input to superconducting circuits: An InGaAs MSM-photodiode on a InP substrate was demonstrated as an optical input module for a flip-chip bonded SFQ-circuit [31], while a silicon MSM-detector integrated on a rapid single flux quantum (RSFQ) chip was demonstrated in [21].

### 1.5.2 Temperature effects in semiconductors

The operating temperatures for industrial devices are typically in the range -40 °C to 100 °C. At these temperatures, most semiconductor devices are expected to perform within their specified values. At significantly higher or lower temperatures, such as 4 K,

the characteristics of the device may change drastically, and may lead to loss of functionality or even improved performance. These changes result from strong temperature-dependences of some material properties. In order to understand the performance and behavior of photodiodes, especially at low temperatures, fundamental properties such as ionization, transport mechanisms and temperature-dependences must be considered. Therefore, in the following section, some basic semiconductor theory, focusing on thermal behavior, is given.

#### *1.5.2.1 Carrier energy distributions*

Equations (9)-(15) are formulated for free electrons and ionized donors. The corresponding equations for holes and ionized acceptors are similar, but are left out for brevity. A reference for the following equations is e.g. [32].

In semiconductors, the carrier densities of electrons and holes can be described by Fermi-Dirac-statistics. The occupation probability for a given energy level $E$ is given by the Fermi-Dirac distribution function:

$$f(E) = \frac{1}{1 + \exp(\frac{E - E_F}{kT})} \tag{8}$$

The carrier density for a given energy level is determined by the product of the occupation probability and the density of states: $n(E) = g(E) \cdot f(E)$. The total number of electrons in the conduction band is often expressed by the effective density of states $N_c$ and the Fermi-integral of order ½:

$$n = \int_{E_c}^{\infty} g(E) f\left(E, E_f\right) dE = \frac{2}{\sqrt{\pi}} N_c\,(T) \cdot F_{1/2}\,, \tag{9}$$

where $E_c$ is the conduction band edge. The effective density of states is given by:

$$N_c \;=\; 2\left(2\pi\, m_e k \frac{T}{h^2}\right)^{\frac{3}{2}}, \tag{10}$$

and the Fermi integral of order ½ is:

$$F_{1/2}(\eta) = \frac{2}{\sqrt{\pi}} \int_0^\infty \frac{\sqrt{x}}{1 + e^{x-\eta}} dx \,, \tag{11}$$

where $\eta = (E_F - E_C)/kT$. The intrinsic carrier density can by calculated by:

$$n_i = \sqrt{N_C N_V} \exp(-\frac{E_g}{2kT}) \tag{12}$$

When the semiconductor has a doping density $N_D$, the number of ionized donors is given by:

$$N_D^+ = N_D\left(1 - f\left(E, E_f\right)\right) = \frac{N_D}{1 + g_D \exp(\frac{E_f - E_D}{kT})} \,, \tag{13}$$

where $E_D$ is the donor energy level and $g_D$ is the degeneracy factor for the donor level.

Near room temperature, $kT \approx E_c - E_D$, and the Fermi function has a significant tail in the conduction band. When the charges are balanced ($n = N_d^+$) the number of free electrons is comparable to the donor concentration $N_d$. It is then common to assume complete ionization ($n = N_d$), as a simplification.

In comparison, at low temperatures, $kT \ll E_c - E_D$, incomplete ionization of carriers becomes significant, as the Fermi-function approaches a step-function in comparison to the energy diagram. When the charges are balanced ($n = N_d^+$), the Fermi level $E_f$ is close to $E_d$, and the number of free carriers is significantly lower than the donor concentration ($n \ll N_d$).

#### *1.5.2.2 Dynamic properties*

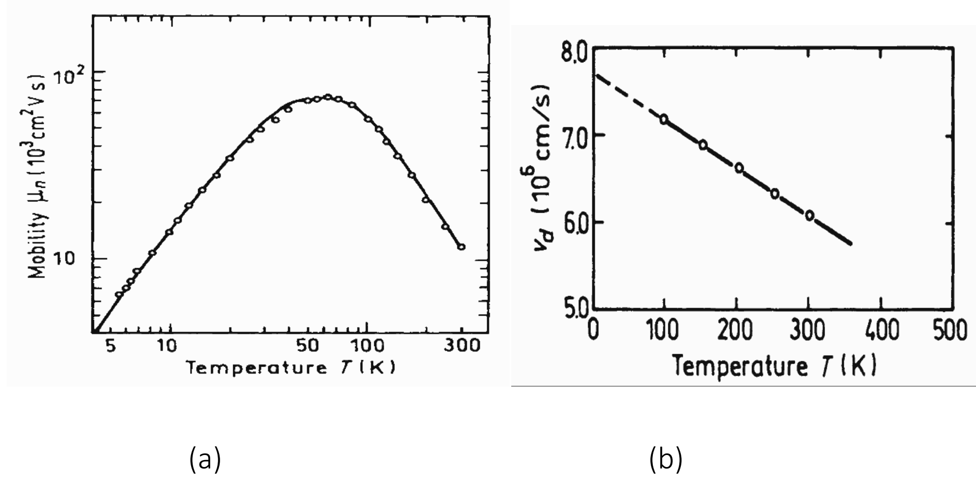
The transport of carriers can be described by the well-known drift-diffusion equations. The electron current density is given by:

$$\mathrm{J_n} = D_n \nabla \mathrm{n} + \mu_\mathrm{n} E \cdot n \,, \tag{14}$$

where $D_n$ is the diffusion coefficient, $\mu_\mathrm{n}$ is the electron mobility and $E$ is the electric field. The time derivative of the free electron concentration is given by:

$$\frac{dn}{dt} = \frac{1}{q}\nabla \mathrm{J_n} + G - R, \tag{15}$$

where $G$ is the generation rate and $R$ is the recombination rate. For photodiodes, $G$ describes the optical generation of carriers, while the recombination term describes the excitation/de-excitation rate of carriers in in equilibrium.




(a) (b)

Figure 4. (a) Electron Hall mobility versus temperature for Ga0.47In0.53As. Reproduced from [33]. (b). Electron saturation velocity versus temperature for Ga0.47In0.53As. Reproduced from [34]. Both graphs reproduced from http://www.ioffe.ru/SVA/NSM/Semicond/GaInAs.

The electron/hole mobilities ($\mu_n, \mu_p$) determine the electron velocity in an electric field: $\mathrm{v} = \mu \cdot \mathrm{E}$. Impurity and phonon scattering are typically the dominant mechanisms that determine the mobility [33]. They are temperature-dependent: At higher temperatures, phonon scattering increases, while the impurity scattering decreases. The mobility is dependent on impurity concentration and has a maximum mobility at an intermediate temperature. For example, in InGaAs, the mobility typically has a maximum near 50 K, as shown in in Figure 4 (a). In [36], if was found that the mobility in thin $In_{x-1}Ga_xAs$ films at 4 K was higher than at 295 K.

Another temperature-dependent property is the saturation velocity $v_d$, which is the maximum speed of the carrier in high electric fields. Figure 4 (b) shows that $v_d$ in InGaAs

can be expected to increase moderately at low temperatures. However, data is lacking for many materials.

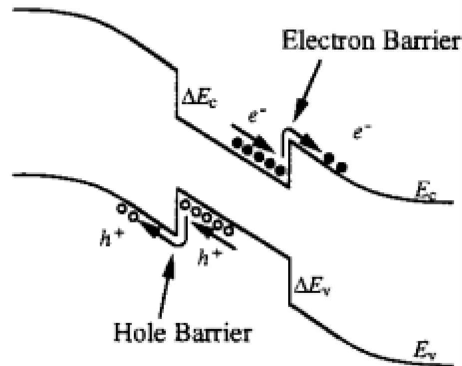



Figure 5: Heterostructure trapping effect. Reproduced from [25].

*Transport across heterojunctions*

InGaAs photodiodes are heterojunction devices, as they are fabricated on InP substrates (InGaAs/InP). Since the two materials have different bandgaps and electron affinity (χ), there are energy barriers between the InGaAs/InP-regions, as shown in Figure 5. Depending on the design of the photodiode, these barriers may limit the frequency response of the photodiode. The transport mechanism across heterojunction barriers is usually understood to be thermionic emission and tunneling, and may be modelled as such [35].

However, the sharp bandgap barrier may be smoothed by using graded bandgap layers to minimize carrier trapping in high-bandwidth photodiodes [36]. In [28], an InGaAs/InP with graded bandgap layers operated at 9 K showed no decrease in performance, indicating that carrier trapping was not an issue.

*Bandgap/absorption*

In general, the bandgap $\mathrm{E_g}$ increases at lower temperatures. This is caused by the change in lattice dimensions due to the shrinking of the crystal. For example, in $In_{0.53}Ga_{0.47}As$, the bandgap increases from 0.75 eV at 300 K to 0.822 eV at 0 K [37]. From the relationship between photon energy and frequency, and conversely, wavelength, $E = hf = \frac{hc}{\lambda}$, it can

be found that the energy of 1550 nm wavelength is smaller than the bandgap at 0 K. Unfortunately, this excludes the use of 1550 nm laser sources for InGaAs PIN-photodiodes operated near 4 K.

## 1.6 Packaging

*Packaging* of microelectronics can be defined "*as the bridge that interconnects the ICs and other components into a system-level board to form electronic products" [38].* There are several considerations when developing the packaging for a given microsystem, such as reliability, thermal management, high-frequency properties, cost and size.

A brief summary of packaging concepts and challenges is given in the following. A more thorough review was given in Article 1 [39].

### 1.6.1 Optical fiber packaging

A uniqueness in packaging of high-speed optoelectronic devices is the requirement of high alignment accuracy between an optical fiber and the optoelectronic chip, such as a laser diode or photodetector. This is due to the small geometrical dimensions of the optical fiber and optoelectronic device: The width of the beam in a single-mode optical fiber is comparable to the fiber core, usually around 8 µm. As the bandwidth of photodiodes increases with lower area, the diameter of the active area is usually less than 30 µm (see e.g. albisopto.com).

Depending on the chip design, different optical fiber assembly techniques may be used. Typically, in commercial optoelectronic modules, the chip is protected from the environment by a metallic housing. The optical fiber may be attached with techniques such as laser welding, adhesive bonding in v-groove-structures, or by using a physical structure such as a TO-can [40].

Due to the ever-increasing desire for higher bandwidths in optical fiber networks, a recent trend in optoelectronic packaging is the development of multiple optical channel packaging. For example, a 100 Gbps photoreceiver module was demonstrated using an 8-channel v-groove fiber ferrule for connecting to flip-chip bonded photodiodes via optical waveguides [41].

Several research groups have reported robust packaging solutions for optical fiber-connected modules operated at 4 K. For example, robust metallic housing modules for aligning superconducting photodetectors coupled to single optical fibers have been demonstrated to have efficient coupling at 4 K [43]. Several other examples are given in Article 1 [39].

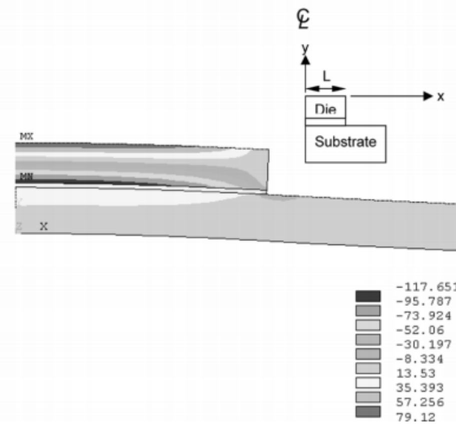



Figure 6: Distribution in axial stress ($\sigma_{xx}$) in silicon die adhesively bonded on organic substrate at $\Delta T = -120°\mathrm{C}$. Reproduced from [42].

### 1.6.2 Thermomechanical considerations for cryogenic environments

The difference between 20 °C and the boiling point of helium around 4 K (-269 °C) is approximately 290 °C. When different materials are bonded together, mechanical stresses and deformations develop due to differences in the coefficient of thermal expansion (CTE), as shown in Figure 6. At lower temperatures, mechanical properties may change significantly. In general, the CTE approaches 0/K at 0 K [44]. Many materials used for bonding, such as epoxies and solders, have significant increases in Young's modulus and changes in strength and ductility [45, 46]. This behavior lead to particular concerns for microelectronic assemblies operating at low temperatures, e.g. issues such as cracking in silicon chips [47, 48].

### 1.6.3 Chip bonding

Depending on chip configuration, photodiodes may be bonded with the active side facing up or down towards the substrate. In the first case, the electrical connections between

the chip and substrate is usually made by wire bonding. In the latter case, the chip is bonded with the active side facing down, with the so-called flip-chip technique, introduced by IBM in the 1960s [38]. Two main advantages of using this technique are:

- Shorter interconnection lengths, which may be of high importance for high-frequency applications.
- Reduced footprint.

In addition, the flip-chip technique may reduce assembly time, as both the mechanical and electrical connections are made in a single step. An adhesive underfill may also be added to improve strength. However, the substrate must be adapted to the chip pad layout, which may increase the cost. The mechanical and electrical connection in flip-chip assemblies may be made by several techniques such as:

- *Thermocompression* bonding, where two metals, typically gold, are joined at elevated temperature using force.
- *Solder* bonding, where the mechanical connection is made by melting a solder having a lower melting point than the adjoining metals.
- *Anisotropic conductive adhesive* (ACA) bonding, where an adhesive filled with metal spheres is used to create the mechanical and electrical contact.

## 1.7 Device requirements

For successful integration of a photodiode module in the JAWS system, it must fulfill several criteria, with respect to both mechanical and electrical properties, as well as restrictions in geometrical size and dimensions.

The feasibility of a cryogenically operated photodiode module depends on its capability to survive the mechanical stresses at low temperatures caused by CTE-mismatch. Failure mechanisms such as cracking in components due to over-stressing, as well as fatigue due to thermal cycling must be avoided.

The JJA chips fabricated by PTB typically consists of a 10 x 10 mm silicon based chip where a pair of Josephson arrays are integrated, spaced apart by approximately 4.5 mm. The signal input to the arrays are via integrated coplanar waveguides (CPW), which are wirebonded to a sample holder.

The photodiode module must therefore have approximately the same width and should house a pair of photodiodes, which may be connected via CPWs to the JJA chip. The module is typically intended to be operated in a helium Dewar inside a metal tube with a diameter of approximately 5 cm. The complete module structure, including photodiodes, optical fibers and electrical connections to external equipment must conform to this tight space.

In [14], the JJA arrays produced by PTB have a critical current of $I_C =$ 2.8 mA. Depending on the design of the Josephson junction, this value may be adjusted. As described in section 1.4, $I_C$ is a target amplitude for the photocurrent, which must be combined with a short rise/fall time, corresponding to a -3dB bandwidth higher than 10 GHz.

# 2 Investigation of assembly and packaging techniques

## 2.1 Introduction

To comply with the requirements outlined in section 1.7, it was necessary to design and produce a customized photodiode module. The design strategy was based on mounting bare photodiodes and optical fibers on silicon substrates with integrated superconducting coplanar waveguides for transmitting the output signal to the Josephson arrays. The investigation of optical fiber alignment techniques is described in the following section, while the photodiode mounting is described in section 2.3.

## 2.2 Optical fiber assembly

The design of the coupling between the optical fiber output and the photodiode influences performance in terms of coupling efficiency and size. As a high coupling efficiency was desired, a direct coupling scheme was used, placing the optical fiber directly towards the active area of the photodiode. Although this strategy increases the vertical profile of the assembly, it eliminated the need for incorporating additional optical elements such as lenses or mirrors.

Former prototypes had revealed challenges with achieving a robust and stable optical connection to the photodiode. An early prototype, illustrated in Figure 7 (a), was based on Albis PDCS20T InGaAs/InP PIN-photodiodes, which were flip-chip bonded onto a silicon substrate. To enable illumination of the 20 µm optical aperture with the optical fiber, a square hole was made through the substrate by anisotropic etching [49], as illustrated in Figure 7 (a). The optical fiber was aligned and glued using a standard optical epoxy, Hysol TRA-BOND F112. The results were unsatisfactory, due to several problems: The optical fiber would easily get deflected by the edges of the hole, resulting in poor optical coupling. Furthermore, the optical connection was poor after curing the glue, likely due to deformations. Most significantly, cooling with liquid nitrogen caused the silicon substrate to crack. An epoxy designed for cryogenic environments, Master Bond EPS-LLPSPAO-1 BLACK, was used to resolve the chip-cracking issue. However, subsequent

tests introduced new problems: The low viscosity of the epoxy caused the optical output to be blocked as it covered the optical fiber facet. Furthermore, due to the small aperture, it was difficult to achieve a stable optical connection.

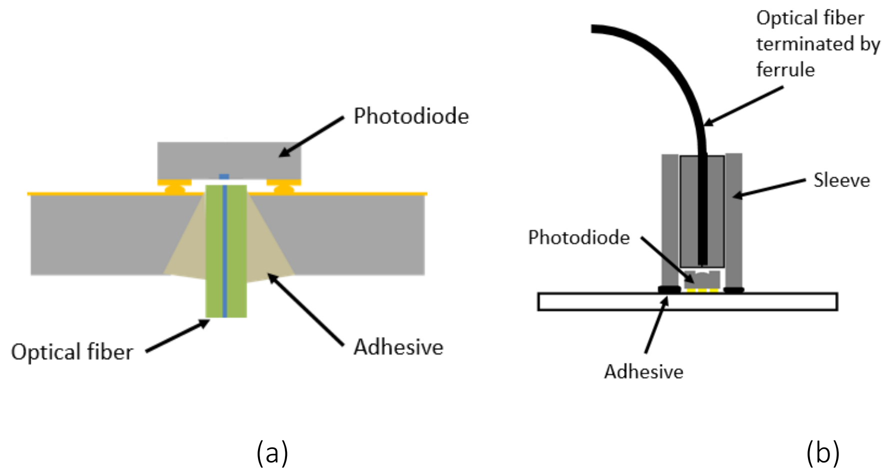



Figure 7: (a) Prototype 1. Albis PDCS20T photodiode with 20 µm optical aperture flip-chip bonded on a silicon substrate. A square hole was made through the substrate by anisotropic etching [49]. (b) Prototype 2. A flip-chip bonded Albis PDCS24L photodiode is illuminated from above by a pigtailed optical fiber supported by an alignment sleeve adhesively bonded to the silicon substrate.

### 2.2.1 Investigation of adhesive optical fiber bonding technique

To resolve the problem with poor optical coupling stability, a design based on a photodiode with a 100 µm integrated lens, Albis PDCS24L, was developed. When flip-chip bonded to a substrate, the photodiode is illuminated from above. A coupling structure, “Prototype 2”, as illustrated in Figure 7 (b), was based on adhesively bonding an alignment sleeve directly to the silicon substrate, into which an optical fiber terminated by a matching ferrule is inserted. The silicon substrate is then adhesively bonded to a printed circuit board (PCB) for connecting the photodiode output to a Josephson junction array or to external measurements.

#### *2.2.1.1 Thermomechanical stress modelling and testing*

As initial tests indicated that cracking in the silicon substrate due to thermal stress was a major risk, different design configurations and materials for the fiber optic structure were

considered. Two types of epoxies commonly used for cryogenic applications were considered: Stycast 1266 [50], in addition to Master Bond EPS-LLPSPAO-1 BLACK. In addition, two types of alignment sleeves, ceramic (zirconia) sleeves (Thorlabs part no: ADAF1) and borosilicate alignment sleeves (Thorlabs part no: 51-2800-1800) were considered.

The effect of the mechanical properties of the PCB, epoxy and alignment sleeve material on thermal stress was investigated using finite element simulations: A 3D finite element method (FEM) model of the adhesive optical fiber assembly (Prototype 2) was built in COMSOL Multiphysics simulation tool to estimate the thermal stresses caused by cooling the structure to 4 K. The simulated assembly contains four different components: The optical fiber alignment sleeve, silicon substrate, PCB substrate and the epoxy bonds. In the simulation, the mechanical stress and strain tensors are calculated, assuming an initial stress-free state at a higher temperature, which was set to be the curing temperature of the epoxy (80° C). With a change in temperature from the stress-free state, the differences in the coefficients of thermal expansion (CTE) between materials lead to stresses in the assembly. Each material has a stress-strain relationship that is given by the Young's modulus E and Poisson's ratio $\nu$. In the simulations, the materials were assumed to be isotropic and have a uniform temperature. A high mesh density was used around the sleeve bond as the solutions predicted high stress concentrations in this area. The assembly has two symmetry planes, forming a cross through the assembly. Therefore, only a quarter of the assembly was simulated, as shown in Figure 8. The boundary conditions were the following: Symmetric boundary conditions were applied on the xz- and yz- cut planes. Furthermore, the origin vertex (0, 0, 0) was fixed, while the vertex (0, 0, -1) was free to move along the z-axis.

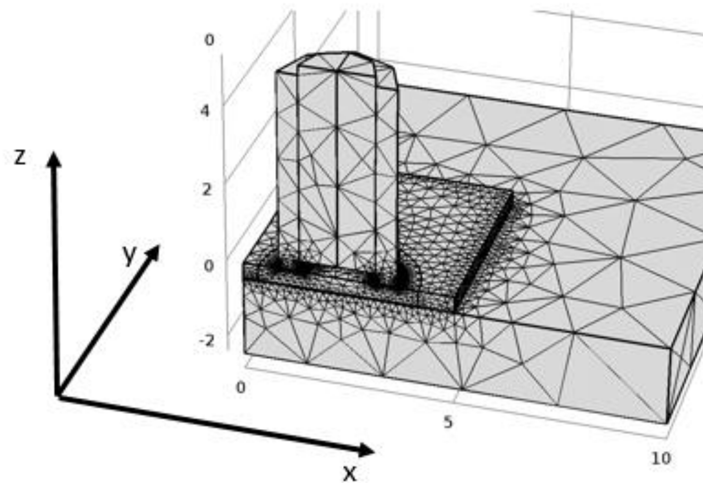



Figure 8: COMSOL model of assembly in Prototype 2.

Due to the extreme temperature-range, it was necessary to include the temperature-dependence of the CTE and Young's modulus. Most temperature-dependences were based on data found in literature. Getting realistic data for the temperature-dependence of the epoxy used is especially important, as different types of epoxy mixtures have differences in both stiffness, strength and thermal expansion, as is well documented (see e.g. [45]). For Master Bond EPS-LLPSPAO-1 BLACK, stiffness and thermal expansion measurements were made at SINTEF, Oslo, using dilatometry and dynamical mechanical thermal analysis (DMTA), as no low-temperature data were available. Results down to approximately 120 K were produced for both stiffness and thermal expansion measurements, as shown in Figure 9. The data obtained by the measurements was then extrapolated to 4 K. The approximate curve shape at the lowest temperatures was found by comparing to available data other epoxies given in literature (see e.g. Figs. 19 and 21 in Article 1). However, this is an assumption that adds to the uncertainty of the simulations.

For the remaining materials, the material properties were found using data from literature. As low-temperature data of most PCB materials are severely lacking, the CTE and Young's modulus were taken as parameters in the simulations. Figure 10 shows the total relative thermal expansion of five materials used in the assembly. All used parameters at 4 K are given in Article 4 [51].

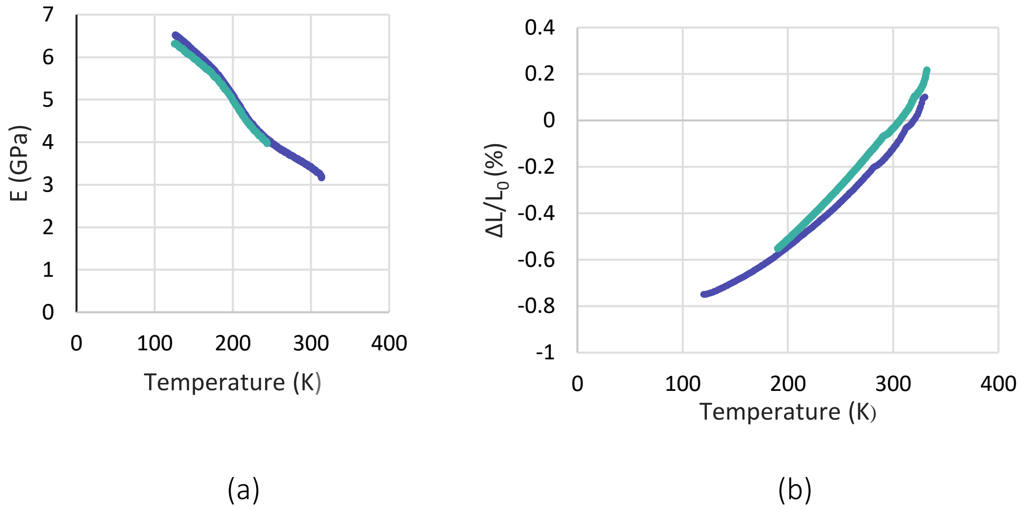



Figure 9: Results of mechanical measurements for two Master Bond EPS-LLPSPAO-1 BLACK samples. (a) Young's modulus $E$. (b) Total relative expansion $\Delta L/L_0$.

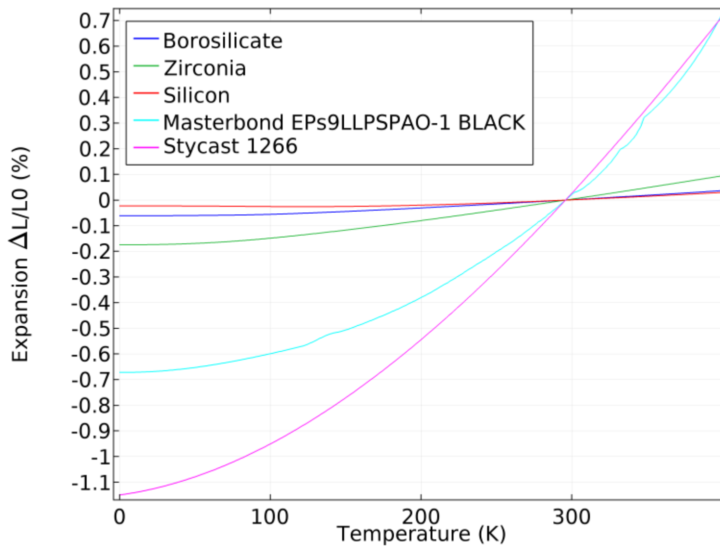


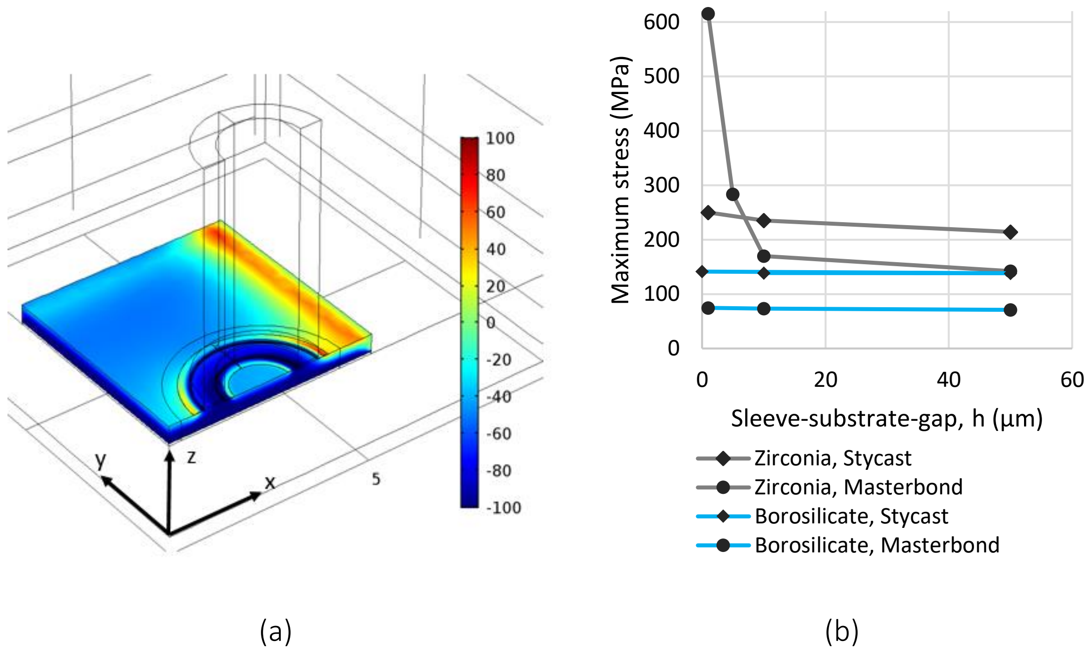

Figure 10: Total relative thermal expansion from room temperature ($\Delta L/L_0$) for components in the assembly.

The results of the FEM simulations showed that the adhesive bonding of the alignment sleeve caused a relatively high increase in tensile stress in the silicon substrate at 4 K compared to a bare silicon substrate. Figure 11 (a) shows an example of the stress distribution of axial stress ($\sigma_{xx}$), while Figure 11 (b) shows the maximum $\sigma_{xx}$ for different assembly configurations. The magnitude depended both on the mechanical properties

of the epoxy and the alignment sleeve material. In particular, using a ceramic type sleeve would increase stress by several hundred MPa compared to a bare silicon substrate, whereas using a borosilicate glass sleeve had a much lower impact on the stress. Furthermore, the epoxy with the lower CTE and Young's modulus caused lower stresses. In most cases, the gap between the alignment sleeve and the substrate had a small impact on the stress, as shown in Figure 11 (b).

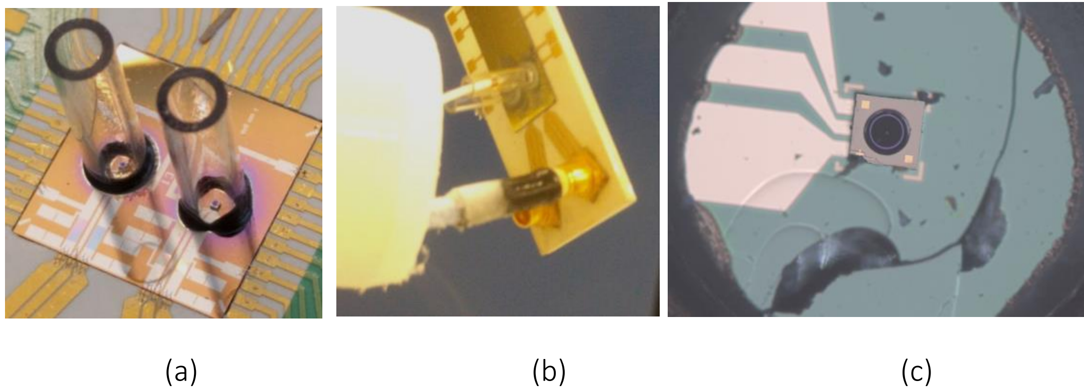
It was also found that other parameters, such as the thickness and type of PCB material influenced the stress. In particular, the surface stress was reduced by using thicker PCB substrates.

Thus, from the simulations, it is clear that the most efficient way to reduce the risk of cracking in the silicon substrate is to use borosilicate glass sleeves. To test this hypothesis, several samples were made for testing the survivability of the assembly. Figure 12 (a) and (b) show two samples where borosilicate alignment sleeves were bonded using the Master Bond and Stycast epoxy, respectively. Both samples were found to tolerate cooling with liquid nitrogen and helium well. In contrast, prototypes made using zirconia alignment sleeves would crack during cooling to 4 K, as shown in Figure 12 (c). Furthermore, as described in section 2.2.2, borosilicate glass sleeves used in combination with silicon alignment fixtures were tested with no mechanical failure incidents. This strengthens the claim of long-term robustness.




(a) (b)

Figure 11: (a) Simulated axial stress ($\sigma_{xx}$) distribution in the silicon substrate at 4 K. The apparent asymmetry between the upper left and upper right chip edges is due to only $\sigma_{xx}$ being shown, while $\sigma_{yy}$ is hidden. (b) Maximum stress $\sigma_{xx}$ in silicon substrate for various assembly configurations.



(a) (b) (c)

Figure 12: (a) and (b): Adhesively bonded borosilicate sleeves on silicon substrate, using (a) Master Bond and (b) Stycast epoxy. (c) Evidence of cracking in silicon substrate for a prototype using zirconia alignment sleeve.

### 2.2.2 Development of alignment fixtures

A biasing concept of the high-speed photodiode, based on operating multiple photodiodes in series, was envisioned early on in the Q-Wave project [52]: By operating one or more photodiodes by a continuous wave (CW), they generate a constant voltage that may be used as the reverse biasing voltage for a pulse-operated photodiode used to generate the current pulses.

In order to implement the optical biasing concept, as well as facilitating dual photodiode channels, multiple photodiodes must be bonded on a single substrate. Depending on the number of photodiodes needed for biasing, up to 2 to 8 photodiodes may be incorporated for each module. Silicon substrates for mounting eight photodiodes in two series (2 x 4) were designed by NPL and produced by PTB. The mask layout is shown in Figure 13. The conducting lines were made from Niobium (Nb), a metal that is superconducting below 10 K.

An assembly process for permanently aligning multiple alignment sleeves was developed for this cause. The concept utilizes an alignment structure for passively aligning and fixing multiple alignment sleeves. Figure 14 shows the concept: Rectangular silicon chips with circular holes are cut from a silicon wafer. It is then bonded on top of the silicon substrate using epoxy. Laser cutting was chosen as the technique for cutting the wafer as it allows for fast prototyping with sufficient accuracy.

A 532 nm Rofin Powerline E laser cutter was used. Several parameters were adjusted to obtain the desired cuts, such as pulse length, scribing speed, number of repetitions, etc. In order to align the silicon fixtures, the fixtures were cut to match features on the silicon substrate, such as width and height, as well as position of bonding pads and conductive lines.

The fixtures were aligned using a Finetech pico die bonder. Due to the relatively large dimensions of the alignment features, repeated test placements were performed to check and adjust the alignment before the final bonding. Figure 15 (a) and (b) shows the fixture before placement, while Figure 15 (c) shows a zoom-in on the wire bond pads

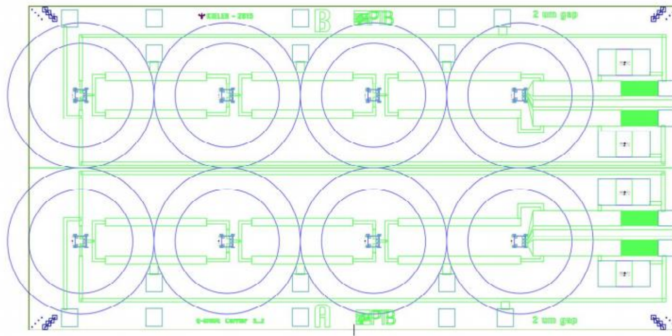


Figure 13: Photodiode substrate diagram, designed by PTB, for flip-chip mounting of two channels of four series coupled photodiodes. Pads for bonding photodiodes are located in the center of each blue ring. On-chip capacitors (shown as solid green) are used to block the DC-component of the current while allowing the pulses through.

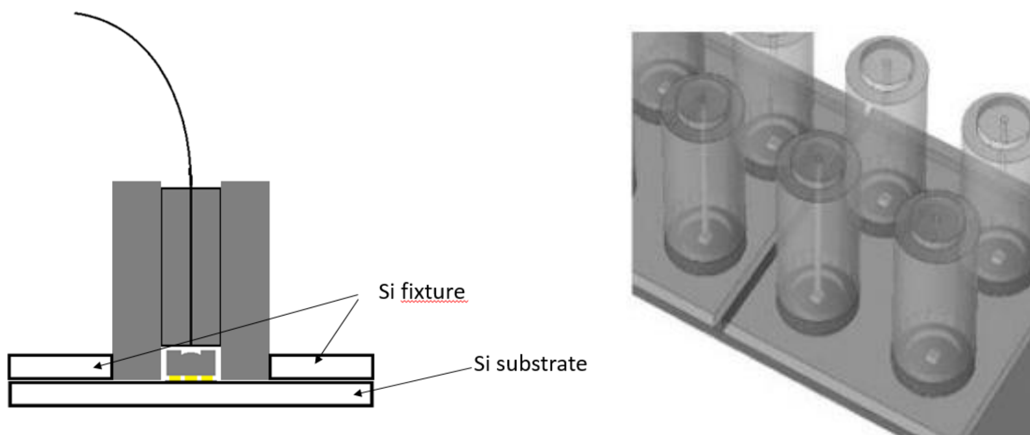



Figure 14: Left: Cross-section view of optical fiber assembly concept in Prototype 3. A rectangular fixture for holding alignment sleeves is made by cutting through silicon wafers. Glass alignment sleeves are inserted into circular holes, where the hole centers are aligned to the photodiode. Right: 3D view of the assembly.

used to check for alignment. Small drops of Master Bond epoxy were applied to the fixture before the final placement. Then, the optical fiber alignment sleeves were pressed into the holes and additional epoxy was applied near the edges of the sleeve to ensure a permanent structure, as shown in Figure 16. The epoxy was then cured according to the standard cure schedule.

The assembly was demonstrated to tolerate cooling to 4 K well, as no cracking occurred in the silicon substrate after repeated testing.

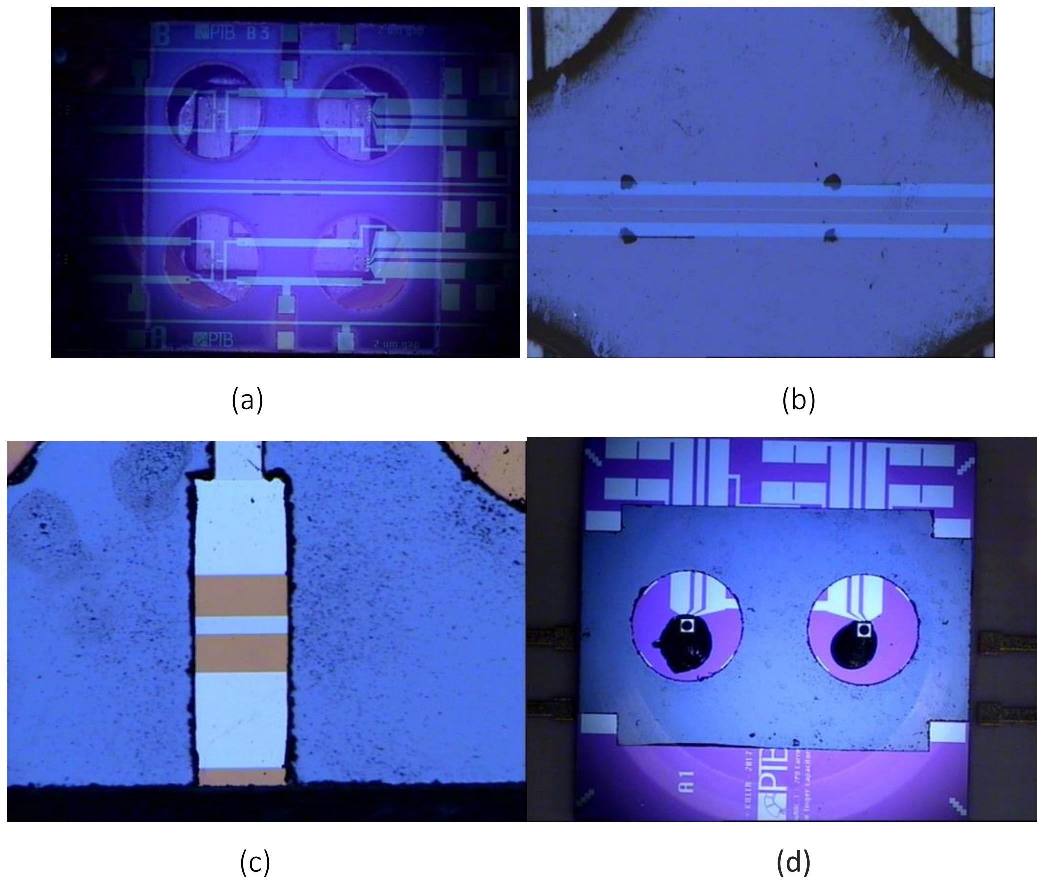



Figure 15: Assembly of silicon fixtures for mounting of alignment sleeves. (a) Overlaid images of bonding surfaces. (b) Close-up of laser cut lines used for alignment to Nb conductive lines. (c) Close-up of silicon fixtures aligned to bonding pads. (d) Image of two-photodiode silicon fixture with flip-chip mounted photodiodes.

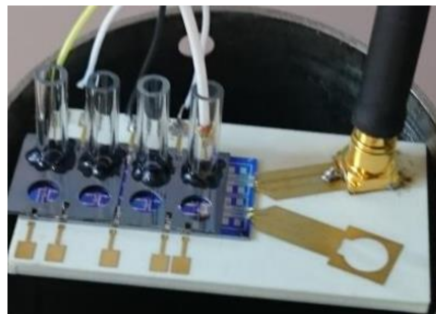


Figure 16: Photodiode module using silicon alignment fixture. An array of four photodiodes/alignment sleeves was assembled for testing. A single optical fiber is connected.

The effect of fiber-to-chip misalignment was estimated in COMSOL by simulating the beam propagation from the fiber facet through the photodiode. The coupling efficiency is given by:

$$\eta = P_f / P_{tot}, \tag{16}$$

where $P_f$ is the optical power incident on the active area, while $P_{tot}$ is the total optical power from the optical fiber. The optical coupling loss in decibel was then calculated as:

$$\eta_{dB} = 10 \log_{10}(\eta), \tag{17}$$

The simulation results showed that up to 40 µm misalignment would result in coupling losses less than 1 dB.

For the assembled samples, the effect of misalignment was estimated by comparing the photocurrent generated by a laser source via a manually aligned optical fiber with the photocurrent generated after assembly of the glass sleeve-ferrule structure. It was found that the photocurrent was reduced by up to 40 % compared to the manually aligned fiber. As the fixture-photodiode misalignment was measured to be smaller than 15 µm, the reduced responsivity indicate that the alignment sleeves had a slight angular misalignment after insertion. Thus, a combination of fiber-chip offsets and angular misalignment likely caused optical loss. By optimizing the hole diameter of the silicon fixture, the effect of angular misalignment may be reduced.

## 2.3 Photodiode bonding

### 2.3.1 Au thermocompression bonding

Au thermocompression bonding was the first bonding technique used for bonding the photodiodes. Gold stud bumps are first formed on a silicon substrate, before the photodiode is bonded using force and heat. It is important that the gold stud bumps used for connecting the photodiode have a small size and uniform shape, as the high ductility of gold causes potentially high deformation of the ball with applied temperature and pressure. As the photodiode used in Prototype 1 had larger bonding pad dimensions, this was previously no issue. However, the Albis PDCS24L photodiode has a pad size of 70 x 70 µm and a pitch of 108 µm, which reduced the tolerance for bump size.

Suitable Au stud bumps were produced at HSN by the lab engineers using 17.5 µm Au wire, as well as fine-tuning the bonding parameters. This allowed the bump diameter to be reduced from 75-85 µm to 65-80 µm, as shown in Figure 17.

However, the shape of the Au stud bumps included long “tails”, protruding in random directions from the top of bumps. This tail is a remainder from the Au wire used in the ball formation, and could not be controlled with sufficient accuracy. Nevertheless, bonding was performed successfully, although occasional failures were found due to short-circuits between stud bumps.

The photodiode bonding process was the following: First, the Au stud bumps were coined: A 1 N force was applied to the top surface of the stud bumps at a temperature of 250 °C, using a silicon die. The photodiode was then bonded using a standard Au thermocompression flip-chip process with the Finetech pico die bonder: The photodiode is picked up, aligned using the overlaid images of the bonding surfaces, before the photodiode is placed on the stud bumps and bonded using force and temperature. A bonding force between 3-5 N was used, at 250 °C for 30 s. The lower bonding force was found to increase yield due to less bump deformation.

Figure 17: Stud bumps formed Si substrate, using 17.5 µm Au wire.

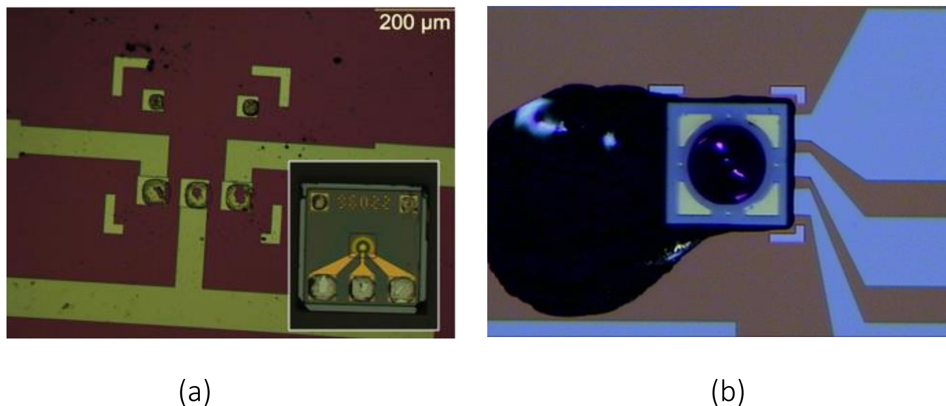
### 2.3.2 AuSn solder and underfill bonding

An alternative to the Au thermocompression bonding was investigated: Photodiodes with a thin (4 µm) layer of AuSn (80 % Au, 20 % Sn) solder deposited on the photodiode bonding pads were delivered by Albis. This solder has a melting point of 280 °C and the photodiodes were therefore bonded in two steps: First by applying 1 N force at 250 °C for 30 s, then 300 °C without force. The first step was intended to bond the photodiode with a weak bond. In the second step, the solder melts, creating the final, stronger bond.

The mechanical properties of the AuSn solder bond are different from the Au solder. Whereas Au is ductile at low temperatures, AuSn solder does not undergo stress relaxation, and may therefore transfer more stress to the chip. In addition, due to the CTE-mismatch between InP and Si, high shear stresses may be induced in the thin AuSn layer. However, due to the small size of the photodiode, these effects are likely minimal. Furthermore, AuSn solder has been demonstrated to survive thermal cycling between 160 °C to and -196 °C (77 K) for chip attachment of silicon and GaAs dies on alumina substrates [53].

AuSn-soldered photodiodes were tested by thermal cycling between room temperature and liquid nitrogen. It was found that the bond was weak, as the photodiode later detached. A microscope image revealed that the break was at the interface between bonding pad, made from AuPd alloy, and the AuSn bump, as shown in Figure 18 (a). Furthermore, the thin (300 nm) AuPd layer was partly removed, which indicates that it was scavenged by the solder.

An epoxy underfill was therefore applied to increase the strength of the bond. Two types of epoxies suitable for cryogenic environments were tested: Master Bond EP29LPSPAO-1 BLACK and Stycast 1266. The properties of these epoxies were discussed in chapter 2.2.1.1. Small drops of epoxy were applied on the silicon substrate near the edge of the photodiode. Although the Master Bond epoxy has a relatively high viscosity, it was found to be able to flow under the photodiode, although slowly. The Stycast epoxy has a much lower viscosity and was able to flow under the photodiode with ease, as shown in Figure 18 (b). In both cases, no epoxy covered the top surface of the photodiode. Photodiodes bonded with this technique were later tested successfully in liquid helium, as described in section 3.4.3.




(a) (b)

Figure 18: (a): Silicon substrate after detachment of thermally cycled AuSn–soldered photodiode. Inset shows bonding side of detached photodiode. (b) AuSn-soldered photodiode underfilled by Stycast 1266.

## 2.4 Sample holder design and fabrication

During operation in the helium Dewar, the device is ordinarily located in a metal tube, for electromagnetic shielding, with a diameter of approximately 4-5 cm, as shown in Figure 2. Due to the relatively tight space, the optical fiber must be bent if the sample is placed vertically in the shielding tube. The PTB sample holders, shown in Figure 2, were designed this way, using edge mounted SMA-connectors. Therefore, use of this sample holder caused difficulty in inserting the sample without causing excessive stress and bending of the optical fiber.

A new sample holder was designed and fabricated to resolve this issue. As the PCB substrate used for the sample holder influences both the mechanical and electromagnetic behavior of the device, parameters such as substrate material and thickness, as well as the dimensions of the transmission lines, must be properly chosen.

In general, the substrate material should have low dielectric loss tangent and low variability in the dielectric constant in order to minimize electrical losses. Typically, FR-4-type materials are avoided for RF applications due high dielectric losses. Furthermore, the conductive transmission lines and connector must be able to transmit high-frequency signals beyond 10 GHz. The horizontal dimensions of the transmission lines determine the characteristic impedance, which should be close to 50 Ω in order to reduce mismatch-losses.

Two different sample holders were produced and tested. For both, an SMP-type (Sub-miniature push on) surface mounted RF connector was chosen, enabling a vertical coaxial cable connection. SnPb solder paste was used to connect the SMP-connector. The transmission line dimensions were found using an online calculator (https://www.microwaves101.com/calculators/864-coplanar-waveguide-calculator).

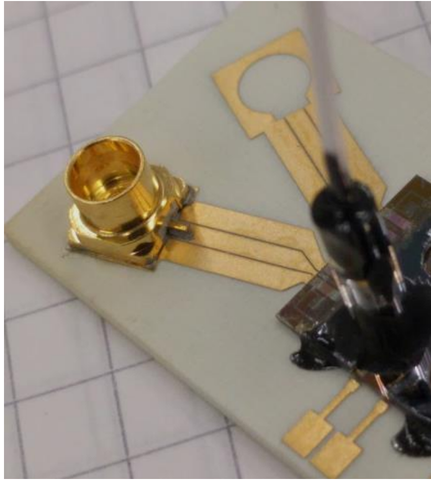
An external manufacturer, Hitech Circuits Co., was used to produce Rogers 4350b PCB boards with gold coated copper lines. A board with 2 mm thickness was chosen, based on the results described in section 2.2.1.1. This material is specialized for RF applications, having a low dielectric loss. Due to the relatively high maximum feature size and low

dielectric constant ($\epsilon = 3.48$) of the board, a relatively thick center conductor (1.00 mm) and a small ground plane spacing (0.10 mm) was used, giving a calculated characteristic impedance of 53 $\Omega$. The PCB can be seen in Figure 19 (a).

In addition, a leftover piece of a gold-plated alumina substrate of 0.5 mm thickness was used to produce a second sample holder type. A standard photolithography process was used to produce the gold pattern: The plate was covered by photoresist and exposed to UV light through a plastic mask. The photoresist was then developed and removed, before the exposed gold was removed.

Both sample holders were tested mechanically using dummy samples. Both sample holders were found to be suitable for attachment of the silicon substrate. However, mechanical attachment of the SMP-connector failed for the alumina sample holder when cooled with liquid nitrogen. This was most likely caused by the larger CTE-mismatch between the brass connector and the ceramic material, in addition to the high stiffness (Young's modulus of approximately 300 GPa) of alumina. Therefore, the PCB sample holder was used in all further tests.

A PCB with shorted transmission lines was brought to NPL for testing the RF properties. A time-domain reflectometry (TDR) measurement was performed, finding that the pulses from the sample holder were not significantly degraded, although some ringing was observed, indicating slight mismatch in characteristic impedance.



(a) (b)

Figure 19: (a) Rogers 4350b substrate with solder bonded SMP-connector and photodiode module after thermal cycling with liquid nitrogen. (b) Ceramic substrate showing delamination of gold layer, which caused failure of SMP-connector after cooling with liquid nitrogen.

# 3 Electrical characterization of the photodiode modules

In order for the photodiode module to be implemented in the JAWS system, the optically generated pulses must fulfill certain performance criteria, as outlined in section 1.7. In essence, a small pulsewidth in combination with high amplitude and low noise is needed for controlling the quantum step accurately. The photodiode should be able to deliver high frequency current pulses at clock frequencies of around 10 GHz or higher, with peak currents higher than 1 mA at 4 K. Additionally, long-term stability, without significant degradation of the performance is necessary for successful implementation of the module in the JAWS system.

The photodiode response to various types of optical and electrical input was tested both at room temperature and at temperatures down to 4 K. Several configurations of photodiode assemblies were tested in order to determine the role of effects such as alignment accuracy, type of substrate and interconnections. The test setups and sample specifications are described in the following chapter. Then, the results of tests are given.

| Sample | Photodiode | Substrate type | PCB/substrate |
|---|---|---|---|
| 1 | PDCS24L | Silicon, Nb lines | Rogers 4350b |
| 2 | PDCS24L | Silicon, AuPd lines | Rogers 4350b |
| 3 | PDCS24L on submount | - | Rogers 4350b |
| 4 | PDCS24L on submount | - | Alumina |

Table 1: Sample specifications.

## 3.1 Test setups and sample specification

### 3.1.1 Sample preparation

Four different sample types were prepared and tested, as listed in Table 1. Samples 1 and 2 consisted of photodiodes flip-chip mounted on silicon substrates, as described in chapter 2. The difference between sample 1 and 2 is that Nb is replaced with AuPd in the conducting lines in sample 2. This change was made to lower the resistance of the thin (200-300 nm) substrate tracks at room temperature. In sample 3 and 4, a photodiode mounted to a small (<1mm) ceramic submount with gold tracks is used, as shown in Figure 20 (a). The photodiode submount was bonded with epoxy directly to the PCB (sample 3) or to a large piece of ceramic substrate (sample 4). In sample 3, the submount is wirebonded to the PCB, while in sample 4, an RF probe is used to contact the photodiode, explained in detail in section 3.3.1.

The effect of changing parameters and module configurations, such as alignment accuracy/silicon substrate/PCB/connectors were of interest, in order to determine the effect of these factors on the frequency response. Thus, photodiode measurements on sample 1 and 2 include both substrate and PCB effects, sample 3 includes just PCB, while in sample 4, the substrate and PCB were removed altogether.

## 3.2 Optoelectronic test setup

DC currents were measured and reverse bias voltages to the photodiodes were applied with a Keithley 4630 sourcemeter.

An R&S ZVL vector network analyzer (VNA) was used to generate the signal and measure the scattering parameters (S-parameter) of the network between the output and input ports in the frequency range 10 kHz to 13.6 GHz. The $S_{21}$ scattering parameter has the meaning of *transmission coefficient* and was used evaluate the frequency response of the network. In the case of a VNA, where the impedance of port 1 and port 2 are identical, $S_{21}$ can be defined as:

$$S_{21} = \frac{V_2}{V_1}, \tag{18}$$

where $V_1$ and $V_2$ are the voltages at port 1 and port 2, respectively. Thus, $S_{21}$ is a measure of the response at the input port (port 2) due to a stimulus at the output port (port 1). In section 3.4.2, the measured frequency responses are shown as $S_{21}$ in decibel (dB), which by convention is given by:

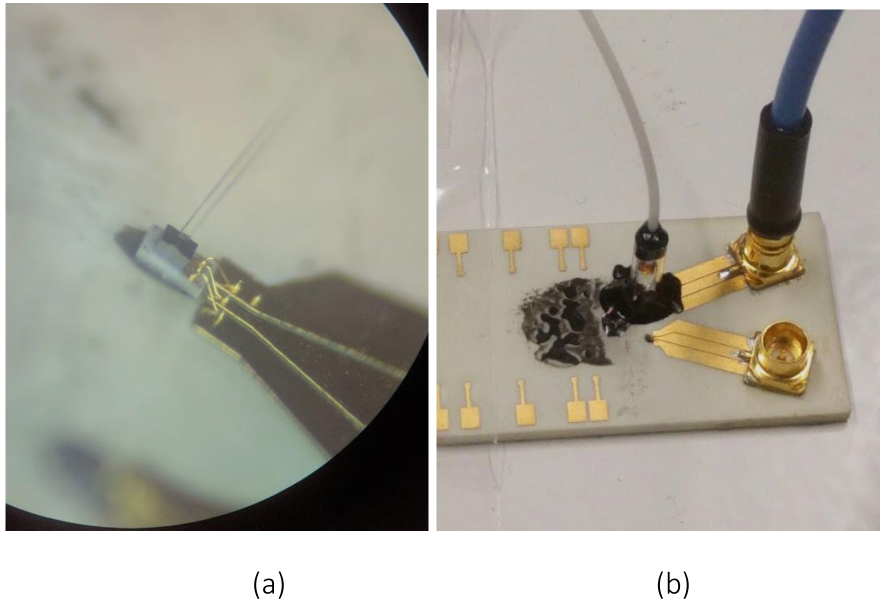
$$S_{21}(dB) = 20\log_{10}(|S_{21}|) \tag{19}$$

Since power is proportional to the voltage squared ($P \propto V^2$), a 3dB reduction in $S_{21}$ corresponds to halving the power ratio ($P_1/P_2$ ).

In the test setup, the network analyzer output was connected to a directly modulated Eudyna FLD3F10NPA DFB 1310 nm laser via a coaxial cable. The laser was also biased by a DC current to power the laser, and a bias voltage was applied to the integrated modulator. The laser is specified to have a -3 dB $S_{21}$ cut-off frequency above 10 GHz.

The optical signal therefore consists of a continuous wave combined with a small RF signal. The optical output from the laser was connected via an optical fiber to the photodiode. The signal output from the photodiode was connected to the input port on the VNA using coaxial cables. Bias voltages were applied to the photodiode by the sourcemeter via a bias tee. Therefore, the measured transmission coefficients include the effect of coaxial cables, laser diodes and optical fiber, in addition to the photodiode.

The RF output power of the VNA was set to 0 dBm, corresponding to 1mW. Since the RF signal is significantly attenuated in the modulated laser, the peak-to-peak power of the modulated optical signal is significantly lower than necessary to generate a RF signal with peak currents of around 1 mA in the photodiode. Therefore, the results only gives an evaluation of the frequency response to a *small signal.* A more sophisticated test setup using RF amplifiers would be required to generate a higher-powered optical RF signal.



(a) (b)

Figure 20: (a) Sample 3: Microscope image of photodiode on ceramic submount adhesively bonded and wirebonded to a Roger4350b PCB. A bare optical fiber is manually aligned for testing. (b) Sample 3 after bonding of the alignment sleeve and optical fiber ferrule.

## 3.3 Low temperature measurement setup

Samples 1, 2 and 3 were directly immersed into liquid helium by lowering the devices into the Dewar. A 2 m coaxial patch cable was used between photodiode and the VNA, while a 1 m optical fiber patch cord was used between the laser output and the photodiode to extend the cable length in all measurements.

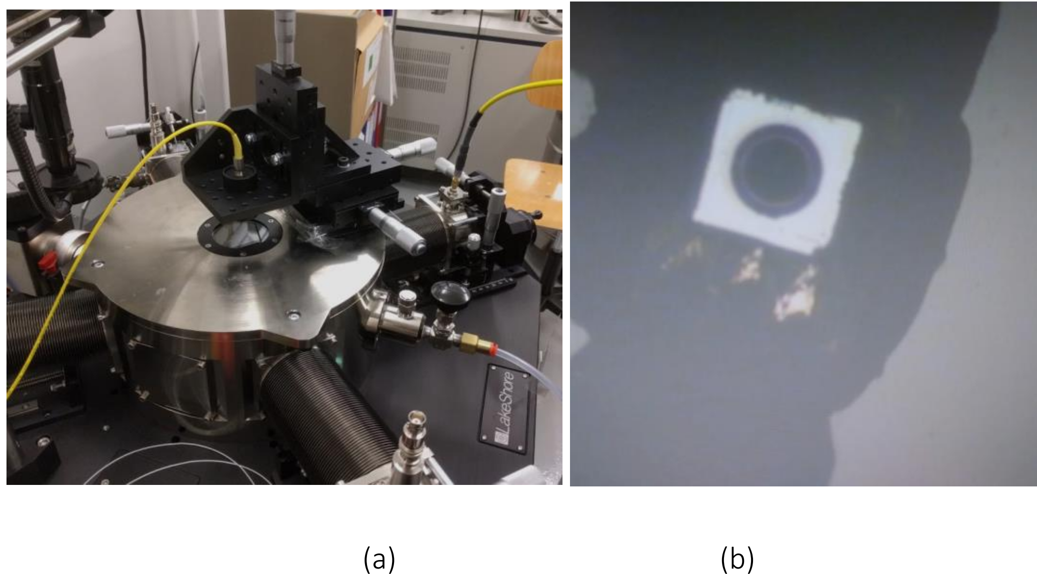
### 3.3.1 Cryoprobe setup

Sample 4 was tested at temperatures ranging from 300 K to 20 K using a Lakeshore CPX cryogenic probe station. Here, the device was tested by aligning an RF probe directly on the chip submount, as shown in Figure 21 (b). The sample was cooled by placing the sample on the cold plate of the vacuum chamber of the probe station, which was cooled using liquid helium.

The optical beam was transmitted from outside the probe station through the top cryoprobe window, while the inner window was removed, as it is opaque to infrared light.

Although the removal of the inner window may cause temperature fluctuations to increase, cooling to low temperatures is still possible.

The optical beam was focused using a biconvex lens with effective focal length of 25 mm. The lens and the optical fiber was fitted to a micrometer stage using an angle bracket placed on the cryoprobe lid, as seen in Figure 21 (a).




(a) (b)

Figure 21: (a) Optical assembly on cryoprobe. The output optical beam is focused from an optical fiber patch cable through the cryoprobe glass window. (b) Image showing photodiode mounted on submount (sample 4) and glued to piece of ceramic material. In the bottom left corner, the RF-probe can be seen.

## 3.4 Results

### 3.4.1 DC characteristics

Several measurements were made to find the photodiode response to continuous optical power as well as different bias voltages. The maximum photocurrent and responsivity are main objects of interest, as relatively high peak currents, up to 10 mA, are required to operate the Josephson junctions. The photodiode responsivity (Photocurrent/Optical power) was estimated by illuminating the photodiode with a 27 mW 1310 nm fiber-coupled laser source. The optical fiber was manually aligned using a micrometer stage and the photocurrent was measured for varying laser currents. The corresponding optical

power was also measured with an optical power meter. The photocurrent vs. optical power is shown in Figure 22. At low optical power, the responsivity was close to 0.9 A/W, which is above the minimum value stated in the data sheet. At higher optical powers, the responsivity dropped off, which is likely due to the high resistance of the Nb conducting lines (~50-100 Ω) at room temperature. An explanation of this is that the power dissipated in the resistive lines ($I_{PD}^2 \cdot R$) cannot exceed the absorbed optical power. Physically, this behavior is due to weakening of the electric field inside the photodiode for high currents/load.

The photodiode response to optical input at cryogenic temperatures was tested for several samples. In all cases, a slight drop in responsivity was observed. Figure 23 shows the photocurrent generated by sample 3 for varying laser currents at room temperature and at 4 K, using optical power up to 27 mW. With no applied photodiode bias, the maximum current decreased from 19.6 mA to 17.9 mA at 4 K, a drop of 9%.

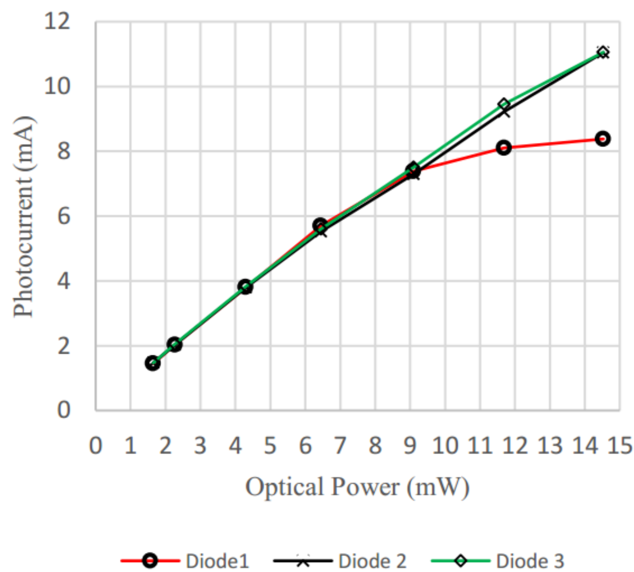



Figure 22: Photocurrent vs. optical input power for three photodiodes mounted on a silicon substrate, all measured at room temperature.

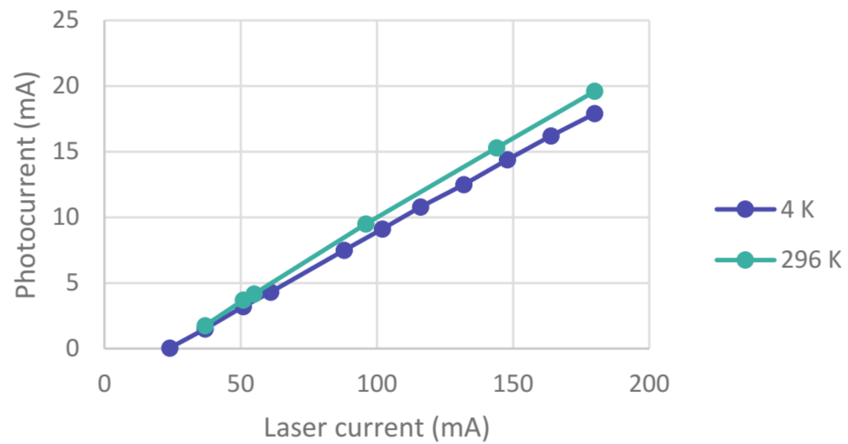



Figure 23: Photocurrent vs. laser current for a photodiode mounted on a Roger4350b substrate (sample 3)

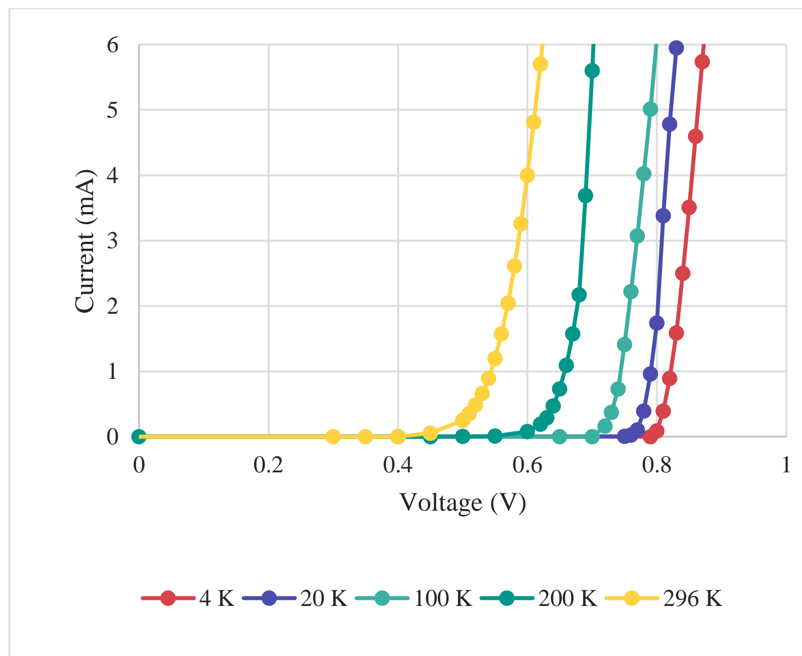



Figure 24: Current vs. voltage at temperatures 4-296 K. Results for 4 K was measured in liquid helium (sample 3), while the remaining results were measured in the cryoprobe (sample 4).

The I-V characteristics were measured at several temperatures from 4 K to room temperature. The results for sample 3 and 4 are given here, as sample 1 and 2 included the resistive lines. Sample 3 was operated in the cryostat from temperatures 20 K to 296 K, while sample 3 was measured at 4 K in liquid helium. The results, as shown in Figure

24, show that the threshold voltage increased from about 0.45 V at room temperature, to about 0.8 V at 4 K. This is consistent with the theoretical increase in band gap and decrease in thermal energy, which lead to an increase of the Fermi level at decreasing temperature.

### 3.4.2 RF characterization

While the photodiode is designed for signals up to 28 Gbps, the capability of the photodiode to produce pulses with these characteristics at low temperatures was uncertain at the start of the project. At various stages during the project, NPL performed tests on samples, both on mounted photodiodes and on the bare silicon carrier. These results indicated that the resistance of the transmission lines on the silicon carrier should be low, on the order of a few Ω, in order to achieve the shortest response time. Therefore, the thin Nb transmission lines needed to be in the superconducting state in order not to limit the transmission.

In order to compare the photodiode RF performance at 4 K to the performance at room temperature, samples with non-superconducting transmission lines were fabricated and tested. Silicon substrates produced by PTB, where 300 nm AuPd was used rather than 200 nm Nb, were found to be unsuitable, as the resistance of the various AuPd line sections were measured to be still relatively high, around 15 – 30 **Ω**, for line segments of length between 5-10 mm. Furthermore, there was no significant drop in resistivity with cooling to 77 K. Figure 25 shows the frequency response measured at room temperature for sample 2. It can be seen that the transmission coefficient $S_{21}$ rapidly dropped off at increasing frequencies and was dominated by noise at the highest frequencies. It was therefore concluded that it was not possible to perform the room-temperature photodiode characterization without high attenuation using the silicon substrates.

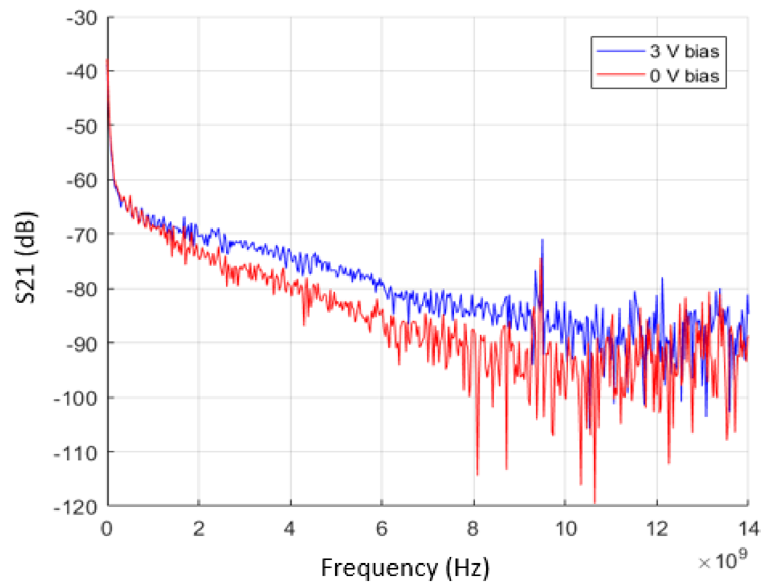



Figure 25: Frequency response ($S_{21}$) of sample 2 from 100 kHz to 14 GHz at room temperature for 0 V and 3 V reverse bias.

In order to remove the influence of the resistive transmission lines altogether, photodiodes flip-chip mounted on small ceramic submounts, less than 1 mm in length, were procured from Albis and were prepared as described in section 3.1.1 (samples 3 and 4). In addition, a commercial high-speed InGaAs photodiode module from Albis, PQW20A, was used to make a comparison to the prepared samples. Sample 3 was first measured using a manually aligned optical fiber. A 2 m coaxial patch cord was used between the photodiode output to the bias tee in all later cryogenic measurements. For comparison, a short (10 cm) SMP-to-SMA cable was connected directly to the bias tee for sample 3 in some measurements. Figure 26 shows the frequency response taken at room temperature for sample 3, 4 and PQW20A. The highest absolute response was measured for sample 3 with the short cable and the manually aligned photodiode. The permanent fiber bonding and insertion of the 2 m patch cord reduced the frequency response slightly, by approximately 4 dB.

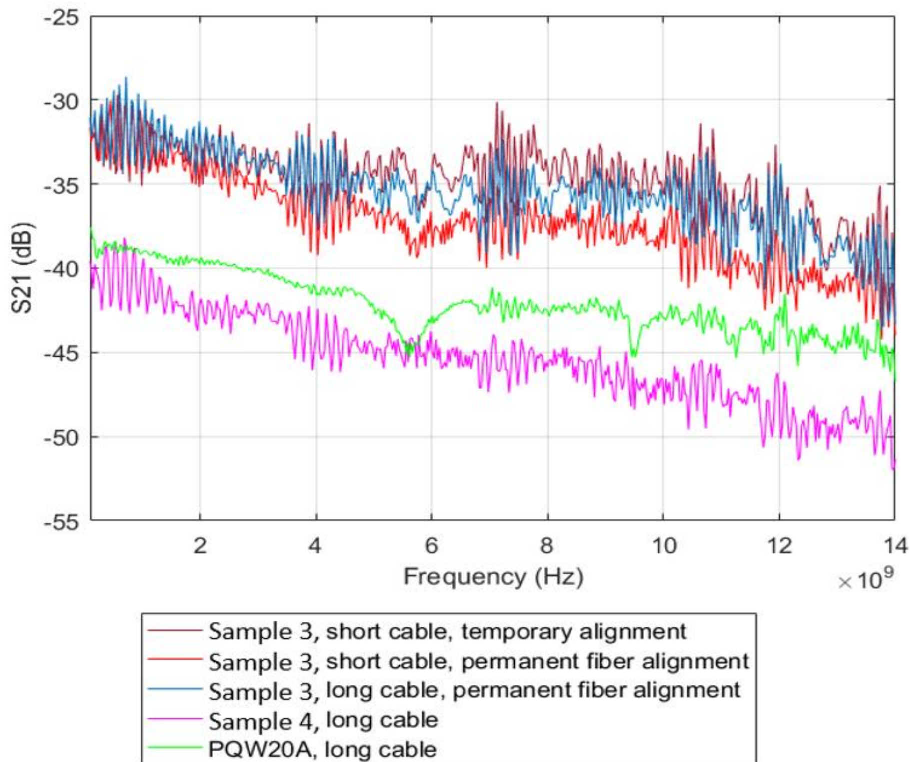



Figure 26: Frequency response ($S_{21}$) for different configurations, measured at room temperature.

In comparison, the frequency response of the PQW module was up to 5 dB lower compared to sample 3 and 4. This is likely due to the use of a 50 Ω matching resistor at the photodiode output of the PQW module, which reduces the photodiode current output by 50 %.

For sample 4, the reduction in coupling efficiency due to the lens focusing reduced the frequency response by up to 10 dB compared to sample 3.

There were large oscillations in the frequency response for sample 3 and 4, by up to 3 dB, with a period of approximately 125 MHz. Likely, this is due to impedance matching issues in the electrical connection between the photodiode and the VNA. By contrast, these oscillations were not present for the PQW20A module. The integrated biasing impedance matching circuit used in this module may explain the reduction of these oscillations.

The measurements were repeated at low temperatures for sample 3 and sample 4. Sample 3 was immersed in liquid helium, while sample 4 was placed in the vacuum

chamber of the probe station, which was cooled with liquid helium. The sample temperature of sample 4 could not be determined accurately, as the temperature in the probe arm was higher (20 K) than the temperature at the sample stage (4 K). Likely, the temperature was closer to 20 K than 4 K due to the thermal resistance from the sample stage to the photodiode. The I-V-characteristic of the photodiode also showed a lower threshold current than was measured for sample 3 in liquid helium.

Frequency response measurements taken at 4 K and 20 K, compared to room temperature measurements, are shown for sample 3 and 4 in Figure 27 and Figure 28, respectively. The results show that the relative frequency response at 4 K was not degraded compared to room temperature. Rather, the measurements show that the photodiode may be operated at full speed at very low reverse bias voltages. At 10 GHz, the change in frequency response when increasing the reverse bias from 0 to 3 V was less than 1 dB for sample 3.

For sample 3, in liquid helium, the frequency response decreased slightly, by about 1.5 dB compared to room temperature. Partly, this can be explained by the drop in responsivity with lower temperature, as was shown in Figure 23, which may be caused by increased misalignment due to thermal deformations.

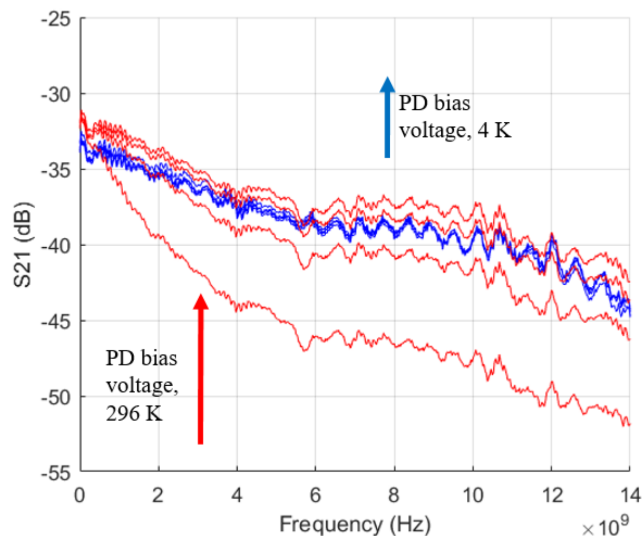



Figure 27: Frequency response ($S_{21}$) at room temperature and 4 K for sample 3.

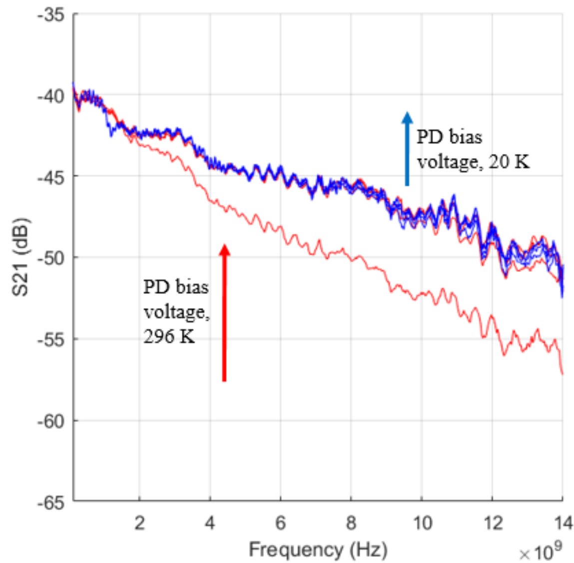



Figure 28: Frequency response ($S_{21}$) at room temperature and 20 K (approximately) for sample 4.

### 3.4.3 Long term stability

The ability of the photodiode to withstand both thermal shock and thermal cycling is of high importance. In this context, long-term reliability means the ability of the photodiode module to operate without failure during its service life. For use in JJA modules, the photodiode should be expected to operate for hours at a time and tens of thermal cycles between room temperature and 4 K.

Damage to the photodiode may occur due to excessive thermomechanical stresses, for example caused by the photodiode bonding. Degradation of photodiode performance is typically manifested in an increase in dark current at reverse bias, which for planar photodiodes is likely due to degradation of the metal contacts [54].

Of around 20 samples tested, degradation of the photodiode response was found in several photodiodes. However, a complete accounting was not made. The failures were observed as a loss of the typical diode I-V- behaviour. Rather, the device resembled a diode and a resistor in parallel, with significant dark current (> 1 mA) at reverse bias.

Electrostatic discharge (ESD) may be the cause of failure in some photodiodes, as no precautions against this was taken during the testing. NPL previously reported protecting the photodiode with Schottky diode to eliminate this effect.

The cause and time of failure cannot be established with certainty, as a systematic study was not performed. However, several photodiodes were tested in liquid nitrogen and helium with no degradation of performance. Some failed photodiodes were observed after storing the sample for several week/months.

The I-V response of four photodiodes bonded with Au stud bumps were tested at NPL, during thermal cycling between room temperature and 4 K using liquid helium. The photodiode resistance (U/I) at 0.9 V forward bias is shown in Figure 29 for the four photodiodes. After the first immersion, the result is relatively stable for the four photodiodes, although there is an indication of increased resistance after the first immersion.

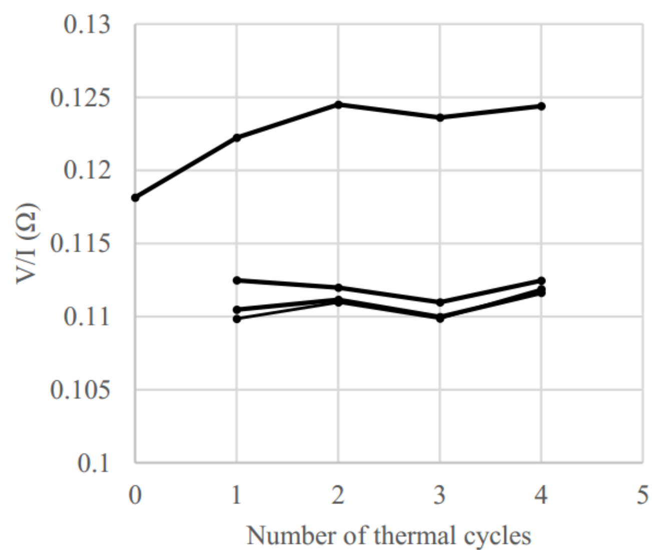



Figure 29: Photodiode resistance (voltage/current) at room temperature for sample 1 versus number of thermal cycles between room temperature and 4 K. Each line corresponds to an individual photodiode. Since the length and width of the resistive Nb lines vary, the measured values also vary between photodiodes.

The response of some AuSn-soldered photodiodes, as described in section 2.3, was tested during several thermal cycles between room temperature and 77 K (liquid nitrogen). One sample was cycled 10 times in liquid nitrogen, before being tested in liquid helium for more than one hour. The sample was stored for several weeks between the two tests.

The results showed that the dark current at -2 V reverse bias was stable and remained lower than 1 nA at room temperature during the test cycles. The I-V-response before the first cooling, after 10 cycles in liquid nitrogen and after cooling with liquid helium is shown in Figure 30. Below the threshold voltage, the change in current for a given voltage was up to 40%. Near the threshold voltage, the current was increased by up to 7%, while at voltages higher than 0.7 V, the change was less than 5%.

The AC-response of a single photodiode was also tested during an extended period in liquid helium. After 30 minutes of continuous operation, the change in frequency response compared to the initial measurement was less than 1 dB for all frequencies, as shown in Figure 31.

In one separate case, a photodiode under test was found to suddenly degrade in performance during testing in liquid helium. This failure occured during the immersion, and was observed as a sudden drop in frequency response. When testing the photodiode with a 27 mW laser in reverse bias, the photodiode appeared as being short-circuited.

To conclude, the long-term stability of the photodiodes is promising, as stable performance both during cold operation and after thermal cycling was demonstrated. However, occasional failures were observed. As the data is limited, a more controlled study is needed to determine the failure modes.

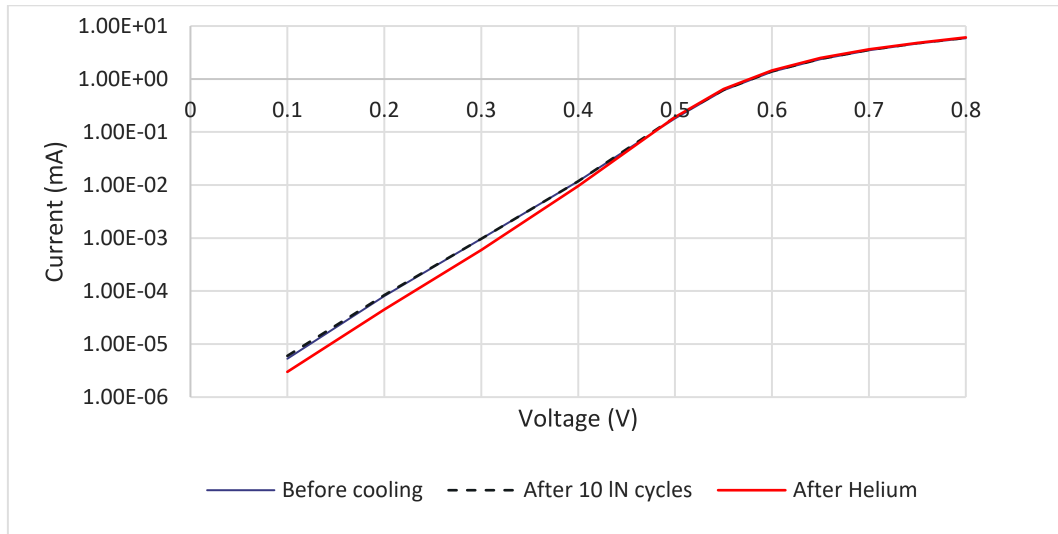



Figure 30: Current vs. voltage at room temperature for sample 2 after thermal cycling using liquid nitrogen (lN) and liquid helium.

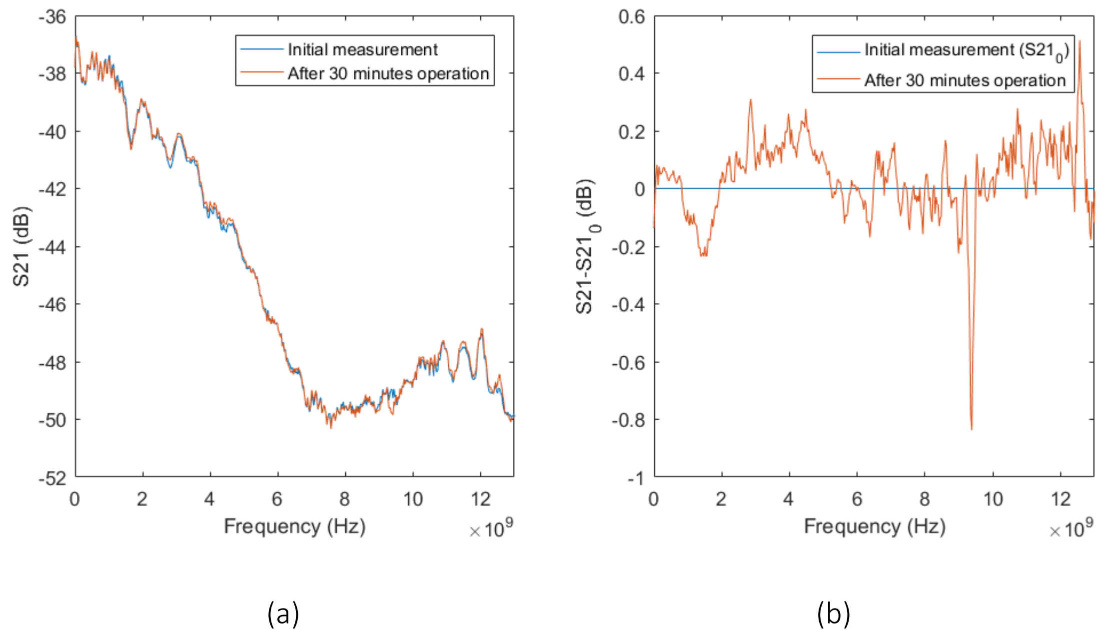



Figure 31: (a) Frequency response for sample 2 at 4 K at two different times: Initial measurement and after 30 minutes in liquid helium. (b) Change in frequency response after 30 minutes of continuous operation in liquid helium.

## 3.5 Low-temperature simulation of photodiode

As outlined in section 1.5.2, fundamental phenomena such as incomplete ionization, tunnelling effects, and the temperature-dependence of physical parameters will affect the response of the photodiode. In order to better understand the photodiode behavior at low temperatures, work was initialized to develop a numerical model to simulate carrier transport in a generic InGaAs/InP photodiode model.

Due to the high complexity of semiconductor modelling and unknown material properties, the following results describe the numerical approach and some early results. Therefore, in the following, results are only preliminary and are given to highlight the numerical challenges and uncertainties. A deeper theoretical basis and further work in developing the simulation model is therefore necessary. In particular, modelling the carrier transport at the heterojunctions needs a firm theoretical basis. In future work, the simulation results should be compared with measurements of photodiodes with known layer structure.

### 3.5.1 Model description

A simple, InGaAs/InP photodiode is considered, consisting of a three-layer structure: P-InP/I-InGaAs/N-InP. The doping concentrations and layer thicknesses are given in Table 2.

| Layer type | Material | Thickness | Doping density | Ionization energy |
|---|---|---|---|---|
| P-doped | InP | 1 µm | $N_A = 1 \cdot 10^{24}/cm^3$ | $\Delta E_A = 25\ meV$ |
| Absorption layer | InGaAs | 1 µm | $N_D = 1 \cdot 10^{21}/cm^3$ | $\Delta E_D = 5\ meV$ |
| N-doped | InP | 0.5 µm | $N_D = 1 \cdot 10^{24}/cm^3$ | $\Delta E_D = 5\ meV$ |

Table 2: Model specification

For solving the drift-diffusion equations, an FEM model using COMSOL's *Semiconductor* module was found to have convergence issues for temperatures below 20 K. A possible reason for these issues is the use of the intrinsic concentration $n_i$ as a reference value in equations; At low temperatures, $n_i$ approaches 0. As it appears as the divisor in some equations, round-off errors become significant.

To resolve this issue, the *Coefficient Form PDE* and *Electrostatics* modules were used to solve the drift-diffusion equations given by equations (9)-(15) and Poisson's equation. Furthermore, a field-dependent velocity model is used to include velocity saturation.

The temperature-dependence of many material properties down to 4 K were unknown. These include hole and electron mobility in InGaAs and InP. Therefore, these properties were taken as parameters in order to understand their role in the photodiode response.

The equilibrium concentration of ionized dopants was treated as a function of free electron and hole concentrations ($N_D^+(n), N_A^-(p)$). Specifically, the equations are solved in MATLAB using the following algorithm for $N_D^+$ (and similarly for $N_A^-$) :

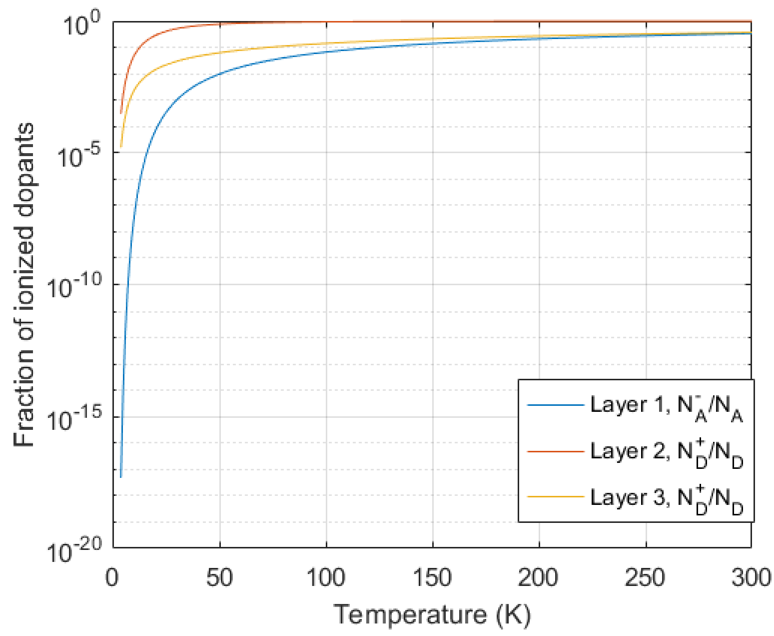
1. The Fermi level, $E_f$, was determined for a set of free carrier concentrations $\{n\} = n_0, n_1 \ldots$, by solving equation (9). The corresponding ionized dopant concentration $N_D^+$ was found from equation (13). The solutions were stored as an array.
2. The array was imported into COMSOL as a function which interpolates between the discrete set of solutions to give as a function $N_D^+(n)$.

At the boundaries (p-contact and n-contact), the charge was assumed to be 0:

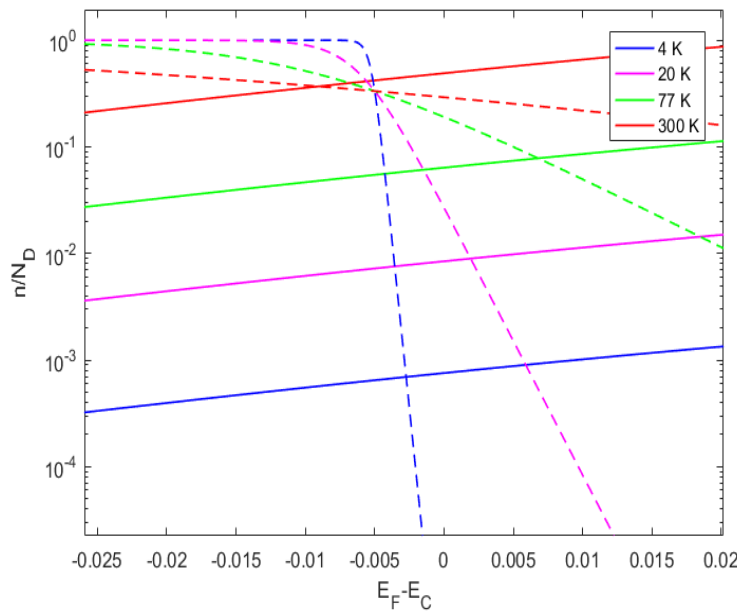
$$N_D^+(0) - n(0) = 0 \quad (20)$$

$$p(L) - N_A^-(L) = 0 \quad (21)$$

The fraction of ionized dopants, assuming charge neutrality, ($n_0 = N_D^+$ and $p_0 = N_A^-$), as a function of temperature are shown in Figure 32 (a). At temperatures near 4 K, the concentration of ionized dopants is much smaller than the doping concentration.




(a)




(b)

Figure 32: (a) Fraction of ionized dopants for layer 1-3. (b) Fraction of ionized dopants $\frac{N_D^+}{N_D}$ (dashed lines) and fraction of free electrons $\frac{n}{N_D}$ (solid lines) versus Fermi level $E_F - E_C$.

Correspondingly, the concentration of free carriers is reduced significantly compared to room temperature.

$N_D^+$ and $N_A^-$ are dependent on the carrier densities $n$ and $p$, however. Figure 32 (b) shows the dependence of the free electron concentration and ionized donor density to Fermi level, $E_F$, for four temperatures. At low temperatures, $N_D^+$ has a sharp dependence on $E_F$, while at higher temperatures, $N_D^+$ has a smoother dependence on $E_F$.

The photodiode has two heterojunctions at the two InP/InGaAs interfaces. As discussed in 1.5.2.2, transport across these interfaces are often modelled by thermionic/tunnelling mechanisms: Modelling these phenomena was attempted, but proved to be particularly challenging, due to convergence issues. Furthermore, at low temperatures, the model predicted that these barriers would limit the photodiode current significantly both for DC and AC-frequencies, which was inconsistent with experimental results.

There may be several explanations for this result:

- The model in itself may be invalid or incomplete. The drift-diffusion model (DD) may be extended or replaced with a *hydrodynamic* (HD) model, in which the local carrier temperature, $T_n$, may be different from the lattice temperature, $T_L$. By contrast, the drift-diffusion model assumes that the carrier energies are in thermal equilibrium with the lattice temperature $T_n = T_L$ [55]. For example, it has been shown that a HD model predicts much faster response time in InGaAs metal-semiconductor-metal (MSM) photodetectors than the DD model [56].
- The heterojunction in real devices have a more complex structure than the modelled structure. In particular, a graded heterojunction may be used to minimize carrier trapping [36].

As a simplifying assumption, in the following, the interfaces were treated as homojunctions, which posed no barrier to carrier transport.

### 3.5.2 Results

Simulations were performed for temperatures 300 K and 6 K. 6 K was used rather than 4 K because of numerical issues.

*Equilibrium concentrations and electric field*

Figure 33-Figure 35 show the carrier concentrations in dark field, corresponding space charge density and electric field at 300 K and 6 K. At both temperatures, a similar distribution of charge is found. However, at 6 K, the transitions are much sharper. While there is a significant concentration of free carriers in the intrinsic InGaAs-region at 300 K, it is completely depleted at 6 K. This effect, in addition to the increase in bandgap and Fermi-level change, lead to a higher overall electric field in the intrinsic layer.

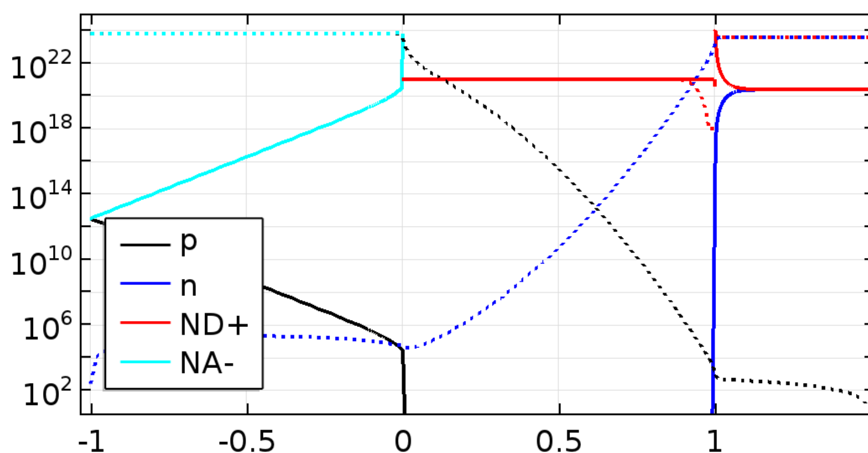



Figure 33: Carrier distributions ($n$, $p$) and ionized dopant distribution ($N_D^+$, $N_A^-$) at 300 K (dotted lines) and 6 K (solid lines).

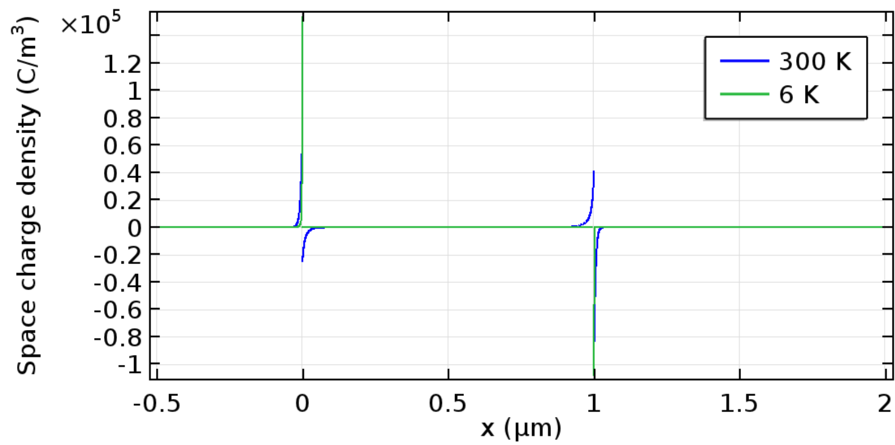



Figure 34: Space charge density ($N_D^+ - N_A^- + p - n$) at 300 K and 6 K.

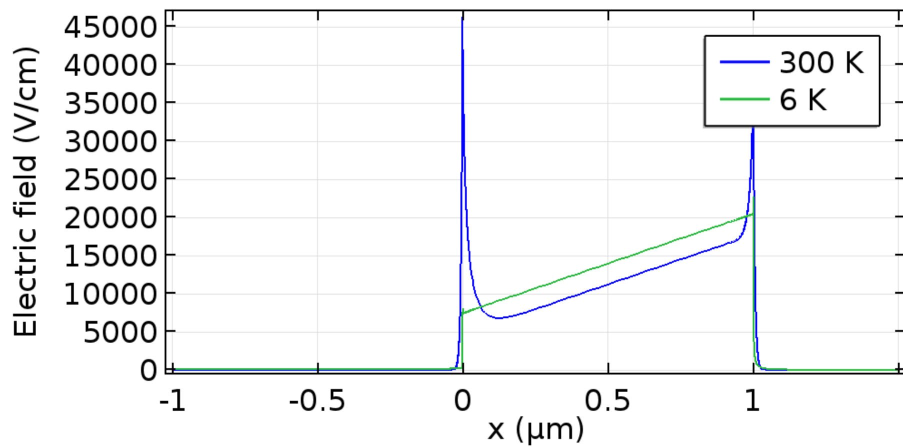


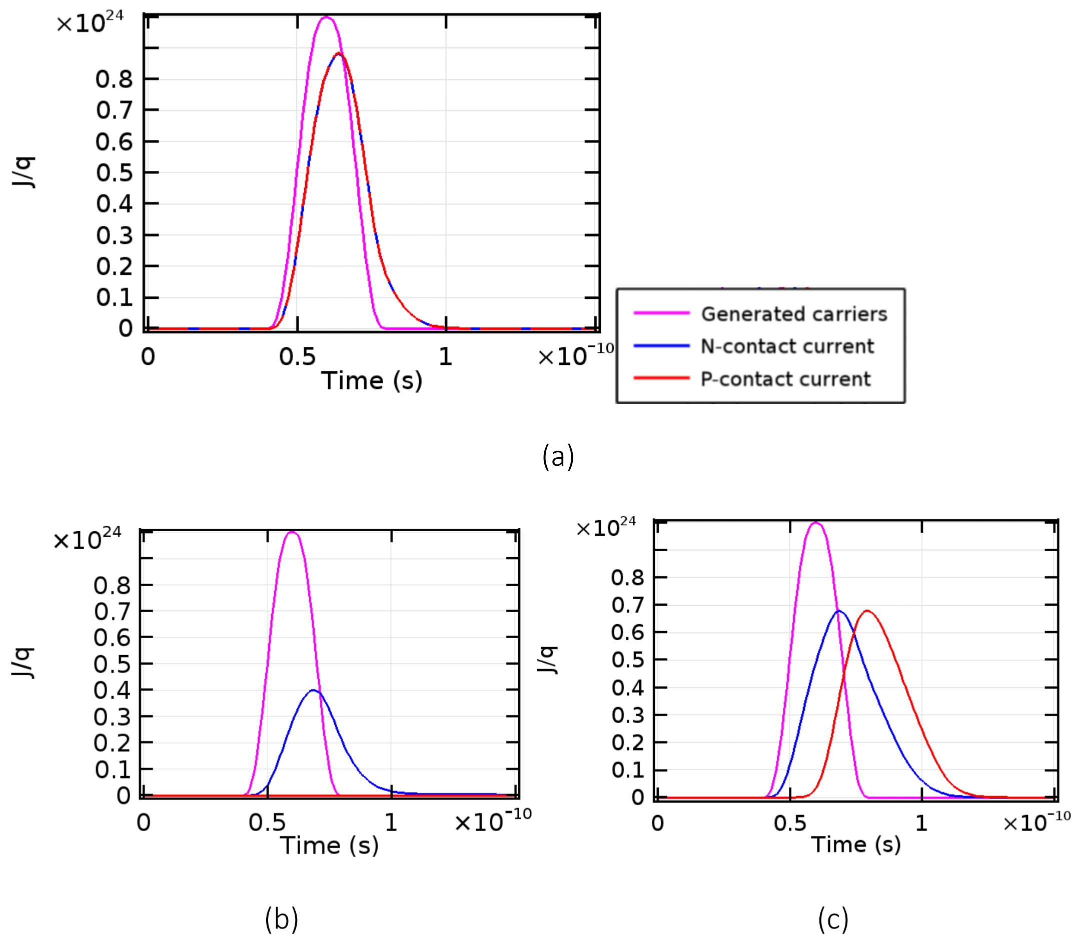

Figure 35: Electric field in photodiode at 300 K and 6 K.

*Pulse response*

Optical generation of carriers for short pulses was simulated by setting a time-dependent electron generation rate *G* in the InGaAs layer, in equation (15) (and similarly for holes). A Gaussian pulse with 20 ps rise time was used.

At 300 K, the simulated currents were identical at both contacts, with a fast pulse response, as shown in Figure 36 (a). At 6 K, the simulated current was dependent on the chosen values for the electrical mobilities in InP, as shown in Figure 36 (b) and (c). When the room-temperature values were used, the pulse response was significantly broadened

and delayed at both contacts, in particular for the hole current. This can be explained by the absence of an electric field in the N- and P-layers. The dominant carrier transport




(a)

(b)

(c)

Figure 36: Photodiode pulse responses for a Gaussian pulse input with 20 ps rise time at (a) 300 K and (b/c) 6 K. 0 V bias voltage were used in all cases. The color legend for all graphs is given in (a). The shown currents are taken at the N- and P-contacts. In (b) the hole and electron mobilities, are set to the room temperature values $\mu_n(6\ K) = \mu_n(300\ K)\ \mu_p$, while in (c), they are set to $\mu_n(6\ K) = 10\mu_n(300\ K)$ and $\mu_p(6\ K) = 400\mu_p(300\ K)$.

mechanism in these regions is therefore diffusion. As the diffusion coefficients are proportional to $T$, $(D = k\ T\mu/q)$, the carrier transport is slow. When the mobilities $\mu_n$ and $\mu_p$ were multiplied by 10 and 400 respectively, the response was improved, although it was still lower than the room-temperature results.

It should be noted that the simulated model does not include effects of an external circuit. These effects would include resistive, inductive and capacitive elements which would influence the voltage across the photodiode, and thereby the pulse-response.

# 4 Discussion

This work was undertaken to develop a solution to a particular packaging challenge for low-temperature environments. Therefore, the methods, materials, components and design were chosen to address the issue of thermal stress. Therefore, compared to state of the art developments in optoelectronic packaging, the results may not be directly transferable. On the other hand, recent trends in optoelectronic packaging have the potential of simplifying certain packaging challenges for low-temperature electronics. In the following, the results in each paper is discussed in regards to these aspects.

In Article 1, a general, broad review of devices and optoelectronics packaging for low-temperature environments was discussed. Since the paper does not contain new research, the main contribution is to summarize and introduce these aspects to other researchers in the field.

In Article 2, an assembly technique using silicon fixtures to align multiple optical fibers to photodiodes on silicon substrates was described. A main advantage of this technique is that it allows a rather cheap and fast solution that can be customized to the chip layout. It was also demonstrated that the structure was mechanically robust, and with the direct optical coupling structure, high photocurrents could be produced, which was a main target for this particular application. A drawback, however, is that the technique is rather time-consuming and dependent on the skill of the operator, and may therefore not be suitable for production of higher volumes. An additional drawback is the limitation in packaging density of the optical fibers; due to the relatively large size of the alignment sleeves/ferrules, the photodiodes must be spaced apart by several millimeters. Furthermore, the perpendicular positioning of the optical fiber ferrules leads to a high vertical profile.

If specialized optical connectors were developed and commercially available, these issues may be resolved. Other research groups specializing in optoelectronic packaging have demonstrated similar optoelectronic packaging techniques that may be adapted for this purpose. For example, using v-groove ferrules for aligning multiple optical fibers may

enable fiber connections with higher density. For example, a glass v-groove ferrule was used to couple light from optical fibers to vertical grating couplers in [41]. Furthermore, using v-groove modules, the vertical profile can be reduced by using optical fibers with an angled facet, which reflects the beam by a near right angle, as in [57].

In Article 3, a commercial photodiode was characterized at low temperatures. The bias voltage requirements at low temperatures were also investigated, and may be of general interest. The results confirmed the results from other groups; that InGaAs photodiodes operate with good performance at low temperatures. As the context of the Article 2 is the Q-WAVE/QuADC programs, the results shows the potential of using commercial photodiodes as current sources for JJA chips. However, more in-depth testing is needed, including the frequency response to optical pulses with higher optical power, capable of producing pulse currents with peak amplitudes above 1 mA.

In Article 4, the main contribution is the discussion of thermal stresses in an optical fiber structure at cryogenic temperature. The structure is similar, but is an alternative solution to that described in Article 2. Other groups have proposed and demonstrated similar structures for optical fiber attachment for cryogenic devices, e.g. [58, 59]. In Article 4 FEM modelling was used to analyze such stresses. The results highlight the importance of proper material selection for cryogenic applications, in particular for a multilayered structure, for reducing the chance of failure due to cracking in silicon. The results may also be of interest in the design of packaging for other superconducting devices.

# 5 Conclusions and outlook

The PhD-work demonstrated practical techniques for packaging and assembly of photodiodes and optical fiber coupling structures. Modules were produced that showed robustness against thermal cycling between room temperature and 4 K. Initial issues with chip cracking were eliminated by replacing ceramic alignment sleeves with borosilicate sleeves. The result was in agreement with thermomechanical simulations.

Assembly of multiple optical-fiber connections on a 20 x 10 mm silicon substrate was demonstrated using laser cut silicon fixtures.

The capability of the photodiodes to produce DC currents above 15 mA at 4 K was demonstrated, while the frequency response of the photodiode was shown to not be negatively affected by cryogenic temperatures. Further work is necessary to determine the response to short optical pulses with peak power above 1 mW, capable of producing current pulses with peak amplitudes above 1 mA. The reverse bias requirement at 4 K can then be determined. Furthermore, the optical biasing concept can be investigated to determine potential advantages, for example in terms of reduced noise compared to using an external bias source.

The long-term reliability of the photodiode at 4 K must be studied further. Some results given here indicate that the electrical response may slightly worsen between each thermal cycle due to thermal stresses. While the mechanical attachment of the photodiode has remained strong in all tests, high stresses in the metallic contacts of the photodiode may lead to degradation of electrical response.

Developing a valid low-temperature simulation model of the photodiode response is an interesting prospect. However, the results found that numerical issues and peculiarities become pronounced at low simulated temperature. Furthermore, data of low-temperature material properties are lacking for many materials, which increases the uncertainty of the results. Combining a photodiode-model with a transmission line/JJA-model may bring interesting results and may be able to better predict photodiode response at high optical power.

To conclude, the results have shown that an optoelectronic module operated at 4 K is feasible, but further work is still needed to validate the concept.

# 6 Summary of papers

*Journal Papers*

## Article 1

In this article, developments and techniques related to optical-fiber-coupled devices operating at cryogenic temperatures were reviewed. Superconducting devices such as transition edge sensors, superconducting nanowire single photon detectors as well as types of Josephson electronics was described. Optical fiber assembly structures, bonding and mechanical properties of materials for cryogenic temperatures was reviewed.

## Article 2

The assembly of an optoelectronic module structure was described. Flip-chip assembly of photodiodes and silicon fixtures for alignment of multiple optical fiber on a silicon substrate was demonstrated. The electrical response to a continuous wave laser inputs was measured at room temperature and at 4 K by direct immersion in liquid helium. The results shows that the assembly technique could facilitate a stable and efficient optical coupling. This paper is an extension of the work presented in Article 5.

Note to article 2: Figs. 1(a) and 5 were reused from Article 5 without proper copyright notice. The correct captions are given here:

- Fig. 1. (a) Silicon carrier, measuring 10 × 20 $mm^2$. Bardalen, E., et al. *Packaging of fiber-coupled optoelectronic module for cryogenic voltage standards*. in *Electronic System-Integration Technology Conference (ESTC), 2016 6th*. 2016. IEEE. ©2016 IEEE. (b) Top view of lensed photodiode.
  photodiode.
- Fig. 5. Images taken by the flip-chip bonding system. (a) Over-layered images of the silicon fixture and the carrier. (b) and (c) Photographs after placement and final alignment of the fixture, showing the details near the bonding pads and the overview. Bardalen, E., et al. *Packaging of fiber-coupled optoelectronic module for cryogenic voltage standards*. in *Electronic System-Integration Technology Conference (ESTC), 2016 6th*. 2016. IEEE. ©2016 IEEE. (b) Top view of lensed photodiode.

## Article 3

The frequency and DC-response of commercial InGaAs/InP photodiodes were tested at room temperature and at temperatures down to 4 K. The frequency-response to a small signal was measured with a vector network analyzer and a directly modulated 1310 nm laser. The results show that the responsivity of the photodiode is not significantly reduced at low temperatures at frequencies below 14 GHz. At 300 K, reverse bias voltages of up to 3 V was required for the highest bandwidth, while at 4 K, the photodiode was operated at nearly full speed even at 0 V reverse bias.

## Article 4

The reliability of a photodiode module intended for operation at 4 K was investigated. Flip-chip bonded photodiodes and an adhesively bonded optical fiber attachment structure were considered. Finite element simulations of the thermomechanical stress were used to evaluate the stresses in different design configurations. Results showed that issues with chip cracking in silicon were eliminated by proper selection of component materials. Photodiode modules were shown to survive thermal cycling to 77 K and extended operation in 4 K.

*Notes to Article 4*: Figure 3 is reused from Article 5 and shows a photodiode bonded using Au stud bumps. In Article 4, it may be interpreted as being bonded using AuSn solder. However, this does not change the results of the article, as the intent of Figure 3 was to show cracking caused by the adhesively bonded fiber structure.

Fig. 3 was reused from Article 5 without proper copyright notice. The correct caption is given here:

- Fig. 3. Microscope image showing cracking in silicon substrate after cooling down to 4 K. Bardalen, E., et al. *Packaging of fiber-coupled optoelectronic module for cryogenic voltage standards*. in *Electronic System-Integration Technology Conference (ESTC), 2016 6th*. 2016. IEEE. ©2016 IEEE.

*Conference Papers*

## Article 5

A technique for assembling multiple optical fibers was developed, using silicon fixtures for mechanically aligning and fixing borosilicate alignment sleeves. In order to simplify assembly, the fixture is aligned by the flip-chip technique and adhesively bonded to the carrier with an epoxy. Sufficient alignment accuracy has been achieved, with an average misalignment of 13 µm between the fixture and the photodiode position. Testing of an assembled module showed promising behavior, achieving a stable optical coupling when immersed in liquid nitrogen and having sufficient strength for operation down to 4 K. This conference paper was later extended and published as Article 2.

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