Electrical, Mechanical, and Hermetic Properties of Low-Temperature, Plasma Activated Direct Silicon Bonded Joints

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The electrical, mechanical, and hermeticity properties of low-temperature, plasma activated direct silicon bonds were investigated. On individual dies with a bonding area ranging from 1–4 mm^2, the bonded interface was found to have a capacitance ranging from 2.62 pF/mm^2–2.89 pF/mm^2 at 1 kHz. Linear I-V curves showed ohmic behavior without hysteresis. A resistance around 2.2 Ω and a current density of 1.1×10^4 A/m^2 was measured at DC. We speculate that the capacitive and resistive responses are related to traps that are formed during the plasma activation process. The applied bonding process resulted in hermetic sealing with 100% yield on 2×481 dies. The maximum leak rate of the seals was 2.4×10^{-11} $mbar \cdot l \cdot s^{-1}$, but could be significantly lower. No gross leaks were observed following a steady-state life test, a thermal shock test, and a moisture resistance test applied on 100 dies.
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Silicon direct bonding is used in several application areas of commercial importance, including silicon-on-insulator material, power electronics, light emitting diodes, and micro electro-mechanical devices.[1] For many applications, the high temperatures required in conventional silicon direct bonding present a problem. Low-temperature bonding enabled by for instance plasma activation, i.e. plasma bonding, is one method for solving the problem.[2] The method and its mechanism have been subject to thorough studies.[1–13] However, studies investigating parameters that are relevant for device applications, presenting measurements on larger number of devices, are scarce. To our knowledge, only one estimate of the leak rate across plasma bonded seals has been presented,[8] and one study presents simultaneous measurements of surface energy and electrical properties.[12]

The current paper aims at assessing properties of plasma bonded seals which are relevant for device applications. We have investigated the electrical, mechanical, and hermetic properties of bonded interfaces resulting from one specific process, which was based on our earlier investigations of process parameters.[13] Further, to our knowledge, we report on the first assessment of the hermeticity of plasma bonded dies which have been subjected to environmental testing. Measurements were conducted on sample sets of 4–481 samples to reduce the uncertainty of the results.

Experimental

Two types of test laminates were prepared: hermeticity laminates (Herm), and laminates for electrical and mechanical measurements (ElMech). Cross-sectional sketches of the die types are shown in Figure 1.

Two Herm laminates were manufactured by bonding a top wafer with membrane structures to a plain silicon wafer. Two double-side polished, ⟨100⟩-oriented, n-type wafers of diameter 150 mm, resistivity 1–2 Ωcm and thickness 280 μm had a 750 nm thick thermal SiO_2 with 481 quadratic openings. Membranes were made by tetra-methyl ammonium hydroxide (TMAH) etching, resulting in membranes with a side edge of 2.5 mm and of thickness 41 μm. The SiO_2 mask was removed in buffered HF (BuHF). The top wafers were bonded to one-side polished, ⟨100⟩-oriented, n-type, 150 mm diameter, 525 μm thick silicon wafers with resistivity 2–20 Ωcm, as described below.

Two ElMech laminates were manufactured by bonding structured wafers to blanket silicon wafers. The structured wafers contained 169 frame structures of outer dimension 3×3 mm^2 and widths of 100, 200, or 400 μm, with or without rounded corners. In addition to the frames, other structures were included to increase the total bond area of the wafer to 38% of the total wafer area. The frame designs and the wafer layout are shown in Figure 2. The design dimensions and number of chips per wafer is found in Table I. The frames were protruding 6 μm above the silicon surface. They were realized on double-side polished, ⟨100⟩-oriented, p-type, 150 mm diameter, 300 μm thick wafers with resistivity 0.01–0.02 Ωcm by deep reactive ion etching (DRIE) applying a 750 nm thick SiO_2 mask. The SiO_2 mask was removed in BuHF after DRIE. The structured wafers were boron implanted with a dose of 2×10^{15} cm^{-2} at 50 keV on both sides. The structured wafers were bonded to double-side polished, ⟨100⟩-oriented, p-type, 150 mm diameter, 300 μm thick silicon wafers of resistivity 0.01–0.02 Ωcm. One of these wafers was boron implanted with a dose of 2×10^{15} cm^{-2} at 50 keV on both sides. The implants were activated by a furnace process at 900°C for 60 minutes in N_2 ambient.

Wafer lamination and annealing.— All wafers to be bonded were cleaned for 10 minutes in fresh cleaning solutions with NH_3, and HCl. Subsequently, all wafers were rendered hydrophilic in NH_3 and exposed to an O_2 plasma for 60 s in an AMS 200 (Alcatel) with a source power of 2500 W and a bias power of 180 W. After activation, the structured wafers were dipped in DI-water for 1 minute and dried. Laminates consisting of one structured and one plain silicon wafer were bonded in an SB6e (Suss) applying a bonding pressure of 350 mbar for 2 minutes at 50°C. The ambient pressure in the bonding chamber was below 5×10^{-3} mbar N_2.

Aluminum of thickness 1 μm was deposited on both sides of laminate ElMech1 and patterned to form separate contacts on one side. Laminate ElMech1 was then diced into four pieces: Q1–Q4. Q2 and Q4 from ElMech1 were annealed at 150°C for 72 hours. Q1 and Q3 from ElMech 1 and the entire laminate ElMech2 were annealed at

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Figure 1. Schematic cross-sections of Herm and ElMech dies. Light gray is silicon, dark gray is p^+-doped silicon, black is aluminum.

150°C for 6 hours. After annealing, ElMech laminates were diced into individual dies of size 6 × 6 mm^2 and subjected to characterization.

Herm laminates were stored in a cleanroom environment for five months after bonding. After the storage, Herm1 and Herm2 laminates were diced into a stripe of 2 × 25 membranes and two quarts: Q1 and Q2. The stripes were subjected to environmental stressing. The quarts Q2 were not further annealed. Q1 from Herm1 was annealed at 150°C for 6 hours, and Q1 from Herm2 was annealed at 150°C for 72 hours. Subsequently, both Q1 quarts were annealed at 600°C for 2 hours. Table II lists an overview of the four bonded laminates, their annealing and environmental stressing.

Environmental stressing.— The stripes from laminates Herm1 and Herm2 were subjected to environmental stressing consisting of a steady-state life test, a thermal shock test, and a moisture resistance test. The steady-state life test was done at 150°C for 1000 hours in an oven (Heraeus Instruments). The thermal shock test employed a two chamber system connected with a lift (Heraeus HT7012 S2). The top chamber was maintained at a constant temperature of +200°C and the bottom chamber was maintained at −65°C. A dwell time in each chamber of 10 min and a transition time of 7 s were employed. Consecutive exposure to both chambers was considered as 1 cycle and the samples were exposed for 50 cycles. The moisture resistance test was done in a chamber with controlled humidity and temperature (Sunrise E series). A 24 h initial conditioning of the samples at 80°C was done to completely dry out the samples. One complete cycle comprised of 7 steps and the relative humidity of the chamber was maintained at 90% for all the steps, as described in MIL-STD-883E. The selected temperature range was from −10°C to 65°C.

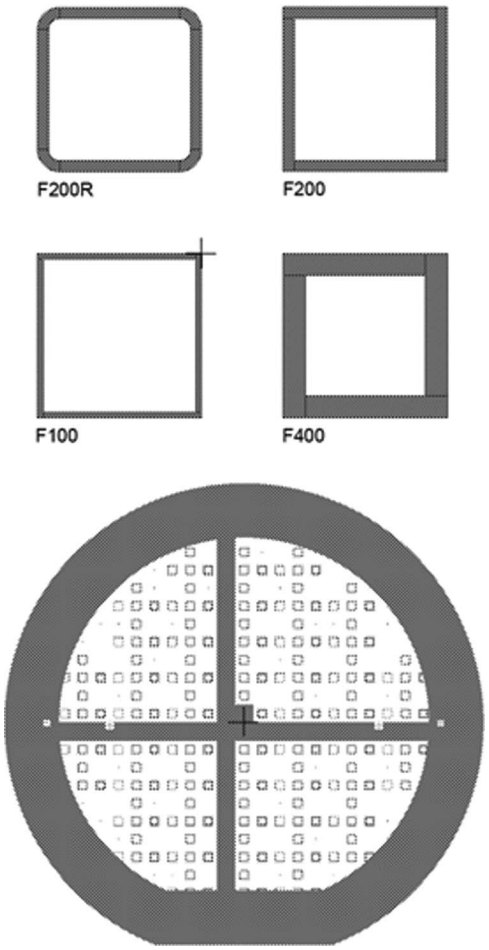

Figure 2. Top: Overview of the four test frames. Bottom: Overview of entire wafer. The gray area is the protruding bond area.

Table I. Frame dimensions and number of dies on the wafer.

Die name	Description	Bond area [mm^2]	No. of dies on wafer
F100	Straight corners, width 100 µm	1.16	37
F200R	Rounded corners, width 200 µm	2.14	47
F200	Straight corners, width 200 µm	2.24	50
F400	Straight corners, width 400 µm	4.16	46

Characterization.— The dicing yield, defined as the percentage of dies that did not delaminate during dicing, was counted on laminates ElMech1 and ElMech2. The tensile strength was measured on 9–12 individual dies of frame width 200 and 400 µm from laminate ElMech2, applying a MiniMat 2000 (Rheometric Inc.) pull tester. The dies were glued to flat-headed screws which were mounted in the pull tester. The applied force and the elongation were recorded, and the force at which the fracture occurred was noted. The fractured surfaces were inspected visually, and the amount of the bond frame where Si had been transferred from one wafer to the other (named 3D-fracture) was estimated to the nearest 10%. The tensile strength was calculates as the fracture force divided by the nominal bond area. The shear strength was measured by a DAGE4000+ (Nordson) on 5–7 individual dies of frame width 100–400 µm from laminate ElMech2.

Table II. Overview of the bonded laminates, annealing and environmental stressing.

Laminate ID	Metal contacts	Annealing	Environmental stressing
Herm1	No	All: RT storage 5 months Q1: first 150°C 6 h, then 600°C 2 h Q2: RT storage	Yes stripe of 2 × 25 dies
Herm2	No	All: RT storage 5 months Q1: first 150°C 72 h, then 600°C 2 h Q2: RT storage	Yes stripe of 2 × 25 dies
ElMech1	Yes	Q1, Q3: 150°C, 6 h Q2, Q4: 150°C, 72 h	No
ElMech2	No	150°C, 6 h	No

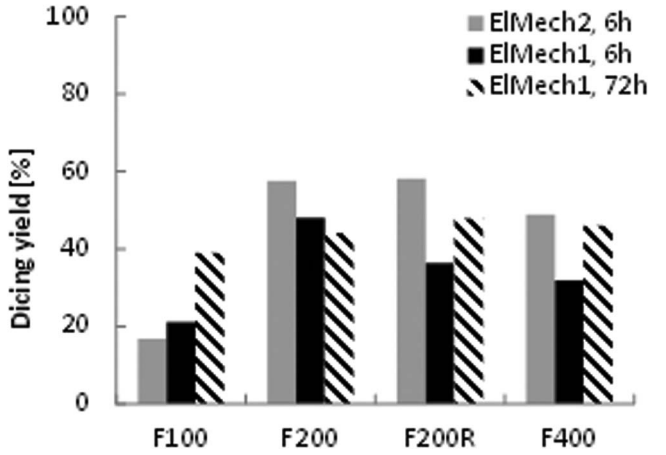

Figure 3. The dicing yield for dies of the different designs for the two ElMech laminates, showing the two different annealing times.

For most samples, the first fracture chipped a small part off the die. The remainder of the die could withstand a higher shear force before breaking completely. However, the mass [kg] at which the first fracture occurred was recorded, and the shear strength was calculated from this mass by multiplication by the gravitational constant *g* and division by the nominal bond area.

Electrical measurements were done on individual dies from laminate ElMech1. The capacitance between the two metal contacts was measured at 1kHz applying a LCR400 (Aim-TTi). Between 11 and 23 dies of each design were measured. The resistance between the two metal contacts was measured by a four-point probe setup using a SourceMeter 2602 (Keithley). The DC voltage was swept and the resulting current was logged. Four dies of each design were measured sweeping the voltage from minus 50 mV to 50 mV and back, and one die of each design was measured sweeping the voltage from 0 V to 2 V.

The occurrence of gas bubbles was investigated by scanning acoustic microscopy (SAM) on quarts Q1 and Q2 from laminates Herm1 and Herm2 after annealing at 150°C and after annealing at 600°C. A SAM450 (Tepla) with a 140 MHz acoustic head and 8 mm focal length was used.

The amount of inward deflection of the membranes on seven dies from laminates Herm1 and Herm2 was measured by a Zygo NewView 6300 white light interferometer (WLI). The deflection measurements were repeated after 22 days. The pressure difference between the inside and the outside of the cavity was calculated using Equation 1.[14] In the calculations, the nominal membrane dimensions were a = 2.5 mm and d = 41 μm were used along with the values $\upsilon = 0.28$ and $E = 1.65 \times 10^{11}$ Pa. The parameter w is the measured deflection and ΔP is the pressure difference.

$$w = (a^{4*}(1 - \upsilon^2)^*\Delta P)/\left(66^*d^{3*}E\right) \quad [1]$$

After environmental stressing, the membranes with inward deflection were identified by visual inspection and the number of membranes that had become flat was recorded.

Results

The dicing yield for both ElMech laminates is plotted in Figure 3. The dicing yield varied between 17% for F100 dies to 58% for F200R dies from laminate ElMech2. The dicing yield was lower for F100 dies than for the dies with wider frame widths. Applying a chi[2] test with a p value of 0.05, there was no significant difference in dicing yield between the laminates that had been annealed for 6 and 72 hours.

Typical individual curves for tensile strength and shear strength measurements are shown in Figure 4. Figure 5 shows all measured tensile strengths, and Figure 6 shows all measured shear strengths. Table III lists averages and standard errors for the measured tensile and

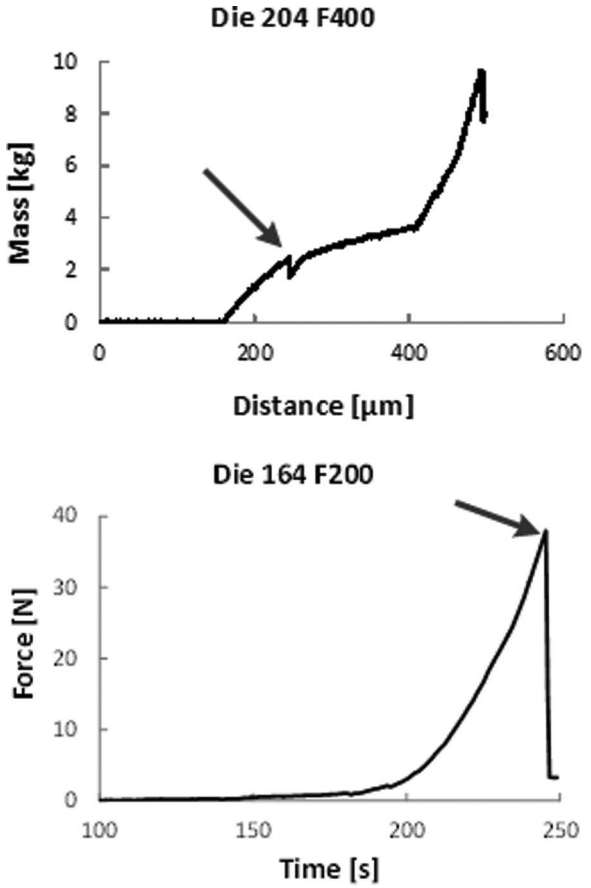

Figure 4. Typical curves recorded during shear testing (top) and tensile testing (bottom). The arrows indicate the values that were used in the strength calculations. For most shear tested samples, a first fracture that chipped a small part off the die, occurred. The remainder of the die could withstand a higher shear force before breaking completely, as seen in the top Figure. However, the mass at which the first fracture occurred was used in the strength calculations.

shear strengths along with the measured forces and masses. Tensile strength averages ranged from 7.3–12.3 MPa while average shear strengths were between 8.9 and 22.0 MPa. A typical fractured interface of a die of type F400 after tensile strength testing is shown in Figure 7. The 3D-fracture in more than 50% of the bond frame is clearly seen. The amount of 3D fracture increased with increasing frame width. All

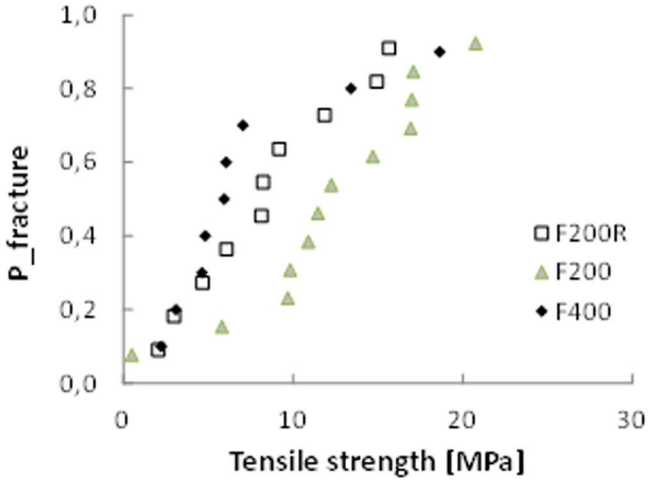

Figure 5. All measurement of tensile strength, plotted in a Weibull plot showing the fracture probability versus tensile strength [MPa].

Table III. Averages and standard error values for measured fracture force (tensile) and measured fracture mass (shear) and calculated pull strength and shear strength values.

Die design	Measured fracture fracture mass [kg]	Measured fracture force [N]	Calculated shear strength [MPa]	Calculated tensile strength [MPa]
F100	3.8 ± 0.2		8.9 ± 1.7	
F200R	4.2 ± 1.2	17.9 ± 3.2	19.4 ± 5.8	8.4 ± 1.5
F200	5.0 ± 1.3	27.5 ± 3.6	22.0 ± 5.7	12.3 ± 1.6
F400	1.4 ± 0.7	30.5 ± 7.4	12.2 ± 1.7	7.3 ± 1.8

dies of type F200R and all except two dies of type F200 had below 25% 3D-fracture. Three dies of type F400 had 50% or higher amount of 3D-fracture. However, there were also four dies of type F400 with less than 10% 3D-fracture.

Figure 8 shows the capacitance per area for all measured dies from laminate ElMech1. Excluding the outliers with capacitance above 4 pF/mm^2 and below 2 pF/mm^2, the average capacitance was 2.62 pF/mm^2–2.89 pF/mm^2 for the three frame types F200, F200R and F400. If this capacitance originated from a thermal oxide at the bonded interface, the thickness of the SiO_2 would be 12–13 nm. There was no difference in capacitance values obtained on the laminates that were annealed for 6 and 72 hours.

Figure 9 is a typical plot of the current between the two metal contacts as a function of the applied voltage. The current-voltage curves were linear without any sign of hysteresis for all the 16 measured dies. The voltage was swept to 2 V on one die of each design. Up to 2 V, the current-voltage plot was linear, without any sign of breakdown.

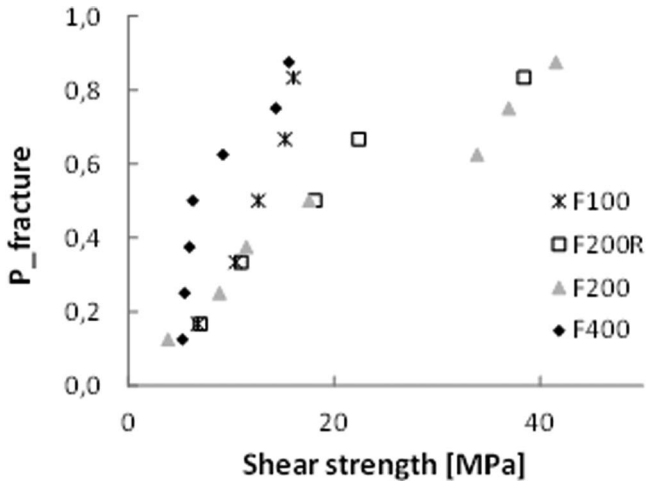

Figure 6. All measurement of shear strength, plotted in a Weibull plot showing the fracture probability versus shear strength [MPa].

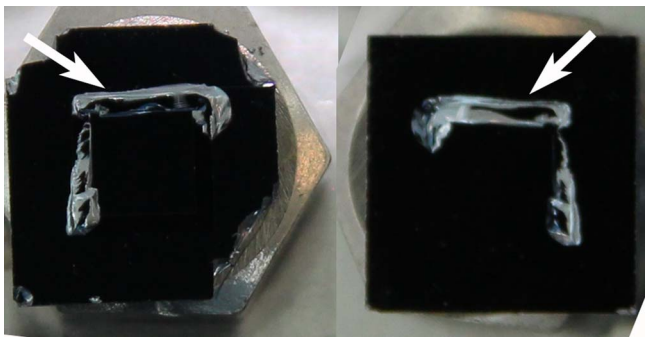

Figure 7. A typical fractured die of type F400 after tensile strength testing. The two fractured interfaces are seen. The two arrows point at the area with 3D-fracture. It is seen that 3D fracture occurred in more than 50% of the bond frame.

The resistance across the measured structure was calculated from the I-V plots obtained between minus 50 mV and 50mV. The resulting average resistances, calculated from measurements of four individual dies of each design, are listed in Table IV. The average current density of dies of design F200 at 50 mV bias was 1.1 × 10^4 A/m^2.

Figure 10 shows SAM and IR images of quarts Q1 from laminates Herm1 and Herm2. No bubbles were seen after annealing at 150°C for 6 or 72 hours (left images). After annealing at 600°C for 2 hours (right images), more than 50 bubbles were seen at the wafer perimeter. Less than 10 bubbles were seen in the device area, even after annealing at 600°C for 2 hours.

Figure 11 shows laminate Herm1 directly after bonding. All 481 membranes deflected inwards, indicating that the cavities were sealed, and that the pressure in the cavities was significantly lower than the ambient pressure. The average deflections measured at time t_1 and t_2 are listed in Table V. Using Equation 1, the pressure difference between the sealed cavity and the ambient at time t_1 was 1132 and 1158 mbar. The deflection differences measured between times t_1 and t_2 indicate that the pressure in the cavity had increased by 29 mbar during the 22 days between t_1 and t_2. This corresponds to a leakage rate of 2.4 × 10^{-11} mbar·l·s^{-1}.

Discussion

The electrical measurements in Figures 8 and 9 and Table IV show that the bonded dies had both capacitive and resistive properties. The I-V curves show that the dies had ohmic behavior without hysteresis for applied DC voltages. Table IV indicates a small increase of the order of 50 mΩ in the measured resistance value with increasing bond area. This is unexpected, as the total resistance would be expected to decrease with increasing contact area. The reason for the apparent increase is unknown. The calculated resistance of the bulk silicon in the dies was between 15 and 96 mΩ, which is significantly lower than the measured resistances of 2.2 Ω. The current density of 1.1 × 10^4 A/m^2 in F200 dies at 50 mV was significantly lower than the

Table IV. Average resistance between the two metal contacts, calculated from 4 individual measurements of dies from each design from laminate ElMech1.

Die design	Average resistance [Ω]
F100	2.16
F200	2.19
F200R	2.19
F400	2.21

Table V. Average deflection of seven dies measured at times t_1 and t_2, where $t_2 = t_1 + 22$ days. The maximum deflection change for an individual membrane is also listed, together with the number of flat membranes observed after environmental stressing.

Laminate	Average deflection t_1 [μm]	Average deflection t_2 [μm]	Max deflection difference t_1 - t_2 [μm]	No. of flat membranes
Herm1	5.57	5.45	0.13	0
Herm2	5.70	5.58	0.14	0

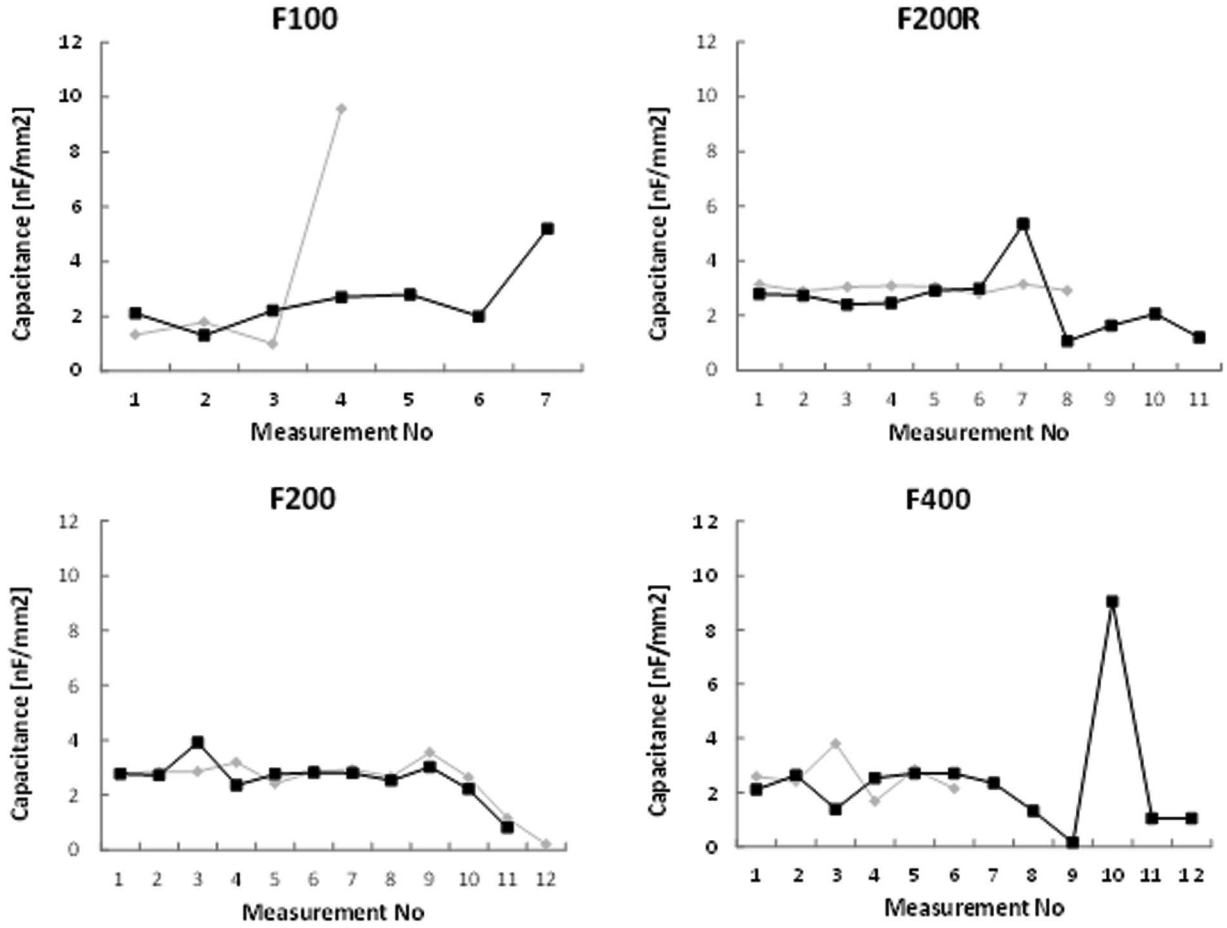

Figure 8. The capacitance/area for the different designs and annealing times of laminate ElMech1. Black lines show 72 h annealing time and gray lines show 6 h annealing time, both at 150°C.

current densities of 4.0–6.2 × 10^4 A/m^2 obtained on high-temperature annealed Si directly bonded dies.[15] This difference does indicate that the current is restricted across the bonded interface produced by the plasma activated direct bonding method presented in this paper.

The linear, ohmic behavior observed on the dies in the current study is in contrast to the non-linear I-V curve reported by Amirfeiz et al.[4]

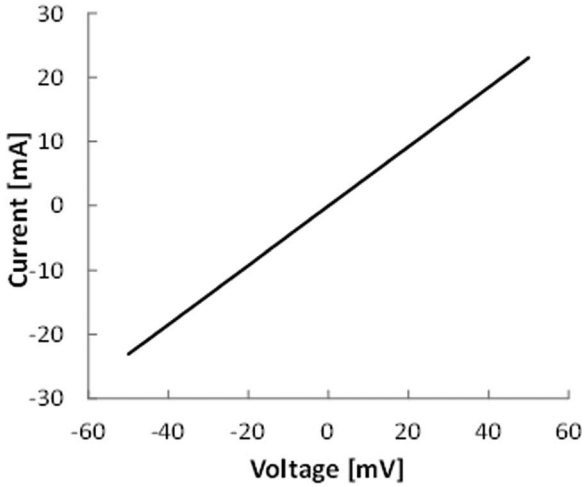

Figure 9. Typical plot of current vs voltage. This measurement was obtained on die 321 of design F100, which had received a 72 h anneal at 150°C.

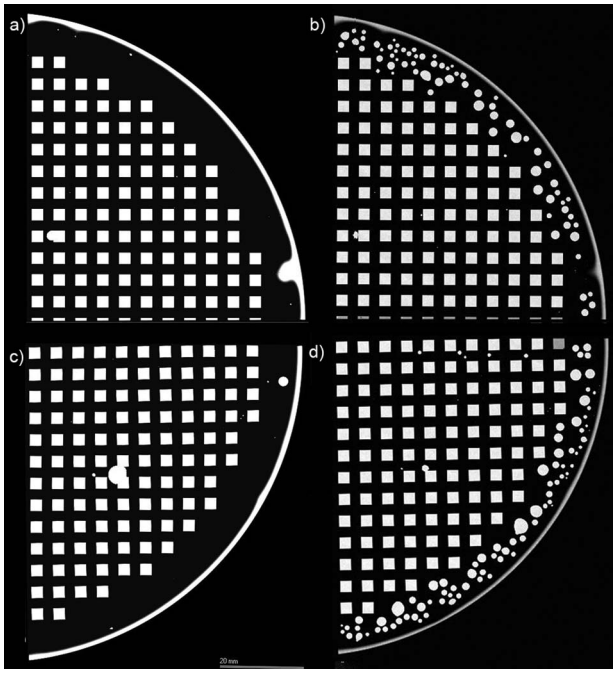

Figure 10. SAM and IR images of quarts Q1 from laminates Herm1 and Herm2. Left images no bubbles were seen after annealing at 150°C for 6 (a) or 72 hours (c). Images (b) and (d) show that bubbles were seen at the wafer perimeter after further annealing at 600°C for 2 hours.

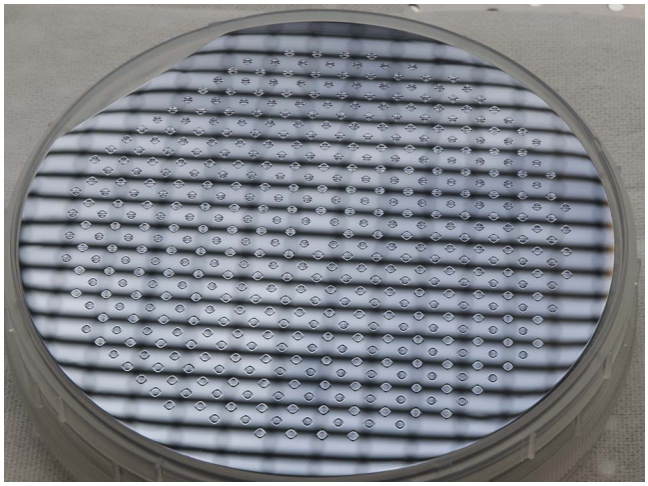

Figure 11. Laminate Herm1 directly after bonding. The hazy spots are membranes that deflect inwards. All 481 membranes deflected inwards.

and by Raeissi et al.[11,12] The reason for the discrepancy is unknown, but it could be related to differences in silicon surface activation process, or to differences in sample preparation. To our knowledge, the current paper is the first presentation of a large sample of I-V measurements on dies with varying bonded area and with a die edge termination controlled by etching, not by dicing. Our present results show that a linear, ohmic DC resistance can be obtained at interfaces realized by low-temperature direct silicon bonding.

The measured capacitances in Figure 8 were correlated with the bonding area, and indicate that the bonded interface induced a capacitive response. The capacitance at 1kHz was equivalent to the capacitance of a thermal SiO_2 of thickness 12–13 nm. However, the fact that no electric breakdown was observed as the voltage was ramped from 0 to 2 V, and the fact that the dies exposed ohmic DC behavior, shows that the capacitive response was not caused by a SiO_2 layer at the bonded interface.

The uncertainty regarding the presence and thickness of an SiO_2 layer at the interface that we found in our current study, is supported by other studies. Amirfeiz et al.[4] found an oxide of thickness 8–10 nm to be produced by plasma activation on a silicon surface, applying capacitance measurements. Ellipsometry measurement on a similarly treated surface showed an oxide of 5 nm thickness, i.e. a reduction of 40–50%.[4] Moriceau et al. had to model a superficial, porous silicon layer on top of the silicon surface in order to obtain a good fit in ellipsometry measurements of the oxide thickness of oxygen RIE plasma treated silicon wafers. In contrast, no noticeable changes in SiO_2 thickness were seen on wafers that were initially covered with 51 nm thermal SiO_2.[10] Michel et al. measured the SiO_2 created during dielectric barrier discharge and found that in one minute, a porous SiO_2 of thickness 2.5 nm and with a pore fraction of approximately 10% was formed.[16]

Our current results and results obtained by other groups indicate that the capacitive response of the plasma bonded interface could be caused by properties of the silicon material.[4,10] The physical thickness of the interface layer between two silicon wafers joined by plasma bonding was measured to be 6.3 nm by transmission electron microscopy.[12] X-ray reflectivity measurements identified a layer of thickness 5–10 nm of low electron density adjacent to the bonded interface.[9,10] Another study found the presence of a space-charge region on both sides of the bonded interface by capacitance measurements.[4] Moriceau et al. proposed that the layers of low electron density provide diffusion paths that are important for bond strengthening.[9,10] Amirfeiz suggested that the plasma activation and subsequent exposure to water result in a strong, porous silica network containing cavities lined with hydroxyl and hydride groups, and which also contain water.[7]

The capacitance values obtained in the current study are highly different from capacitance values obtained in similarly shaped test dies, bonded by high-temperature annealed direct silicon (fusion) bonding.[15] Fusion bonded samples made from bonding Si wafers without thermal SiO_2 had ohmic behavior and no measureable capacitance when measured after bond anneal.[15] In contrast, samples fabricated by bonding a Si wafer with a 60 nm thick thermal SiO_2 to a wafer with no thermal SiO_2 exposed the expected 574 pF/mm^2. This result suggests that the electrical properties of the bonded interface is different for interfaces formed by Si-Si fusion bonding and plasma bonding.

We propose that the capacitances measured on plasma bonded samples in the current study can be related to layers of low electron density, a hydrated porous silica network, oxide charges induced by the plasma treatment process, or a combination of the three. It is likely that the formation of the low electron density layer[9,10] also results in the formation of electron and hole traps in the silicon material. It has been shown that plasma activation processes intended for wafer bonding increased the oxide fixed charge and the interface trap density,[17,18] and that transistors manufactured on SOI wafers realized by plasma bonding had poorer performance compared to transistors manufactured on conventional SOI wafers.[18] Moreover, it is likely that the formation of a porous silica network during plasma treatment, and the subsequent hydration of this network results in a change in the capacitive property of the network. We propose that the capacitance that we measure at 1 kHz is caused by the presence of traps and/or water, and their response to the applied AC voltage. It is possible that the DC conductivity is not affected, and that point contacts across the bonded interface cause the ohmic DC conductance. Further studies of the capacitance and resistance across the bonded interface at different AC frequencies are required to obtain a better model.

The dicing yield for the ElMech laminates, plotted in Figure 3, was below 58% for all laminates and die types. This relatively low value is thought to be caused by the presence of individual frame structures on the wafer. The frame structures are believed to reduce the bond yield since they prevent the propagation of a continuous contact wave at the interface to be bonded, as described by Plössl and Kräuter.[1] The Herm laminates were structured by cavities, but did allow the propagation of a continuous contact wave, since there was a connected silicon surface that was to be bonded. All the cavities of the Herm laminates were sealed, applying the same bonding process as for the ElMech laminates. This result shows that the low dicing yield in Figure 3 was caused by the wafer design, and not by the bonding process. There is currently no generally accepted design rule describing the minimum width of a line that is to be bonded, as this width will also depend on the bow, roughness, and previous processing of the wafer prior to bonding.

The mechanical strength of low-temperature direct silicon bonds is commonly assessed by its surface energy.[5,6,10] Energies above 1 J/m^2 are considered to indicate strong bonds. However, application in device packaging commonly requires that the tensile and shear strengths are known. Our group has found a weak correlation between surface energy and tensile strengths.[13] Therefore, tensile and shear strength measurements were performed in the current work. The average tensile strengths obtained on the presented structures are similar to the 9.0 MPa found by Visser et al.,[8] and higher than the 4.6 MPa found earlier by our group.[13] The student t test using a 95% confidence interval showed that the there was no statistically significant difference between the tensile or shear strengths for the different frame widths. Wafer bonding technologies currently used in device packaging include anodic[19] bonding, glass frit bonding,[20] and high-temperature silicon direct bonding.[21] The tensile strengths of these technologies are reposted to be between 10 MPa[15] and 20 MPa.[20,21] The average tensile strengths measured in the current study ranged from 7.3–12.3 MPa, and are somewhat lower than the reported strengths of currently used methods. Depending on the device, the strength found in the current study may still be sufficient for its packaging.

All the 2 × 481 membranes on laminates Herm1 and Herm2 deflected inwards after bonding. The deflection corresponded to a

differential pressure of 1132 and 1158 mbar, which are higher than the commonly accepted atmospheric pressure of 1013 mbar. It is assumed that uncertainties in the actual membrane dimensions caused the large values of calculated differential pressures. However, the calculated differential pressures indicate that the actual pressure in the sealed cavity was below a few mbar. None of the 2 × 50 membranes had turned flat after the environmental stressing. These results show that the investigated bonding process has potential for hermetic sealing of devices. By measuring differences in membrane deflection at a time interval of 22 days, a maximum leak rate of 2.4×10^{-11} mbar·l·s^{-1} was estimated. Our group found an improved leak rate maximum estimate of 1.5×10^{-14} mbar·l·s^{-1} on dies from Herm1 laminate, using residual gas analysis.[22] Visser et al. found a maximum leak rate of 8×10^{-13} mbar·l·s^{-1} for low-temperature direct Si-Si bonded seals of width 20–70 μm.[8] There is no disagreement between these three estimates, as they all represent maxima, limited by their respective measurement technique. In all three cases, the actual leak rate could be significantly lower.

Increasing the annealing time at 150°C from 6 to 72 hours did not improve the dicing yield (Figure 3), nor did it change the capacitive response (Figure 8). Annealing at 150°C did not result in bubble formation (Figure 10). Hermetic sealing with a leakage rate below the range of 10^{-11} mbar·l·s^{-1} was obtained without any annealing after bonding. Together, these four observations could indicate that annealing at 150°C did not affect the macroscopic properties of the bonds produced in our study significantly. However, Eichler et al. found that the surface energy of plasma activated, directly bonded Si-Si wafer laminates increased with annealing at temperatures above 100°C.[23] Similarly, in wet activated bonded Si-Si wafers, Tong et al. found a significant increase in surface energy following annealing in air at 150°C.[3] Ventosa et al. deduced that water at the bonded interface reacted with silicon to form SiO_2 at temperatures as low as 150°C.[24] Hence, the literature shows that siloxane bonds can be formed during annealing at 150°C. It is likely that the surface energy of the dies in the current study did increase due to the anneal at 150°C, but that no effect of increasing the time from 6 to 72 hours was discernible in the dicing yield or the capacitive response.

Bubbles occurred only at the wafer perimeter even after 2h anneal at 600°C. This suggests that the cavity distribution efficiently prevented the formation of gas bubbles in the device area. The hydrogen produced by the oxidation of the silicon by the interfacial trapped water migrated into the cavities, avoiding bubble formation. At the wafer perimeter, no cavities were present to incorporate the hydrogen, and a lot of bubbles were generated. This is consistent with the results of a previous study.[5]

Conclusions

The electrical, mechanical, and hermetic properties of low-temperature, plasma activated direct silicon bonds were investigated. On dies with a bonded area of 1–4 mm^2, the bonded interface was found to have a capacitance ranging from 2.62–2.89 pF/mm^2 at 1 kHz. Linear I-V curves showing ohmic behavior, no hysteresis and a resistance of 2.2 Ω were measured at DC. Individual frame structures had a yield below 58% while 100% yield was obtained on wafers that allowed the propagation of a continuous contact wave during bonding. The applied bonding process resulted in sealed cavities with a pressure below a few mbar. The maximum leak rate of the seals was 2.4×10^{-11} mbar·l·s^{-1}, but could be significantly lower. No gross leaks were observed following a steady-state life test, a thermal shock test, and a moisture resistance test applied on 100 dies.

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