Ultra-low power electronics for energy harvesting node

by

Aleksandar Žujović

BSc. University of Belgrade - School of Electrical Engineering (2014)

Submitted to the Department of Micro- and Nanosystem Technology
in partial fulfillment of the requirements for the degree of

Master of Science in Smart Systems Integration

at the

UNIVERSITY OF SOUTH-EAST NORWAY

July 2016

Author .....
Department of Micro- and Nanosystem Technology
July 01, 2016

Certified by .....
Mehdi Azadmehr
Associate Professor
Thesis Supervisor

Ultra-low power electronics for energy harvesting node

by

Aleksandar Žujović

Submitted to the Department of Micro- and Nanosystem Technology
on July 01, 2016, in partial fulfillment of the
requirements for the degree of
Master of Science in Smart Systems Integration

Abstract

Apart from providing detailed insight about the energy harvesting system as a whole, this work tackles the challenges of efficient control of the interface circuit of an electrostatic vibration energy harvester, with severely limited power consumption allowance for the controlling electronics. Used interface circuit consists of double charge-pump topology, comprising a storage element (pre-charged reservoir capacitance), dual antiphase variable capacitance and an intermediate storage element, with an inductive flyback return path. Since high voltages are expected in the long term operation, switch component of the interface circuit is realized as a high-voltage PMOS device from *AMSH35* process by AMS.

Concerning the interface circuit, theoretical analysis was introduced, to demonstrate the requirement for precise synchronization of the switch with the circuit voltage levels, with the purpose of optimizing the harvested energy. Previous work was addressed, and this work was built upon it. For decreasing the power consumption of the critical component, a low power clock-signal generator was designed, with power consumption of approximately $0.35nW$, and accompanying stable current reference with constant power consumption of $0.57nW$, and $4.7\%/V$ current deviation caused by variations in the supply voltage.

Additionally, issues accompanying the long term operation, and thus increase in the pre-charge voltage, were discussed in details, and subject of interest for further research and promising possible improvements were suggested.

Thesis Supervisor: Mehdi Azadmehr
Title: Associate Professor

Acknowledgments

I would like to express my most sincere gratefulness to Assoc. Prof. Mehdi Azadmehr for his relentless guidance and support during the work on this project, and constructive criticism during the thesis writing.

Additionally, I would like to acknowledge and express my thankfulness to the *SSI Consortium*, for creating this course programme and providing me with the opportunity to take part in it. It has been my honor and pleasure to participate in this programme for two years.

Finally I would like to express my deepest and eternal gratitude to my parents, who have effortlessly provided me with their never-ending love and enthusiastic support, and without whom I would not be the person that I am today.

Contents

Acknowledgments . . . . . **v**

1 Introduction **1**
1.1 Motivation 1
1.2 Concept of energy harvesting 2
1.3 Ambient energy sources and applications 2
1.4 Wireless Sensor Nodes 4
1.5 Vibration energy harvesting 5
1.5.1 Generalized system 5
1.5.2 Mechanical structure working principle 6
1.5.3 Electro-mechanical energy conversion 8
1.6 Circuit for power management 12
1.7 Thesis scope and limitations 14
1.8 Thesis Outline 14

2 Study of the Electrostatic Vibration Energy Harvesting System . **15**
2.1 Electrostatic Transducer 15
2.1.1 Out of plane capacitor with gap closing 17
2.1.2 In-plane capacitor with variable overlap surface 17
2.1.3 In-plane comb capacitor with variable overlap 18
2.1.4 In-plane comb capacitor with gap closing 19
2.1.5 In plane capacitor with variable patterned surface 20
2.1.6 Summary 21
2.1.7 Discussion 21
2.2 Power management circuit topologies 22
2.2.1 Primitive (continuous) topologies 22
2.2.2 Charge Constrained Topology 23
2.2.3 Voltage Constrained Topology 26
2.2.4 Charge pump topologies 27

2.3 Summary and Discussion 32

3 Interface circuit and flyback switch control circuit design 33
3.1 Software tools 33
3.2 Process technology 33
3.3 Transducer model 34
3.4 Interface circuit topology 37
3.5 Previous Work 39
3.5.1 Return path circuit 39
3.5.2 Voltage level shifter 40
3.5.3 Synchronous switch control circuit 41
3.6 Self-sustaining topology considerations 48
3.6.1 Bump-circuit clocking 48
3.6.2 Low-power clock signal generator - literature review 50
3.7 CMOS Relaxation oscillator 51
3.8 Current Reference 53
3.8.1 Design methodology 55
3.9 Considerations for mid-term operation 61
3.10 Discussion 62
3.10.1 Voltage regulator 65
3.10.2 Power consumption considerations 67

4 Conclusions, improvements and future work 69
4.1 Chapter summaries 69
4.2 Improvements and future work 71

References 78

Chapter 1

Introduction

1.1 Motivation

Ambient energy is present in many forms in our surroundings, including solar (light) energy, thermal energy, wind energy, mechanical energy, electromagnetic or radiation energy, energy from chemical reactions and many others. Mankind has utilized this ambient, or environmental energy, throughout history to facilitate and improve their daily lives, which can be seen in the appearance of waterwheels and windmills that date back hundreds of years, or hydroelectric power plants, solar panels in the last century. Considering this, it is obvious that the concept of energy harvesting is anything but new.

In the more recent years, energy harvesting is placed in another context, meaning the utilization of harvested energy as a power supply for miniaturized electronic devices, such as wireless sensor nodes, wearable electronics or RFID tags and such. These devices are designed to be very power efficient, with maximum power consumption up to miliwatts, depending on the energy harvesting capability). However, they impose strong requirements for reliability w.r.t. power supply variation and size, depending on application. For microscale electronic devices which rely on energy harvesting for power supply, energy sources of practical interest are electromagnetic (such as those in RFID), mechanical vibrations and thermal gradients. Although these sources have certain efficiency limitations, they are practically unlimited if they are present at the device working location [1].

This chapter will briefly introduce the reader to the main idea, problems and challenges of microscale energy harvesting, outline different sources, applications of use and various conversion principles, i.e. types of transducers that are used in state-of-the-art energy harvesting systems.

1.2 Concept of energy harvesting

Energy harvesting (also known as energy scavenging or power harvesting) is essentially the process of collecting and converting the energy from an external environmental source, or sources, and utilizing that energy to supply power to a device or accumulating and storing them for later use [2]. An efficient energy harvesting system must properly convert, condition and manage harvested energy and make it available in appropriate form to its electrical load, i.e. the device itself, whether it is a sensor, a passive RFID tag or a battery that is being charged.

1.3 Ambient energy sources and applications

As mentioned before, there are many external energy sources available in the environment, which gives one method for classification of energy harvesting systems. A compact way of classifying the energy sources is with respect to their nature:

- **Mechanical sources:** such as mechanical vibrations and mechanical stress-strain,
- **Thermal sources:** waste energy from furnaces or machines, or friction sources,
- **Radiation sources:** includes sunlight or light-sources, ambient RF waves or infrared waves,
- **Natural energy:** from water flow, wind etc.,
- **Biochemical sources:** includes sources based on chemical reactions.

Energy from these sources is utilized for various applications ranging from mega-watt to nano-watt scale, which can be summarized as:

- **Mega-watt range:** Power supply for domestic (household) and industrial use. Commonly used sources are hydraulic flow and potential energy [3], wind energy [4] and solar energy [5].
- **Mili/micro-watt range:** low power applications such as vibration powered wrist watches [6], solar powered calculators [7], micromachined thermopiles for harvesting on human bodies [8], shoe-mounted piezoelectric generator [9], electrostatic and electromagnetic generators [10] etc.
- **Nano-watt range:** electrostatic harvesters with limited variation range, piezoelectric nanowires, nanosensor noise harvesters [11], carbon nanotubes [12] etc.

For electronic devices and wireless sensor nodes mili-nano watt range is of a particular interest. For this purpose we consider some sources to be more appropriate and pay more attention to them. Figure 1-1 illustrates power densities for different ambient energy sources.

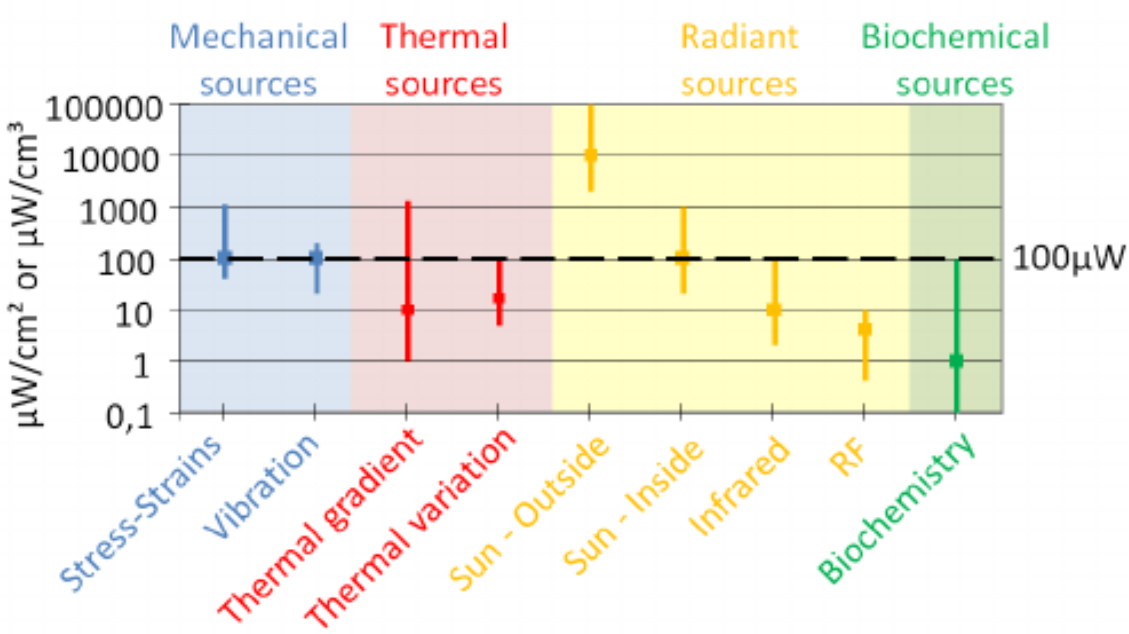


Figure 1-1: *Power densities available from different ambient energy sources* [13]

As seen Figure 1-1, highest available power density is available from direct sunlight. Although solar energy harvesters are frequently used in a wide range of power levels and scale sizes, two major limitations prevent solar energy from being the most popular and attractive source of ambient energy. Namely, the cost of manufacturing for high power and large scale generators reduce its availability for commercial use, and on the other side low light availability for small scale devices reduces the efficiency of such harvesting systems [14, 15]. Some devices harvest thermal energy in form of thermal gradients [16], but normally a high temperature gradient, or temperature variation is required to achieve effective harvesting which limits the scope of application, especially in micro-scale devices, where it is hard to find temperature differences greater than approx. 10°C. Mechanical vibrations are present in various environments that require monitoring, i.e. sensors and sensor networks, such as factories, bridges, cars etc. This makes vibration energy harvesting more and more attractive for wireless sensors applications, such as ones presented in [17, 18].

1.4 Wireless Sensor Nodes

There is an increasing number of applications for which servicing and maintenance of devices, such as battery replacement or data collection, is difficult or inconvenient due to inaccessibility. Such applications include, but are not limited to, various sensors for monitoring temperature, humidity and/or pressure in rain forests, monitoring state of industrial machines such as motors, pumps and turbines, or perhaps implantable devices for vital functions monitoring and many others. Ideal devices would be accessible remotely, and self-sustaining, meaning that they would function properly only from harvested energy over a long period of time. Data collection can be done wireless, to eliminate the need for data wires or necessity of physical access for collection of data. Other challenge is for the system to be self-powered from the environment energy, which poses a big challenge, since environmental energy is unpredictable and might not be available at all times. This imposes the necessity of a power storage element, so the harvested energy can be stored for further use. Recent technology advancement, especially in microelectronic technology allows design and production of very low-power devices that would efficiently consume the limited harvested energy.

Typical topology of a WSN (*Wireless Sensor Node*) is shown in Figure 1-2 [19] in the form of a block diagram.

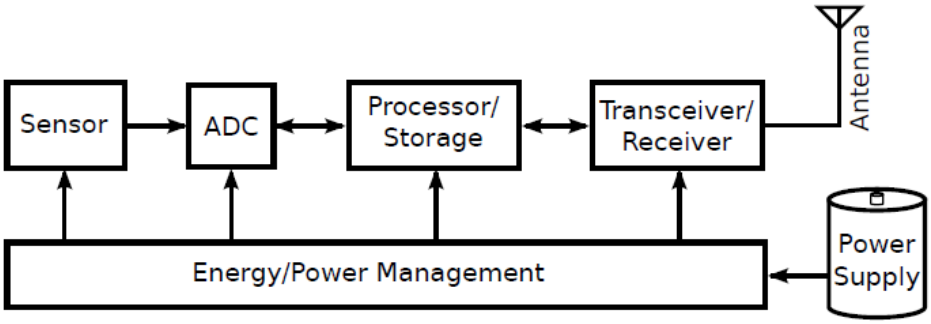


Figure 1-2: *Typical WSN architecture* [20]

Power consumption of such a system is typically dominated by communication and sensing operations, but these occur very infrequently due to the slow changing nature of environmental variables such as air pressure or temperature. Consequently, processing, sensing and communication units can be idle, and consume no to very little power, while the harvesting cycle replenishes the power supply.

1.5 Vibration energy harvesting

Energy harvesting from mechanical vibrations is a relatively new concept, compared to for instance harvesting of solar energy through photovoltaic cells, or electromagnetic energy for RFID circuits. It began to take off more rapidly in 2000's with the increased research of MEMS devices.

1.5.1 Generalized system

Generalized form of the vibration harvesting system is illustrated in Figure 1-3. The model for vibration micro-generator was first introduced in [21] by Yates and Williams.

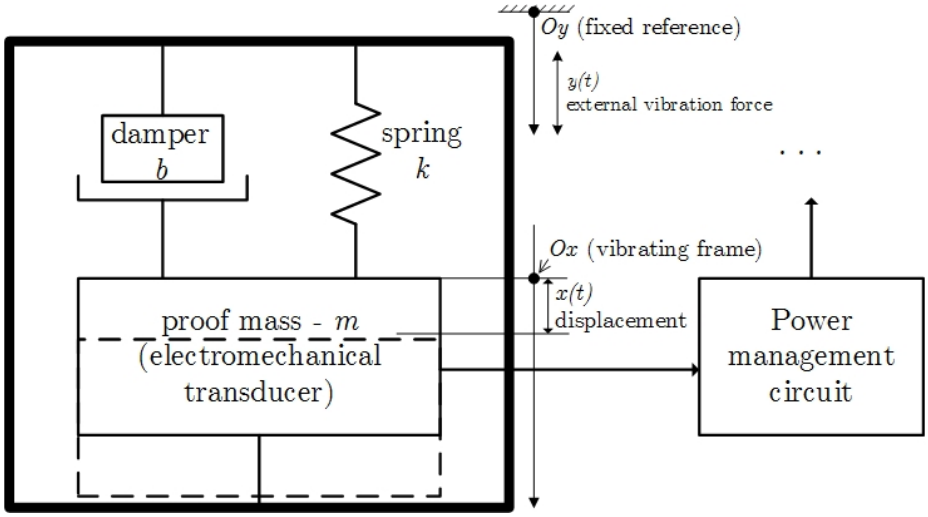


Figure 1-3: *General model of a VEH*

As described in various studies, vibration energy harvesting can be accomplished in two steps:

1. Mechanical energy is "captured" by a mechanical part of the system, modeled with the spring-coupled proof-mass

2. Accumulated kinetic energy is converted into electrical form, modeled with the damping element

The transducer is usually a mechanical resonator, consisting of a proof-mass which is suspended from the frame via an elastic structure, i.e. a spring. In this domain, there are two references, the global reference frame Oy, in which vibrations take place ($y(t)$), and the reference Ox related to the oscillating system in which the proof-mass

is located, and with respect to which the displacement of the proof mass is measured ($x(t)$). According to Landau [22], if the external vibrations are represented as $y(t)$, then the overall acceleration of the inertial system is $a_{ext}(t) = \ddot{y}(t)$, and the relative motion of the referent system Ox can be modeled by applying force to the proof-mass totaling to $f(t) = -m \times a_{ext}(t) = -m \times \ddot{y}(t)$, where m is the mass of the proof-mass. Additionally, the proof-mass is elastically coupled with the frame Ox via spring, and the mass accumulates kinetic energy due to movement in the referent system.

The conversion of the collected kinetic energy to electrical energy is modeled with the damping element, which means that ideally, the dominant damping force acting on the suspended proof-mass should be of electrical origin. In other words, it should perform negative work w.r.t. mechanical vibration, intentionally decreasing the kinetic energy of the system. This damping force can be induced by a electric field, magnetic field or a mechanical strain in piezo-electric material, depending on the type of the electro-mechanical transducer that is used. Each of the transducer types has its own characteristics, i.e. benefits and drawbacks, and consequently is used in the most suitable application scenario. Additionally, the type of transducer specifies the characteristics of the power management circuit in order to achieve a functioning energy harvester, in terms of energy accumulation and power supply to the load, e.g. sensor or transceiver.

To summarize, design procedure for a vibration energy harvester include design and optimization of : *a*) mechanical structure, in order to maximize the amount of "captured" kinetic energy; *b*) transducer, in order to maximize the conversion efficiency; and *c*) power management electronic circuit, to accumulate, store and distribute harvested energy as efficiently as possible while consuming very low amount of power itself [19].

1.5.2 Mechanical structure working principle

Mechanical structure, modeled as a suspended mass-spring-dashpot system, can be one of two types: 1) non-resonant, which is typically used in applications where the amplitude of vibrations is large enough w.r.t. maximum allowed mass displacement and the vibration power is spread over a wider spectrum of low frequencies; 2) resonant, typically used in applications where the amplitude is relatively small compared to feasible mass displacement and designed to target a specific narrow band of frequencies.

Considering a given resonant mechanical structure, the maximum mass displace-

ment is given when the external vibration frequency equals the structure's resonant frequency, and the displacement drastically lowers with even the slightest deviation from the structure's resonant frequency. This is a major challenge for the designers, since the ambient vibrations can be, and usually are inconsistent or variable, and with the linear resonators having very narrow and selective frequency bands, there is a possibility that it will not perform in real conditions, which renders it unusable for any real-life application.

The efforts to overcome these challenges take form of widening the response bandwidth of the mechanical resonator structures, involving the utilization of non-linear mechanical properties to create more complex coupling between the mass and the referent frame. Such works exist in different forms, including resonators with non-linear springs [23, 24], bi-stable springs [25] or non-linear springs with two mass elements [26]. These approaches contribute to the increase in efficiency by allowing a "conversion" of frequency, i.e. a resonator made for low frequency, with a low quality factor is used as excitation of a resonator designed for high frequency and has a high quality factor, which is used as the transducer.

According to [27], maximum obtainable power by a mechanical resonator structure can be described with simple equation:

$$P_{max} = \frac{1}{2} X_{max} m \omega A_{ext} \tag{1.1}$$

where X_{max} is the maximum proof-mass displacement, m is the mass, ω is the angular frequency and A_{ext} is the amplitude of the external vibrations. This expression relates solely to the mechanical structure and is not related to the transducer or its electro-mechanical efficiency, but simply represents the maximum power that the the resonating structure can collect from the vibrations. Based on the literature review of some existing harvester designs, Table 1.1 presents a brief comparison, and the evolution of micro-mechanical resonating structures, and their absolute power limit according to (1.1).

Table 1.1: Overview of several micro-scale resonator designs concerning their maximum achievable power

Design	Year	X_{max} [μm]	m [g]	f [Hz]	A_{ext} [m/s^2]	P_{max} [μW]
Roundy et. al. [28]	2003	250	0.1	50	1	3.93
Despesse et. al. [29]	2005	95	2	50	1	2.98
Paracha et. al. [30]	2009	50	0.066	250	1	2.59
Guillemet et. al. [31]	2013	46	0.046	163	1	1.08

Maximum achievable power in the mechanical resonator reflects the amount of kinetic energy the structure can collect from the external vibrations, which is supported by the results presented in Table 1.1, seeing as the structures fabricated with older technologies are larger and are allowed higher maximum displacement, they have the potential of achieving more power for the same amplitude of external vibrations. However the efficiency of electro-mechanical conversion and power management circuits are much higher, and so is the overall harvesting efficiency, which will be illustrated in following sections.

The design of the mechanical structure is out of the scope of this thesis. However, the author recognizes the importance of understanding the working principle and the connection it bears to the rest of the harvester system, and therefore considers that a brief, but not in-depth, explanation is appropriate.

1.5.3 Electro-mechanical energy conversion

As explained earlier, electro-mechanical transducer is the element which converts harvested mechanical energy into electrical energy, and as such it is the second major design point in the process of vibration energy harvester design, which contributes greatly to the overall harvester efficiency, and also determines the architecture of the power management electronic circuit. On a macro scale, electrical power generation is dominantly based on electromagnetic transducers, e.g. windmills, hydroelectric power plants etc. Electrostatic and piezoelectric transduction is highly impractical and inefficient on a macro scale, but well suited and effective when it comes to micro-scale devices. Thus, for the purpose of micro-scale harvesting systems, three basic methods are recognized and used for energy conversion: 1) electromagnetic; 2) piezoelectric; and 3) electrostatic energy conversion. Consequently, we recognize three types of transducers for each of the methods.

Electromagnetic transducers

The main principle of electromagnetic energy conversion is based the Faraday's law of induction, which is illustrated in Figure 1-4). The change of magnetic flux Φ, through a coil with N windings, induces a voltage:

$$v(t) = -N d\Phi/dt, \tag{1.2}$$

forcing a current $i(t)$ through a closed circuit. Φ is given by:

$$\Phi = \iint_{\Sigma(t)} \mathbf{B}(t) d\mathbf{A},$$

where $d\mathbf{A}$ is an infinitesimally small element of surface area of the moving surface $\Sigma(t)$ and $\mathbf{B}$ is the magnetic field. The total force $f(t)$ on the charges moving through the magnetic field is opposing the relative motion (Lenz's law), i.e. it acts as a damper in the mass-spring-dashpot micro-generator system illustrated in Figure 1-3. Energy converted to heat, due to resistance, and stored in the coil, due to inductance, comes from the mechanical work done against the opposing force. There are a lot of issues

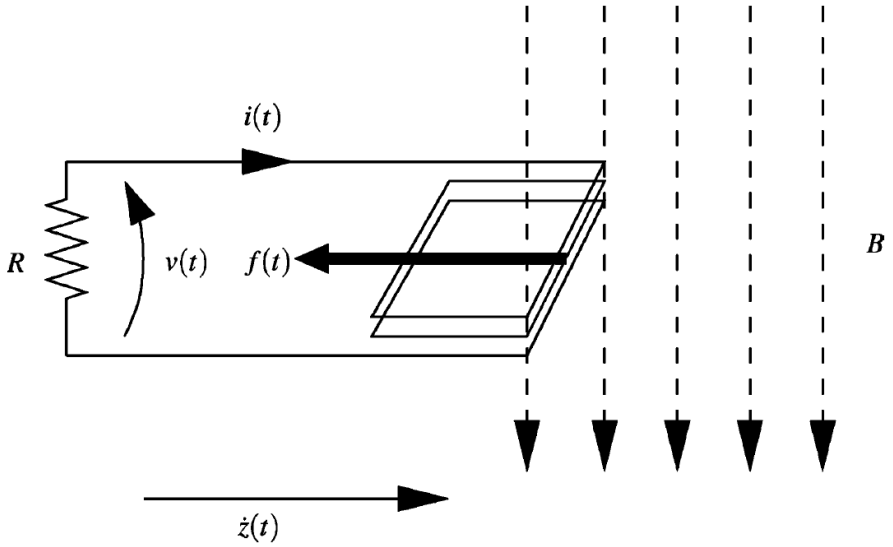


Figure 1-4: *Electromagnetic transduction principle* [27]

of utilizing electromagnetic transduction on a micro-scale, including the difficulty to integrate or fabricate a large number of windings on a MEMS device resulting in low output voltages, which imposes a requirement for the integration of ferromagnetic materials or permanent magnets for the flux path. Another inconvenience is that the strong damping forces require rapid flux variations, according to equation (1.2), whereas ambient vibrations are in a low frequency range.

Piezorelectric transducers

These transducers are based on a phenomenon called piezoelectric effect, whereby a material experiencing mechanical strain from applied stress exhibits induction of an electric field in that material, and vice versa, an applied electric field causes the material to experience strain [32]. Piezoelectric transducers utilize the former to act

as micro-generators, in terms that some of the mechanical work done by an external force to produce strain is stored as elastic strain energy, and the rest is stored in the electric field associated with the polarization of the material [27]. Principle of operation of piezoelectric transducers is illustrated in Figure 1-5. When an external conduction path is provided the result is a current that neutralizes the net charge. Materials that exhibit piezoelectric properties with high electromechanical coupling

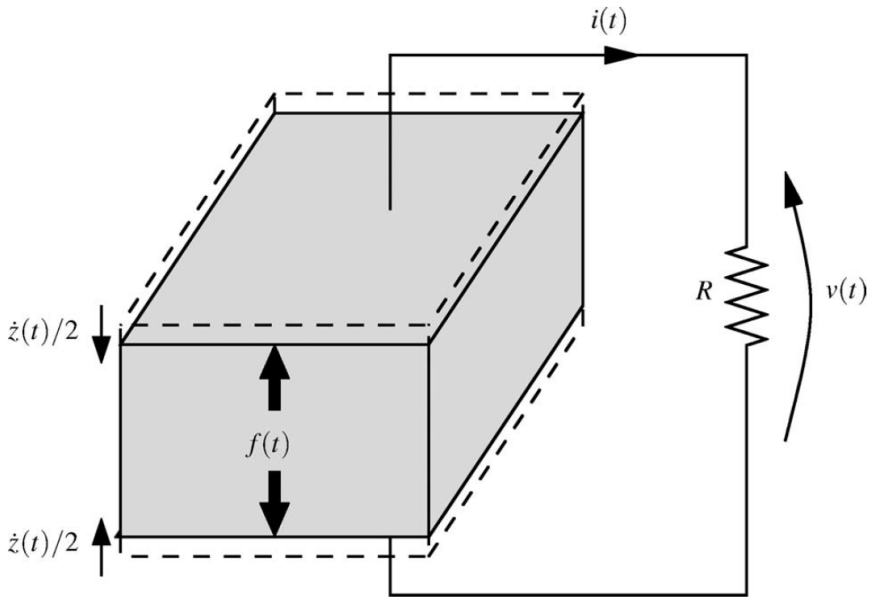


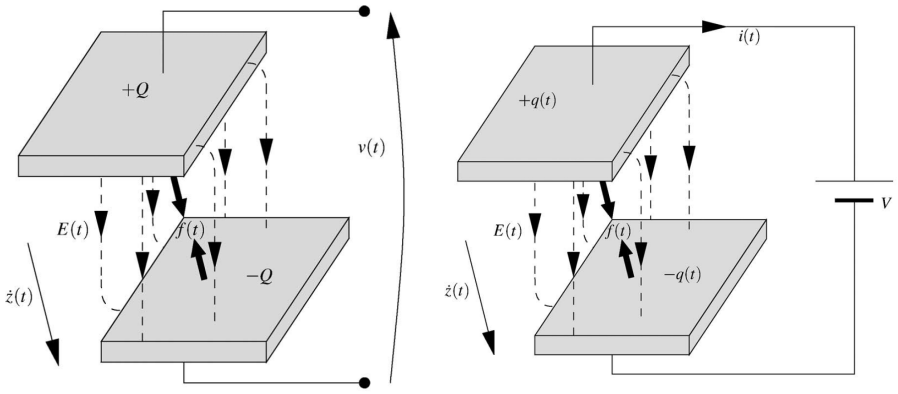
Figure 1-5: *Piezoelectric transduction principle* [27]

factors are in general ceramics (e.g. lead zirconate titanate - PZT, or aluminum nitride - AlN), and as such they do not tolerate high values of strain. They are normally used in form of thin films, spread across another material that exhibits large values of displacement, and consequently strain. Most common structure of this type of transducer is a proof-mass suspended on a cantilever with a thin film of a piezoelectric material.

Electrostatic transducers

When it comes to electrostatic transducers, work done by external forces is performed against the attractive force between oppositely charged parts. Practically, this represents a variable capacitor, whose gap between the plates vary as a consequence to external vibrations [33]. Two main modes of operation are distinguished: continuous and switched. Switched mode implies reconfiguration in the transducer's surrounding circuitry at certain moments of the operation cycle, through the operation of switches [27]. They can be configured to operate in two different modes: *a*)

charge constrained operation Figure 1-6a; and *b*) voltage constrained operation 1-6b.



(a) *Charge constrained configuration*

(b) *Voltage constrained configuration*

Figure 1-6: *Electrostatic transducer* [27]

Charge constrained mode (Figure 1-6a) with a fixed overlap length and a variable gap between the plates (i.e. horizontal component of $\dot{z}(t)$ is zero) operates as follows: electric field is proportional to the charge, which is constant, and energy density is independent of the gap. As the external force exerts work against attractive electrostatic force, and the gap increases, the increased volume of the electric field will store added potential energy. If, on the contrary, the plates are moved laterally, i.e. the vertical component of $\dot{z}(t)$ is zero, mechanical work, done by external forces, is exerted against the fringing field. This causes an increase in stored energy, since the reduction in plate overlap increases electric field strength.

Voltage constrained mode is illustrated in Figure 1-6b. If the plates move vertically, with a fixed overlap, electric field strength reduces, causing the charges to move in the external conduction path, forming a current $i(t)$. If the plates move laterally, electric field strength stays remains unchanged, but the reduction in the volume of electric field forces the current to flow through the external conduction path. In either case, exerted mechanical work is converted into added electrical potential energy in the source [27].

In both of these modes, the basic equations for the capacitor apply: charge $Q = CV$, and energy that is stored in the capacitor $W_s = \frac{1}{2}CV^2$. Electrostatic force is found to be proportional to the rate of change of the capacitance in the direction orthogonal to the plates surface:

$$F = \frac{1}{2}V^2 dC/dz \tag{1.3}$$

Having explained these two modes from physics point of view, some additional explanations from electronics point of view will be left for further sections.

One drawback of electrostatic transducers is that they require pre-charging in order to function properly. An alternative to pre-charging is the use of electret materials, which are dielectric materials with quasi-permanent electric charge or dipole polarization. Even with this drawback, electrostatic transducer have an advantage over electromagnetic and piezoelectric transducer, due to the ease of integration and compatibility with MEMS and IC fabrication processes.

Comparison of electromechanical transducers

Main advantages and drawbacks of these three types of transducers are summarized in Table 1.2.

Table 1.2: Comparison summary for different types of transducers [13]

	Electromagnetic	Piezoelectric	Electrostatic
Advantages	-robustness -high output currents -proven long lifetime	-no need to control gaps -high output voltages -high capacitances	-lower system costs -high output voltages -coupling factors easier to manipulate -feasible high coupling factors -size reduction increases capacitances
Drawbacks	-low output voltages -typically expensive (material) -inefficient for low frequencies and small size devices -not suitable for MEMS processes	-expensive (material) -coupling factor highly dependent on material properties	-low capacitances -highly affected by parasitics -necessity for control of μm dimensions -no direct electro-mechanical transduction without electret materials

1.6 Circuit for power management

Power management circuit is the next major design point, since it greatly contributes to harvesting efficiency, in terms of performance in capturing, storing and redistributing the energy converted by the transducer. As mentioned before, the type of transducer determines the architecture of the circuit. Consequently, harvesters with electromagnetic transducers typically use simple topology, involving a rectifying bridge

to rectify relatively low AC voltage [34]. Harvesters with piezoelectric transducers usually require rectification as well, and often voltage level conversion, i.e. regulation, since the transducer output voltage is dependent on many factors. Electrostatic harvesters, on the other hand, require control circuitry, to control charge/discharge process and to store the harvested energy efficiently.

Figure 1-7 illustrates the architecture of a vibration harvesting system, outlines the power management circuit. Interface circuit is used to properly transfer the energy converted in the transducer to the energy storage element, whereas the voltage regulator is most likely necessary to provide consistent operating conditions for the load.

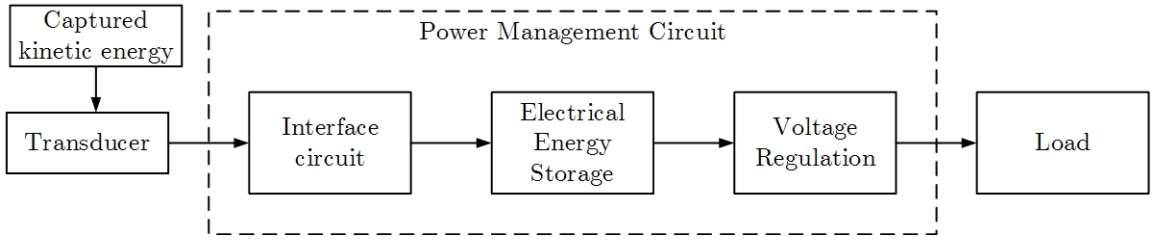


Figure 1-7: *Block diagram of a VEH system* [35]

Obvious requirements for the power management circuits include low power consumption and self-starting properties. For instance, basic electrostatic harvester that requires pre-charging is not self-starting, but one with an integrated electret for start-up is. Aside from low power consumption, the circuit should minimize the losses between the transducer and the storage element.

A more complex property of a power management circuit is the ability to adapt, i.e. reconfigure itself based on the current requirements. For example, if the ambient energy suddenly becomes insufficient, and the harvester dissipates more power than it harvests, the harvester should be able to recognize this, and enter "sleep" mode until the ambient energy becomes sufficient again. Otherwise, the power management and load circuits might consume all the available energy in the storage element, even the one needed for start-up, rendering the harvester useless and in need of maintenance.

Since this work is based on an electrostatic energy harvester, main focus will be on the circuit topologies relevant for electrostatic energy harvesters, and some of the power management topologies will be presented in Chapter 2.

1.7 Thesis scope and limitations

The main goal of this work is to produce a functional design for an autonomous, self-sustaining power management circuit for a VEH system, starting with study and optimization of the work presented in [36], and adapting the topology to fit the requirements.

Most of the previous works done on the topic of electrostatic vibration energy harvesting, as shown in literature review, uses relatively high power circuits for power management, due to the availability of harvested energy. However, the mechanical structure and transducer considered in this work, greatly limit power consumption requirement for this power management circuit due to low amount of harvested energy. As shown in equation (1.3), the electrostatic force which exerts work to generate electrical energy is proportional to the rate of change of capacitance, and this work uses a comb drive capacitor with very small variations which results in low harvested power. Compared to some works, harvested power is up to three orders of magnitude lower, making this project significantly challenging, in terms of power consumption of the power management circuit itself.

Additionally, most designs utilize some external signals for proof of concept, whereas this work aims at a completely autonomous design, including clock signals, current sources etc. Aside from aiming at maximum efficiency of storing the harvested power, this work also focuses decreasing the power consumption of the power management circuit as well.

1.8 Thesis Outline

This chapter stated the motivation for this project and briefly introduced the reader to basic principles of energy harvesting, its purpose and applications.

Chapter 2 focuses on the study of the used harvester structure, for the purpose of specifying the requirements for the power management circuit and description of available topologies for power management circuits.

Chapter 3 explains in details the functionality and purpose of each individual block of the circuit and presents the simulation results achieved in the circuit design.

Final Chapter concludes this thesis with the summary of results and suggestions for improvement and future work.

Chapter 2

Study of the Electrostatic Vibration Energy Harvesting System

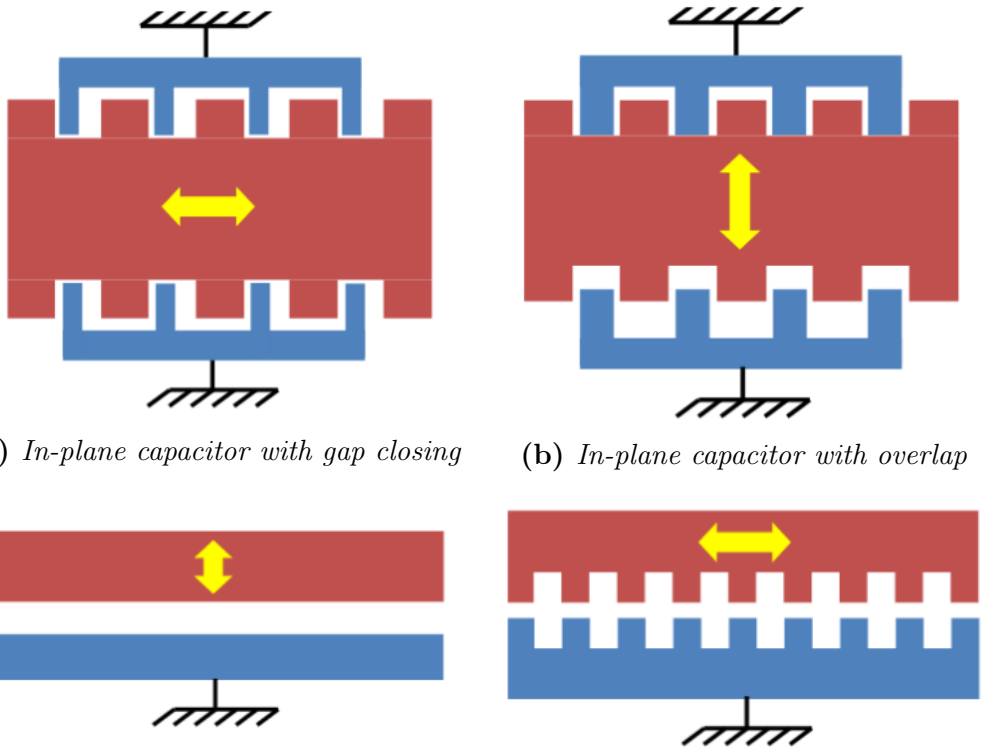
As mentioned in the previous chapter, this work is based on an electrostatic vibration energy harvesting system, since electrostatic transducers are more convenient in a number of ways, including the miniaturization and integration compatibility with MEMS processes. This chapter will focus more on the details of the electrostatic vibration energy harvesting system, highlighting the power management circuit different topologies.

2.1 Electrostatic Transducer

Electrostatic harvesting systems are based on variable capacitors, i.e. the moving mechanical part is usually one of the electrodes of the capacitor, which achieves the variation in the capacitance. Based on the movement type, in the previous chapter we recognized the capacitors with lateral and vertical plate movement. However that was purely conceptual classification. In reality, there are four main structure types for variable MEMS capacitors used in modern harvesting systems as outlined in [13]. These are shown in Figure 2-1 as: *a*) in-plane with gap closing; *b*) in-plane with overlap; *c*) out of plane with gap closing; and *d*) in-plane with variable surface.

All four of these basic shapes can be fabricated as electret-free or electret-based capacitors. Due to ease of integration of such structures in MEMS processes, an abundance of work with different structures has been done, including design, simulations, fabrication and characterization. Some examples can be found in [28, 29, 31, 37] etc.

Seeing as the electrostatic forces acting between the capacitor plates, and the capacitor values are determined by shape of each individual structure, the following



(a) *In-plane capacitor with gap closing*

(b) *In-plane capacitor with overlap*

(c) *Out of plane capacitor with gap closing*

(d) *In-plane capacitor with variable surface*

Figure 2-1: *Basic variable capacitor structures* [13]

sections will outline the main equations for these quantities. But first, let us examine a basic parallel-plate capacitor with an electret layer, shown in Figure 2-2.

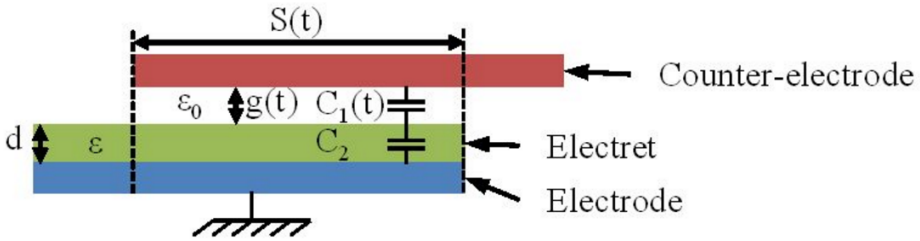


Figure 2-2: *Variable parallel-plate capacitor* [13]

Due to the integrated electret layer, equivalent capacitance can be calculated as two capacitors in series as:

$$C_1(t) = \frac{\varepsilon_0 S(t)}{g(t)}; \quad C_2(t) = \frac{\varepsilon S(t)}{d} = \frac{\varepsilon_0 \varepsilon_r S(t)}{d} \tag{2.1}$$

$$C_{eq}(t) = \frac{C_1(t)C_2(t)}{C_1(t) + C_2(t)} = \frac{\varepsilon_0 S(t)}{g(t) + d/\varepsilon_r} \tag{2.2}$$

where ε_0, ε_r, d, S, g are the vacuum permittivity, electret relative permittivity, electret thickness, overlap surface area, and gap between the parallel plates, respectively.

Attractive electrostatic force, F_{el}, between the capacitor's parallel plates is given by:

$$F_{el} = \frac{d}{dx}\left(W_{el}\right) = \frac{d}{dx}\left(\frac{1}{2}C_{eq}(x)U_c^2(x)\right) = \frac{d}{dx}\left(\frac{1}{2}\frac{Q_c^2(x)}{C_{eq}(x)}\right) \tag{2.3}$$

These equations for the basic parallel plate capacitor will make the derivation of the following equations easier and more comprehensible. It should be noted that these equations are derived for structures with an electret layer. Equations for electret-free structures are simply obtained by setting setting the electret thickness to be 0, i.e. $d = 0$.

2.1.1 Out of plane capacitor with gap closing

Equations for configuration shown in Figure 2-3 can be derived straight from the basic parallel plate model, by substituting the terminology from the figure. Plate movement is modeled as deviation x from the initial gap value g_0, while the overlap surface S is constant.

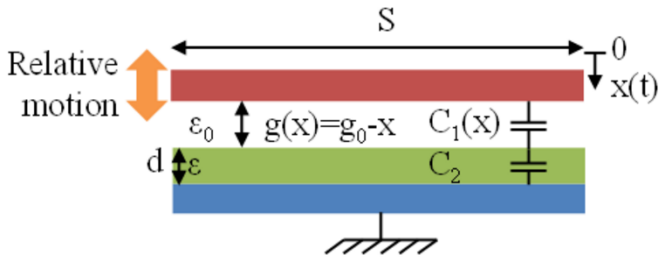


Figure 2-3: *Out of plane gap closing capacitor* [13]

$$C(x) = \frac{\varepsilon_0 S}{(g_0 - x) + d/\varepsilon_r} \tag{2.4}$$

2.1.2 In-plane capacitor with variable overlap surface

Similar to the previous example, equations can be easily derived from the basic model, with the difference of relative plate movement. Namely, in this case the movement is lateral, i.e. the gap is constant and the overlap surface S is variable, which is easily modeled as $S(x) = w\,l(x) = w\,(l_0 - x)$, where l_0 is the initial overlap length, and w is the width of the plate (orthogonal dimension). This can be seen in Figure 2-4.

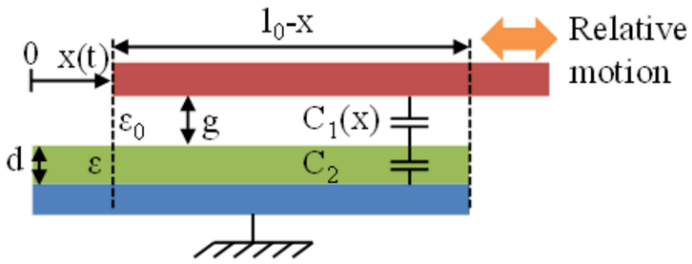


Figure 2-4: *In-plane with variable overlap surface capacitor* [13]

Variable capacitance is now modeled as:

$$C(x) = \frac{\varepsilon_0 \, w}{g + d/\varepsilon_r} \, (l_0 - x) \tag{2.5}$$

2.1.3 In-plane comb capacitor with variable overlap

Illustrated in Figure 2-5 is the comb capacitor with N fingers, and in-plane variable overlap. If top and bottom electrodes are not connected, this structure acts as a dual capacitor, whose capacitances, C_{c1} and C_{c2} vary in anti-phase, i.e. when one capacitance increases due to increase in overlap on its side, the other capacitance decreases for the same value, due to decrease in overlap on its side.

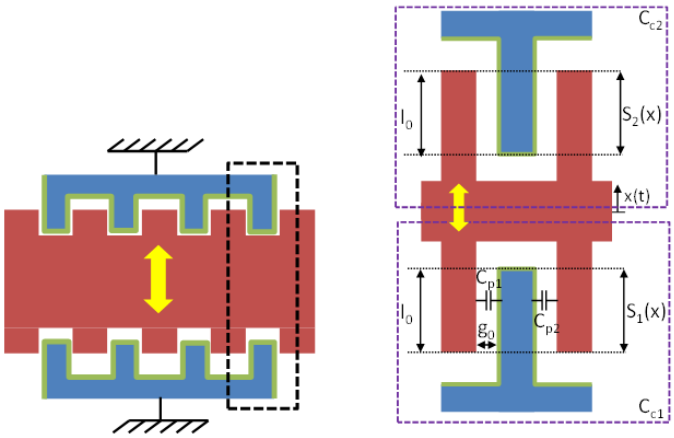


Figure 2-5: *In-plane comb capacitor with variable overlap surface* [13]

Gap between the fingers is considered constant, g_0, and equal for all N fingers of the comb. Thickness of fingers is w (orthogonal dimension), and initial overlap is l_0, and is equal for both sides in absence of excitation. Variable overlap surfaces are modeled as: $S_1(x) = w\,(l_0 - x)$ and $S_2(x) = w\,(l_0 + x)$. Variable capacitances can

now be modeled as:

$$C_{c1}(x) = \frac{\varepsilon_0 N w}{g_0 + d/\varepsilon_r}(l_0 - x) \tag{2.6}$$

$$C_{c2}(x) = \frac{\varepsilon_0 N w}{g_0 + d/\varepsilon_r}(l_0 + x) \tag{2.7}$$

It should be noted that this is a simplified calculation, and that fringing capacitance, along with the capacitance contribution from the tip of the fingers are neglected. This is justified for long, thick and narrow fingers, or if the gap at the tip of the fingers is sufficiently large.

2.1.4 In-plane comb capacitor with gap closing

Similar to the previous example, with the difference in the relative structure motion, this structure has constant overlap length, and therefore constant overlap surface S. Gap between fingers is variable, with the initial value of g_0. As shown in the Figure 2-6, one of the fingers can be modeled as two parallel capacitors, with anti-phase gap variation, i.e. the gap on one side increases, whereas on the other side it decreases. These capacitances can be represented as:

$$C_{p1}(x) = \frac{\varepsilon_0 S}{(g_0 - x) + d/\varepsilon_r} \tag{2.8}$$

$$C_{p2}(x) = \frac{\varepsilon_0 S}{(g_0 + x) + d/\varepsilon_r} \tag{2.9}$$

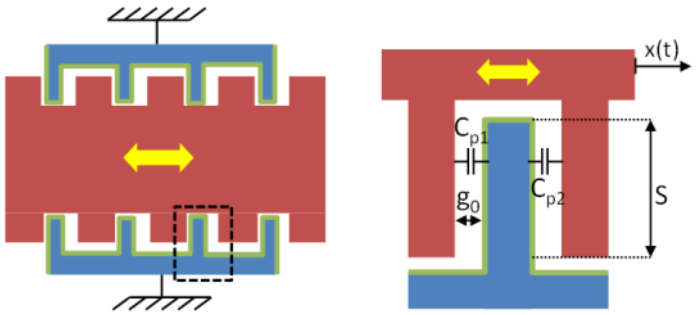


Figure 2-6: *In-plane comb capacitor with gap closing* [13]

Total capacitance contribution of one finger is obtained by adding C_{p1} and C_{p2}. Total capacitance of the structure can be obtained by multiplying with the number

of fingers, N:

$$C_{tot}(x) = C_{p1}(x) + C_{p2}(x) = \frac{2\,N\,\varepsilon_0\,S\,(g_0 + d/\varepsilon_r)}{(g_0 + d/\varepsilon_r)^2 - x^2} \tag{2.10}$$

Same as in previous case, contribution of the tip of the finger to the total finger capacitance is neglected.

2.1.5 In plane capacitor with variable patterned surface

The motivation behind this structure is to increase the capacitance variation for a given lateral displacement x. The structure is similar to the basic parallel plate capacitor, but the electrode surfaces have been patterned, as shown in Figure 2-7.

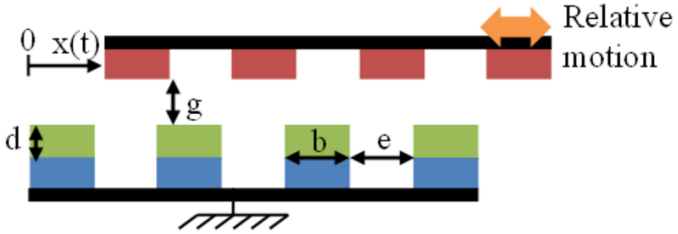


Figure 2-7: *In-plane capacitor with patterned surface electrode* [13]

If the structure is micro-patterned as shown in the figure above, it experiences significantly higher capacitance variation then the other presented structures, for a given displacement, which makes it very desirable for low-amplitude vibrations. Accurate analytical modeling is very difficult for this structure, due to a significant influence of fringe effects, and it is practically impossible to accurately calculate the capacitance. Even the FEM analysis would take unreasonable amount of time to calculate the capacitance as a function of displacement point-by-point. However, it is shown that if dimensions e and b are sufficiently small, capacitance experiences sinusoidal-like variation as a function of displacement, with two extrema: C_{min} and C_{max} [38]. These two values are relatively easy to obtain with FEM analysis, since it is a computation of capacitance for only two displacement values. Once the two values are computed, variable capacitance is conveniently expressed as:

$$C(x) = \frac{C_{max} + C_{min}}{2} + \frac{C_{max} - C_{min}}{2} \times \cos\left(\frac{2\,\pi\,x}{e + b}\right) \tag{2.11}$$

2.1.6 Summary

Previous section gave a brief overview for different MEMS variable capacitor structures. Electrostatic forces are calculated from (2.3), by deriving the electrostatic energy stored in the capacitor. For electret-based devices, the calculation is not as simple as expression change of both voltage and charge of the capacitor when the geometry is changing [13]. The results for electrostatic force for electret-free devices are summarized in Table 2.1 for both voltage and charge constrained mode of operation.

Table 2.1: Electrostatic force for different variable capacitor structures, for both charge and voltage constrained operation modes

Structure	F_{el}-charge constrained	F_{el}-voltage constrained
Out of plane gap closing	$\frac{Q_{const}^2}{2\,\varepsilon_0\,S}$	$\frac{\varepsilon_0\,S\,U_{const}^2}{2(g_0-x)^2}$
In-plane overlap	$\frac{Q_{const}^2\,g_0}{2\,\varepsilon_0\,w(l_0-x)^2}$	$\frac{\varepsilon_0\,w\,U_{const}^2}{2\,g_0}$
In-plane comb overlap (C_{c2})	$\frac{Q_{const}^2\,g_0}{2\,N\,\varepsilon_0\,w\,(l_0+x)^2}$	$\frac{\varepsilon_0\,N\,w\,U_{const}^2}{2\,g_0}$
In-plane comb gap closing	$\frac{Q_{const}^2\,x}{2\,N\,\varepsilon_0\,g_0\,S}$	$\frac{2\,N\,\varepsilon_0\,g_0\,S\,x\,U_{const}^2}{\left(g_0^2-x^2\right)^2}$

2.1.7 Discussion

Even though they offer many advantages, the most important being compatibility and ease of integration with MEMS processes, electrostatic energy harvesters are still the lesser known harvester, especially compared to piezoelectric harvesters. However, with technology advancements, and recent exponential growth of research devoted to MEMS technology, electrostatic harvesters are receiving increased attention of the researchers.

Some limitations should be addressed when it comes to electrostatic transducer structures.

i) Vibration frequency bandwidth and device operation frequency. Environmental vibrations are typically low frequency (< 100Hz). Furthermore, examination of vibration spectrum shows that they are widespread. This calls for low-frequency broadband harvesters. Many solutions are being investigated with complex, non-linear springs. For small-size devices, long and thin springs are needed to achieve this, which makes the structure less robust, since the springs undergo high stress from relatively large proof-masses.

ii) Some structures require gap control. Seeing as large capacitance variation is the key factor for achieving higher output power, it needs to be maximized, imposing the necessity for precise gap control to avoid the pull-in of the electrodes and discharge of accumulated charge, while considering the mechanical properties, such as maximum allowed strain.

iii) The problem of start-up voltage. Can be easily solved with the usage of electret materials. However this imposes a new problem of electret stability, which is highly affected by external conditions, e.g. temperature and humidity. Additionally, necessary precautions must be taken to prevent contacts between electrodes and electret material to avoid discharge of electrets.

2.2 Power management circuit topologies

2.2.1 Primitive (continuous) topologies

Circuit shown in Figure 2-8 represents the most primitive interface circuit [39], consisting of a transducer modeled as a variable capacitor C_{var}, much larger reservoir capacitor C_{res} and a load. While this circuit has very little use for practical implementations in energy harvesters, it can be used in laboratory settings for transducer characterization [29].

Operation of the circuit relies on the assumption that the net charge of both C_{var} and C_{res} is constant in time, meaning that the capacitors are ideal and there are no leakage currents, which is not feasible for real devices. For the sake of simulations, we can use ideal components. The reservoir capacitance must be pre-charged. Initially, before the the variation of C_{var} starts, there is charge redistribution between the pre-charged C_{res} and C_{var}. Once the variations start, the charge will start flowing

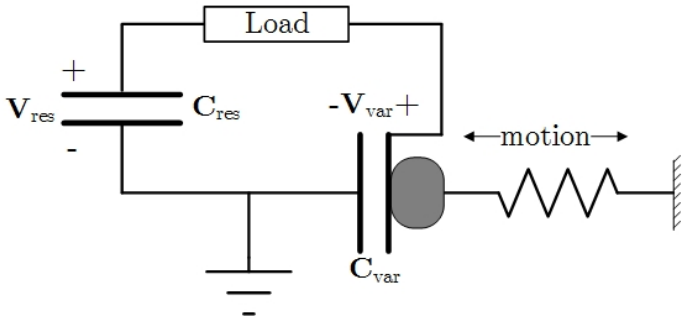


Figure 2-8: *Primitive countinuous interface circuit*

through the load back and forth between the two capacitances. Energy dissipated by the load is restored by the effort of external force that causes capacitance variation. For further illustration of the charge redistribution process, simulation results are shown in Figure 2-9.

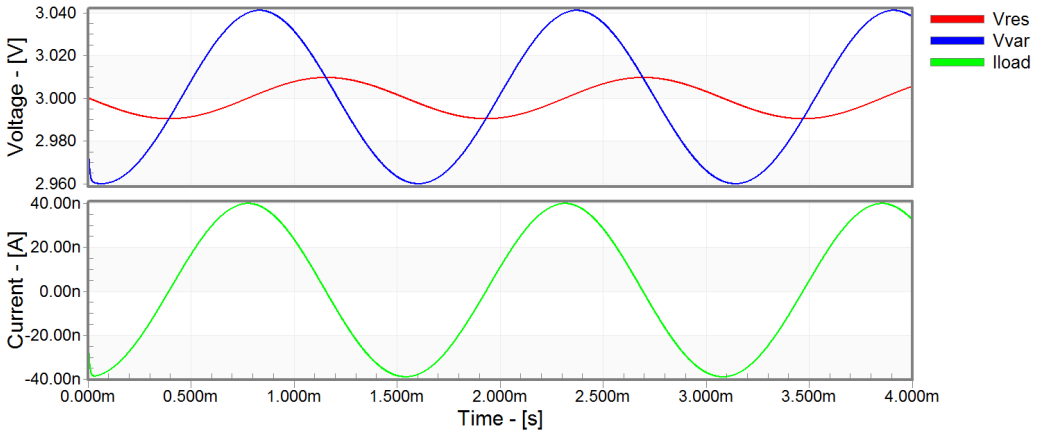


Figure 2-9: *Waveforms for V_{res}, V_{var} and I_{LOAD}*

As seen in figure above, this circuit is unable to increase the pre-charge voltage, it only restores small amount of energy dissipated by the load. Were this a real circuit, the leakage currents would eventually dissipate all the charge stored in capacitors, and the device would not function. Another drawback is that the load is supplied by an AC signal, which imposes the need for additional circuitry for rectification.

2.2.2 Charge Constrained Topology

Charge constrained topology has previously been describe in Chapter 1 from a physics theory point of view. In this section, a more electrical approach is explained. Figure 2-10 illustrates the difference between a charge constrained and voltage constrained energy conversion in the $Q - V$ plane. Both types of conversion start once the

capacitance has reached its maximum value, i.e. the $Q - V$ characteristic has the maximum slope. At that point charge is injected by an external source, which in most cases is a pre-charged reservoir capacitance.

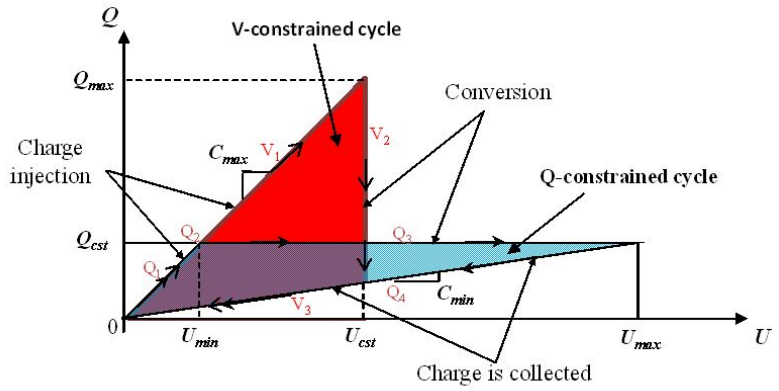


Figure 2-10: *Energy conversion cycles for electret-free devices* [13]

Figure 2-11 depicts a typical charge constrained operation cycle, to further illustrate the charge constrained energy conversion. The cycle starts once the capacitance reaches its maximum value $C_{max}(Q_1)$. At this point, an external source supplies the charge Q_{cst}, and the device is left floating, with a terminal voltage of U_{min}. Due to the work exerted by external forces, capacitance decreases until it reaches the value C_{min}, while the voltage increases, according to equation $Q_{const} = U(t)\,C(t) = U_{max}\,C_{min} = U_{min}\,C_{max}$. Typically the device is now coupled back into a circuit to resupply the storage element.

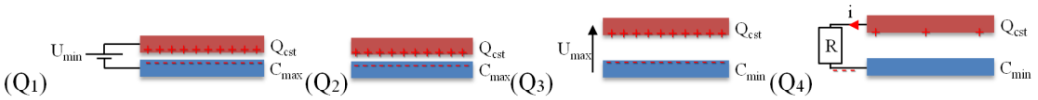


Figure 2-11: *Charge constrained cycle* [13]

Total amount of harvested energy is evaluated as:

$$W_{harvested} = \frac{1}{2}\,Q_{const}^2 \left(\frac{1}{C_{min}} - \frac{1}{C_{max}}\right) \tag{2.12}$$

A charge constrained interface circuit topology, proposed by Meninger et. al. [40] is illustrated in Figure 2-12. It uses an inductor as an intermediate element for energy transfer, and two switches. This circuit also requires pre-charging of the large reservoir capacitance.

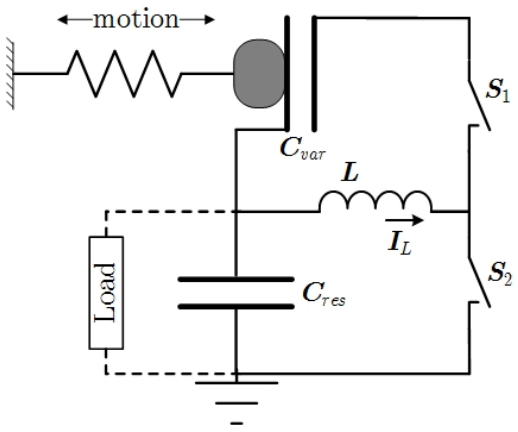
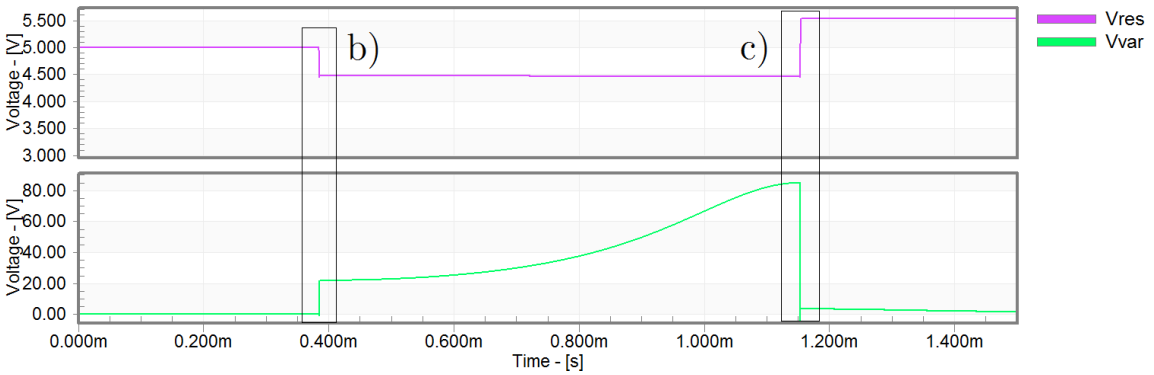
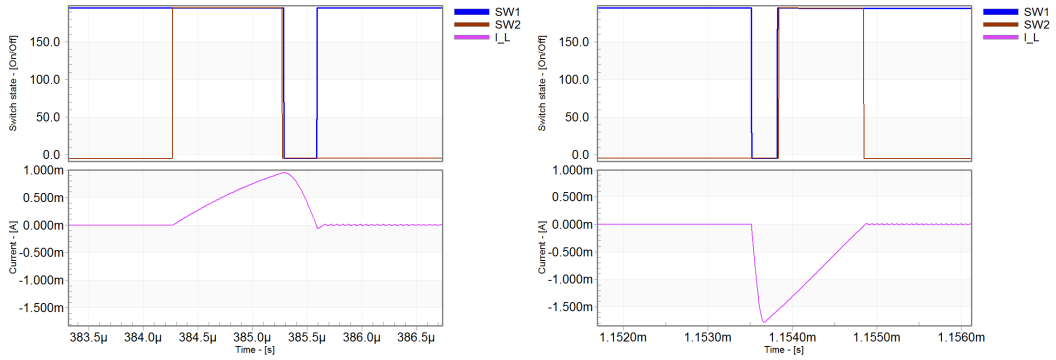


Figure 2-12: *Charge constrained interface circuit*

To illustrate the operation of this circuit in terms of voltage and current waveforms, a simple design was implemented and a simulation was performed. Representative waveforms for one harvesting cycle are presented in Figure 2-13.



(a) *Voltage waveforms for C_{res} and C_{var}*



(b) *State of switches, and inductor current for C_{max}*

(c) *State of switches, and inductor current for C_{min}*

Figure 2-13: *Simulated waveforms for the charge constrained interface circuit*

Operation can be described in a few steps: *i*) When C_{var} reaches its maximum

value, S_2 is closed, and the inductor L is charged-up with the energy from the pre-charged C_{res}; *ii*) S_2 opens and S_1 closes. Energized inductor continues to conduct, now charging C_{var}, which can be seen in Figure 2-13b; *iii*) both switches are open, and the capacitance varies slowly until it reaches its minimum value, while the voltage V_{var} increases; *iv*) S_1 closes, and the inductor is charged-up with the energy from the variable capacitance, with a higher current, due to the high voltage of the variable capacitor now has high voltage; *v*) S_1 opens, S_2 closes, and the energized inductor recharges the reservoir capacitance. It should be noted that the simulation results in Figure 2-13 are for illustration purposes only, because capacitor and inductor values were not chosen to resemble a realistic scenario, but more as a proof of concept illustration.

2.2.3 Voltage Constrained Topology

Voltage constrained energy conversion cycle is illustrated in Figure 2-14. Similar to charge constrained cycle, this cycle also begins when the variable capacitance reaches its maximum value. The capacitor is then connected to an external source, which creates a constant voltage U_{cst} between the plates of the capacitor (V_1). In contrast with the charge constrained cycle, the external source is not disconnected from the transducer, and constant voltage will be maintained at the electrodes throughout the cycle. Having a constant voltage, while the capacitance decreases, the amount of charge will also decrease according to $U_{cst} = \frac{Q(t)}{C(t)}$. In other words there will be a current $i = \frac{dQ}{dt} = C\frac{\partial U}{\partial t} + V\frac{\partial C}{\partial t} = V\frac{dC}{dt}$ flowing from the capacitance and resupplying the source (V_2). By the time the capacitance reaches its minimum value C_{min}, total charge of the capacitor will have been collected and stored in the supply (V_3).

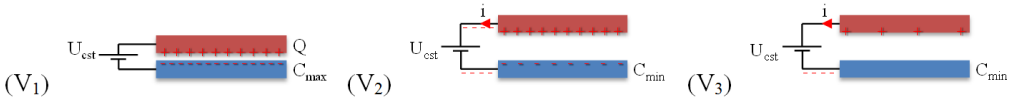


Figure 2-14: *Voltage constrained cycle* [13]

Total amount of harvested energy is evaluated as:

$$W_{harvested} = -\int_{t_0}^{t_1} u(t)\, i(t)\, dt = U_{const}^2\,(C_{max} - C_{min}) \tag{2.13}$$

A simple voltage constrained circuit topology, proposed by Torres et. al. [41] is shown in Figure 2-15. Their proposed circuit uses small thin film Li-Ion polymer battery

instead of a reservoir capacitance, five switches for circuit reconfiguration, an inductor as an intermediate element for energy conversion and a variable capacitor.

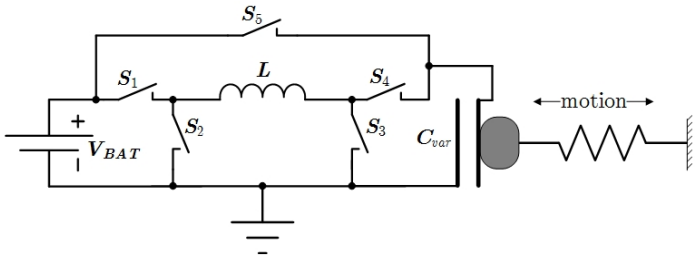


Figure 2-15: *Voltage constrained interface circuit*

A typical operation cycle can be described with two phases: *i*) Pre-charge phase: battery energizes the inductor through switches S_1 and S_3. Inductor current linearly increases, and when the inductor energy becomes sufficient, S_1 and S_3 open. Next step is to drive the energy stored in the inductor to the variable capacitor whose capacitance has reached its maximum value C_{max}. This is accomplished by closing the switches S_2 and S_4, which causes the variable capacitor to be charged to the battery voltage level; *ii*) Harvesting phase begins once switch S_5 closes. Since the voltage on both battery and C_{var} is constant, and the variable capacitance decreases, causing the charge to flow from C_{var} into the battery. Harvesting cycle ends once C_{var} reaches its minimal value. Theoretically, third phase can be energy recovery phase. After harvesting phase, there is still some energy stored in the variable capacitor, which can be recovered through a process reverse of the pre-charge. However the power consumption of the circuit controlling the switches, and power losses of non-ideal components are usually higher than the amount of recovered energy, which would decrease the overall efficiency of the system.

2.2.4 Charge pump topologies

Charge pump interface circuit has one major advantage over the circuits previously mentioned. Namely, they are self-oscillating in terms of charge transfer onto and out of the variable capacitor, by using diodes instead of switches, which significantly simplifies the interface circuit and increases overall system efficiency by decreasing the power dissipation. Several topologies are presented in the following subsections.

Basic charge pump

Basic charge pump circuit, proposed by [28] is shown in Figure 2-16. Operation of the circuit consists of three phases. Initially, diodes are off, and once C_{var} reaches

C_{max}, diode D_1 is on, and charge is transfered from C_res to C_{var}. Once the capacitance starts to decrease, both diodes will be off, until the decrease of capacitance causes sufficient increase in voltage to turn on D_2. In the third phase charge is transferred to an intermediate storage capacitor C_{store}.

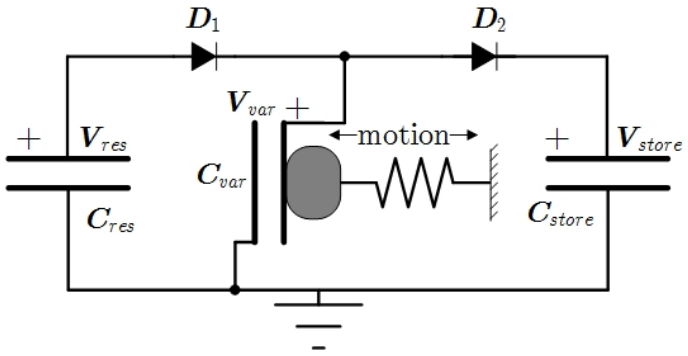
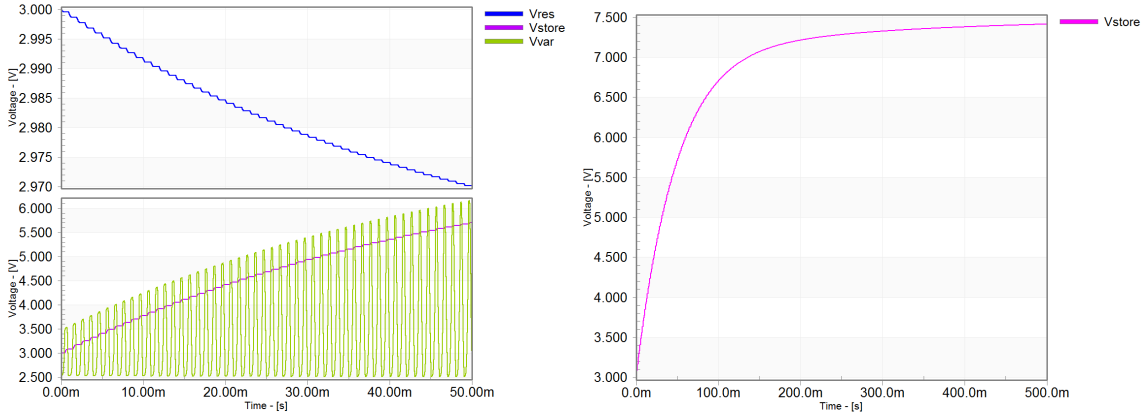


Figure 2-16: *Basic charge pump interface circuit*

Since the diodes only enable a unidirectional flow of charge ($C_{res} \rightarrow C_{var} \rightarrow C_{store}$), this circuit has no practical significance. After a number of oscillation intervals, the voltage at C_{store} will begin to saturate at:

$$V_{store,sat} = \left(\frac{C_{max}}{C_{min}}\right) V_{res} \tag{2.14}$$

which can be seen in the simulation waveforms shown in Figure 2-17b. Following sections will present a few possible methods for a return path, so the harvested energy is used to resupply C_{res}.



(a) *Waveforms for V_{res}, V_{var} and V_{store}* **(b)** *Saturation of V_{store} over a longer period*

Figure 2-17: *Simulation results for the basic charge pump circuit*

Charge pump with resistive return path

The simplest method for resupplying C_{res} is by using a resistor in the return path from C_{store} to C_{res} [42], as shown in Figure 2-18. Now, there are two paths for flow of charges, one from the reservoir capacitor to storage capacitor pumped by the variable capacitor and diodes, and another in the opposite direction, through the resistor, due to the voltage drop $V_{resistor} = V_{store} - V_{res}$.

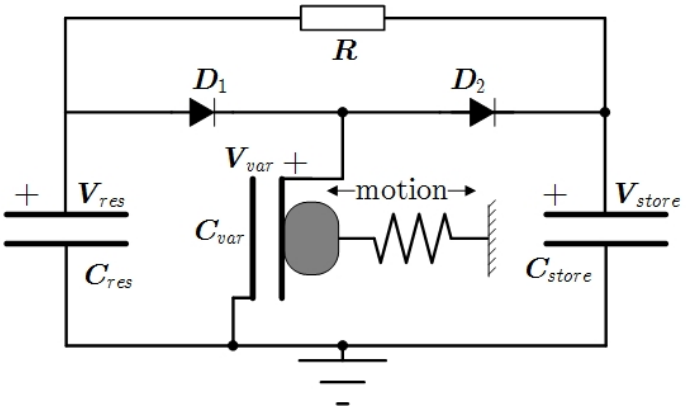


Figure 2-18: *Charge pump with a resistive return path*

Although it offers simplicity, this circuit also has very little use in energy harvesters, except for laboratory testing [31], transducer characterization and such. A major drawback of the circuit is that it cannot increase the pre-charge voltage V_{res}, because the energy cannot be accumulated, as illustrated with simulated waveforms shown in Figure 2-19, it only restores energy dissipated by the resistance. In a real setting, capacitors would have some leakage, and eventually capacitors would discharge and circuit would become inactive.

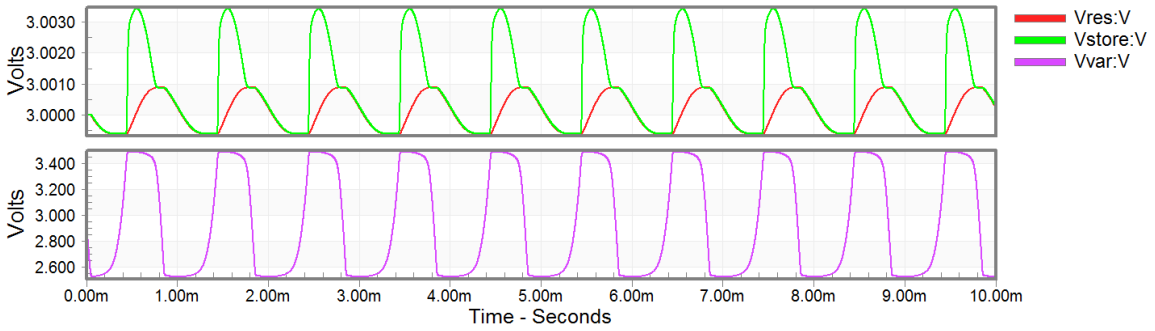


Figure 2-19: *Voltage waveforms for simulated charge pump with a resistive return path*

Charge pump with inductive flyback path

This circuit is based on a famous Buck converter, and was proposed by Yen et. al. [42], and is shown in Figure 2-20. This topology offers various advantages, the most important of which is acuumulation of energy. Namely, while the switch is kept open, the inductive flyback path is not connected, allowing the charge to accumulate on C_{store}, and once the switch closes, the charge is transferred to C_{res}, through the flyback inductor. Diode D_{fly} has the purpose of maintaining the inductor current after the switch opens. As the load is not connected, the energy accumulates on C_{res} which allows increase of the pre-charge voltage. Another advantage is the reduced complexity of the switch control circuit, compared to previously presented circuits, since there is only one switch in the circuit and its state is a function of V_{store} instead of C_{var}.

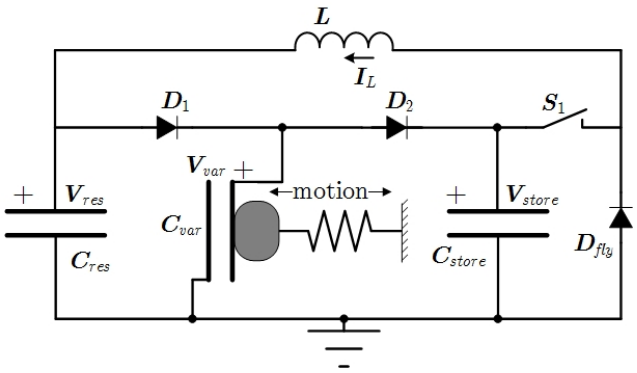


Figure 2-20: *Charge pump with a inductive flyback return path*

Figure 2-21 represents simulated waveforms for V_{res} and V_{store} over a longer period of time. It is shown that once the V_{store} rises to the proximity of its saturation voltage, the switch is closed, and the charge is transferred from C_{store} to C_{res}, through the inductor, causing the increase in V_{res}.

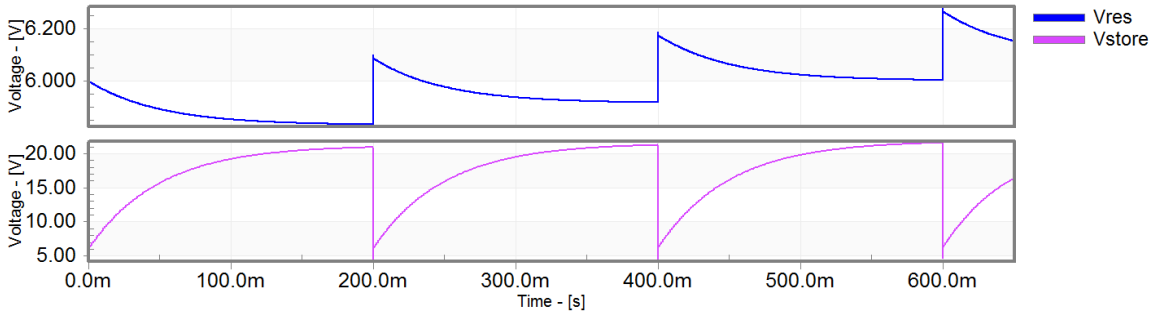


Figure 2-21: *Voltage waveforms for simulated charge pump with an inductive return path*

Double charge pump

For transducers which allow having two anti-phase variable capacitances, such as the one shown in Figure 2-5, double charge pump circuit can be used, such as the one shown below in Figure 2-22. This circuit has the same working principle as basic charge pump, but it has twice the frequency of charge flow from C_{res} to C_{store}. In the first half-period, $C_{var1} = C_{max}$, $C_{var2} = C_{min}$. Consequently, diodes D_1 and D_4 are on, whereas D_2 and D_4 are off, allowing C_{res} to transfer its charge to C_{var1} and C_{var2} to C_{store}. In the second half-period, state of the diodes is complement.

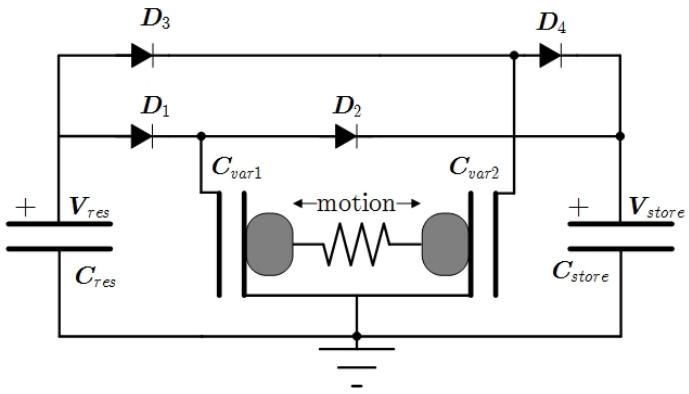
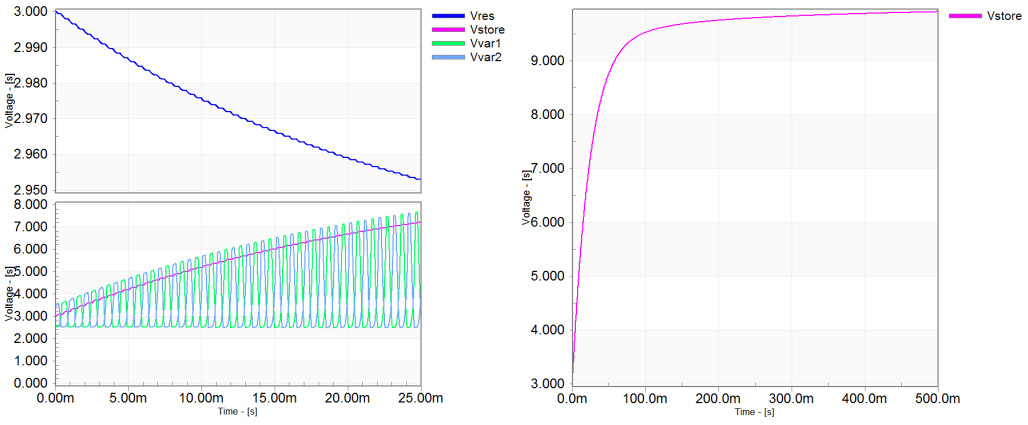


Figure 2-22: *Double charge pump interface circuit*

Circuit has been simulated with the same operating conditions and parameter values as the basic charge pump, and the simulation results are presented in Figure 2-23. The charge is transferred from C_res with twice the frequency: in the first half-period to C_{var1} and in the second C_{var2}, as shown in Figure 2-23a. Consequently, the saturation voltage $V_{store,sat}$ on C_{store} is reached twice as fast, making this circuit topology twice as effective as basic charge pump. Additionally it is easily expanded with an inductive flyback path.



(a) *Simulated waveforms for V_{res}, V_{var} and V_{store}*

(b) *Saturation of V_{store} over a longer period*

Figure 2-23: *Simulation results for the double charge pump circuit*

2.3 Summary and Discussion

This chapter presented various transducer structures, outlining their advantages and drawbacks. In summary, structures that offer higher capacitance variations tend to be more efficient for energy harvesting applications, if coupled with an effective interface circuit. In traditional structures, such as ones shown Figures 2-3,2-4, 2-6 and 2-5 capacitance variation is restricted by the by mechanical limits, i.e. maximum displacement of the proof mass, which in some cases makes it difficult to achieve high variations. Structures such as the one shown in Figure 2-7, offer higher capacitance variation with very little limitation from maximum displacement. This comes at the expense of fabrication cost and complexity, since the patterned surface needs to fulfill certain requirements.

Second part of this chapter focused on the energy interface circuits, in terms of their role in energy harvesters, their efficiency requirements and different existing topologies. Even though voltage constrained circuits seem to offer higher efficiency than their charge constrained counterparts [43], their accompanying control circuit is much more complex, and therefore much more power hungry. To avoid the complex operation of switch synchronization with the variable capacitance, charge pump topologies offer a convenient self-oscillating mode of operation, as illustrated above. Since this project is based on a comb structured transducer, with dual, anti-phase variable capacitances, double charge pump topology is chosen as the interface circuit, due to the many advantages it offers. The return path is with an inductive flyback element, because it offers the possibility of energy accumulation, and hence the pre-charge voltage increase, whereas conversely the resistive return cannot.

Chapter 3

Interface circuit and flyback switch control circuit design

This chapter is dedicated entirely to the electronic circuit part of the harvesting system. First two sections provide technical information concerning the project. Following sections are dedicated to the previous work on this project, concerning the interface circuit, as well as modifications made in this project, followed up by additional components necessary to make this circuit autonomous.

3.1 Software tools

For the purpose of this project, *Tanner EDA Tools v16.3* was used for circuit design and simulations. Tanner EDA Tools is an integral part of *Mentor Graphics*®, which allows full analog-mixed signal design process, including schematic capture (*S-Edit*), circuit simulation (*T-Spice*), waveform viewing (*W-Edit*), IC layout design with parasitic extraction (*L-Edit*) and verification (*Verify DRC* and *LVS*). This project was focused on circuit design in schematic view and simulations with *T-Spice*.

3.2 Process technology

For the purpose of this project, energy harvester node with energy accumulation, higher than standard voltages are expected, and to that end, high-voltage CMOS process from Austria-Microsystems was used (*AMSH35*). Originally released in 2004, it is a very mature process, with vast experience among the circuit designers and reliable models for components. It offers *MIM* capacitors and both low and high-

voltage MOSFETs.

The most important process parameters are outlined in Table 3.1. Technology is based around a $3.3V$ MOS transistors using thin oxide, with a minimum feature of $0.35\mu m$. Aside from that, there are transistors which can withstand higher gate voltages, $5V$ and $20V$, using medium and thick oxide. Capacitors can be designed using the two available poly-silicon layers, however higher poly-silicon resistivity should be taken into consideration, since it degrades the capacitor properties, such as linearity, ESR etc. Advantage is that the same capacitance occupies less area than its MOS counterpart.

Table 3.1: Relevant 0.35μm process parameters

Process technology	HV CMOS 0.35μm
Gate oxide capacitance	$4.54\ fF/\mu m^2$
V_{th} for standard NMOS short/long channel	$0.5/0.46\,V$
Gain factor K_N for standard NMOS	$170\,\mu A/V^2$
V_{th} for standard PMOS short/long channel	$-0.68/-0.65\,V$
Gain factor K_N for standard PMOS	$58\,\mu A/V^2$
V_{th} for thin oxide HV NMOS short/long channel	$0.45/0.47\,V$
V_{th} for thin oxide HV PMOS short/long channel	$-0.63/-0.7\,V$
Supply voltage	$3.3V$, $5V$, $20V$, $50V$
$\lvert V_{G-S/B,max}\rvert$ for thin, medium, thick oxide devices	$3.3V, 5V, 20V$

In this design, $20V$ HV MOS transistors with thin oxide are used in high-voltage interface circuits, to be able to withstand higher voltages in the long-term circuit operation. There are several drawbacks of using HV transistors, including the need for longer channel devices in order to achieve high breakdown voltages, which increases the channel resistance as well as higher gate capacitance. However, HV transistors are a necessity, since the circuit would ideally increase the voltage to a higher value, but understanding the limitations of the technology is an important design point for creating a functional and reliable design.

3.3 Transducer model

As was previously mentioned, transducer considered for this project is a comb-drive based structure, consisting of a relatively large proof-mass suspended by four springs which are connected to two fixed electrodes (anchors), with N being number of overlap fingers, l_0 initial overlap without excitation, g_0 constant gap, as shown in Figure 3-1.

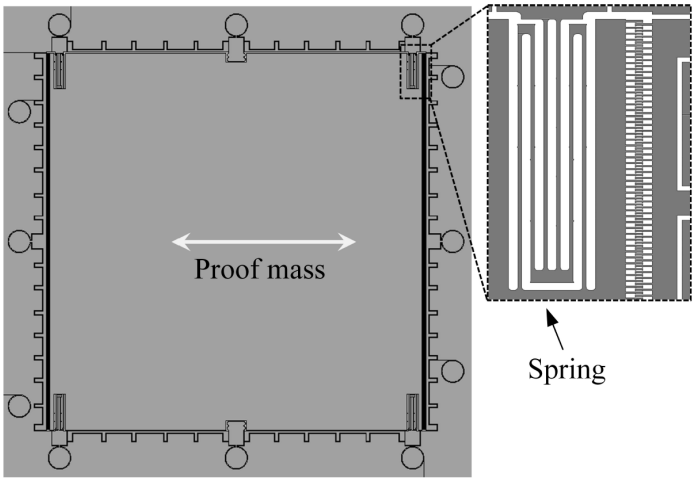


Figure 3-1: *In-plane comb capacitor with variable overlap* [36]

Variable capacitance can be expressed as:

$$C_{c1/2}(x) = \frac{N\,\varepsilon_0\,w}{g_0}(l_0 \mp -x) = \frac{N\,\varepsilon_0\,w\,l_0}{g_0}\left(1 \mp \frac{x}{l_0}\right) = C_0\left(1 \mp -\frac{x}{l_0}\right) \tag{3.1}$$

where ε_0 and x are vacuum permittivity and proof-mass displacement, respectively. However, there is a parasitic capacitance in parallel with the variable capacitor. Including this effect, the transducer can be modeled in electrical domain as shown in Figure 3-2. In real devices, these parasitic capacitances are not equal, due to process variations and mismatch effects, but their difference can be considered negligible for this analysis.

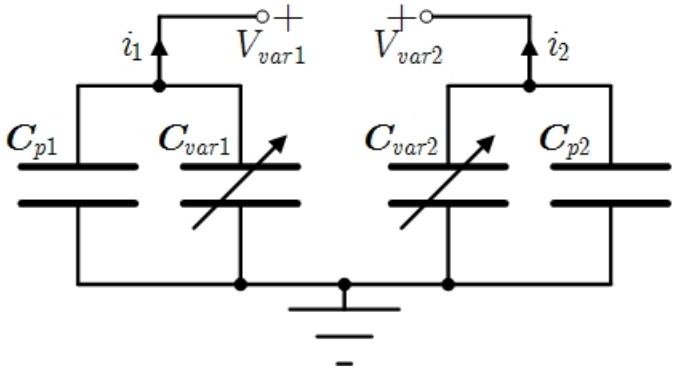


Figure 3-2: *Electrical domain transducer model*

Take note that the currents $i_1 = -\dot{q}_1$ and $i_2 = -\dot{q}_2$ represent the charge flow due to capacitance variation, q_1 and q_2 being charge of the individual capacitors. Transducer

interface voltages can now be expressed as:

$$V_{var1/2} = \frac{q_{1/2}}{C_{var1/2}(x) + C_p} \tag{3.2}$$

Capacitance variation

In order to continue with circuit design and implementation, parameters for the variable capacitors are needed. Disregarding process variations and mismatch effects, variable capacitances are considered to have same parameters, as are their respective parasitic capacitances. These parameters are summarized in Table 3.2.

Table 3.2: Parameters of the transducer

Parameter	Value
Capacitance when idle, C_0	2.3 pF
Parasitic Capacitance, C_p	2 pF
Overlap when idle, l_0	16 μm
Maximum displacement, x_{max}	15μm
Resonant frequency, f_0	650 Hz

For the purpose of simulations, a single harmonic vibration at resonant frequency is assumed. If the the vibration force has a sinusoidal shape, considering linear springs, response of the transducer, in terms of proof-mass displacement, i.e. overlap length x will have the following form:

$$x(t) = x_{max} \sin(2\pi f_0 t) \tag{3.3}$$

Total variable capacitance, under such excitation is obtained by substituting (3.3) into (3.1) and including the parasitic capacitance:

$$C_{v1/2} = C_p + C_{var1/2} = C_p + C_0 \left(1 \mp \frac{x_{max} \sin(2\pi f_0 t)}{l_0}\right) \tag{3.4}$$

For further simplification and convenience, expression (3.4) can be rewriten as:

$$C_{v1/2} = (C_p + C_0) \mp C_0 \frac{x_{max}}{l_0} \sin(2\pi f_0 t) = C_{const} + \Delta C \sin(2\pi f_0 t) \tag{3.5}$$

where $C_{const} = C_p + C_0 = 4.3\text{pF}$ and $\Delta C = C_0 \frac{x_{max}}{l_0} = 2.16\text{pF}$. Consequently, the capacitance variation range is: $C_{v1/2} \in [\, C_{min},\, C_{max} \,] = [\, 2.14,\, 6.46 \,]$ pF.

These capacitances are modeled in Tanner Tools' *S-Edit* by instantiating a sine-wave voltage source with a DC offset of 4.3 and amplitude of 2.16, and using its output as a parameter with which to multiply a 1pF capacitance.

3.4 Interface circuit topology

Due to transducer structure with two anti-phase variable capacitances, a double charge pump topology is used, utilizing an inductive flyback return path. Final interface circuit, with the exception of the flyback switch control circuit, can be seen in Figure 3-3. Switch control circuit will be described in details in following sections.

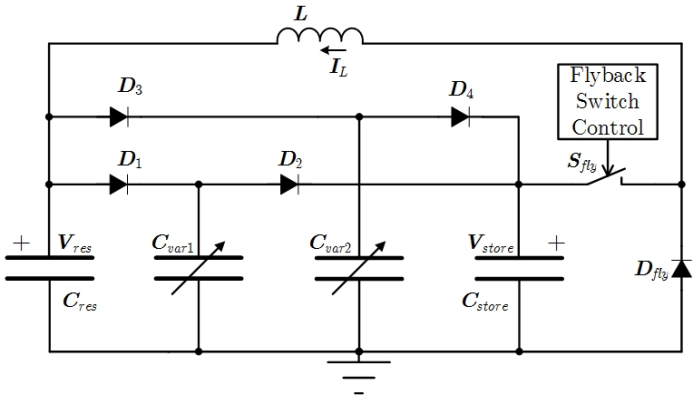


Figure 3-3: *Double charge pump interface circuit with inductive flyback return path*

To illustrate energy harvesting process with this circuit topology and transducer parameters, a simulation was preformed using the circuit seen in Figure 3-3, and simulation results are shown in Figure 3-4. For the purpose of this simulation, and estimation of harvested energy with an externally controlled switch, an appropriately connected, ideal pulse generator was used. V_{res} voltage waveform is presented in Figure 3-4.

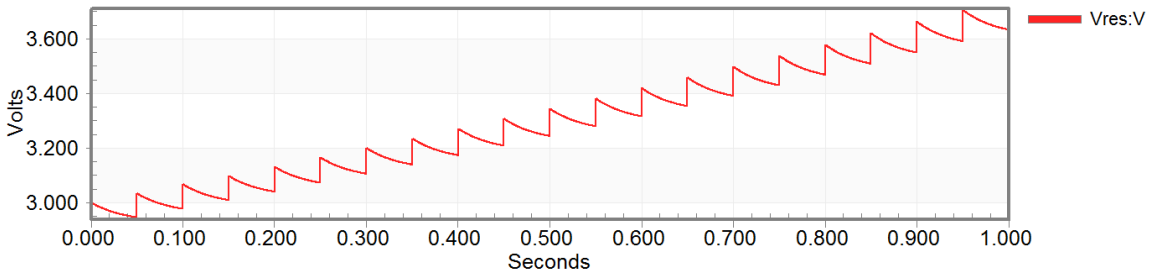


Figure 3-4: *Voltage waveform of V_{res} externally controlled double charge pump circuit*

As seen in figure above, a voltage simulated increase over $1s$ of simulation time amounts to $\Delta V_{res} = 0.63V$. Estimation of harvested energy can be expressed as a

difference of stored energy in the reservoir capacitance at the end and the beginning of the simulation.

$$W_{harvested} = \Delta W_{res} = \frac{1}{2} C_{res} \left(V_{res}^2 \mid_{t=t_{sim}} - V_{res}^2 \mid_{t=0} \right) = 8.33nJ \tag{3.6}$$

or in terms of harvested power averaged over time period of $1s$:

$$P_{harvested,ext} = \frac{W_{harvested}}{\Delta t} = \frac{W_{harvested}}{t_{sim}} = 8.33nW \tag{3.7}$$

Initially, parametric simulations were performed to determine optimal period and pulse width of the pulse generator. It was noticed that maximum voltage increase on C_{res}, for $1s$ simulation time, is achieved with a period $T_{pulse} = 50ms$ and pulse width of $\tau = 1.2\mu s$. Choosing an optimal value for the period reflects the trade-off between the amount of the charge collected from C_store for one switching cycle and the average amount of charge collected over a longer period. Since the voltage increase on C_{store} has a logarithmic form and a saturation limit, waiting longer for harvesting phase is not very efficient. On the other hand, analysis of choosing an optimal pulse width, i.e. the time during which the switch is on, is a more complex analysis which will be explained later. For now, it should be noted that lower pulse width would cause Table 3.3 offers a comparison of harvested energy for different pulse signal periods, with initial, pre-charge voltage $V_{res} = 3V$ and pulse width $\tau = 1.2\mu s$.

Table 3.3: Harvested energy vs. pulse signal period

Pulse period, T_{pulse}	$V_{res}\|_{t=1s}$	Harvested energy, $W_{harvested}$
$1.563ms$	$3.0002V$	$0.006nJ$
$2ms$	$3.00V7$	$0.210nJ$
$10ms$	$3.084V$	$2.555nJ$
$25ms$	$3.204V$	$6.328nJ$
$50ms$	$3.266V$	$8.334nJ$
$100ms$	$3.145V$	$4.455nJ$
$500ms$	$2.975V$	$-0.747nJ$

Discussion of the results

It should be noted that even though harvested energy is negative for $T_{pulse} = 500ms$, average harvested power over a longer period of time would not be. This happened because C_{store} is well saturated before the switching happens, and the time waited for the switch to open is not justified by the amount of energy harvested. It happened that during $1s$ of simulated circuit operation C_{store} saturated twice,

whereas switch turned on only once. In other words, had the simulation time been $10\mu s$ longer, the switch would have activated, and total harvested energy would be positive. Additionally, as seen from the table that the lowest amount of harvested energy is obtained for very low switching period, $T_{pulse} = 1.563ms$. In fact, this switching period is the same as the vibration oscillation period, meaning that the energy is harvested every complete capacitance variation cycle, and practically the harvested energy only restores the power dissipated by the switch, and V_{res} only oscillates around its pre-charge value. If the pulse period is decreased further, this circuit would behave almost exactly like the one with resistive return path. On a different note, if the pulse period is increased too much, the circuit will eventually dissipate

3.5 Previous Work

As mentioned previously, this project is based on a project by an MSc. student, Tra Nguyen Phan [36], which produced a functional, but not a completely self-sustaining, interface circuit with synchronous switch control. This section covers major design points of the previous work, while providing additional analysis and including necessary circuit considerations, in order to: *i*) offer deeper understanding of the work previously done; *ii*) help reader relate design decisions of the two projects; and *iii*) single out major considerations for future work.

3.5.1 Return path circuit

Return path features a flyback inductor, realistically modeled with its inductance L, series resistance R_w and its core resistance R_{core} parallel to the inductance, and a diode D_{fly} used to maintain inductor current after switch is turned off, as shown in Figure 3-5.

The fact that the switch is in high-side configuration, makes the control circuit more complex. When off, the switch is connected between the highest potential in the circuit, V_{store}, and significantly lower voltage V_{res}. If NMOS transistor was to be used as a switch, the gate voltage necessary to turn it on would have to be higher than V_{store}, thus using a high-voltage PMOS switch is a more reasonable design decision. High-voltage MOSFET components used in this circuit are thin-oxide devices. Even though their maximum allowed voltage between drain and source terminals can be higher ($3.3V, 5V, 20V, 50V$, depending on the component), they have a lower gate-

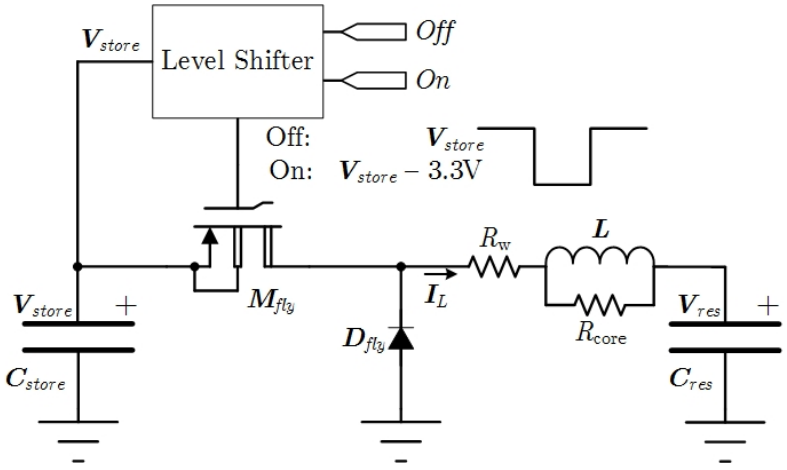


Figure 3-5: *Simplified illustration of the flyback return path*

source/bulk voltage limit ($3.3V$). Therefore, in order to successfully drive this switch, gate voltage of the PMOS transistor should have a voltage swing within the range of: $[V_{store} - 3.3V, V_{store}]$. This is achieved using a voltage level shifter circuit.

3.5.2 Voltage level shifter

Many level shifting circuits exist today, such as ones presented in [44, 45, 46], but many of them do not fit the requirements for this circuit, in terms of power consumption or process technology. However, a topology of a flip-flop level shifter proposed in [47] has zero static power consumption, and it is compatible with HV process used in this project. This circuit acts as an analog flip-flop, where flip-flop action is reflected in two possible states that the circuit can provide on its output. Flip-flop level shifter is presented in Figure 3-6. It consists of high voltage PMOS transistors M_{P4} and M_{P5} and two capacitors C_1 and C_2. Diode connected MOSFETs serve the purpose of limiting the voltage across PMOS devices, and switch pairs $M_{P6} - M_{P7}$ and $M_{P8} - M_{P9}$ to allow charging/discharging current of nodes $set/reset$ only when transistors M_{N1}/M_{N2} are on, i.e in the presence of On/Off pulses. Transistor M_{SW} is in fact the flyback switch.

The circuit is controlled by low voltage (e.g. $3.3V$) external signals on and off, and depending on impulses introduced to the gates of M_{N1} and M_{N2}, output set will have either the value of V_S, which is actually V_{store}, or $V_{store} - 3V$. If On receives a short pulse, C_1 is charged to $3V$ through $M_{P6} - M_{P7}$ pair switch and diode connected MOSFETs, which reflects in the voltage at set node as $V_{set} = V_S - 3V$. Consequently, this turns on M_{P4}, causing the voltage at $reset$ node to be pulled-up at V_S, which in turn discharges C_2. Analogously, circuit operates in similar manner for Off sig-

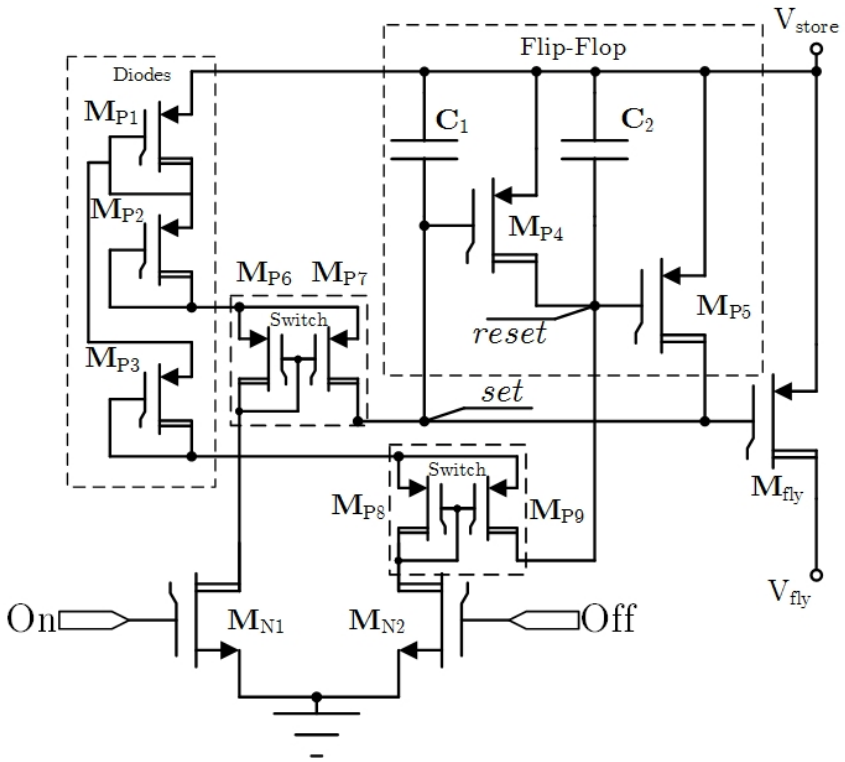


Figure 3-6: *Flip-flop level shifter*

nal pulse. Interestingly, the only two current paths in the circuit are controlled by transistors M_{N1} and M_{N2}. Consequently, in the absence of these pulses, there are no current paths, and thus no power consumption.

3.5.3 Synchronous switch control circuit

For further discussion of the decision-making circuit design, an analysis of switching time, in terms of pulse signal period and pulse width, is required. Let us consider again the circuit illustrated in Figure 3-5, starting from the moment the switch turns on. We can justify neglecting the effect variable capacitances, inductor related resistances and PMOS switch R_{ON} resistance for the purpose of this analysis, since their influence is negligible due to their respective values. Resulting circuit consists of serially connected C_{res}, L and C_{store}. There are four governing equations for this circuit, concerning the current-voltage relations for all three elements and one KVL equation relating the voltages in the circuit. Current-voltage relations are differential equations, so in order to simplify this analysis, *Laplace* transform will be used. To get an accurate evaluation of transient response with the *Laplace* transform, initial condition values need to be considered carefully, specifically the initial condition concerning the inductor current, and voltages of C_{res} and C_{store}. The analysis of the circuit if con-

sidered at the moment of the switch closing, represented by $t = 0$. Before the switch closing $t = 0^-$, the inductor current was zero, and due to energy conservation law, the inductor current cannot change instantaneously, thus the initial condition for the inductor current is $i_L(t = 0^-) = i_L(t = 0) = i_L(t = 0^+) = 0$. Initial values for capacitor voltages are more complex to estimate. However, as these values are relevant for the switching time optimization, this analysis will be performed in the next section. For now, simulated initial values are used, and they are: $V_{res}(t = 0^+) = 2.965$ and $V_{store}(t = 0^+) = 6.137V$. Noting that $i_L(t) = i_{C_{res}}(t) = -i_{C_{store}}$, we can write the governing equations and their Laplace transforms:

$$v_L(t) = L\frac{di_L(t)}{dt} \quad \xrightarrow{\mathcal{L}} \quad V_L = L\left(sI_L - i_L(0)\right) \tag{3.8}$$

$$i_{res}(t) = C_{res}\frac{dv_{res}(t)}{dt} \quad \xrightarrow{\mathcal{L}} \quad I_{res} = C_{res}\left(sV_{res} - v_{res}(0)\right) \tag{3.9}$$

$$i_{store}(t) = C_{store}\frac{dv_{store}(t)}{dt} \quad \xrightarrow{\mathcal{L}} \quad I_{store} = C_{res}\left(sV_{store} - v_{store}(0)\right) \tag{3.10}$$

$$v_L(t) = v_{store}(t) - v_{res}(t) \quad \xrightarrow{\mathcal{L}} \quad V_L = V_{store} - V_{res} \tag{3.11}$$

Solving for I_L, we get the expression for inductor current in *Laplace* domain, and in time domian after applying the inverse *Laplace* transform:

$$I_L = \sqrt{\frac{C_{series}}{L}}v_L(0)\frac{\omega_0}{s^2 + \omega_0^2} \quad \xrightarrow{\mathcal{L}^{-1}} \quad i_L(t) = \sqrt{\frac{C_{series}}{L}}v_L(0)\sin(\omega_0 t) \tag{3.12}$$

with $v_L(0) = v_{store}(0) - v_{res}(0)$ being the initial inductor voltage, $\omega_0 = \frac{1}{\sqrt{L\,C_{series}}}$ the circuit resonant frequency and $C_{series} = \frac{C_{store}C_{res}}{C_{store}+C_{res}}$. Note that the switch closing action reconfigures this circuit into a resonant LC circuit with the resonant frequency $f_0 = \frac{\omega_0}{2\pi} = 241\,kHz$. The inductor current has a transient response in the form of a pure sine wave with the period $T_0 = 4.15\mu s$, and amplitude $I_{L,max} = 523\mu A$. We can make the following conclusions: *i*) Once the switch closes, inductor starts storing the energy from C_{store} with current following a sine wave shape; *ii*) To optimize harvested energy, the switch should be closed once the inductor is fully energized, i.e. when its current reaches its peak value, $I_{L,max}$.; *iii*) According to (3.12), this will happen, once the sine function reaches its first maximum, i.e. $\tau = T_0/4 = 1.03\mu s$ after the switch closes, which determines the optimal pulse width; *iv*) Once the switch closes, energized inductor will lower the potential of the diode D_{fly} enough so the diode can conduct. This way the inductor can fully discharge its stored energy into C_{res}.

To support previous analysis, another simulation of the circuit presented in Figure

3-4 has been performed, but with the focus on the first harvesting phase, that is after the first $t = 50ms$ of operation. Simulation results are presented in Figure 3-7. It can be seen that when the switch opens, the inductor voltage becomes negative, which is necessary to turn on the diode. From that momen, the diode takes over all of the inductor's current. Markers are placed on the plot at the moment of switch closing and at the moment determined by the analysis. It can be seen that the analysis was accurate to a high extent. However, there is a slight deviation from the calculated value. This is due to the non-ideal components, i.e. the resistance of the switch and the inductor related resistances.

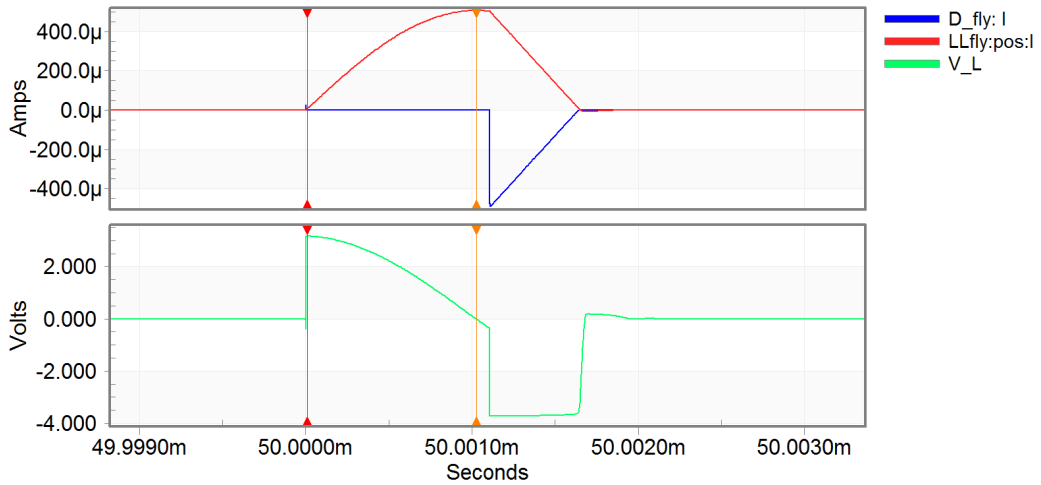


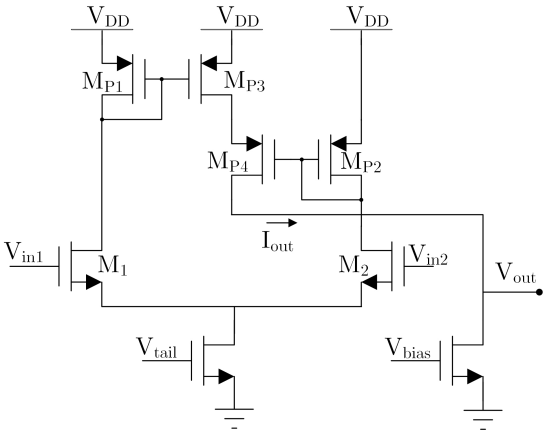
Figure 3-7: *Simulation results supporting the pulse width analysis*

The tendency of this design is to be fully autonomous, reliable and flexible. With that in mind, it is not a good practice to make a pulse generator which would turn on the switch with a constant period. Instead, the switch should be controlled by the response of the interface circuit. As it was determined that the optimal switching time is when the inductor current reaches its peak value, this will be the decision making event for the switch opening. It is hard and impractical for many reasons to monitor the current of the inductor, and determine whether it reached its maximum value. A more practical approach is to monitor the voltage of the inductor, because, according to (3.8), inductor voltage will be zero when the current is at the maximum value. This can also be seen on the waveform.

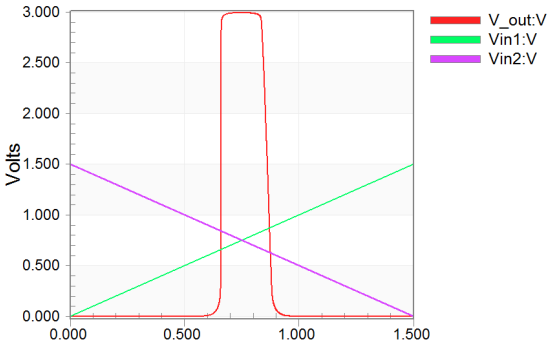
Following parts cover the voltage monitoring circuit and other relevant components.

"Bump" circuit

For monitoring voltage of the inductor a "Bump" circuit topology was used [48]. As shown in Figure 3-8a, bump circuit employs a simple current correlator consisting of four transistors, $M_{P1} - M_{P4}$ and an input differential pair M_1 and M_2 with a transistor for controlling the tail current. This is essentially a transconductance circuit, which converts the differential input voltage to the output current. Thus an externally biased transistor is added at the output, allowing the circuit to have a voltage response.



(a) *Schematic*



(b) *Bump circuit voltage response*

Figure 3-8: *"Bump" circuit*

Off event decision

An instance of the bump circuit is responsible for generating *off* pulse for the switch controlling flip-flop level-shifter. Input differential pair receives the voltages of inductor terminals, and once the inductor voltage reaches zero, it generates an output pulse. Quickly after the pulse, switch is turned off, the inductor voltage changes to a value $\neq 0$, and the output of the bump circuit becomes zero again. In other words, the operation of this instance is required only during the time for which the switch is on. Therefore, the *tail* transistor of this circuit is controlled by an enable signal, synchronous with the switch state. This signal is generated by a CMOS NOR based *SR latch*. *Set* and *Reset* inputs of this latch are controlled with the same signals as *On* and *Off* inputs of the flip-flop level shifter. Additionally, an output buffer stage was connected to the output of the bump circuit, consisting of two CMOS inverters for additional signal conditioning, in terms of sharper edges and more stable output voltage level.

On event decision

Analysis of the optimal time for *On* event generation is far more complex than it is for *Off* event. In order to simplify this analysis we will assume that the diodes are ideal. The purpose of this analysis is to evaluate the trade-off between the switching period and amount of energy harvested for every switching event. Amount of energy harvested for every switch closing action is directly related to the maximum inductor current, as per equation (3.12). If we single out the amplitude of the current, and write $v_L(0)$ as a function of v_{res} and v_{store}:

$$I_{L,max} = \sqrt{\frac{C_{series}}{L}}(v_{store}(0) - v_{res}(0)) \tag{3.13}$$

We can see that the current of the inductor is directly proportional to the initial voltage difference between the reservoir and storage capacitances. In other words, if we wait more vibration cycles before turning on the switch, voltage difference between these two capacitors will be higher, hence more energy will be harvested per one switching action. However, due to saturation of voltage on C_{store}, if the optimal number of full vibration cycles is exceeded, harvested power will not be optimal. In other words the optimization relates to average harvested power:

$$P_{harvested} = \frac{W_{harvested}}{\Delta t} \tag{3.14}$$

Averaging period can be expressed as $\Delta t = 2nT$, where T is vibration cycle period and n number of full vibration cycles. We need to express the harvested power in terms of optimization variables, i.e. voltage $V_{store} = V_1$ at the optimal switching time $t = t_1$, and initial voltage $V_{res}(0) = V_{store}(0) = V_0$. At the beginning of charge pump operation, energy stored in these two capacitors can be expressed as

$$W_0 = \frac{1}{2}(C_{res} + C_{store})V_0^2 \tag{3.15}$$

Energy at $t = t_1$ is:

$$W_1 = \frac{1}{2}\left(C_{res}\, V_{res1}^2 + C_{store}\, V_1^2\right) \tag{3.16}$$

Voltage $V_{res}(t_1) = V_{res1}$ can be found from the charge conservation, and it law amounts to:

$$V_{res1} = \left(1 + \frac{C_{store}}{C_{res}}\right) V_0 - \frac{C_{store}}{C_{res}} V_1 \tag{3.17}$$

Combining these equations we obtain the expression for harvested energy:

$$W_{harvested} = \frac{1}{2} C_{store} \left(1 + \frac{C_{store}}{C_{res}}\right) (V_1 - V_{res1})^2 \tag{3.18}$$

Adapting equation (8) from [42] for our, double-charge pump, topology, we can also express n as a function of these voltages:

$$n = \frac{1}{2} \log_{\frac{C_{store}}{C_{store}+C_{res}}} \frac{V_1/V_0 - C_{max}/C_{min}}{1 - C_{max}/C_{min}} \tag{3.19}$$

Substituting (3.18) and (3.19) into (3.14), and using notation $\theta = V_1/V_0$, $a = C_{max}/C_{min}$ and $K = const.$ includes remaining values, we obtain:

$$P_{harvested} = K \frac{(1-\theta)^2}{\ln \frac{\theta - a}{1-a}} \tag{3.20}$$

The optimization variable for harvested power is θ, since the remaining terms are parameters, which are fixed for a given transducer. Differentiating (3.20) with respect to θ and equating to zero we obtain a transcendental equation:

$$\frac{\theta - 1}{\theta - a} = 2\, ln \frac{\theta - a}{1 - a} \tag{3.21}$$

Substituting the value for a, and using the *Newton-Raphson* method to solve for θ we obtain:

$$\theta_{opt} = 2.445 \tag{3.22}$$

Diode-connected MOSFETs as voltage divider

Previous analysis determined the optimal time for switch closing, in terms of V_{store}/V_{res} voltage ratio. Since another bump circuit is used to generate *On* event, a scaled down, by a factor of θ_{opt}, V_store is compared to V_{res}. For the purpose of scaling down the voltage, a diode-connected PMOS voltage divider is used. It consists of series diode-connected PMOS transistors, and the output voltage depends on the position of the output node. Voltage divider is also used for scaling down the inductor voltage.

Final circuit at this design stage is presented in Figure 3-9. Operating principle can be described briefly in a few steps: Charge pumping action from C_{res} to C_{store} through $C_{var1/2}$ will occur normally, as with the regular double-charge pump circuit. Consequently, V_{store} will increase over time, and once it reaches the value of $V_{store} = \theta_{opt} \cdot V_{res}$, *Bump Circuit* 2 will generate the *On* signal, which in turn closes the switch

through *Flip-Flop Level Shifter*, and enables *Bump Circuit* 1 through *SR latch*. The harvesting phase occurs as previously described in section 3.4. Once the inductor is fully energized, its voltage becomes zero and *Bump Circuit* 2 generates *Off* signal, which turns off the switch through the level shifter, and resets *SR latch*, which in turn disables *Bump Circuit* 2. Subsequently, another charge pumping cycle begins, and thus, fully automated circuit operation is achieved.

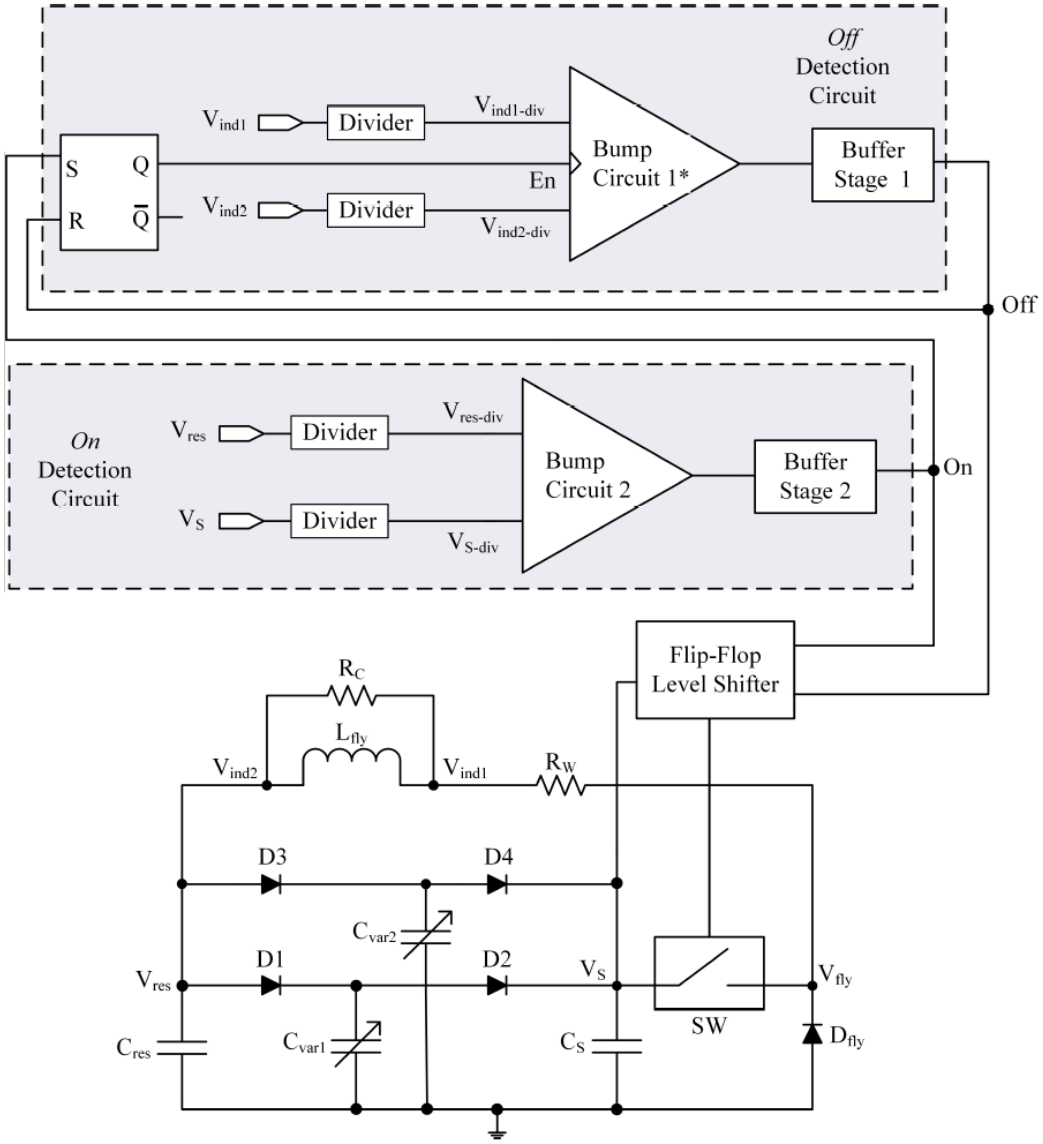


Figure 3-9: *Interface circuit with integrated switch-control* [36]

3.6 Self-sustaining topology considerations

Circuit seen in Figure 3-9, even though fully automated, is not self-sustaining for the given transducer parameters, and at this stage, it cannot be, since the circuit for switch control consumes more power than it is generated and stored in the reservoir capacitance. The functionality of the circuit was tested and verified, with external power supplies for the control circuit. If these individual components were to be supplied from the voltage provided by the reservoir capacitance, they would deplete the capacitor quickly, rendering the circuit inactive. Initially, components such as buffers, *SR latch* and bump circuits were not optimized (i.e. they were introduced in the circuit with default values for transistor sizes), hence the circuit was examined thoroughly to determine the components that need to be optimized, determine their optimal parameters and look for improvements possibilities. Even though the extensive theoretical analysis was performed to determine optimal values of individual optimization variables, these values only serve as a good starting point in the iterative optimization process. This iterative process of simulations, parameter variations and comparison, is a rather complex and time consuming task, since many optimization variables are contrary to one another. Additional difficulty is that the effect of some of the optimization variables can be seen only in the medium-term operation (e.g. $1s$), and such simulation take hours to complete.

Initial goal was to decrease the current through every current path (e.g. buffers, *SR latch* etc.) as much as possible without compromising the functionality of the circuit, in terms of introducing significant delays. If the current is decreased too much, even though the consumed power is reduced, the bandwidth of that component is significantly reduced as well which introduces significant delay, and for time-sensitive events, such as *Off* event, it may result in a non-optimal harvesting.

3.6.1 Bump-circuit clocking

A major item of interest for optimization is the bump circuit, since it has the highest power consumption in the circuit, due to the large current it draws from the source for the given transistor sizes. In fact, non optimized switch control circuit, excluding bump circuits, could be sustained from the energy stored in C_{res}, with the system still performing as a harvester, although with very low efficiency. So majority of the focus of the following sections is dedicated to power reduction of the bump circuit. Note that *Bump Circuit* 1, even though power hungry, is only turned on with a very

low duty cycle, making its medium-term power consumption not as relevant as the one of *Bump Circuit* 2. The fact is that *Bump Circuit* 2 should continuously monitor for the *On* event trigger, making it the bottleneck of this system. Power consumption of the standalone, non optimized bump circuit is in the range of tens of μW.

Power consumption of the bump circuit can be drastically decreased by using a clock signal with a low duty cycle for periodical monitoring of the inductor voltage. As a proof-of-concept, simulation results of the harvesting systems, using an external clock generator to controll *Bump Circuit 2*, is presented in Figure 3-10. Clock period and pulse width are $50Hz$ and $0.5\mu s$, respectively. Presented waveforms are for V_{res}, $V_{res,div}$ and $V_{store,div}$ as differential input of the *Bump Circuit* 2, and signal S as the bump circuit output.

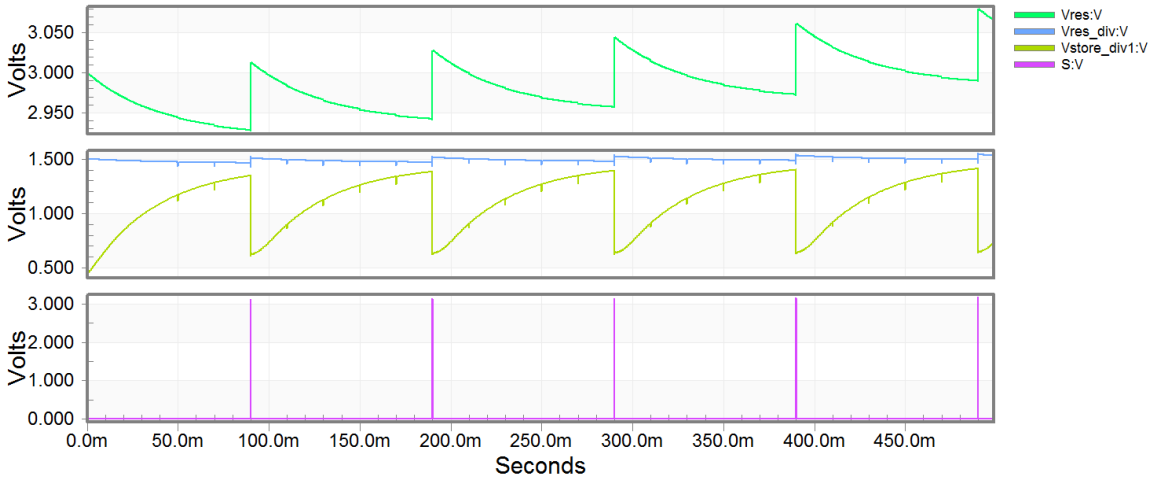


Figure 3-10: *Circuit operation with clocked "Bump Circuit 2"*

In this configuration, harvested power, accumulated on C_{res}, estimated according to (3.14) amounts to $P_{harv,res} = 5.6nW$, compared to the circuit with external switch control (3.7). In other words, by employing a clocking signal for bump circuit control, average power consumption of the entire switch control circuit has been reduced to $P_{switch-control} = 2.69nW$ (note that the harvested power was negative before clock signal implementation)

Pulse width, during witch the circuit is operating, is limited by the time needed for the circuit to generate a stable output to turn on the switch. In other words, it is determined by the propagation delay through the buffer at the output and reaction time of the level shifter or the *SR latch* controlling the second bump circuit. These delays are contrasted with the current reduction of individual elements, as mentioned before.

Clock period, on the other hand, is tightly connected to the sensitivity of the bump circuit, i.e. the differential input range for which the circuit responds with an active output, as they both define the trade-off between the frequency of the harvesting cycle and amount of energy harvested per one cycle.

3.6.2 Low-power clock signal generator - literature review

In order to avoid using an LC or crystal quartz oscillators, which are not entirely suitable for this application due to their intended frequency range, bulkiness or power consumption, design of an on-chip CMOS oscillator was one of the primary goals of the project. As shown in the previous section, the clock signal needs to be low-frequency, and in order to make this a fully autonomous circuit, it needs to be very low power to be supplied from the energy available from C_{res}. Many different topologies were investigated, however very few of them had potential to fit the requirements of this circuit. An extensive literature review was conducted in order to find a suitable topology, yielding very few results, since this is a rather peculiar set of requirements for a clock generator, e.g. invariable w.r.t. supply voltage, low-frequency, ultra low power, very low duty cycle etc. Typically CMOS oscillators are used in high frequency applications, such as circuits involving switched capacitors [49], VCOs [50, 51].

Typically CMOS clock generators are based on ring oscillator involving CMOS inverters, and though they do come in low-power and adjustable duty cycle topologies (such as ones presented in [52, 53, 54]) they do not fulfill one or more requirements for this circuit, due to their rather complex structures and design inflexibility.

Finally, two different topologies have shown promise to be used in this project, since their power can be reduced with careful design methods, and MOSFET operation in subthreshold region. A ring oscillator topology, based on OTA-C (Operation Transconductance Amplifier-Capacitor) [55]. However, to achieve very low frequency would require either a high number of OTAs or unreasonably large devices which would introduce a necessary delay between a small number of stages. On the other hand, a relaxation oscillator based topology seem to offer the best compromise between complexity, power consumption and accuracy. A design proposal presented by Denier et. al. [56] proved the capability of this topology to operate in a nano-watt range, and thus provided a good starting point for the design of this component.

3.7 CMOS Relaxation oscillator

A relaxation oscillator topology is presented in Figure 3-11. It consists of a voltage reference generator (transistors M_1, M_2), a voltage comparator (transistors M_3, M_4), a charge-discharge capacitor and referent current sources which define the period of the oscillator. Output stage acts as a pulse generator, and along with $M_{discharge}$ defines the pulse width. As mentioned previously, this topology offers many advantages, some of which are relative simplicity in terms of number of current paths and adjustable pulse width.

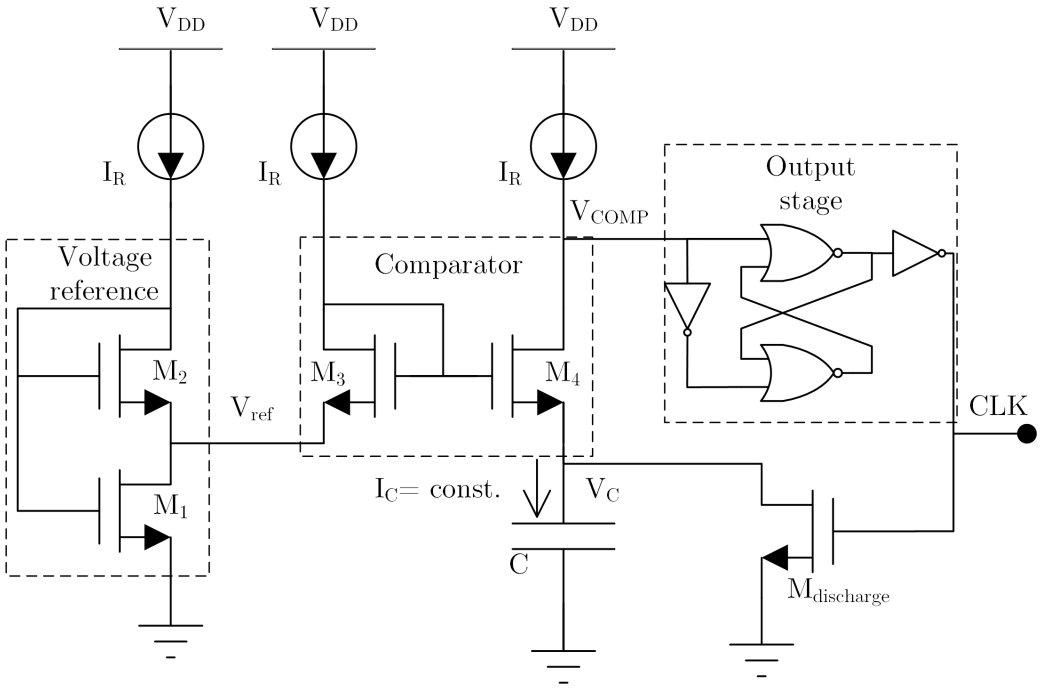


Figure 3-11: *Schematic of a relaxation oscillator*

If we assume that that C is initially discharged, and it is being charged by a constant current I_R, its voltage will linearly increase, as per capacitor voltage-current relation expressed for a constant current scenario:

$$V_C(t) = V(0) + \frac{t}{C} I_R = \frac{t}{C} I_R \tag{3.23}$$

This linearly increasing voltage is being compared with a referent voltage generated by the SCM (Self-Cascode MOSFET) structure, also well known by its property of generating a PTAT (proportional to absolute temperature) voltage reference. Output voltage of this structure, assuming sub-threshold operation of both transistors [57],

can be expressed as:

$$V_{REF} = \phi_t \cdot \ln\left(2\frac{(W/L)_2}{(W/L)_1}\right) \tag{3.24}$$

Once V_C slightly surpasses the value set by V_{REF}, comparator is thrown out of balance, causing its output voltage V_{COMP} to rise. At this point there is digital block output stage which generates the clock pulse, and in turn activates $M_{discharge}$, a transistor which, once activated, fully discharges the capacitor, resulting in a saw-tooth signal. Approximated period of the saw-tooth, and thus the clock pulse is estimated as:

$$T_{CLK} = \frac{C\,V_{REF}}{I_R} \tag{3.25}$$

Table 3.4 indicates relevant design variables of the designed circuit.

Table 3.4: Important circuit parameters

Element	(W/L)/Value
M_1	$4\mu m/28\mu m$
M_1	$4\mu m/4\mu m$
M_3, M_4	$1\mu m/1\mu m$
$M_{discharge}$	$20\mu m/0.35\mu m$
I_R	$100pA$
C	$29.15pF$

Estimated power consumption of the relaxation oscillator is can be expressed with two terms:

$$P_{osc} = P_{static} + P_{dynamic} \tag{3.26}$$

where $P_{static} = V_{supply}\,(3 \cdot I_R)$ is the static power consumption, and based on the value of reference current, it can be very low (a few multiples of $100pW$). Dynamic power a CMOS digital gate can be expressed as: $P_{dynamic,1} = f_{CLK} \cdot C_{LOAD} \cdot V_{DD}$, and the total dynamic power as the sum of power dissipation for two inverters and two NOR gates. Seeing as the switching activity of the digital part of the circuit is relatively low (aimed value is $50Hz$) it is obvious that this circuit will be low-power.

Simulation results

Figure 3-12 shows relevant waveforms for the simulated design, with $V_{DD} = 1V, I_R = 100pA$. As expected, once V_C slightly surpasses the referent voltage, V_{COMP} starts exponentially rising, until it triggers the output circuit. Output circuit generates a short pulse $t_{pulse} = 593ns$, which represents the clock signal. Simulated power consumption for this circuit is $P_{CLK} = 0.368nW$, of which $0.3nW$ is due to constant

currents, and the remainder due to dynamic power consumption of the output block.

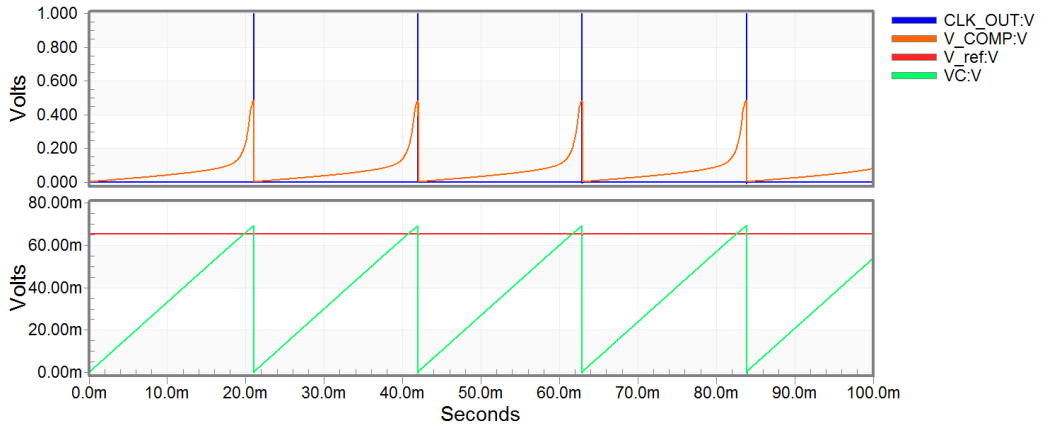


Figure 3-12: *Simulated waveforms illustrating operation of the circuit*

In the initial design, output circuit comprised a chain of inverters, but this proved to be an ineffective solution for two reasons. Namely, the input signal for the digital gates has a gentle slope, and it would "slowly" trigger the inverters, making the delay, and thus the pulse width, a lot higher than intended. Additionally, it creates a longer lasting conduction in the first few inverters, thus increasing the power consumption. Conversely, when a *D-latch* was implemented (as seen in Figure 3-11), once the input signal triggers the first inverter, the feedback of the *NOR* gates latches the value much faster, thus cutting off the current of the subsequent gates.

An obvious drawback of the circuit is that it requires a reliable current reference, since the clock period is inversely proportional to the current I_R. Even though an additional component is required for this circuit to be fully on-chip, this topology has proven to be the most suitable for this project.

3.8 Current Reference

Overall performance of the relaxation oscillator described above, is highly dependent on the current sources used in the schematic. That includes the power consumption and robustness, i.e. sensitivity to variations in the supply voltage or temperature. For a fully autonomous on-chip design, a reliable integrated current reference is necessary. Additionally, it needs to be sufficiently low-power to be supplied from the energy stored in V_{res}. A topology known as SBCS (*Self Biased Current Reference*) utilizes MOSFET devices operated in weak and moderate inversion, and thus achieves very high efficiency. Using an adaptation of this topology, [58] reports a $2nW$ current

reference, capable of operating with very low voltages while maintaining robustness. Therefore, this current reference topology has been selected for this project.

Schematic of the circuit is presented in Figure 3-13. It comprises an SCM structure operated in moderate inversion, a voltage following current mirror, operated in weak inversion, and further current mirroring transistors, depending on application.

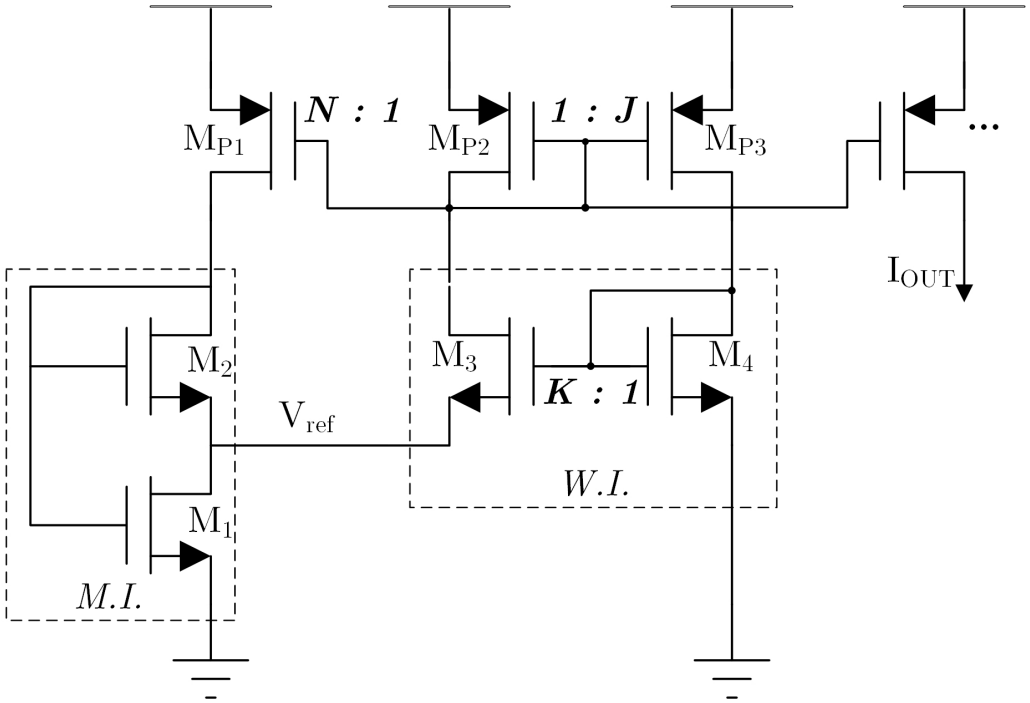


Figure 3-13: *Schematic of the proposed current reference circuit*

A considerable advantage of this circuit is the ability to operate with very low voltages. Namely, the minimal supply is constrained by one of the branches with the highest number of transistors (two branches on the left). In other words:

$$V_{DD} \geq max\left[V_{ref} + V_{DSsat_3} + V_{SG_{P2}},\, V_{GS1} + V_{SDsat_{P1}}\right] \tag{3.27}$$

Design is aiming at sub-threshold operation, so if we assume that PMOS transistors are saturated so that $V_{SDsat_P} \approx 100mV$, and have inversion coefficient close to 1 so that $V_{SG_P} \approx V_{T_P}$, that M_{N2} operates in moderate inversion so that $V_{ref} \leq 100mV$, the minimum required V_{DD} can be approximated to:

$$V_{DD} \geq max[|V_{T_P}| + 200mV,\, V_{T_N} + 100mV] \tag{3.28}$$

$$V_{DD} \geq |V_{T_P}| + 200mV \tag{3.29}$$

which for the used process technology amounts to $V_{DD,min} = 0.88V$ Another obvious

advantage of this circuit is that it is fully implementable in CMOS technology, without using external components (resistors, capcitors etc.) or their integrated counterparts which would require large chip area [59].

3.8.1 Design methodology

For analysis of the circuit, and derivation of design equations, ACM - a current-based MOSFET model will be presented first, which allows a design methodology that is more convenient for proper sizing of transistors operated in sub-threshold operation.

ACM - A Current-based MOSFET model

ACM model, as presented in [60], is based on the sub-threshold MOSFET model, and it relies on the concept of the inversion level in MOS devices. As stated by the model, drain current of a MOSFET can be split into two components - forward I_F and reverse I_R. Now the current can be expressed as:

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{3.30}$$

$$I_S = \frac{W}{L} I_{S0} = S \cdot I_{S0} \tag{3.31}$$

$$I_{S0} = \mu C_{OX} n \frac{\phi_t^2}{2} \tag{3.32}$$

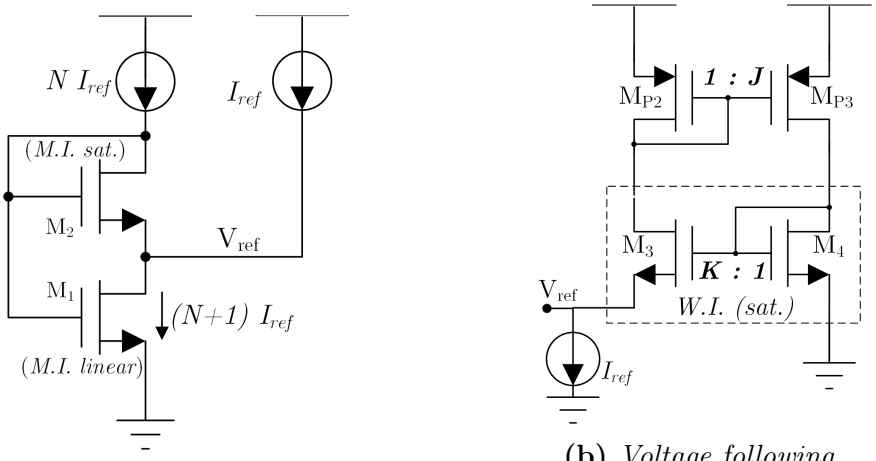
Current I_F (I_R) depends on gate-to-source (drain) voltage. For instance, in forward saturation $I_F \gg I_R$, and consequently $I_D \approx I_F = i_f \cdot I_S$. Forward (reverse) inversion coefficient, $i_f(i_r)$ represents the multiple of the technology current for a current component, and is a function of gate-source (drain) voltage. I_{S0} is also known in literature as technology (or technology-specific) current since it depends only on the process parameters: μ (carrier mobility), C_{OX} (gate oxide capacitance), n is the body (slope) factor and $\phi_t = \frac{kT}{q}$ is the thermal voltage. Voltage current relationship is now expressed as:

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{3.33}$$

with $V_P = (V_G - V_{T0})/n$ being the pinch-off voltage, and V_{T0} being the threshold voltage. Technology currents I_{S0} for *AMSH35* process is $I_{SN} \approx 70n$ for NMOS, and $I_{SP} \approx 25n$ for PMOS devices.

Design equations

Shown in Figure 3-14a is the core component of this current reference, as it has proven to be a very useful structure for building low-power and low-voltage analog blocks [61, 59].



(a) *Self-cascode MOSFET*

(b) *Voltage following current mirror*

Figure 3-14: *Main circuit components*

According to (3.30), we can express the drain currents of M_2 (saturated) and M_1 (in linear region), as:

$$I_{D2} \approx I_{F2} = i_{f2} \cdot I_{S2} \tag{3.34}$$

$$I_{D1} = I_{F1} - I_{R1} = I_{S1}(i_{f1} - i_{r1}) = (N+1)I_{ref} \tag{3.35}$$

On the other hand, we have that $V_{P1} = V_{P2}$, since their gate terminals are at the same potential, and that $V_{D1} = V_{S2}$, which reflects to $i_{r1} = i_{f2}$. Combining (3.34) and (3.35), we can derive the following relation:

$$i_{f1} = i_{f2}\left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right] \tag{3.36}$$

By applying (3.33) to node V_{ref} for the source of M_2 and drain of M_1 we can express their VI relations as:

$$\frac{V_P - V_{ref}}{\phi_t} + 1 = \left(\sqrt{1 + i_{f2}} - 1\right) + \ln\left(\sqrt{1 + i_{f2}} - 1\right) \tag{3.37}$$

$$\frac{V_P}{\phi_t} + 1 = \left(\sqrt{1 + i_{f1}} - 1\right) + \ln\left(\sqrt{1 + i_{f1}} - 1\right) \tag{3.38}$$

Expressions (3.36)–(3.38) are the primary design equations for this circuit, with three

unknowns V_P, i_{f1}, i_{f2}. Assuming that a voltage reference sets V_{ref} to a given value, and a current mirror defines the ratio N, then the inversion coefficients, and therefore the currents of M_1, M_2, are easily determined.

On another note, structure shown in Figure 3-14b is used to define the referent voltage V_{ref}. Noting that $V_{ref} = V_{S3}$, $V_{P3} = V_{P4}$, $I_{D3} = I_{D4}/J$ (current mirror M_{P2}-M_{P3}), and assuming weak inversion saturation of M_3 and M_4, and applying (3.33) to express the referent voltage as:

$$V_{ref} = \phi_t \ln(JK) \tag{3.39}$$

where $J = S_{P3}/S_{P2}$ an $K = S_3/S_2$. As shown in (3.39), the referent voltage is relatively independent of supply and process parameters variations as long as transistors operate in weak inversions.

Referent current sensitivity

To evaluate the relative change of current as a function of change in the referent voltage, we will assume $N = 1$, and a variation of V_{ref} equal to δV_{ref}. From previous equations we can derive an expression which gives the relative sensitivity of the referent current to V_{ref}:

$$\frac{\delta i_{ref}/i_{ref}}{\delta V_{ref}} = \frac{2}{\phi_t \left[\sqrt{1+i_{f1}} - \sqrt{1+\frac{i_{f1}}{\left(1+2\frac{S_2}{S_1}\right)}}\right]} \tag{3.40}$$

Relative sensitivity to V_{ref} has been plotted in MATLAB for three different S_2/S_1 ratios, as shown in Figure 3-15.

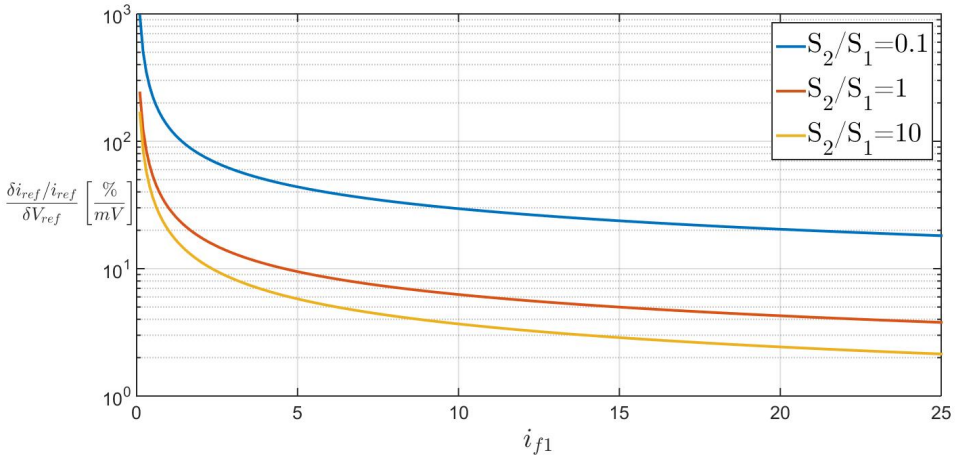


Figure 3-15: *Relative sensitivity of the referent current vs.* i_{f1}

It can be seen that the current sensitivity is very high for low inversion levels of M_1. It has been reported that the current variation with respect to V_{DD} is inversely proportional to the factor given in square brackets in (3.40) [58], so in order to minimize it M_2 should not be operated in very low inversion levels.

By setting M_2 to operate in moderate inversion with e.g. $i_{f2} = 3$, from (3.34) we get $V_P = V_{ref}$. Combining (3.37) and (3.38), we can acquire the desired value for i_{f1}, for a given $J \cdot K$ product from a transcendental equation:

$$\sqrt{i_{f1}+1} = 2 + \ln\left(\frac{J \cdot K}{\sqrt{i_{f1}+1}-1}\right) \tag{3.41}$$

Having calculated V_{ref} and i_{f1}, from (3.36) we can find the ratio:

$$\frac{S_2}{S_1} = \frac{i_{f1} - i_{f2}}{i_{f2}\left(1+\frac{1}{N}\right)} \tag{3.42}$$

Since i_{f2} was already chosen, we can find S_2 from (3.34) by substituting the desired value of the referent current:

$$S_2 = \frac{N \cdot I_{ref}}{i_{f2} \cdot I_{S0}} \tag{3.43}$$

Desired mode of operation for M_3 and M_4 is weak inversion, and for $J \cdot I_{ref} \ll I_{SN}$, $S_9 = J$ will keep these transistors saturated. The last consideration is the inversion coefficient for PMOS transistors M_{P1}–M_{P3}, which is chosen to be close 0.1 in order to keep them in weak inversion.

Empirically obtained values $N = J = 1$ and $K = 9$ were adopted as design variables, and the transistors are sized in accordance to the design equations. Beside these values, referent current is aimed to be $200pA$ to minimize the power consumption while maintaining relatively low sensitivity to variations. Summary of the transistor geometries is presented in the Table 3.5.

Table 3.5: Transistor sizes for SBCS circuit

Device	i_f	$W[\mu m]$	$L[\mu m]$	S
M_1	10.19	0.4	504	1/1260
M_2	3	0.4	420	1/1050
M_3	3×10^{-4}	90	10	9
M_4	2.5×10^{-3}	10	10	1
M_{P1-3}	0.1	1	12.5	2/25

Simulation results

Using the results presented in the previous section, the design was simulated using standard $0.35\mu m$ CMOS process from AMS. Simulation results for sweeping of supply voltage can be seen in Figure 3-16.

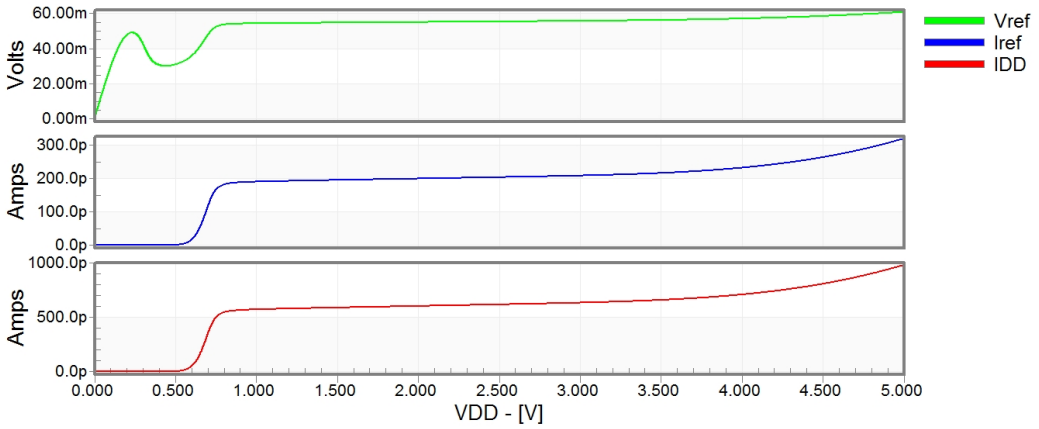


Figure 3-16: *Simulation results for V_{DD} sweep* $[0, 5]V$

Presented waveforms illustrate the behavior of the referent voltage, referent current and total current drawn from the supply, for V_{DD} variation $0V$–$5V$. A few conclusions can be made:

i) Simulation reports $V_{DD,min} = 850mV$, which verifies the estimation previously made $(880mV)$;

ii) The chosen design method is highly accurate. Calculated parameters produce the intended current within $10pA$ deviation;

iii) Referent voltage is justly referred to as PTAT voltage, since its variation is relatively small for the swept V_{DD} range. Relative current variation is $6.2\%/mV$ for the change in V_{ref};

iv) Relative current variation is only $4.79\%/V$ for V_{DD} range $[0.9, 3.5]V$**;

v) Temperature dependence has been simulated, and illustrated in Figure 3-17;

vi) Ultra-low power was achieved, as demonstrated with the total current consumption, which varies between $564pA$ and $632pA$ for the $[0.9, 3.5]V$ range of V_{DD}. In other words power consumption is $[0.51, 1.89]nW$ for the same V_{DD} range.

***Note* The upper limit of the V_{DD} range for which the variation has been measured has been chosen intentionally below the maximum swept voltage. The reason is the

maximum recommended supply voltage for standard CMOS process is $3.5V$, even though the maximum voltage that thin oxide devices can withstand is $5V$.

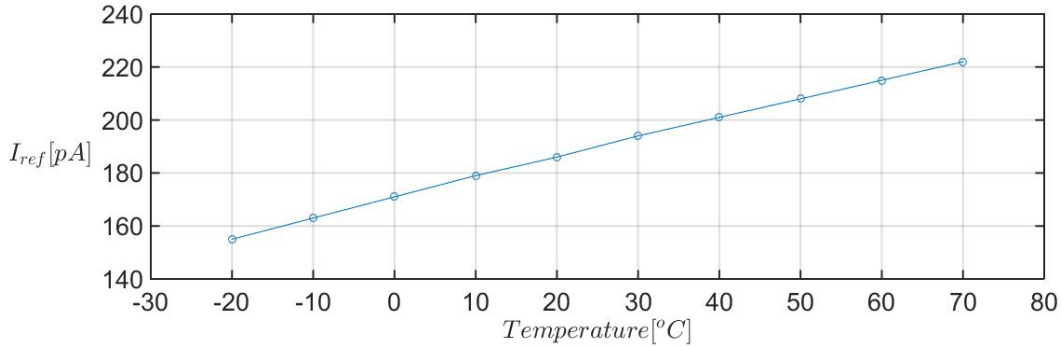


Figure 3-17: *Plotted I_{ref} vs. Temperature*

An obvious drawback of this circuit is that it requires a large on-chip surface, due to the sizes of devices. According to Montoro et. al. [62], the use of trapezoidal transistors with the same equivalent length, can significantly reduce the physical transistor length. However, it is uncertain if these transistors are available in the AMS process technology.

Achieved results are summarized in Table 3.6. It can be noticed that this design

Table 3.6: Summary of simulation results

Parameter	Value	Unit
I_{ref} sensitivity to V_{DD}	4.79	$\%/V$
I_{ref} sensitivity to T	0.39	$\%/^oC$
V_{ref} sensitivity to V_{DD}	1.31	$\%/V$
V_{ref} sensitivity to T	0.35	$\%/^oC$
Power (at $0.9V$)	0.51	nW
Power (at $3.5V$)	1.89	nW
$V_{DD.min}$	0.85	V

has significantly lower power consumption minimum supply voltage compared to [58], due to fewer current paths used, and lower reference current. The ability to generate lower reference current with higher precision, and dimensions in the same rage, comes from the benefits of using newer process technology with better parameters and smaller minimum feature.

Upon implementing the designed current reference in the clock signal generator, instead of the ideal current sources, by mirroring the referent current with $2:1$ ratio, power consumption, according to simulations is $P_{CLK,tot} = 0.924nW$, tested for $V_{DD} = 1V$ and $1s$ simulation time. Constant power consumption of the circuit, contributed

to the three conduction paths of the current reference and three conduction paths of the relaxation oscillator is $P_{const} = 0.858nW$, whereas the remaining power dissipation is attributed to the digital output stage dynamic power consumption.

3.9 Considerations for mid-term operation

After designing and verifying both standalone and coupled operation, of the clock signal and the current reference generator, they were implemented in the top-level circuit (Figure 3-9). They are supplied directly from the harvesters storage element (unregulated V_{res}), and the output (CLK signal) was connected to the tail transistor of the *Bump Circuit* 2. That way, the bump circuit is turned on periodically with a $T_{CLK}S$ and pulse width τ_{PW}. This should, theoretically decrease the relatively large power consumption of the bump circuit by a factor of $D = \frac{\tau_{PW}}{T_{PER}}$. For the designed clock generator, this represents the duty cycle, and amounts to $D = 2.75 \times 10^{-5}$.

For functional verification of this design, a mid-term operation was simulated, and the operations is illustrated in Figure 3-18.

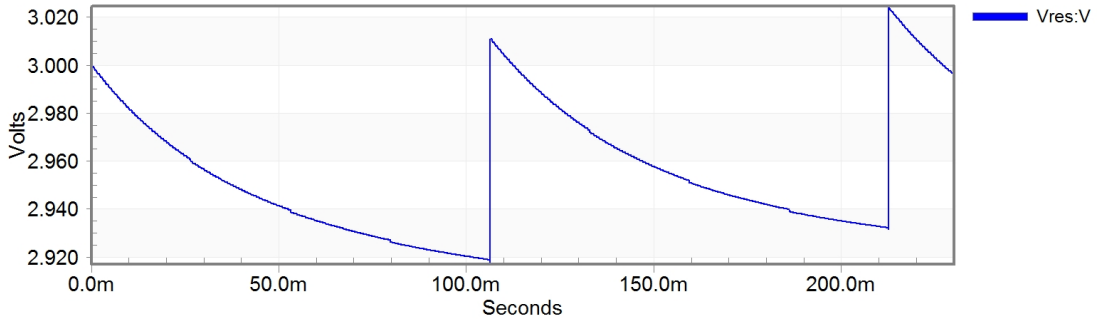


Figure 3-18: *V_{res} waveform after clock signal implementation*

Note that the clock signal period is changed to $\approx 25ms$, instead of the originally intended $20ms$. It was found as a more optimal value in the trade-off between the clock period and bump circuit selectivity. This causes the harvesting cycle to be initiated with a lower frequency, but in contrast, more energy is harvested per one cycle.

Waveform is shown for only two harvesting cycles, so it can be clearly seen, from the increase in V_{res} that additional energy is being collected and stored in C_{res}, thus proving the **fully autonomous** operation of the interface circuit (including switch

control). Average harvested power on V_{res}, estimated according to (3.14) is now:

$$P_{harv,res} = \frac{\Delta W_{res}}{\Delta t} = \frac{\frac{1}{2}C_{res}\left(V_{res}^2(t_{sim}) - V_{startup}^2\right)}{t_{sim}} = 3.61nW \tag{3.44}$$

It can be noticed that the harvested power is considerably lower. Bump circuit is turned on periodically, and this can be seen in the simulated waveform as a sudden decrease in V_{res}. The decrease is not large, due to the very short pulse, and overall the harvested power is positive.

3.10 Discussion

Design presented in Section 3.5 formed a basis of this project. As it was thoroughly explained in the same section, design comprised a synchronous (automated) switch control circuit, but it was not fully autonomous (self-sustaining) due to large power consumption of individual components of the switch control circuit. In other words, if the switch control circuit was supplied from the harvesters storage element, the system would shortly dissipate all the energy stored in C_{res}, thus it would not operate as an energy harvester. To conserve the energy harvesting property of the system, two actions can be taken: *i)* Increasing the harvesting capability of the transducer: This can be achieved by increasing the capacitance variation, as explained in previous chapter. This however, is not within the scope of this thesis; *ii)* Increasing the efficiency of the interface circuit: efficiency of the interface circuit has been maximized for the given transducer properties, which leaves only the optimization of the control circuit, in terms of reducing the overall power consumption of the switch control circuit.

Presented designs accomplish exactly that, and after their implementation in the complete interface circuit, autonomous operation was achieved, followed by a decrease in harvested power of $2.33nW$.

Many attempts were made to further optimize the net power gained in the harvesting system, during the short-to-medium term operation. This simulation time was focused on, because simulations require very small time steps, in order to facilitate convergence of the solutions of the clock signal generator.

However, the main topic of this discussion are the consequences of the design choices, and oversights made during the system planning phase. Namely, what previous work did not account for, and was inherently adopted in this project, was the effect of the long-term operation on the performance and stability of the system. Two

major oversights have been recognized during the late phases of this project, and they both relate to unregulated voltage supply for low-voltage blocks.

First, all the blocks, save for *Flip-Flop Level Shifter*, were designed using low-voltage (standard) thin-oxide CMOS devices, which are intended for $3.3V$ power supply/gate voltage. Of course, these components have higher tolerance, but from the perspective of long-term operation, V_{res} is intended to rise over time to a significantly higher value, which would compromise the reliability of the circuit. One way to solve this problem would be to use high-voltage CMOS devices, which would require additional analysis, due to different characteristics of the devices.

Second point relates to unregulated voltage supply in terms of circuit functionality. Even when considering the long-term operation where the supply voltage V_{res} has not increased sufficiently to damage the devices, some major functionality issues have been noticed after only $\sim 2s$ of simulated time. To illustrate this, Figure 3-19 is presented, which illustrates how the slight increase in the unregulated supply voltage affects the operation of the circuit, and even renders the circuit ineffective. Note that some changes were made to obtain this figure for lower simulation time, and that this malfunction normally happens after $3s$.

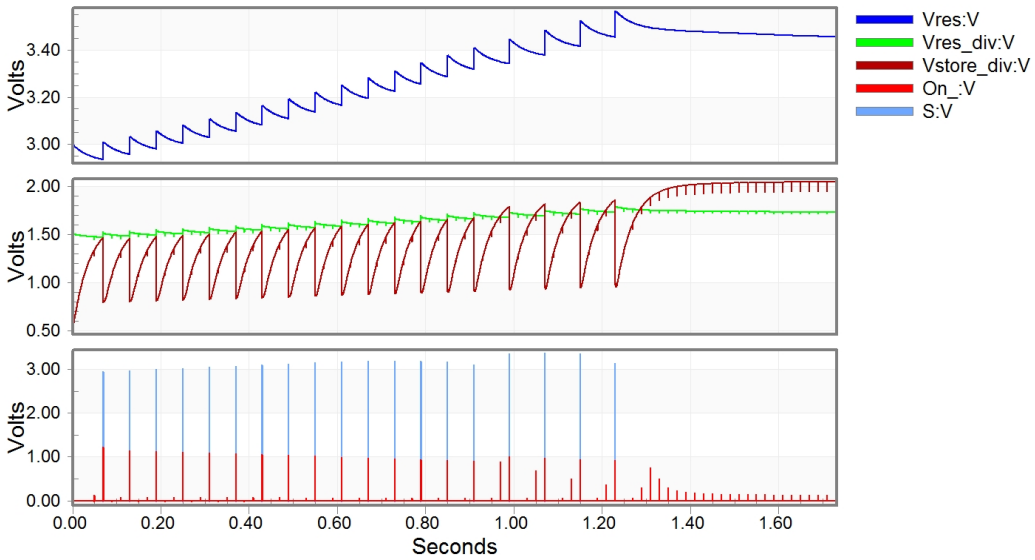


Figure 3-19: *Circuit malfunction during long-term operation*

As shown in the figure, the circuit operates as expected until V_{res} reaches a certain value, V_{max} at $t \approx 1.22s$. Subsequently, the harvesting phase does not start, voltage on C_store saturates, and the circuit continuously dissipates the energy stored in V_{res}. After troubleshooting the circuit operation, the reason was found to be the bump circuit responsible for initiating the harvesting phase by turning on the switch. As

previously explained, the circuit is namely a transconductance circuit in its original form, converting the differential voltage into the output current. In order to have a voltage output, a transistor with a "constant" bias voltage has been added, and the output collected from its drain. However, the "constant" voltage is obtained from a voltage divider that fractions V_{res}. As it was established, V_{res} increases over time, and so do its fractions. This is reflected in a "stronger" bias of the output transistor, i.e. larger V_{GS}. Knowing that the transistor is supplied by a relatively constant current, determined by the bump circuit, higher V_{GS} moves the transistor out of saturation into triode region, consequently with lower V_{DS}, which is in fact the output voltage. Therefore, the bump circuit output voltage decreases over time. (*)

On another note, a signal conditioning buffer connected to the output node of previously discussed bump circuit, is also supplied from unregulated V_{res}. Knowing the Input-Output characteristic of an inverter, inverter threshold voltage is determined by transistor geometry and the supply voltage. Since the geometry is constant, relative threshold voltage will not change, but due to the variation of the supply, the absolute threshold increases linearly with V_{DD}. (**)

From (*) and (**) it is obvious that at some point the output voltage will not be enough to overcome the threshold of the inverter, and consequently will not initiate the harvesting phase. Therefore, the circuit will start to dissipate power, and in turn decrease V_{res}, but this does not allow the circuit to continue its normal operation once V_{res} decreases sufficiently. Conversely, it will dissipate power until C_{res} is completely discharged. This is the case due to high selectivity of the bump circuit. Namely, bump circuit inputs are fractions of C_{res} and C_{store} voltages, $V_{res,div}$ and $V_{store,div}$. Once $V_{store,div}$ reaches the value of $V_{res,div}$, and the clock signal enables it, the output generates a short pulse, which initiates the harvesting phase. When the harvesting phase is not initiated, C_{store} has no way of transferring its charge to C_{res}, which means that V_{res} continues to grow towards $V_{store,sat}$. On the other hand, V_{res} decreases continuously, and at some point (V_{min}) bump circuit can provide a valid output, but at this point $V_{store,div}$ is higher than $V_{res,div}$, and the comparative property of the bump circuit defines no output pulse. Thus the circuit is "stuck" and cannot operate properly.

Some possible solutions were investigated, but all of them have their drawbacks:

i) Bump circuit selectivity reduction: it would fix the problem, but make the circuit extremely inefficient, for two reasons. First, it would mean intentionally changing the optimal moment for the harvesting phase, thus reducing the energy harvested in a single cycle. Second, once the V_{res} starts to decrease from V_{max},

at a sufficiently lower level, it will enable harvesting again, and this will happen indefinitely. In other words, the circuit would have a zero long-term harvested power, since V_{res} would vary between V_{min} and V_{max}

ii) Inverter threshold shift: since the inverter geometry defines a relative threshold voltage, this solution only prolongs the inevitable. This was verified through simulations, by increasing $\frac{(W/L)_N}{(W/L)_P}$ in the first inverter, normal circuit operation was maintained for additional 1s. This is also the case with the output transisor of the bump circuit, however it would require a more significant change in geometry compared to the inverter.

iii) Voltage regulation. Voltage regulation is the most promising solution, and it will be investigated further in the following subsection.

iv) Finally, if we assume additional components in the system, such as sensor and transceiver, which would also occasionally consume power, keeping V_{res} within operation limits, the system can be considered *quasi-stable*

3.10.1 Voltage regulator

In order to verify the solution using a regulated voltage supply, a basic CMOS voltage regulator [63] topology presented in Figure 3-20 was designed and simulated.

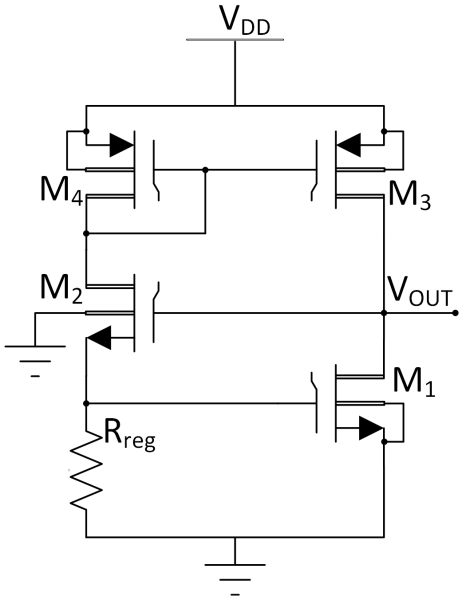


Figure 3-20: *Voltage regulator schematic*

High-voltage transistors were used, since they provide a significantly steadier response for large changes in the supply voltage, and a reliable operation for large voltages. Regulated voltage is expressed as:

$$V_{out} = V_{GS1} + V_{GS2} \tag{3.45}$$

This structure exhibits self-compensation, i.e. when I_{D1} is increased due to V_{DD} variation, V_{GS1} increases with $\sqrt{V_{DD}}$, causing the increase in V_{DS2}, which in turn decreases V_{GS2}, keeping the output voltage constant.

To illustrate the very low slope that the regulator produces at its output, and the regulated voltage levels for different values of the current limiting resistor, Figure 3-21 is presented below.

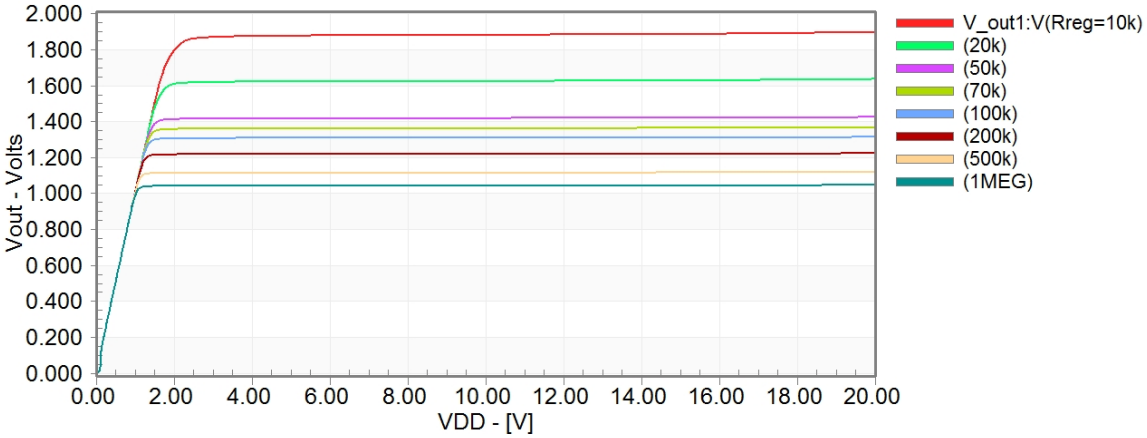
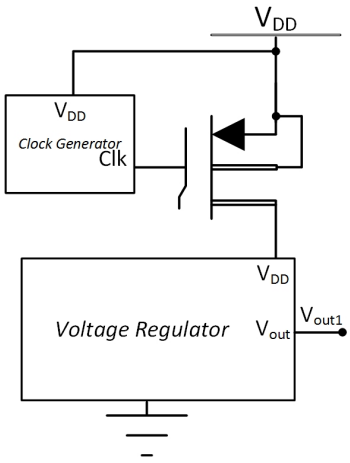


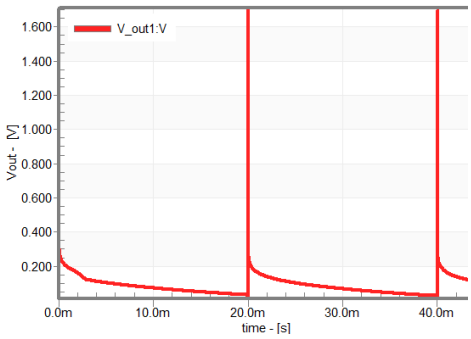
Figure 3-21: *Regulated voltage for different values of* R_{REG}

Voltage regulator clocking

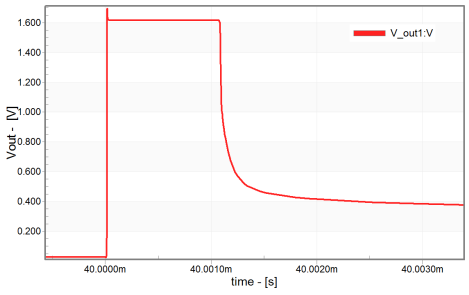
Ultra low-power voltage regulators are scarce in integrated CMOS circuits. No suitable topology was found to be sustainable. Even the presented voltage regulator is very power consuming, and it cannot be constantly supplied from the reservoir capacitance. For now, voltage regulator is dedicated only for improving the bump circuit operation. Therefore, it was decided to use the clock signal to periodically turn on the regulator supplying the bump circuit, instead of clocking the bump circuit directly. Clocking technique is illustrated in Figure 3-22a, and simulated waveforms for regulated output are presented in Figures 3-22b and 3-22c (magnified short pulse).



(a) *Clocking technique*



(b) *Waveform of the clocked regulated output*



(c) *Magnified short pulse of the regulated voltage*

Figure 3-22: *Clocked voltage regulator loaded with the bump circuit*

3.10.2 Power consumption considerations

Implemented voltage regulator successfully fixes the problem of variable supply and bias for the bump circuit. However, voltage regulation needs to be investigated further, and a suitable low-power topology should be implemented for to serve as the power supply for all low-voltage blocks. This goes to ensure, long term operation of low-voltage blocks in high voltage circuit, and drastically limit the increase in power consumption. It is obvious that if the switch control circuit blocks are supplied from an increasing voltage, and assuming that the functionality will not be compromised, the power consumption will start to increase, and at some point it will equate to the harvested power. Effectively, the harvesting system will only be able to recover its own internal losses, which defies the purpose of a harvesting system with a synchronous inductive return path (this is a trait of circuit with passive feedback).

On the other hand, by using a regulated voltage supply for all the power blocks we ensure two important characteristics: *i)* The circuit will be deterministic, i.e. the

power supply will not affect the functionality in no manner; and *ii)* power consumption of the circuit will be constant, and will not increase with the increase of V_{res}. These two properties, ideally, allow indefinite long-term operation.

Chapter 4

Conclusions, improvements and future work

4.1 Chapter summaries

Chapter 1

The first chapter introduced the reader with the general concept of energy harvesting, in terms of different ambient energy sources, their capabilities, applications and usability for different scales of harvested energy. Microscale energy harvesters typically find their application in wireless sensor nodes, and consequently one section was dedicated to illustrate the purpose and requirement for WSNs. Seeing as vibration energy harvester is the central part of this thesis, VEH systems were given more attention, as opposed to the harvesters exploiting energy from other ambient energy sources. General working principle, from a mechanical perspective, was briefly introduced, as well as types of transducers and their respective advantages and drawbacks. Additionally, a brief overview of the requirements concerning the power management circuit was introduced as well.

Chapter 2

The second chapter was focused on the study of electrostatic vibration energy harvester. This includes brief theoretical analysis of more common electrostatic transducer structures, their drawbacks and advantages. Additionally, substantial amount of attention was given to the interface circuit topologies, as they have a major impact on the overall behavior and efficiency of the energy harvester. Many different topologies have been presented, explained and simulated for pure illustrative purposes. The conclusion can be drawn that an efficient energy harvesting interface circuit must

have the ability to accumulate energy, i.e. to increase the start-up voltage, in case of electrostatic transducers. Consequently, circuits with an intermediate energy storage (inductive) element are the ones of practical meaning. These include charge and voltage constrained based topologies and charge pump topologies. Voltage constrained topologies, theoretically, offer higher efficiency (up to 80% compared to 30% for charge constrained circuits). However, these circuits typically require rather complex control circuits, due to many switching elements and the requirement for their precise synchronization, which can drastically reduce their overall efficiency. It is for that reason that charge-pump topologies are of the highest interest for this project, since they have the property of self-switching for the charge pumping phases of operation (due to diodes). They require only one switch, for the flyback return path, which is controlled as a function of a voltage, instead as a function of the variable capacitance, which is the case of voltage and charge constrained circuit. Consequently, the switch-control circuit is far less complex. Double charge pump interface circuit was used, due to transducer's innate property of having dual, anti-phase variable capacitance.

Chapter 3

The third chapter introduced the problem from an electronics perspective. Starting with the used process technology brief overview, a requirement for high-voltage CMOS components was explained. Additionally, this chapter addressed the transducer modeling as a variable capacitance, and determination of numerical values which are included in the circuit simulation. Previous work was addressed to offer better understanding of the individual components involved in the switch-control circuit, and illustrate the importance of individual factors that needed to be taken into account to optimize harvested energy while keeping the circuit power consumption minimal. Added difficulty was that the capacitance variation is very small, causing the maximum harvested power to be only $8.33nW$, even with external switch control. This significantly limits the allowed power consumption of the switch-control, and further increases the difficulty of producing a self-sustaining circuit. Consequent to optimization of individual components, the most power-hungry part was the *Bump Circuit* monitoring the inductor voltage. It was determined that with periodic operation of the circuit the power consumption can be decreased drastically, even to that extent where the circuit is self-sufficient. Thus, an ultra-low power clock generator was designed, drawing only $3 \times 100pA$ constant current, and having a digital output stage which generates the pulse, and in turn defines a very low duty cycle. Low duty cycle (2.75×10^{-5}) ensures the drastic decrease in the power consumption of the bump circuit. However, the clock signal generator required a stable current

reference, which was the next design point. Using a very accurate and convenient design methodology, a $200pA$ current reference with only $\sim 1nW$ power consumption (for $V_{DD} = 1V$) was achieved, and upon implementation of these low power components in the circuit, a self-sustaining topology was accomplished, although for only short-to-mid term operation, which will be further addressed in the following section.

4.2 Improvements and future work

Due to unregulated voltage, low voltage blocks in the circuit exhibit unstable/undesirable operation with the increase in the voltage of the reservoir capacitance, V_{res}, as explained in the Discussion part of the previous chapter. This is not limited only to the bump circuit, and the subsequent buffer stage as explained previously, but all low-voltage blocks which are supplied by the V_{res}, or have some transistors biased by a fraction of it. For example, it can affect the absolute threshold level of the output logic in the clock signal generator, which in turn modifies the clock signal period and therefore compromises the optimal switching time for maximum energy harvesting. Therefore, voltage regulator is a necessity for a stable, deterministic long term operation of the low-voltage blocks, and thus the overall interface circuit. However, voltage regulators themselves are relatively power hungry circuits (relative to this application), and no topology was found to be suitable for this application. Voltage regulator presented in the previous chapter was only introduced to demonstrate the problem of the bump circuit malfunction, but it could not be used to continuously regulate the voltage for the low voltage part of the circuit, as its power consumption was too high. The regulator would have to have power consumption of a couple of nW at its maximum, which is by far the most difficult requirement for the circuit, and need further and more elaborate research.

Conversely, a possible improvement which might be interesting to investigate instead, is a different topology of a bump circuit, as a voltage sensing component, which could be possible to design for ultra low-power consumption (in order of nW), as presented in [64]. This circuit also requires requires external current sources, for which purpose the current reference designed in this work can be utilized, since the currents are in order of nA. However, the variation of the supply voltage has not been investigated for this circuit, meaning that it also presents a subject of interest for further research. This concludes the thesis.

References

[1] Adnan Harb. Energy harvesting: State-of-the-art. *Renewable Energy*, 36(10):2641–2654, 2011.

[2] A. Kansal and M. B. Srivastava. An environmental energy harvesting framework for sensor networks. In *Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on*, pages 481–486, Aug 2003.

[3] C.C. Warnick. *Hydropower engineering*. Prentice-Hall, 1984.

[4] T. Ackermann. *Wind Power in Power Systems*. Wiley, 2005.

[5] D.K. Prasad and M. Snow. *Designing with Solar Power: A Source Book for Building Integrated Photovoltaics (BiPV)*. Designing with Series. Images, 2005.

[6] T. E. Starner. Powerful change part 1: batteries and possible alternatives for the mobile market. *IEEE Pervasive Computing*, 2(4):86–88, Oct 2003.

[7] S.A. Roen. Solar powered portable calculator, April 12 1977. US Patent 4,017,725.

[8] Z. Wang, V. Leonov, P. Fiorini, and C. Van Hoof. Micromachined thermopiles for energy scavenging on human body. In *TRANSDUCERS 2007 - 2007 International Solid-State Sensors, Actuators and Microsystems Conference*, pages 911–914, June 2007.

[9] N. S. Shenck and J. A. Paradiso. Energy scavenging with shoe-mounted piezoelectrics. *IEEE Micro*, 21(3):30–42, May 2001.

[10] C. B. Williams, C. Shearwood, M. A. Harradine, P. H. Mellor, T. S. Birch, and R. B. Yates. Development of an electromagnetic micro-generator. *IEE Proceedings - Circuits, Devices and Systems*, 148(6):337–342, Dec 2001.

[11] Igor Neri, Flavio Travasso, Helios Vocca, and Luca Gammaitoni. Nonlinear noise harvesters for nanosensors. *Nano Communication Networks*, 2(4):230 – 234, 2011.

[12] A. E. Aroudi, M. López-Suarez, E. Alarcón, R. Rurali, and G. Abadal. Nonlinear dynamics in a graphene nanostructured device for energy harvesting. In *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, pages 2727–2730, May 2013.

[13] G. Despesse S. Boisseau and B. Ahmed Seddik. *Small-Scale Energy Harvesting*. InTech, 2012.

[14] J. B. Lee, Zizhang Chen, M. G. Allen, A. Rohatgi, and R. Ayra. A high voltage solar cell array as an electrostatic mems power supply. In *Micro Electro Mechanical Systems, 1994, MEMS '94, Proceedings, IEEE Workshop on*, pages 331–336, 1994.

[15] Hung-Ching Lu and Te-Lung Shih. Design of dc/dc boost converter with fnn solar cell maximum power point tracking controller. In *2010 5th IEEE Conference on Industrial Electronics and Applications*, pages 802–807, June 2010.

[16] R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill, and C. Caylor. Energy harvesting for electronics with thermoelectric devices using nanoscale materials. In *2007 IEEE International Electron Devices Meeting*, pages 367–370, Dec 2007.

[17] S P Beeby, M J Tudor, and N M White. Energy harvesting vibration sources for microsystems applications. *Measurement Science and Technology*, 17(12):R175, 2006.

[18] P. D. Mitcheson, T. C. Green, E. M. Yeatman, and A. S. Holmes. Architectures for vibration-driven micropower generators. *Journal of Microelectromechanical Systems*, 13(3):429–440, June 2004.

[19] Andrii Dudka. *Study, optimization and silicon implementation of a smart high-voltage conditioning circuit for electrostatic vibration energy harvesting system*. PhD thesis, Universite Pierre et Marie Curie, 2014.

[20] L. Huang, V. Pop, R. de Francisco, R. Vullers, G. Dolmans, H. de Groot, and K. Imamura. Ultra low power wireless and energy harvesting technologies- an ideal combination. In *Communication Systems (ICCS), 2010 IEEE International Conference on*, pages 295–300, Nov 2010.

[21] C.B. Williams and R.B. Yates. Proceedings of the 8th international conference on solid-state sensors and actuators eurosensors ix analysis of a micro-electric generator for microsystems. *Sensors and Actuators A: Physical*, 52(1):8 – 11, 1996.

[22] L.D. Landau and E.M. Lifshitz. *Course of Theoretical Physics: Mechanics*. Oxford UK, 1976.

[23] L. C. Julin Blystad and E. Halvorsen. A piezoelectric energy harvester with a mechanical end stop on one side. In *Design Test Integration and Packaging of MEMS/MOEMS (DTIP), 2010 Symposium on*, pages 259–262, May 2010.

[24] D S Nguyen, E Halvorsen, G U Jensen, and A Vogl. Fabrication and characterization of a wideband mems energy harvester utilizing nonlinear springs. *Journal of Micromechanics and Microengineering*, 20(12):125009, 2010.

[25] F. Cottone, H. Vocca, and L. Gammaitoni. Nonlinear energy harvesting. *Phys. Rev. Lett.*, 102:080601, Feb 2009.

[26] T. Galchev, E. E. Aktakka, and K. Najafi. A piezoelectric parametric frequency increased generator for harvesting low-frequency vibrations. *Journal of Microelectromechanical Systems*, 21(6):1311–1320, Dec 2012.

[27] P. D. Mitcheson, E. M. Yeatman, G. K. Rao, A. S. Holmes, and T. C. Green. Energy harvesting from human and machine motion for wireless electronic devices. *Proceedings of the IEEE*, 96(9):1457–1486, Sept 2008.

[28] P. K. Wright S. Roundy and K. S. J. Pister. Micro-electrostatic vibration-to-electricity converters. In *ASME 2002 International Mechanical Engineering Congress and Exposition*, pages 487–496, Dec 2002.

[29] Ghislain Despesse, Thomas Jager, Chaillout Jean-Jacques, Jean-Michel Léger, Andrea Vassilev, Skandar Basrour, and Benoit Charlot. Fabrication and characterization of high damping electrostatic micro devices for vibration energy scavenging. *Proc. Design, Test, Integration and Packaging of MEMS and MOEMS*, pages 386–390, June 2005. ISBN:2-84813-057-1.

[30] A. M. Paracha, P. Basset, D. Galayko, F. Marty, and T. Bourouina. A silicon mems dc/dc converter for autonomous vibration-to-electrical-energy scavenger. *IEEE Electron Device Letters*, 30(5):481–483, May 2009.

[31] R. Guilllemet, P. Basset, D. Galayko, F. Cottone, F. Marty, and T. Bourouina. Wideband mems electrostatic vibration energy harvesters based on gap-closing interdigited combs with a trapezoidal cross section. In *Micro Electro Mechanical Systems (MEMS), 2013 IEEE 26th International Conference on*, pages 817–820, Jan 2013.

[32] L. Solymar and D. Walsh. *Lectures on the electrical properties of materials*. Oxford science publications. Oxford University Press, 1993.

[33] P.D. Mitcheson et. al. Electrostatic microgenerators. *Measurement and Control*, 41(4):114–119, May 2008.

[34] S P Beeby, M J Tudor, and N M White. Energy harvesting vibration sources for microsystems applications. *Measurement Science and Technology*, 17(12):R175, 2006.

[35] V. P. Dragunov and Vitaly Yu. Dorzhiev. Mems electrostatic vibration energy harvester without switches and inductive elements. *Journal of Physics Conference Series*, 4(6):781–784, 2014.

[36] Tra Nguyen Phan. Ultra low-power electronics for energy harvesting node. Master's thesis, Buskerud and Vestfold University College - Department of Micro and Nanosystems Technology, 2015.

[37] V. Dorzhiev, A. Karami, P. Basset, F. Marty, V. Dragunov, and D. Galayko. Electret-free micromachined silicon electrostatic vibration energy harvester with the bennet's doubler as conditioning circuit. *IEEE Electron Device Letters*, 36(2):183–185, 2015.

[38] S Boisseau, G Despesse, and A Sylvestre. Optimization of an electret-based energy harvester. *Smart Materials and Structures*, 19(7):075015, 2010.

[39] P Basset, D Galayko, A Mahmood Paracha, F Marty, A Dudka, and T Bourouina. A batch-fabricated and electret-free silicon electrostatic vibration energy harvester. *Journal of Micromechanics and Microengineering*, 19(11):115025, 2009.

[40] S. Meninger, J. O. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, and J. H. Lang. Vibration-to-electric energy conversion. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 9(1):64–76, Feb 2001.

[41] E. O. Torres and G. A. Rincon-Mora. Electrostatic energy harvester and li-ion charger circuit for micro-scale applications. In *2006 49th IEEE International Midwest Symposium on Circuits and Systems*, volume 1, pages 65–69, Aug 2006.

[42] B. C. Yen and J. H. Lang. A variable-capacitance vibration-to-electric energy harvester. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 53(2):288–295, Feb 2006.

[43] P. D. Mitcheson and T. C. Green. Maximum effectiveness of electrostatic energy harvesters when coupled to interface circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 59(12):3098–3111, Dec 2012.

[44] B. Keeth and W.K. Waller. Low-to-high voltage cmos driver circuit for driving capacitive loads, September 23 1997. US Patent 5,670,905.

[45] D. Pan, H. W. Li, and B. M. Wilamowski. A low voltage to high voltage level shifter circuit for mems application. In *University/Government/Industry Microelectronics Symposium, 2003. Proceedings of the 15th Biennial*, pages 128–131, June 2003.

[46] J. Doutreloigne, H. De Smet, and A. Van Calster. A versatile micropower high-voltage flat-panel display driver in a 100-v 0.7- mu;m cmos intelligent interface technology. *IEEE Journal of Solid-State Circuits*, 36(12):2039–2048, Dec 2001.

[47] A Dudka, P Basset, F Cottone, E Blokhina, and D Galayko. Wideband electrostatic vibration energy harvester (e-veh) having a low start-up voltage employing a high-voltage integrated interface. *Journal of Physics: Conference Series*, 476(1):012127, 2013.

[48] T. Delbruck. 'bump' circuits for computing similarity and dissimilarity of analog voltages. In *Neural Networks, 1991., IJCNN-91-Seattle International Joint Conference on*, volume i, pages 475–479 vol.1, Jul 1991.

[49] P. Torkzadeh, J. Javidan, and M. Atarodi. A 640mhz cmos switched-capacitor sigma-delta adc with 12 bits of resolution by using double sampling technique. In *Circuits and Systems for Communications, 2008. ICCSC 2008. 4th IEEE International Conference on*, pages 572–575, May 2008.

[50] K. Kwok and H. C. Luong. Ultra-low-voltage high-performance cmos vcos using transformer feedback. *IEEE Journal of Solid-State Circuits*, 40(3):652–660, March 2005.

[51] C. K. Hsieh, Kun-Yao Kao, and K. Y. Lin. An ultra-low-power cmos complementary vco using three-coil transformer feedback. In *2009 IEEE Radio Frequency Integrated Circuits Symposium*, pages 91–94, June 2009.

[52] Venigalla Ravi Kanth and K Naresh Kumar. Low power and low frequency cmos ring oscillator design. *European Journal of Advances in Engineering and Technology*, 2(7):82–87, 2015.

[53] Ashis Kumar Mal Rishi Todani and Kanchan Baran Maji. Low frequency ring oscillator and its use in non overlapping clock generation. *International Journal of Engineering and Technology*, 4(6):781–784, 2012.

[54] A. K. Mahato. Ultra low frequency cmos ring oscillator design. In *Engineering and Computational Sciences (RAECS), 2014 Recent Advances in*, pages 1–5, March 2014.

[55] A. E. Mourabit, Guo-Neng Lu, and P. Pittet. Wide-linear-range subthreshold ota for low-power, low-voltage, and low-frequency applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(8):1481–1488, Aug 2005.

[56] U. Denier. Analysis and design of an ultralow-power cmos relaxation oscillator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(8):1973–1982, Aug 2010.

[57] B. H. Calhoun, A. Wang, and A. Chandrakasan. Modeling and sizing for minimum energy operation in subthreshold circuits. *IEEE Journal of Solid-State Circuits*, 40(9):1778–1786, Sept 2005.

[58] E. M. Camacho-Galeano, C. Galup-Montoro, and M. C. Schneider. A 2-nw 1.1-v self-biased current reference in cmos technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 52(2):61–65, Feb 2005.

[59] F. Serra-Graells and J. L. Huertas. Sub-1-v cmos proportional-to-absolute temperature references. *IEEE Journal of Solid-State Circuits*, 38(1):84–88, Jan 2003.

[60] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro. An mos transistor model for analog circuit design. *IEEE Journal of Solid-State Circuits*, 33(10):1510–1519, Oct 1998.

[61] C. C. Enz and E. A. Vittoz. Cmos low-power analog circuit design. In *Designing Low Power Digital Systems, Emerging Technologies (1996)*, pages 79–133, 1996.

[62] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss. Series-parallel association of fet's for high gain and high frequency applications. *IEEE Journal of Solid-State Circuits*, 29(9):1094–1101, Sep 1994.

[63] A. M. Sodagar and K. Najafi. A wide-range supply-independent cmos voltage reference for telemetry-powering applications. In *Electronics, Circuits and Systems, 2002. 9th International Conference on*, volume 1, pages 401–404 vol.1, 2002.

[64] J. Lu, T. Yang, M. S. Jahan, and J. Holleman. Nano-power tunable bump circuit using wide-input-range pseudo-differential transconductor. *Electronics Letters*, 50(13):921–923, June 2014.