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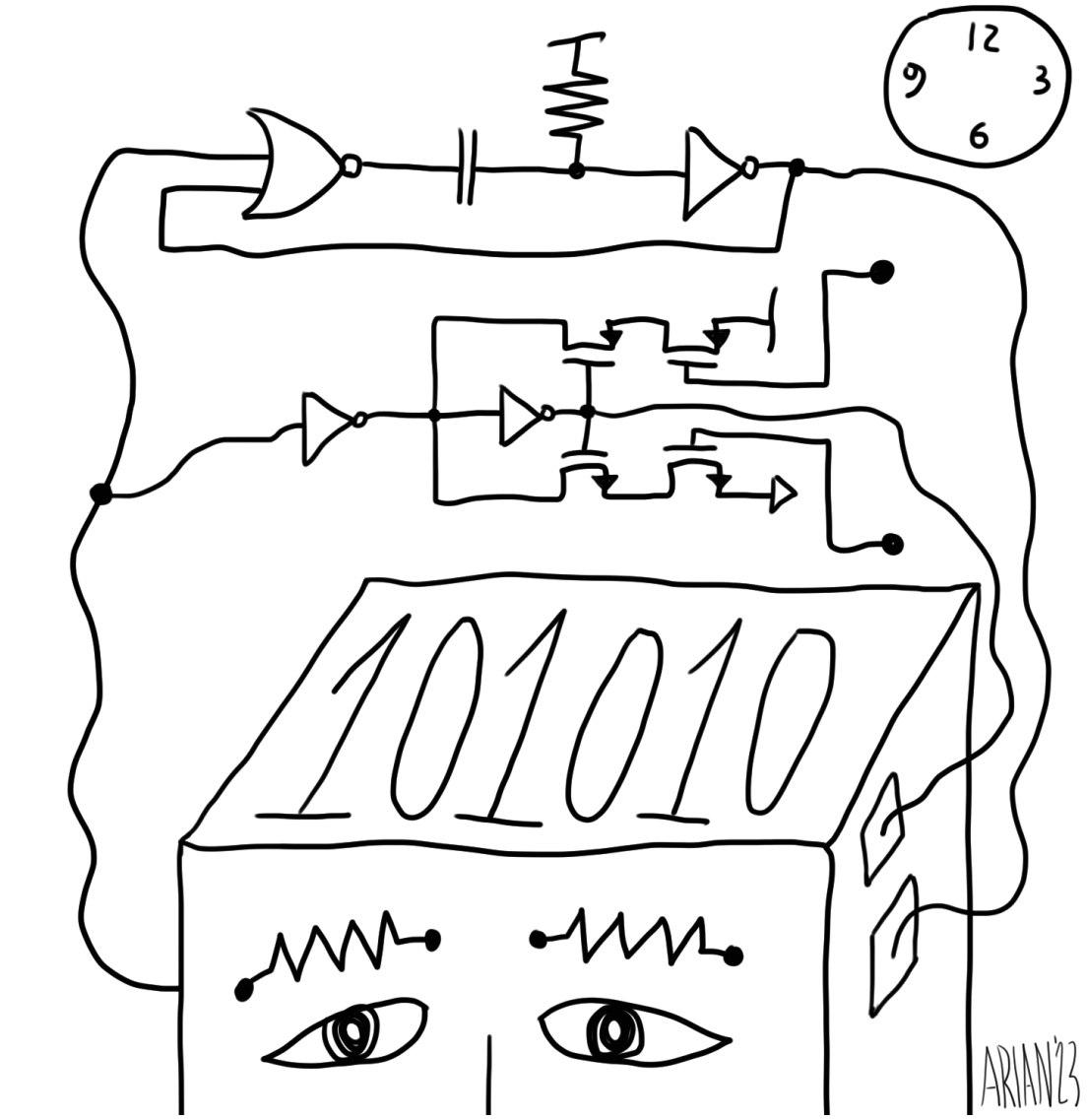
Arian Nowbahari

Low Power Circuits and Architectures for Wireless Sensor Networks



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Low Power Circuits and Architectures for Wireless Sensor Networks

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Dedication

To my grandfather, in loving memory.

Preface

This thesis is submitted for the degree of Philosophiae Doctor at the University of South-Eastern Norway. The research was conducted under the supervision of Associate Professor Mehdi Azadmehr and co-supervision of Associate Professor Luca Marchetti in the Department of Microsystems, University of South-Eastern Norway, Vestfold, between November 2019 and September 2022.

From October 2022 to December 2022, I worked as a visiting researcher in the Department of Mechanical, Aerospace, and Nuclear Engineering, Rensselaer Polytechnic Institute, NY, USA under the supervision of Professor Diana-Andra Borca-Tasciuc.

I hereby declare that all material presented in this thesis is my own research unless otherwise stated.

Acknowledgements

I would like, first and foremost, to express my sincere gratitude to my main supervisor Mehdi Azadmehr, for his continuous support and his trust in my research ideas. Working with him made me grow not only as a researcher, but also as a human. Without his supervision, the work presented in this thesis would not be possible. I also would like to express my sincere gratitude to my co-supervisor Luca Marchetti, who made me really passionate about Electronics. The help received from him is invaluable. I also would like to thank Einar Halvorsen for the useful discussions.

I am thankful to my colleagues at the University of South-Eastern Norway, Mahdieh, Hamed, Nabin and Osman. Thank you for all the coffee breaks. In particular, I would like to thank my friend and colleague Amirfereydoon.

I also would like to express my gratitude to Diana-Andra Borca-Tasciuc, who gave me the opportunity to work with her research team. I say thanks to my colleagues at the Rensselaer Polytechnic Institute, Hannah, Matt and Meg.

Last but not least, I say thanks to my mother and my father for their constant love, support, and encouragement. Thank you.

Abstract

Wireless sensor networks (WSNs), due to their multidisciplinary applications, represent one of the main enabling technologies of the Internet-of-Things paradigm. These networks, consisting of sensor nodes characterized by processing and transmitting capabilities, are implemented in various fields such as oceanography, disaster prevention, the oil and gas industry, health, commercial, and military applications. A critical challenge in designing WSNs is optimizing the sensor node's power consumption, which determines the network lifetime. One of the most efficient energy-saving approaches consists of integrating Wake-Up Receivers (WuRxs), which allow selective activation of the sensor nodes on demand. This thesis reports three novel WuRx architectures and six low power circuit implementations. Two of the implementations, one based on tunable current starved inverters and one on tunable NOR-based multivibrators, present the lowest power consumption reported for an underwater acoustic WuRx. Their performances have been experimentally validated through an ASIC (AMS-350nm CMOS process) by decoding an acoustic wake-up call transmitted underwater. Both circuits consume less than 500 nW. The tunable current starved inverter-based WuRx consumes 265 nW, it has an area of 0.058 mm^2, and a data rate of 250 bit/s. At simulation level, one of the circuit implementations (Single Transistor) presents the lowest power consumption reported for an acoustic WuRx (7.2 nW). In this thesis, also analytical models for the subthreshold operation of some Schmitt triggers (STs), which are extensively implemented in sensor node architectures, have been derived. The hysteresis voltages of a tunable ST and of a low power ST have been analytically modeled. The derived expressions provide physical insight into the behavior of the circuits, by relating the hysteresis voltages to the transistors' geometrical parameters. Furthermore, the models can be used to predict the effect of supply voltage and temperature variations on the characteristics and to estimate the minimum supply voltage for which hysteresis occurs. The models have been experimentally validated, with a maximum error below 10 %, relative to the supply voltage. Overall, the proposed circuits and architectures can be used in implementation of low power sensor nodes.

List of Articles

Wake-up receivers:

1. A. Nowbahari, L. Marchetti and M. Azadmehr, 'A Delay-Based Wake-Up Receiver for Wireless Sensor Networks,' in *2021 International Conference on Electrical, Communication, and Computer Engineering (ICECCE)*, 2021, pp. 1–5. DOI: 10.1109/ICECCE52056.2021.9514246

2. A. Nowbahari, L. Marchetti and M. Azadmehr, 'An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks,' in *2021 IEEE 7th World Forum on Internet of Things (WF-IoT)*, 2021, pp. 380–384. DOI: 10.1109/WF-IoT51360.2021.9595159

3. A. Nowbahari, L. Marchetti and M. Azadmehr, 'Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks,' in *2022 11th International Conference on Communications, Circuits and Systems (ICCCAS)*, 2022, pp. 187–191. DOI: 10.1109/ICCCAS55266.2022.9825344

4. A. Nowbahari, L. Marchetti and M. Azadmehr, 'An Oscillator-Based Wake-Up Receiver for Wireless Sensor Networks,' in *2021 IEEE Sensors Applications Symposium (SAS)*, 2021, pp. 1–5. DOI: 10.1109/SAS51076.2021.9530093

Unpublished article, not included in online edition

5. A. Nowbahari, L. Marchetti and M. Azadmehr, 'Low Power Wake-Up Receivers for Underwater Acoustic Wireless Sensor Networks,' *IEEE Transactions on Green Communications and Networking*, Under Review.

Schmitt triggers:

6. A. Nowbahari, L. Marchetti and M. Azadmehr, 'Weak Inversion Model of an Inverting CMOS Schmitt Trigger,' in *2022 11th International Conference on Communica-*

tions, Circuits and Systems (ICCCAS), 2022, pp. 1–5. DOI: 10.1109/ICCCAS55266.2022.9824290

7. A. Nowbahari, L. Marchetti and M. Azadmehr, 'Analysis of a Low Power Inverting CMOS Schmitt Trigger Operating in Weak Inversion,' *International Journal of Electrical and Electronic Engineering & Telecommunications*, vol. 11, no. 6, pp. 392–397, 2022. DOI: 10.18178/ijeetc.11.6.392-397. [Online]. Available: http://www.ijeetc.com/uploadfile/2022/1014/20221014033458167.pdf

8. A. Nowbahari, L. Marchetti and M. Azadmehr, 'Subthreshold Modeling of a Tunable CMOS Schmitt Trigger,' *IEEE Access*, vol. 11, pp. 10 977–10 984, 2023. DOI: 10.1109/ACCESS.2023.3241492

Other[1]:

9. A. Nowbahari, A. Roy and L. Marchetti, 'Junctionless Transistors: State-of-the-Art,' *Electronics*, vol. 9, no. 7, 2020. DOI: 10.3390/electronics9071174

10. M. Azadmehr, A. Nowbahari, L. Marchetti and R. Langoy, 'A Low Power Front-End for Resistive Sensors based on Switch-Cap Current Reuse,' in *2022 IEEE 15th Dallas Circuit And System Conference (DCAS)*, 2022, pp. 1–5. DOI: 10.1109/DCAS53974.2022.9845572

11. J. Li, H. Ouro-Koura, H. Arnow, A. Nowbahari, M. Galarza, M. Obispo, X. Tong, M. Azadmehr, M. M. Hella, J. A. Tichy and D.-A. Borca-Tasciuc, 'A Novel Comb Design for Enhanced Power and Bandwidth in Electrostatic MEMS Energy Converters,' in *2023 IEEE 36th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2023, pp. 728–731. DOI: 10.1109/MEMS49605.2023.10052590

[1]These publications are not included in this thesis, because they are not closely related to aims and objectives of the performed research. Nevertheless, they contributed in developing skills and knowledge implemented in this work.

List of Figures

List of Abbreviations

Abbreviation	Definition
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
CPGA	Ceramic Pin Grade Array
DTMOS	Dynamic Threshold Metal-Oxide-Semiconductor
EKV	Enz-Krummenacher-Vittoz
FET	Field-Effect Transistor
IoT	Internet-of-Things
LED	Light-Emitting Diode
MAC	Medium Access Control
MEMS	MicroElectroMechanical Systems
MOS	Metal-Oxide-Semiconductor
MPW	Multi-Project-Wafer
NMOS	N-Type Metal-Oxide-Semiconductor
NOAA	National Oceanographic and Atmospheric Administration
PCB	Printed Circuit Board
PMOS	P-Type Metal-Oxide-Semiconductor
pMUT	Piezoelectric Micromachined Ultrasonic Transducer
RF	Radio Frequency
RX	Receive
SOSUS	Sound Surveillance System
SRAM	Static Random Access Memory
ST	Schmitt Trigger
TWSN	Terrestrial Wireless Sensor Network

Abbreviation	**Definition**
TX	Transmit
UAWSN	Underwater Acoustic Wireless Sensor Network
UOWSN	Underwater Optical Wireless Sensor Network
UWSN	Underwater Wireless Sensor Network
WSN	Wireless Sensor Network
WuC	Wake-Up Call
WuRx	Wake-Up Receiver
µC	Microcontroller

List of Symbols

Symbol	Description
W	MOSFET Channel Width
L	MOSFET Channel Length
$\mu_{n(p)}$	Electron (Hole) Mobility
C_{ox}	MOSFET Oxide Capacitance
$C_{dep,n(p)}$	NMOS (PMOS) Depletion Layer Capacitance
$n_{n(p)}$	NMOS (PMOS) Slope Factor
V_H	Schmitt Trigger Hysteresis Voltage
V_{HL}	Schmitt Trigger High-To-Low Voltage
V_{LH}	Schmitt Trigger Low-To-High Voltage
$V_{th,n(p)}$	NMOS (PMOS) Threshold Voltage
V_{dd}	Supply Voltage
$S_{n(p)}$	NMOS (PMOS) Subthreshold Swing
T	Temperature
k_B	Boltzmann Constant
q	Electric Charge
ϕ	Thermal Voltage

Contents

1 Introduction

1.1 Background

One of the main pillars of how the ”things”-oriented vision of the Internet-of-Things (IoT) paradigm is implemented, is through Wireless Sensor Networks (WSNs) [12]. A WSN can be defined as a group of spatially distributed sensor nodes (Fig.1.1(a)), characterized by processing and transmitting capabilities [13]. From an architecture point of view, a sensor node can be decomposed into four main sub-units (Fig.1.1(b)): communication unit, to receive and transmit data; power unit, to supply the node; sensing unit, to acquire environmental data; processing unit, to manage data acquisition and transmission [14], [15].

The first WSN resembling a modern system has been attributed to the Sound Surveillance System (SOSUS), developed in the early 1950s by the United States Navy to track and detect Soviet submarines [16]. The system was composed of a network of hydrophones,

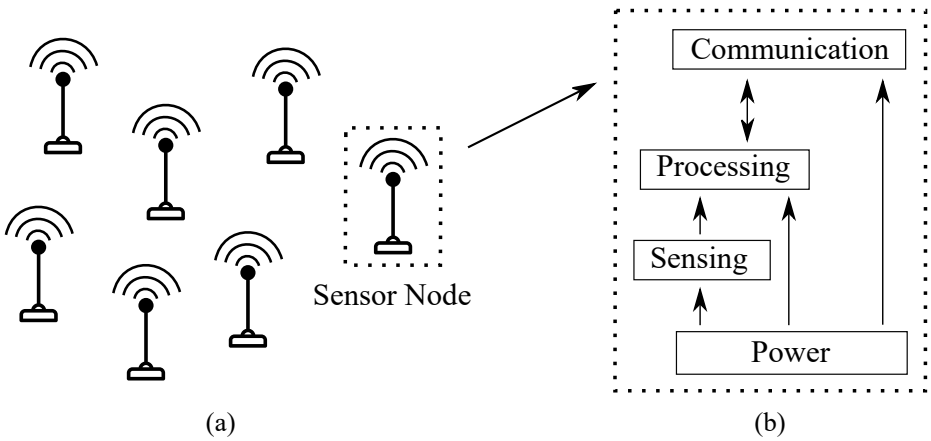


Figure 1.1: (a) Wireless sensor network and (b) simplified sensor node architecture.

distributed in the Pacific and Atlantic oceans [17]. Nowadays, SOSUS is still operating and is used for civil scientific research, e.g. ocean monitoring by the National Oceanographic and Atmospheric Administration (NOAA) [18]. Therefore, one can claim that the first WSN was an Underwater system (UWSN). Modern UWSNs typically consist of a complex ensemble of different sensor nodes, which can be static, semi-mobile and mobile [19]–[21]. Static sensor nodes are leaned on the seafloor, and can be cabled or wirelessly connected to other nodes. Semi-mobile sensor nodes can be moored or attached to a buoy or a ship, e.g. as Remotely Operated Vehicles (ROVs). Mobile sensor nodes generally consist of Autonomous Underwater Vehicles (AUVs). In a typical scenario (Fig.1.2), the data collected by the underwater sensor nodes are sent to a surface sink (e.g. a ship), which transmits the data to a satellite and/or to an onshore sink [22]. In terms of applications, UWSNs are employed for: ocean monitoring, e.g. ocean currents, climate change, pollution and biological monitoring; disaster prevention, e.g. seismic and volcanic activity analysis; oil and gas industry, e.g. corrosion detection in pipes; oceanography, e.g. seafloor mapping; assisted navigation and military surveillance [23]–[27].

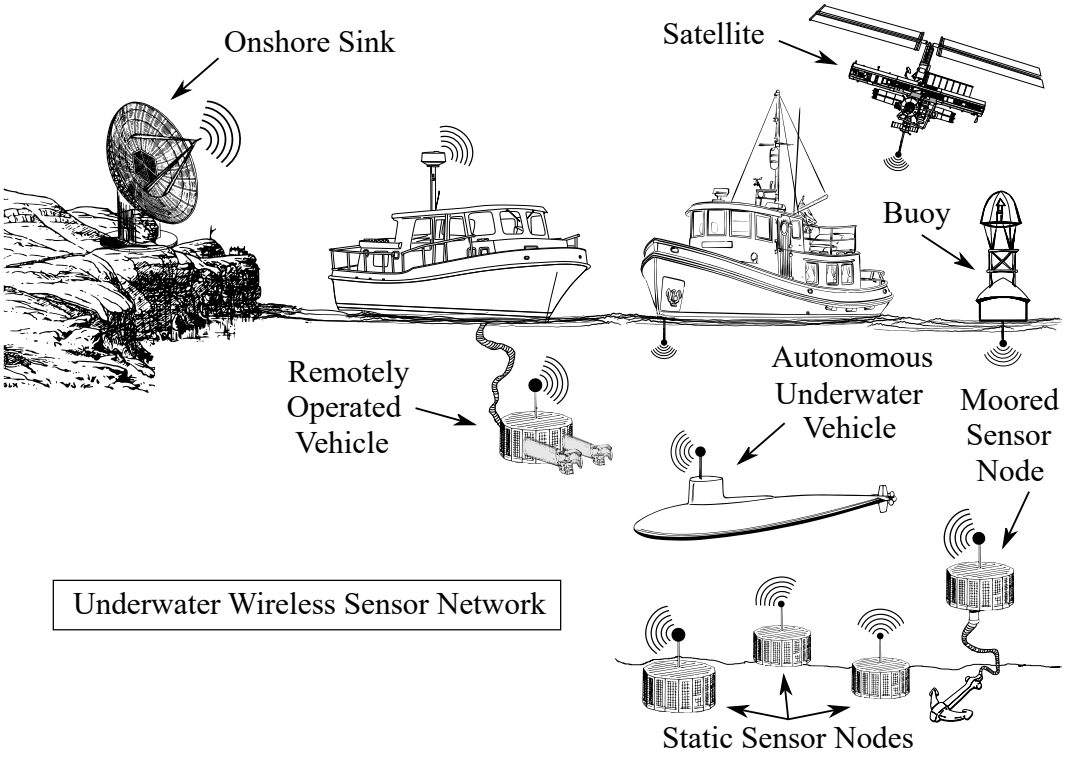


Figure 1.2: Illustration of an UWSN (not in scale). Adapted from [5].

WSNs are not limited to underwater applications, and Terrestrial Wireless Sensor Networks (TWSNs) are also extensively employed [28], [29]. These are implemented in various fields, such as: health applications, e.g. telemonitoring physiological data, drug administration and patient tracking [30], [31]; home applications, e.g. temperature and light regulation [32], [33]; environmental applications, e.g. biodiversity monitoring and fire detection [34], [35]; commercial and military applications [36], [37].

The number of sensor nodes in a WSN ranges from a few to thousands of units, depending on the application. Generally, the minimum number of sensor nodes is set by the required network coverage of the sensing field, while the maximum number is constrained by the energy consumption and the cost [38]–[40]. The field of application also determines the type of signals used by the communication unit (Fig.1.1(b)), which can be Radio-Frequency (RF), optical or acoustic. RF signals are not particularly suitable for underwater communication, due to the required high transmission power and large antenna size. Their use is typically restricted to shallow waters and short distances (e.g. within swarms of AUVs) [41]–[43]. Underwater Optical Wireless Sensor Networks (UOWSNs) typically present low latency and high data rates (Gbps) [44]. But due to line-of-sight requirements, the alignment of optical transceivers underwater is challenging [45]. Instead, Underwater Acoustic Wireless Sensor Networks (UAWSNs) are suitable for subsea applications since their are characterized by longer transmission range and reduced attenuation, with respect to the RF counterpart. However, UAWSNs present higher latency, lower data rate and limited bandwidth [23], [46], [47]. Different types of signal can coexist in the same network, i.e. also hybrid architectures have been investigated, e.g. acoustic-optical and RF-optical WSNs [48], [49].

1.2 Motivation

Regardless of the considered transmission medium and type of signal, a critical challenge common to all WSN architectures is the optimization of the sensor node's power consumption [50]–[52]. The power unit (Fig.1.1(b)) typically consists of a battery with a limited energy budget, and/or relies on energy harvesting. In some applications (e.g. underwater), replacing and/or recharging the power units is not feasible and is costly. [53]. The main reason for improving the energy efficiency of WSNs is to extend the network

lifetime, which represents one of the most important metrics for performance evaluation [54]–[56]. The literature about WSNs & Energy is quite extensive: considering only IEEE Xplore®, more than six thousand journal articles and thirty thousand conference papers have been published so far. Nevertheless, the State-of-the-Art is still improving, considering that only in 2022, six hundred journal articles have been reported. In this dissertation, the target is to optimize the sensor node's power consumption at the hardware level, i.e. all the contributions are electronics-related. Therefore, the main motivation behind this dissertation is to provide low power circuits and architectures for improving the lifetime of wireless sensor networks, and so advancing the State-of-the-Art.

1.3 Methodology

The methodology employed in this work consists of three main steps: first, a general sensor node architecture is defined step-by-step, with the aim of identifying the critical blocks; next, optimizing circuits and architectures are designed; finally, an experimental setup is realized, and the designs are validated through measurements.

1.3.1 Sensor Node Architecture

In Fig.1.3(a), the sensor node architecture is divided in four sub-units, i.e. communication, processing, sensing and power units. The communication unit is typically implemented through transducers, which are used to Transmit (TX) and Receive (RX) power and/or information. Depending on the architecture, a single device can be used for both transmission and reception (i.e. a transceiver). The type of transducer is dependent on the application, e.g. antennas for RF-based WSNs, LEDs/photodiodes for optical-based WSNs, and piezoelectric transducers for acoustic ones [57], [58]. The sensing unit consists of sensors which acquire data from the external environment (Fig.1.3(b)) [59]. The data acquired by the sensors are sent to the processing unit, which typically consists of a microcontroller (µC) [60]. Depending on the implemented µC, an Analog-to-Digital Converter (ADC) is interposed between the sensors and the microcontroller. In the following, it is assumed that the µC has a built-in ADC for simplicity. The power unit supplies the sensors, the µC and the communication unit (Fig.1.3(c)), i.e. it acts as an energy storage

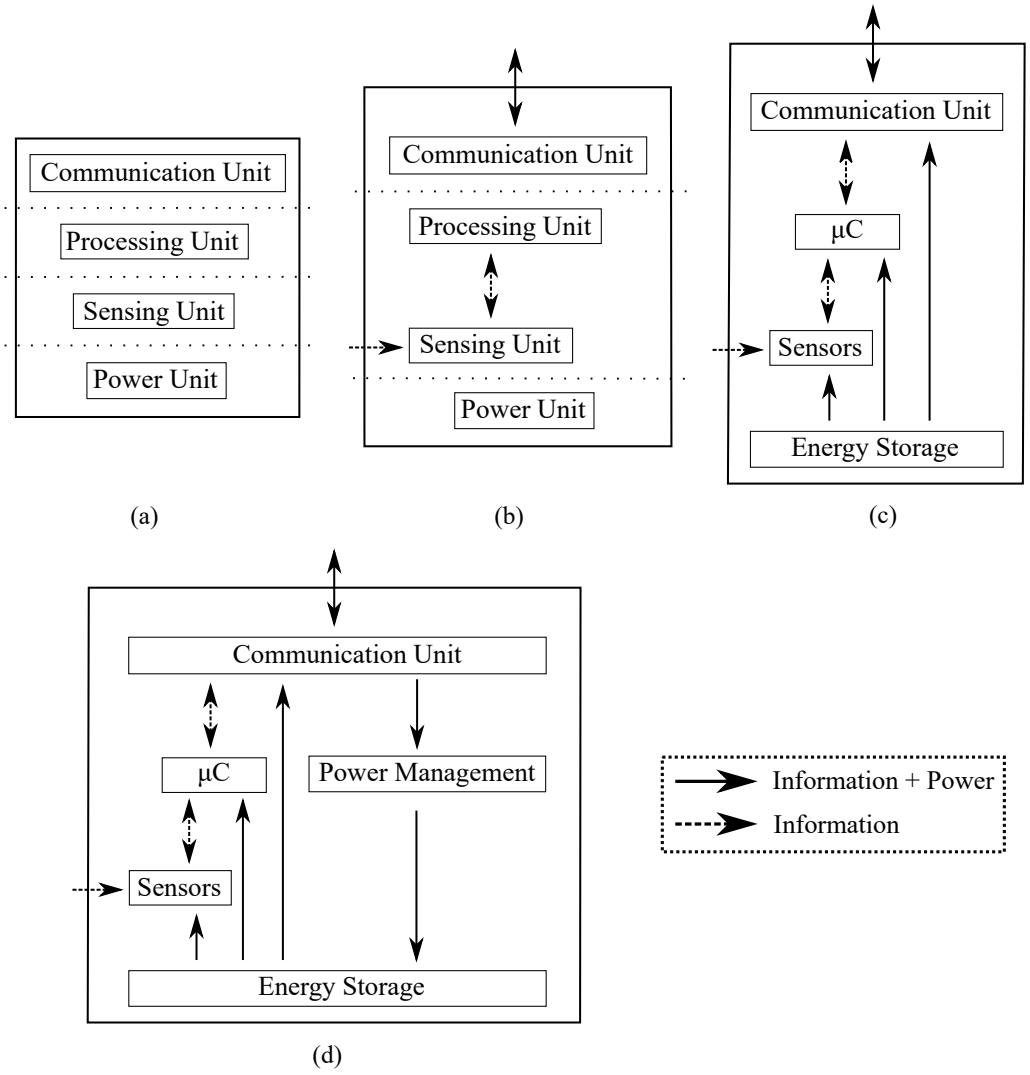


Figure 1.3: Definition of a general and simplified sensor node architecture. (a) Main units. (b) Connection between sensing and processing units. (c) Non-rechargeable and (d) rechargeable sensor node architectures.

(e.g. alkaline or lithium battery) [61]. As represented in Fig.1.3(c), the energy storage is not rechargeable, i.e. the communication unit does not transfer power to the sensor node. Nevertheless, sensor nodes can also rely on energy harvesting [62]. In this case, an additional unit, defined as power management unit, is interposed between the communication unit and the energy storage, as shown in Fig.1.3(d). It should be pointed out that the presented architectures are oversimplified and not totally accurate with respect to real implementations. For instance, in some architectures, the transducers used to harvest energy do not coincide with those used for communication [63]. Furthermore, additional

units can be present (e.g. location finder unit) [64]. However, the simplified architecture in Fig.1.3(d) represents an useful starting point for the analysis of the critical blocks, as explained in the following.

1.3.2 Circuits and Architectures

Referring to the sensor node architectures in Figs.1.3(c) and (d), the most critical component results to be the energy storage since it supplies all the other units. The identification of the most energy-draining unit is a complex task, because the power consumption depends on the implemented application and technology. Generally, the most power consuming unit is the communication one, although also the processing and sensing units can result power-hungry, specially when composed of many active sensors (e.g. sonar rangers and imagers) [65]–[67].

To minimize the power consumption of the communication unit, different energy saving protocols have been proposed [52], [68]. A widely implemented method consists in powering off the sensor nodes as long and as often as possible, so that the communication between any two nodes takes place only when they are simultaneously on, i.e. a communication protocol is required [69]. The way through which the sensor nodes communicate is referred to as *rendezvous*. As it will be explained in detail in a dedicated section (Chapter 2), one of the most energy-efficient rendezvous scheme consists in the integration of Wake-Up Receivers (WuRxs). These additional units wake up the sensor nodes only when a well defined signal, called Wake-Up Call (WuC), is received. Therefore, they allow selective activation on demand [70]. A sensor node architecture integrating WuRxs is shown in Fig.1.4, where it has been assumed, for simplicity, that the WuRx has its own battery, i.e. it does not rely on the energy storage unit. Nevertheless, WuRxs can also rely on energy harvesting. The majority of the proposed WuRxs are RF-based, and designed for terrestrial wireless sensor networks [71]. Recently, acoustic solutions started to gain attention because of the significant advancements in the fields of underwater wireless sensor networks and acoustics [72]–[75]. Therefore, in this work, it has been decided to focus on the development of novel wake-up receivers architectures with State-of-the-Art performance for UAWSNs.

In this work, the optimization has not been restricted only to the design of new WuRx architectures. In fact, also Schmitt Trigger (ST) circuits have been analyzed. STs are

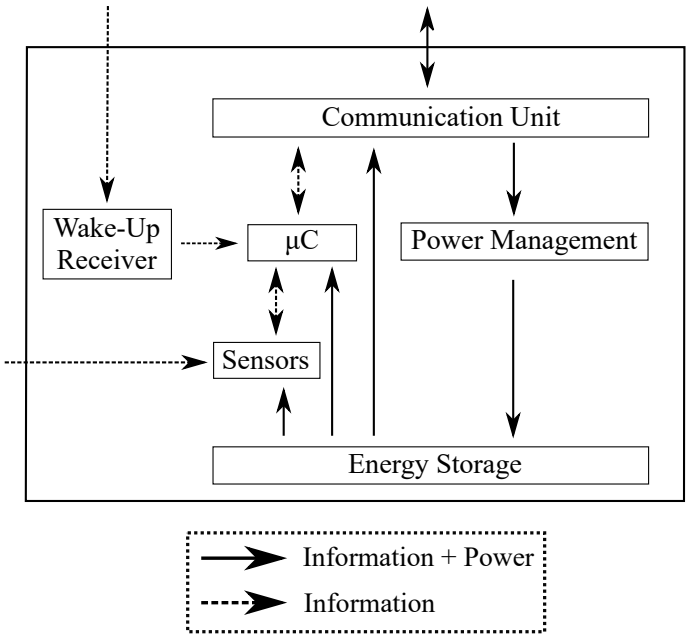


Figure 1.4: Rechargeable sensor node architecture with wake-up receiver integration.

extensively employed in sensor node architectures, e.g. for signal shaping in transceivers, memory cell implementation in µCs, noise reduction in sensor interfaces, and DC/DC converters drivers in energy harvesting interfaces [76]–[82]. Therefore, they can be implemented in all the units in Fig.1.3(d). Over the last decades, researchers focused on the optimization of ST circuits for low voltage and low power applications, due to the increasing demand of energy-efficient electronics [83], [84]. In particular, current literature focuses on the analysis and modeling of STs operated in subthreshold region [85]. In this work, two Complementary Metal-Oxide-Semiconductor (CMOS) ST circuits have been analyzed and modeled in subthreshold region. The first circuit, labeled as *Type 1* in this thesis, is the low power CMOS ST proposed by Al-Sarawi (Fig.1.5(a)) in 2002 [86]. It has been decided to analyze *Type 1* because, among the single input STs, it presents one of the best figure of merits, according to [87]. The second circuit, labeled as *Type 2*, is the tunable single input CMOS ST proposed by Wang (Fig.1.5(b)) in 1991 [88]. It has been decided to analyze *Type 2* because of its simplicity and versatility. At the time of writing, this is the first single input tunable CMOS ST modeled in subthreshold region. An overview of ST circuits operated in subthreshold region is reported in a dedicated section (Chapter 3). Therefore, in this thesis, optimization has been performed on two levels: at architecture level, by developing novel wake-up receiver architectures; at circuit

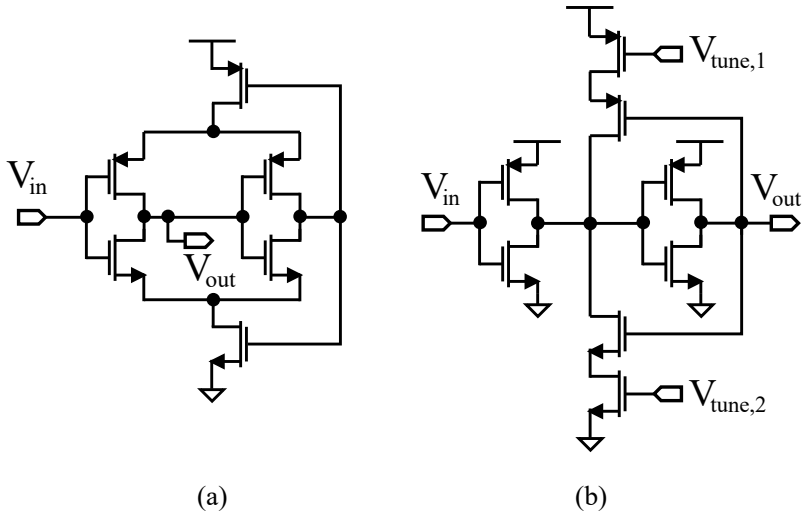


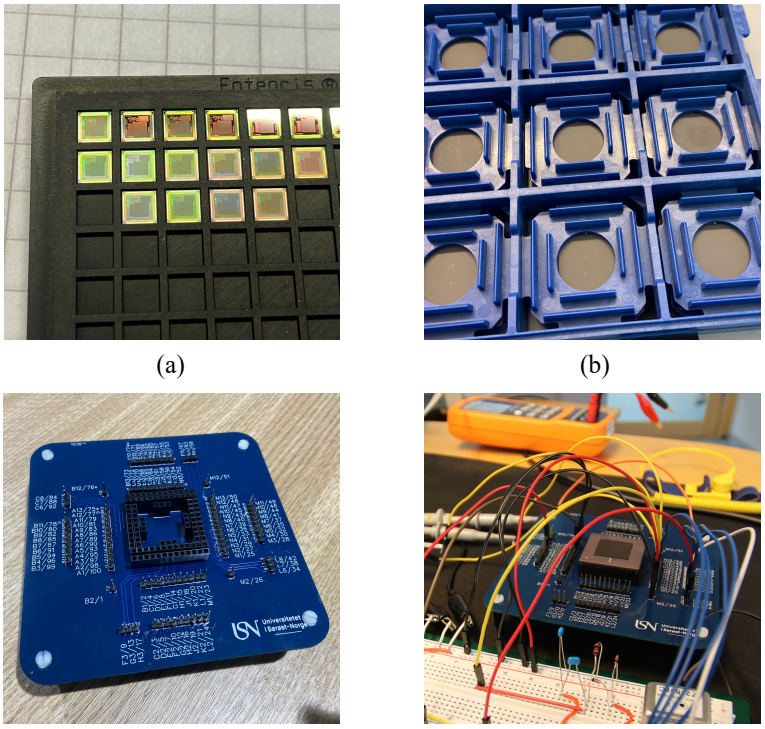
Figure 1.5: (a) Al-Sarawi's (*Type 1*) [86] and (b) Wang's (*Type 2*) [88] Schmitt trigger circuits under analysis in this work.

level, by developing analytical models which can be used to optimize the design of low power Schmitt trigger circuits operated in subthreshold region.

1.3.3 Experimental Setup

The designed circuits and architectures have been validated through an Application Specific Integrated Circuit (ASIC). The layout and the micrograph are reported in Appendix A. Initially, the WuRxs have been designed and simulated by considering a TSMC-180nm CMOS process[1]. Once the 2021 Multi-Project-Wafer (MPW) runs from Europractice[2] have been disclosed, the circuits have been redesigned in AMS-350nm CMOS process[3] due to funding and timing constraints. The circuits have been designed through Cadence[4] (version 6.1.8-64b, TECH_C35B4). Thirty identical ASICs have been delivered, and ten of them have been packaged. The realized ASICs, shown in Fig.1.6(a), have dimensions 3 mm × 3 mm, and are packaged into a ceramic pin grid array (CPGA100) with sealed lid, as shown in Fig.1.6(b). The CPGA100 is then mounted on a Printed Circuit Board (PCB), shown in Fig.1.6(c), designed and fabricated through JLCPCB[5].

[1] (https://www.tsmc.com/)
[2] (https://europractice-ic.com/)
[3] (https://ams.com/)
[4] (https://www.cadence.com/)
[5] (https://jlcpcb.com/)



(a) (b) (c) (d)

Figure 1.6: (a) ASICs in AMS-350nm CMOS process. (b) ASICs packaged into CPGA100s (sealed lid). (c) Designed PCB used to access the ASIC's pads. (d) Example of setup for signal acquisition.

The input/output signals are then applied/acquired directly through the PCB, and/or by means of a breadboard, as shown in Fig.1.6(d). As previously mentioned, the WuRxs have been designed for UAWSNs. Therefore, a simple experimental setup composed of a water tank, two transducers (TX & RX), a signal generator, and an oscilloscope has been realized (Fig.1.7(a)). For simplicity, the circuitry required to drive the ASIC (e.g. power supplies) is not included in Fig.1.7(a). Due to the complexity of ASIC packaging for underwater operation, only the transducers have been placed underwater, i.e. communication takes place underwater but the ASIC is placed out of the tank. To transmit/receive the wake-up call signal, commercial piezoelectric transducers (HESENTEC[6]) have been used. These transducers are not intended for underwater use. Therefore, a thin layer of epoxy has been applied on the electrical contacts, to make them waterproof. The resonance frequency (40 kHz) has been then measured through a R&S ZVL13 Vector Network Analyzer (Figs.1.7(b) and (c)). The water tank, shown in Fig.1.7(d), is made of polyethylene, and it has dimensions 100 cm × 120 cm × 76 cm. The tank has been filled with

[6](http://www.hesentec.com/)

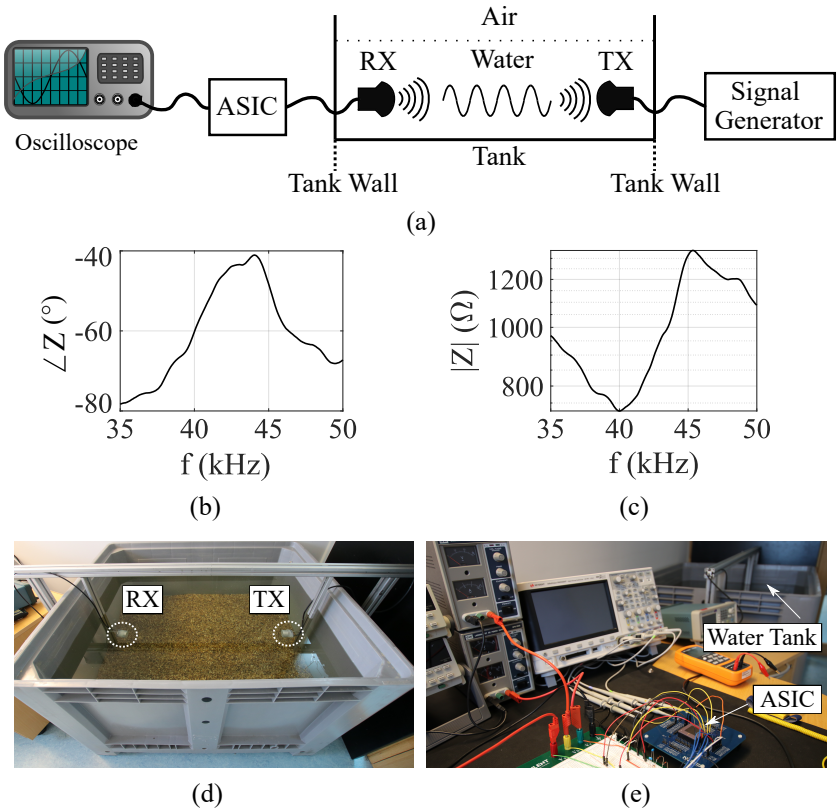


Figure 1.7: (a) Simplified scheme of the experimental setup for underwater testing. Measured impedance (b) magnitude and (c) phase of the piezoelectric transducers. (d) Water tank and transducers. (e) Example of full setup. Adapted from [5].

distilled water. An example of full setup is shown in Fig.1.7(e). Clearly, the implemented setup is not accurate with respect to real application scenarios where different phenomena, such as path loss (geometric spreading, scattering, attenuation), ambient noise, multipath propagation, and Doppler spread take place simultaneously [89]. For instance, the proposed setup strongly suffers from multipath propagation, due to the small size of the tank, and to the short distance between the transducers and the water/air and water/tank interfaces. On the bottom, a 3 cm thick layer of crushed rocks (grain diameter from 3 mm to 5 mm) has been deposited to reduce reflections [90]. Besides that, no other optimization has been performed on the water tank (e.g. coating the inner walls of the tank with a phono-absorbing material). Nevertheless, the realization of an anechoic chamber was out of scope in this work since the focus was only on the circuitry. Regarding the Schmitt trigger circuits, they have been tested by using a setup similar to that in Fig.1.6(d).

1.4 Research Contributions

In this thesis, novel wake-up receiver architectures and analytical models for the subthreshold operation of Schmitt trigger circuits have been developed. The proposed circuits and architectures can be used to optimize the power consumption of wireless sensor networks. Regarding the wake-up receivers, three different types of architecture have been developed: inverter-based, multivibrator-based, and oscillator-based acoustic WuRxs for wireless sensor networks. The inverter-based and multivibrator-based WuRxs are similar in terms of decoding mechanism, but present different circuit implementations. The first inverter-based WuRx (called Delay-based) has been proposed, at simulation level, in [1] (Appendix B.1); although low power, it does not present State-of-the-Art power consumption. Nevertheless, it is the first WuRx that implements one of the novel wake-up decoding mechanisms proposed in this work. However, the delay-based WuRx has been then improved, leading to the tunable current starved inverter-based WuRx called *Type A* in this thesis (Appendix B.5) [5]. *Type A* presents the lowest power consumption reported for an underwater acoustic WuRx, and it has been experimentally validated. Regarding the multivibrator-based WuRxs, three different circuit implementations have been proposed. The first one uses a NOR-based monostable multivibrator (Appendix B.2) [2] , the second one uses a single transistor (Appendix B.3) [3], while the third one, called *Type B* in this thesis, is an improved version (tunability) of the NOR-based architecture (Appendix B.5) [5]. Also *Type B* has been experimentally validated, and it presents State-of-the-Art power consumption as well. The single transistor multivibrator-based WuRx presents, at simulation level, the lowest power consumption reported for a non-underwater acoustic WuRx, and it overcomes the performances of *Type A* and *Type B*. The oscillator-based WuRx is a low power wake-up receiver, but does not overcome, in terms of performance, the other proposed WuRxs (Appendix B.4) [4]. It should be pointed out that the novel wake-up decoding mechanisms proposed in this work are not limited only to acoustic applications, i.e. the design of all the WuRx circuits can be easily adapted to RF applications. Regarding the Schmitt trigger circuits, analytical models for the hysteresis voltages in subthreshold region of two STs, i.e. Al-Sarawi's ST (*Type 1*) and Wang's ST (*Type 2*) shown in Fig.1.5, have been proposed. The models allow to design the two STs with desired hysteresis as a function of the transistors' geometrical parameters. Furthermore, they provide physical insight into the circuit behavior, by relating the hysteresis voltage to the supply and thermal voltages. The derived expressions can

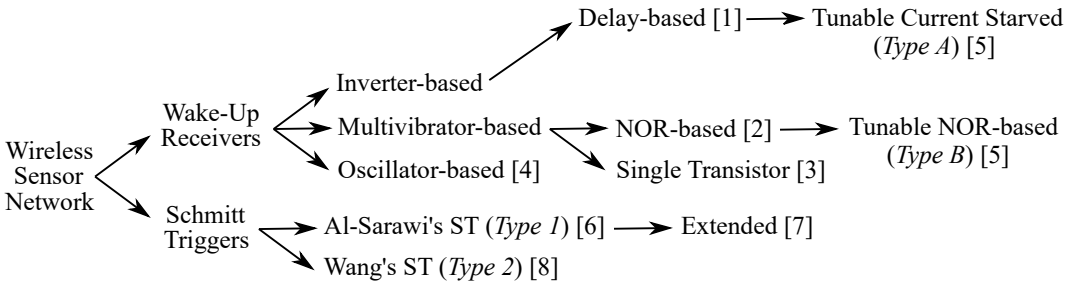


Figure 1.8: Graphical overview of the research contributions.

be used to optimize the design of STs circuits in subthreshold region, e.g. estimating the minimum supply voltage for which hysteresis occurs and predict the effect of temperature variations on the characteristics. The analytical model of *Type 1* has been first proposed and validated through simulations and experiments (Appendix C.1) [6]. Next, the model has been further analyzed by also considering simplified equivalent circuits and different designs (Appendix C.2) [7]. Regarding *Type 2*, its analytical model has been proposed and validated through simulations and experiments in [8] (Appendix C.3). The accuracy of the model has been also analyzed in terms of supply voltage, temperature and process variations. A graphical overview of the research contributions is shown in Fig.1.8. In summary, the proposed WuRxs optimize the power consumption of the communication unit, while the developed analytical models can be used to optimize the design of low power ST circuits, thus virtually allowing optimization of all the units. Therefore, the research contributions in this work consist of low power circuits and architectures which optimize the sensor nodes' power consumption.

1.4.1 Dissertation Outline

In Chapter 2, an overview of WuRxs and energy conservation techniques for WSNs is reported, and the proposed architectures are described. In Chapter 3, an overview of ST circuits operated in subthreshold region is reported, and the main results are discussed. The conclusions and future directions are in Chapter 4. The layout and the micrograph of the ASIC are in Appendix A, while the articles associated to the WuRxs and the ST circuits are in Appendices B and C, respectively.

2 Wake-Up Receivers

2.1 Background

From a taxonomic point of view, three main energy conservation schemes for wireless sensor networks can be identified, i.e. mobility-based, data-driven, and duty cycling schemes [68]. Depending on the application, the sensor nodes in a network can be placed far away from each other. In order to reach the sink, the data collected by the most distant nodes are sent to intermediate ones, according to a routing scheme. Thus, some routing paths can be more loaded than others, resulting in some sensor nodes (e.g. the ones near to the sink) being more active than others. In *mobility-based* schemes, mobile sinks are used to evenly distribute the sensor nodes' power consumption [91], [92].

Data-driven schemes consist of data reduction and energy-efficient data acquisition techniques [68]. Data reduction techniques reduce the sensor nodes' power consumption by implementing data compression, data prediction, and in-network processing schemes [93]. In data compression schemes, data are typically encoded at the sensor nodes, and decoded at the sink [94]. This results in less power consumption for the transmission of information. In data prediction schemes, the sensor nodes and the sink implement a model describing the sensed phenomena [95], [96]. Depending on the accuracy of the measured data with respect to the model prediction, less amount of data is transmitted to the sink, i.e. the sink does not need the exact data because of the predicted values. Regarding in-network processing techniques, data aggregation is performed at intermediate nodes in order to reduce the amount of data transmitted to the sink. Instead, energy-efficient data acquisition techniques are mostly based on adaptive sampling (e.g. by means of spatio-temporal correlation) and hierarchical sampling (e.g. by establishing an acquisition hierarchy among the various sensors in a node) [97], [98]. Regarding *duty cycling* techniques, they are divided in topology control and power management schemes. In topology control

schemes, the network redundancy is exploited in order to adaptively maintain active only a minimum number of sensor nodes. The criteria used to determine which subset of nodes should be active are based on location and connectivity [99], [100]. Power management schemes mostly consist of wake-up/sleep protocols. As mentioned in the introduction (Chapter 1.3.2), a typical approach consists in powering off the nodes as often and as long as possible, so that the communication between any two nodes takes place only when they are both on. The protocol through which two nodes communicate is called *rendezvous* [69]. Three main rendezvous protocols can be identified, i.e. pure synchronous, pseudo-asynchronous and pure asynchronous protocols. In a pure synchronous rendezvous scheme, the sensor nodes are presynchronized to turn on during specific time slots [70]. This scheme, which is mostly used by duty cycled Medium Access Control (MAC) protocols, is more energy-efficient with respect to an always-on approach. Nevertheless, it suffers from idle listening (i.e. nodes are on when no communication is required) and overhearing (i.e. a node receives data not intended to it) [101]. In pseudo-asynchronous rendezvous schemes, the nodes are still activated during specific time slots, but communication takes place according to a beaconing approach, i.e. a preamble signal is used to indicate the willingness to communicate [50], [102]. Although more energy-efficient that pure synchronous schemes, this approach still suffers from power consumption due to the required periodic activation. The third rendezvous scheme is the pure asynchronous one. Under this approach, the sensor nodes integrate an auxiliary receiver in their architecture, i.e. a wake-up receiver (Fig.1.4). In a typical scenario, the sensor nodes are normally in sleep mode, i.e. the processing unit is in low power mode and the communication unit is off [103]–[105]. Whenever communication is required, a wake-up call signal is transmitted to a targeted node. Upon correct detection of the WuC signal by the WuRx, the sensor node is woken up and communication takes place [70]. The implementation of WuRxs solves idle listening and overhearing issues since communication takes place only on demand. On the other hand, it implies additional hardware components, which can be costly depending on the implemented technology and the number of nodes. Nevertheless, the WuRx-based approach represents one of the most energy-efficient rendezvous scheme for the optimization of the power consumption in wireless sensor networks [106].

As for wireless sensor networks, on the basis of the application, three main types of WuRxs can be implemented, i.e. RF-based, optical and acoustic WuRxs [71], [107]–[116]. Terrestrial wireless sensor networks typically employ RF-based WuRxs due to the higher

data rate and lower latency with respect to the acoustic ones. However RF-based WuRxs are not suitable for the detection of signals underwater or intra-body due to higher attenuation [108], [117]. Acoustic WuRxs are characterized by lower data rate and higher latency with respect to RF-based and optical solutions. Nevertheless, they are less affected by attenuation underwater [118]. Optical WuRxs are typically more energy-efficient with respect to RF-based and acoustic WuRxs, but they suffer from line-of-sigh requirements [112]. Nevertheless, different solutions have been proposed to improve underwater optical WuRxs [119]–[121]. However, acoustic solutions are still considered the reference technology for UWSNs [122].

The majority of the proposed acoustic WuRxs are designed for non-underwater applications, although also solutions for UAWSNs have been proposed. In 2008, Khan et al. proposed an underwater acoustic modem which incorporates a 100 µA WuRx for the detection of wake-up call signals at 18 kHz, with a supply voltage (V_{dd}) of 5 V [123]. In 2011, Yadav et al. proposed an amplifier-based WuRx for air applications, which is fabricated in CMOS 65 nm and it consumes 4.4 µW ($V_{dd} = 0.6$ V) at 41 kHz [124]. In 2012, Sánchez et al. realized an underwater acoustic modem which makes use of commercial piezoelectric transducers and a commercial WuRx (AS3933), consuming 2.7 µA ($V_{dd} = 3.3$ V) with a data rate of 1 kbit/s and carrier frequency 85 kHz [125]. In 2013, Lattanzi et al. proposed a comparator-based ultrasonic wake-up receiver for air applications which consumes 874 nA ($V_{dd} = 2$ V) at 40 kHz [126]. In 2014, Höflinger et al. proposed a WuRx architecture for home applications, based on commercial MicroElectroMechanical System (MEMS) microphone and WuRx (AS3933), which consumes 56 µW ($V_{dd} = 3$ V) at 18 kHz [127]. In 2015, Bannoura et al. improved the WuRx in [127] by considering filtering for noise cancellation. The system consumes 140 µA when decoding a 20 kHz signal, and 15 µA in sleep mode ($V_{dd} = 3$ V) [128]. In 2017, Fuketa et al. proposed a Colpitts oscillator-based WuRx for IoT applications, which is fabricated in CMOS 250 nm and it consumes 1 µW ($V_{dd} = 0.3$ V) with a data rate of 250 bit/s [129]. In 2018, Oletic et al. implemented a 3-channel acoustic wake-up interface for underwater applications, which consumes 19.4 µA ($V_{dd} = 1.8$ V) at approximately 2 kHz [130], [131]. In 2019, Pop et al. proposed a Piezoelectric Micromachined Ultrasonic Transducer (pMUT) array-based wake-up receiver for intra-body links, consuming only 1 µA when receiving a 700 kHz signal [108]. In the same year, Rekhi and Arbabian demonstrated a wake-up receiver fabricated in CMOS 65 nm, which makes use of precharged transducers, and it is characterized by a power consumption of

8 nW (V_{dd} = 0.5 V) at 57 kHz [116]. To the best knowledge of the author, the WuRx in [116] represents the State-of-the-Art acoustic wake-up receiver for non-underwater applications. Instead, the WuRx in [125] represents the State-of-the-Art acoustic wake-up receiver for underwater applications.

In this work, an acoustic wake-up receiver for underwater application with power consumption of 265 nW (V_{dd} = 2 V) at 40 kHz has been experimentally validated [5]. The proposed WuRx overcomes, in terms of performance, the wake-up receiver in [125]. Furthermore, a 7.2 nW (V_{dd} = 2 V) WuRx has been proposed at simulation level in [3]. Therefore, the designed WuRxs present State-of-the-Art power consumption.

2.2 Proposed Architectures

In this section, first simplified block diagrams of the proposed WuRx architectures are described. Next, the circuit implementations are discussed. As previously reported (Chapter 1.4), three types of WuRx architectures have been proposed in this work, i.e. inverter-based (2 circuit implementations), multivibrator-based (3 circuit implementations) and oscillator-based (1 circuit implementation). The inverter-based and multivibrator-based WuRx architectures present similar decoding mechanisms, while that of the oscillator-based WuRx is completely different. In the following, it is assumed that the WuC signal consists of a sequence of sinusoidal bursts, and that the presence of a burst is associated to a high logic level (i.e. '1') while its absence to a low one (i.e. '0') [132]. Furthermore, it is assumed, for simplicity, that the duration of the '1's is equal to that of the '0's, i.e. the duty cycle of the WuC signal is 50 %. Nevertheless, the proposed decoding mechanisms work for lower as well higher duty cycles.

From a block diagram point of view, the inverter-based and multivibrator-based WuRxs can be described with the simplified architecture shown in Fig.2.1(a), where it is assumed, for explanatory purposes, that the WuRx is designed to decode the WuC signal '101'. As can be observed, the architecture is composed of four main blocks, i.e. rectification, pulse, switch, and logic gate blocks. The rectification block is used to rectify the bursts of the WuC signal, i.e. the sequence of bursts (S_{WuC}) is converted to a sequence of pulses (S_{rect}), as shown in Fig.2.1(b). As soon as the first rectified burst reaches the first pulse block (Pulse 1), a reference pulse signal (S_{ref_1}), which is longer than the first rectified burst, is

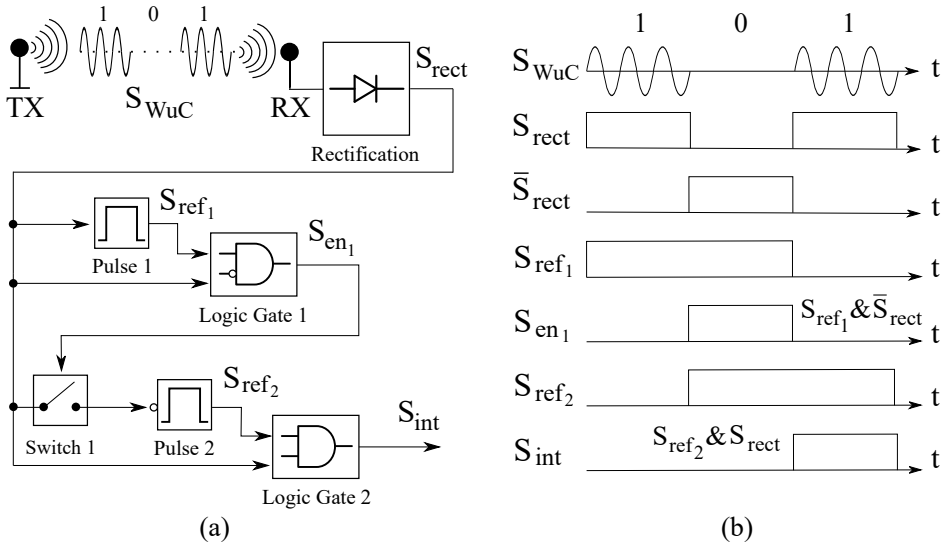


Figure 2.1: (a) Simplified block diagram and (b) ideal waveforms describing the behavior of the inverter-based and multivibrator-based WuRx architectures when decoding the WuC signal '101'.

generated. The proposed inverter-based and multivibrator-based WuRxs decode the logic levels in the WuC signal by comparing, through the logic gate blocks, the amplitude and duration of the reference pulses with those of the rectified bursts. Therefore, in order to decode the '0' in the WuC signal, the first logic gate should implement the logical AND operation between the inverted first rectified burst and the first reference pulse, i.e. $\overline{S}_{rect}\&S_{ref_1}$. In case of correct detection, the output of the first logic gate (S_{en_1}) enables, through the block Switch 1, the connection between S_{rect} and the successive pulse block (Pulse 2). Next, the inverted rectified burst is used to trigger Pulse 2, which generates a reference pulse (S_{ref_2}) aligned with the last '1' in the WuC signal. To detect the last '1', the second logic gate should implement the logical AND operation between S_{ref_2} and S_{rect}, i.e. $S_{rect}\&S_{ref_2}$. If this occurs, the output of Logic Gate 2 goes high, and the interrupt signal (S_{int}), which wakes up the sensor node, gets asserted. Longer wake-up call signals can be decoded by simply cascading switch, pulse and logic gate blocks. The '1's ('0's) are decoded by comparing the reference signals with the (inverted) rectified bursts. The proposed decoding mechanism is simple, and intrinsically energy-efficient since the activation of the blocks is fully sequential, i.e. in case of wrong logic level detection the successive blocks are not activated. It should be pointed out that the block diagram in Fig.2.1(a) is a simplified description of the proposed architectures, which does not accurately describe the actual behavior of all the designed WuRxs. The difference between the inverter-based and multivibrator-based WuRxs lies on the circuit implementation of

the pulse blocks, which has important consequences on the generation of the reference pulse signals, as it will be explained when discussing each specific WuRx. Nevertheless, the block diagram in Fig.2.1(a) correctly describes the main decoding mechanism concept common to both architectures.

Regarding the oscillator-based WuRx, a simplified block diagram describing its architecture is shown in Fig.2.2(a), where it is assumed again, for explanatory purposes, that the WuC signal is '101'. The oscillator-based WuRx is composed of six main blocks, i.e. rectification, pulse extractor, oscillator, counter, switch, and logic gate blocks. First, the wake-up call signal is rectified. Next, the pulse extractor extracts the pulses $S_{1,2,3}$. The duration of S_1 is equal to that of the first '1' in the WuC signal, while the durations of S_2 and S_3 are equal to those of the '0' and the second '1', respectively. In order to decode the first '1', the WuRx employs an oscillator in conjunction with a counter. In the following, it is assumed that for a correct logic level detection, the counters have to count

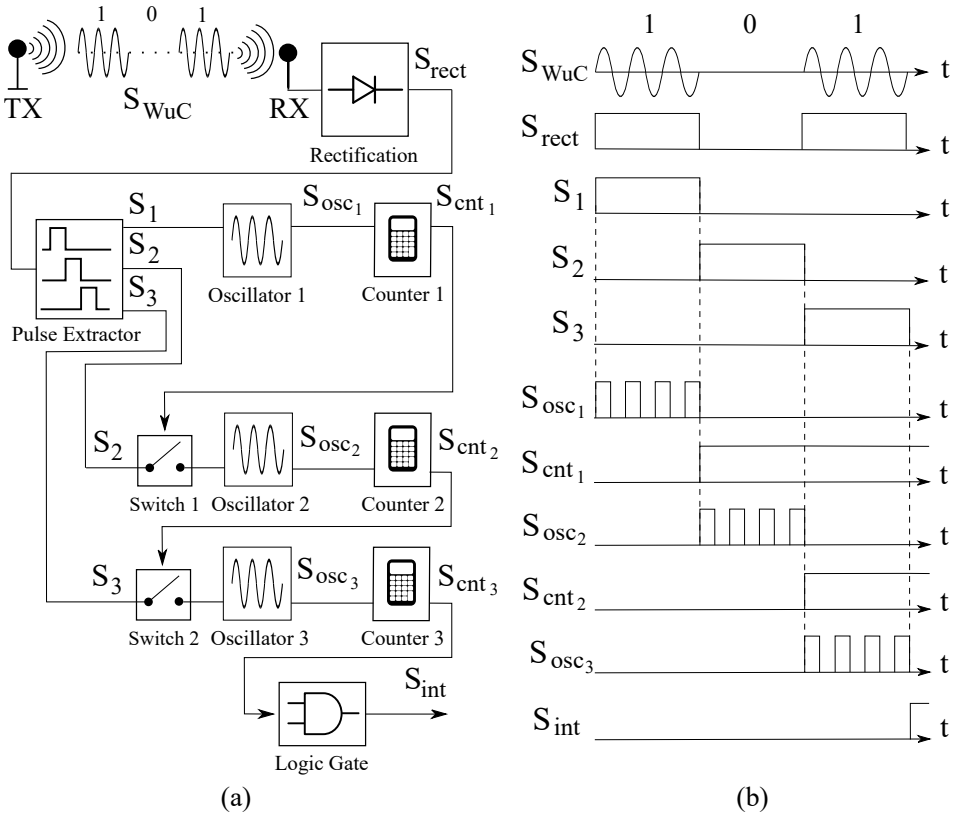


Figure 2.2: (a) Simplified block diagram and (b) ideal waveforms describing the oscillator-based WuRx architecture when decoding the WuC signal '101' with a counting parameter equal to four.

four oscillations per logic level. As can be observed in Fig.2.2(b), as soon as Oscillator 1 oscillates four times (S_{osc_1}), the output of Counter 1 (S_{cnt_1}) goes high. So the block Switch 1 enables the connection between the second extracted pulse (S_2) and Oscillator 2, which in conjunction with Counter 2 verifies that exactly four oscillations occur during the '0' in the WuC. The same reasoning applies for the successive stage: in case in which the second '1' is correctly measured, finally Logic Gate generates the interrupt signal S_{int}. The block Pulse Extractor is necessary for the measurement of the '0's. As for the inverter-based and oscillator-based WuRxs, the decoding mechanism is sequential. The oscillator-based WuRx is more accurate since it also measures the duration of the first '1' in the WuC signal, while the inverter-based and multivibrator-based WuRxs use the first '1' only as a trigger for the block Pulse 1. On the other hand, the oscillator-based WuRx generates an interrupt signal not aligned with the WuC, as can be observed in Fig.2.2(b). It should be pointed out that the presented architecture represents a simplified description of the actual oscillator-based WuRx, which is far more complex, as it will be shown in the following. Nevertheless, the block diagram in Fig.2.2(a) correctly describes its decoding mechanism concept.

It should be now clear that the proposed architectures can also be implemented for RF-based and non-underwater (i.e. acoustic in air) applications since the decoding mechanisms simply require rectified pulses as input signals.

2.2.1 Inverter-Based

The first proposed inverter-based wake-up receiver was the so called *delay-based* WuRx [1]. This circuit is the first one to report the novel decoding mechanism based on the sequential verification of the WuC signal (Fig.2.1). The block Pulse has been implemented with the circuit shown in Fig.2.3. The reason for which the WuRx in [1] has been called *delay-based* relies on the reference signal generation mechanism. Referring to Fig.2.3, assuming that V_{rect} and V_{sw} are initially high, and so that the switch $M_{n,sw}$ is initially closed, the active load implemented through $M_{p,act}$ would result on. As a consequence, a voltage (V_C) will result across the RC group. This voltage is then *delayed* through the inverter-based buffer in order to obtain a voltage (V_{ref}) high during the next logic level. Once the delayed signal goes low, V_{sw} turns off the active load through $M_{p,sw}$. The logic gate blocks are implemented through CMOS (N)AND gates, while the switch blocks through simple

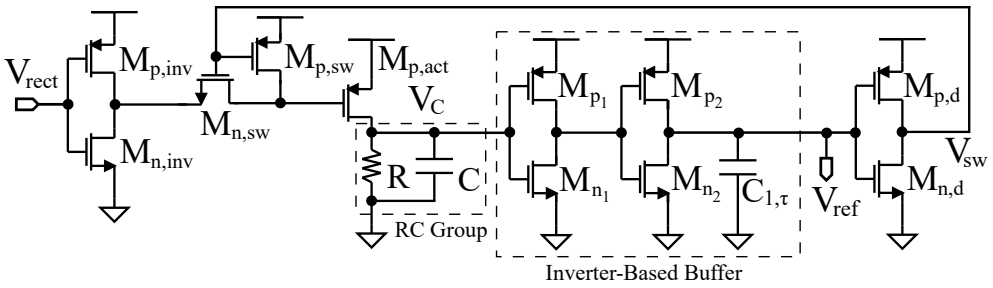


Figure 2.3: Circuit used by the delay-based wake-up receiver for the generation of a reference signal. Redrawn from [1]. ©2021 IEEE.

PMOS transistors. An example of full WuRx implementation is reported in the associated article (Appendix B.1) [1]. The circuit operation has been verified through simulations, by considering a TSMC-180nm CMOS process, and a 40 kHz burst frequency. The circuit consumes about 42 µW ($V_{dd} = 1.2$ V) for the detection of the WuC signal '1101', with each high (low) logic level having a duration of 3 ms (1.5 ms). An alternative idea could be to use a (tunable) Schmitt trigger in the buffer stage. A critical problem of the proposed circuit implementation is that in order to obtain delays in the millisecond range, relatively high capacitances are required in the buffer stage. Therefore, as designed in [1], the circuit is not suitable for ASIC integration.

This circuit has been then dramatically optimized, by designing the so called *Type A* WuRx [5]. This wake-up receiver has been experimentally validated through an ASIC designed in AMS-350nm CMOS process. Its block Pulse has been implemented through a tunable current starved inverter topology, shown in Fig.2.4. The capacitor has a value of 3 pF. The circuit is starved only on the PMOS side, in order to tune only the falling edge of the generated reference voltage. The logic gate blocks are implemented through CMOS AND gates, while the switch blocks through CMOS transmission gates (Appendix

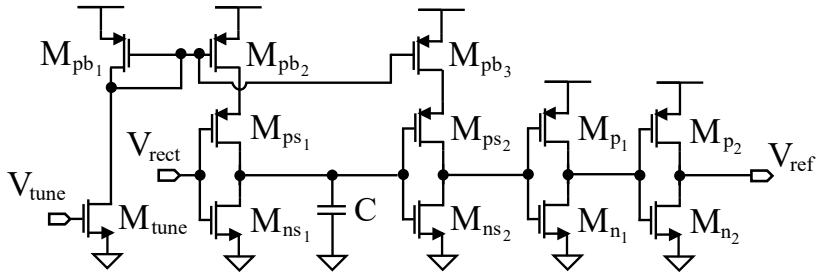


Figure 2.4: Current starved inverter-based circuit used by the *Type A* wake-up receiver for the generation of a reference signal. Redrawn from [5].

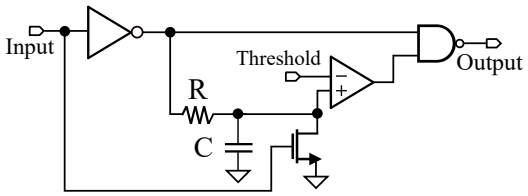


Figure 2.5: Simplified equivalent circuit associated to the circuit in Fig.2.4. Redrawn from [5].

B.5). An important feature of this circuit is that the duration of the reference voltage is a function of the rising and falling edges of the rectified voltage. This dependency can be better understood through the simplified equivalent circuit of the block Pulse of *Type A*, shown in Fig.2.5. When the input (i.e. V_{rect}) goes high, the capacitor is shorted and the output (i.e. V_{ref}) is high. Once the input goes low, the output goes low according to a time set by the RC group and by the threshold of the inverter composed by $M_{n(p)s_2}$ in Fig.2.4. In the associated article [5], the pulse blocks of *Type A* are called monostable circuits, because they produce a single output pulse when they are triggered at their inputs. Typically, the duration of the output of a monostable circuit is not dependent on the duration of the input signal. Nevertheless, it has been decided to keep this definition while describing the circuit in Fig.2.4 in the associated article. On the basis of the this definition, one can argue that *Type A* should be considered a multivibrator-based WuRx and not an inverter-based one. However, when focusing on a single block Pulse, the reference voltage results to be generated through a current starved inverter topology. In other words, the block Pulse of *Type A behaves* as a monostable circuit when considering it as a black box. But in terms of actual circuit implementation, it uses a current starved inverter topology. Although both the delay-based and *Type A* WuRxs use CMOS inverters for the generation of the reference voltage, their behavior is quite different. In Fig.2.6, their reference voltages (S_{ref_1}) when decoding the WuC signal '101' are shown. As can be observed, the reference voltage of the delay-based WuRx is not aligned with the rising edge of the rectified burst. This is due to the CMOS buffer stage, which *delays* the voltage V_C generated by the RC group in Fig.2.3. Instead, the reference voltage of *Type A* is aligned with the rising edge of the rectified burst, and it stays high for all the duration of the WuC signal. As explained in detail in [5], this is due to the capacitor in Fig.2.4: the output of the block Pulse 1 does not go low because the second rectified burst does not allow the capacitor to be fully charged and cross the threshold of the inverter. As can

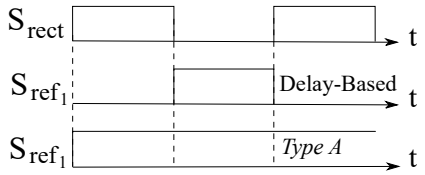


Figure 2.6: Ideal reference voltages of block Pulse 1 of the delay-based and *Type A* WuRxs when decoding the WuC signal '101'.

be observed, the waveforms associated to the simplified block diagram in Fig.2.1 are not totally coherent with those in Fig.2.6. However, both circuit implementations decode the WuC signal by generating a reference voltage which is high during the comparison with the logic levels.

In the associated article (Appendix B.5) [5], *Type A* has been extensively characterized in terms of tuning, duty cycle, and power consumption. When decoding the WuC '10101' (logic level duration equal to 500 µs) the measured power consumption is 0.7 µW (V_{dd} = 2 V). Instead, when the logic level duration is equal to 4 ms, the measured power consumption is 0.27 µW (V_{dd} = 2 V). *Type A* presents the lowest power consumption reported for an underwater acoustic wake-up receiver. The layout and the micrograph of *Type A* are shown in Appendix A.2.1.

2.2.2 Multivibrator-Based

Three different circuit implementations of the multivibrator-based WuRx architecture have been proposed. In the first one, the block Pulse has been implemented with the NOR-based multivibrator, shown in Fig.2.7(a) (Appendix B.2) [2]. This is the first *multivibrator-based* WuRx proposed. The circuit has been simulated by considering a TSMC-180nm CMOS process, and a 40 kHz burst frequency. The circuit consumes about 0.8 µW (V_{dd} = 1.2 V) for the detection of the WuC signal '1001', with each logic level having a duration of 1.5 ms. The capacitances are in the order of 20 pF, thus not resulting suitable for ASIC integration. The second circuit implementation is based on a *single transistor*, and it is shown in Fig.2.7(b) (Appendix B.3) [3]. As can be observed, two transistors are present. However, transistor M_{sw} acts as a simple switch. The circuit consumes about 32.8 nW (V_{dd} = 1.2 V) for the detection of the WuC signal '101', with each logic level having a duration of 1.5 ms. When decoding eleven logic levels ('10101010101'), the

circuit consumes 153 nW. When lowering the supply voltage to 0.6 V, the power consumption lowers to 7.2 nW. This WuRx overcomes, at simulation level, the performance of the State-of-the-Art device presented in [116], i.e. it presents the lowest power consumption reported for an acoustic wake-up receiver. The last circuit implementation is that of the so called *Type B* wake-up receiver, presented in [5] (Appendix B.5). The block Pulse has been implemented through a tunable NOR-based multivibrator, shown in Fig.2.7(c). The circuit is an optimized version of the circuit reported in [2] (Fig.2.7(a)). The architecture of *Type B* is more complex than that of the other multivibrator-based WuRxs. In fact, *Type B* has an extra block, called Control, which prevents the various pulse blocks to be unnecessarily triggered during the decoding phase, as explained in detail in Appendix B.5. Together with *Type A*, *Type B* has been experimentally validated through an ASIC designed in AMS-350nm CMOS process, and extensively characterized in terms of tuning, duty cycle, and power consumption. The layout and the micrograph of *Type B* are shown

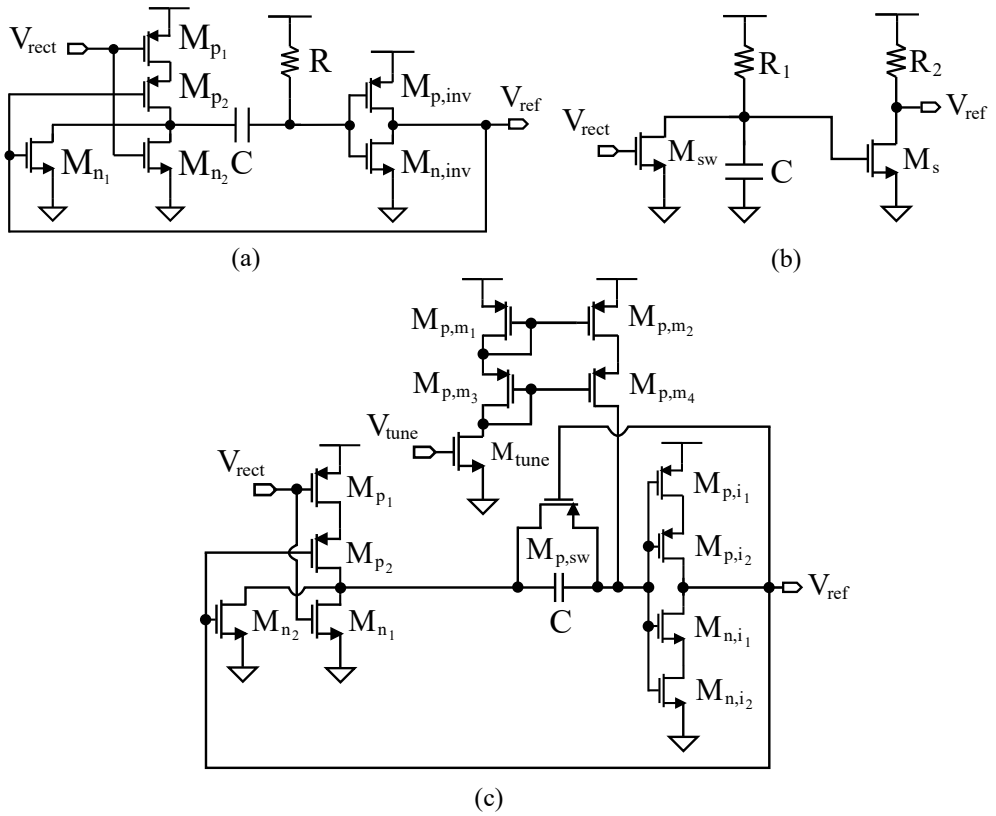


Figure 2.7: Circuit implementations of the block Pulse of the multivibrator-based WuRx architectures: (a) NOR-based multivibrator, redrawn from [2] ©2021 IEEE; (b) Single transistor, redrawn from [3] ©2022 IEEE; (c) optimized tunable NOR-based (*Type B*), redrawn from [5].

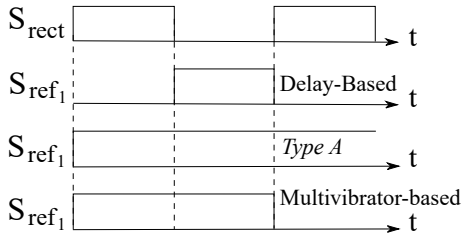


Figure 2.8: Ideal reference voltages of block Pulse 1 of the delay-based, *Type A* and multivibrator-based WuRxs when decoding the WuC signal '101'.

in Appendix A.2.2. Its performance is similar to that of *Type A*. When decoding the WuC '10101' (logic level duration equal to 500 µs) the measured power consumption is 0.98 µW ($V_{dd} = 2\,\mathrm{V}$). Instead, when the logic level duration is equal to 4 ms the measured power consumption is 0.46 µW ($V_{dd} = 2\,\mathrm{V}$). An important difference between the pulse blocks of *Type A* and *Type B* relies on the dependence of the reference voltage on the rectified burst. While the output of the block Pulse of *Type A* is dependent on the rising and falling edges of the rectified burst, that of *Type B* only depends on the rising edge. This is due to the fact that the duration of the output voltage of the multivibrators of *Type B* is determined by their RC groups only since the rectified burst only acts as a trigger signal. Instead, in *Type A*, the duration of the rectified burst also affects the (dis)charging process of the capacitor in its Pulse block (Fig.2.5). In Fig.2.8, the ideal reference voltages of the multivibrator-based WuRxs are shown, together with those of the delay-based and *Type A* WuRxs. A detailed comparison between *Type A* and *Type B* is reported in the associated article (Appendix B.5) [5].

2.2.3 Oscillator-Based

The oscillator-based WuRx presents the most complex architecture among the proposed wake-up receivers (Appendix B.4) [4]. A general architecture is shown in Fig.2.9. As can be observed, it is composed of different *Pulse Meters*. These blocks are in charge of decoding the pulses extracted by the WuC signal by measuring their durations. Each pulse meter has one oscillator, two counters, a switch, a logic gate, and a one shot monostable. The first pulse meter does not have a logic gate since it is triggered by the first extracted pulse, while the last one has an additional one shot and logic gate for interrupt signal generation. In each Pulse Meter, the first counter (e.g. Counter 1 of P_1 in Fig.2.9) verifies that exactly M oscillations occurs, where M is the number of oscillations required for

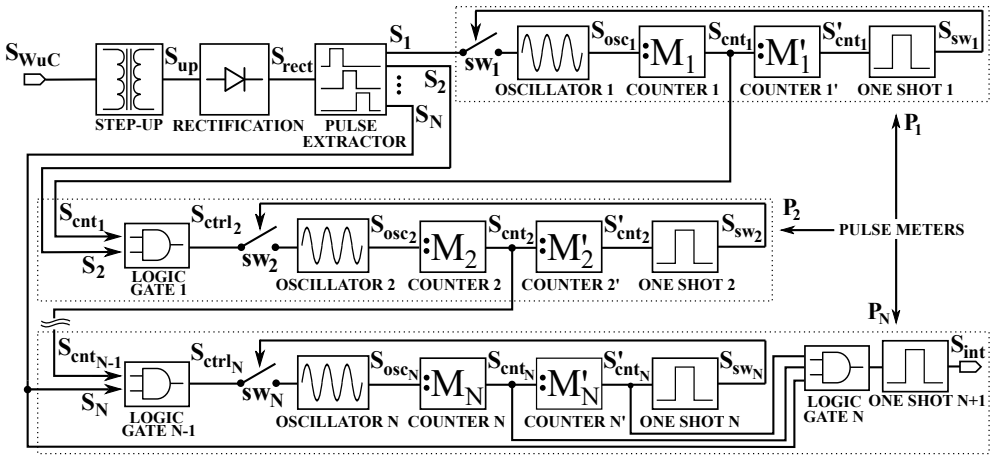


Figure 2.9: General architecture of the proposed oscillator-based WuRx. Redrawn from [4] ©2021 IEEE.

a correct logic level detection. The second counter (e.g. Counter 1'), in conjunction with the adjacent block One Shot, is used to decouple the oscillator (e.g. Oscillator 1), through a switch (e.g. sw_1), from the block Pulse Extractor in case in which more than M oscillations occur. In other words, the second counter of each pulse meter prevents the oscillator to consume unnecessary power in case in which a wrong logic level is received. If exactly M oscillations occur, a logic gate block allows the successive extracted pulse to be measured by the successive pulse meter, i.e. the decoding mechanism is sequential. A circuit implementation with $M = 2$ has been validated through simulations in TSMC-180nm CMOS process. The oscillator has been implemented through a simple current starved ring oscillator, while the counter through a cascaded divide-by-2 CMOS counter. All the circuits are reported in [4] (Appendix B.4). The simulated circuit implementation is not optimized in terms of power consumption. It consumes 16.1 µW ($V_{dd} = 1.2$ V) when decoding the WuC signal '101', with each logic level having a duration of 0.5 ms. No further optimization has been performed since the performance of the multivibrator-based WuRxs was more promising during the design phase.

2.3 Conclusions

Three types of WuRx architectures have been proposed, i.e. inverter-based, multivibrator-based, and oscillator-based. The inverter-based makes use of CMOS inverters for the generation of the reference signals used for decoding the WuC signal. Two implement-

ations have been proposed. In the first one, i.e. the delay-based WuRx, the reference voltages are generated through buffered CMOS inverters. In the second one, i.e. *Type A*, a tunable current starved topology is employed to generate the reference voltages. *Type A* represents, at the time of writing, the State-of-the-Art acoustic WuRx for underwater applications. Its performance has been experimentally measured through an ASIC in AMS-350nm CMOS process.

Regarding the multivibrator-based WuRxs, three different circuit implementations have been proposed. The first one uses a NOR-based multivibrator, while the second one uses a single transistor. The NOR-based multivibrator-based WuRx has been optimized by experimentally prototyping the *Type B* WuRx, which presents State-of-the-Art power consumption, together with *Type A*. Therefore, it has been also demonstrated that a low technological node is not necessarily required for low power implementation since State-of-the-Art performance has been achieved. The implementation based on a single transistor represents, at simulation level, the State-of-the-Art acoustic WuRx in terms of power consumption.

Finally, also an oscillator-based WuRx has been proposed. However, the proposed circuit implementation does not overcome the performance of *Type A* and *Type B*. The future directions are reported in the overall conclusions of the dissertation (Chapter 4) since they are dependent on results presented in the next chapter, where the contributions about Schmitt trigger circuits are reported.

3 Schmitt Triggers

3.1 Background[1]

In 1937, Otto H. Schmitt invented a trigger circuit, which was initially intended to emulate a synthetic nerve [133]. One year later, he invented a thermionic trigger [134], then renamed as *Schmitt trigger* (ST) [135]. Although the circuit was initially intended for biomedical applications, nowadays STs are employed in various electronic systems. For instance, they are used in waveform generators and oscillators [136]–[142], SRAMs and latches [82], [143]–[149], timers and receivers [150]–[153], converters [154]–[161], and various sensor interfaces [162]–[168]. Therefore, they find applications in digital and analog systems.

As reported in the introduction (Chapter 1.3.2), recently researchers focused on the analysis and modeling of ST circuits in subthreshold region, due to the increasing demand of low power electronics [83]–[85]. In 2007 Kulkarni et al. implemented an SRAM cell through a simplified version of the classical CMOS ST shown in Fig.3.1(b) [169]. The feedback is present only on the pull-down branch since the pull-up one is used to hold the '1' state in the considered SRAM cell. In 2012, Lotze and Manoli demonstrated that Schmitt trigger logic can allow operation at low supply voltage ($< 63\,\text{mV}$) [170]. Instead, in 2017 they extended their analysis by providing a systematic study of Schmitt trigger gates operated in subthreshold region [84]. In 2017, Melek et al. analytically modeled the DC transfer characteristic of the classical CMOS Schmitt trigger shown in Fig.3.1(a) [85]. Furthermore, they determined the minimum supply voltage (75 mV at room temperature) for which hysteresis can be observed. In 2018, Melek et al. extended their analysis by considering the Schmitt trigger operated in amplifier mode, and they compared its performance with that of the classical CMOS inverter [171]. They demonstrated that

[1] Part of this section previously appeared in [8].

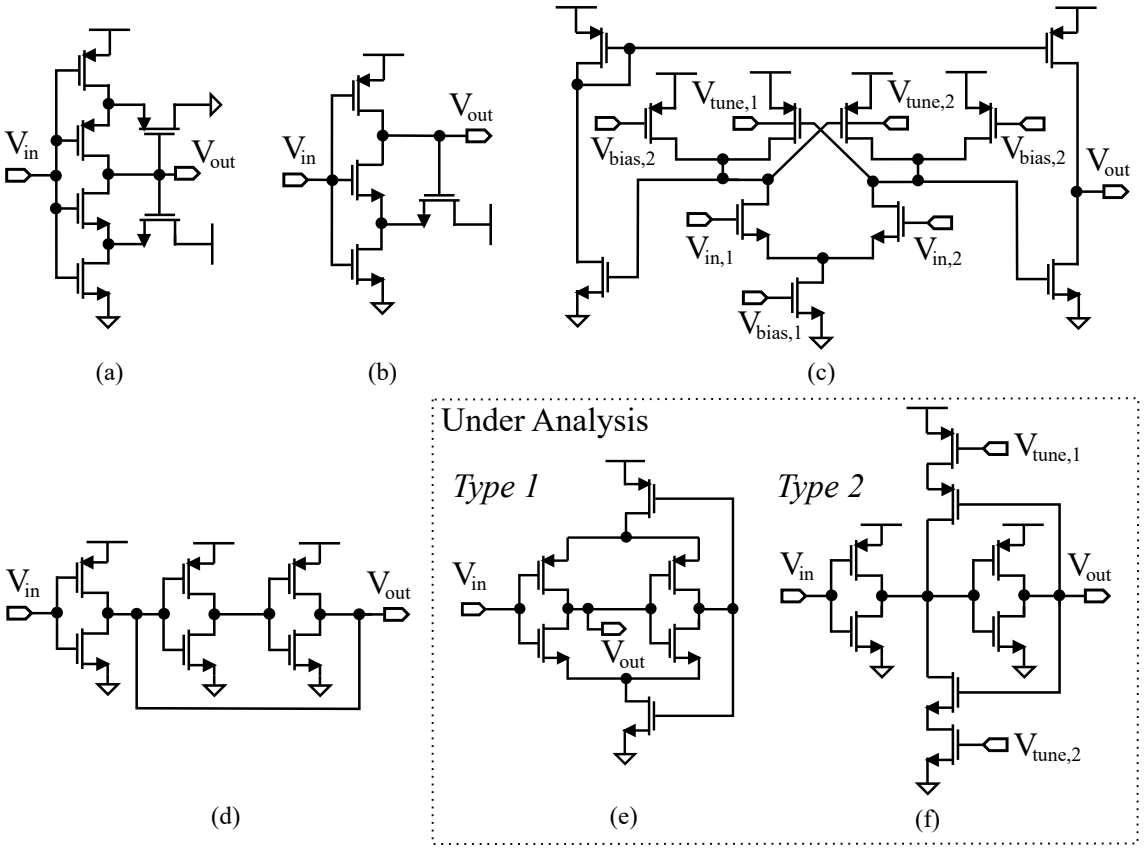


Figure 3.1: (a) Classical 6-transistor CMOS ST analyzed in [85]. (b) Modified classical CMOS ST analyzed in [169]. (c) Differential CMOS ST analyzed in [173]. (d) 3-inverter CMOS ST analyzed in [175]. (e) Al-Sarawi's ST circuit [86], analyzed in this work. (f) Wang's ST circuit [88], analyzed in this work. The bulk terminal connections are not shown for simplicity.

the ST can work with a supply voltage lower than 32 mV (at 300 K), while the limit of the standard CMOS inverter is above 35 mV. Bastan et al. proposed in 2020 a differential CMOS Schmitt trigger, which presents a power consumption of 150 nW when driven by 0.4 V [172]. In the same year, Radfar et al. proposed a differential tunable CMOS Schmitt trigger, shown in Fig.3.1(c) [173]. The circuit consumes less than 1.4 µW, and is characterized by a tuning range of approximately 110 mV. In 2021, Nejati et al. reported a 120 nW differential CMOS Schmitt trigger [174]. In the same year, Fernandes et al. presented an analysis in subthreshold region of the 3-inverter CMOS ST shown in Fig.3.1(d) [175]. They implemented an oscillator which is supplied by less than 63 mV. One year later, Sandiri et al. reported an analysis of Schmitt trigger gates by considering Dynamic Threshold MOS (DTMOS) technique in subthreshold region [176].

In this thesis, the subthreshold characteristics of two ST circuits have been modeled and

analyzed: the low power CMOS ST proposed by Al-Sarawi (renamed here as *Type 1*, Fig.3.1(e)) in 2002 [86], and the tunable single input CMOS ST proposed by Wang (renamed here as *Type 2*, Fig.3.1(f)) in 1991 [88]. Among the single input STs, *Type 1* presents one of the best figure of merits [87], while *Type 2* is the first single input tunable CMOS ST modeled in subthreshold region. For both circuits, analytical expressions for the high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages, which define the hysteresis width ($V_H = |V_{HL} - V_{LH}|$), have been determined. The derived expressions relate the hysteresis width to the dimensions of the transistors, the supply voltage, and the temperature. Therefore, they allow performance optimization in subthreshold region by relating physical parameters to the characteristics. The derived expressions are based on the Enz-Krummenacher-Vittoz (EKV) model [177], [178], and they have been validated with simulations and experiments, by prototyping an ASIC in AMS-350nm CMOS process. Although validation has been performed with a quite old technological node, the considered EKV model has been used to model STs in CMOS 180 nm [175], and to investigate the operation of circuits realized in lower technological nodes (e.g. 90 nm and 65 nm) [179], [180].

As reported in the introduction (Chapter 1.4), from the analysis of *Type 1* and *Type 2*, three articles have been produced: regarding *Type 1*, the analytical model has been first proposed and validated through simulations and experiments (Appendix C.1) [6], and next it has been further analyzed by considering different designs, simplified equivalent circuits and power consumption (Appendix C.2) [7]; regarding *Type 2*, its analytical model has been proposed and validated through simulations and experiments by also considering supply voltage, temperature and process variations (Appendix C.3) [8]. In the following subsection the used EKV model is reported. Next, the main results regarding *Type 1* and *Type 2* are reported.

3.1.1 EKV Model

In subthreshold region [177], [178], the drain current can be expressed as

$$I_{d,n(p)} = I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}} \cdot \left(e^{-\frac{V_{SB(BS)}}{\phi}} - e^{-\frac{V_{DB(BD)}}{\phi}} \right) \tag{3.1}$$

where:

$$I_{0,n(p)} = 2 \cdot n_{n(p)} \cdot \mu_{n(p)} \cdot C_{ox} \cdot \frac{W}{L} \cdot \phi^2 \cdot e^{-\frac{|V_{th,n(p)}|}{n_{n(p)} \cdot \Phi}} \tag{3.2}$$

- B, G, S and D refer to the bulk, gate, source and drain terminals, respectively;
- $n_{n(p)} \rightarrow$ NMOS (PMOS) slope factor;
- $\phi \rightarrow$ thermal voltage ($k_B T/q$);
- $\mu_{n(p)} \rightarrow$ electron (hole) mobility;
- $C_{ox} \rightarrow$ oxide capacitance;
- $W/L \rightarrow$ transistor width to length ratio;
- $V_{th,n(p)} \rightarrow$ NMOS (PMOS) threshold voltage.

The drain-source voltage contribution in (3.1) can be neglected when transistors are in saturation ($|V_{DS}| \geq 3 \cdot \phi$ [181]). This results in the following approximated drain current expression:

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)} - n_{n(p)} \cdot V_{SB(BS)}}{n_{n(p)} \cdot \phi}}. \tag{3.3}$$

Furthermore, if the bulk-source voltage is equal to zero volts, (3.3) can be simplified as

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}}. \tag{3.4}$$

The current scaling factor $I_{0,n(p)}$ is mainly dependent on the W/L ratio. The subthreshold swing ($S_{n(p)}$) can be defined as the change in the gate voltage required to obtain a change of one decade in the subthreshold drain current. The slope factor ($n_{n(p)}$) can be related to the subthreshold swing through [182]:

$$S_{n(p)} = ln(10)\frac{k_b T}{q}\left(1 + \frac{C_{dep,n(p)}}{C_{ox}}\right) = ln(10)\frac{k_b T}{q} n_{n(p)} \tag{3.5}$$

where $C_{dep,n(p)}$ is the depletion layer capacitance. The extracted values are $n_n = 1.25$ and $n_p = 1.3$.

3.2 Type 1

Type 1 is a single-input single-output inverting voltage mode CMOS ST proposed by Al-Sarawi in 2002 [86]. The circuit, its symbol and its characteristics are shown in Fig.3.2. A procedure to obtain the high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages in strong inversion is reported in [87]. The same methodology has been implemented in this thesis, but by considering transistors biased in weak inversion. In the following, the full derivation of V_{HL}, i.e. the input voltage at which the output goes from high to low, is reported. By *high* is meant the supply voltage V_{dd}, while by *low* the ground. Referring to Fig.3.3(a), when the input is low, the output is high due to the inverting topology. This results in M_3 being off, and M_4 on. As a consequence, M_5 is on and the voltage at the node $V_{m,p}$ is approximately V_{dd}, i.e. it is assumed that the on resistance of M_5 is negligible as shown in Fig.3.3(b). By *negligible* it is meant that during the transition the transistor can be considered a short circuit. Furthermore, it is assumed that the on resistance of M_4 is negligible as well. This results in M_6 being diode-connected. In strong inversion, M_6 would result in saturation since $V_{GS,6} = V_{DS,6}$. But in weak inversion, M_6 would be in saturation only if its drain-source voltage is at least three times the thermal voltage. The simplified equivalent circuit that approximates the circuit state before the high-to-low transition is shown in Fig.3.3(c). Moreover, it is assumed that all transistors are in saturation during the transition. The voltage V_{HL} can be determined by finding the switching voltage of the inverter composed of M_1 and M_2, considering the voltage $V_{m,n}$

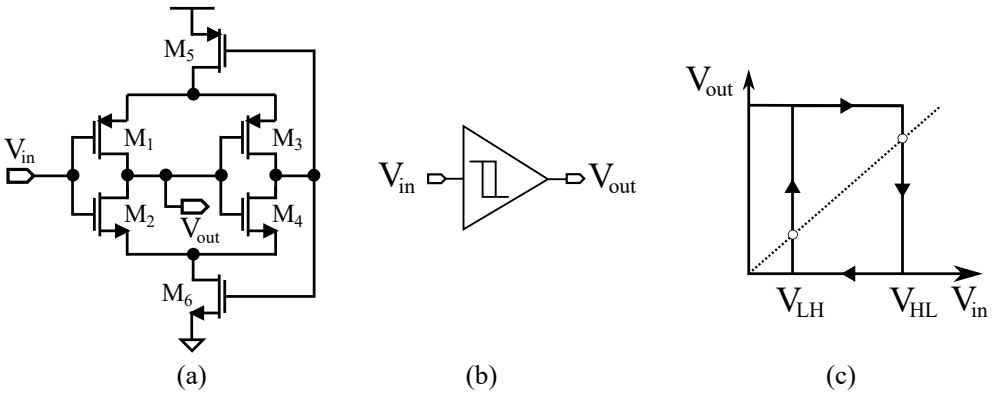


Figure 3.2: (a) *Type 1* circuit. (b) Inverting voltage mode Schmitt trigger symbol and (c) associated characteristics. Redrawn from [6] ©2022 IEEE.

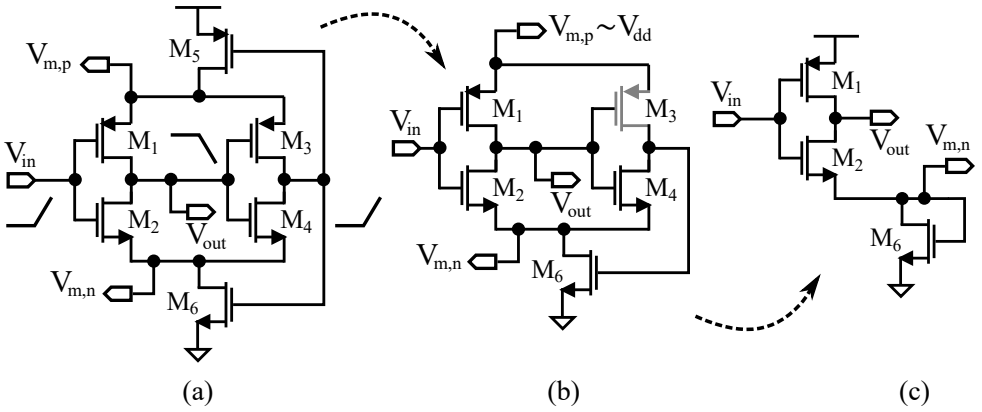


Figure 3.3: *Type 1 V_{HL}* analysis. (a) Circuit. (b) Assuming that the on resistance of M_5 is negligible. (c) Simplified equivalent circuit. Redrawn from [6] ©2022 IEEE.

across M_6. This translates into imposing:

$$I_{0,p1} \cdot e^{\frac{V_{dd}-V_{HL}}{n_p \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{HL}-n_n \cdot V_{m,n}}{n_n \cdot \phi}}. \tag{3.6}$$

To determine the unknown variable in (3.6), i.e. $V_{m,n}$, the following equation relating M_2 and M_6 is imposed:

$$I_{0,n6} \cdot e^{\frac{V_{m,n}}{n_n \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{HL}-n_n \cdot V_{m,n}}{n_n \cdot \phi}}, \tag{3.7}$$

$$V_{m,n} = \frac{V_{HL} + n_n \cdot \phi \cdot log\left(\frac{I_{0,n2}}{I_{0,n6}}\right)}{1+n_n}. \tag{3.8}$$

Finally by substituting $V_{m,n}$ in (3.6) and solving for V_{HL}, the following expression is obtained:

$$V_{HL} = \frac{n_n \cdot \left\{V_{dd} \cdot (1+n_n) - n_p \cdot \phi \cdot \left[log\left(\frac{I_{0,n2}}{I_{0,p1}}\right) + n_n \cdot log\left(\frac{I_{0,n6}}{I_{0,p1}}\right)\right]\right\}}{n_n^2 + n_n + n_p}. \tag{3.9}$$

As can be observed in (3.9), the high-to-low voltage is linearly dependent on the supply voltage and the temperature, and logarithmically dependent on the dimensions of M_1, M_2 and M_6. Therefore, the model is based on the assumption that M_5 and the second inverter (M_3 and M_4) do not influence the high-to-low transition voltage. The derivation of the low-to-high voltage (V_{LH}) is complementary, and it is reported in the articles (Appendices

C.1 and C.2) [6], [7]. The expression of V_{LH} is given by:

$$V_{LH} = \frac{n_n \cdot \left\{ V_{dd} - n_p \cdot \phi \cdot \left[n_p \cdot log\left(\frac{I_{0,n2}}{I_{0,p5}}\right) + log\left(\frac{I_{0,n2}}{I_{0,p1}}\right) \right] \right\}}{n_p^2 + n_p + n_n}. \tag{3.10}$$

Complementary to (3.9), V_{LH} depends on M_1, M_2 and M_5, i.e. it is assumed that M_6 and the second inverter (M_3 and M_4) do not influence the characteristics.

3.2.1 Simulation Results

As previously reported, the model is based on the assumptions that the on resistances of the second inverter (M_3 and M_4) are negligible during the transitions, and that M_5 (M_6) does not influence V_{HL} (V_{LH}). Therefore, it is expected that the model can more accurately describe the circuit behavior when these transistors are large, with respect to the minimum channel length. Two designs have been initially considered. In *Design 1*, the PMOS transistors are sized $2/0.5$ while the NMOS $1/0.5$. Instead in *Design 2* the PMOS transistors are sized $40/0.5$ and the NMOS ones $20/0.5$. The simulation parameters are reported in Table 3.1. The simulated V_{HL} has been extracted by performing a DC sweep of the input voltage from zero volts up to V_{dd}. The extraction of V_{LH} is complementary. The model has been validated against the supply voltage, by considering V_{dd} values ranging from 0.5 V to 0.6 V. For lower supply voltages, the circuit does not correctly work, i.e. no transition. When ($V_{dd} = 0.6$ V), M_2 still operates in subthreshold region since $V_{m,n}$ is approximately 100 mV. To quantitatively compare the analytical and simulated values

Table 3.1: *Type 1* Simulation Parameters.

Parameter	***Design 1***	***Design 2***
	Value	**Value**
L	0.5 µm	0.5 µm
$W_{2,4,6}$	1 µm	20 µm
$W_{1,3,5}$	2 µm	40 µm
$V_{th,2}$	559 mV	574.2 mV
$V_{th,6}$	533.4 mV	563.7 mV
$V_{th,1,5}$	−744.1 mV	−734.5 mV
$\lvert\beta_{1,5}\rvert$	174.2 µA/V^2	1.795 mA/V^2
$\beta_{2,6}$	303 µA/V^2	6.834 mA/V^2

the following errors are defined:

$$\Delta_{HL(LH)} = |V_{HL(LH)} - V_{HL(LH),sim}|, \tag{3.11}$$

$$\delta_{HL(LH)} = \frac{\Delta_{HL(LH)}}{V_{HL(LH),sim}} \cdot 100\%, \tag{3.12}$$

$$\delta_{V_{dd},HL(LH)} = \frac{\Delta_{HL(LH)}}{V_{dd}} \cdot 100\%. \tag{3.13}$$

Regarding *Design 1*, the simulated and analytical V_{HL} and V_{LH} as a function of V_{dd} are shown in Figs.3.4(a) and (b), respectively. As can be observed, the simulated and analytical V_{HL} are both linear, although an offset error is present. Regarding V_{LH}, also a gain error can be observed. For *Design 1*, the maximum absolute errors are $\Delta_{HL,1} = 19\,\text{mV}$ and $\Delta_{LH,1} = 48\,\text{mV}$, while the relative ones are $\delta_{HL,1} = 8\,\%$ and $\delta_{LH,1} = 66\,\%$. Regarding *Design 2*, the simulated and analytical V_{HL} and V_{LH} as a function of V_{dd} are shown in Figs.3.4(c) and (d), respectively. As can be observed, the analytical V_{LH} now better resembles the simulated behavior. For *Design 2*, the maximum absolute errors are $\Delta_{HL,2} = 20\,\text{mV}$ and $\Delta_{LH,2} = 20\,\text{mV}$, while the relative ones are $\delta_{HL,2} = 8\,\%$ and $\delta_{LH,2} = 33\,\%$. In *Design 2*, only the error in V_{LH} has improved since $\Delta_{HL,1} \approx \Delta_{HL,2}$. Therefore, the discrepancy between the analytical and simulated transition voltages can not be only attributed to the on resistances since the implementation of wider transistors did not improve $\Delta_{HL,2}$. To further investigate the model assumptions, the transition voltages of the simplified equivalent circuits in Fig.3.4(e) have been extracted. The V_{out} vs V_{in} plot of the *full* circuit is shown in Fig.3.4(f). The characteristic of the simplified equivalent circuit for the high-to-low transition is shown in Fig.3.4(g). As can be observed, the output does not go to zero volts, which is due to M_6. The characteristic of the simplified equivalent circuit for V_{LH} is shown in Fig.3.4(h). In this case the output does not reach the supply rail because of M_5. The maximum error between the *full* and the simplified equivalent circuits is approximately 2 mV. This proves that the simplified equivalent circuits represent an accurate approximation of the full circuit behavior during the transition. On the other side, it can be concluded that the model does not accurately describe the circuit behavior since the absolute errors ($\Delta_{HL(LH)}$) are larger by one order of magnitude with respect to the error between the *full* and simplified equivalent circuits. Since the derived expressions are based on the simplified equivalent circuits, a possible source of error can be attributed to the assumption that transistors are in saturation during the transition. Besides

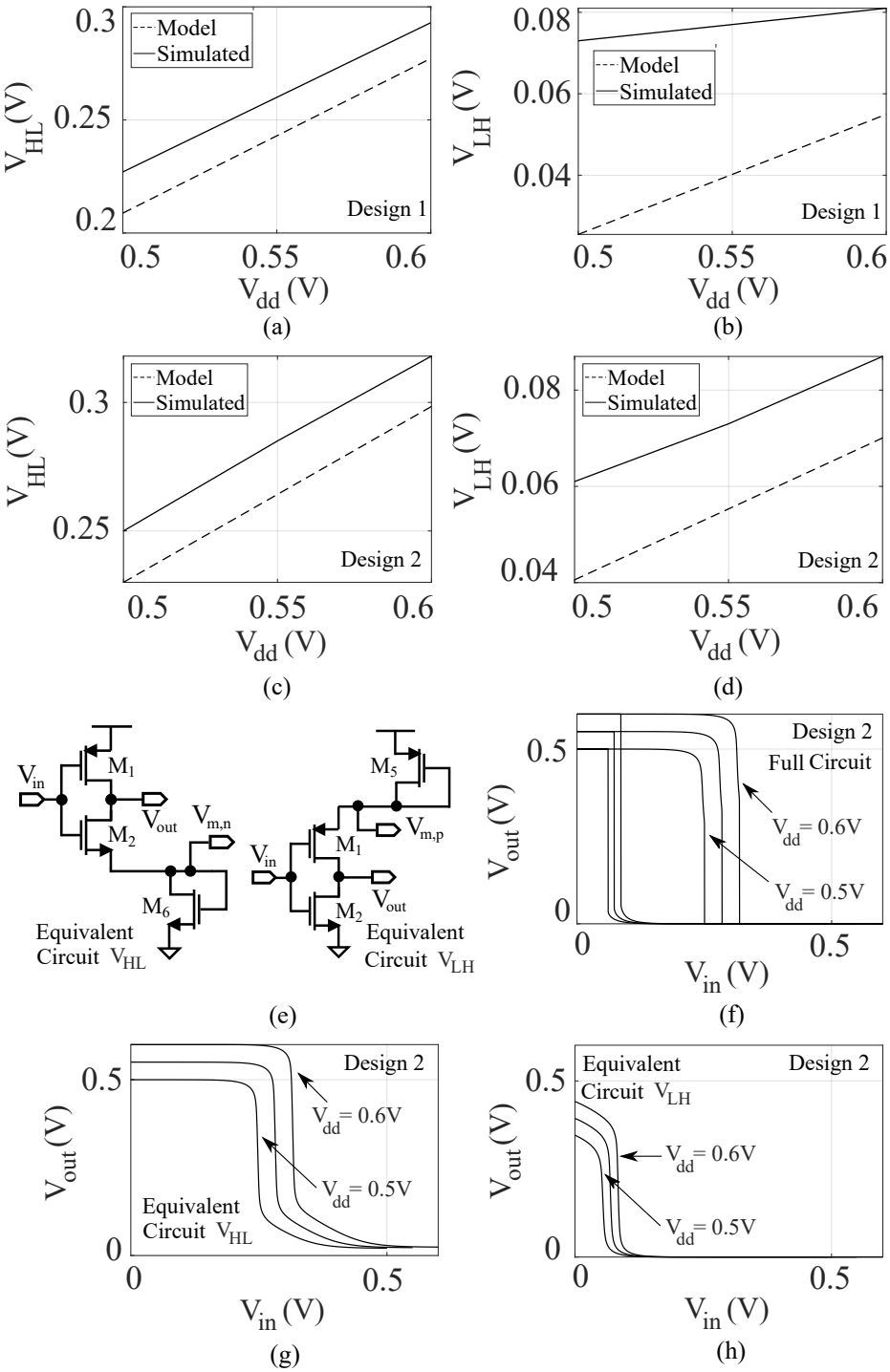


Figure 3.4: *Type 1* simulation results. *Design 1*: analytical and simulated (a) V_{HL} and (b) V_{LH} vs V_{dd}. *Design 2*: analytical and simulated (c) V_{HL} and (d) V_{LH} vs V_{dd}. (e) Simplified equivalent circuits. (f) V_{out} vs V_{in} (full circuit). (g) V_{out} vs V_{in} (simplified circuit for V_{HL}). (g) V_{out} vs V_{in} (simplified circuit for V_{LH}).

that, another source of error can be attributed to the extracted simulation parameters. According to the model assumptions, only M_3, M_4, M_5 and M_6 should be enlarged, but in *Design 2* all transistors have been enlarged. The model has also been verified by enlarging only the above mentioned transistors and by implementing different sizing strategies, and the error relative to V_{dd} resulted to be in the same order of magnitude (below 10 %). No further investigation has been performed on the proposed analytical model since greater effort has been put on the analysis of *Type 2*, which presents tunability and therefore more versatility in terms of applications.

3.2.2 Experimental Results

An ASIC in AMS-350nm CMOS process has been realized for experimental validation. The NMOS transistors are sized 1/1 and the PMOS ones 18/1 (*Design 3*). This design provides a relatively large hysteresis (250 mV) with respect to V_{dd}. When the PMOS transistors are small as compared to the NMOS ones, the hysteresis further reduces. Initially, it was planned to implement multiple designs in the ASIC. But due to the limited number of pads, it has been decided to only include *Design 3*. The layout and the micrograph of the circuit are reported in Appendix A.3. The circuit occupies an area of 49 µm × 25 µm. The output has been acquired by applying a low frequency triangular wave (200 mHz). For higher frequencies, the circuit does not toggle. This is expected since high speed operation is typically challenging in subthreshold region [183]. The supply voltage has been fixed to 0.6 V because for lower values the output does not toggle. A critical challenge during the measurement phase was to decouple the oscilloscope (KEYSIGHT InfiniiVision DSOX3024T) probe from the circuit. When the output of the ST is directly connected, through the pad, to the probe, the output signal toggles but

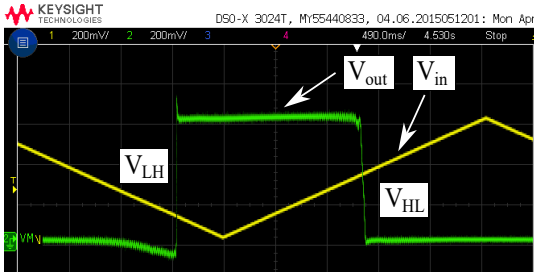


Figure 3.5: Example of measured input and output voltages. ($V_{dd} = 0.6$ V). ©2022 by A. Nowbahari, L. Marchetti, M. Azadmehr [7] CC BY-NC-ND 4.0.

with approximately half of the expected amplitude. This has been attributed to the series resistance of the oscilloscope probe. To decouple the impedances, a voltage follower implemented through an OP-AMP (TL072, Texas Instruments) has been placed between the probe and the pad. The voltage follower correctly decoupled the two points. An example of measurement is shown in Fig.3.5. For *Design 3*, $V_{HL} = 317\,\text{mV}$ and $V_{LH} = 96\,\text{mV}$. Regarding the absolute error with respect to the measurements, $\Delta_{HL,meas} = 12\,\text{mV}$ and $\Delta_{LH,meas} = 35\,\text{mV}$. The errors are attributed to parasitic components. The power consumption of the circuit has not been evaluated through measurements because of the very small currents in the circuit ($< 1\,\text{nA}$). Therefore, it has been analyzed through simulations (Appendix C.2).

3.2.3 Conclusions

An analytical model for the subthreshold characteristics of *Type 1* has been proposed. The maximum error between the simulated and analytical transition voltages is below 10 % with respect to V_{dd}, for the considered designs. The derived expressions are based on the assumption that the second inverter and the feedback transistors have negligible on resistances during the transitions. The model is more accurate when the transistors are large as compared to the minimum channel length. The model assumptions have been validated by considering simplified equivalent circuits. The error between the simulated full and simplified equivalent circuits is of few millivolts, but the model is not equally accurate although it is based on the same considered approximations. The analytical model allows designers to predict the effect of supply voltage scaling and temperature variations on the characteristics. Therefore, it can be used to optimize the design of ST-based circuits in subthreshold region. For instance, it can be used to design low power DC/DC converters drivers for energy harvesting interfaces for sensor node architectures.

3.3 Type 2

Type 2 is a single-input single-output non-inverting tunable voltage mode CMOS ST proposed by Wang in 1991 [88]. The circuit, its symbol and its characteristics are shown in Figs.3.6(a), (b) and (c), respectively. More focus has been placed on the analysis of

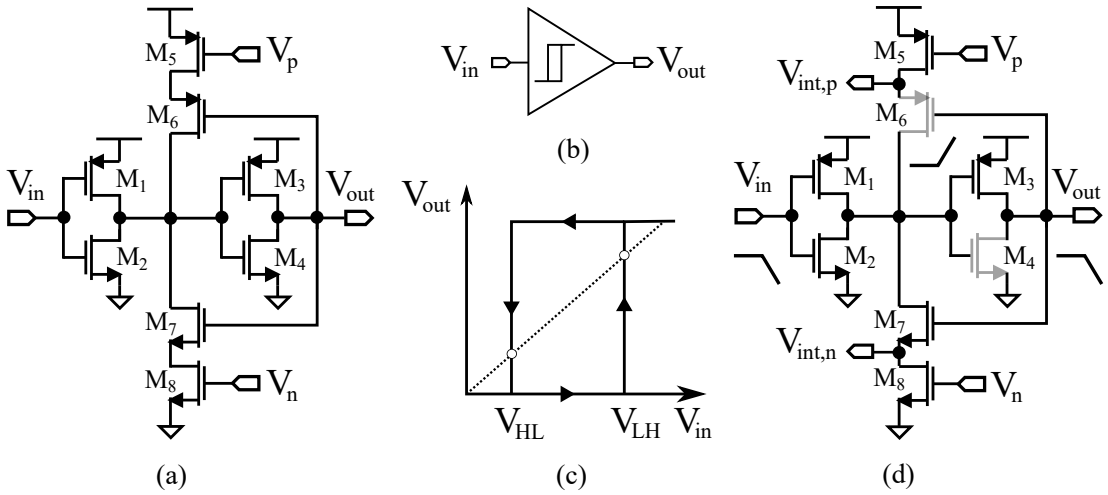


Figure 3.6: (a) *Type 2* circuit. (b) Inverting voltage mode Schmitt trigger symbol and (c) associated characteristics. (d) Circuit for V_{HL} derivation. ©2023 by A. Nowbahari, L. Marchetti, M. Azadmehr [8] CC BY 4.0.

Type 2, with respect to that of *Type 1*, because it is the first single-input tunable ST to be modeled in weak inversion. Therefore, it is practically more versatile in terms of applications, because of its tunability. As for *Type 1*, the high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages have been modeled in subthreshold region. Furthermore, supply voltage, temperature, and process variations have been considered for model validation. Moreover, a simple method for the estimation of the minimum supply voltage for which hysteresis occurs is reported [8]. The same methodology used to derive the analytical model of *Type 1* has been used for *Type 2*, i.e. the transition voltages have been determined by finding the switching voltage of the inverter composed by M_1 and M_2. As for *Type 1*, only the derivation of V_{HL} is reported since the low-to-high voltage can be complementary derived. The model is validated through simulations and experiments. The analytical model is mainly based on the assumption that the hysteresis transition points are independent of each other, i.e. V_{HL} depends only on the first inverter and the NMOS tuning transistor (M_8) through M_7, while V_{LH} only on the first inverter and the PMOS tuning transistor (M_5) through M_6. The assumption has been validated analytically, and through experiments and simulations. Referring to Fig.3.6(d), when V_{in} is high, V_{out} is high too due to the non-inverting topology. This results in M_4 and M_6 being off, and M_3 and M_7 being on. The conduction of M_5, which is dependent on its tuning voltage V_p, is irrelevant since M_6 decouples it for the middle node of the circuit. Regarding M_8, it is considered to be on since it takes care of the tuning action. As for *Type 1*, it is also

assumed that all transistors are in saturation during the transition. The switching voltage of the first inverter can be determined by imposing:

$$I_{0,n2} \cdot e^{\frac{V_{HL}}{n_n \cdot \phi}} + I_{0,n7} \cdot e^{\frac{V_{dd} - n_n \cdot V_{int,n}}{n_n \cdot \phi}} - I_{0,p1} \cdot e^{\frac{V_{dd} - V_{HL}}{n_p \cdot \phi}} = 0. \tag{3.14}$$

In order to solve (3.14), the following approximation is introduced [184]:

$$n_n \approx n_p \approx n \tag{3.15}$$

Furthermore, $I_{1,p}$ is redefined as:

$$I'_{0,p1} = I_{0,p1} \cdot exp(V_{dd}/(n \cdot \phi)). \tag{3.16}$$

Next (3.14) is divided by $I'_{0,p1}$ and rewritten as

$$\frac{I_{0,n2}}{I'_{0,p1}} \cdot e^{\frac{V_{HL}}{n \cdot \phi}} - e^{-\frac{V_{HL}}{n \cdot \phi}} = -\frac{I_{0,n7}}{I'_{0,p1}} \cdot e^{\frac{V_{dd} - n \cdot V_{int,n}}{n \cdot \phi}}. \tag{3.17}$$

The unknown variable in (3.17) is $V_{int,n}$, i.e. the drain-source voltage across M_8. To determine the unknown variable the following equation relating M_7 and M_8 is imposed:

$$I_{0,n7} \cdot e^{\frac{V_{dd} - n \cdot V_{int,n}}{n \cdot \phi}} = I_{0,n8} \cdot e^{\frac{V_n}{n \cdot \phi}} \cdot \left(1 - e^{-\frac{V_{int,n}}{\phi}}\right), \tag{3.18}$$

$$V_{int,n} = \phi \cdot log\left(1 + \frac{I_{0,n7}}{I_{0,n8}} \cdot e^{\frac{V_{dd} - V_n}{n \cdot \phi}}\right). \tag{3.19}$$

As can be observed, this last equation relates the drain-source voltage of M_8 to the tuning voltage. By substituting (3.19) in (3.17), the dependence of the high-to-low voltage on the tuning voltage becomes explicit:

$$\frac{I_{2,n}}{I'_{0,p1}} \cdot e^{\frac{V_{HL}}{n \cdot \phi}} - e^{-\frac{V_{HL}}{n \cdot \phi}} = -\frac{I_{0,n7}}{I'_{0,p1}} \cdot e^{\frac{V_{dd} - n \cdot \phi \cdot log\left(1 + \frac{I_{0,n7}}{I_{0,n8}} \cdot e^{\frac{V_{dd} - V_n}{n \cdot \phi}}\right)}{n \cdot \phi}}. \tag{3.20}$$

Next the following temporary variables are defined:

$$x = \frac{V_{HL}}{n \cdot \phi}, \tag{3.21}$$

$$a = \frac{I_{0,n2}}{I'_{0,p1}}, \tag{3.22}$$

$$b = -\frac{I_{0,n7}}{I'_{0,p1}} \cdot e^{\frac{V_{dd} - n\cdot\phi\cdot log\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right)}{n\cdot\phi}} = -\frac{I_{0,n7}}{I_{0,p1}} \cdot \frac{1}{1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}}. \tag{3.23}$$

Equation (3.20) can be then rewritten as in (3.24) and solved for the variable x:

$$a\cdot e^{x} - e^{-x} = b, \tag{3.24}$$

$$x = -log\left[\frac{1}{2}\cdot\left(\sqrt{4\cdot a + b^2} - b\right)\right] \tag{3.25}$$

Finally by replacing all the temporary variables in (3.25), the analytical expression (3.26) for V_{HL} is obtained:

$$V_{HL} = -n\cdot\phi\cdot log\left[\frac{1}{2}\cdot\left(\sqrt{4\cdot\frac{I_{0,n2}}{I_{0,p1}}\cdot e^{-\frac{V_{dd}}{n\cdot\phi}} + \left(\frac{I_{0,n7}}{I_{0,p1}}\right)^2 \cdot \frac{1}{\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right)^2}} + \frac{I_{0,n7}}{I_{0,p1}}\cdot\frac{1}{1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}}\right)\right] \tag{3.26}$$

The derivation of V_{LH} is complementary, and is reported in the associated article (Appendix C.3) [8]. Its expression is given by:

$$V_{LH} = -n\cdot\phi\cdot log\left[\frac{1}{2}\cdot\left(\sqrt{4\cdot\frac{I_{0,n2}}{I_{0,p1}}\cdot e^{-\frac{V_{dd}}{n\cdot\phi}} + \left(\frac{I_{0,p6}}{I_{0,p1}}\right)^2 \cdot \frac{1}{\left(1+\frac{I_{0,p6}}{I_{0,p5}}\cdot e^{\frac{V_p}{n\cdot\phi}}\right)^2}} - \frac{I_{0,p6}}{I_{0,p1}}\cdot\frac{1}{1+\frac{I_{0,p6}}{I_{0,p5}}\cdot e^{\frac{V_p}{n\cdot\phi}}}\right)\right] \tag{3.27}$$

As can be observed, the dependence on the thermal voltage and slope factor is linear, while the dependence on the tuning voltage, supply voltage, and the transistors' dimensions is logarithmic. Coherently with the model assumptions, V_{HL} depends on the first inverter (M_1 and M_2) and M_7 and M_8, while V_{LH} depends on the first inverter and M_5 and M_6.

3.3.1 Simulation Results

In the following, the NMOS transistors have dimensions 1/1, while the PMOS ones 20/1. Wider PMOS transistors lead to wider hysteresis width, therefore allowing more flexibility

during the measurement phase. The extracted NMOS transistor $V_{th,n}$ is 515.8 mV, while $V_{th,p} = -731.3$ mV. To guarantee subthreshold behavior, V_{dd} has been initially fixed to 0.45 V. Lower, as well as higher, supply voltages have been also considered during the characterization. As previously described, in order to solve (3.14), the slope factors approximation in (3.15) has been used. This results in $n \approx 1.28$. Instead, the non-averaged values ($n_{n(p)} = 1.25(1.3)$) are used when computing $I_{0,n(p)}$. Regarding the transconductance parameters, $\beta_n = 162.26\,\mu A/V^2$ while $\beta_p = 1.01\,mA/V^2$. The transition voltages have been extracted through a DC sweep, as for *Type 1*, and the errors are equivalently defined as in (3.11), (3.12), and (3.13). When extracting $V_{HL(LH)}$, only $V_{n(p)}$ is varied. Nevertheless, it has been verified that the transition voltages can be independently adjusted, through the tuning voltages. The analytical and simulated V_{HL} as a function of the tuning voltage V_n are shown in Fig.3.7(a). As can be observed, the model resembles the circuit behavior in the entire tuning range. For $V_n > 0.3$ V, no transition is observed, i.e. the output stays high. Instead, V_{LH} vs V_p is shown in Fig.3.7(b). In this case, the transition voltages for $V_p > 0.3$ V are not shown because the characteristic is almost constant.

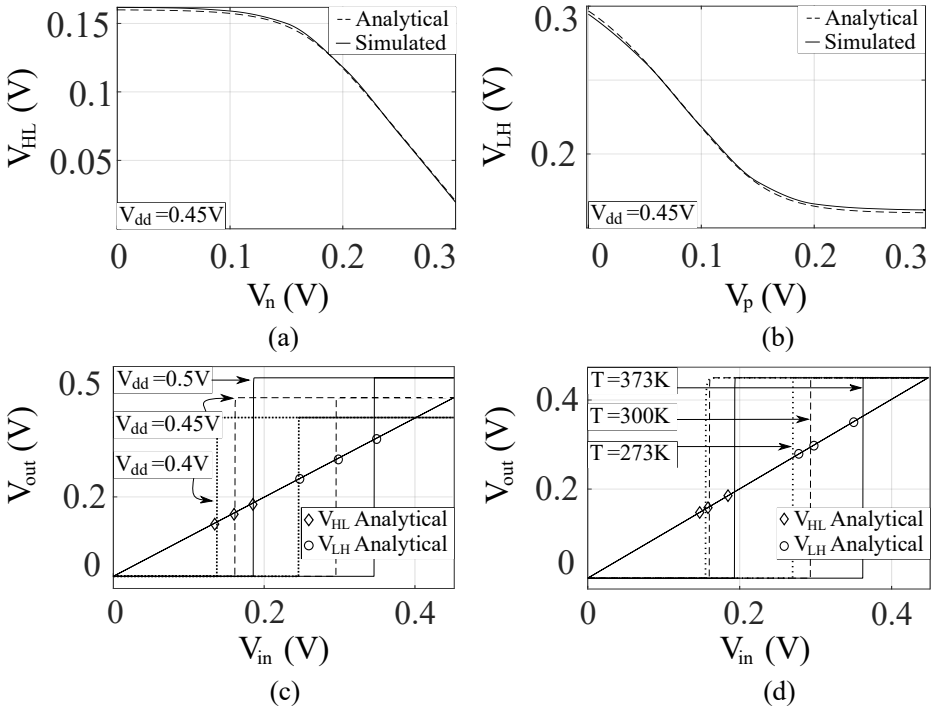


Figure 3.7: *Type 2* simulation results. Analytical and simulated (a) V_{HL} vs V_n and (b) V_{LH} vs V_p. Simulated V_{out} vs V_{in} for (c) different V_{dd} and $T = 300$ K, and (d) different T and $V_{dd} = 0.45$ V.

Regarding the maximum absolute errors, $\Delta_{HL} = 2.2\,\text{mV}$ and $\Delta_{LH} = 2.4\,\text{mV}$. Regarding the errors relative to the the simulated values, $\delta_{HL} = 1.3\,\%$ and $\delta_{LH} = 0.8\,\%$. Instead $\delta_{V_{dd},HL(LH)} < 0.5\,\%$. The discrepancy between the simulated and analytical values is attributed to the slope factor approximation in (3.15). Similar results, i.e. errors in the same order of magnitude, have been obtained for other designs (shorter L and more narrow transistors). The analytical model of *Type 2* is more accurate than that of *Type 1*, although the same methodology for the model derivation has been considered. This can be attributed to the less complex architecture of *Type 2*: the two inverters are not connected to the feedback stages, which results in having the sources of the PMOS (NMOS) transistors referred to V_{dd} (ground). The proposed model has also been validated in terms of supply voltage and temperature variations. For this analysis, the tuning voltages have been fixed to zero volts, because when $V_{n(p)} = 0\,\text{V}$ the error is maximum, i.e. a worst case analysis is considered. Different V_{out} vs V_{in} for different supply voltages are shown in Fig.3.7(c). V_{dd} ranges from 0.4 V to 0.5 V. The analysis has been performed with steps of 50 mV, but only three values are reported for simplicity. For $V_{dd} < 0.4\,\text{V}$ the ST does not correctly trigger, while for $V_{dd} > 0.5\,\text{V}$ the ST does not operate in subthreshold anymore. The maximum error occurs at $V_{dd} = 0.4\,\text{V}$. The model resembles the circuit behavior with an error $\delta_{V_{dd},HL(LH)} < 3\,\%$. Regarding temperature variations, the characteristics have been evaluated for T ranging from 273 K to 373 K (Fig.3.7(d)). Both errors are maximum for $T = 373K$. In this case the model is less accurate since the errors relative to the simulated values are $\delta_{HL} = 4.8\,\%$ and $\delta_{LH} = 3.7\,\%$. The performed analysis does not represent an accurate characterization of *Type 2* since the considered design is not an optimized one. Nevertheless, it represents a starting point for future model refinement and circuit characterization. The model accuracy has also been evaluated by running Monte Carlo simulations (process and mismatch variations), as reported in [8] (Appendix C.3). Also a simple method for the estimation of the minimum supply voltage for which hysteresis occurs has been proposed. The method simply consists in plotting the analytical transition voltages, and evaluate when V_{HL} (which normally occurs before V_{LH} as can be seen in Fig.3.6) becomes negative, i.e. undefined. The analytical model has been also validated by considering nominal values provided by the datasheet of the AMS process. Errors in the same order of magnitude have been obtained.

3.3.2 Experimental Results

The fabricated circuit (AMS-350nm CMOS process) has the same dimensions associated to Figs.3.7(a) and (b), i.e. PMOS (NMOS) transistors sized 20/1 (1/1). The area of the circuit is 42 µm × 45 µm. The layout and micrograph of the circuit are reported in Appendix A.3. The PMOS transistors are implemented with two 10 µm gates, because of technological constraints. This results in a difference less than $1mV$ in the transition voltages between the pre-layout and post-layout simulations. The transition voltages have been extracted by applying a 1 Hz triangular wave. The maximum operating frequency is 20 Hz. As compared to the implemented *Type 1* circuit (200 mHz), *Type 2* is one hundred times faster. It has been correctly verified that the transition voltages can be independently adjusted. In Fig.3.8 the analytical and measured hysteresis voltages are shown. The axis associated to the tuning voltage V_p is reversed with respect to that of V_n in order to show the minimum and maximum V_H. The maximum error in the hysteresis voltage is $\Delta_H = 23$ mV, which occurs when $V_n = 0.3$ V and $V_p = 0$ V. As for *Type 1*, it was not possible to measure the power consumption, due to the very small currents (< 1 nA). Therefore the power consumption has been analyzed only through simulations, as reported in [8] (Appendix C.3). At $V_{dd} = 0.45$ V, *Type 2* consumes 423 pA (V_{HL}) and 416 pA (V_{LH}), when $V_p = 0$ V and $V_n = 0.3$ V (worst case). Instead, *Type 1* consumes 159 pA and 615 pA during V_{HL} and V_{LH}, respectively ($V_{dd} = 0.5$ V). Clearly, *Type 2* presents higher power consumption (even at lower supply voltage), but this is expected considering that it has two additional transistors and the PMOS transistors are wider than those of *Type 1*.

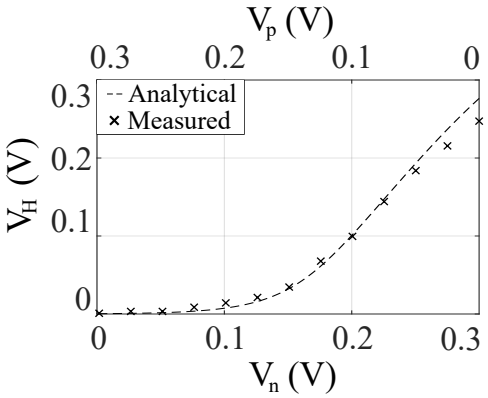


Figure 3.8: Analytical and measured hysteresis voltage (V_H), when $V_{dd} = 0.45$ V.

3.3.3 Conclusions

An analytical model for the subthreshold characteristics of *Type 2* has been proposed. The maximum error between the simulated and analytical transition voltages is below 6 % for the considered design; when considering other designs, the errors are in the same order of magnitude. The analytical model of *Type 2* is more accurate than that of *Type 1*. The model can correctly predict the circuit behavior when considering supply voltage ($V_{dd} = [0.4\,\mathrm{V} - 0.5\,\mathrm{V}]$) and temperature variations ($\boldsymbol{T} = [273\,\mathrm{K} - 373\,\mathrm{K}]$) with a maximum error below 5 %. Similarly to *Type 1*, the proposed model can be used to optimize the design of ST-based circuits in subthreshold region, e.g. it can be used to design low voltage interfaces for noise removal at the input of sensor node architectures.

4 Conclusions and Future Work

The work presented in this thesis consists of novel wake-up receiver architectures and analytical models for Schmitt trigger circuits in subthreshold region. The wake-up receivers optimize the power consumption of the sensor nodes by allowing selective activation on demand. The analytical models allow performance optimization in subthreshold region of two Schmitt trigger circuits, which can be used in wake-up receivers and other parts of sensor nodes' units. Therefore, all the contributions can be used to improve the power consumption of sensor node architectures.

Three types of wake-up receiver architectures have been reported in this thesis, i.e. inverter-based, multivibrator-based, and oscillator-based. Two different circuit implementations of the inverter-based architecture have been proposed, i.e. the delay-based WuRx and the tunable current starved inverter-based WuRx (*Type A*). *Type A* has been experimentally validated with an ASIC in AMS-350nm CMOS process, by decoding a wake-up call signal transmitted underwater. Its architecture is characterized by modularity and tunability. At $V_{dd} = 2\,\mathrm{V}$, when decoding a 5 bit wake-up call signal, it consumes 265 nW (700 nW) with a data rate of 250 bit/s (2 kbit/s). *Type A* presents the lowest power consumption reported for an underwater acoustic WuRx. The multivibrator-based architecture has been implemented with three different multivibrator circuits, i.e. NOR-based, single transistor, and tunable NOR-based (*Type B*). Similarly to *Type A*, *Type B* has been experimentally validated, and it presents State-of-the-Art performance as well by consuming less than 500 nW. The single transistor WuRx presents, at simulation level, the lowest power consumption reported for a (non-underwater) acoustic WuRx, and it overcomes the performances of *Type A* and *Type B*. An oscillator-based architecture has been also proposed, but the performance of its circuit implementation does not overcome those of *Type A* and *Type B*.

Regarding the Schmitt trigger circuits, two typologies have been analyzed, i.e. the low

power single input ST (*Type 1*) proposed by Al-Sarawi, and the tunable single input ST (*Type 2*) proposed by Wang. The hysteresis voltages of the two ST circuits have been analytically modeled, for the first time, in subthreshold region. The derived expressions allow designing the two STs with desired hysteresis width as a function of the transistors' geometrical parameters. Furthermore, they can be used to predict the effect of supply voltage and temperature variations on the characteristics. Moreover, they can be used to estimate the minimum supply voltage for which hysteresis occurs. Therefore, they allow to optimize the design of ST-based circuits in subthreshold region, e.g. low voltage and low power sensor interfaces for sensor node architectures. The derived expressions have been validated through simulations and experiments, by prototyping an ASIC in AMS-350nm CMOS process. The analytical model of *Type 1* has been validated with an error below 10 %, relative to V_{dd}. The analytical model of *Type 2* is more accurate, with an error below 0.5 %, relative to V_{dd}, for the considered design.

Regarding the future work, different directions can be followed. A first idea is to redesign *Type A* and *Type B* in a lower technological node. By doing that, the power supply can be scaled, thus eventually allowing further reduction of the power consumption. A second idea is to design them in subthreshold region, so that the power consumption can be lowered to the sub-nanowatt region. Furthermore, it would be also interesting to implement a high frequency version of the proposed circuits, e.g. for RF-based applications. The WuRx architecture based on single transistor should be better investigated (e.g. ASIC integration and tunability). The oscillator-based WuRx should be optimized in terms of power consumption. An idea can be to use one of the modeled Schmitt trigger circuits as oscillator. Furthermore, the STs can be used at the input of the WuRxs for noise reduction. Regarding the ST circuits, the analytical model of *Type 1* should be better investigated, in order to clearly understand the sources of errors. *Type 2* should be better characterized in terms of optimal performance, by relating sizing, hysteresis width, power consumption and speed. For both ST circuits, a small signal model analysis in subthreshold region should be performed. Furthermore, it would be interesting to validate the models by considering lower technological nodes, where short channel effects can be more dominant.

References

[1] A. Nowbahari, L. Marchetti and M. Azadmehr, 'A Delay-Based Wake-Up Receiver for Wireless Sensor Networks,' in *2021 International Conference on Electrical, Communication, and Computer Engineering (ICECCE)*, 2021, pp. 1–5. DOI: 10.1109/ICECCE52056.2021.9514246.

[2] A. Nowbahari, L. Marchetti and M. Azadmehr, 'An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks,' in *2021 IEEE 7th World Forum on Internet of Things (WF-IoT)*, 2021, pp. 380–384. DOI: 10.1109/WF-IoT51360.2021.9595159.

[3] A. Nowbahari, L. Marchetti and M. Azadmehr, 'Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks,' in *2022 11th International Conference on Communications, Circuits and Systems (ICCCAS)*, 2022, pp. 187–191. DOI: 10.1109/ICCCAS55266.2022.9825344.

[4] A. Nowbahari, L. Marchetti and M. Azadmehr, 'An Oscillator-Based Wake-Up Receiver for Wireless Sensor Networks,' in *2021 IEEE Sensors Applications Symposium (SAS)*, 2021, pp. 1–5. DOI: 10.1109/SAS51076.2021.9530093.

[5] A. Nowbahari, L. Marchetti and M. Azadmehr, 'Low Power Wake-Up Receivers for Underwater Acoustic Wireless Sensor Networks,' *IEEE Transactions on Green Communications and Networking*, Under Review.

[6] A. Nowbahari, L. Marchetti and M. Azadmehr, 'Weak Inversion Model of an Inverting CMOS Schmitt Trigger,' in *2022 11th International Conference on Communications, Circuits and Systems (ICCCAS)*, 2022, pp. 1–5. DOI: 10.1109/ICCCAS55266.2022.9824290.

[7] A. Nowbahari, L. Marchetti and M. Azadmehr, 'Analysis of a Low Power Inverting CMOS Schmitt Trigger Operating in Weak Inversion,' *International Journal of Electrical and Electronic Engineering & Telecommunications*, vol. 11, no. 6, pp. 392–397, 2022. DOI: 10.18178/ijeetc.11.6.392-397. [Online]. Available: http://www.ijeetc.com/uploadfile/2022/1014/20221014033458167.pdf.

[8] A. Nowbahari, L. Marchetti and M. Azadmehr, 'Subthreshold Modeling of a Tunable CMOS Schmitt Trigger,' *IEEE Access*, vol. 11, pp. 10 977–10 984, 2023. DOI: 10.1109/ACCESS.2023.3241492.

[9] A. Nowbahari, A. Roy and L. Marchetti, 'Junctionless Transistors: State-of-the-Art,' *Electronics*, vol. 9, no. 7, 2020. DOI: 10.3390/electronics9071174.

[10] M. Azadmehr, A. Nowbahari, L. Marchetti and R. Langoy, 'A Low Power Front-End for Resistive Sensors based on Switch-Cap Current Reuse,' in *2022 IEEE 15th Dallas Circuit And System Conference (DCAS)*, 2022, pp. 1–5. DOI: 10.1109/DCAS53974.2022.9845572.

[11] J. Li, H. Ouro-Koura, H. Arnow *et al.*, 'A Novel Comb Design for Enhanced Power and Bandwidth in Electrostatic MEMS Energy Converters,' in *2023 IEEE 36th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2023, pp. 728–731. DOI: 10.1109/MEMS49605.2023.10052590.

[12] L. Atzori, A. Iera and G. Morabito, 'The Internet of Things: A survey,' *Computer Networks*, vol. 54, no. 15, pp. 2787–2805, 2010, ISSN: 1389-1286. DOI: 10.1016/j.comnet.2010.05.010.

[13] A. Flammini and E. Sisinni, 'Wireless Sensor Networking in the Internet of Things and Cloud Computing Era,' *Procedia Engineering*, vol. 87, pp. 672–679, 2014, EUROSENSORS 2014, the 28th European Conference on Solid-State Transducers, ISSN: 1877-7058. DOI: 10.1016/j.proeng.2014.11.577.

[14] W. Dargie and C. Poellabauer, 'Node architecture,' in *Fundamentals of Wireless Sensor Networks: Theory and Practice*. 2011, pp. 47–68. DOI: 10.1002/9780470666388.ch3.

[15] L. Cui, F. Wang, H. Luo, H. Ju and T. Li, 'A Pervasive Sensor Node Architecture,' in *Network and Parallel Computing*, Berlin, Heidelberg: Springer Berlin Heidelberg, 2004, pp. 565–567. DOI: 10.1007/978-3-540-30141-7_84.

[16] P. Mandal, L. P. Roy and S. K. Das, 'Internet of UAV Mounted RFID for Various Applications Using LoRa Technology: A Comprehensive Survey,' in *Internet of Things and Its Applications*, K. Dahal, D. Giri, S. Neogy, S. Dutta and S. Kumar, Eds., Singapore: Springer Nature Singapore, 2022, pp. 369–380. DOI: 10.1007/978-981-16-7637-6_33.

[17] Silicon Lab. Inc., Austin, TX, USA, White Paper Rev, 'The Evolution of Wireless Sensor Networks,' Tech. Rep., 2013, pp. 1–5.

[18] C.-Y. Chong and S. Kumar, 'Sensor Networks: Evolution, Opportunities, and Challenges,' *Proceedings of the IEEE*, vol. 91, no. 8, pp. 1247–1256, 2003. DOI: 10.1109/JPROC.2003.814918.

[19] J. Heidemann, M. Stojanovic and M. Zorzi, 'Underwater sensor networks: Applications, advances and challenges,' *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 370, no. 1958, pp. 158–175, 2012.

[20] I. Vasilescu, K. Kotay, D. Rus, M. Dunbabin and P. Corke, 'Data Collection, Storage, and Retrieval with an Underwater Sensor Network,' in *Proceedings of the 3rd International Conference on Embedded Networked Sensor Systems*, ser. SenSys '05, San Diego, California, USA: Association for Computing Machinery, 2005, pp. 154–165, ISBN: 159593054X. DOI: 10.1145/1098918.1098936.

[21] A. S. S. and S. C. Dhongdi, 'Review of Underwater Mobile Sensor Network for ocean phenomena monitoring,' *Journal of Network and Computer Applications*, vol. 205, p. 103 418, 2022, ISSN: 1084-8045. DOI: 10.1016/j.jnca.2022.103418.

[22] E. Felemban, F. K. Shaikh, U. M. Qureshi, A. A. Sheikh and S. B. Qaisar, 'Underwater Sensor Network Applications: A Comprehensive Survey,' *International Journal of Distributed Sensor Networks*, vol. 11, no. 11, p. 896 832, 2015. DOI: 10.1155/2015/896832.

[23] M. Jouhari, K. Ibrahimi, H. Tembine and J. Ben-Othman, 'Underwater Wireless Sensor Networks: A Survey on Enabling Technologies, Localization Protocols, and Internet of Underwater Things,' *IEEE Access*, vol. 7, pp. 96 879–96 899, 2019. DOI: 10.1109/ACCESS.2019.2928876.

[24] A. Gkikopouli, G. Nikolakopoulos and S. Manesis, 'A survey on Underwater Wireless Sensor Networks and applications,' in *2012 20th Mediterranean Conference on Control & Automation (MED)*, 2012, pp. 1147–1154. DOI: 10.1109/MED.2012.6265793.

[25] A. Davis and H. Chang, 'Underwater wireless sensor networks,' in *2012 Oceans*, 2012, pp. 1–5. DOI: 10.1109/OCEANS.2012.6405141.

[26] M. Jahanbakht, W. Xiang, L. Hanzo and M. Rahimi Azghadi, 'Internet of Underwater Things and Big Marine Data Analytics—A Comprehensive Survey,' *IEEE Communications Surveys & Tutorials*, vol. 23, no. 2, pp. 904–956, 2021. DOI: 10.1109/COMST.2021.3053118.

[27] S. Fattah, A. Gani, I. Ahmedy, M. Y. I. Idris and I. A. Targio Hashem, 'A survey on Underwater Wireless Sensor Networks: Requirements, Taxonomy, Recent Advances, and Open Research Challenges,' *Sensors*, vol. 20, no. 18, 2020, ISSN: 1424-8220. DOI: 10.3390/s20185393.

[28] S. Khisa and S. Moh, 'Survey on Recent Advancements in Energy-Efficient Routing Protocols for Underwater Wireless Sensor Networks,' *IEEE Access*, vol. 9, pp. 55 045–55 062, 2021. DOI: 10.1109/ACCESS.2021.3071490.

[29] M. Ayaz, I. Baig, A. Abdullah and I. Faye, 'A survey on routing techniques in underwater wireless sensor networks,' *Journal of Network and Computer Applications*, vol. 34, no. 6, pp. 1908–1927, 2011, Control and Optimization over Wireless Networks, ISSN: 1084-8045. DOI: 10.1016/j.jnca.2011.06.009.

[30] E. D. Zubiete, L. F. Luque, A. V. M. Rodríguez and I. G. Gonzalez, 'Review of wireless sensors networks in health applications,' in *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, 2011, pp. 1789–1793. DOI: 10.1109/IEMBS.2011.6090510.

[31] A. Darwish and A. E. Hassanien, 'Wearable and Implantable Wireless Sensor Network Solutions for Healthcare Monitoring,' *Sensors*, vol. 11, no. 6, pp. 5561–5595, 2011, ISSN: 1424-8220. DOI: 10.3390/s110605561.

[32] B. R. Stojkoska, A. P. Avramova and P. Chatzimisios, 'Application of Wireless Sensor Networks for Indoor Temperature Regulation,' *International Journal of Distributed Sensor Networks*, vol. 10, no. 5, p. 502 419, 2014. DOI: 10.1155/2014/502419.

[33] D. Basu, G. Moretti, G. Sen Gupta and S. Marsland, 'Wireless sensor network based smart home: Sensor selection, deployment and monitoring,' in *2013 IEEE Sensors Applications Symposium Proceedings*, 2013, pp. 49–54. DOI: 10.1109/SAS.2013.6493555.

[34] F. Mao, K. Khamis, S. Krause, J. Clark and D. M. Hannah, 'Low-Cost Environmental Sensor Networks: Recent Advances and Future Directions,' *Frontiers in Earth Science*, vol. 7, 2019, ISSN: 2296-6463. DOI: 10.3389/feart.2019.00221.

[35] P. Corke, T. Wark, R. Jurdak, W. Hu, P. Valencia and D. Moore, 'Environmental Wireless Sensor Networks,' *Proceedings of the IEEE*, vol. 98, no. 11, pp. 1903–1917, 2010. DOI: 10.1109/JPROC.2010.2068530.

[36] M. P. Đurišić, Z. Tafa, G. Dimić and V. Milutinović, 'A survey of military applications of wireless sensor networks,' in *2012 Mediterranean Conference on Embedded Computing (MECO)*, 2012, pp. 196–199.

[37] I. Akyildiz, W. Su, Y. Sankarasubramaniam and E. Cayirci, 'Wireless sensor networks: A survey,' *Computer Networks*, vol. 38, no. 4, pp. 393–422, 2002, ISSN: 1389-1286. DOI: 10.1016/S1389-1286(01)00302-4.

[38] Z. Yang, Y. Yong and J. He, 'Determining the number of nodes for wireless sensor networks,' in *Proceedings of the IEEE 6th Circuits and Systems Symposium on Emerging Technologies: Frontiers of Mobile and Wireless Communication (IEEE Cat. No.04EX710)*, vol. 2, 2004, 501–504 Vol.2. DOI: 10.1109/CASSET.2004.1321935.

[39] F. A. El-Qawasma, T. M. Elfouly and M. H. Ahmed, 'Minimising number of sensors in wireless sensor networks for structure health monitoring systems,' *IET Wireless Sensor Systems*, vol. 9, no. 2, pp. 94–101, 2019.

[40] J. Yick, B. Mukherjee and D. Ghosal, 'Wireless sensor network survey,' *Computer Networks*, vol. 52, no. 12, pp. 2292–2330, 2008, ISSN: 1389-1286. DOI: 10.1016/j.comnet.2008.04.002.

[41] A. Khan, I. Ali, A. Ghani *et al.*, 'Routing Protocols for Underwater Wireless Sensor Networks: Taxonomy, Research Challenges, Routing Strategies and Future Directions,' *Sensors*, vol. 18, no. 5, 2018, ISSN: 1424-8220. DOI: 10.3390/s18051619.

[42] A. Al-Shamma'a, A. Shaw and S. Saman, 'Propagation of electromagnetic waves at MHz frequencies through seawater,' *IEEE Transactions on Antennas and Propagation*, vol. 52, no. 11, pp. 2843–2849, 2004. DOI: 10.1109/TAP.2004.834449.

[43] M. R. Frater, M. J. Ryan and R. M. Dunbar, 'Electromagnetic Communications within Swarms of Autonomous Underwater Vehicles,' ser. WUWNet '06, Los Angeles, CA, USA: Association for Computing Machinery, 2006, ISBN: 1595934847. DOI: 10.1145/1161039.1161053.

[44] D. Anguita, D. Brizzolara and G. Parodi, 'Optical wireless communication for underwater Wireless Sensor Networks: Hardware modules and circuits design and implementation,' in *OCEANS 2010 MTS/IEEE SEATTLE*, 2010, pp. 1–8. DOI: 10.1109/OCEANS.2010.5664321.

[45] H. Luo, J. Wang, F. Bu, R. Ruby, K. Wu and Z. Guo, 'Recent Progress of Air/Water Cross-Boundary Communications for Underwater Sensor Networks: A Review,' *IEEE Sensors Journal*, vol. 22, no. 9, pp. 8360–8382, 2022. DOI: 10.1109/JSEN.2022.3162600.

[46] D. Menaka, S. Gauni, C. T. Manimegalai and K. Kalimuthu, 'Challenges and vision of wireless optical and acoustic communication in underwater environment,' *International Journal of Communication Systems*, vol. 35, no. 12, e5227, 2022. DOI: 10.1002/dac.5227.

[47] N. Saeed, A. Celik, T. Y. Al-Naffouri and M.-S. Alouini, 'Energy Harvesting Hybrid Acoustic-Optical Underwater Wireless Sensor Networks Localization,' *Sensors*, vol. 18, no. 1, 2018, ISSN: 1424-8220. DOI: 10.3390/s18010051.

[48] M. F. Ali, D. N. K. Jayakody and Y. Li, 'Recent Trends in Underwater Visible Light Communication (UVLC) Systems,' *IEEE Access*, vol. 10, pp. 22 169–22 225, 2022. DOI: 10.1109/ACCESS.2022.3150093.

[49] K. Y. Islam, I. Ahmad, D. Habibi, M. I. A. Zahed and J. Kamruzzaman, 'Green Underwater Wireless Communications Using Hybrid Optical-Acoustic Technologies,' *IEEE Access*, vol. 9, pp. 85 109–85 123, 2021. DOI: 10.1109/ACCESS.2021.3088467.

[50] C. Schurgers, V. Tsiatsis, S. Ganeriwal and M. Srivastava, 'Optimizing sensor networks in the energy-latency-density design space,' *IEEE Transactions on Mobile Computing*, vol. 1, no. 1, pp. 70–80, 2002. DOI: 10.1109/TMC.2002.1011060.

[51] F. Bouabdallah, N. Bouabdallah and R. Boutaba, 'On Balancing Energy Consumption in Wireless Sensor Networks,' *IEEE Transactions on Vehicular Technology*, vol. 58, no. 6, pp. 2909–2924, 2009. DOI: 10.1109/TVT.2008.2008715.

[52] T. Rault, A. Bouabdallah and Y. Challal, 'Energy efficiency in wireless sensor networks: A top-down survey,' *Computer Networks*, vol. 67, pp. 104–122, 2014, ISSN: 1389-1286. DOI: 10.1016/j.comnet.2014.03.027.

[53] J. Roselin, P. Latha and S. Benitta, 'Maximizing the wireless sensor networks lifetime through energy efficient connected coverage,' *Ad Hoc Networks*, vol. 62, pp. 1–10, 2017, ISSN: 1570-8705. DOI: 10.1016/j.adhoc.2017.04.001.

[54] Y. Chen and Q. Zhao, 'On the lifetime of wireless sensor networks,' *IEEE Communications Letters*, vol. 9, no. 11, pp. 976–978, 2005. DOI: 10.1109/LCOMM.2005.11010.

[55] I. Dietrich and F. Dressler, 'On the Lifetime of Wireless Sensor Networks,' *ACM Trans. Sen. Netw.*, vol. 5, no. 1, Feb. 2009, ISSN: 1550-4859. DOI: 10.1145/1464420.1464425.

[56] M. Tolani, Sunny and R. K. Singh, 'Lifetime improvement of wireless sensor network by information sensitive aggregation method for railway condition monitoring,' *Ad Hoc Networks*, vol. 87, pp. 128–145, 2019, ISSN: 1570-8705. DOI: 10.1016/j.adhoc.2018.11.009.

[57] T. D. C. Little, P. Dib, K. Shah, N. Barraford and B. Gallagher, 'Using LED Lighting for Ubiquitous Indoor Wireless Networking,' in *2008 IEEE International Conference on Wireless and Mobile Computing, Networking and Communications*, 2008, pp. 373–378. DOI: 10.1109/WiMob.2008.57.

[58] S. Gao, X. Dai, Z. Liu and G. Tian, 'High-Performance Wireless Piezoelectric Sensor Network for Distributed Structural Health Monitoring,' *International Journal of Distributed Sensor Networks*, vol. 12, no. 3, p. 3 846 804, 2016. DOI: 10.1155/2016/3846804.

[59] D. Puccinelli and M. Haenggi, 'Wireless sensor networks: Applications and challenges of ubiquitous sensing,' *IEEE Circuits and Systems Magazine*, vol. 5, no. 3, pp. 19–31, 2005. DOI: 10.1109/MCAS.2005.1507522.

[60] M. Matin and M. Islam, 'Overview of Wireless Sensor Network,' in *Wireless Sensor Networks*, M. A. Matin, Ed., Rijeka: IntechOpen, 2012, ch. 1. DOI: 10.5772/49376.

[61] O. Ali, M. K. Ishak, C. A. Ooi and M. K. L. Bhatti, 'Battery characterization for wireless sensor network applications to investigate the effect of load on surface temperatures,' *Royal Society Open Science*, vol. 9, no. 2, p. 210 870, 2022. DOI: 10.1098/rsos.210870.

[62] F. K. Shaikh and S. Zeadally, 'Energy harvesting in wireless sensor networks: A comprehensive review,' *Renewable and Sustainable Energy Reviews*, vol. 55, pp. 1041–1054, 2016, ISSN: 1364-0321. DOI: 10.1016/j.rser.2015.11.010.

[63] A. Zahid Kausar, A. W. Reza, M. U. Saleh and H. Ramiah, 'Energizing wireless sensor networks by energy harvesting systems: Scopes, challenges and approaches,' *Renewable and Sustainable Energy Reviews*, vol. 38, pp. 973–989, 2014, ISSN: 1364-0321. DOI: 10.1016/j.rser.2014.07.035.

[64] V. Ramasamy, 'Mobile Wireless Sensor Networks: An Overview,' in *Wireless Sensor Networks*, P. Sallis, Ed., Rijeka: IntechOpen, 2017, ch. 1. DOI: 10.5772/intechopen.70592.

[65] A. Moschitta and I. Neri, 'Power consumption Assessment in Wireless Sensor Networks,' in *ICT - Energy - Concepts Towards Zero*, G. Fagas, L. Gammaitoni, D. Paul and G. A. Berini, Eds., Rijeka: IntechOpen, 2014, ch. 9. DOI: 10.5772/57201.

[66] A. K. Sangaiah, M. Sadeghilalimi, A. A. R. Hosseinabadi and W. Zhang, 'Energy Consumption in Point-Coverage Wireless Sensor Networks via Bat Algorithm,' *IEEE Access*, vol. 7, pp. 180 258–180 269, 2019. DOI: 10.1109/ACCESS.2019.2952644.

[67] V. Raghunathan, C. Schurgers, S. Park and M. Srivastava, 'Energy-aware wireless microsensor networks,' *IEEE Signal Processing Magazine*, vol. 19, no. 2, pp. 40–50, 2002. DOI: 10.1109/79.985679.

[68] G. Anastasi, M. Conti, M. Di Francesco and A. Passarella, 'Energy conservation in wireless sensor networks: A survey,' *Ad Hoc Networks*, vol. 7, no. 3, pp. 537–568, 2009, ISSN: 1570-8705. DOI: 10.1016/j.adhoc.2008.06.003.

[69] E.-Y. Lin, J. Rabaey and A. Wolisz, 'Power-efficient rendez-vous schemes for dense wireless sensor networks,' in *2004 IEEE International Conference on Communications (IEEE Cat. No.04CH37577)*, vol. 7, 2004, 3769–3776 Vol.7. DOI: 10.1109/ICC.2004.1313259.

[70] I. Demirkol, C. Ersoy and E. Onur, 'Wake-up receivers for wireless sensor networks: Benefits and challenges,' *IEEE Wireless Communications*, vol. 16, no. 4, pp. 88–96, 2009. DOI: 10.1109/MWC.2009.5281260.

[71] R. Piyare, A. L. Murphy, C. Kiraly, P. Tosato and D. Brunelli, 'Ultra Low Power Wake-Up Radios: A Hardware and Networking Survey,' *IEEE Communications Surveys & Tutorials*, vol. 19, no. 4, pp. 2117–2157, 2017. DOI: 10.1109/COMST.2017.2728092.

[72] A. F. Harris, M. Stojanovic and M. Zorzi, 'When Underwater Acoustic Nodes Should Sleep with One Eye Open: Idle-Time Power Management in Underwater Sensor Networks,' in *Proceedings of the 1st ACM International Workshop on Underwater Networks*, ser. WUWNet '06, Los Angeles, CA, USA: Association for Computing Machinery, 2006, pp. 105–108, ISBN: 1595934847. DOI: 10.1145/1161039.1161061.

[73] A. Sanchez, S. Blanc, P. Yuste and J. Serrano, 'RFID Based Acoustic Wake-Up System for Underwater Sensor Networks,' in *2011 IEEE Eighth International Conference on Mobile Ad-Hoc and Sensor Systems*, 2011, pp. 873–878. DOI: 10.1109/MASS.2011.103.

[74] M. Chaudhary, N. Goyal, A. Benslimane, L. K. Awasthi, A. Alwadain and A. Singh, 'Underwater Wireless Sensor Networks: Enabling Technologies for Node Deployment and Data Collection Challenges,' *IEEE Internet of Things Journal*, pp. 1–1, 2022. DOI: 10.1109/JIOT.2022.3218766.

[75] M. C. Domingo, 'An overview of the internet of underwater things,' *Journal of Network and Computer Applications*, vol. 35, no. 6, pp. 1879–1890, 2012, ISSN: 1084-8045. DOI: 10.1016/j.jnca.2012.07.012.

[76] H.-J. Song, Y.-H. Kim, S.-C. Park and H.-J. Yoo, 'A fully integrated HF multi-standard RFID transceiver for compact mobile terminals,' in *2010 IEEE International Conference on RFID-Technology and Applications*, 2010, pp. 245–250. DOI: 10.1109/RFID-TA.2010.5529924.

[77] W.-H. Cho, Y. Li, Y. Kim *et al.*, 'A 5.4-mW 4-Gb/s 5-band QPSK transceiver for frequency-division multiplexing memory interface,' in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1–4. DOI: 10.1109/CICC.2015.7338373.

[78] S. Koppa, D. Park, Y. Joo and S. Jung, 'A 105.6dB DR and 65dB peak SNR self-reset CMOS image sensor using a Schmitt trigger circuit,' in *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011, pp. 1–4. DOI: 10.1109/MWSCAS.2011.6026323.

[79] K. Ishibashi and S. Takahashi, 'A 375 nA Input Off Current Schmitt Triger LDO for Energy Harvesting IoT Sensors,' in *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2018, pp. 187–190. DOI: 10.1109/ISVLSI.2018.00043.

[80] J. Yoo, S. Lee and H.-J. Yoo, 'A 1.12pJ/b resonance compensated inductive transceiver with a fault-tolerant network controller for wearable body sensor networks,' in *2008 IEEE Asian Solid-State Circuits Conference*, 2008, pp. 313–316. DOI: 10.1109/ASSCC.2008.4708790.

[81] K. Ishida, T.-C. Huang, K. Honda *et al.*, 'Insole Pedometer With Piezoelectric Energy Harvester and 2 V Organic Circuits,' *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 255–264, 2013. DOI: 10.1109/JSSC.2012.2221253.

[82] S. Ahmad, M. K. Gupta, N. Alam and M. Hasan, 'Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell,' *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 8, pp. 2634–2642, 2016. DOI: 10.1109/TVLSI.2016.2520490.

[83] M. Tache, W. Ibrahim, F. Kharbash and V. Beiu, 'Reliability and performance of optimised Schmitt trigger gates,' *The Journal of Engineering*, vol. 2018, no. 8, pp. 735–744, 2018. DOI: 10.1049/joe.2018.0091.

[84] N. Lotze and Y. Manoli, 'Ultra-Sub-Threshold Operation of Always-On Digital Circuits for IoT Applications by Use of Schmitt Trigger Gates,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 11, pp. 2920–2933, 2017. DOI: 10.1109/TCSI.2017.2705053.

[85] L. A. Pasini Melek, A. L. da Silva, M. C. Schneider and C. Galup-Montoro, 'Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 4, pp. 869–878, 2017. DOI: 10.1109/TCSI.2016.2631726.

[86] S. Al-Sarawi, 'Low power Schmitt trigger circuit,' *Electronics Letters*, vol. 38, 1009–1010(1), 18 2002. DOI: 10.1049/el:20020687.

[87] M. R. Elmezayen, W. Hu, A. M. Maghraby, I. T. Abougindia and S. U. Ay, 'Accurate Analysis and Design of Integrated Single Input Schmitt Trigger Circuits,' *Journal of Low Power Electronics and Applications*, vol. 10, no. 3, 2020. DOI: 10.3390/jlpea10030021.

[88] Z. Wang, 'CMOS adjustable Schmitt triggers,' *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 601–605, 1991. DOI: 10.1109/19.87026.

[89] K. Awan, D. P. A. Shah, K. Iqbal, S. Gilani, W. Ahmad and Y. Nam, 'Underwater Wireless Sensor Networks: A Review of Recent Issues and Challenges,' *Wireless Communications and Mobile Computing*, vol. 2019, pp. 1–20, Jan. 2019. DOI: 10.1155/2019/6470359.

[90] F. Meneghello, F. Campagnaro, R. Diamant, P. Casari and M. Zorzi, 'Design and Evaluation of a Low-Cost Acoustic Chamber for Underwater Networking Experiments,' in *Proceedings of the 11th ACM International Conference on Underwater Networks & Systems*, New York, NY, USA: Association for Computing Machinery, 2016, ISBN: 9781450346375. DOI: 10.1145/2999504.3001086.

[91] L. Nguyen and H. T. Nguyen, 'Mobility based network lifetime in wireless sensor networks: A review,' *Computer Networks*, vol. 174, p. 107 236, 2020, ISSN: 1389-1286. DOI: 10.1016/j.comnet.2020.107236.

[92] E. Ekici, Y. Gu and D. Bozdag, 'Mobility-based communication in wireless sensor networks,' *IEEE Communications Magazine*, vol. 44, no. 7, pp. 56–62, 2006. DOI: 10.1109/MCOM.2006.1668382.

[93] L. Tan and M. Wu, 'Data Reduction in Wireless Sensor Networks: A Hierarchical LMS Prediction Approach,' *IEEE Sensors Journal*, vol. 16, no. 6, pp. 1708–1715, 2016. DOI: 10.1109/JSEN.2015.2504106.

[94] K. L. Ketshabetswe, A. M. Zungeru, B. Mtengi, C. K. Lebekwe and S. R. S. Prabaharan, 'Data Compression Algorithms for Wireless Sensor Networks: A Review and Comparison,' *IEEE Access*, vol. 9, pp. 136 872–136 891, 2021. DOI: 10.1109/ACCESS.2021.3116311.

[95] H. Jiang, S. Jin and C. Wang, 'Prediction or Not? An Energy-Efficient Framework for Clustering-Based Data Collection in Wireless Sensor Networks,' *IEEE Transactions on Parallel and Distributed Systems*, vol. 22, no. 6, pp. 1064–1071, 2011. DOI: 10.1109/TPDS.2010.174.

[96] M. Mohamed, W. Wu and M. Moniri, 'Data Reduction Methods for Wireless Smart Sensors in Monitoring Water Distribution Systems,' *Procedia Engineering*, vol. 70, pp. 1166–1172, 2014, 12th International Conference on Computing and Control for the Water Industry, CCWI2013, ISSN: 1877-7058. DOI: 10.1016/j.proeng.2014.02.129.

[97] V.-A. Le, L. Nguyen and T. X. Nghiem, 'Multistep Predictions for Adaptive Sampling in Mobile Robotic Sensor Networks Using Proximal ADMM,' *IEEE Access*, vol. 10, pp. 64 850–64 861, 2022. DOI: 10.1109/ACCESS.2022.3183680.

[98] C. Alippi, G. Anastasi, C. Galperti, F. Mancini and M. Roveri, 'Adaptive Sampling for Energy Conservation in Wireless Sensor Networks for Snow Monitoring Applications,' in *2007 IEEE International Conference on Mobile Adhoc and Sensor Systems*, 2007, pp. 1–6. DOI: 10.1109/MOBHOC.2007.4428700.

[99] H. Karl and A. Willig, *Protocols and architectures for wireless sensor networks*. John Wiley & Sons, 2007, ch. 10.

[100] P. Santi, 'Topology Control in Wireless Ad Hoc and Sensor Networks,' *ACM Comput. Surv.*, vol. 37, no. 2, pp. 164–194, Jun. 2005, ISSN: 0360-0300. DOI: 10.1145/1089733.1089736.

[101] J. Oller, I. Demirkol, J. Casademont, J. Paradells, G. U. Gamm and L. Reindl, 'Has Time Come to Switch From Duty-Cycled MAC Protocols to Wake-Up Radio for Wireless Sensor Networks?' *IEEE/ACM Transactions on Networking*, vol. 24, no. 2, pp. 674–687, 2016. DOI: 10.1109/TNET.2014.2387314.

[102] W. Ye, J. Heidemann and D. Estrin, 'An energy-efficient MAC protocol for wireless sensor networks,' in *Proceedings.Twenty-First Annual Joint Conference of the IEEE Computer and Communications Societies*, vol. 3, 2002, 1567–1576 vol.3. DOI: 10.1109/INFCOM.2002.1019408.

[103] J. Deng, Y. S. Han, W. B. Heinzelman and P. K. Varshney, 'Scheduling sleeping nodes in high density cluster-based sensor networks,' *Mobile Networks and Applications*, vol. 10, no. 6, pp. 825–835, 2005. DOI: 10.1007/s11036-005-4441-9.

[104] R. Dahiya, A. Arora and V. Singh, 'Modelling the energy efficient sensor nodes for wireless sensor networks,' *Journal of The Institution of Engineers (India): Series B*, vol. 96, no. 3, pp. 305–309, 2015. DOI: 10.1007/s40031-014-0149-1.

[105] L. Wang and Y. Xiao, 'Energy saving mechanisms in sensor networks,' in *2nd International Conference on Broadband Networks, 2005.*, 2005, 724–732 Vol. 1. DOI: 10.1109/ICBN.2005.1589678.

[106] F. Z. Djiroun and D. Djenouri, 'MAC Protocols With Wake-Up Radio for Wireless Sensor Networks: A Review,' *IEEE Communications Surveys & Tutorials*, vol. 19, no. 1, pp. 587–618, 2017. DOI: 10.1109/COMST.2016.2612644.

[107] G. Kim, Y. Lee, S. Bang *et al.*, 'A 695 pW standby power optical wake-up receiver for wireless sensor nodes,' in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, 2012, pp. 1–4. DOI: 10.1109/CICC.2012.6330603.

[108] F. Pop, B. Herrera, W. Zhu *et al.*, 'Zero-Power Acoustic Wake-Up Receiver Based on DMUT Transmitter, PMUTS Arrays Receivers and MEMS Switches for Intrabody Links,' in *2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems Eurosensors XXXIII (TRANSDUCERS EUROSENSORS XXXIII)*, 2019, pp. 150–153. DOI: 10.1109/TRANSDUCERS.2019.8808176.

[109] D. Shetty, C. Steffan, G. Holweg, W. Bösch and J. Grosinger, 'Submicrowatt CMOS Rectifier for a Fully Passive Wake-Up Receiver,' *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 11, pp. 4803–4812, 2021. DOI: 10.1109/TMTT.2021.3098694.

[110] V. Mangal and P. R. Kinget, 'Sub-nW Wake-Up Receivers With Gate-Biased Self-Mixers and Time-Encoded Signal Processing,' *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3513–3524, 2019. DOI: 10.1109/JSSC.2019.2941010.

[111] J. Moody, P. Bassirian, A. Roy *et al.*, 'Interference Robust Detector-First Near-Zero Power Wake-Up Receiver,' *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2149–2162, 2019. DOI: 10.1109/JSSC.2019.2912710.

[112] U. Dudko and L. Overmeyer, 'Optical Wake-Up From Power-Off State for Autonomous Sensor Nodes,' *IEEE Sensors Journal*, vol. 21, no. 3, pp. 3225–3232, 2021. DOI: 10.1109/JSEN.2020.3023817.

[113] I. Ozkaya, A. Cevrero, P. A. Francese *et al.*, 'A 56Gb/s burst-mode NRZ optical receiver with 6.8ns power-on and CDR-Lock time for adaptive optical links in 14nm FinFET CMOS,' in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 266–268. DOI: 10.1109/ISSCC.2018.8310286.

[114] S. Yee, Y. C. Wong, S. L. Loh and H. Zhang, 'On-chip ultra low power optical wake-up receiver for wireless sensor nodes targeting structural health monitoring,' *TELKOMNIKA (Telecommunication Computing Electronics and Control)*, vol. 18, p. 2257, Oct. 2020. DOI: 10.12928/telkomnika.v18i5.13378.

[115] Y. C. Wong, S. Tan, R. S. S. Singh, H. Zhang, A. R. Syafeeza and N. A. Hamid, 'Low power wake-up receiver based on ultrasound communication for wireless sensor network,' *Bulletin of Electrical Engineering and Informatics*, vol. 9, no. 1, pp. 21–29, 2020, ISSN: 2302-9285. DOI: 10.11591/eei.v9i1.1654.

[116] A. S. Rekhi and A. Arbabian, 'Ultrasonic Wake-Up With Precharged Transducers,' *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1475–1486, 2019. DOI: 10.1109/JSSC.2019.2892617.

[117] X. Che, I. Wells, G. Dickers, P. Kear and X. Gong, 'Re-evaluation of RF electromagnetic communication in underwater sensor networks,' *IEEE Communications Magazine*, vol. 48, no. 12, pp. 143–151, 2010. DOI: 10.1109/MCOM.2010.5673085.

[118] X. Fu, C. Ross and K. El-Sankary, 'A Super-Regenerative-Oscillator Wake-up Receiver for Underwater Applications with Improved PVT Immunity,' *Analog Integr. Circuits Signal Process.*, vol. 100, no. 3, pp. 593–611, Sep. 2019, ISSN: 0925-1030. DOI: 10.1007/s10470-019-01504-z.

[119] J. Shen, J. Wang, C. Yu *et al.*, 'Single LED-based 46-m underwater wireless optical communication enabled by a multi-pixel photon counter with digital output,' *Optics Communications*, vol. 438, pp. 78–82, 2019, ISSN: 0030-4018. DOI: 10.1016/j.optcom.2019.01.031.

[120] M. Zhao, X. Li, X. Chen *et al.*, 'Long-reach underwater wireless optical communication with relaxed link alignment enabled by optical combination and arrayed sensitive receivers,' *Opt. Express*, vol. 28, no. 23, pp. 34 450–34 460, Nov. 2020. DOI: 10.1364/OE.410026.

[121] G. Schirripa Spagnolo, L. Cozzella and F. Leccese, 'Underwater Optical Wireless Communications: Overview,' *Sensors*, vol. 20, no. 8, 2020, ISSN: 1424-8220. DOI: 10.3390/s20082261.

[122] N. Saeed, A. Celik, T. Y. Al-Naffouri and M.-S. Alouini, 'Underwater optical wireless communications, networking, and localization: A survey,' *Ad Hoc Networks*, vol. 94, p. 101 935, 2019, ISSN: 1570-8705. DOI: 10.1016/j.adhoc.2019.101935.

[123] M. O. Khan, A. A. Syed, W. Ye, J. Heidemann and J. Wills, 'Bringing Sensor Networks Underwater with Low-Power Acoustic Communications,' in *Proceedings of the 6th ACM Conference on Embedded Network Sensor Systems*, ser. SenSys '08, Raleigh, NC, USA: Association for Computing Machinery, 2008, pp. 379–380, ISBN: 9781595939906. DOI: 10.1145/1460412.1460461.

[124] K. Yadav, I. Kymissis and P. R. Kinget, 'A 4.4-μW Wake-Up Receiver Using Ultrasound Data,' *IEEE Journal of Solid-State Circuits*, vol. 48, no. 3, pp. 649–660, 2013. DOI: 10.1109/JSSC.2012.2235671.

[125] A. Sánchez, S. Blanc, P. Yuste, A. Perles and J. J. Serrano, 'An Ultra-Low Power and Flexible Acoustic Modem Design to Develop Energy-Efficient Underwater Sensor Networks,' *Sensors*, vol. 12, no. 6, pp. 6837–6856, 2012, ISSN: 1424-8220. DOI: 10.3390/s120606837.

[126] E. Lattanzi, M. Dromedari, V. Freschi and A. Bogliolo, 'A Sub-μA Ultrasonic Wake-Up Trigger with Addressing Capability for Wireless Sensor Nodes,' *ISRN Sensor Networks*, vol. 2013, pp. 1–10, 2013. DOI: 10.1155/2013/720817.

[127] F. Höflinger, G. U. Gamm, J. Albesa and L. M. Reindl, 'Smartphone remote control for home automation applications based on acoustic wake-up receivers,' in *2014 IEEE International Instrumentation and Measurement Technology Conference (I2MTC) Proceedings*, 2014, pp. 1580–1583. DOI: 10.1109/I2MTC.2014.6861012.

[128] A. Bannoura, F. Höflinger, O. Gorgies, G. U. Gamm, J. Albesa and L. M. Reindl, 'Acoustic Wake-Up Receivers for Home Automation Control Applications,' *Electronics*, vol. 5, no. 1, 2016, ISSN: 2079-9292. DOI: 10.3390/electronics5010004.

[129] H. Fuketa, S. O'uchi and T. Matsukawa, 'A 0.3-V 1-μW Super-Regenerative Ultrasound Wake-Up Receiver With Power Scalability,' *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 9, pp. 1027–1031, 2017. DOI: 10.1109/TCSII.2016.2621772.

[130] D. Oletic, L. Korman, M. Magno and V. Bilas, 'Time-frequency pattern wake-up detector for low-power always-on sensing of acoustic events,' in *2018 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, 2018, pp. 1–6. DOI: 10.1109/I2MTC.2018.8409577.

[131] D. Oletic, M. Gazivoda and V. Bilas, 'A Programmable 3-Channel Acoustic Wake-Up Interface Enabling Always-On Detection of Underwater Events within 20 µA,' *Proceedings*, vol. 2, no. 13, 2018, ISSN: 2504-3900. DOI: 10.3390/proceedings2130768.

[132] G. U. Gamm, M. Sippel, M. Kostic and L. M. Reindl, 'Low power wake-up receiver for wireless sensor nodes,' in *2010 Sixth International Conference on Intelligent Sensors, Sensor Networks and Information Processing*, 2010, pp. 121–126. DOI: 10.1109/ISSNIP.2010.5706778.

[133] M. Valentinuzzi, 'Otto Herbert Arnold Schmitt (1913-1998), a pioneer (an overview of Schmitt's scientific production),' *IEEE Engineering in Medicine and Biology Magazine*, vol. 23, no. 6, pp. 42–46, 2004. DOI: 10.1109/MEMB.2004.1378632.

[134] O. H. Schmitt, 'A thermionic trigger,' *Journal of Scientific instruments*, vol. 15, no. 1, p. 24, 1938.

[135] J. M. Harkness, 'A Lifetime of Connections: Otto Herbert Schmitt, 1913-1998,' *Physics in Perspective*, vol. 4, no. 4, pp. 456–490, 2002. DOI: 10.1007/s000160200005.

[136] H. A. Alzaher, 'Novel Schmitt Trigger and Square-Wave Generator Using Single Current Amplifier,' *IEEE Access*, vol. 7, pp. 186 175–186 181, 2019. DOI: 10.1109/ACCESS.2019.2961640.

[137] A. Panda, A. K. Singh, R. Tirupathi and S. K. Kar, 'A Low-Power Tunable Square-Wave Generator for Instrumentation Applications,' *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 7, pp. 5051–5057, 2020. DOI: 10.1109/TIM.2019.2954236.

[138] W.-S. Chung, H. Kim, H.-W. Cha and H.-J. Kim, 'Triangular/square-wave generator with independently controllable frequency and amplitude,' *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 1, pp. 105–109, 2005. DOI: 10.1109/TIM.2004.840238.

[139] I. A. A. Al-Darkazly and S. M. R. Hasan, 'Dual-Band Waveform Generator With Ultra-Wide Low-Frequency Tuning-Range,' *IEEE Access*, vol. 4, pp. 3169–3181, 2016. DOI: 10.1109/ACCESS.2016.2557843.

[140] A. Chaney and R. Sundararajan, 'Simple MOSFET-based high-voltage nanosecond pulse circuit,' *IEEE Transactions on Plasma Science*, vol. 32, no. 5, pp. 1919–1924, 2004. DOI: 10.1109/TPS.2004.835966.

[141] M. Abuelma'atti, S. Buhalim and H. Alzaher, 'A novel single-capacitor single-operational-amplifier sinusoidal oscillator,' *IEEE Transactions on Education*, vol. 38, no. 4, pp. 391–393, 1995. DOI: 10.1109/13.473163.

[142] M. Siniscalchi, F. Silveira and C. Galup-Montoro, 'Ultra-Low-Voltage CMOS Crystal Oscillators,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 6, pp. 1846–1856, 2020. DOI: 10.1109/TCSI.2020.2971110.

[143] E. Abbasian, F. Izadinasab and M. Gholipour, 'A Reliable Low Standby Power 10T SRAM Cell With Expanded Static Noise Margins,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 4, pp. 1606–1616, 2022. DOI: 10.1109/TCSI.2021.3138849.

[144] R. Pandey, V. Saripalli, J. P. Kulkarni, V. Narayanan and S. Datta, 'Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability,' *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 393–395, 2014. DOI: 10.1109/LED.2014.2300193.

[145] A. Sekiyama, T. Seki, S. Nagai, A. Iwase, N. Suzuki and M. Hayasaka, 'A 1-V operating 256-kb full-CMOS SRAM,' *IEEE Journal of Solid-State Circuits*, vol. 27, no. 5, pp. 776–782, 1992. DOI: 10.1109/4.133168.

[146] Y.-C. Lai and S.-Y. Huang, 'A Resilient and Power-Efficient Automatic-Power-Down Sense Amplifier for SRAM Design,' *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 10, pp. 1031–1035, 2008. DOI: 10.1109/TCSII.2008.926797.

[147] M. Glorieux, S. Clerc, G. Gasiot, J.-L. Autran and P. Roche, 'New D-Flip-Flop Design in 65 nm CMOS for Improved SEU and Low Power Overhead at System Level,' *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4381–4386, 2013. DOI: 10.1109/TNS.2013.2284604.

[148] S. Lin, Y.-B. Kim and F. Lombardi, 'Analysis and Design of Nanoscale CMOS Storage Elements for Single-Event Hardening With Multiple-Node Upset,' *IEEE Transactions on Device and Materials Reliability*, vol. 12, no. 1, pp. 68–77, 2012. DOI: 10.1109/TDMR.2011.2167233.

[149] M. Moghaddam, M. H. Moaiyeri and M. Eshghi, 'Design and Evaluation of an Efficient Schmitt Trigger-Based Hardened Latch in CNTFET Technology,' *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 267–277, 2017. DOI: 10.1109/TDMR.2017.2665780.

[150] W.-S. Chung, H.-W. Cha and H.-J. Kim, 'Current-controllable monostable multivibrator using OTAs,' *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 5, pp. 703–705, 2002. DOI: 10.1109/TCSI.2002.1001963.

[151] A. Paidimarri, D. Griffith, A. Wang, G. Burra and A. P. Chandrakasan, 'An RC Oscillator With Comparator Offset Cancellation,' *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1866–1877, 2016. DOI: 10.1109/JSSC.2016.2559508.

[152] A. Kochhar, M. E. Galanko, M. Soliman *et al.*, 'Resonant Microelectromechanical Receiver,' *Journal of Microelectromechanical Systems*, vol. 28, no. 3, pp. 327–343, 2019. DOI: 10.1109/JMEMS.2019.2898984.

[153] A. M. Elgani, F. Renzini, L. Perilli *et al.*, 'A Clockless Temperature-Compensated Nanowatt Analog Front-End for Wake-Up Radios Based on a Band-Pass Envelope Detector,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 8, pp. 2612–2624, 2020. DOI: 10.1109/TCSI.2020.2987850.

[154] H. Kim, W.-S. Chung, H.-J. Kim and S.-H. Son, 'A Resistance Deviation-to-Pulsewidth Converter for Resistive Sensors,' *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 2, pp. 397–400, 2009. DOI: 10.1109/TIM.2008.2003318.

[155] G. Di Cataldo and G. Palumbo, 'A theoretical approach to the design of A/D converter by means of Schmitt triggers,' *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 39, no. 2, pp. 126–129, 1992. DOI: 10.1109/82.205819.

[156] A. Bonanno, M. Crepaldi, I. Rattalino, P. Motto, D. Demarchi and P. Civera, 'A 0.13 µm CMOS Operational Schmitt Trigger R-to-F Converter for Nanogap-Based Nanosensors Read-Out,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 4, pp. 975–988, 2013. DOI: 10.1109/TCSI.2012.2220455.

[157] E. D. Kyriakis-Bitzaros, N. A. Stathopoulos, S. Pavlos, D. Goustouridis and S. Chatzandroulis, 'A Reconfigurable Multichannel Capacitive Sensor Array Interface,' *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 9, pp. 3214–3221, 2011. DOI: 10.1109/TIM.2011.2123170.

[158] Y. Xu, W. Zhong, B. Li *et al.*, 'An Integrator and Schmitt Trigger Based Voltage-to-Frequency Converter Using Unipolar Metal-Oxide Thin Film Transistors,' *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 144–150, 2021. DOI: 10.1109/JEDS.2020.3045160.

[159] J.-H. Jung, S.-K. Hong and O.-K. Kwon, 'A Highly Reliable SIMO Converter Using Hybrid Starter and Overcharging Protector for Energy Harvesting Systems,' *IEEE Access*, vol. 8, pp. 162 172–162 179, 2020. DOI: 10.1109/ACCESS.2020.3021230.

[160] M. Karimi, M. Ali, A. Hassan, M. Sawan and B. Gosselin, 'An Active Dead-Time Control Circuit With Timing Elements for a 45-V Input 1-MHz Half-Bridge Converter,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 1, pp. 30–41, 2022. DOI: 10.1109/TCSI.2021.3096522.

[161] J. Goeppert and Y. Manoli, 'Fully Integrated Startup at 70 mV of Boost Converters for Thermoelectric Energy Harvesting,' *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1716–1726, 2016. DOI: 10.1109/JSSC.2016.2563782.

[162] Z. Tang, Y. Fang, Z. Shi, X.-P. Yu, N. N. Tan and W. Pan, 'A 1770-µm^2 Leakage-Based Digital Temperature Sensor With Supply Sensitivity Suppression in 55-nm CMOS,' *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 781–793, 2020. DOI: 10.1109/JSSC.2019.2952855.

[163] J. Hu, B. Liu, R. Ma, M. Liu and Z. Zhu, 'A 32 × 32-Pixel Flash LiDAR Sensor With Noise Filtering for High-Background Noise Applications,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 2, pp. 645–656, 2022. DOI: 10.1109/TCSI.2020.3048367.

[164] Z. Tang, Z. Huang, X.-P. Yu, Z. Shi and N. N. Tan, 'A 0.26-pJ $\cdot$ k^2 2400-μm^2 Digital Temperature Sensor in 55-nm CMOS,' *IEEE Solid-State Circuits Letters*, vol. 4, pp. 96–99, 2021. DOI: 10.1109/LSSC.2021.3072989.

[165] E. Rahiminejad, A. Parvizi-Fard, M. M. Iskarous, N. V. Thakor and M. Amiri, 'A Biomimetic Circuit for Electronic Skin With Application in Hand Prosthesis,' *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 29, pp. 2333–2344, 2021. DOI: 10.1109/TNSRE.2021.3120446.

[166] S. Malik, K. Kishore, L. Somappa *et al.*, 'A Dual-Slope-Based Capacitance-to-Time Signal Conditioning Circuit for Leaky Capacitive Sensors,' *IEEE Transactions on Instrumentation and Measurement*, vol. 70, pp. 1–8, 2021. DOI: 10.1109/TIM.2021.3101325.

[167] Y. Sui, A. C. Benken, Y. Ma, A. Trickey-Glassman, T. Li and Y. B. Gianchandani, 'An Autonomous Environmental Logging Microsystem (ELM) for Harsh Environments,' *IEEE Sensors Journal*, vol. 21, no. 18, pp. 20 796–20 806, 2021. DOI: 10.1109/JSEN.2021.3095143.

[168] S.-Y. Lu and Y.-T. Liao, 'A 19µW, 50 kS/s, 0.008-400 V/s Cyclic Voltammetry Readout Interface With a Current Feedback Loop and On-Chip Pattern generation,' *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 2, pp. 190–198, 2021. DOI: 10.1109/TBCAS.2021.3062377.

[169] J. P. Kulkarni, K. Kim and K. Roy, 'A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM,' *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, 2007. DOI: 10.1109/JSSC.2007.897148.

[170] N. Lotze and Y. Manoli, 'A 62 mV 0.13µ m CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic,' *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, 2012. DOI: 10.1109/JSSC.2011.2167777.

[171] L. A. Pasini Melek, M. C. Schneider and C. Galup-Montoro, 'Operation of the Classical CMOS Schmitt Trigger As an Ultra-Low-Voltage Amplifier,' *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1239–1243, 2018. DOI: 10.1109/TCSII.2017.2783975.

[172] Y. Bastan, A. Nejati, S. Radfar, P. Amiri, M. Nasrollahpour and S. Hamedi-Hagh, 'An Ultra-Low-Voltage Sub-Threshold Pseudo-Differential CMOS Schmitt Trigger,' in *2018 31st IEEE International System-on-Chip Conference (SOCC)*, 2018, pp. 1–5. DOI: 10.1109/SOCC.2018.8618561.

[173] S. Radfar, A. Nejati, Y. Bastan *et al.*, 'A Sub-Threshold Differential CMOS Schmitt Trigger with Adjustable Hysteresis Based on Body Bias Technique,' *Electronics*, vol. 9, no. 5, 2020. DOI: 10.3390/electronics9050806.

[174] A. Nejati, S. Radfar, P. Amiri and M. H. Maghami, 'A bulk-driven differential CMOS schmitt trigger with adjustable hysteresis for ultra-low-voltage operation,' *Microelectronics Journal*, vol. 114, p. 105 129, 2021, ISSN: 0026-2692. DOI: 10.1016/j.mejo.2021.105129.

[175] T. Darós Fernandes, C. Galup-Montoro and M. C. Schneider, 'Analysis and Design of the Three-Inverter Schmitt Trigger for Supply Voltages Down to 50 mV,' *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2302–2306, 2021. DOI: 10.1109/TCSII.2021.3058358.

[176] R. Sandiri, Y. Chimata, Y. Nalamasa and P. Arra, 'Design of Noise Immune Subthreshold Circuits using Dynamic Threshold Schmitt Trigger Logic,' in *2022 IEEE Region 10 Symposium (TENSYMP)*, 2022, pp. 1–6. DOI: 10.1109/TENSYMP54529.2022.9864364.

[177] C. C. Enz, F. Krummenacher and E. A. Vittoz, 'An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications,' *Analog Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, 1995. DOI: 10.1007/BF01239381.

[178] C. C. Enz and E. A. Vittoz, *Charge-based MOS transistor modeling: the EKV model for low-power and RF IC design*. John Wiley & Sons, 2006.

[179] M. A. Eldeeb, Y. H. Ghallab, Y. Ismail and H. Elghitani, 'Low-voltage subthreshold CMOS current mode circuits: Design and applications,' *AEU - International Journal of Electronics and Communications*, vol. 82, pp. 251–264, 2017, ISSN: 1434-8411. DOI: 10.1016/j.aeue.2017.08.049.

[180] M. Alioto, 'Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1597–1607, 2010. DOI: 10.1109/TCSI.2009.2034233.

[181] Y. Zhou, J. Mercier and F. Yuan, 'A Comparative Study Of Injection Locked Frequency Divider Using Harmonic Mixer In Weak And Strong Inversion,' in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018, pp. 97–100. DOI: 10.1109/MWSCAS.2018.8623850.

[182] R. J. E. Hueting, T. Van Hemert, B. Kaleli, R. A. M. Wolters and J. Schmitz, 'On Device Architectures, Subthreshold Swing, and Power Consumption of the Piezoelectric Field-Effect Transistor (π -FET),' *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 149–157, 2015. DOI: 10.1109/JEDS.2015.2409303.

[183] B. H. Calhoun, A. Wang, N. Verma and A. Chandrakasan, 'Sub-Threshold Design: The Challenges of Minimizing Circuit Energy,' in *ISLPED'06 Proceedings of the 2006 International Symposium on Low Power Electronics and Design*, 2006, pp. 366–368. DOI: 10.1145/1165573.1165661.

[184] S. M. Sharroush, 'Analysis of the subthreshold CMOS logic inverter,' *Ain Shams Engineering Journal*, vol. 9, no. 4, pp. 1001–1017, 2018, ISSN: 2090-4479. DOI: 10.1016/j.asej.2016.05.005.

Appendix A

ASIC Layout

A.1 Overview

The ASIC has been fabricated in AMS-350nm CMOS process through Europractice. The design has been performed through Cadence (version 6.1.8-64b, TECH_C35B4). The ASIC has dimension $3\,\text{mm} \times 3\,\text{mm}$, and it is packaged into a ceramic pin grid array (CPGA100). The pads of the ASIC are connected to the pins of the CPGA100 through wire bonding. Standard pads provided by AMS have been implemented. A simplified block diagram showing the connections between the pads of the ASIC and the pins of the CPGA100 is shown in Fig.A.1. The ASIC contains several cells, as can be seen in Fig.A.2. Each cell includes a specific circuit, and each circuit has its own V_{dd} and *GND* pad, to prevent the failure of the entire ASIC in case of short circuits. The cells relevant to this thesis are:

- Cell A $\rightarrow$ *Type A* Wake-Up Receiver;
- Cell B $\rightarrow$ *Type B* Wake-Up Receiver;
- Cell E $\rightarrow$ *Type 2* Schmitt Trigger;
- Cell F $\rightarrow$ *Type 1* Schmitt Trigger.

A micrograph of the entire ASIC is shown in Fig.A.3, where the relevant cells are highlighted. Thirty identical ASICs have been delivered, and ten of them have been packaged.

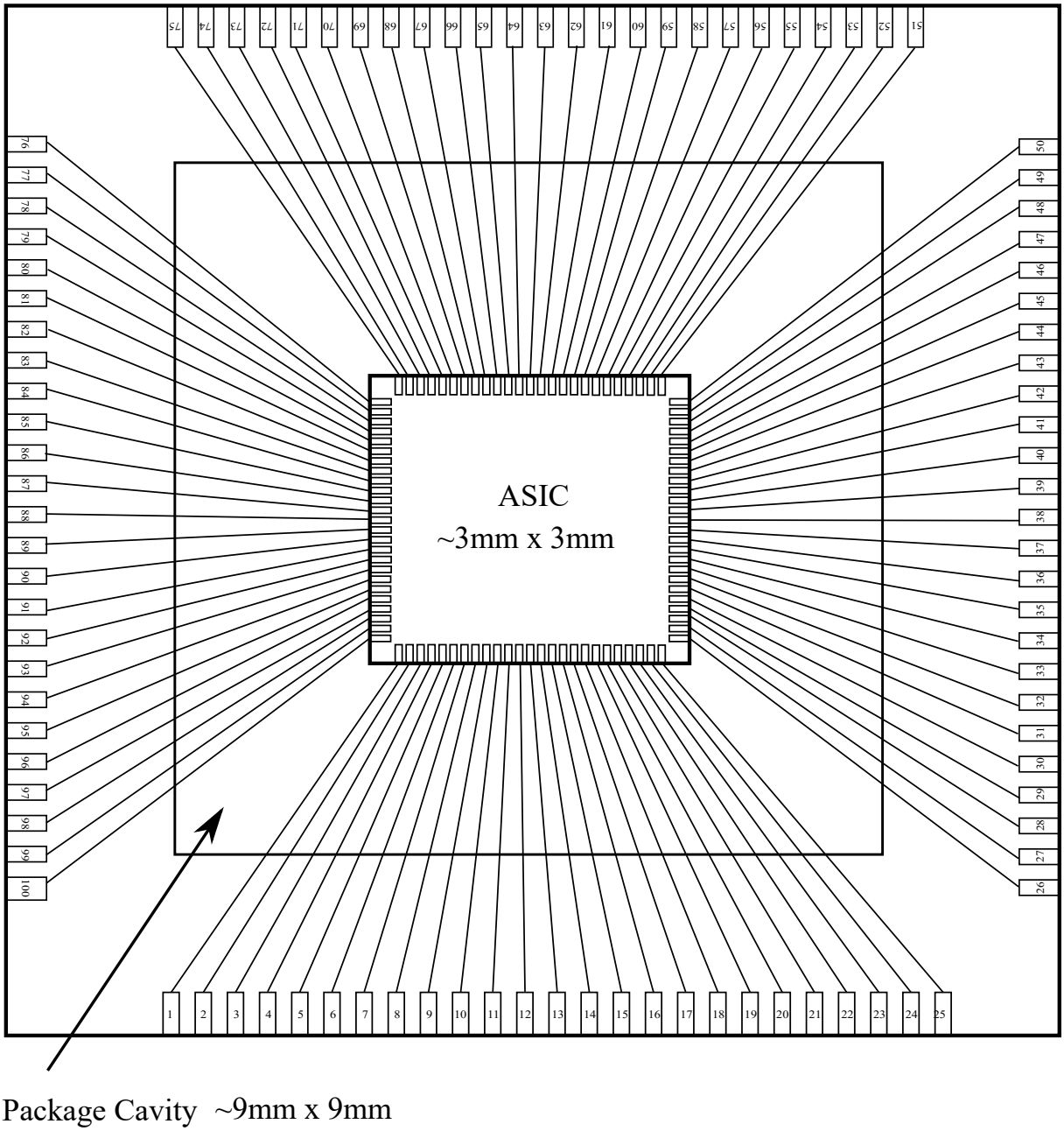


Figure A.1: Simplified block diagram showing the connections between the ASIC and the CPGA100 (not in scale).

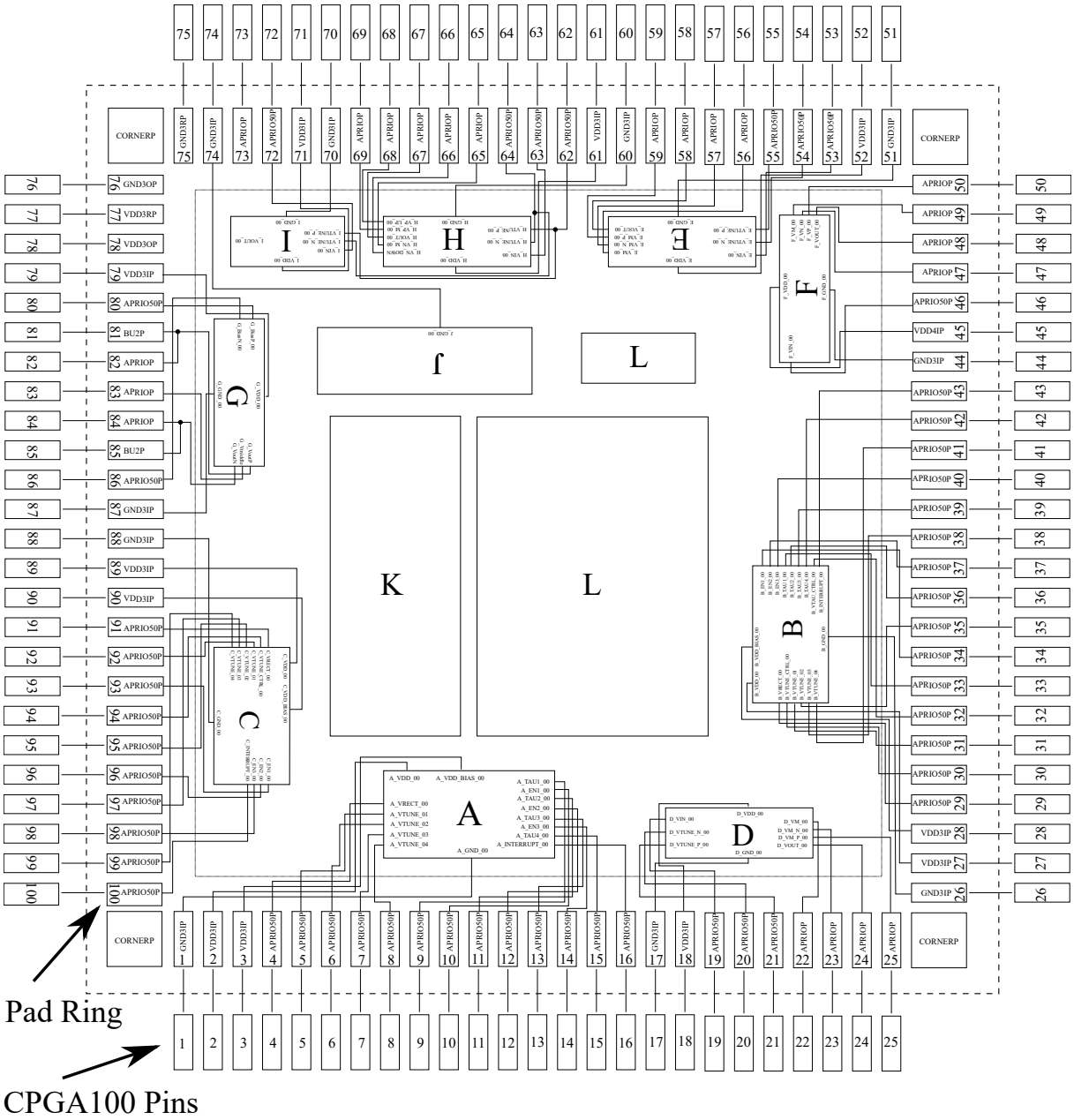


Figure A.2: Simplified block diagram showing the cells included in the designed ASIC (not in scale).

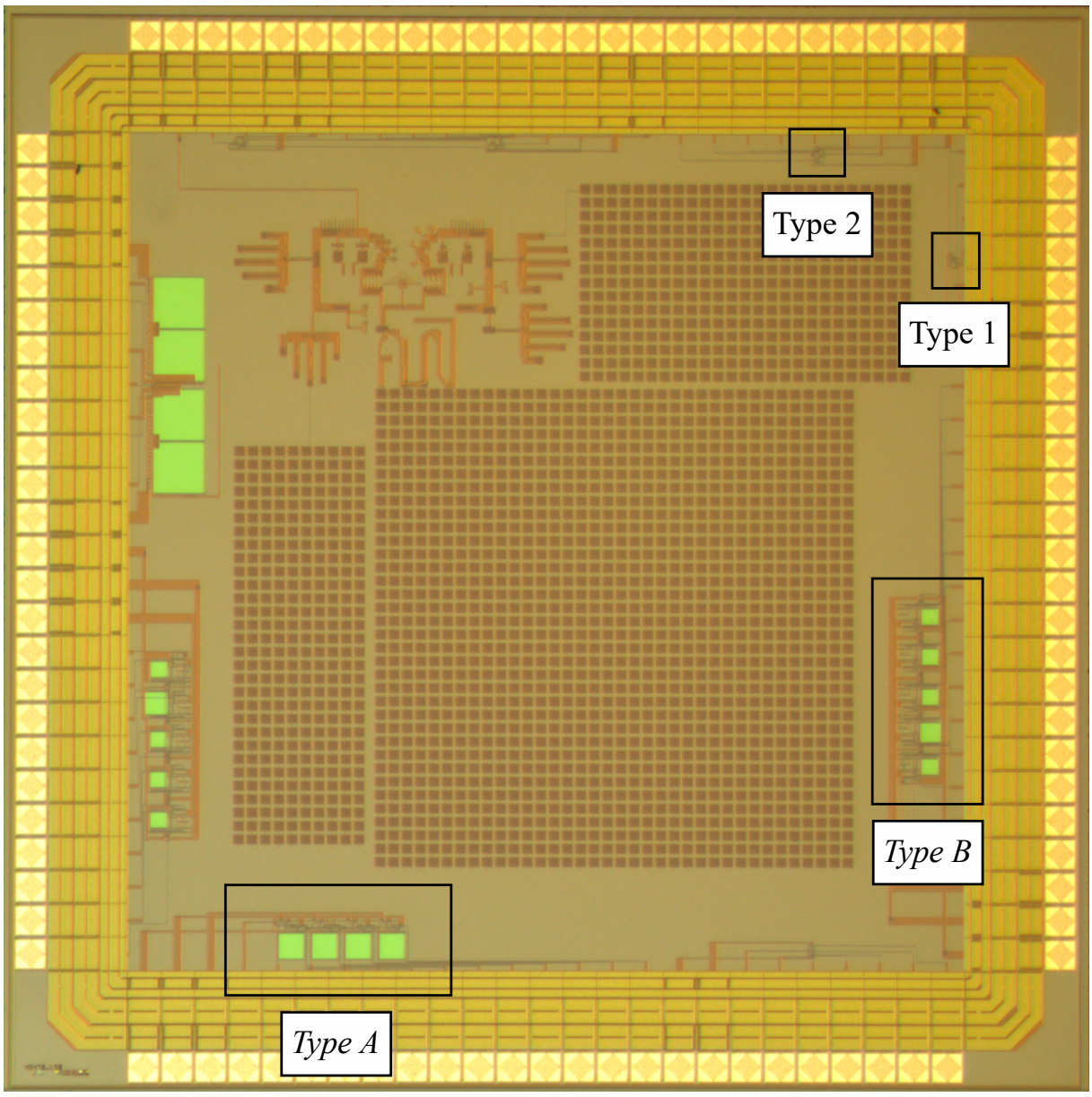


Figure A.3: Micrograph of the ASIC.

A.2 Wake-Up Receivers Layouts

A.2.1 *Type A*

In this section the layout of *Type A*, described in Chapter 2 and [5] (Appendix B.5), is reported. The top cell and the subcells are shown in Fig.A.4. As can be observed, the names associated to the pins do not coincide with those used in Chapter 2. This is due to the fact that only after ASIC tapeout a well defined nomenclature has been developed for the signals and blocks of the designed WuRxs. In the following, the terms *delay line*, *monostable block*, and *pulse block* are to be considered synonyms, i.e. they refer to the blocks which generate the reference signals for WuC signal decoding. The pins indicated in Fig.A.4 are the only ones that can be accessed during the measurements. As can be observed, there are two supply voltages, i.e. ***V_DD*** and ***A_VDD_BIAS***. This design choice has been performed in order to distinguish the power consumption of the bias stage from that of the other stages during the measurement phase. The output of the rectifier stage, which has been implemented through discrete components as described in [5], is the input of the WuRx, i.e. ***A_VRECT***. For each monostable block, a specific pin for the tuning voltage has been implemented. This design choice has been performed in order to allow flexibility while tuning, i.e. process variations can cause the various monostable blocks to behave differently in terms of timing. The pins associated to the enable signals of the logic gate blocks are called ***A_EN***s, while the pins associated to the outputs of the monostable blocks, i.e. the reference signals in Fig.2.1(b), are called ***A_TAU***s. The blocks and the circuits associated to the subcells are shown in Fig.A.5.

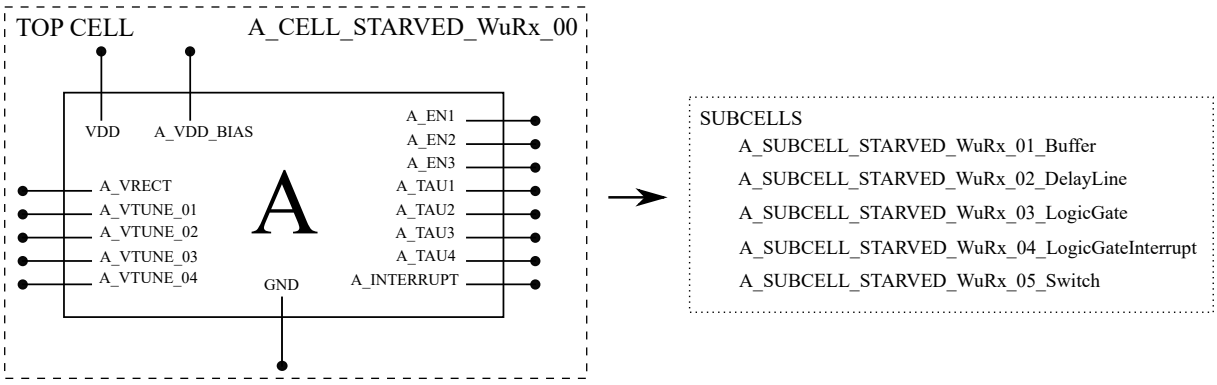


Figure A.4: Top cell and subcells of *Type A*.

The subcells 03 (LogicGate) and 04 (LogicGateInterrupt) are identical in terms of circuit implementation, but they have been distinguished at block diagram level because of pin mapping constraints. The connections between the subcells are shown in Fig.A.6, while their layouts are in Fig.A.7. The capacitor of the delay line is not shown in order to make clearer the layout of the circuitry. No particular layout strategy has been performed. The only concern was to verify that the post-layout and pre-layout performances were similar. The full layout of *Type A*, together with a micrograph, is shown in Fig.A.8. The large squares are the 5 pF capacitors of the delay lines. The circuit occupies an area of 403 µm × 144 µm.

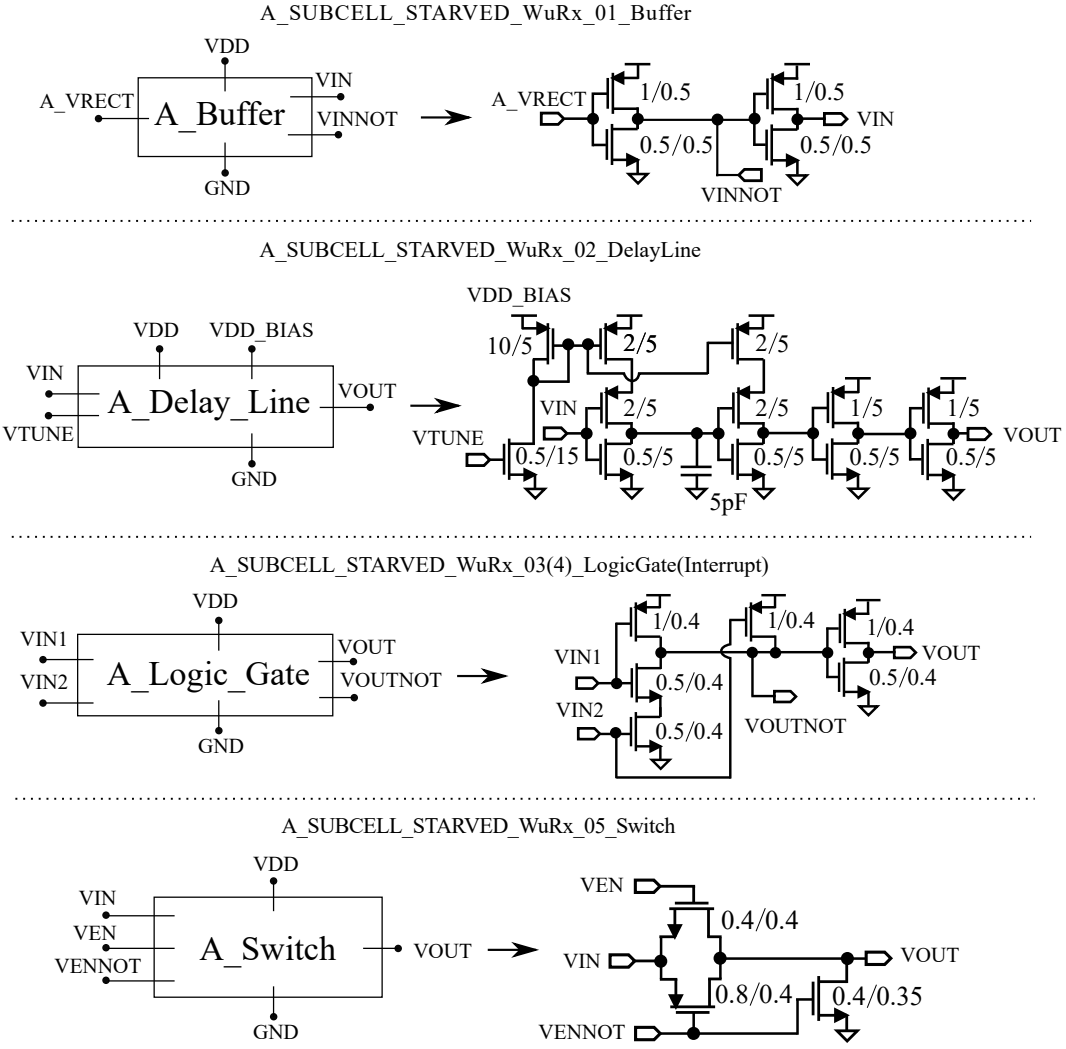


Figure A.5: Blocks and circuits associated to the subcells of *Type A*.

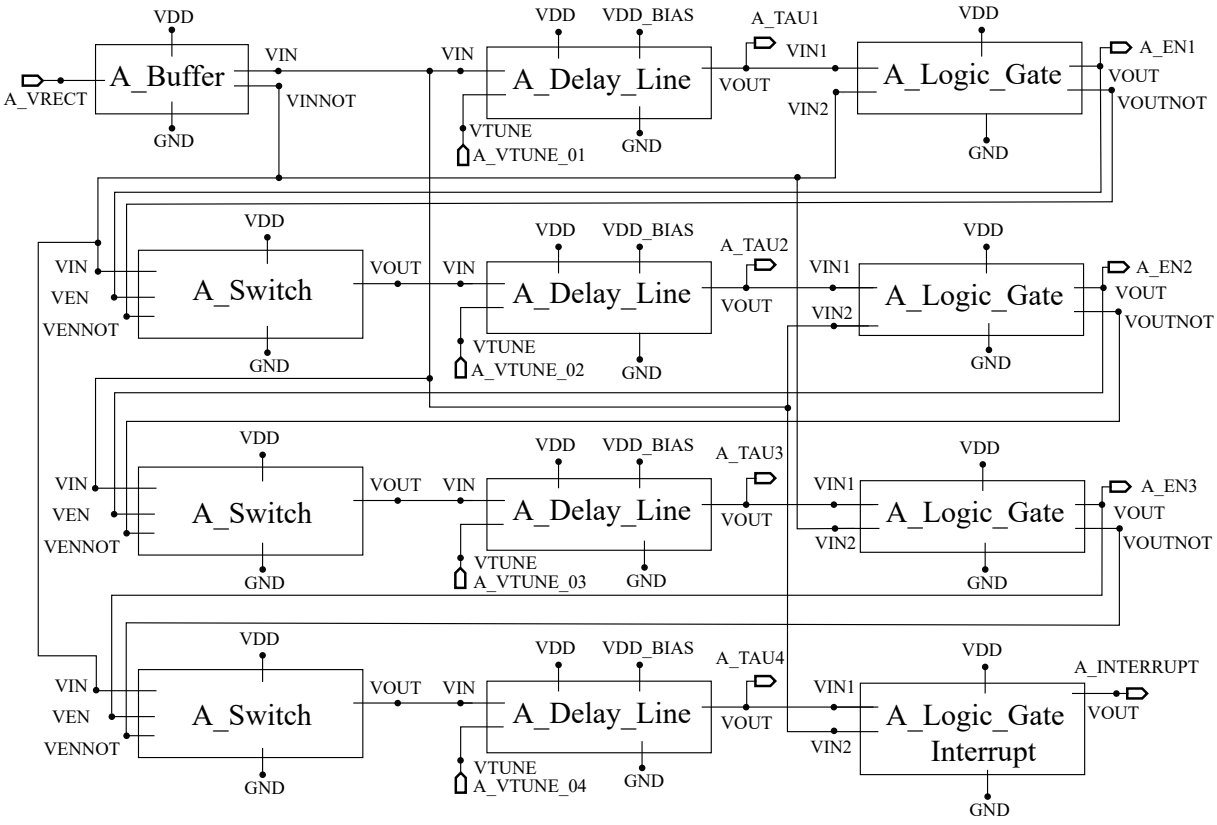


Figure A.6: Subcells connections of *Type A*.

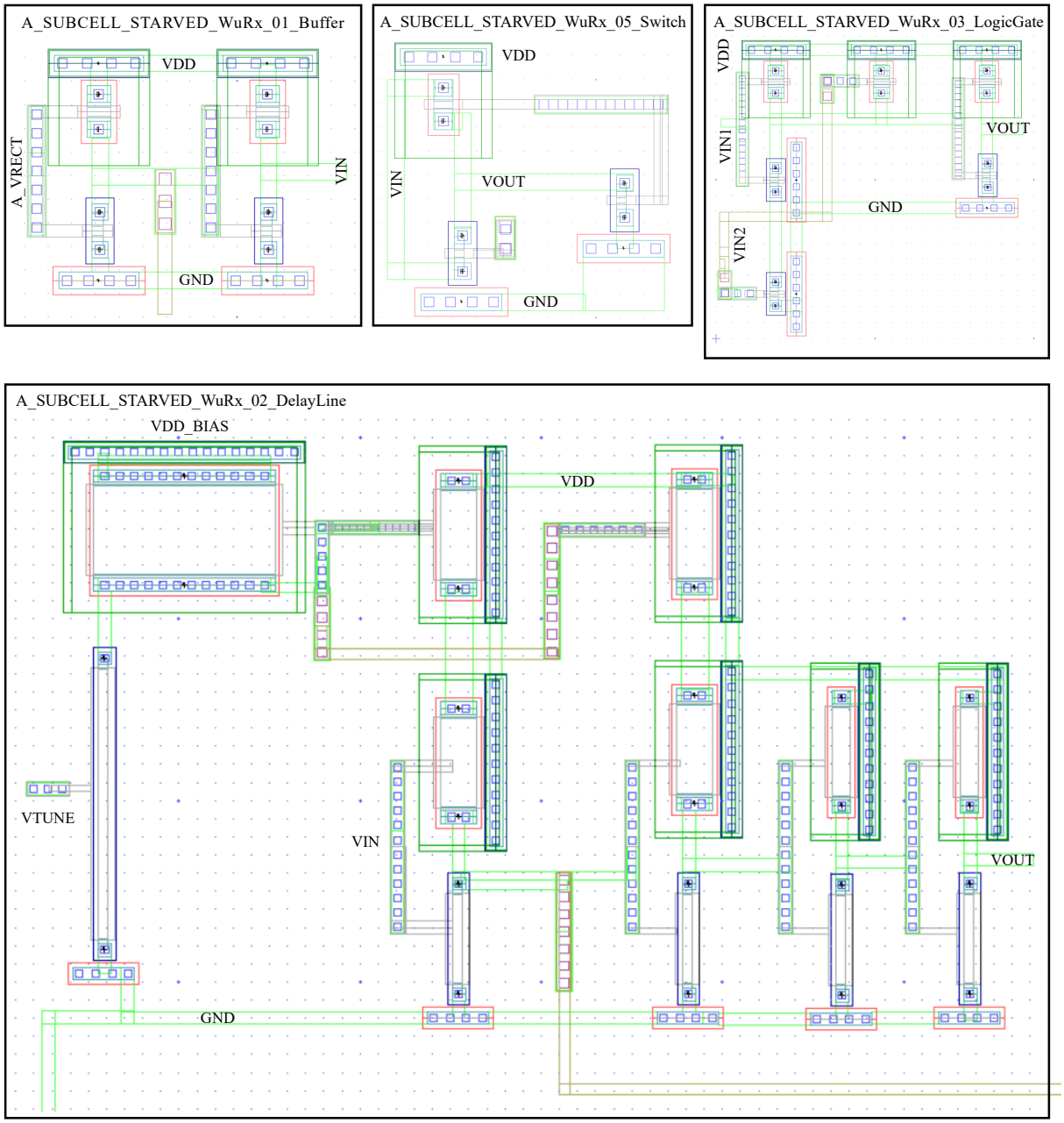


Figure A.7: Layouts of the subcells of *Type A*.

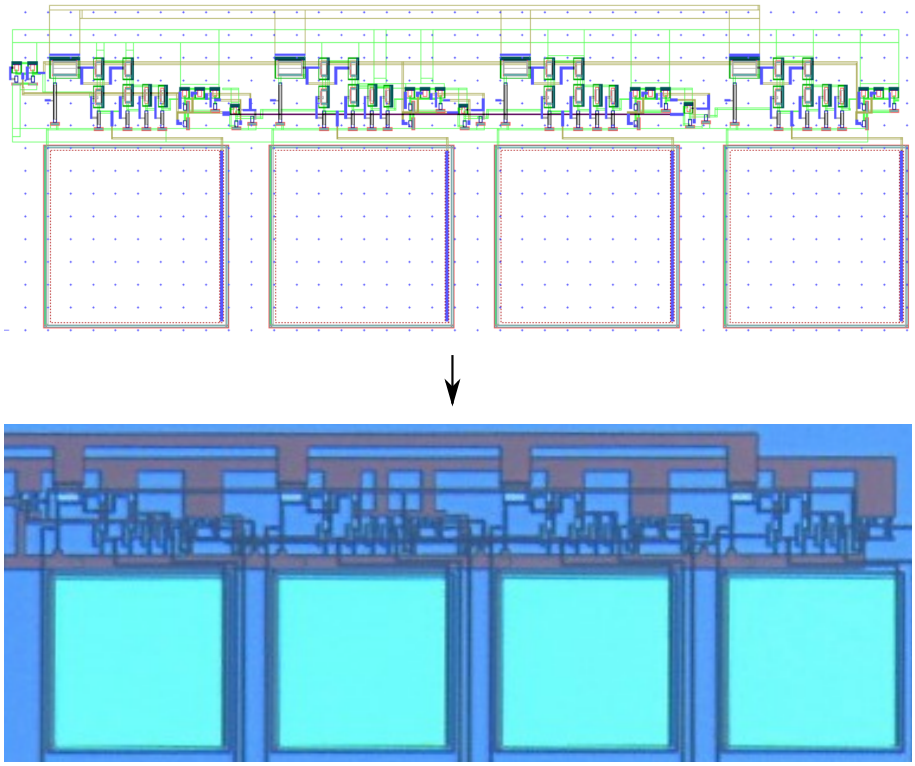


Figure A.8: Full layout and micrograph of *Type A*.

A.2.2 *Type B*

In this section the layout of the *Type B*, described in Chapter 2 and [5] (Appendix B.5), is reported. The top cell and the subcells are shown in Fig.A.9(a). As for *Type A*, the names associated to the pins do not coincide with those used in Chapter 2. In the following, the terms *one shot block*, *multivibrator block*, *monostable block*, and *pulse block* are to be

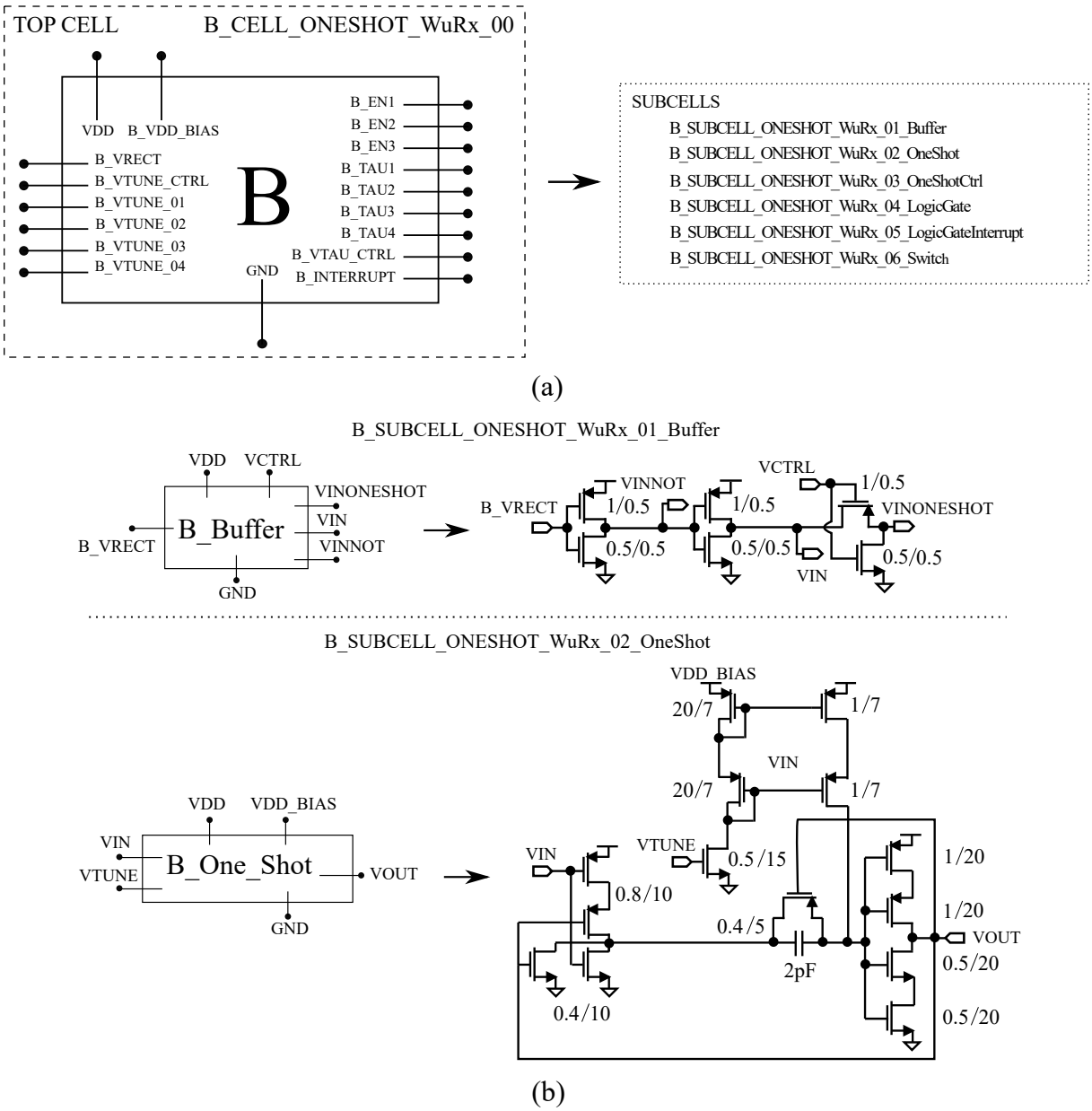


Figure A.9: (a) Top cell and subcells of *Type B*. (b) The circuits which differ from those of *Type A*.

considered synonyms, i.e. they refer to the blocks which generate the reference signals for WuC signal decoding. As for *Type A*, there are two supply voltages, i.e. ***V_DD*** and ***B_VDD_BIAS*** for power consumption measurement. The logic gate and switch blocks of *Type B* are equal to those of *Type A*. The only different circuits are those associated to the buffer and one shot blocks. The subcells 02 (OneShot) and 03 (OneShotCtrl) present similar circuit implementations. The only difference is the capacitance, i.e. the capacitor of OneShotCtrl has a capacitance of 3 pF. The connections between the subcells of *Type B* is shown in Fig.A.10. The layouts of the subcells in Fig.A.9(b) are shown in Fig.A.11. The full layout and micrograph of *Type B* are shown in Fig.A.12. The larger square is that of the control multivibrator.

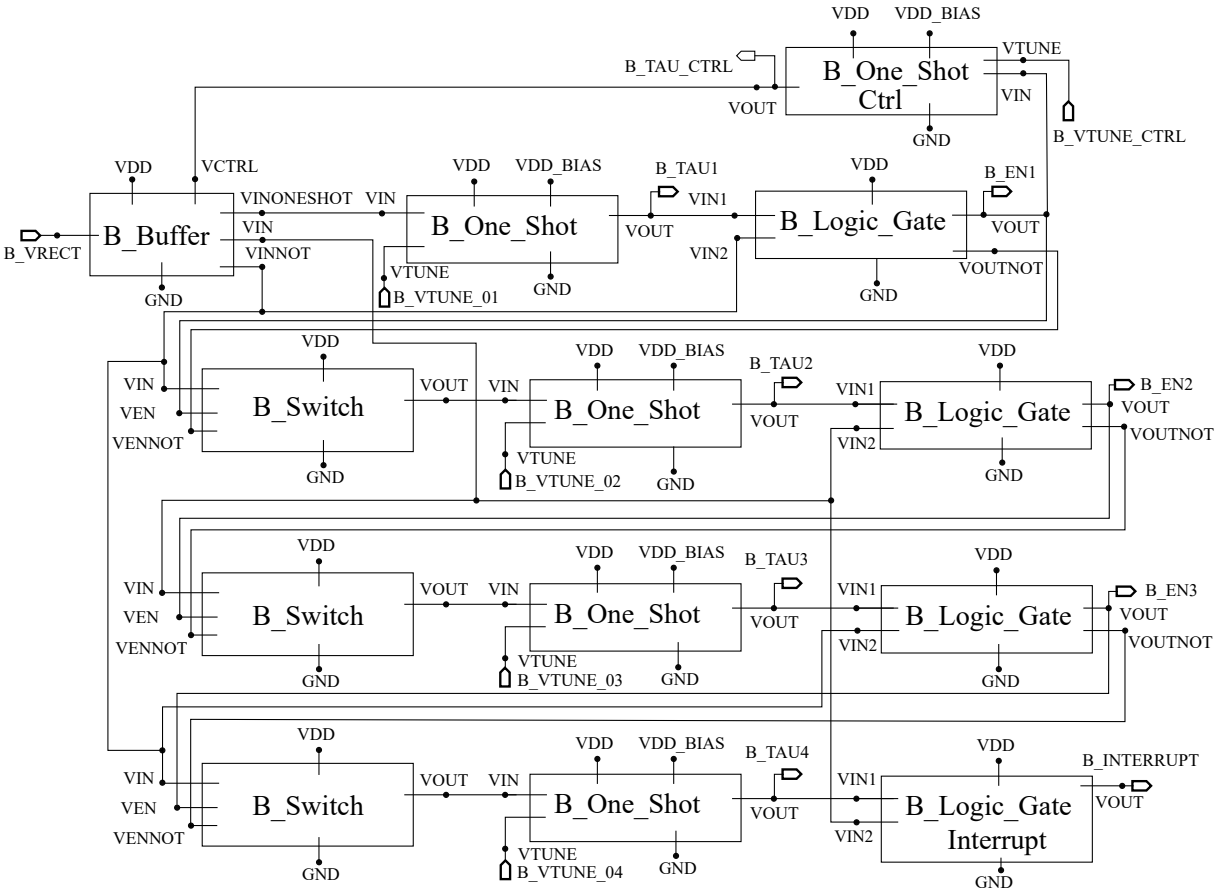


Figure A.10: Subcells connections of *Type B*.

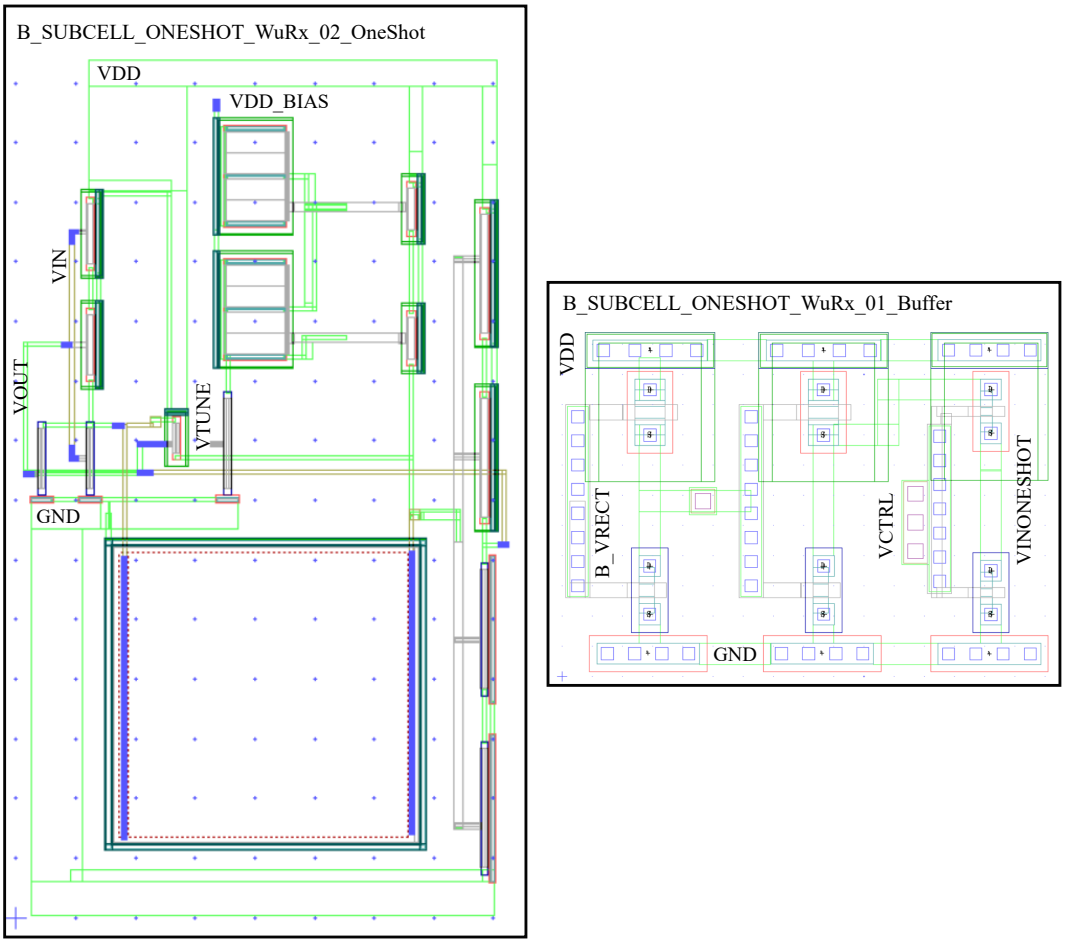


Figure A.11: Layouts of the subcells in Fig.A.9(b) of *Type B*.

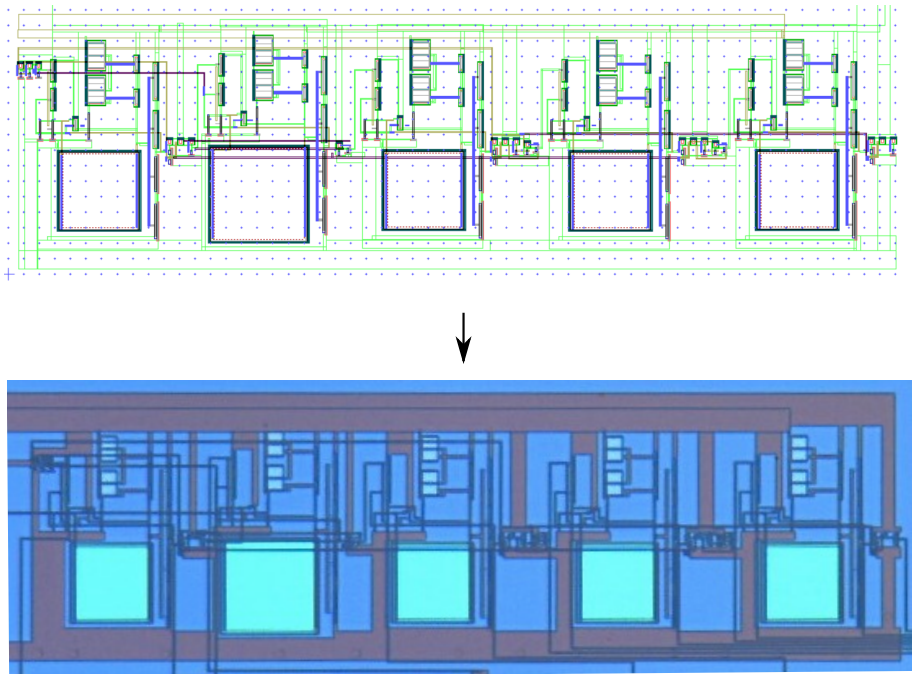


Figure A.12: Full layout and micrograph of *Type B*.

A.3 Schmitt Triggers Layouts

A.3.1 *Type 1* and *Type 2*

In this section the layouts and the micrographs of *Type 1* and *Type 2* are reported. Due to the simple design, only one top cell for each circuit, shown in Fig.A.13(a), has been defined. The layouts and micrographs of *Type 1* and *Type 2* are shown in Figs.A.13(b) and (c), respectively. *Type 1* occupies an area of 49 µm × 25 µm. *Type 2* occupies an area of 42 µm × 45 µm. Due to technological constraints, the PMOS transistors of *Type 2* are fabricated with two gates, each with a 10 µm width stripe.

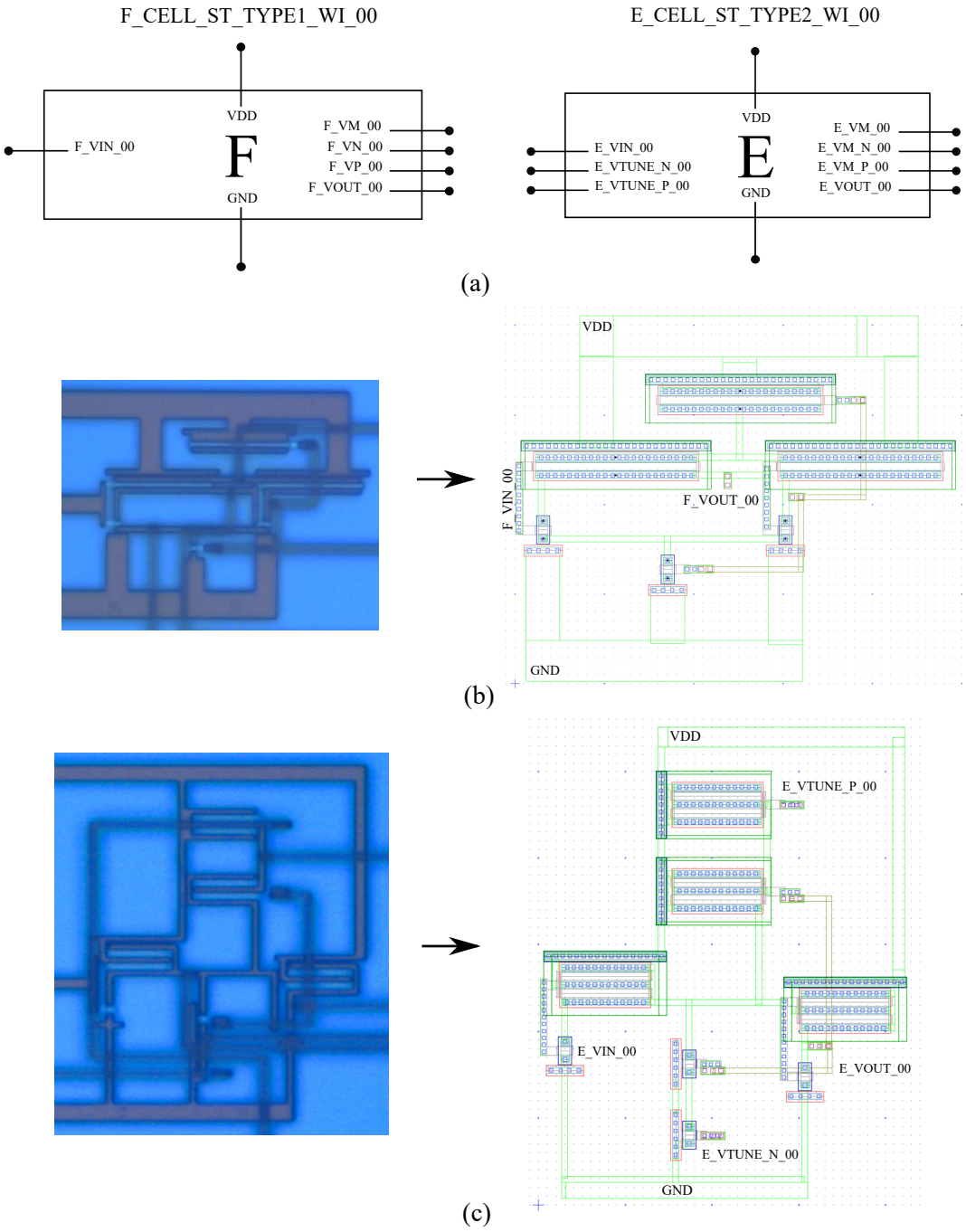


Figure A.13: (a) Top cells of *Type 1* (Block F) and *Type 2* (Block E). Layouts and micrographs of (b) *Type 1* and (c) *Type 2*.

Appendix B

Publications on Wake-Up Receivers

B.1 A Delay-Based Wake-Up Receiver for Wireless Sensor Networks

A. Nowbahari, L. Marchetti and M. Azadmehr, 'A Delay-Based Wake-Up Receiver for Wireless Sensor Networks,' in *2021 International Conference on Electrical, Communication, and Computer Engineering (ICECCE)*, 2021, pp. 1–5. DOI: 10.1109/ICECCE52056.2021.9514246

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A Delay-Based Wake-Up Receiver for Wireless Sensor Networks

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***Abstract*—One of the main limitations in the design of wireless sensor networks is the optimization of the power management. A possible solution is the implementation of wake-up receivers (WuRxs), which activate the sensor nodes from deep sleep only when communication is required. The majority of WuRxs presents complex architectures based on amplifiers, comparators and demodulators. In this work we propose a new low power WuRx concept based on complementary circuitry. The proposed WuRx receives and measures the width of the input signal with different predefined signal pulse widths using delay lines. If the received signal resembles the correct wake-up call, i.e. it has the right duty cycles, it sequentially activates the WuRx and wakes up the sensor node. A possible circuit implementation in TSMC-180nm CMOS process is reported. The simulation results confirm the proposed delay comparison mechanism. The WuRx consumes 35µA when receiving a 12ms selective wake-up call signal, and 337nA when in the idle mode.**

***Index Terms*—CMOS, low power, sensor node, wake-up receiver, wireless sensor network.**

I. Introduction

A wireless sensor network (WSN) consists of groups of wireless sensor nodes, often powered by batteries, able to sense, process and transmit signals [1]. One of the main research topics in the design of the WSNs is the optimization of the power, since the lifetime and performance are mainly limited by the sensor nodes power consumption [2], [3]. A typical energy-saving solution is the duty-cycled Medium Access Control (MAC) protocol, which consists into periodically activate the sensors node [4]. A sleep phase follows the activation period. But this approach suffers from energy waste associated to the *idle listening* when active, even if no transmission is present [5]. Another problem associated to presynchronized activation protocols is the *overhearing*, which occurs when sensor nodes that are not intended to be activated, are triggered [6]. Unnecessary wake-ups could be avoided by implementing wake-up receiver (WuRx) designs [7], [8]. In this approach the sensor nodes are normally in deep sleep mode. When the WuRx detects the wake-up call (WuC) signal, which can be radio-based or acoustic, an interrupt signal is generated and the sensor node is activated (Fig.1) [9]. This approach is identity-based and therefore energy-efficient since sensor nodes wake up only when required [10], [11]. The majority of reported WuRxs presents complex architectures based on amplifiers, comparators, demodulators and correlator circuits [9]. In this work we present a low power and simple wake-up receiver concept, and a possible circuit implementation of the proposed architecture. In section II the WuRx working principle is explained. In section III a CMOS circuit implementation is reported, while the simulation results are presented in section IV.

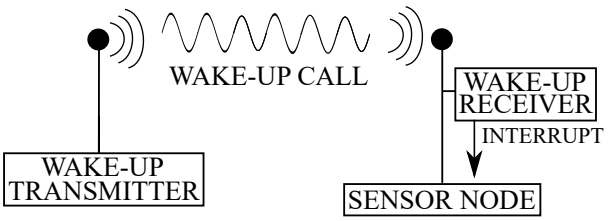

Fig. 1. Wake-up receiver concept: the sensor node wakes up only when the correct wake-up call is detected.

II. Architecture

The block diagram of the proposed wake-up receiver is shown in Fig.2. The amplitude of the high frequency input signal S_{in} may be small, depending on the distance from the source, the losses and the application. Therefore the amplitude of S_{in} may first be increased (S_{up}) using a step-up block such as a transformer. Next, the signal is rectified (S_{rect}) to create a continuous pulse with a width equal to the duration of S_{in}. Then S_{rect} is sent into the first state detector D_1, which is composed of a delay line τ_1 and a logic gate. After a predefined delay $\Delta\tau_1$, the signal S_{τ_1} is compared with the rectified signal S_{rect} through a logic gate. The comparison result is the enabling signal S_{en_1}, which drives the switch sw_1. If the input signal is not resembling the predefined wake-up call signal, the second delay line τ_2 does not activate. Instead, if it is correct, the second delay line activates and the signal S_{τ_2} results at the output of τ_2. The latter is again compared with the rectified signal through a logic gate, producing a second enable signal S_{en_2} which is used to drive the successive delay line, similar as in the first delay comparison. The number

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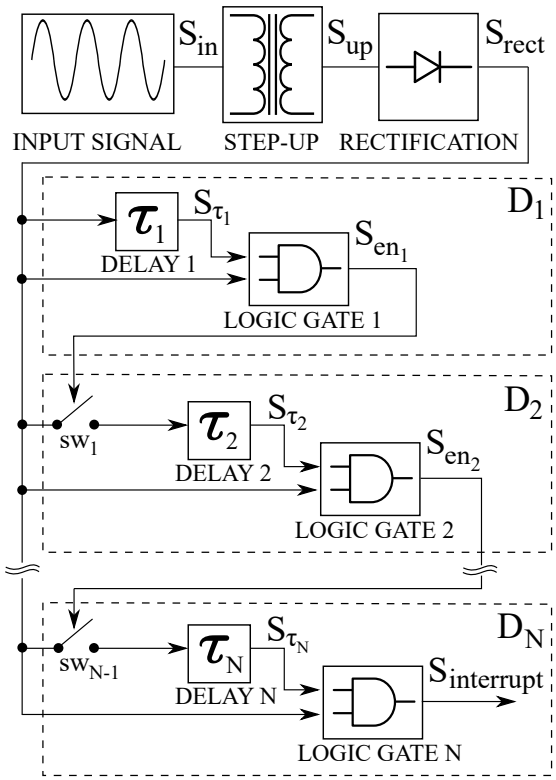

Fig. 2. Block diagram of the proposed delay-based wake-up receiver.

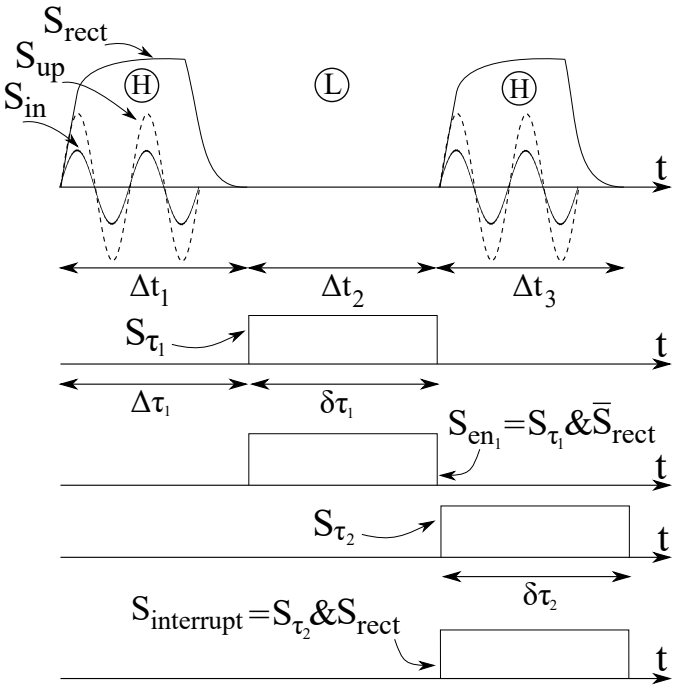

Fig. 3. Waveforms when the WuRx receives the WuC signal H-L-H.

of state detector blocks D_1 to D_N is proportional to the complexity of the wake-up call signal. Each state detector block can have different delay lines for detecting signals with a given pulse width. The wake-up signal $S_{interrupt}$ will activate the sensor node only if all the comparisons results are sequentially correct. The concept can be better understood with the example shown in Fig.3, where a WuRx with two state detector blocks D1 and D2 is considered. The wake-up call signal is assumed to be a sequence of two 'high' (H) states, separated by one 'low' (L) state. The WuC signal may be an ultrasound or a radio wave. The 'high' state is associated to the presence of the high frequency input signal for a well defined time interval, while the 'low' state is associated to its absence. The WuC signal is therefore considered to be H-L-H in this example. The input signal is applied for a time interval Δt_1, and the signal S_{τ_1} goes 'high' for a time δt_1, after a delay $\Delta\tau_1$. During Δt_2, we expect no signal at the input. Thus to correctly detect the WuC signal, the logic gate 1 should implement the logic function $S_{\tau_1}\&\overline{S}_{rect}$, where $\&$ is the logic AND operation, and $\overline{S}_{rect}$ is the inverted state of the rectified signal. If the comparison result is correct, as it is in this example, S_{en_1} goes 'high'. As a consequence, during Δt_3, S_{τ_2} goes 'high' for a time δt_2. Since we expect the third state to be a 'high' one for the correct detection, the interrupt signal $S_{interrupt}$ goes 'high' only if the logic gate 2 implements the logic function $S_{\tau_2}\&S_{rect}$. The interrupt signal does not become 'high' if all the enable signals do not sequentially become 'high' too. The proposed approach is conceptually simple, since only delay elements and logic comparisons between two signals are required.

III. Circuit Implementation

A possible circuit implementation of the proposed architecture is shown in Fig. 4. The input signal V_{in} is passively amplified and rectified through a Delon voltage doubler, which is composed of a step-up transformer ($L_{p,s}$), two diodes ($D_{1,2}$) and two capacitors ($C_{1,2}$). At the secondary side of the transformer the voltage is:

$$V_{up} = \frac{V_{in}}{N} \tag{1}$$

where N is the transformer turn ratio ($N_p/N_s = N$). Amplification occurs if $N < 1$ or equivalently $L_p < L_s$. When V_{in} is 'high', the rectified voltage can be approximately expressed as:

$$V_{rect} = 2\left(\frac{|V_{in}|}{N} - V_\gamma\right) \tag{2}$$

where V_γ is the diode voltage drop. As V_{in} goes 'low', the rectified voltage is discharged through the resistor R.

A. Delay Line

The delay line τ_1 is composed of two inverters (M_{inv_1}, M_{d_1}), two switches (M_{n,sw_1}, M_{p,sw_1}), an active load (M_{p,act_1}), an RC group (R_{τ_1}, C_{τ_1}) and a buffer ($M_{p_{1,2},\tau_1}$, $M_{n_{1,2},\tau_1}$, C_{1,τ_1}). The inverter M_{inv_1} inverts the rectified signal. Therefore (2) should be large enough to trigger M_{inv_1}. The inverter M_{d_1} drives the switches, which are used to

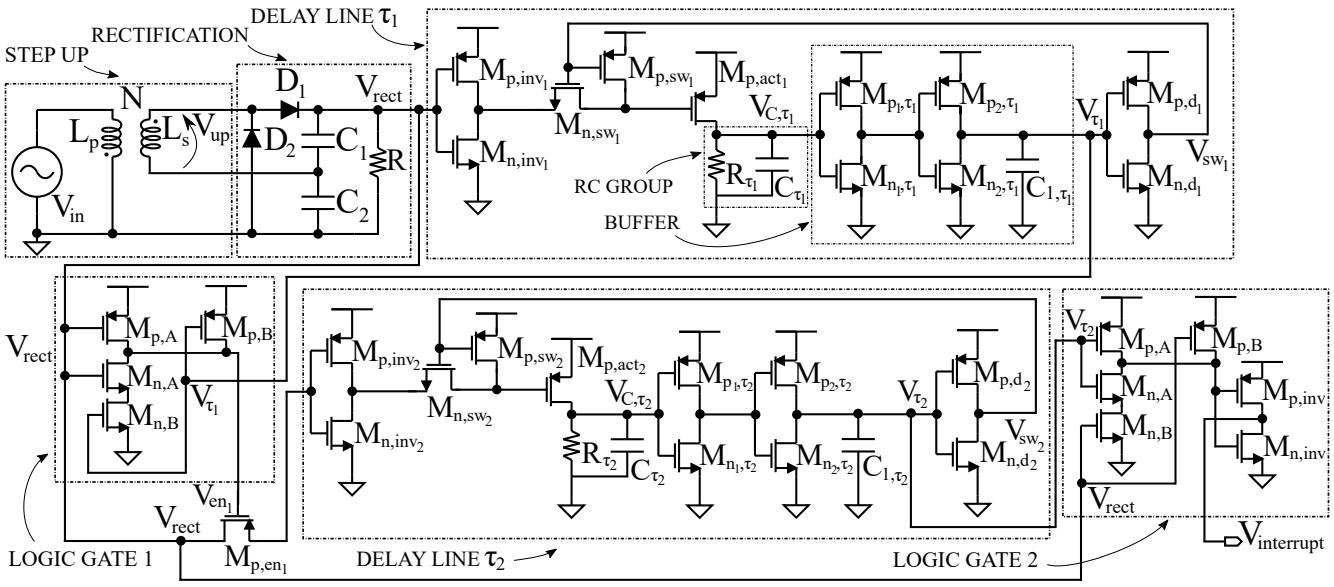

Fig. 4. Circuit implementation of the proposed WuRx, with two delay lines and logic gates.

decouple the delay line from the input. To explain the delay line operation, we can assume that the rectified voltage is 'high', the switch M_{n,sw_1} is initially close and so that V_{sw_1} is 'high'. Under these assumptions, the rectified voltage is 'low' after M_{inv_1}. Since M_{n,sw_1} is closed, the transistor M_{p,act_1} is on because its source-gate voltage is equal to the supply voltage V_{dd}. As a consequence a voltage V_{C,τ_1} results across the capacitor C_{τ_1}. The transient characteristics of V_{C,τ_1} (e.g. δt_1 in Fig.3) is established by the time constant of the RC group. The voltage V_{C,τ_1} is then delayed through the buffer, resulting in the voltage V_{τ_1}, which is the delay line output. The delay introduced by the buffer is $\Delta\tau_1$ in Fig.3. The higher the number of buffer stages, the larger the delay of V_{τ_1} with respect to V_{C,τ_1}. Once the delay process is performed, the voltage at the output of the inverter M_{d_1} goes 'low'. As a consequence M_{n,sw_1} is now open, and M_{p,sw_1} is closed. The latter connects the M_{p,act_1} gate to V_{dd} thus turning it off.

B. Logic Gate

The logic gates are used to enable the successive delay lines and produce the interrupt voltage $V_{interrupt}$. If the input signal resembles the predefined wake-up call, all the delay lines sequentially activate, and the interrupt voltage $V_{interrupt}$ becomes 'high'. To detect a 'high' state two possible approaches could be followed. The first one is shown in Fig.4, where the logic gate 1 is a NAND and the enabling transistor is a PMOS switch. This choice implies that the enabling transistor M_{p,en_1} connects the second delay line to the rectified voltage if and only if the rectified (V_{rect}) and delayed (V_{τ_1}) voltages are both 'high' at the same time. The second one consists into replace the NAND gate and the PMOS enabling transistor with an AND gate and an NMOS transistor respectively. The AND gate can be implemented by inverting the NAND one. Instead the implementation of the 'low' state detector is conceptually more complex. A possible approach consists into remove the inverter M_{inv_2}, and to NAND the rectified signal (which is assumed to be 'low') after the inverter M_{inv_1} with the delayed one (V_{τ_1}). Since the inverted and delayed signals are 'high' at the same time, at the NAND output the enabling signal V_{en_1} will result 'low', thus activating the enabling transistor M_{p,en_1}. The reason for which M_{inv_2} has to be removed is due to the fact that the active load M_{p,act_2} is a PMOS. So if the rectified and the enabling signals are 'low' and M_{inv_2} is present, then M_{p,act_2} is off. The logic gate 2 in Fig.4 is an AND gate. Thus the interrupt voltage becomes 'high' if and only if the rectified (V_{rect}) and delayed (V_{τ_2}) voltages are both 'high'.

IV. Simulation Results

To verify the proposed WuRx concept, simulations were performed in TSMC-180nm CMOS process with the parameters in Tab.I. A WuRx with three delay lines and three logic gates is considered. Each delay line has two cascaded buffers. Logic gate 1 is an AND gate that drives an NMOS enabling transistor ('high' state detector). Logic gate 2 is a 'low' state detector, and logic gate 3 is an AND gate. The input signal is a sequence of pulsed sine waves, with amplitude $200mV$ and frequency $40kHz$. For the correct wake-up call detection, it is assumed that each state has a duration T of $3ms$. A 'high' state has a pulse duration T_{on} equal to $1.5ms$, and so a $T_{off} = T - T_{on} = 1.5ms$. The wake-up call is set to be H-H-L-H (Fig.5(a)). The supply voltage V_{DD} is equal to $1.2V$. The channel length is $1\mu m$ for all the transistors, and the widths are sized in order to have a symmetric switching point around $V_{dd}/2$. The simulation results confirm the proposed WuRx concept. The delayed voltage V_{τ_1} goes 'high' around $3ms$ because of the first input pulse (Fig.5(b)). Since logic gate 1 is a 'high' state detector

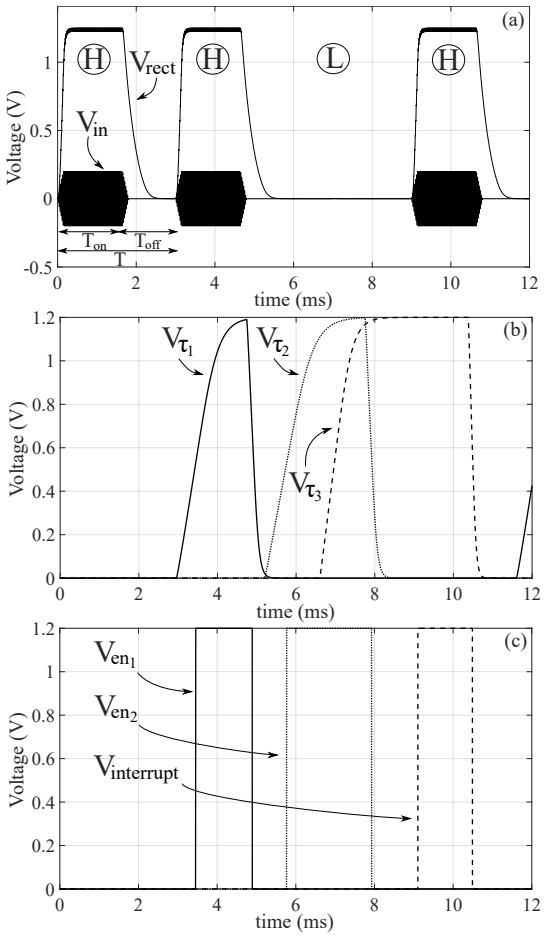

Fig. 5. Simulation results: (a) input (V_{in}) and rectified (V_{rect}) voltages. (b) Delay voltages ($V_{\tau_{1,2,3}}$). (c) Enable ($V_{en_{1,2}}$) and interrupt ($V_{interrupt}$) voltages.

and a second pulse is present after T, V_{en_1} goes 'high' as well (Fig.5(c)). As a consequence the second delay line is activated and V_{τ_2} goes 'high' around $5ms$. The third state is a 'low' one, and logic gate 2 is a 'low' state detector. Therefore V_{en_2} goes 'high' and activates V_{τ_3}. Finally the the interrupt voltage $V_{interrupt}$ is obtained because the third logic gate is a 'high' state detector, and both the input signal and V_{τ_3} are 'high' at the same time. If the input voltage does not resemble the wake-up call H-H-L-H, the interrupt voltage does not become 'high'. From a technological point of view, the resistances and capacitances used for the simulations are large as compared to the typical values implemented in ASICs. Therefore to implement an IC version of the proposed circuit, the resistors should be replaced by transistors, and the capacitances should be further reduced. From a power consumption point of view, the critical components are the PMOS active loads. The power consumption can be minimized by increasing the resistance and decreasing the capacitance of the RC groups, keeping unchanged their time constants. The average current for the detection of the $12ms$ WuC signal in Fig.5(a) is $35\mu A$, with an average power consumption of $42\mu W$. The average current

TABLE I
CIRCUIT SIMULATION PARAMETERS

Component	Parameter	Value
Supply Voltage	V_{DD}	$1.2V$
Transformer	L_p	$4\mu H$
	L_s	$400\mu H$
Rectifier	$C_{1,2}$	$100nF$
	R	$7k\Omega$
Delay Line τ_1	R_{τ_1}	$50k\Omega$
	C_{τ_1}	$80nF$
	C_{1,τ_1}	$50nF$
	C_{2,τ_1}	$15nF$
Delay Line τ_2	R_{τ_2}	$120k\Omega$
	C_{τ_2}	$30nF$
	C_{1,τ_2}	$20nF$
	C_{2,τ_2}	$15nF$
Delay Line τ_3	R_{τ_3}	$300k\Omega$
	C_{τ_3}	$15nF$
	C_{1,τ_3}	$15nF$
	C_{2,τ_3}	$10nF$

TABLE II
POWER CONSUMPTION COMPARISON WITH OTHER WURXS

$\mathbf{P_{idle}}$	$\mathbf{P_{active}}$	Work
$404nW$	$42\mu W$	This
$1.2\mu W$	$63\mu W$	[12]
$1.276\mu W$	$70.6\mu W$	[13]
$10.8\mu W$	$24\mu W$	[14]
$12.4\mu W$	$368.1\mu W$	[15]

in the idle state is $337nA$, with an average power consumption of $404nW$. A comparison with other WuRxs is reported in Tab.II. P_{idle} is the power consumption during listening mode, while P_{active} is the power consumption during active mode (i.e. when receiving and decoding the WuC) [9]. The power in the active mode is dependent on the wake-up call signal, the architecture and the implemented technology. Therefore a more meaningful comparison could be done by considering the power in the idle mode. As compared to other WuRxs, the proposed circuit results to be low power both in the idle and active modes.

V. CONCLUSIONS

In this work we propose a delay-based wake-up receiver concept for wireless sensor nodes. The interrupt wake-up signal is generated by sequential delay blocks. Each delay block measures the width of the input signal with a predefined time interval. A possible circuit implementation in TSMC-180nm CMOS process is proposed. The simulations confirmed the proposed concept. The circuit consumes about $400nW$ in the idle state, and $42\mu W$ for the detection of a $12ms$ selective wake-up call signal. The power consumption is dependent on the amount of delay lines and so on the complexity of the WuC signal. Future work will focus on the minimization of the power consumption by reduction of power supply and other techniques.

ACKNOWLEDGMENT

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REFERENCES

[1] S. Zhang and H. Zhang, "A review of wireless sensor networks and its applications," in *2012 IEEE International Conference on Automation and Logistics*, 2012, pp. 386–389.

[2] S. Kumar, A. Arora, and T. H. Lai, "On the lifetime analysis of always-on wireless sensor network applications," in *IEEE International Conference on Mobile Adhoc and Sensor Systems Conference, 2005.*, 2005, pp. 3 pp.–188.

[3] F. Engmann, F. A. Katsriku, J.-D. Abdulai, K. S. Adu-Manu, and F. K. Banaseka, "Prolonging the lifetime of wireless sensor networks: A review of current techniques," *Wireless Communications and Mobile Computing*, vol. 2018, 2018.

[4] F. Z. Djiroun and D. Djenouri, "MAC Protocols With Wake-Up Radio for Wireless Sensor Networks: A Review," *IEEE Communications Surveys Tutorials*, vol. 19, no. 1, pp. 587–618, 2017.

[5] I. Demirkol, C. Ersoy, and E. Onur, "Wake-up receivers for wireless sensor networks: benefits and challenges," *IEEE Wireless Communications*, vol. 16, no. 4, pp. 88–96, 2009.

[6] D. Ghose, F. Y. Li, and V. Pla, "MAC Protocols for Wake-Up Radio: Principles, Modeling and Performance analysis," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 5, pp. 2294–2306, 2018.

[7] J. Oller, I. Demirkol, J. Casademont, J. Paradells, G. U. Gamm, and L. Reindl, "Has Time Come to Switch From Duty-Cycled MAC Protocols to Wake-Up Radio for Wireless Sensor Networks?" *IEEE/ACM Transactions on Networking*, vol. 24, no. 2, pp. 674–687, 2016.

[8] H. Bello, Z. Xiaoping, R. Nordin, and J. Xin, "Advances and Opportunities in Passive Wake-Up Radios with Wireless Energy Harvesting for the Internet of Things Applications," *Sensors*, vol. 19, no. 14, p. 3078, 2019.

[9] R. Piyare, A. L. Murphy, C. Kiraly, P. Tosato, and D. Brunelli, "Ultra Low Power Wake-Up Radios: A Hardware and Networking Survey," *IEEE Communications Surveys Tutorials*, vol. 19, no. 4, pp. 2117–2157, 2017.

[10] O. Kanoun, S. Bradai, S. Khriji, G. Bouattour, D. El Houssaini, M. Ben Ammar, S. Naifar, A. Bouhamed, F. Derbel, and C. Viehweger, "Energy-Aware System Design for Autonomous Wireless Sensor Nodes: A Comprehensive Review," *Sensors*, vol. 21, no. 2, p. 548, 2021.

[11] D. Griffith, "Wake-Up Radio for Low-Power Internet of Things Applications: An Alternative Method to Coordinate Data Transfers," *IEEE Solid-State Circuits Magazine*, vol. 11, no. 4, pp. 16–22, 2019.

[12] M. Magno, V. Jelicic, B. Srbinovski, V. Bilas, E. Popovici, and L. Benini, "Design, Implementation, and Performance Evaluation of a Flexible Low-Latency Nanowatt Wake-Up Radio Receiver," *IEEE Transactions on Industrial Informatics*, vol. 12, no. 2, pp. 633–644, 2016.

[13] M. Del Prete, D. Masotti, A. Costanzo, M. Magno, and L. Benini, "A 2.4 GHz-868 MHz dual-band wake-up radio for wireless sensor network and IoT," in *2015 IEEE 11th International Conference on Wireless and Mobile Computing, Networking and Communications (WiMob)*, 2015, pp. 322–328.

[14] J. Oller, E. Garcia, E. Lopez, I. Demirkol, J. Casademont, J. Paradells, U. Gamm, and L. Reindl, "IEEE 802.11-enabled wake-up radio system: design and performance evaluation," *Electronics Letters*, vol. 50, no. 20, pp. 1484–1486, 2014.

[15] T. Takiguchi, S. Saruwatari, T. Morito, S. Ishida, M. Minami, and H. Morikawa, "A Novel Wireless Wake-Up Mechanism for Energy-Efficient Ubiquitous Networks," in *2009 IEEE International Conference on Communications Workshops*, 2009, pp. 1–5.

B.2 An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks

A. Nowbahari, L. Marchetti and M. Azadmehr, 'An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks,' in *2021 IEEE 7th World Forum on Internet of Things (WF-IoT)*, 2021, pp. 380–384. DOI: 10.1109/WF-IoT51360.2021.9595159

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An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks

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***Abstract*—In recent years wireless sensor networks (WSNs) have gained significant attention because of their implementation in many different fields. As the nodes in WSNs are typically battery-powered, their lifetime is mainly limited by the sensor nodes power consumption. A typical energy-saving solution consists in implementing wake-up receivers (WuRxs), which are responsible for the sensor node activation only when required. In this work an ultra-low power multivibrator-based WuRx concept is proposed. The WuRx is composed of several input-triggered multivibrators, which generate pulses of fixed duration. These pulses are compared to the input signal through logic gates, which are predefined according to the wake-up call. The sensor node is activated if the codes match. An implementation in TSMC-180nm CMOS process is proposed and simulated. The WuRx consumes 0.8µW when detecting a 6ms wake-up call signal, and 58.4pW when in idle mode.**

***Index Terms*—CMOS, low power, multivibrator, sensor node, wake-up receiver, wireless sensor network**

I. Introduction

A wireless sensor network (WSN) can be defined as the ensemble of wirelessly connected sensor nodes capable of sensing, processing and transmitting signals [1]. WSNs are implemented in many applications (health, environmental, military), and are one of the main enabling technologies of the Internet-of-Things [2], [3]. They are typically powered by batteries, so their primary limitation is the sensor nodes power consumption, which limits the network lifetime [4]. Different energy-saving solutions have been investigated to optimize the WSN power management [5]. A possible method consists into set in sleep mode the sensor nodes, and wake up them according to a certain *rendezvous* scheme [6]. For instance in pure synchronous rendezvous schemes, sensor nodes are presynchronized to activate according to a well defined sleep schedule. But this approach is intrinsically affected by *idle listening* and *overhearing*. Idle listening occurs when the sensor node is active, but no communication is required, thus resulting in wasted energy [7]. Overhearing occurs when a sensor node overhears data that are not intended to it, thus being uselessly activated [8]. A practical solution to these problems is the implementation of pure asynchronous rendezvous schemes, where the sensor nodes are woken up according to an identity-based approach [9]. From a hardware point of view this translates in the implementation of wake-up receivers (WuRxs) [10]. In such a scheme (Fig.1) the sensor nodes are normally in deep sleep mode. When the correct wake-up call (WuC) is detected, the WuRx activates the sensor node through an interrupt signal. This approach is conceptually energy-saving, since the sensor nodes are activated only on demand. Wake-up receivers could be mainly classified in RF based and non-RF based WuRxs. The majority of WuRxs uses radio signals [11]–[15], while non-RF based solutions employ acoustic [16]–[22] and optical signals [23]–[26]. Most of the proposed WuRxs in the literature presents complex and power consuming architectures. In this work a simple and low power WuRx concept is proposed. In Section II the WuRx architecture is reported. In Section III a circuit implementation is presented, while the simulations results are in Section IV.

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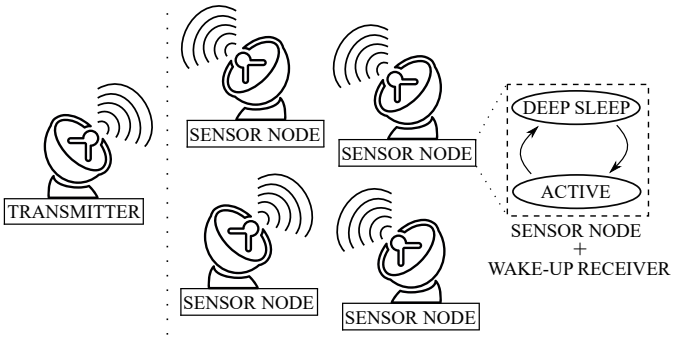

Fig. 1. Wireless sensor network implementing wake-up receivers.

II. Architecture

The architecture of the proposed WuRx is shown in Fig.2. Since the amplitude of the received input signal S_{in} could be small (e.g. because of losses and/or distance from the transmitter), a step-up block may be considered. The second block (rectification) is used to convert the AC input signal into square-shaped waves with duration equal to that of S_{in}. This rectified signal (S_{rect}) goes into the first state detector D_1, which is composed of a monostable (also called *one-shot* [27]) multivibrator and a logic gate. The multivibrator generates the pulse S_{p_1} in response to the input pulse (i.e.

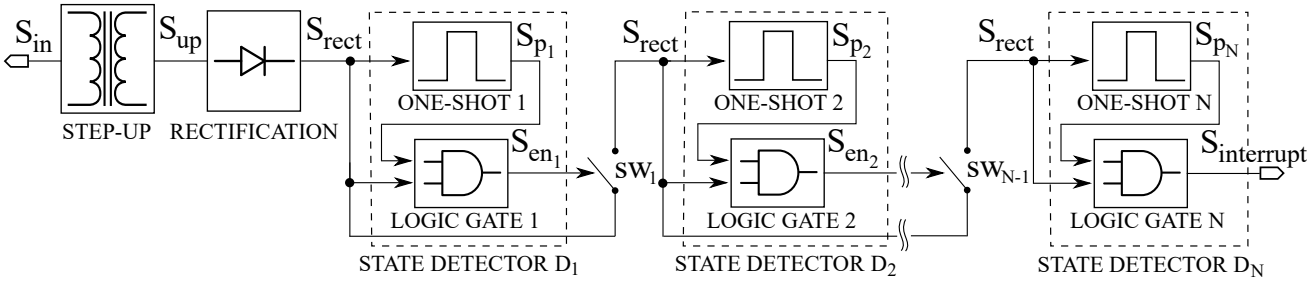

Fig. 2. Multivibrator-based WuRx block diagram.

S_{rect}). S_{p_1} has a longer duration than that of S_{rect}. Next these two signals go into logic gate 1, and are compared. If S_{rect} resembles the predefined WuC, logic gate 1 will enable the second state detector D_2 through the switch sw_1. D_2 in turn will generate a new pulse S_{p_2}, and compare it to S_{rect}. Again the comparison result is used as enabling signal of the successive state detector. Therefore the identification process consists into generating a pulse signal, and comparing it to the input one. The sensor node will be activated by the wake-up interrupt signal $S_{interrupt}$ only if all the state detectors are sequentially enabled, thus guaranteeing an identity-based wake-up. The WuRx has N logic gates and multivibrators, and $N-1$ switches, since the first state detector is by default enabled. Logic gates from 1 to $N-1$ are used to drive the enabling switches, while the Nth logic gate asserts the interrupt signal. The more complex the WuC signal, the larger the number of state detectors. An example of WuRx waveforms is depicted in Fig.3, where two state detectors are implemented, and the WuC signal is H-L-H. By H is meant a 'high' state, i.e. S_{in} (and consequently S_{rect}) is present at the WuRx input for a certain time window. By L is meant a 'low' state, i.e. the input signal is not present at the WuRx input ($V_{in} = 0V$). During the time window Δt_1 the input signal S_{in} is rectified. In response to S_{rect}, the multivibrator generates the pulse S_{p_1} with duration $\delta\tau_1$. In order to correctly detect the 'low' state and generate the first enabling signal, logic gate 1 has to implement the logic function $S_{p_1}\&\overline{S}_{rect}$. The $\&$ symbol represents the logical conjunction operation, while the bar over $\overline{S}_{rect}$ represents the signal opposite state. Therefore since S_{rect} is 'low' and S_{p_1} is 'high' during Δt_2, the enabling signal S_{en_1} goes 'high'. Consequently the second state detector D_2 is now enabled. Next $\overline{S}_{rect}$ is used to trigger the second multivibrator, thus generating a new pulse S_{p_2} with duration $\delta\tau_2$. As before, the generated pulse is compared to the rectified signal, which is 'high' during the time window Δt_3. If logic gate 2 implements the logic operation $S_{p_2}\&S_{rect}$, then the interrupt signal $S_{interrupt}$ goes 'high', and the sensor node wakes up. The sensor node activation is therefore associated to a sequential verification of the WuC signal.

III. Circuit Implementation

The proposed WuRx has been implemented with the circuit in Fig.4. The circuit configuration depends on the WuC signal.

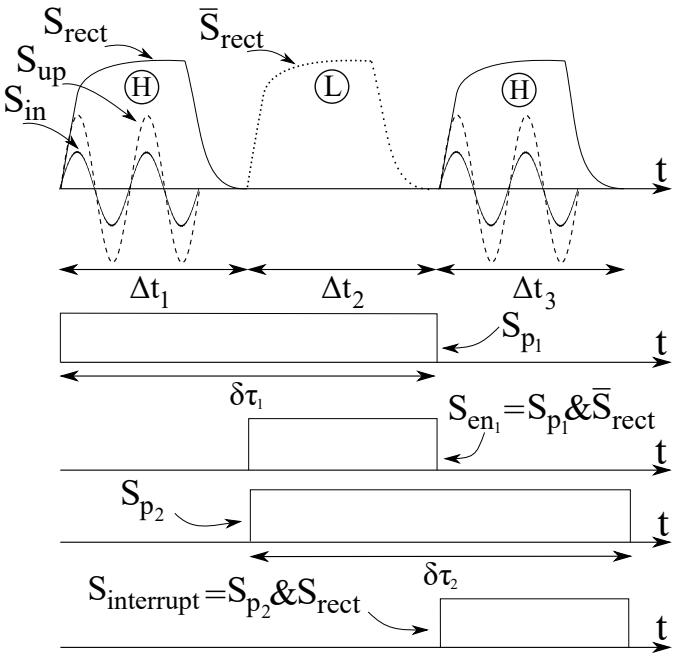

Fig. 3. WuRx waveforms when the WuC is H-L-H.

In this case two state detectors are considered: the first one (D_1) is a 'low' state detector, while D_2 is a 'high' one. This implies that the circuit in Fig.4 can detect the WuC signal H-L-H (Fig.3). The step-up and rectification blocks are realized through a Delon circuit [28]. The resistor R is used to discharge the rectified voltage.

A. Monostable Multivibrator

The monostable multivibrator is implemented through a 2-input NOR gate ($M_{p,A,B}$, $M_{n,A,B}$), a resistor (R_p), a capacitor (C_p) and an inverter ($M_{p,inv}$, $M_{n,inv}$) [27]. Considering multivibrator 1, suppose that initially the voltage at the input of $M_{p_1,A}$ and $M_{n_1,A}$ is 'low', and the NOR gate output is 'high'. Under these assumptions, V_{m_1} is 'high' because of R_{p_1}, and consequently the inverter output is 'low'. When a pulse is applied to the input (e.g. V_{rect}), V_{m_1} and the NOR gate output voltage go to zero volts, and so the inverter output goes 'high'. Since the inverter output is fed back to the NOR

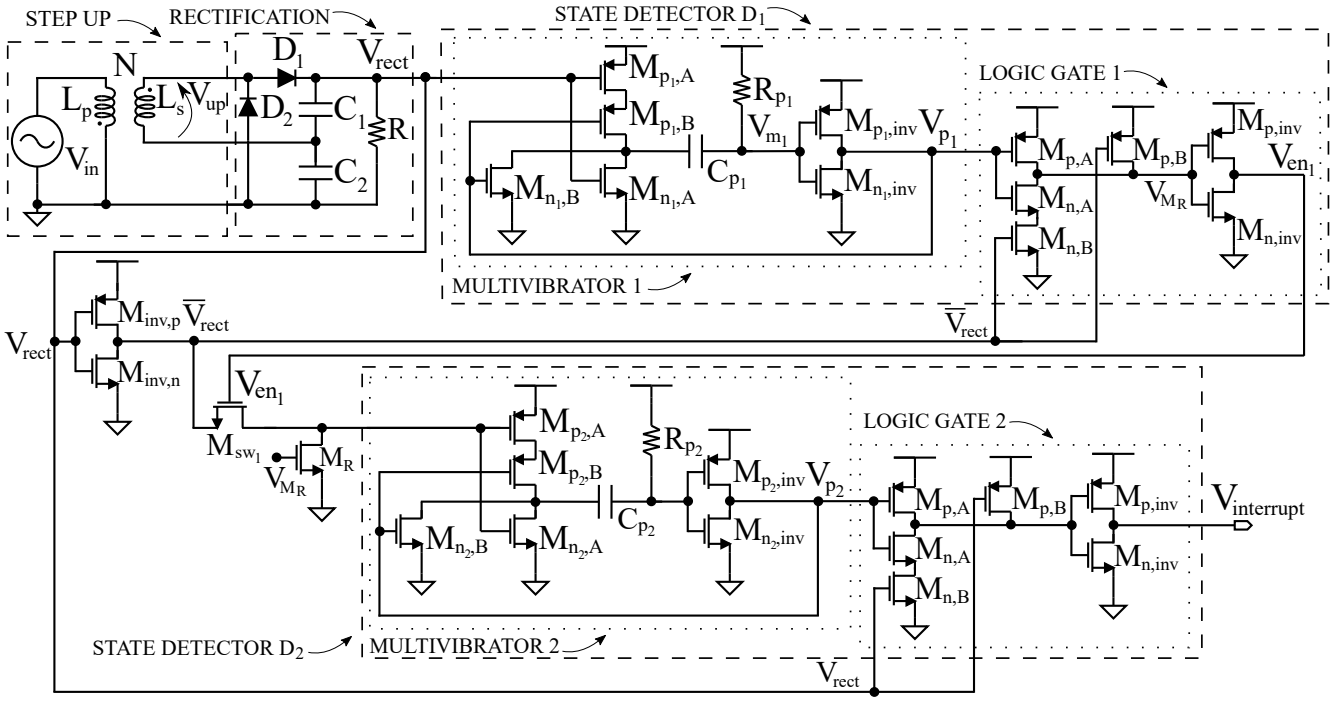

Fig. 4. Circuit implementation of the proposed WuRx, with two multivibrators and logic gates.

gate input ($M_{p_1,B}$ and $M_{n_1,B}$), the NOR gate output voltage is held at zero volts. At this point C_{p_1} starts to get charged through R_{p_1}, so V_{m_1} increases. The voltage across C_{p_1} can be expressed as:

$$V_{C_{p_1}} = V_{DD}\left(1 - \exp\left(-\frac{t}{R_{p_1}C_{p_1}}\right)\right) \quad (1)$$

where V_{DD} is the supply voltage. Assuming that the inverter threshold voltage $V_{th,inv}$ is $V_{DD}/2$, it follows that C_{p_1} will be charged up to $V_{th,inv}$ in a time given by:

$$t = R_{p_1}C_{p_1}ln\left(\frac{V_{DD}}{V_{DD} - V_{th,inv}}\right) = R_{p_1}C_{p_1}ln(2) \quad (2)$$

from which follows that the multivibrator output pulse V_{p_1} has a duration of approximately $0.7R_{p_1}C_{p_1}$ ($\delta\tau_1$ in Fig.3). As soon as the inverter gets triggered, the voltage V_{m_1} goes to $V_{dd} + V_{dd}/2$. The time required to re-trigger the multivibrator is therefore dependent on the time needed to V_{m_1} to decrease back to V_{dd}. From a process variations point of view, the multivibrator resistor and capacitor are the most critical components, since they determine the signals comparison time window.

B. Logic Gate

The logic gates compare the multivibrators outputs with the rectified voltage. Logic gate 1 in Fig.4 is an AND gate realized by inverting a NAND gate. Its output (V_{en_1}) is 'high' when both the inputs are 'high' at the same time. So logic gate 1 drives an NMOS switch (M_{sw_1}). Alternatively is possible to use a NAND gate and a PMOS switch. In order to detect a 'low' state, V_{rect}, which is assumed to be 'low', is inverted by ($M_{inv,p}$, $M_{inv,n}$). Therefore since V_{p_1} and $\overline{V}_{rect}$ are both 'high', $V_{en,1}$ is 'high' as well and enables the switch M_{sw_1}. In order to trigger the multivibrator of the second state detector, a 'high' voltage is required at its input. A possible solution is to use the inverted rectified voltage. Transistor M_R is used to discharge the inverted rectified voltage when M_{sw_1} turns off. So multivibrator 2 is triggered, and a pulse V_{p_2} results at its output. Since D_2 is a 'high' state detector, logic gate 2 receives V_{rect} at the other input, thus generating the interrupt voltage.

IV. Simulation Results

Simulations in TSMC-180nm CMOS process were performed to verify the proposed architecture. The simulated WuRx is composed of three state detectors. D_1 and D_2 are 'low' state detectors, while D_3 is a 'high' state detector. Therefore the WuRx wakes up the sensor node if the WuC H-L-L-H is received. Each state has a period $T = 1.5ms$, so a four-states WuC has a duration of $6ms$. The applied input voltage V_{in} consists of pulsed sine waves, with frequency $40kHz$ and amplitude $200mV$ (Fig.5(a)). Therefore an acoustic WuRx is considered [16], [18]–[20]. The circuit simulation parameters are reported in Table I. The circuit can be tuned to operate at different frequencies, by modifying the step-up and the rectification stages. The multivibrators resistors are implemented with a cascade of two diode-connected PMOS, with unit width and length. The NOR and NAND gates are sized with minimum channel width and length, while the inverters

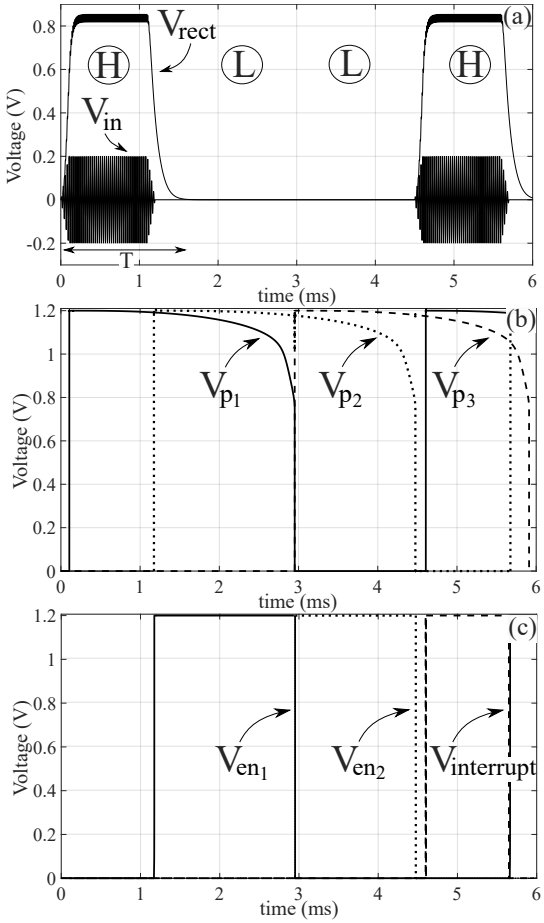

Fig. 5. WuRx simulation results: (a) V_{in} and V_{rect}. (b) V_{p_1}, V_{p_2} and V_{p_3}. (c) V_{en_1}, V_{en_2} and $V_{interrupt}$.

have a symmetric switching point around $V_{DD}/2$, where V_{DD} is equal to $1.2V$. The simulation results validated the concept. V_{rect} is initially 'high' for a time window $T = 1.5ms$. So D_1 is triggered, and its multivibrator generates the pulse V_{p_1}, which stays 'high' for $3ms$ (Fig.5(b)). During the second time window ($t = 1.5ms$ to $t = 3ms$), V_{rect} is 'low'. Since D_1 is a 'low' state detector, the enabling signal V_{en_1} goes 'high' as shown in Fig.5(c). Consequently D_2, which is a 'low' state detector as D_1, is now active. As explained in Sect.III, to detect a 'low' state the inverted rectified voltage is used to trigger the second multivibrator. The latter generates the pulse V_{p_2}, which stays 'high' approximately for $3ms$. As before, the enabling signal V_{en_2} goes 'high', thus activating D_3, which is a 'high' state detector. Again the inverted rectified voltage is used to trigger the successive multivibrator, which generates the pulse V_{p_3} ($t = 3ms$ to $t = 6ms$). Since V_{rect} is 'high' as well in the time window ($t = 4.5ms$ to $t = 6ms$), logic gate 3 finally generates $V_{interrupt}$.

A. Power Consumption

During the detection of the WuC (H-L-L-H) the WuRx consumes $0.66\mu A$, at which corresponds an average power consumption of $0.8\mu W$. Instead in the idle mode the WuRx consumes $48.6pA$, at which corresponds an average power consumption of $58.4pW$. The power consumption in the active mode is WuC dependent, i.e. a longer WuC would imply more state detectors and therefore a higher power consumption; when detecting the WuC H-L-L-H-L-H, the WuRx consumes $1.1\mu W$. A comparison with other acoustic WuRxs is reported in Table II. The circuit is ultra-low power both in active and idle mode.

TABLE I
CIRCUIT SIMULATION PARAMETERS

Component	Parameter	Value
Supply Voltage	V_{DD}	$1.2V$
Transformer	L_p	$4\mu H$
	L_s	$400\mu H$
Rectifier	$C_{1,2}$	$200nF$
	R	$1k\Omega$
Multivibrators	C_{p_1}	$25pF$
	C_{p_2}	$29pF$
	C_{p_3}	$26pF$

TABLE II
POWER CONSUMPTION COMPARISON WITH OTHER WURXS

$\mathbf{P_{idle}}$	$\mathbf{P_{active}}$	$\mathbf{f_{input}}$	$\mathbf{V_{dd}}$	**Work**
$58.4pW$	$0.8\mu W$	$40kHz$	$1.2V$	This
$3\mu W$	$8.1\mu W$	$85kHz$	$3.3V$	[19]
$1.64\mu W$	$14\mu W$	$40kHz$	$2V$	[18]
–	$4\mu W$	$43kHz$	$0.6V$	[16]
$45\mu W$	$420\mu W$	$20kHz$	$3V$	[20]

V. CONCLUSIONS

In this work an ultra-low power multivibrator-based WuRx concept for wireless sensor networks is proposed. The WuRx compares the duration of the input signal to predefined pulses of fixed duration, generated by multivibrators. The system exploits the operation of complementary circuit design, such as simple logic gates, to achieve low power system operation. The input wake-up call is sequentially decoded and verified by the proposed WuRx, to generate the interrupt signal. An implementation in TSMC-180nm CMOS process is proposed and simulated, confirming the concept. The proposed implementation of the WuRx consumes $0.8\mu W$ and $58.4pW$ in the active and idle modes respectively.

REFERENCES

[1] A. Flammini and E. Sisinni, "Wireless Sensor Networking in the Internet of Things and Cloud Computing Era," *Procedia Engineering*, vol. 87, pp. 672–679, 2014.

[2] D. Kandris, C. Nakas, D. Vomvas, and G. Koulouras, "Applications of Wireless Sensor Networks: An Up-to-Date Survey," *Applied System Innovation*, vol. 3, no. 1, p. 14, 2020.

[3] A. Al-Fuqaha, M. Guizani, M. Mohammadi, M. Aledhari, and M. Ayyash, "Internet of Things: A Survey on Enabling Technologies, Protocols, and Applications," *IEEE Communications Surveys Tutorials*, vol. 17, no. 4, pp. 2347–2376, 2015.

[4] G. Anastasi, M. Conti, M. Di Francesco, and A. Passarella, "Energy conservation in wireless sensor networks: A survey," *Ad hoc networks*, vol. 7, no. 3, pp. 537–568, 2009.

[5] I. Demirkol, C. Ersoy, and E. Onur, "Wake-up receivers for wireless sensor networks: benefits and challenges," *IEEE Wireless Communications*, vol. 16, no. 4, pp. 88–96, 2009.

[6] E.-Y. A. Lin, J. M. Rabaey, and A. Wolisz, "Power-efficient rendezvous schemes for dense wireless sensor networks," in *2004 IEEE International Conference on Communications (IEEE Cat. No.04CH37577)*, vol. 7, 2004, pp. 3769–3776 Vol.7.

[7] A. Rasul and T. Erlebach, "Reducing Idle Listening during Data Collection in Wireless Sensor Networks," in *2014 10th International Conference on Mobile Ad-hoc and Sensor Networks*, 2014, pp. 16–23.

[8] D. Ghose, F. Y. Li, and V. Pla, "MAC Protocols for Wake-Up Radio: Principles, Modeling and Performance analysis," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 5, pp. 2294–2306, 2018.

[9] J. Oller, I. Demirkol, J. Casademont, J. Paradells, G. U. Gamm, and L. Reindl, "Has Time Come to Switch From Duty-Cycled MAC Protocols to Wake-Up Radio for Wireless Sensor Networks?" *IEEE/ACM Transactions on Networking*, vol. 24, no. 2, pp. 674–687, 2016.

[10] R. Piyare, A. L. Murphy, C. Kiraly, P. Tosato, and D. Brunelli, "Ultra Low Power Wake-Up Radios: A Hardware and Networking Survey," *IEEE Communications Surveys Tutorials*, vol. 19, no. 4, pp. 2117–2157, 2017.

[11] D. Galante-Sempere, D. Ramos-Valido, S. Lalchand Khemchandani, and J. Del Pino, "Low-Power RFED Wake-Up Receiver Design for Low-Cost Wireless Sensor Network Applications," *Sensors*, vol. 20, no. 22, p. 6406, 2020.

[12] D. D. Wentzloff, A. Alghaihab, and J. Im, "Ultra-Low Power Receivers for IoT Applications: A Review," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2020, pp. 1–8.

[13] J. Moody, P. Bassirian, A. Roy, N. Liu, N. S. Barker, B. H. Calhoun, and S. M. Bowers, "Interference Robust Detector-First Near-Zero Power Wake-Up Receiver," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2149–2162, 2019.

[14] S. Koeble, S. Heller, and P. Woias, "A narrow-band and ultra-low-power 433 MHz wake-up receiver," in *Journal of Physics: Conference Series*, vol. 1407, no. 1. IOP Publishing, 2019, p. 012093.

[15] T. Ma, "A Bit Sampled Wake-Up Receiver with Logarithmic Detector Architecture," in *2017 International Conference on Cyber-Enabled Distributed Computing and Knowledge Discovery (CyberC)*. IEEE, 2017, pp. 445–449.

[16] K. Yadav, I. Kymissis, and P. R. Kinget, "A 4.4uW wake-up receiver using ultrasound data communications," in *2011 Symposium on VLSI Circuits - Digest of Technical Papers*, 2011, pp. 212–213.

[17] Y. C. Wong, S. H. Tan, R. S. S. Singh, H. Zhang, A. Syafeeza, and N. Hamid, "Low power wake-up receiver based on ultrasound communication for wireless sensor network," *Bulletin of Electrical Engineering and Informatics*, vol. 9, no. 1, pp. 21–29, 2020.

[18] E. Lattanzi, M. Dromedari, V. Freschi, and A. Bogliolo, "A sub-μA ultrasonic wake-up trigger with addressing capability for wireless sensor nodes," *International Scholarly Research Notices*, vol. 2013, 2013.

[19] A. Sánchez, S. Blanc, P. Yuste, A. Perles, and J. J. Serrano, "An Ultra-Low Power and Flexible Acoustic Modem Design to Develop Energy-Efficient Underwater Sensor Networks," *Sensors*, vol. 12, no. 6, pp. 6837–6856, 2012.

[20] A. Bannoura, F. Höflinger, O. Gorgies, G. U. Gamm, J. Albesa, and L. M. Reindl, "Acoustic Wake-Up Receivers for Home Automation Control Applications," *Electronics*, vol. 5, no. 1, p. 4, 2016.

[21] H. Fuketa, S. O'uchi, and T. Matsukawa, "A 0.3-V 1-μW Super-Regenerative Ultrasound Wake-Up Receiver With Power Scalability," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 9, pp. 1027–1031, 2016.

[22] F. Höflinger, G. U. Gamm, J. Albesa, and L. M. Reindl, "Smartphone remote control for home automation applications based on acoustic wake-up receivers," in *2014 IEEE International Instrumentation and Measurement Technology Conference (I2MTC) Proceedings*. IEEE, 2014, pp. 1580–1583.

[23] J. Chen, Z. Dai, and Z. Chen, "Development of Radio-Frequency Sensor Wake-Up with Unmanned Aerial Vehicles as an Aerial Gateway," *Sensors*, vol. 19, no. 5, p. 1047, 2019.

[24] U. Dudko and L. Overmeyer, "Optical Wake-Up From Power-Off State for Autonomous Sensor Nodes," *IEEE Sensors Journal*, vol. 21, no. 3, pp. 3225–3232, 2021.

[25] G. Kim, Y. Lee, S. Bang, I. Lee, Y. Kim, D. Sylvester, and D. Blaauw, "A 695 pW standby power optical wake-up receiver for wireless sensor nodes," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*. IEEE, 2012, pp. 1–4.

[26] W. Lim, T. Jang, I. Lee, H.-S. Kim, D. Sylvester, and D. Blaauw, "A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*. IEEE, 2016, pp. 1–2.

[27] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*. John Wiley & Sons, 2019, ch. 18, pp. 539–540.

[28] A. Mouapi, N. Hakem, and N. Kandil, "Performances Comparison of Shottky Voltage Doubler Rectifier to support RF Energy Harvesting," in *2020 IEEE International Conference on Environment and Electrical Engineering and 2020 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, 2020, pp. 1–5.

B.3 Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks

A. Nowbahari, L. Marchetti and M. Azadmehr, 'Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks,' in *2022 11th International Conference on Communications, Circuits and Systems (ICCCAS)*, 2022, pp. 187–191. DOI: 10.1109/ICCCAS55266.2022.9825344

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Nano-Power Monostable-Based Wake-Up Mechanism for Wireless Sensor Networks

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***Abstract*— Wireless sensor networks (WSNs) generally consist of thousands of sensor nodes, each one supplied by a battery or harvested energy. To prolong the lifetime of wireless sensor networks, wake-up receivers (WuRxs) are typically employed. WuRxs can selectively activate sensor nodes by decoding a signal called wake-up call (WuC). Therefore, they optimize the power management of WSNs, by allowing communication when requested. In this article, an ultra-low power implementation of a sequential WuRx concept is proposed. The WuRx is composed of AND gates, switches, and monostable circuits. The monostable circuit is implemented through a transistor that generates a pulse according to a simple RC network and a switch. The proposed WuRx decodes the WuC signal by comparing the duty cycle of the received signal with the output signals of the monostable circuits. The ultra-low power implementation is validated at simulation level. The WuRx consumes 32.8nW when decoding a 3-bit wake-up call signal and 153nW when decoding 11 bits.**

Keywords— CMOS, low power, monostable, sensor node, wake-up receiver, wireless sensor network

I. Introduction

The Internet-of-Things paradigm is mainly enabled by wireless sensor networks (WSNs), which consist of groups of sensors with processing and communication capabilities, called sensor nodes (Fig.1(a)) [1], [2]. The network size ranges from a few units up to thousands, depending on the application. WSNs are highly versatile in terms of applications since they are employed in agriculture, smart buildings, animal and vehicle tracking, security, surveillance, health care, and many other application areas [3]. From an architecture point of view, a sensor node is generally composed of four units, i.e., wireless communication, sensing, processing, and power management units, as shown in Fig.1(b) [4]. The wireless communication unit is in charge of transmitting and receiving data and/or power. The sensing unit acquires data from the environment. The acquired data are then elaborated by the processing unit, which usually is a microcontroller. All these blocks are typically supplied by a power management unit, which can be a simple battery or a more complex circuit based on energy harvesting [5]. Generally, the most power-consuming unit is the processing one, which therefore represents the bottleneck of the sensor node architecture. Therefore the power management unit is critically important since it determines the network lifetime by managing the supplied power [6]. Researchers proposed different solutions for improving the network lifetime, such as topology control, power management optimization, data reduction, energy-efficient acquisition, mobile-sink, mobile-relay, routing, data gathering, and network coding [7]–[11]. At hardware level, a typical power-efficient approach consists into implementing wake-up receivers (WuRxs). WuRxs can selectively activate a sensor node when a well-defined signal, the wake-up call (WuC) signal, is decoded [12]–[14]. Therefore, they allow activation of sensor nodes on demand. From an architecture point of view, they enable the link between the processing and power management units, i.e., when the correct WuC signal is detected, they wake up the processing unit, which sends the elaborated data to the communication unit, as shown in Fig.1(c). In the latter figure, the WuRx is supplied by the power management unit. But depending on the architecture, WuRxs can also be powered by the WuC signal too. The WuC can be based on radio, optical and acoustic signals depending on the transmission medium. In our previous work, we proposed an ultra-low power WuRx based on a NOR-based monostable multivibrator topology for acoustic applications [15]. In this article, we report

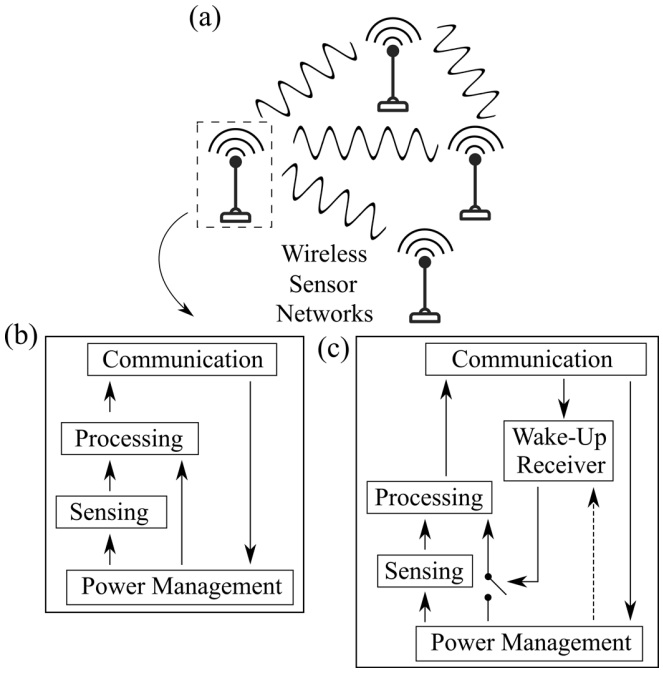

Fig. 1. (a) Wireless sensor network. (b) Typical sensor node architecture. (c) Integration of wake-up receivers (WuRxs). The arrow between the WuRx and the power management unit is dashed because in some architectures WuRxs are powered by the communication unit.

This work was supported by the Research Council of Norway [273248].

a simpler and less power-consuming monostable circuit, composed of only two transistors, two resistors, and a capacitor. Instead, the monostable in [15] is composed of six transistors, one capacitor, and one resistor. The proposed circuit is verified by simulations, by considering an acoustic WuC signal with a carrier frequency of 40kHz. The WuRx consumes 32.8nW when detecting the WuC signal 101, where each logic level has a duration of 1.5ms. To detect this code, the WuRx requires 22 transistors. We also evaluated the average power consumption for more complex WuC signals. The average power consumption and the number of implemented transistors linearly increase with the number of bits in the WuC signal. When considering 11 bits, the WuRx consumes 153nW and it requires 94 transistors. The proposed circuit is described in Section II. The simulation results are reported in Section III, and in the same section the proposed WuRx is compared with other WuRxs in the literature. The conclusions are in Section IV.

II. Circuit Description

The proposed WuRx decodes the WuC signal by measuring its duty cycle. The WuC signal consists of a series of bursts. We associate the high logic value 1 to the presence of the burst, and the low logic value 0 to the absence of the burst. To explain the WuRx operation, it is assumed that the WuC signal is 101, which is the simplest code that can be decoded. The block diagram associated to this example is shown in Fig.2(a). In real application scenarios, the sensor nodes are placed far away from each other. This implies that the communication unit can be unable to manage the amplitude of the received bursts. Thus a Step-Up block is considered. After passively amplifying the received burst (S_{RX}), the signal goes into the block Rectification. The latter generates the signal S_R which has a duration equal to that of the received burst. The first received burst triggers Monostable 1, which in response generates the pulse S_{m_1}. The monostable is designed so that its output duration is equal at least to the burst period. To decode the second value in the WuC signal (i.e. the 0 in 101), the AND operation is performed between the inverted rectified signal and the first monostable output. This closes Switch 1, which connects the rectified signal with the second monostable. To detect the last value of the WuC signal (i.e. the last 1 in 101), the AND operation between the rectified signal and the output of Monostable 2 is performed. The final output is the interrupt signal, which wakes up the sensor node by connecting the processing unit to the power management one. The proposed architecture is modular, i.e. a longer WuC signal can be decoded by cascading other monostables, AND gates and switches. For an N-value WuRx, $N-2$ switches and $N-1$ monostables and AND gates are necessary. The process through which the WuC signal is decoded is sequential, so if a wrong bit is detected the successive stages are not activated. The circuit associated with this example is shown in Fig.2(b). The passive amplification and rectification are performed through a loaded voltage doubler. A CMOS inverter-based buffer is used to smooth the received voltage, and to generate the inverted rectified voltage. The AND gate is an inverted NAND. The switch circuit also avoids floating gate at the input of the monostables. As reported in the introduction, this WuRx concept has been proposed in our previous work [15]. The novelty of this work is the simplification of the monostable circuit. Instead of using a NOR-based monostable multivibrator

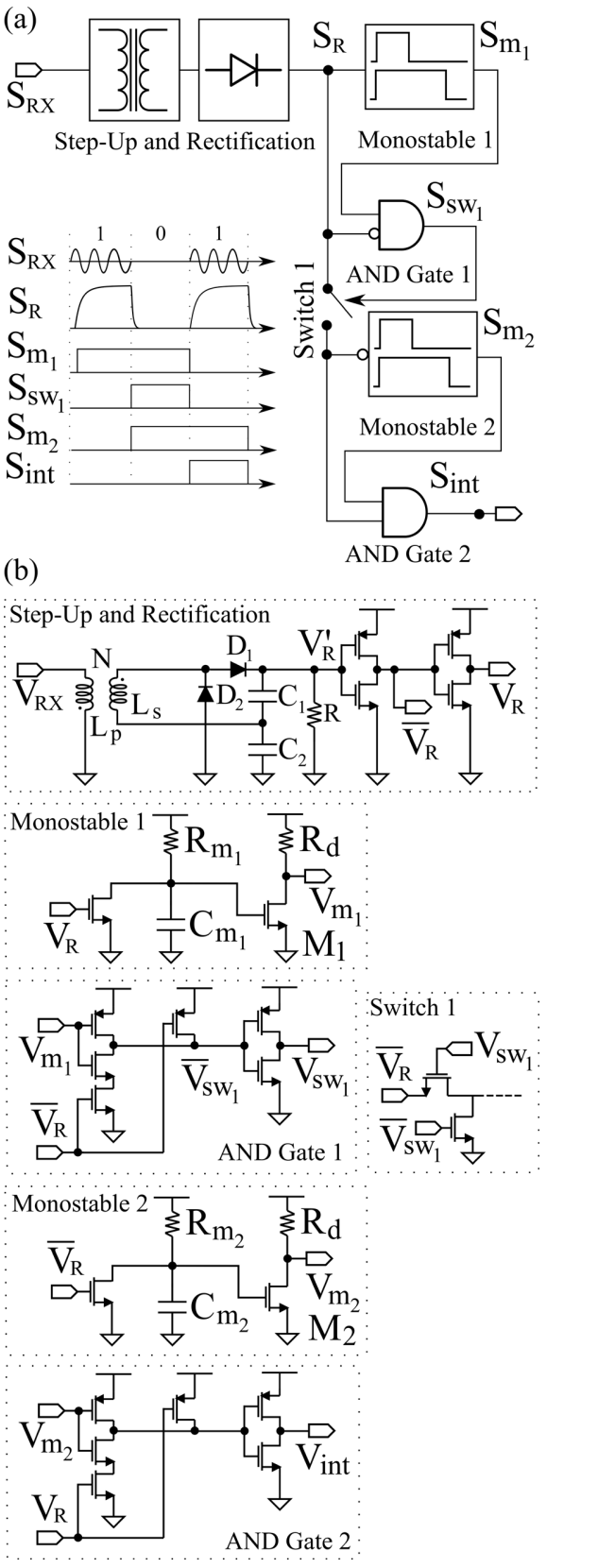

Fig. 2. (a) WuRx block diagram and example of waveforms when assuming that the WuC signal is 101. (b) Associated WuRx circuit implementation.

(6 transistors, 1 capacitor, 1 resistor) [16], we use a simpler circuit composed of 2 transistors, 1 capacitor and 2 resistors. This monostable works as follows: once V_R reaches the first monostable circuit, the capacitor C_{m_1} is discharged and transistor M_1 is switched off. As soon as V_R goes down, C_{m_1} gets charged with a time given by $C_{m_1} \times R_{m_1}$. Once the threshold voltage of M_1 is reached, V_{m_1} goes low, and the circuit works as a simple timer, triggered by the received voltage. The same reasoning applies for the others monostable circuits, which are enabled through the switches.

III. Simulations results

The proposed circuit implementation is validated at simulation level, by considering a TSMC-180nm CMOS model. An acoustic WuC signal with frequency $f_{input} = 40kHz$ is used as the input. The duration of the high and low logic values influences the design of the step-up and rectification circuits as well as the time constant of the monostables. The minimum duration of a logic value has to be greater than the period of the input signal, i.e. $T = 25\mu s$ for a correct rectifier operation. In our previous work we fixed the duration of the logic value to 1.5ms. Clearly, a shorter or longer duration can be considered since the time constant of the monostables is a design variable. In order to make a comparison with the previously proposed NOR-based monostable multivibrator, we fixed the duration of the logic values to 1.5ms, and the burst period to 3ms, i.e. same values considered in [15]. Initially the WuC signal 101 is considered. The parameters used for the simulations are shown in Table I. The supply voltage is 1.2V. The rectifier is designed so that its time constant is fast enough to be aligned with the associated burst. The monostables are designed so that their output voltages are high during the time intervals in which the comparison with the voltages V_R and $\overline{V}_R$ is performed. The transistors are designed to minimize the power consumption. Resistors with very high resistance (100MΩ) are used to minimize the average current and so the power consumption. Clearly these resistors are not feasible for Integrated Circuits, but they can be eventually mounted off-chip. In Fig.3(a) the voltage V_{RX} is shown which consists of two bursts with a frequency of 40kHz and an amplitude of 300mV. The voltage V'_R is the voltage across the resistor in the rectifier in Fig.2(b). This voltage has to be higher than the threshold voltage of the CMOS buffer. Thus the voltage after the buffer, i.e. V_R, ranges from zero volts to V_{DD} as required. As can be observed, V_R is aligned with V_{RX} and so with the WuC signal. In Fig.3(b) the output voltage of the first monostable (V_{m_1}) is shown.

TABLE I. Parameters used in the simulations

Component	Parameter	Value
Supply Voltage	V_{DD}	$1.2V$
Transformer	L_p	$4\mu H$
	L_s	$400\mu H$
Rectifier	C	$200nF$
	R	300Ω
Monostable	C_m	$51pF$
	R_m	$100M\Omega$
	R_d	$100M\Omega$

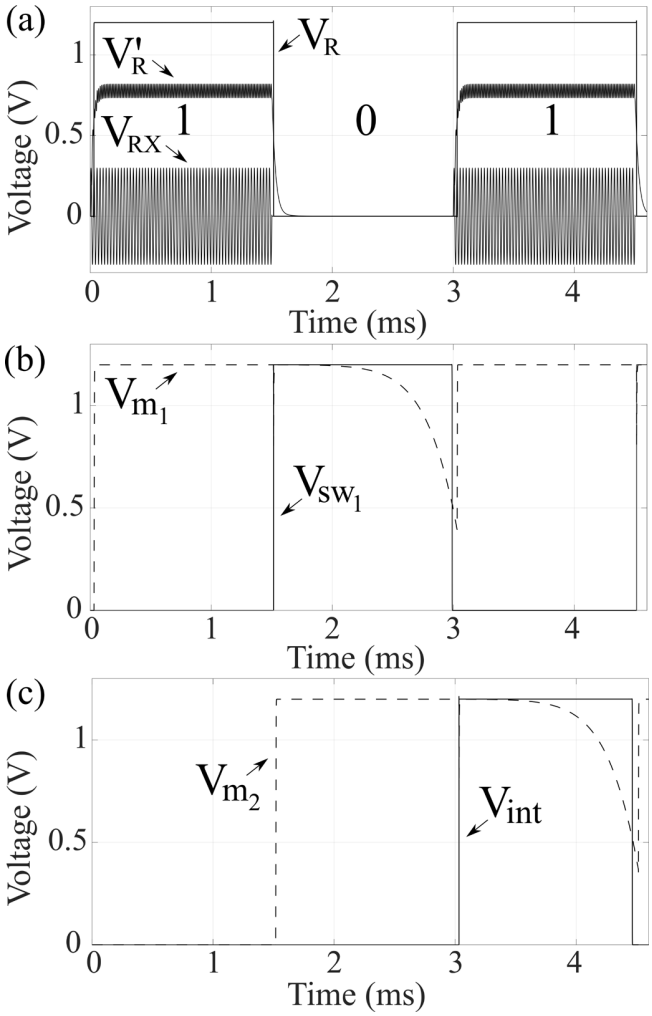

Fig. 3. Simulations results when the WuRx decodes the WuC signal 101: (a) V_{RX}, V'_R and V_R. (b) V_{m_1} and V_{sw_1}. (c) V_{m_2} and V_{int}.

As can be observed, once V_R goes low, V_{m_1} slowly goes low too. But around 3ms the output of the first monostable goes high again, since the capacitor C_{m_1} gets discharged by the last 1 in the WuC signal. This phenomenon does not affect the decoding mechanism, since the logic gate compares $\overline{V}_R$ with V_{m_1} during the time window [1.5ms–3.5ms]. As expected, V_{sw_1} closes Switch 1, resulting in the triggering of the second monostable. The latter generates V_{m_2}, which is then compared with V_R to produces V_{int}, as shown in Fig.3(c).

A. Power Consumption

When decoding the WuC signal 101, the simulated 3-value WuRx consumes 27.3nA which corresponds to an average power consumption of 32.8nW. Clearly, the power consumption is a function of the WuC signal complexity. In order to characterize the power consumption as a function of the number of decoded bits, different simulations have been performed. In particular, we considered five different N-value WuRxs, with N ranging from 3 up to 11, with steps of 2. This means that the less complex considered WuC signal is 101, decoded by a WuRx

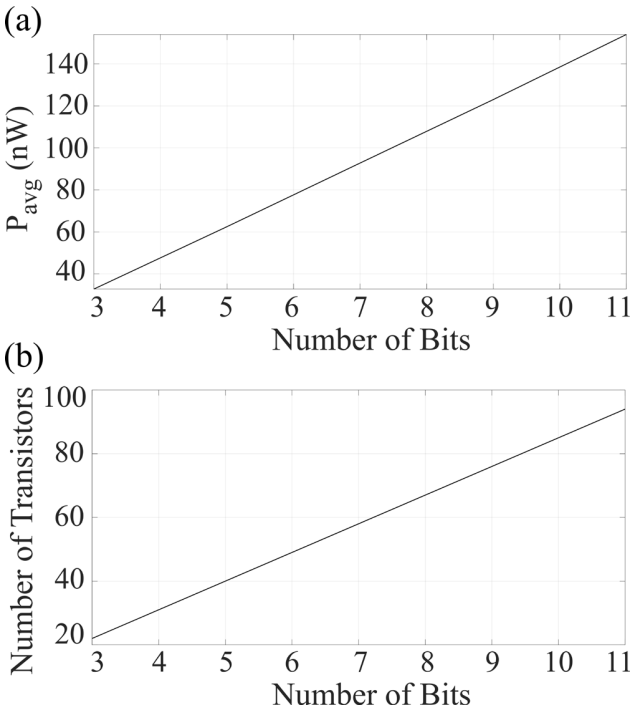

Fig. 4. (a) Simulated average power consumption and (b) number of required transistors as a function of number of bits in the WuC signal.

with two monostables and AND gates and one switch; while the more complex one is 10101010101, decoded by a WuRx with ten monostables and AND gates and nine switches. The average power consumption as a function of the decoded bits is shown in Fig.4(a). As can be observed, the power consumption linearly increases with the number of bits. When 3 bits are considered, the power consumption is 32.8nW, while when 11 bits are considered, the power consumption is 153nW. Each stage introduces about 15nW to the power consumption. In our previous work, the computed average power consumption when decoding a 4-value WuC was about 800nW, while the new implementation consumes about 47nW when decoding a WuC signal with the same complexity. Therefore the proposed monostable implementation is about 17 times more efficient than the NOR-based one. Regarding the number of required transistors, a 3-value WuRx needs 22 transistors, i.e. 9 per decoded bit, plus four transistors in the CMOS buffer. As previously explained, the first bit is used to trigger the system. For a 5-value WuRx the number of required transistors will be 40. For a 11-value WuRx 94 transistors are required.

TABLE II. PERFORMANCE COMPARISON

P_{active}	f_{input}	V_{DD}	Work
$32.8nW$	$40kHz$	$1.2V$	This
$8.1\mu W$	$85kHz$	$3.3V$	[18]
$420\mu W$	$20kHz$	$3V$	[19]
$14\mu W$	$40kHz$	$2V$	[20]
$4\mu W$	$43kHz$	$0.6V$	[21]
$8nW$	$57kHz$	$0.5V$	[17]
$1\mu W$	$41kHz$	$0.3V$	[22]

As can be observed in Fig.4(b), the number of transistors linearly increases with the number of bits. We compared the performance of the proposed WuRx with other WuRxs in Table II. We considered WuRxs to work in the same frequency range of the implemented one. As can be observed the proposed WuRx is ultra-low power, although it is not the least power consuming since the work in [17] consumes 8nW. However in that work the supply voltage is 0.5V. By reducing the supply voltage in our circuit to 0.6V, increasing the amplitude of the transmitted voltage to 400mV and increasing R_m to 200MΩ, the power consumption of our architecture lowers to 7.2nW. Clearly a fabricated low voltage WuRx would require a more precise design, due to leakages and the parasitics.

IV. CONCLUSIONS

In this article we proposed an ultra-low power monostable-based wake-up receiver for wireless sensor networks. The implemented circuit uses a simple timer for wake-up call decoding. It consumes 32.8nW when decoding three bits, and 153nW when decoding 11 bits with a supply voltage of 3.3V. The power consumption lowers to 7.2nW when the supply voltage is scaled down to 2V. Future work will focus on ASIC integration and circuit optimization.

REFERENCES

[1] G. Eason, N. Khalil, M. R. Abid, D. Benhaddou, and M. Gerndt, "Wireless sensors networks for Internet of Things," in 2014 IEEE Ninth International Conference on Intelligent Sensors, Sensor Networks and Information Processing (ISSNIP), 2014, pp. 1–6.

[2] S. M. Oteafy and H. S. Hassanein, "Resource Re-use in Wireless Sensor Networks: Realizing a Synergetic Internet of Things." J. Commun., vol. 7, no. 7, pp. 484–493, 2012.

[3] S. R. Jino Ramson and D. J. Moni, "Applications of wireless sensor networks — A survey," in 2017 International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology (ICEEIMT), 2017, pp. 325–329.

[4] W. Dargie and C. Poellabauer, Fundamentals of wireless sensor networks: theory and practice. John Wiley & Sons, 2010.

[5] F. K. Shaikh and S. Zeadally, "Energy harvesting in wireless sensor networks: A comprehensive review," Renewable and Sustainable Energy Reviews, vol. 55, pp. 1041–1054, 2016.

[6] F. Engmann, F. A. Katsriku, J.-D. Abdulai, K. S. Adu-Manu, and F. K. Banaseka, "Prolonging the lifetime of wireless sensor networks: a review of current techniques," Wireless Communications and Mobile Computing, vol. 2018, 2018.

[7] G. Anastasi, M. Conti, M. Di Francesco, and A. Passarella, "Energy conservation in wireless sensor networks: A survey," Ad hoc networks, vol. 7, no. 3, pp. 537–568, 2009.

[8] H. Yetgin, K. T. K. Cheung, M. El-Hajjar, and L. H. Hanzo, "A Survey of Network Lifetime Maximization Techniques in Wireless Sensor Networks," IEEE Communications Surveys Tutorials, vol. 19, no. 2, pp. 828–854, 2017.

[9] S. M. Chowdhury and A. Hossain, "Different energy saving schemes in wireless sensor networks: A survey," Wireless Personal Communications, vol. 114, no. 3, pp. 2043–2062, 2020.

[10] F. D. Tolba and P. Lorenz, "Based Energy-Efficient for Extending Mobile Wireless Sensor Networks Lifetime," Journal of Communications, vol. 14, no. 12, 2019.

[11] N. Lavanya and T. Shankar, "Energy efficient cluster head selection using hybrid squirrel harmony search algorithm in WSN," Energy, vol. 10, no. 12, 2019.

[12] R. Piyare, A. L. Murphy, C. Kiraly, P. Tosato, and D. Brunelli, "Ultra Low Power Wake-Up Radios: A Hardware and Networking Survey," IEEE Communications Surveys Tutorials, vol. 19, no. 4, pp. 2117–2157, 2017.

[13] H. Bello, Z. Xiaoping, R. Nordin, and J. Xin, "Advances and opportunities in passive wake-up radios with wireless energy harvesting

for the internet of things applications," Sensors, vol. 19, no. 14, p. 3078, 2019.

[14] I. Demirkol, C. Ersoy, and E. Onur, "Wake-up receivers for wireless sensor networks: benefits and challenges," IEEE Wireless Communications, vol. 16, no. 4, pp. 88–96, 2009.

[15] A. Nowbahari, L. Marchetti, and M. Azadmehr, "An Ultra-Low Power Multivibrator-Based Wake-up Receiver for Wireless Sensor Networks," in 2021 IEEE 7th World Forum on Internet of Things (WF-IoT), 2021, pp. 380–384.

[16] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation. John Wiley & Sons, 2019, ch. 18, pp. 539–540.

[17] A. S. Rekhi and A. Arbabian, "Ultrasonic Wake-Up With Precharged Transducers," IEEE Journal of Solid-State Circuits, vol. 54, no. 5, pp. 1475–1486, 2019.

[18] A. Sanchez, S. Blanc, P. Yuste, A. Perles, and J. J. Serrano, "An Ultra-´ Low Power and Flexible Acoustic Modem Design to Develop EnergyEfficient Underwater Sensor Networks," Sensors, vol. 12, no. 6, pp. 6837–6856, 2012.

[19] A. Bannoura, F. Hoflinger, O. Gorgies, G. U. Gamm, J. Albesa, and¨ L. M. Reindl, "Acoustic Wake-Up Receivers for Home Automation Control Applications," Electronics, vol. 5, no. 1, p. 4, 2016.

[20] E. Lattanzi, M. Dromedari, V. Freschi, and A. Bogliolo, "A sub-µA ultrasonic wake-up trigger with addressing capability for wireless sensor nodes," International Scholarly Research Notices, vol. 2013, 2013.

[21] K. Yadav, I. Kymissis, and P. R. Kinget, "A 4.4uW wake-up receiver using ultrasound data communications," in 2011 Symposium on VLSI Circuits - Digest of Technical Papers, 2011, pp. 212–213.

[22] H. Fuketa, S. O'uchi, and T. Matsukawa, "A 0.3-V 1-µW SuperRegenerative Ultrasound Wake-Up Receiver With Power Scalability," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 9, pp. 1027–1031, 2017.

B.4 An Oscillator-Based Wake-Up Receiver for Wireless Sensor Networks

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An Oscillator-Based Wake-Up Receiver for Wireless Sensor Networks

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***Abstract*—The Internet of Things (IoT) concept is mainly enabled by wireless sensor networks (WSNs), which are continuously gaining attention, due to their multidisciplinary applications. To enhance the WSNs energy efficiency, different solutions have been proposed. One of them is the integration of wake-up receivers (WuRxs), which activate the sensor nodes through an identity-based approach. In this work a low power oscillator-based WuRx architecture is presented, and verified by simulations in TSMC-180nm CMOS process. The WuRx sequentially verifies if the received signal resembles the wake-up call (WuC) one by means of oscillators, counters and logic gates. It consumes 16.1µW when detecting a 1.6ms WuC signal, and 1.2nW in idle mode.**

***Keywords*—Logic circuits, low-power electronics, oscillators, receivers, wireless sensor networks.**

I. Introduction

The Internet of Things (IoT) paradigm is continuously raising attention both in academia and industry: by the end of 2026, the number of IoT connections is expected to be about 26.9 billion [1]. One of the main IoT enabling technologies is the wireless sensor network (WSN) one, which refers to a group of wirelessly connected sensor nodes [2]. The latter are able to collect, elaborate, and transmit signals, and are typically battery-powered. The sensor node power management is critically important, since it determines the WSN energy efficiency and lifetime. The latter can be increased by optimizing the network power consumption, implementing energy harvesting techniques, and employing backscatter networks [3]. A largely employed energy-saving protocol is the duty-cycled Medium Access Control (MAC) one, which consists in turning on/off the sensor nodes during specific time windows. Such a protocol intrinsically suffers from idle listening (sensor nodes are on even if no access is required) and overhearing (a sensor node receives a message not intended to it). These issues could be solved by integrating wake-up receivers (WuRxs), which wake up the sensor nodes from sleep mode only when the wake-up call (WuC) signal is received (Fig. 1) [4]. This implies that the sensor nodes are on only when required, resulting in an energy efficient solution [5]. WuRxs can be RF based or non-RF based, depending on the application. Most of the reported WuRxs are RF based [6]–[10], but also optical [11]–[14] and acoustic receivers have been proposed [15]–[21]. In this work a low power oscillator-based WuRx concept is proposed. The architecture block diagram is described in section II. A circuit implementation is presented in section III. The simulations results are in section IV, while the conclusions are in section V.

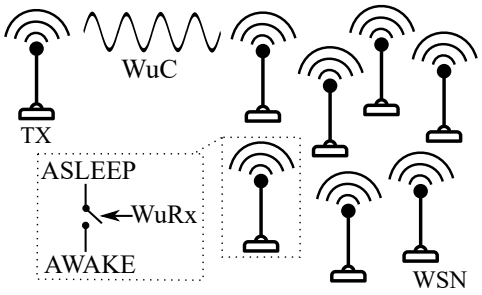

Fig. 1. A wireless sensor network integrating WuRxs.

II. Architecture

The proposed architecture is shown in Fig. 2. The transmitter sends the WuC signal (S_{WuC}), which typically consists of sinusoidal bursts. The burst duration establishes the number of high states ('1's) associated to that burst, while the time interval between two bursts establishes the number of low states ('0's) associated to that time interval. The amplitude of S_{WuC} is typically affected by losses (e.g. attenuation) during the transmission. Therefore the amplitude of the received signal (S_{in}) could be increased through a step-up transformer (S_{up}). Next this signal is rectified (S_{rect}), and sent into the pulse extractor. The latter generates N square waves (e.g. $S_{1,2,3}$ in Fig. 2), with duration equal to that of the received '0's and '1's. After the extraction, the first pulse (S_1) is sent into the first pulse meter (P_1), which is composed of a switch, an oscillator, two counters and a one shot monostable. The pulse meters verify if the received signal (S_{in}) resembles the wake-up call one: the oscillators, in conjunction with the counters, measure the duration of the extracted pulses. The verification process is sequential, i.e. if the duration of the first extracted pulse does not resemble the first state of the WuC signal, the successive pulse meters are not enabled. To explain the WuRx operation, suppose that the WuC signal is a sequence of $N = 3$ states (e.g. '101'), and that M oscillations are associated to the correct detection of each state. Assume also that the switches $sw_{1,2,3}$ are all initially closed, and that all the counters are divide-by-M counters. Considering the first pulse meter, at the oscillator 1 output three cases can be distinguished:

- case 1: there are less than M oscillations;
- case 2: there are more than M oscillations;

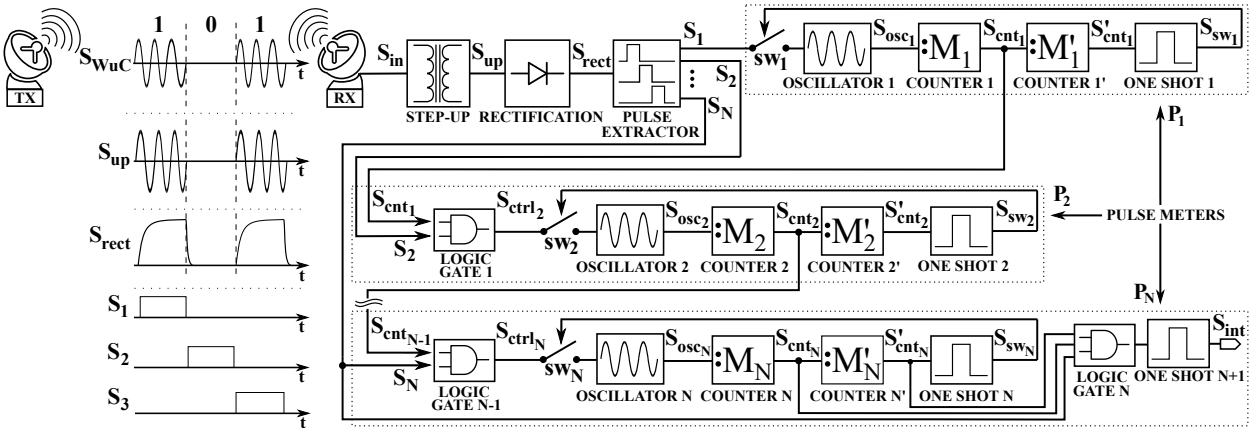

Fig. 2. Oscillator-based wake-up receiver architecture.

- case 3: there are exactly M oscillations.

In case 1, the oscillator 1 output (S_{osc_1}) has less than M oscillations. Consequently both the counters and one shot 1 are off. The output of counter 1 (S_{cnt_1}) goes, together with the second extracted pulse (S_2), into logic gate 1. Since counter 1 is off, the logic gate 1 output (S_{ctrl_2}), which is the control signal of oscillator 2, is not asserted. Hence the second pulse meter (P_2) is not enabled. In case 2, there are more than M oscillations at the counter 1 input. Therefore also the counter $1'$ output (S'_{cnt_1}) is asserted. The latter activates one shot 1, which opens the switch sw_1. Counter $1'$ and one shot 1 are used to avoid extra oscillations, thus minimizing the power consumption. In case 3, the counter 1 output is asserted, since exactly M oscillations are present at its input, while counter $1'$ and one shot 1 are off. As a consequence logic gate 1 will let S_2 reach the second oscillator, thus enabling P_2. The control signal (S_{ctrl_2}) coincides with the second pulse (S_2) only if exactly M oscillations are detected. As before, oscillator 2, in conjunction with the counters and one shot 2, verifies if S_2 resembles the WuC signal. If this is the case, logic gate 2 will let S_3 reach the last oscillator. If the last state is correct (i.e. S_3 causes M oscillations), the logic gate 3 output will be asserted, and one shot 4 will finally generate the wake-up interrupt signal (S_{int}), which activates the sensor node. For an N states WuC signal, the proposed architecture has: N switches, oscillators, and logic gates, $2N$ counters and $N+1$ one shots. All the pulse meters have a logic gate at their input, except the first one (P_1), which is by default enabled. The last pulse meter (P_N) has an additional logic gate and one shot for interrupt signal generation.

III. Circuit Implementation

In this section the circuit implementation of an oscillator-based WuRx with $M = 2$ is proposed. A Delon voltage doubler, shown in Fig. 3(a), is implemented to step up (V_{up}) and rectify (V'_{rect}) the received input voltage (V_{in}) [22]. The resistor (R) is used to discharge V'_{rect}, which is then buffered. The buffer output (V_{rect}) is sent into the pulse extractor. The latter is designed according to the predefined WuC signal.

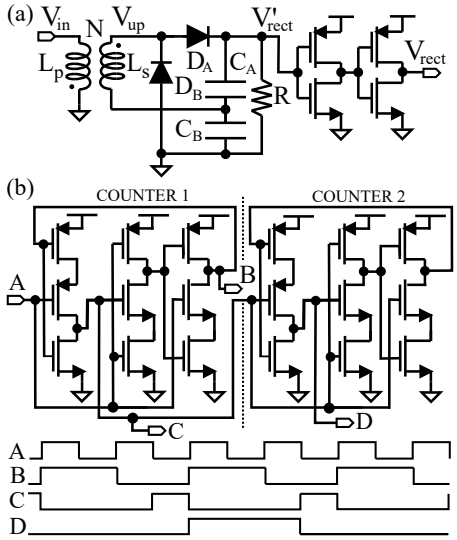

Fig. 3. (a) Delon voltage doubler. (b) Cascade of divide-by-two counters.

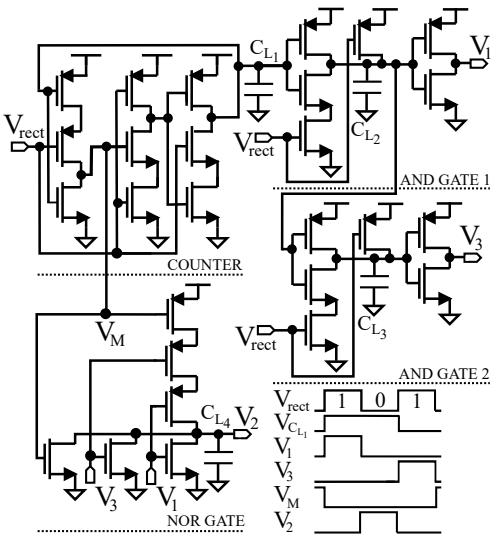

Fig. 4. Circuit implementation of a '101' pulse extractor.

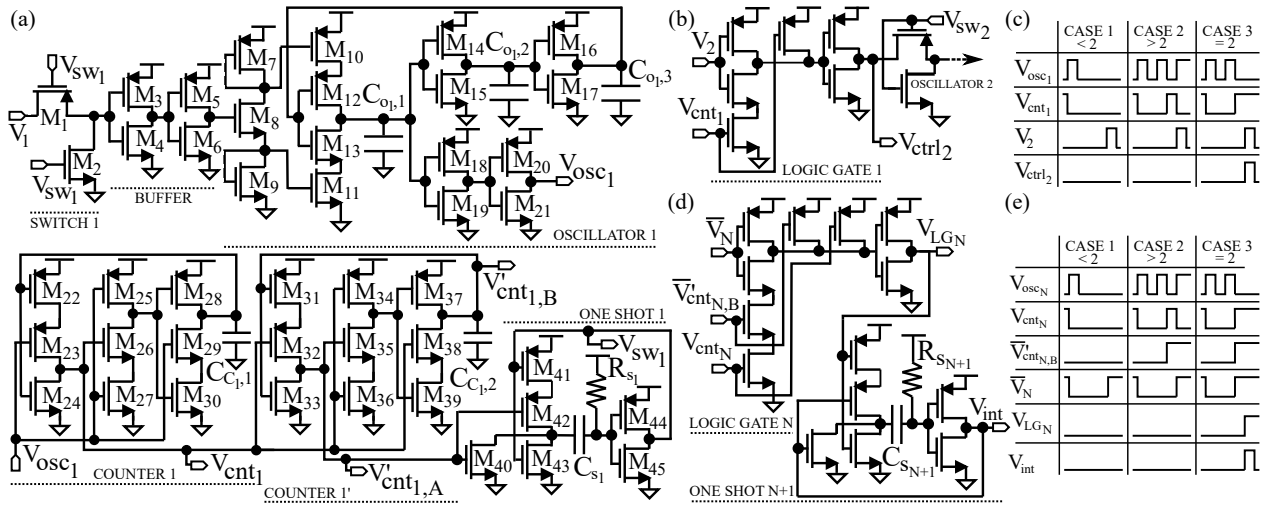

Fig. 5. (a) Pulse meter 1 (P_1). (b) Logic gate 1 and (c) its waveforms. (d) Logic gate N and (e) its waveforms.

A possible approach consists into using logic gates, and the CMOS counter shown in Fig. 3(b) [23]. A '101' pulse extractor implementation is shown in Fig. 4. The counter has two outputs: $V_{C_{L_1}}$ and V_M, i.e. signals B and C in Fig. 3(b). The first pulse (V_1) could be extracted through the AND logical operation $V_{C_{L_1}} \cdot V_{rect}$. The third pulse ($V_3$) could be obtained through the AND logical operation $\overline{V_1} \cdot V_{rect}$, where $\overline{V_1}$ is the inverted first pulse. The pulse associated to the state '0' could be obtained by using the NOR logical operation $\overline{V_M + V_1 + V_3}$. Longer WuCs could be extracted by simply implementing more counters and logic gates. After the extraction process, the first pulse is sent into the first pulse meter (P_1), shown in Fig. 5(a). Transistors M_{1-2} implement the switch sw_1 in Fig. 2, while transistors M_{3-6} implement a buffer. Oscillator 1 (M_{7-21}) is implemented as a current starved ring oscillator with output-switching [24]. Counter 1 (M_{22-30}) and 1′ (M_{31-39}) are divide-by-two counters (Fig. 3(b)), while the transistors M_{40-45}, the resistor R_{S_1} and the capacitor C_{S_1} implement one shot 1 [25]. The adopted counter topology implies that the extracted pulse has to cause two oscillations (i.e. $M = 2$) for a correct pulse detection. If more oscillations are detected, the output of counter 1′ ($V'_{cnt_1,A}$) will be asserted. Consequently one shot 1 will be triggered, and its output (V_{sw_1}) will disconnect, trough M_{1-2}, oscillator 1 from the pulse extractor. According to Fig. 2, the counter 1 output goes, together with the second extracted pulse, into logic gate 1, which is implemented as an AND gate (Fig. 5(b)). The latter is present at the input of all the pulse meters, except the first one, which is by default enabled (Fig. 5(a)). As shown in Fig. 5(c), the logic gate 1 output (V_{ctrl_2}) is asserted only if exactly two oscillations are detected by counter 1. Other input combinations lead to zero volts. The last pulse meter (P_N) is the one that asserts the wake-up interrupt voltage (V_{int}). As compared to the other pulse meters, it presents an additional logic gate and one shot, shown in Fig. 5(d). The interrupt signal is asserted only if the last pulse (V_N) causes two oscillations. Logic gate N receives also the inverted last pulse ($\overline{V_N}$) in order to not trigger the one shot $N+1$ when case 2 happens.

IV. Simulation Results

To verify the proposed architecture, a WuRx with $N = 3$ states has been simulated in TSMC-180nm CMOS process. The simulation parameters are in Table 1. The input, stepped up and rectified voltages are shown in Fig. 6(a). The WuC signal is '101', with each burst having a frequency of $100kHz$ and a duration of $0.5ms$. WuRxs working with frequencies ranging from $20kHz$ to $100kHz$ are typically acoustic ones. A burst with higher frequency would imply different Delon voltage doubler components, as well as a different oscillator design. The supply voltage (V_{DD}) is $1.2V$, and the inverters are sized with symmetric switching point around $V_{DD}/2$. The logic gates transistors are sized with unit width and length. The oscillator bias stage is sized in order to oscillate $M = 2$ times for each state. All the one shots resistors are implemented through a cascade of two diode-connected PMOS with minimum width and length. A buffer has been added to the last one shot. The simulations results validated the proposed concept. Considering P_1, when V_1 is longer than expected, more than two oscillations (V_{osc_1}) are observed (Fig. 6(b)). So the counter

Table 1. Circuit simulation parameters.

Component	Parameter	Value
Voltage Doubler	$L_{p,s}$	$4\mu H$,$400\mu H$
	$C_{A,B}$	$200nF$
	R	500Ω
Pulse Extractor	$C_{L,1,2,3,4}$	$5pF, 1pF, 15pF, 1pF$
Pulse Meter 1	$C_{o_1,1,2,3}$	$180pF$,$520pF$,$1.8nF$
	$C_{C_1,1,2}$	$5pF, 1pF$
	C_{s_1}	$3pF$
Pulse Meter 2	$C_{o_2,1,2,3}$	$100pF$,$570pF$,$2.1nF$
	$C_{C_2,1,2}$	$5pF, 1pF$
	C_{s_2}	$3pF$
Pulse Meter 3	$C_{o_3,1,2,3}$	$320pF$,$550pF$,$900pF$
	$C_{C_3,1,2}$	$5pF, 1pF$
	$C_{s_{3,4}}$	$3pF, 3.4pF$

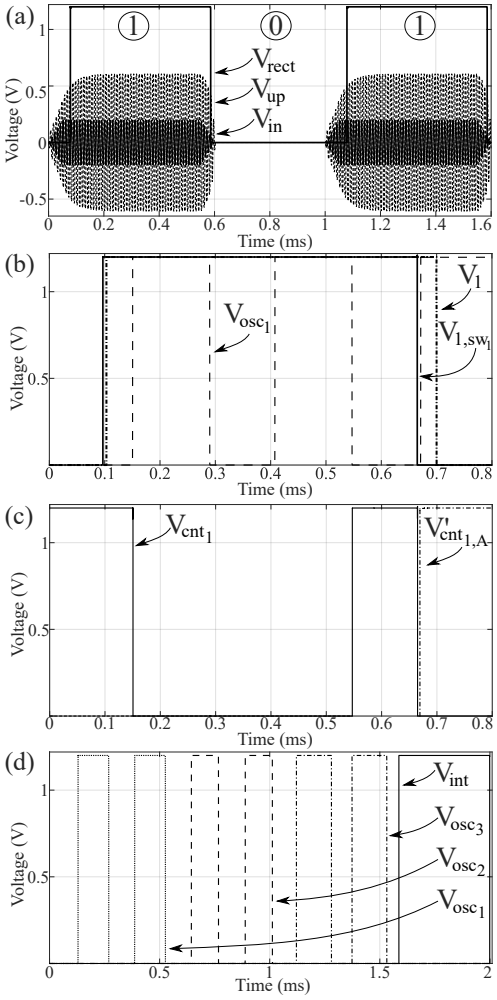

Fig. 6. (a) V_{in}, V_{up} and V_{rect}. (b) V_{osc_1}, V_1 and V_{1,sw_1} (case 2). (c) V_{cnt_1} and $V'_{cnt_{1,A}}$(case 2). (d) $V_{osc_{1,2,3}}$ and V_{int} (case 3).

$1'$ output ($V'_{cnt_{1,A}}$) goes high, as shown in Fig. 6(c). As a consequence the one shot 1 opens switch sw_1, and the resulting voltage (V_{1,sw_1}) after the switch is shorter, thus preventing extra oscillations, and so higher power consumption. If all the extracted pulses cause two oscillations per pulse meter, finally the interrupt voltage (V_{int}) is generated (Fig. 6(d)). The duration of V_{int} is set by the RC group of one shot 4, and is application dependent. In active mode (i.e. when detecting the $1.6ms$ WuC signal), the WuRx consumes $13.4\mu A$, at which corresponds an average power consumption of $16.1\mu W$. In idle mode (i.e. $V_{in} = 0V$), the WuRx consumers $1nA$, at which corresponds an average power consumption of $1.2nW$. The power consumption in the active mode is dependent on the complexity of the WuC signal and on the adopted counter topology. A longer WuC signal would imply more pulse meters, while a higher measurement precision would require more counters per pulse meter. A comparison with other WuRxs working in the same frequency range is reported in Table 2. The proposed circuit implementation is low power in active mode, and ultra-low power in idle mode.

Table 2. Power consumption comparison.

$\mathbf{P_{idle}}$	$\mathbf{P_{active}}$	$\mathbf{f_{input}}$	$\mathbf{V_{dd}}$	**Work**
$1.2nW$	$16.1\mu W$	$100kHz$	$1.2V$	This
$3\mu W$	$8.1\mu W$	$85kHz$	$3.3V$	[18]
$1.64\mu W$	$14\mu W$	$40kHz$	$2V$	[17]
–	$4\mu W$	$43kHz$	$0.6V$	[15]
$45\mu W$	$420\mu W$	$20kHz$	$3V$	[19]

V. Conclusions

In this work an oscillator-based wake-up receiver concept for wireless sensor networks is proposed. The WuRx extracts pulses associated to the duration of the received states. So it uses oscillators in conjunction with counters and logic gates to sequentially verify if the received signal resembles the WuC signal. The WuRx is able to manage cases in which the pulse measurement is not correct, avoiding unnecessary power consumption. Simulations in TSMC-180nm CMOS process verified the architecture. For the detection of a $1.6ms$ WuC signal it consumes $16.1\mu W$, while in idle mode only $1.2nW$. Future research directions will focus on power consumption optimization and experimental validation.

Acknowledgment

This work was supported by the Research Council of Norway [273248].

References

[1] "Ericsson Mobility Report," Ericsson, Stockholm, Sweden, Tech. Rep., November 2020.

[2] A. Al-Fuqaha, M. Guizani, M. Mohammadi, M. Aledhari, and M. Ayyash, "Internet of Things: A Survey on Enabling Technologies, Protocols, and Applications," *IEEE Communications Surveys Tutorials*, vol. 17, no. 4, pp. 2347–2376, 2015.

[3] D. Ciuonzo, G. Gelli, A. Pescapé, and F. Verde, "Decision fusion rules in ambient backscatter wireless sensor networks," in *2019 IEEE 30th annual international symposium on personal, indoor and mobile radio communications (PIMRC)*. IEEE, 2019, pp. 1–6.

[4] I. Demirkol, C. Ersoy, and E. Onur, "Wake-up receivers for wireless sensor networks: benefits and challenges," *IEEE Wireless Communications*, vol. 16, no. 4, pp. 88–96, 2009.

[5] R. Piyare, A. L. Murphy, C. Kiraly, P. Tosato, and D. Brunelli, "Ultra Low Power Wake-Up Radios: A Hardware and Networking Survey," *IEEE Communications Surveys Tutorials*, vol. 19, no. 4, pp. 2117–2157, 2017.

[6] D. Galante-Sempere, D. Ramos-Valido, S. Lalchand Khemchandani, and J. Del Pino, "Low-Power RFED Wake-Up Receiver Design for Low-Cost Wireless Sensor Network Applications," *Sensors*, vol. 20, no. 22, p. 6406, 2020.

[7] D. D. Wentzloff, A. Alghaihab, and J. Im, "Ultra-Low Power Receivers for IoT Applications: A Review," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2020, pp. 1–8.

[8] J. Moody, P. Bassirian, A. Roy, N. Liu, N. S. Barker, B. H. Calhoun, and S. M. Bowers, "Interference Robust Detector-First Near-Zero Power Wake-Up Receiver," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2149–2162, 2019.

[9] S. Koeble, S. Heller, and P. Woias, "A narrow-band and ultra-low-power 433 MHz wake-up receiver," in *Journal of Physics: Conference Series*, vol. 1407, no. 1. IOP Publishing, 2019, p. 012093.

[10] T. Ma, "A Bit Sampled Wake-Up Receiver with Logarithmic Detector Architecture," in *2017 International Conference on Cyber-Enabled Distributed Computing and Knowledge Discovery (CyberC)*. IEEE, 2017, pp. 445–449.

[11] J. Chen, Z. Dai, and Z. Chen, "Development of Radio-Frequency Sensor Wake-Up with Unmanned Aerial Vehicles as an Aerial Gateway," *Sensors*, vol. 19, no. 5, p. 1047, 2019.

[12] U. Dudko and L. Overmeyer, "Optical Wake-Up From Power-Off State for Autonomous Sensor Nodes," *IEEE Sensors Journal*, vol. 21, no. 3, pp. 3225–3232, 2021.

[13] G. Kim, Y. Lee, S. Bang, I. Lee, Y. Kim, D. Sylvester, and D. Blaauw, "A 695 pW standby power optical wake-up receiver for wireless sensor nodes," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*. IEEE, 2012, pp. 1–4.

[14] W. Lim, T. Jang, I. Lee, H.-S. Kim, D. Sylvester, and D. Blaauw, "A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*. IEEE, 2016, pp. 1–2.

[15] K. Yadav, I. Kymissis, and P. R. Kinget, "A 4.4uW wake-up receiver using ultrasound data communications," in *2011 Symposium on VLSI Circuits - Digest of Technical Papers*, 2011, pp. 212–213.

[16] Y. C. Wong, S. H. Tan, R. S. S. Singh, H. Zhang, A. Syafeeza, and N. Hamid, "Low power wake-up receiver based on ultrasound communication for wireless sensor network," *Bulletin of Electrical Engineering and Informatics*, vol. 9, no. 1, pp. 21–29, 2020.

[17] E. Lattanzi, M. Dromedari, V. Freschi, and A. Bogliolo, "A sub-μA ultrasonic wake-up trigger with addressing capability for wireless sensor nodes," *International Scholarly Research Notices*, vol. 2013, 2013.

[18] A. Sánchez, S. Blanc, P. Yuste, A. Perles, and J. J. Serrano, "An Ultra-Low Power and Flexible Acoustic Modem Design to Develop Energy-Efficient Underwater Sensor Networks," *Sensors*, vol. 12, no. 6, pp. 6837–6856, 2012.

[19] A. Bannoura, F. Höflinger, O. Gorgies, G. U. Gamm, J. Albesa, and L. M. Reindl, "Acoustic Wake-Up Receivers for Home Automation Control Applications," *Electronics*, vol. 5, no. 1, p. 4, 2016.

[20] H. Fuketa, S. O'uchi, and T. Matsukawa, "A 0.3-V 1-μW Super-Regenerative Ultrasound Wake-Up Receiver With Power Scalability," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 9, pp. 1027–1031, 2016.

[21] F. Höflinger, G. U. Gamm, J. Albesa, and L. M. Reindl, "Smartphone remote control for home automation applications based on acoustic wake-up receivers," in *2014 IEEE International Instrumentation and Measurement Technology Conference (I2MTC) Proceedings*. IEEE, 2014, pp. 1580–1583.

[22] A. Mouapi, N. Hakem, and N. Kandil, "Performances Comparison of Shottky Voltage Doubler Rectifier to support RF Energy Harvesting," in *2020 IEEE International Conference on Environment and Electrical Engineering and 2020 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, 2020, pp. 1–5.

[23] J.-R. Yuan, "Efficient CMOS counter circuits," *Electronics Letters*, vol. 24, no. 21, pp. 1311–1313, 1988.

[24] G. Jovanovic, M. Stojcev, and Z. Stamenkovic, "A CMOS voltage controlled ring oscillator with improved frequency stability," *Scientific Publications of the State University of Novi Pazar, Series A: Applied Mathematics, Informatics and mechanics*, vol. 2, no. 1, pp. 1–9, 2010.

[25] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*. John Wiley & Sons, 2019, ch. 18, pp. 539–540.

B.5 Low Power Wake-Up Receivers for Underwater Acoustic Wireless Sensor Networks

A. Nowbahari, L. Marchetti and M. Azadmehr, 'Low Power Wake-Up Receivers for Underwater Acoustic Wireless Sensor Networks,' *IEEE Transactions on Green Communications and Networking*, Under Review.

Unpublished article, not included in online edition

Appendix C

Publications on Schmitt Triggers

C.1 Weak Inversion Model of an Inverting CMOS Schmitt Trigger

A. Nowbahari, L. Marchetti and M. Azadmehr, 'Weak Inversion Model of an Inverting CMOS Schmitt Trigger,' in *2022 11th International Conference on Communications, Circuits and Systems (ICCCAS)*, 2022, pp. 1–5. DOI: 10.1109/ICCCAS55266.2022.9824290

The attached paper is the accepted version of the IEEE copyrighted paper.

Weak Inversion Model of an Inverting CMOS Schmitt Trigger

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***Abstract*— In this article the subthreshold characteristics of an inverting single input CMOS Schmitt trigger circuit are analyzed. Analytical expressions for the low-to-high and high-to-low hysteresis transition voltages are determined. The analytical model provides physical insight into the circuit behavior. The derived expressions are linearly dependent on the supply voltage and the temperature, and logarithmically dependent on the dimensions of the transistors. Simulation results validated the proposed model, with a maximum error between the analytical and simulated transition points smaller than 14mV. An ASIC in AMS 0.35µm CMOS process has been fabricated to experimentally validate the derived expressions. The maximum error between the analytical and measured transition points is below 36mV.**

Keywords—CMOS, hysteresis, low voltage, Schmitt trigger, subthreshold, weak inversion.

I. INTRODUCTION

The Internet-of-Things paradigm is continuously raising attention both in industry and academia. According to the McKinsey Global Institute the IoT is expected to have an economic impact of $11.1 trillion by 2025 [1], with more than 30 billion units connected. At hardware level, one critical challenge is to optimize the energy efficiency of the implemented electronic devices. Considering, for instance, wireless sensor networks, which are one of the main IoT enabling technologies, the power consumption of the employed devices represents the main limitation in terms of network lifetime [2]. Different solutions have been proposed for optimizing the energy efficiency of these networks [3], [4]. At device level, a widely implemented technique consists into scaling the supply voltage, thus reducing the power consumption of the circuits [5]. When the supply voltage becomes lower than the threshold voltages of the transistors, the latter are said to work in subthreshold region. When this occurs, transistors do not operate in strong inversion, but in weak inversion. This implies that different analytical models have to be used to correctly describe the behavior of the electronic circuits [6]. Both in analog and digital applications, a widely implemented circuit is the Schmitt trigger (ST) one. The symbol of a single input voltage mode ST circuit is shown in Fig. 1(a), while its typical hysteretic characteristic is shown in Fig. 1(b). STs are implemented in comparators, oscillators, converters and many others circuits [7]. Due to the voltage supply scaling trend, many researchers are modeling and employing Schmitt trigger circuits in weak inversion [8]–[14]. In this article we analyze the subthreshold characteristics of the Schmitt trigger circuit proposed by Al-Sarawi in 2002 [15]. The circuit under analysis is a single input inverting CMOS Schmitt trigger, and it is shown in Fig. 1(c). The bulk terminals are not shown for simplicity. The PMOS transistors have the bulk terminals connected to the supply voltage, while the NMOS transistors to the ground. This circuit has not been yet modeled in weak inversion. We have chosen to model the subthreshold characteristics of this circuit because is a low power Schmitt trigger circuit [7]. In this article we derive simple expressions for the high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages, which define the hysteresis of the ST, as can be observed in Fig. 1(b). The derived expressions have been validated with simulations and measurements, by testing a ST circuit fabricated in AMS 0.35µm CMOS process, through EUROPRACTICE MPW.

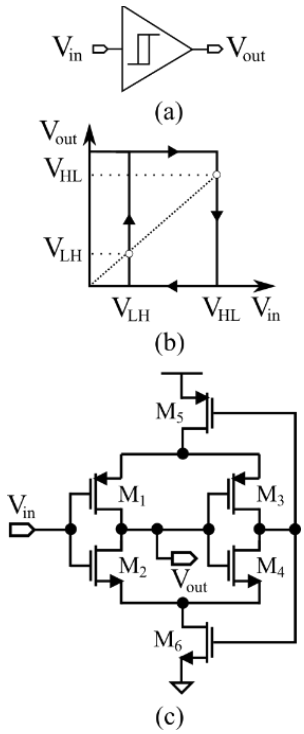

Fig. 1. (a) Schmitt trigger symbol. (b) Typical V_{out} vs V_{in}. (c) Schmitt trigger circuit analyzed in this work.

This work was supported by the Research Council of Norway [273248].

The derived mathematical model provides physical insight into the circuit behavior, allowing designers to have a clear understanding of the influence of the involved parameters. The expressions show the relationship between the hysteresis transition voltages and the supply voltage. Furthermore, they also show the dependence on the temperature, through the thermal voltage. The model is derived in Section II, and validated through simulations and experiments in Section III. The conclusions are in Section IV.

II. Analytical Model

In weak inversion, the MOSFET drain current, according to EKV model [16], can be expressed as

$$I_{d,n(p)} = I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}} \cdot \left(e^{-\frac{V_{SB(BS)}}{\phi}} - e^{-\frac{V_{DB(BD)}}{\phi}} \right) \quad (1)$$

$$I_{0,n(p)} = 2 \cdot n_{n(p)} \cdot \mu_{n(p)} \cdot C_{ox} \cdot \frac{W}{L} \cdot \phi^2 \cdot e^{\frac{|V_{th,n(p)}|}{n_{n(p)}}} \quad (2)$$

where:

- G → gate, D → drain, S → source, B → bulk;
- $n_{n(p)}$ → is the NMOS (PMOS) slope factor;
- ϕ → thermal voltage;
- $\mu_{n(p)}$ → NMOS (PMOS) carrier mobility,
- C_{ox} → oxide capacitance;
- W → MOSFET width;
- L → MOSFET length;
- $V_{th,n(p)}$ → NMOS (PMOS) threshold voltage.

When in saturation ($|V_{DS}| \gtrsim 3 \cdot \phi$ [17]), the drain current expression (1) can be simplified to

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)} - n_{n(p)} \cdot V_{SB(BS)}}{n_{n(p)} \cdot \phi}}. \quad (3)$$

Moreover, if the bulk-source voltage is equal to zero volts, the last equation can be expressed as

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}}. \quad (4)$$

First we show how to derive the high-to-low voltage (V_{HL}), i.e. the input voltage at which V_{out} goes from high to low. According to Fig. 2(a), when the input (V_{in}) is low, V_{out} is high since the ST circuit under analysis is an inverting one. Under these assumptions, M_3 is off, while $M_{1,4,5}$ are conducting. V_{HL} can be then determined by finding the switching voltage of the inverter composed of $M_{1,2}$, with finite voltage $V_{m,n}$ across M_6 [7]. Assuming all transistors in saturation, the equation relating transistors M_1 and M_2 is given by:

$$I_{0,p1} \cdot e^{\frac{V_{dd} - V_{HL}}{n_p \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{HL} - n_n \cdot V_{m,n}}{n_n \cdot \phi}} \quad (5)$$

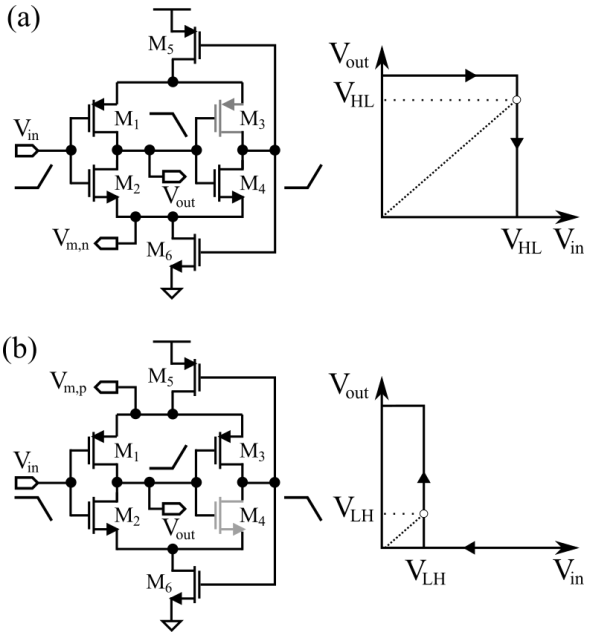

Fig. 2. Schmitt trigger circuits for (a) high-to-low (V_{HL}) and (b) low-to-high (V_{LH}) transition voltages analysis.

where V_{dd} is the supply voltage. As can be observed, the voltage across M_6 ($V_{m,n}$) is unknown in (5). To determine $V_{m,n}$, we can equate the current in M_2 and M_6:

$$I_{0,n6} \cdot e^{\frac{V_{m,n}}{n_n \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{HL} - n_n \cdot V_{m,n}}{n_n \cdot \phi}}, \quad (6)$$

$$V_{m,n} = \frac{V_{HL} + n_n \cdot \phi \cdot log\left(\frac{I_{0,n2}}{I_{0,n6}}\right)}{1 + n_n}. \quad (7)$$

Now that an expression for $V_{m,n}$ is determined, we can substitute (7) in (5), and solve for V_{HL}. The final result is shown in (8).

$$V_{HL} = \frac{n_n \cdot \left\{ V_{dd} \cdot (1 + n_n) - n_p \cdot \phi \cdot \left[log\left(\frac{I_{0,n2}}{I_{0,p1}}\right) + n_n \cdot log\left(\frac{I_{0,n6}}{I_{0,p1}}\right) \right] \right\}}{n_n^2 + n_n + n_p} \quad (8)$$

As can be observed, V_{HL} is linearly dependent on the supply voltage and the thermal voltage. Instead, the dependence on the transistors dimensions is logarithmic. Interestingly, if the ratios $I_{0,n2}/I_{0,p1}$ and $I_{0,n6}/I_{0,p1}$ are equal to one, then V_{HL} would be determined only by the slope factors and the supply voltage. The proposed model is simple, and it does not include the influence of the second inverter, composed of M_3 and M_4, on the high-to-low transition voltage. The derivation of the low-to-high transition voltage (V_{LH}) is complementary, due to the symmetrical configuration of the transistors. Considering Fig. 2(b), when V_{in} is high, V_{out} is low. This results in M_4 off and M_3 on. As for V_{HL}, we can obtain an expression for V_{LH} by initially imposing that:

$$I_{0,p1} \cdot e^{\frac{V_{dd} - V_{LH} - n_p \cdot (V_{dd} - V_{m,p})}{n_p \cdot \phi}} = I_{0,n2} \cdot e^{\frac{V_{LH}}{n_n \cdot \phi}}. \quad (9)$$

Next $V_{m,p}$ is determined, by equating the currents in M_1 and M_5:

$$I_{0,p1} \cdot e^{\frac{V_{dd}-V_{LH}-n_p\cdot(V_{dd}-V_{m,p})}{n_p\cdot\phi}} = I_{0,p5} \cdot e^{\frac{V_{dd}-V_{m,p}}{n_p\cdot\phi}}, \quad (10)$$

$$V_{m,p} = \frac{V_{LH} + n_p \cdot \left[V_{dd} + \phi \cdot log\left(\frac{I_{0,p5}}{I_{0,p1}}\right)\right]}{1+n_p}. \quad (11)$$

So we substitute (11) in (9), and finally by solving for V_{LH} the expression in (12) is obtained.

$$V_{LH} = \frac{n_n \cdot \left\{V_{dd} - n_p \cdot \phi \cdot \left[n_p \cdot log\left(\frac{I_{0,n2}}{I_{0,p5}}\right) + log\left(\frac{I_{0,n2}}{I_{0,p1}}\right)\right]\right\}}{n_p^2 + n_p + n_n} \quad (12)$$

As for V_{HL}, V_{LH} is linearly dependent on the supply voltage and the thermal voltage. The dependence on the transistors dimensions is logarithmic. V_{HL} depends on M_1, M_2 and M_6. Instead V_{LH} depends on M_1, M_2 and M_5. Designers can use the derived analytical expressions to optimize the design of the Schmitt trigger circuit under analysis. For instance, to make the low-to-high transitition voltage more insensitive to temperature variations, the terms inside the square bracket in (12) should be minimized. This can be done by increasing the size of M_5 and M_1. Instead, for V_{HL} the dependence on the temperature can be minimized by increasing the size of M_1.

III. Model Validation

To validate the proposed model, simulations in AMS 0.35µm CMOS process have been performed. The threshold voltage of the NMOS transistor ($V_{th,n}$) is $515.8mV$, while $V_{th,p} = -731.3mV$. The slope factors are $n_n = 1.25$ and $n_p = 1.3$. The transconductance parameters ($\beta_{n(p)} = \mu_{n(p)} \cdot C_{ox} \cdot W/L$) are $|\beta_{1,5}| = 908\mu A/V^2$ and $\beta_{2,6} = 160\mu A/V^2$. The PMOS transistors are sized 18/1, while the NMOS transistors 1/1. We have chosen these dimensions because this design provides the required hysteresis voltage for further applications. In order to characterize the derived model, we extracted the transition voltages for different supply voltages. The simulated V_{HL} as a function of the supply voltage is shown Fig. 3(a). V_{dd} ranges from $0.5V$ to $0.6V$, therefore all the modeled transistors are in weak inversion since the threshold voltage of the PMOS is greater, in absolute value, than 700mV and the NMOS threshold voltage is approximately 516mV. One can argue that for $V_{dd} > 0.516mV$ the transistor M_2 is not weak inversion. But as can be observed in Fig. 3(b), the resulting voltage at the source of M_2 (i.e. $V_{m,n}$) is greater than $3\cdot\phi \approx 78mV$ at the initial circuit state (i.e. $V_{in} = 0V$). Regarding M_4, it should not have influence on the transition voltage, under the considered assumptions during the model derivation. As can be observed in Fig. 3(a), the model resembles the circuit behavior, and the transition voltage is linearly related to the supply voltage. However an offset can be observed. To quantify the error between the modeled and simulated transition voltages, we define the absolute and relative errors:

$$AE_{HL(LH)} = \left|V_{HL(LH)} - V_{HL(LH),sim}\right|, \quad (13)$$

$$RE_{HL(LH)} = \frac{AE_{HL(LH)}}{V_{HL(LH),sim}} \cdot 100\%. \quad (14)$$

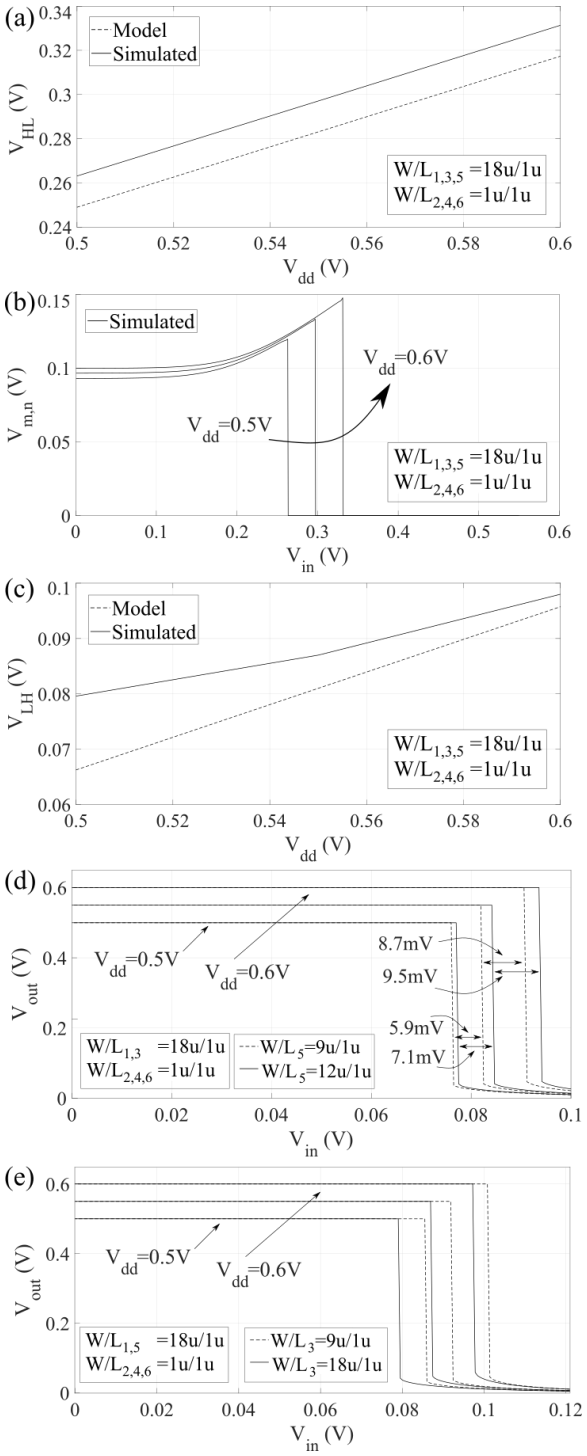

Fig. 3. Modeled and simulated (a) V_{HL} vs V_{dd}. (b) Simulated $V_{m,n}$ vs V_{in} for different V_{dd}. (c) Modeled and simulated V_{LH} vs V_{dd}. (d) Simulated V_{out} vs V_{in} for different V_{dd} and widths of M_5. (e) Simulated V_{out} vs V_{in} for different V_{dd} and widths of M_3.

For V_{HL}, we have that AE_{HL} = $13.9mV$ and RE_{HL} = 7%. Regarding V_{LH}, the simulated and modeled transition voltages as a function of V_{dd} are shown in Fig.3(c). At $V_{dd} = 0.5V$ we have the maximum errors, i.e. AE_{LH} = $13mV$ and RE_{LH} = 17%. As can be observed, for V_{dd} ranging from $0.55V$ to $0.6V$, both

curves are linear, but in the range $[0.5V-0.55V]$ the simulated curve becomes less linear. This phenomenon has been initially attributed to transistor M_5, as can be observed in Fig.3(d), where the simulated V_{out} vs V_{in} is plotted for different V_{dd} and widths of M_5. The solid line refers to the case in which M_5 has a width of $12u$, while the dashed one to the case in which the width is $9u$. As can be observed, the difference between the curves for $V_{dd} = 0.5V$ and $V_{dd} = 0.55V$ is $7.1mV$, when the width is $12u$. When the width is $9u$ this step reduces to $5.9mV$. When the width is $18u$, the step is $7.4m$V. Instead, the distance between the curves for $V_{dd} = 0.55V$ and $V_{dd} = 0.6V$ is $9.5mV$ when M_5 has a width of $12u$, $8.7mV$ when M_5 has a width of $9u$, and $11mV$ when the width is $18u$. This clearly implies that M_5 has an influence on the transition voltage which is not included in the simple derived model. Moreover, also the inverter composed of M_3 and M_4 has an influence on the characteristics. In Fig.3(e), we can observe how a variation in the width of M_3 causes a variation in the output voltage. It is therefore clear that the assumption that M_3 has no influence on the transition voltage is wrong. Unfortunately, the model at this stage does not include the influence of M_3 on the transition voltages. This represents the main limitation of the simple proposed model. An ASIC in AMS 0.35µm CMOS process has been fabricated through EUROPRACTICE MPW for model validation. A photograph of the circuit and the associated layout are shown in Fig. 4. The circuit occupies an area of $49\mu m \times 25\mu m$. We tested the Schmitt Trigger circuit by applying a $1Hz$ triangular wave at the input, considering $V_{dd} = 0.6V$. For this supply voltage, the analytical $V_{HL,model}$ is $317mV$, while $V_{LH,model} = 96mV$. Instead the measured values are $V_{HL,meas} = 329mV$ and $V_{LH,meas} = 131mV$. Therefore the errors between the modeled and measured transition voltages are $AE_{HL,meas} = 12mV$ and $AE_{LH,meas} = 35mV$. The larger errors in the measured transition voltages are mainly attributed to parasitic effects.

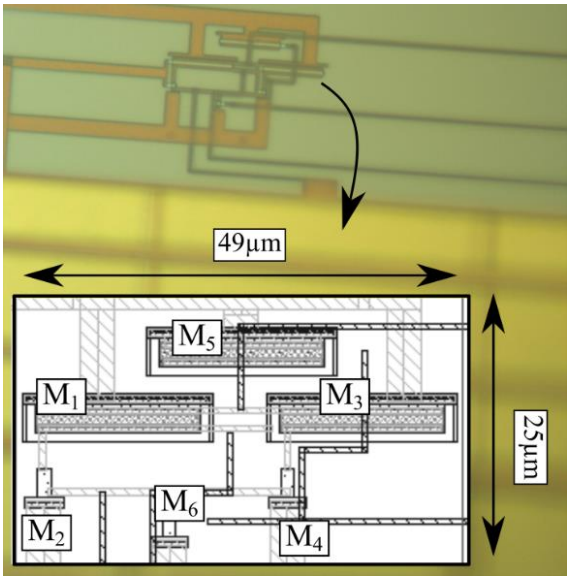

Fig. 4. Photograph of the fabricated circuit in AMS 0.35µm CMOS process (EUROPRACTICE MPW) and associated layout.

IV. Conclusions

In this article we analyzed the subthreshold characteristics of an inverting CMOS Schmitt Trigger circuit. We derived simple equations for the high-to-low and low-to-high transition voltages. The derived expressions are linearly dependent on the supply voltage and the thermal voltage, and logarithmically dependent on the transistors dimensions. The model allows designers to have a clear understanding of the influence of the involved parameters. For instance it allows to optimize the design of the Schmitt trigger circuit against power supply and temperature variations. We performed simulations in AMS 0.35µm CMOS process to verify the proposed analytical model. The maximum error between the analytical and simulated transition points is smaller than 14mV. An ASIC in AMS 0.35µm CMOS process has been fabricated to experimentally validate the derived expressions. The maximum error between the analytical and measured transition points is below 36mV. Future work will focus on model improvement.

Acknowledgment

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References

[1] J. Manyika, M. Chui, P. Bisson, J. Woetzel, R. Dobbs, J. Bughin, and D. Aharon, The Internet of Things: Mapping the value beyond the hype. McKinsey Global Institute New York, NY, USA, 2015, vol. 24.

[2] F. Engmann, F. A. Katsriku, J.-D. Abdulai, K. S. Adu-Manu, and F. K. Banaseka, "Prolonging the lifetime of wireless sensor networks: a review of current techniques," Wireless Communications and Mobile Computing, vol. 2018, 2018.

[3] H. Yetgin, K. T. K. Cheung, M. El-Hajjar, and L. H. Hanzo, "A Survey of Network Lifetime Maximization Techniques in Wireless Sensor Networks," IEEE Communications Surveys Tutorials, vol. 19, no. 2, pp. 828–854, 2017.

[4] G. Anastasi, M. Conti, M. Di Francesco, and A. Passarella, "Energy conservation in wireless sensor networks: A survey," Ad hoc networks, vol. 7, no. 3, pp. 537–568, 2009.

[5] R. Gonzalez, B. M. Gordon, and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," IEEE Journal of Solid-State Circuits, vol. 32, no. 8, pp. 1210–1216, 1997.

[6] C. C. Enz and E. A. Vittoz, "CMOS low-power analog circuit design," in Emerging Technologies: Designing Low Power Digital Systems. IEEE, 1996, pp. 79–133.

[7] M. R. Elmezayen, W. Hu, A. M. Maghraby, I. T. Abougindia, and S. U. Ay, "Accurate Analysis and Design of Integrated Single Input Schmitt Trigger Circuits," Journal of Low Power Electronics and Applications, vol. 10, no. 3, p. 21, 2020.

[8] L. A. Pasini Melek, A. L. da Silva, M. C. Schneider, and C. GalupMontoro, "Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 4, pp. 869–878, 2017.

[9] T. D. Fernandes, C. Galup-Montoro, and M. C. Schneider, "Analysis and Design of the Three-Inverter Schmitt Trigger for Supply Voltages Down to 50 mV," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 7, pp. 2302–2306, 2021.

[10] L. A. Pasini Melek, M. C. Schneider, and C. Galup-Montoro, "Operation of the Classical CMOS Schmitt Trigger As an Ultra-Low-Voltage Amplifier," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 9, pp. 1239–1243, 2018.

[11] S. Radfar, A. Nejati, Y. Bastan, P. Amiri, M. H. Maghami, M. Nasrollahpour, and S. Hamedi-Hagh, "A Sub-Threshold Differential CMOS Schmitt Trigger with Adjustable Hysteresis Based on Body Bias Technique," Electronics, vol. 9, no. 5, p. 806, 2020.

[12] A. Nejati, S. Radfar, P. Amiri, and M. H. Maghami, “A bulk-driven differential CMOS schmitt trigger with adjustable hysteresis for ultralow-voltage operation,” Microelectronics Journal, vol. 114, p. 105129, 2021.

[13] Y. Bastan, A. Nejati, S. Radfar, P. Amiri, M. Nasrollahpour, and S. Hamedi-Hagh, “An Ultra-Low-Voltage Sub-Threshold Pseudo Differential CMOS Schmitt Trigger,” in 2018 31st IEEE International System-on-Chip Conference (SOCC), 2018, pp. 1–5.

[14] A. Nejati, Y. Bastan, and P. Amiri, “0.4 V ultra-low voltage differential CMOS Schmitt trigger,” in 2017 Iranian conference on electrical engineering (ICEE). IEEE, 2017, pp. 532–536.

[15] S. Al-Sarawi, “Low power Schmitt trigger circuit,” Electronics letters, vol. 38, no. 18, pp. 1009–1010, 2002.

[16] C. C. Enz, F. Krummenacher, and E. A. Vittoz, “An analytical MOS transistor model valid in all regions of operation and dedicated to low voltage and low-current applications,” Analog integrated circuits and signal processing, vol. 8, no. 1, pp. 83–114, 1995.

[17] Y. Zhou, J. Mercier, and F. Yuan, “A comparative study of injection locked frequency divider using harmonic mixer in weak and strong inversion,” in 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS). IEEE, 2018, pp. 97–100.

C.2 Analysis of a Low Power Inverting CMOS Schmitt Trigger Operating in Weak Inversion

A. Nowbahari, L. Marchetti and M. Azadmehr, 'Analysis of a Low Power Inverting CMOS Schmitt Trigger Operating in Weak Inversion,' *International Journal of Electrical and Electronic Engineering & Telecommunications*, vol. 11, no. 6, pp. 392–397, 2022. DOI: 10.18178/ijeetc.11.6.392-397. [Online]. Available: http://www.ijeetc.com/uploadfile/2022/1014/20221014033458167.pdf

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This journal article is an extended version, on invitation, of the conference paper presented at the 2022 11th International Conference on Communications, Circuits and Systems [6] (Appendix C.1).

Analysis of a Low Power Inverting CMOS Schmitt Trigger Operating in Weak Inversion

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***Abstract*—This article analyzes the operation of a low power inverting CMOS Schmitt trigger in weak inversion. The analysis is based on an earlier proposed analytical model, which relates the hysteresis voltages to the transistors' dimensions, the supply voltage, and the temperature. The maximum error between the analytical and simulated transition voltages is below 10%, relative to the supply voltage. By optimizing the device sizes, the error reduces to 4%. The operation of the Schmitt trigger in weak inversion is also experimentally validated through an ASIC fabricated in AMS 0.35µm CMOS process. The maximum error between the modeled and measured transition voltages is below 7%. Furthermore, the power consumption as a function of the supply voltage is analyzed. Overall, the proposed model may be used to optimize the operation of the analyzed Schmitt trigger circuit for low power operation.**

***Index Terms*—CMOS, hysteresis, low voltage, low power, Schmitt trigger, subthreshold, weak inversion**

I. Introduction

Supply voltage scaling represents one of the most effective techniques for reducing the power consumption of electronic circuits [1]. When the supply voltage is reduced to values below the threshold voltage of the transistors, the system operates in the subthreshold region. At device level, subthreshold operation means that transistors are biased in weak inversion. From an analytical point of view, subthreshold operation implies that alternative models have to be used to correctly describe and understand the behavior of the circuits [2]. A widely implemented circuit, both in digital and analog systems, is the Schmitt Trigger (ST) one. The symbol of a single input inverting voltage mode Schmitt trigger is shown in Fig. 1 (a). The characteristic of Schmitt trigger circuits is typically hysteretic, as can be shown in Fig. 1 (b). STs are implemented in many different circuits, such as comparators, oscillators, converters, and others [3]. Recently researchers have also presented models of Schmitt trigger circuits in weak inversion [4]–[10] for low voltage and low power applications. By developing analytical model for ST circuits, designers can have a physical insight into the circuit behavior, thus allowing optimization of the circuit performance. In this article we analyze the subthreshold operation of the inverting CMOS Schmitt trigger circuit proposed by Al-Sarawi, shown in Fig. 1 (c) [11]. The bulk terminals of the PMOS transistors are connected to the supply voltage, while those of the NMOS transistors to ground. They are not shown for simplicity. In our previous work [12], we derived a simple analytical model for the high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages, which define the hysteresis width, as shown in Fig. 1 (b). This article is an extended version of the work presented in [12], and provides a more accurate discussion about the proposed analytical model. In particular, the model assumptions are investigated, by analyzing two different design cases, and by validating simplified equivalent circuits. Furthermore, we provide an analysis of the circuit power consumption. The article is organized as it follows. In Section II we report the proposed analytical model, which is then validated with simulations and measurements in Section III. In Section IV the circuit power consumption is analyzed, while the conclusions are in Section V.

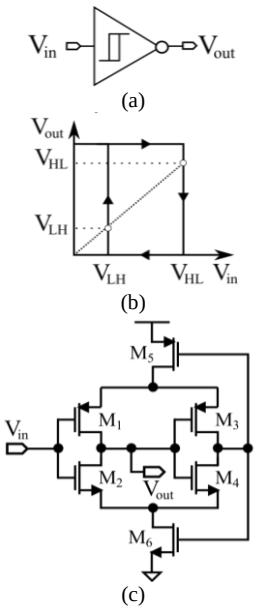

Fig. 1. Schmitt trigger: (a) Single input inverting voltage mode symbol, (b) typical V_{out} vs V_{in} of (a), and (c) Schmitt trigger circuit under analysis. The bulk terminals are not shown for simplicity.

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II. Analytical Model

The MOSFET drain current in weak inversion can be modeled using the Enz-Krummenacher-Vittoz (EKV) model in [13] expressed as

$$I_{d,n(p)} = I_{0,n(p)} e^{\frac{V_{\mathrm{GB(BG)}}}{n_{n(p)}\phi}} \left(e^{-\frac{V_{\mathrm{SB(BS)}}}{\phi}} - e^{-\frac{V_{\mathrm{DB(BD)}}}{\phi}} \right) \quad (1)$$

$$I_{0,n(p)} = 2n_{n(p)}\mu_{n(p)}C_{\mathrm{ox}}\frac{W}{L}\phi^2 e^{\frac{-\left|V_{\mathrm{th},n(p)}\right|}{n_{n(p)}}} \quad (2)$$

- G → gate, D → drain, S → source, B → bulk;
- $n_{n(p)}$→ is the NMOS (PMOS) slope factor;
- ϕ→ thermal voltage;
- $\mu_{n(p)}$→ NMOS (PMOS) carrier mobility;
- C_{ox}→ oxide capacitance;
- W/L→ MOSFET width to length ratio;
- $V_{\mathrm{th},n(p)}$→ NMOS (PMOS) threshold voltage.

In saturation ($|V_{\mathrm{DS}}| \geq 3\phi$ [14]) expression (1) can be simplified to

$$I_{d,n(p)} \approx I_{0,n(p)} e^{\frac{V_{\mathrm{GB(BG)}} - n_{n(p)}V_{\mathrm{SB(BS)}}}{n_{n(p)}\phi}}. \quad (3)$$

Assuming the bulk-source voltage is equal to zero, the expression (3) can be further simplified as

$$I_{d,n(p)} \approx I_{0,n(p)} e^{\frac{V_{\mathrm{GB(BG)}}}{n_{n(p)}\phi}}. \quad (4)$$

Fig. 2 shows the circuit behavior for both threshold voltages of the Schmitt trigger, i.e., low-to-high voltage (V_{LH}), and high-to-low voltage (V_{HL}). The high-to-low voltage (V_{HL}), i.e. when the output voltage (V_{out}) goes from high to low is shown in Fig. 2 (a). In this state V_{in} is low initially and V_{out} is high since the circuit is an inverting ST. In this case, M_1 is on, M_3 is off, and M_5 pulls $V_{m,p}$ to the supply voltage (V_{dd}) since M_4 is on as well. Therefore M_5 is excluded from the figure and M_6 becomes diode-connected. V_{HL} can be determined by finding the switching voltage of the inverter composed of M_1 and M_2, by considering the finite voltage $V_{m,n}$ across M_6 [3]. Assuming that all MOSFETs are in saturation, then M_1 and M_2 are related by:

$$I_{0,p_1} e^{\frac{V_{\mathrm{dd}} - V_{\mathrm{HL}}}{n_p \cdot \phi}} = I_{0,n2} e^{\frac{V_{\mathrm{HL}} - n_n V_{m,n}}{n_n \phi}}. \quad (5)$$

The unknown variable in (5) is the voltage across M_6, i.e. $V_{m,n}$. To determine $V_{m,n}$, we can equate the current in M_2 and M_6:

$$I_{0,n6} e^{\frac{V_{m,n}}{n_n \phi}} = I_{0,n2} e^{\frac{V_{\mathrm{HL}} - n_n V_{m,n}}{n_n \phi}} \quad (6)$$

$$V_{m,n} = \frac{V_{\mathrm{HL}} + n_n \phi \log\left(\frac{I_{0,n2}}{I_{0,n6}}\right)}{1 + n_n}. \quad (7)$$

Next (7) is substituted into (5), and solved for V_{HL} as

$$V_{\mathrm{HL}} = \frac{n_n \left\{ V_{\mathrm{dd}}(1+n_n) - n_p\phi \left[\log\left(\frac{I_{0,n_2}}{I_{0,p_1}}\right) + n_n \log\left(\frac{I_{0,n_6}}{I_{0,p_1}}\right) \right] \right\}}{n_n^2 + n_n + n_p}. \quad (8)$$

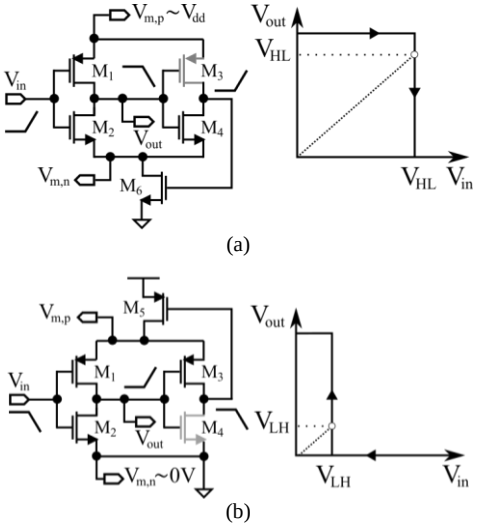

Fig. 2. ST circuits for (a) high-to-low (V_{HL}) and (b) low-to-high (V_{LH}) transition voltages derivation.

From (8) we can read that V_{HL} is linearly dependent on the supply voltage, the thermal voltage, and the temperature. On the other hand, the dependence on the transistors' dimensions is logarithmic. The derived model is simple, and it is based on two assumptions, that M_3 and M_4 do not influence V_{HL} and that $V_{m,p}$ is pulled up to V_{dd}, i.e. M_5 does not influence V_{HL}. As can be noted in (8), if the ratios inside the logarithms are equal to one, then V_{HL} would be dependent only on the slope factors and the supply voltage. In practice, matching these transistors is not trivial, due to process variations and typically different slope factors. The derivation of the low-to-high transition voltage (V_{LH}) is complementary since the transistors are symmetrically arranged. Referring to Fig. 2 (b), when V_{in} is high, V_{out} is low. Therefore, it results that M_4 is off and M_3 is on. M_6 is on which pulles $V_{m,n}$ to gnd, i.e., M_6 does not influence the threshold voltage V_{LH}. As for V_{HL}, we can determine an expression for V_{LH} by initially imposing that:

$$I_{0,p_1} e^{\frac{V_{\mathrm{dd}} - V_{\mathrm{LH}} - n_p(V_{\mathrm{dd}} - V_{m,p})}{n_p \phi}} = I_{0,n_2} e^{\frac{V_{\mathrm{LH}}}{n_n \phi}}. \quad (9)$$

Next we equate the currents in M_1 and M_5, to determine $V_{m,p}$:

$$I_{0,p_1} e^{\frac{V_{\mathrm{dd}} - V_{\mathrm{LH}} - n_p(V_{\mathrm{dd}} - V_{m,p})}{n_p \phi}} = I_{0,p_5} e^{\frac{V_{\mathrm{dd}} - V_{m,p}}{n_p \phi}} \quad (10)$$

$$V_{m,p} = \frac{V_{\mathrm{LH}} + n_p \left[V_{dd} + \phi \log\left(\frac{I_{0,p_5}}{I_{0,p_1}}\right) \right]}{1 + n_p}. \quad (11)$$

Substituting (11) in (9), and solving for V_{LH} the expression in (12) is finally obtained as

$$V_{\mathrm{LH}}=\frac{n_n\left\{V_{\mathrm{dd}}-n_p\phi\left[n_p\log\left(\frac{I_{0,n_2}}{I_{0,p_5}}\right)+\log\left(\frac{I_{0,n_2}}{I_{0,p_1}}\right)\right]\right\}}{n_p^2+n_p+n_n}. \quad (12)$$

As for V_{HL}, V_{LH} is linearly dependent on the supply voltage, the thermal voltage, and on the temperature and logarithmic on the transistors' dimensions. V_{HL} depends on M_1, M_2, and M_6. Instead V_{LH} depends on M_1, M_2, and M_5. Therefore the proposed analytical model provides physical insight into the circuit behavior, since it relates the hysteresis transition voltages (Thresholds) to the power supply and the temperature. From a design point of view, the derived expressions allow designers to optimize the ST circuit under analysis. For instance, by minimizing the terms inside the square brackets in (8) and (12), the circuit can be made more insensitive to temperature variations. Clearly, the model is valid under the assumptions that the second inverter does not influence the transition points and that the resistances of M_5 and M_6 are negligible during the high-to-low and low-to-high transitions, respectively. As will be verified in the next section, these assumptions are validated when the transistors are wide with respect to the channel length. This is due to the fact the wide transistors present lower ON resistance.

III. Model Validation

To verify the derived expressions, simulations have been performed. First we show a worst-case design (Design 1), i.e., we implement a ST with not optimized transistors dimensions. Next we provide an optimized design (Design 2), which respects the model assumptions. To quantify the error between the analytical and simulated voltages, we introduce the absolute and relative errors as

$$\mathrm{AE}_{\mathrm{HL(LH)}}=\left|V_{\mathrm{HL(LH)}}-V_{\mathrm{HL(LH),sim}}\right| \quad (13)$$

$$\mathrm{RE}_{\mathrm{HL(LH)}}=\frac{\mathrm{AE}_{\mathrm{HL(LH)}}}{V_{\mathrm{HL(LH),sim}}}\times 100\%. \quad (14)$$

The relative errors are computed against $V_{\mathrm{HL(LH),sim}}$, i.e. the simulated transition voltages are considered as reference values.

A. Design 1

The simulation parameters used for Design 1 are shown in Table I, second column. The slope factors of transistors n_n and n_p are 1.25 and 1.3, respectively. The transconductance is defined as $\beta_{n(p)}=\mu_{n(p)}C_{\mathrm{ox}}W/L$. V_{HL} is extracted for supply voltages V_{dd} ranging from 0.5V to 0.6V, therefore all the modeled transistors (M_1, M_2, and M_6) are in weak inversion. For $V_{\mathrm{dd}}>V_{\mathrm{th,2}}$, the transistor M_2 is still in weak inversion because the resulting voltage at its source ($V_{m,n}$) is greater than $3\phi \approx 78$mV at the initial circuit state (when V_{in}=0V). This has been verified through simulations, as can be seen in Fig. 3 (b). Regarding M_4, it should not influence V_{HL}, according to the model assumptions. The analytical and simulated V_{HL} as a function of V_{dd} are shown in Fig. 3 (a). The model resembles the simulated behavior, and V_{HL} is linearly related to the supply voltage, as expected from (8). The maximum absolute error for V_{HL} in Design 1 is $\mathrm{AE}_{\mathrm{HL},1}$=19mV, while the relative one is $\mathrm{RE}_{\mathrm{HL},1}$=8%, when V_{dd}=0.5V. The analytical and simulated V_{LH} as a function of V_{dd} are shown in Fig. 3 (c). In this case both offset and gain errors are present. The maximum absolute error is $\mathrm{AE}_{\mathrm{LH},1}$=48mV, while the relative one is $\mathrm{RE}_{\mathrm{LH},1}$=66%. The error is attributed to M_3, M_4, M_5 and M_6. As previously explained, the model assumes that M_3 and M_4 act as ideal switches, forcing M_5 and M_6 in diode-connected configuration.

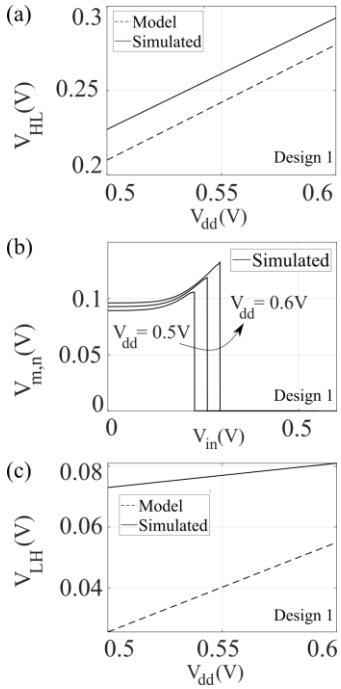

Fig. 3. Design 1: (a) modeled and simulated V_{HL} vs V_{dd}, (b) simulated $V_{m,n}$ vs V_{in} for different V_{dd}, and (c) modeled and simulated V_{LH} vs V_{dd}.

TABLE I: Simulation Parameters

Parameter	Design 1	Design 2
	Value	Value
L	0.5μm	0.5μm
$W_{2,4,6}$	1μm	20μm
$W_{1,3,5}$	2μm	40μm
$V_{\mathrm{th,2}}$	559mV	574.2mV
$V_{\mathrm{th,6}}$	533.4mV	563.7mV
$V_{\mathrm{th,1,5}}$	−744.1mV	−734.5mV
$\lvert\beta_{1,5}\rvert$	174.2μA/V^2	1.795mA/V^2
$\beta_{2,6}$	303μA/V^2	6.834mA/V^2

Furthermore, it assumes that the ON resistances across M_5 and M_6 are negligible as shown in Fig. 2.

B. Design 2

In Design 2 we increase the width of the transistors, to validate the model assumptions. The widths of M_1, M_3, and M_5 are set to 40μm, while those of M_2, M_4, and M_6 to 20μm. The simulation parameters used for Design 2 are shown in Table I, third column. The analytical and simulated V_{HL} and V_{LH} as a function of V_{dd} are shown in Fig. 4 (a) and Fig. 4 (b). The maximum absolute error for

V_{HL} is $AE_{HL,2}$=20mV, while the relative one is $RE_{HL,2}$=8%, when V_{dd}=0.5V. The maximum absolute error for V_{LH} in is $AE_{LH,2}$=20mV, while the relative one is $RE_{LH,2}$=33%. $RE_{LH,2}$ is higher than $RE_{HL,2}$ because $AE_{LH,2}$ is divided by a smaller number since V_{LH} occurs for lower voltages, with respect to V_{HL}. On the basis of this analysis it can be concluded that the model is more accurate when the transistors in the ST circuit are large as compared to the minimum channel length. In Design 2 we enlarged the widths of all transistors, although the model only requires M_3, M_4, M_5 and M_6 to be enlarged. We also considered the case in which M_3, M_4, M_5 and M_6 are large, while M_1 and M_2 are small. What we observed is that if the transistors of the first inverter are too small as compared to the transistors in the feedback, the error does not improve as in the case in which all transistors are enlarged. Nevertheless, the error relative to V_{dd}, i.e. $AE_{HL(LH)}/V_{dd}$, is always below 10% for the designed circuits, implying that the worst case analysis is relatively the worst.

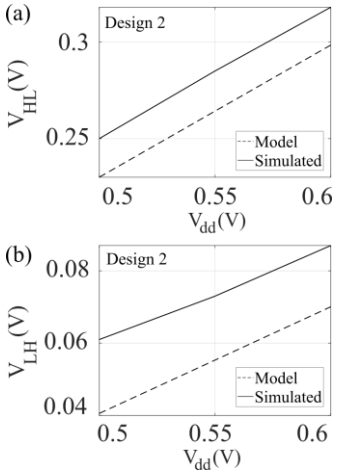

Fig. 4. Design 2: modeled and simulated (a) V_{HL} vs V_{dd} and (b) V_{LH} vs V_{dd}.

C. Simplified Equivalent Circuits

To further analyze the model assumptions, the simplified equivalent circuits in Fig. 5 (a) and Fig. 5 (b) are simulated. The circuits in Fig. 5 (a) and Fig. 5 (b) are the simplified equivalent circuits associated to those Fig. 2 (a) and Fig. 2 (b), respectively. These circuits approximate the circuit behavior at the initial state, i.e. V_{in}=0V for V_{HL} and V_{in}=V_{dd} for V_{LH}. The transistors are sized as in Design 2. In Fig. 5 (c) the simulated V_{out} vs V_{in} of the full circuit for different V_{dd} are shown. As can be observed, the output swings between the supply rails. In Fig. 5 (d) the simulated V_{out} vs V_{in} of the simplified equivalent circuit in Fig. 5 (a) is shown. The output does not reach 0V since in the simplified circuit M_6 is always diode-connected. Nevertheless, V_{HL} is almost the same for both full and simplified circuits since the maximum difference is below 2mV. In Fig. 5 (e) the simulated V_{out} vs V_{in} of the simplified equivalent circuit in Fig. 5 (b) is shown. As can be observed, the output does not reach V_{dd}. This is attributed to M_5, which is always on. Nevertheless, V_{LH} is almost the same for both full and simplified circuits since the maximum difference is below 2mV, as for V_{HL}. On the basis of these results it can be concluded that the simplified equivalent circuits correctly describes the ST circuit under analysis, when the transistors are correctly sized.

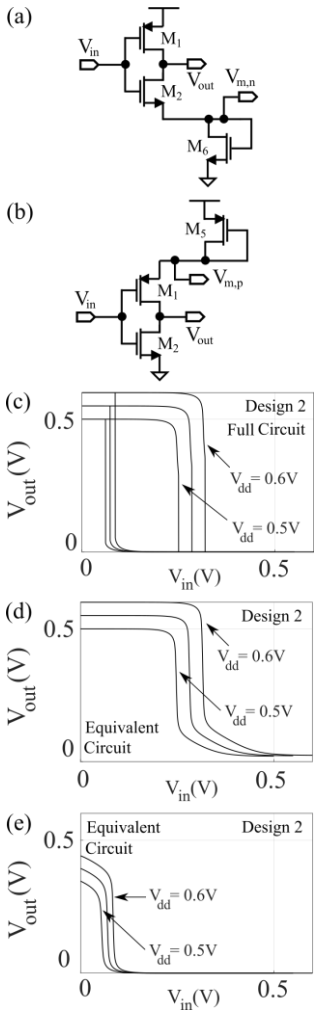

Fig. 5. Simplified equivalent circuits for (a) V_{HL} and (b) V_{LH} analysis. Design 2: (c) simulated V_{out} vs V_{in} for different V_{dd} when considering the full circuit; simulated V_{out} vs V_{in} for different V_{dd} when considering the simplified equivalent circuits for (d) V_{HL} and (e) V_{LH}.

D. Experimental Validation

A prototype realized in AMS 0.35µm CMOS process has been tested. The fabricated circuit and the layout are shown in Fig. 6 (a). The area occupied by the circuit is 49µm×25µm. The channel length is 1µm, while the NMOS and PMOS transistors are sized 1/1 and 18/1, respectively. This design provides the desired hysteresis for further applications. The transition voltages have been extracted at V_{dd}=0.6V, by applying a low frequency ($1/f$=5s) triangular wave, as shown in Fig. 6 (b). For this design, the analytical V_{HL} is 317mV, while V_{LH}=96mV. The measured transition voltages are $V_{HL,meas}$=329mV and $V_{LH,meas}$=131mV. Therefore, we have that $AE_{HL,meas}$=12mV and $AE_{LH,meas}$=35mV. The larger errors in the measured transition voltages are mainly attributed to the experimental setup, e.g. parasitic components associated to the ASIC pads.

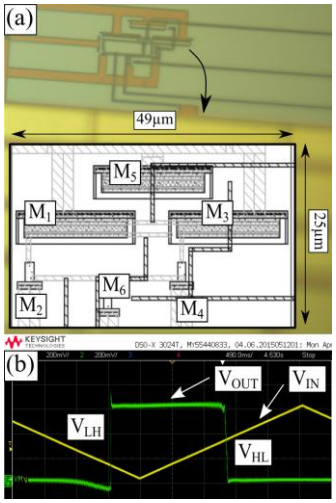

Fig. 6. Fabricated circuit (AMS 0.35 µm CMOS Process): (a) Photograph and layout of the ST circuit, and (b) measured V_{out} vs V_{in}.

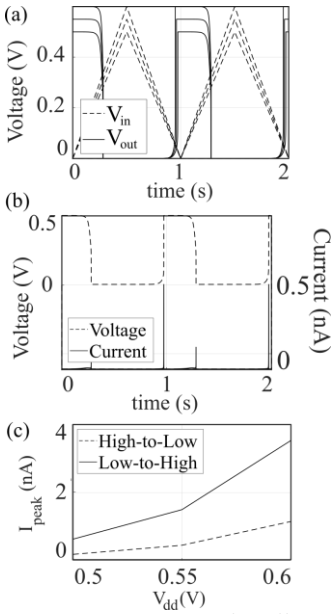

Fig. 7. Simulation results: (a) V_{out} and V_{in} for different V_{dd}, (b) current drawn from V_{dd}, and V_{out} when V_{dd}=0.5V, and (c) maximum peak currents during the high-to-low and low-to-high transitions for different V_{dd}.

IV. Power Consumption

In this section, we analyze the power consumption of the ST circuit. The transistors are sized according to Design 2. We performed a transient analysis by applying a 1Hz triangular wave at the input of the ST circuit loaded by a capacitance of 1pF. In Fig. 7 (a) the output and input voltages are depicted, for different supply voltages. In Fig. 7 (b) the current drawn by the supply voltage is shown for V_{dd}=0.5V. As can be observed, the peaks in the current occur during the high-to-low and low-to-high transitions. This is expected since the power consumption of a ST is mainly due to the switching current. During the high-to-low transition, the peak current has a value of 159pA, while during the low-to-high transition, the peak value is 615pA. The higher power consumption during the low-to-high transition is attributed to transistors M_5, which is in diode-connected configuration during the transition. The maximum peak currents are shown in Fig. 7 (c). As can be observed, the peak currents associated to the low-to-high transition are higher than those associated to the high-to-low one. The peak current can be decreased by reducing the widths of the transistors in the PMOS branch. When the same circuit is driven at 3.3V, which is the nominal voltage of the considered CMOS process, the maximum peak of the current has a value of 1.74mA, which is more than six orders of magnitude larger than the case in which the supply voltage is 0.5V. Therefore, the proposed model allows to optimize the performance of the circuit for low power operation, since the presented analysis shows the contribution of the transistors during the switching phase (Fig. 5 (a) and Fig. 5 (b)).

V. Conclusion

In this article, we analyzed the subthreshold operation of an inverting CMOS Schmitt trigger. We derived analytical expressions of the high-to-low and low-to-high hysteresis transition voltages. The model provides physical insight into the circuit behavior, i.e., the transition voltages are linearly related to the supply voltage and the temperature and logarithmically dependent on the transistors' dimensions. We analyzed the model limitations by investigating different designs. When the widths of the transistors are large as compared to the minimum channel length, the error between the analytical and simulated transition voltages is reduced. When the transistors' dimensions are optimized, the maximum absolute error for both transition voltages is 20mV. Instead, the error relative to the supply voltage is below 10%. The model assumptions have been validated by analyzing simplified equivalent circuits. The error between the full circuit and the simplified ones is below 2mV, when the model assumptions are respected. A prototype in AMS 0.35 µm CMOS process has been fabricated to experimentally validate the derived expressions, providing a maximum error below 36mV. The power consumption of the circuit has been analyzed by performing transient simulations for different supply voltages. When the subthreshold operation is exploited (V_{dd}=0.5V), the performance of the circuit has an improvement of more than six orders of magnitude in the switching current, with respect to the case in which the supply voltage is 3.3V.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

A. Nowbahari derived the analytical model, and performed simulations and measurements; L. Marchetti and M. Azadmehr supervised the work; all authors had approved the final version.

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REFERENCES

[1] R. Gonzalez, B. M. Gordon, and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 8, pp. 1210–1216, 1997.

[2] C. C. Enz and E. A. Vittoz, "CMOS low-power analog circuit design," in *Emerging Technologies: Designing Low Power Digital Systems*, IEEE, 1996, pp. 79–133.

[3] M. R. Elmezayen, W. Hu, A. M. Maghraby, I. T. Abougindia, and S. U. Ay, "Accurate analysis and design of integrated single input schmitt trigger circuits," *Journal of Low Power Electronics and Applications*, vol. 10, no. 3, p. 21, 2020.

[4] L. A. P. Melek, A. L. D. Silva, M. C. Schneider, and C. Galup Montoro, "Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 64, no. 4, pp. 869–878, 2017.

[5] T. D. Fernandes, C. Galup-Montoro, and M. C. Schneider, "Analysis and design of the three-inverter Schmitt trigger for supply voltages down to 50 mV," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2302–2306, 2021.

[6] L. A. P. Melek, M. C. Schneider, and C. Galup-Montoro, "Operation of the classical CMOS Schmitt trigger as an ultra-low-voltage amplifier," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1239–1243, 2018.

[7] S. Radfar, A. Nejati, Y. Bastan, P. Amiri, M. H. Maghami, M. Nasrollahpour, and S. Hamedi-Hagh, "A sub-threshold differential CMOS Schmitt trigger with adjustable hysteresis based on body bias technique," *Electronics*, vol. 9, no. 5, p. 806, 2020.

[8] A. Nejati, S. Radfar, P. Amiri, and M. H. Maghami, "A bulk-driven differential CMOS Schmitt trigger with adjustable hysteresis for ultralow-voltage operation," *Microelectronics Journal*, vol. 114, 2021.

[9] Y. Bastan, A. Nejati, S. Radfar, P. Amiri, M. Nasrollahpour, and S. Hamedi-Hagh, "An ultra-low-voltage sub-threshold pseudo differential CMOS Schmitt trigger," in *Proc. 31st IEEE International System-on-Chip Conference (SOCC)*, 2018, pp. 1–5.

[10] A. Nejati, Y. Bastan, and P. Amiri, "0.4 V ultra-low voltage differential CMOS Schmitt trigger," in *Proc. Iranian Conference on Electrical Engineering (ICEE)*, 2017, pp. 532–536.

[11] S. Al-Sarawi, "Low power Schmitt trigger circuit," *Electronics Letters*, vol. 38, no. 18, pp. 1009–1010, 2002.

[12] A. Nowbahari, L. Marchetti, and M. Azadmehr, "Weak inversion model of an inverting CMOS Schmitt trigger," presented at 11th International Conference on Communications, Circuits and Systems (ICCCAS), Singapore, May 13-15, 2022.

[13] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, 1995.

[14] Y. Zhou, J. Mercier, and F. Yuan, "A comparative study of injection locked frequency divider using harmonic mixer in weak and strong inversion," in *Proc. IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, IEEE, 2018, pp. 97–100.

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C.3 Subthreshold Modeling of a Tunable CMOS Schmitt Trigger

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RESEARCH ARTICLE

Subthreshold Modeling of a Tunable CMOS Schmitt Trigger

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ABSTRACT In this article, the subthreshold characteristics of a tunable single input CMOS Schmitt trigger (ST) are modeled for the first time. The high-to-low and low-to-high hysteresis transition points are analytically determined as a function of the tuning voltages and the transistors' geometrical parameters. The derived expressions allow to design the ST with desired hysteresis width in subthreshold region. Furthermore, the proposed model allows to estimate the minimum supply voltage for which hysteresis occurs. The derived expressions also provide physical insight into the circuit behavior, by predicting the effect of supply voltage and temperature variations on the hysteresis width. The model is validated through simulations, and the maximum error between the analytical and simulated transition points is less than 5%. The model is also experimentally validated with an ASIC fabricated in AMS 0.35μm CMOS process. The maximum error between the analytical and measured transition points is below 6%. The analytical model allows performance optimization in subthreshold region for low power applications.

INDEX TERMS CMOS, hysteresis, low voltage, Schmitt trigger, subthreshold.

I. INTRODUCTION

The first Schmitt trigger (ST) was invented by Otto H. Schmitt in 1938, and it was intended to model the nerve membrane behavior [1], [2]. Although the primary application was in the biomedical field, Schmitt predicted that its circuit could be employed in various applications, such as thermostating, oscillography, and light control. Indeed, today STs are extensively implemented in both analog and digital systems [3]. For instance, they are used in triangular/square-wave generators [4], [5], [6], resistance-to-frequency converters [7], [8], capacitive-to-frequency converters [9], modulators [10], [11], SRAMs and latches [12], [13], [14], and different sensing and measuring applications [15], [16], [17], [18], [19], [20], [21], [22]. STs can work in current or voltage mode and be inverting or non-inverting. They can have single or differential input and have tunable hysteresis [23]. Currently, researchers are focusing on analyzing and modeling the subthreshold operation of STs [24], [25], [26], [27], [28], [29]. This is mainly due to the supply voltage reduction trend, which represents a key design technique in the power consumption optimization of electronic systems [30]. Operation at low voltages results in energy efficiency in battery-powered circuits, where the power consumption limits the system lifetime. In systems powered by energy harvesters, the level of the required supply voltage often determines the startup mechanisms. Lowering power consumption is also particularly advantageous in IoT enabling technologies, such as wireless sensor networks, where thousands of electronic devices are typically employed [31]. Supply voltage scaling is therefore critically important, considering that the number of connected devices is expected to increase to more than 30 billion in 2027 [32]. On the other side, subthreshold operation implies that MOSFETs are biased in weak inversion, which results in more complex analytical models [33]. In 2007, Kulkarni et al. implemented a modified version of the classical 6-transistor CMOS Schmitt trigger in 0.13μm CMOS process to implement an SRAM cell for subthreshold operation [34]. In 2012, Lotze and Manoli analyzed supply voltage reduction

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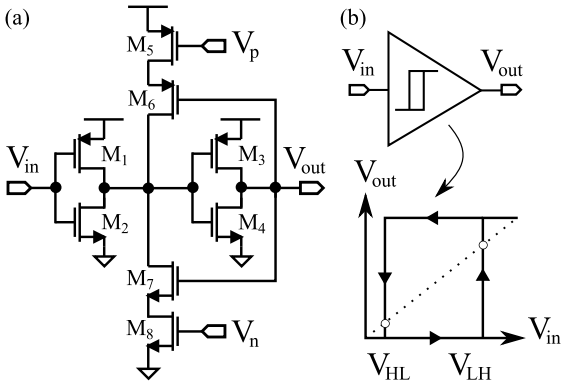

FIGURE 1. (a) Tunable CMOS Schmitt trigger (ST) circuit under analysis [40]. (b) Single input voltage mode ST symbol and characteristics. The bulk terminals are not shown for simplicity.

by considering ST logic, and analyzed the operation of digital circuits with a supply voltage of $62mV$ [35]. In 2017, the same authors proposed an in-depth analysis of ST gates in subthreshold, by considering the optimum transistors sizing [31]. In the same year, Melek et al. determined the DC transfer characteristic of the classical 6-transistor Schmitt trigger (0.18μm CMOS process) in subthreshold [24]. They analytically determined the hysteresis width and the minimum supply voltage ($2ln(2+\sqrt{5})k_BT/q = 75mV$ at room temperature) for which hysteresis occurs. One year later, Melek et al. analyzed the same ST in amplifier mode [26]. They theoretically found a minimum supply voltage of $31.5mV$ (at $300K$) for voltage amplification. In 2018, Bastan et al. proposed a subthreshold pseudo-differential ST in 0.18μm CMOS process, which consumes $150nW$ when operating at $0.4V$ [36]. In 2020, Radfar et al. presented a differential ST circuit (0.18μm CMOS process) with tunable hysteresis based on body biasing [28]. The circuit has a tuning range of approximately $110mV$, and it consumes $1.38\mu W$ with a supply voltage of $0.6V$. One year later, a less power consuming ($120nW$, with supply voltage of $0.4V$) differential ST circuit (0.18μm CMOS process) has been proposed by Nejati et al. [29]. In 2021, Fernandes et al. analyzed the subthreshold operation of a 3-inverter CMOS Schmitt trigger [25]. They analyzed the transition from amplifier mode to hysteresis mode, and they implemented a relaxation oscillator in 0.18μm CMOS process supplied by only $62mV$. In 2022, Sandiri et al. analyzed ST logic gates using Dynamic Threshold MOS (DTMOS) technique [37]. In the same year, we derived in [27], [38] an analytical model for the hysteresis voltage of the low power CMOS ST proposed by Al-Sarawi [39]. In this article, the subthreshold characteristics of the tunable single input CMOS Schmitt trigger proposed by Wang [40] in 1991 are modeled for the first time. The circuit under analysis is shown in Fig. 1(a) and is the first single input tunable CMOS ST modeled in subthreshold. In this article, the expressions for the low-to-high (V_{LH}) and high-to-low (V_{HL}) transition voltages, shown in Fig. 1(b), are analytically determined. These two voltages define the hysteresis width ($V_H = V_{LH} - V_{HL}$). The proposed analytical model allows the design of the ST with desired hysteresis as a function of the transistors' geometrical parameters and tuning voltages. Furthermore, it provides physical insight into circuit behavior by relating the supply voltage and the temperature to the transition voltages. Moreover, the analytical model can be used to estimate the minimum supply voltage for which hysteresis occurs. The derived expressions have been validated through simulations and measurements by prototyping an ASIC in AMS 0.35μm CMOS process. The analytical model is derived in Section II. In Section III the model is validated at simulation level, and the expressions are verified against tuning voltages. The model accuracy is also verified by considering supply voltage, temperature and process variations. The circuit power consumption has been also analyzed. The experimental results are reported in Section IV, while the conclusions are in Section V. Overall, the aim of this paper is to provide a deeper understanding of the subthreshold behavior of the analyzed Schmitt trigger, which is a common block in different analog and digital electronic systems.

II. ANALYTICAL MODEL

The subthreshold drain current expression (EKV [41]) is

$$I_{d,n(p)} = I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}} \cdot \left(e^{-\frac{V_{SB(BS)}}{\phi}} - e^{-\frac{V_{DB(BD)}}{\phi}} \right) \quad (1)$$

where:

$$I_{0,n(p)} = 2 \cdot n_{n(p)} \cdot \mu_{n(p)} \cdot C_{ox} \cdot \frac{W}{L} \cdot \phi^2 \cdot e^{-\frac{|V_{th,n(p)}|}{n_{n(p)} \cdot \Phi}} \quad (2)$$

- B, G, S and D refer to the bulk, gate, source and drain, respectively;
- $n_{n(p)}$ is the NMOS (PMOS) slope factor;
- ϕ is the thermal voltage (kT/q);
- $\mu_{n(p)}$ is the electron (hole) mobility;
- C_{ox} is the oxide capacitance;
- W/L is the transistor width to length ratio;
- $V_{th,n(p)}$ is the NMOS (PMOS) threshold voltage.

Equation (1) can be simplified when transistors are in saturation ($|V_{DS}| \geq 3 \cdot \phi$ [42]) as

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)} - n_{n(p)} \cdot V_{SB(BS)}}{n_{n(p)} \cdot \phi}}. \quad (3)$$

When $V_{SB(BS)} = 0V$, then (3) is further simplified to

$$I_{d,n(p)} \approx I_{0,n(p)} \cdot e^{\frac{V_{GB(BG)}}{n_{n(p)} \cdot \phi}}. \quad (4)$$

In the circuit under analysis, the bulks of all PMOS are connected to V_{dd}, while those of the NMOS are grounded. To simplify further analysis, the hysteresis transition points are assumed to be independent of each other, i.e. the high-to-low transition point (V_{HL}) depends only on the NMOS tuning transistor (M_8), while the low-to-high (V_{LH}) one only on the PMOS one (M_5). This assumption has been verified analytically, and through simulations and measurements. V_{HL} is

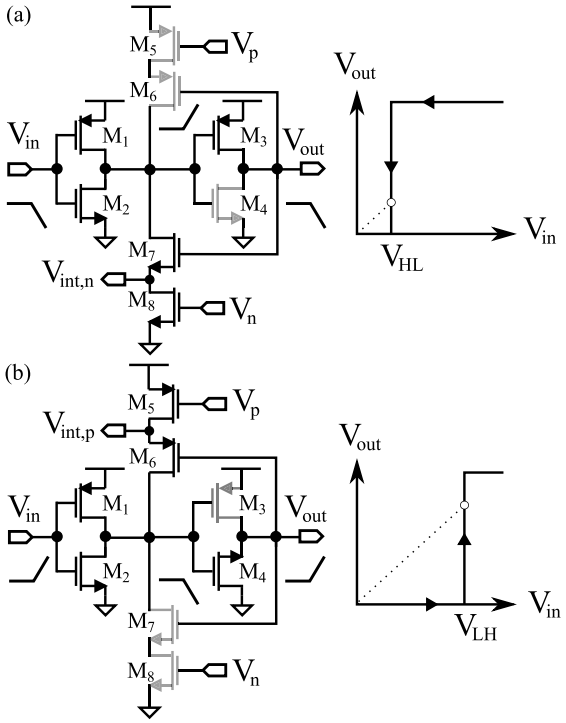

FIGURE 2. ST circuit and characteristics for (a) V_{HL} and (b) V_{LH} analysis.

analyzed first. At initial state when the input (V_{in}) is high, the output (V_{out}) is high as well, due to two cascaded inverters as shown in Fig. 2(a). As a consequence M_4 is off, while $M_{2,3,7}$ are conducting. M_8 conduction depends on the tuning voltage V_n. The input voltage at which the output switches from high-to-low (V_{HL}) can be determined by finding the switching voltage of the inverter composed of $M_{1,2}$, plus the contribution of M_7. Assuming transistors in saturation region during the transition [23], the current through $M_{1,2,7}$ is found using Kirchhoff's current law as

$$I_{0,n2}\cdot e^{\frac{V_{HL}}{n_n\cdot\phi}}+I_{0,n7}\cdot e^{\frac{V_{dd}-n_n\cdot V_{int,n}}{n_n\cdot\phi}}-I_{0,p1}\cdot e^{\frac{V_{dd}-V_{HL}}{n_p\cdot\phi}}=0 \quad (5)$$

where V_{dd} is the supply voltage. To solve (5), the slope factors are approximated as $n_n\approx n_p\approx n$ [43], and $I_{0,p1}$ is redefined as $I'_{0,p1}=I_{0,p1}\cdot exp(V_{dd}/(n\cdot\phi))$. Equation (5) is then divided by $I'_{0,p1}$ and rewritten as

$$\frac{I_{0,n2}}{I'_{0,p1}}\cdot e^{\frac{V_{HL}}{n\cdot\phi}}-e^{-\frac{V_{HL}}{n\cdot\phi}}=-\frac{I_{0,n7}}{I'_{0,p1}}\cdot e^{\frac{V_{dd}-n\cdot V_{int,n}}{n\cdot\phi}}. \quad (6)$$

To solve (6), it is necessary to determine the drain-source voltage across M_8, i.e. $V_{int,n}$. The latter can be obtained by equating the currents in $M_{7,8}$ and solving for $V_{int,n}$:

$$I_{0,n7}\cdot e^{\frac{V_{dd}-n\cdot V_{int,n}}{n\cdot\phi}}=I_{0,n8}\cdot e^{\frac{V_n}{n\cdot\phi}}\cdot\left(1-e^{-\frac{V_{int,n}}{\phi}}\right), \quad (7)$$

$$V_{int,n}=\phi\cdot log\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right). \quad (8)$$

As can be observed in (8), $V_{int,n}$ is linearly dependent on the thermal voltage, and so directly proportional to the temperature. Instead the dependence on the dimensions of $M_{7,8}$ and the tuning voltage V_n is logarithmic. By substituting (8) in (6) the following equation is obtained:

$$\frac{I_{2,n}}{I'_{0,p1}}\cdot e^{\frac{V_{HL}}{n\cdot\phi}}-e^{-\frac{V_{HL}}{n\cdot\phi}}=-\frac{I_{0,n7}}{I'_{0,p1}}\cdot e^{\frac{V_{dd}-n\cdot\phi\cdot log\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right)}{n\cdot\phi}}. \quad (9)$$

Next the following temporary variables are defined:

$$x=\frac{V_{HL}}{n\cdot\phi}, \quad (10)$$

$$a=\frac{I_{0,n2}}{I'_{0,p1}}, \quad (11)$$

$$b=-\frac{I_{0,n7}}{I'_{0,p1}}\cdot e^{\frac{V_{dd}-n\cdot\phi\cdot log\left(1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}\right)}{n\cdot\phi}}=-\frac{I_{0,n7}}{I_{0,p1}}\cdot\frac{1}{1+\frac{I_{0,n7}}{I_{0,n8}}\cdot e^{\frac{V_{dd}-V_n}{n\cdot\phi}}}. \quad (12)$$

Equation (9) can be then rewritten as in (13) and solved for the variable x:

$$a\cdot e^{x}-e^{-x}=b, \quad (13)$$

$$x=-log\left[\frac{1}{2}\cdot\left(\sqrt{4\cdot a+b^2}-b\right)\right] \quad (14)$$

Finally by replacing all the temporary variables in (14), the analytical expression (15), as shown at the bottom of the next page, for V_{HL} is obtained. Regarding the low-to-high transition voltage (V_{LH}), its expression is shown below that of V_{HL} in (16), as shown at the bottom of the next page, and its derivation is complementary. Referring to Fig. 2(b), first $V_{int,p}$ is determined by equating the current in $M_{5,6}$:

$$I_{0,p5}\cdot e^{\frac{-V_p}{n\cdot\phi}}\cdot\left(1-e^{-\frac{V_{dd}-V_{int,p}}{\phi}}\right)=I_{0,p6}\cdot e^{-\frac{V_{dd}-V_{int,p}}{\phi}}, \quad (17)$$

$$V_{int,p}=V_{dd}-\phi\cdot log\left(\frac{I_{0,p6}}{I_{0,p5}}\cdot e^{\frac{V_p}{n\cdot\phi}}+1\right). \quad (18)$$

Next the currents in $M_{1,2,6}$ are equated:

$$I_{0,p1}\cdot e^{\frac{V_{dd}-V_{LH}}{n\cdot\phi}}+I_{0,p6}\cdot e^{\frac{V_{dd}-n\cdot(V_{dd}-V_{int,p})}{n\cdot\phi}}=I_{0,n2}\cdot e^{\frac{V_{LH}}{n\cdot\phi}}. \quad (19)$$

Then, (18) is substituted in (19), and the resulting expression is divided by $I'_{0,p1}$. Next the temporary variables are defined, and the expression in (16) is finally obtained. Both derived expressions, (15) and (16), are linearly dependent on the slope factor and the thermal voltage, and logarithmically dependent on the tuning voltages and the transistors' dimensions. The high-to-low transition point depends on $M_{1,2,7,8}$ and V_n, while the low-to-high one on $M_{1,2,5,6}$ and V_p. Therefore, the analytical model is based on the assumption that the hysteresis transition voltages can be independently adjusted.

III. SIMULATION RESULTS

The proposed analytical model has been validated through simulations in AMS 0.35μm CMOS process. All the simulation results refer to post-layout simulations. The simulated NMOS threshold voltage is $V_{th,n} = 515.8mV$, while the PMOS one is $-731.3mV$. The supply voltage has been initially fixed to $V_{dd} = 0.45V$ to guarantee subthreshold operation. As can be observed in (15) and (16), the M_1 aspect ratio (included in $I_{0,p1}$ as defined in (2)) is at the denominator of the terms inside the logarithms; this implies that a wider PMOS transistor will lead to a higher V_{LH} and V_{HL}. Therefore, the PMOS have been sized 20/1, while the NMOS 1/1, to obtain a larger hysteresis during the measuring phase. When computing $I_{0,n(p)}$, the extracted slope factors $n_{n(p)} = 1.25(1.3)$ are used. Instead, when computing the other terms in (15) and (16), the average value ($n \approx 1.28$) is considered [43]. This last approximation is required in order to solve (5). The NMOS extracted transconductance parameter ($\beta_{n(p)} = \mu_{n(p)} \cdot C_{ox} \cdot W/L$) is $162.26\mu A/V^2$, while the PMOS one is $1.01mA/V^2$. The simulated $V_{LH,HL}$ are extracted by sweeping the input voltage from $0V$ to V_{dd}, and vice versa. In Fig. 3(a), the analytical and simulated V_{HL} as a function of V_n are shown. As can be observed, the analytical model resembles the simulated behavior. The same holds for V_{LH}, which is shown in Fig. 3(b). The transition voltages are evaluated for $V_{n(p)} < 0.3V$, because for higher tuning voltages V_{out} does not toggle (i.e. no high-to-low transition), while V_{LH} is almost constant, for the given design. It has been verified through simulations that the hysteresis transition voltages are strongly independent of each other, i.e. $V_{HL(LH)}$ does not vary with $V_{p(n)}$, as assumed by the proposed analytical model. To evaluate the error between the two curves, the maximum absolute and relative errors between the analytical ($V_{HL(LH)}$) and simulated ($V_{HL(LH),sim}$) transition points are defined:

$$\Delta_{HL(LH)} = |V_{HL(LH)} - V_{HL(LH),sim}|, \tag{20}$$

$$\delta_{HL(LH)} = \left| \frac{V_{HL(LH)} - V_{HL(LH),sim}}{V_{HL(LH),sim}} \right| \cdot 100\%. \tag{21}$$

Δ_{HL} is $2.2mV$ while Δ_{LH} is $2.4mV$. Instead, δ_{HL} is 1.3% while δ_{LH} is 0.8%. Relatively to the supply voltage

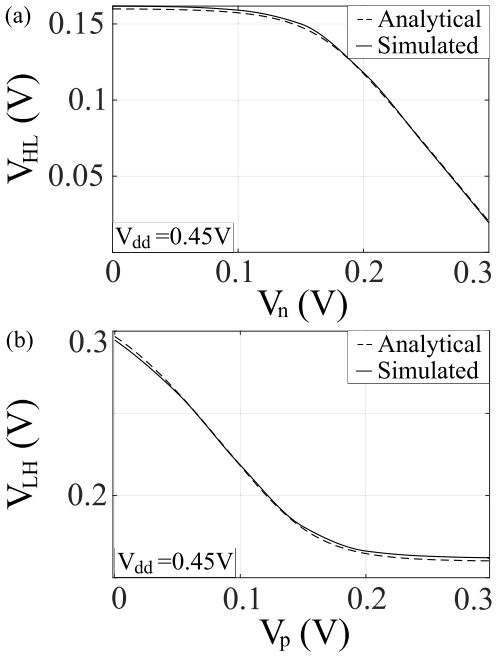

FIGURE 3. Analytical and simulated (a) V_{HL} vs V_n and (b) V_{LH} vs V_p ($V_{dd} = 0.45V$).

($\Delta_{HL(LH)}/V_{dd}$), the maximum errors are below 0.5%. The error between the curves is mainly attributed to the considered approximation $n_n \approx n_p \approx n$. The analytical model has also been verified by considering different designs, shorter channel lengths (e.g. $L = 0.35\mu m$) and narrower transistors, and the maximum error resulted to be in the same order of magnitude of that of the reported design. The derived expressions have been validated by also considering data provided by the datasheet of the AMS 0.35μm CMOS process. Results similar to those obtained with the extracted ones have been obtained, i.e. errors in the same order of magnitude. Although the proposed analytical model has been validated with a relatively old CMOS process technology, the same EKV model has been used to correctly model STs in 0.18μm technology [25], as well as analyze circuits in lower technological nodes (e.g. 90nm and 65nm) [44], [45].

$$V_{HL} = -n \cdot \phi \cdot log\left[\frac{1}{2} \cdot \left(\sqrt{4 \cdot \frac{I_{0,n2}}{I_{0,p1}} \cdot e^{-\frac{V_{dd}}{n \cdot \phi}} + \left(\frac{I_{0,n7}}{I_{0,p1}}\right)^2 \cdot \frac{1}{\left(1 + \frac{I_{0,n7}}{I_{0,n8}} \cdot e^{\frac{V_{dd}-V_n}{n \cdot \phi}}\right)^2}} + \frac{I_{0,n7}}{I_{0,p1}} \cdot \frac{1}{1 + \frac{I_{0,n7}}{I_{0,n8}} \cdot e^{\frac{V_{dd}-V_n}{n \cdot \phi}}}\right)\right] \tag{15}$$

$$V_{LH} = -n \cdot \phi \cdot log\left[\frac{1}{2} \cdot \left(\sqrt{4 \cdot \frac{I_{0,n2}}{I_{0,p1}} \cdot e^{-\frac{V_{dd}}{n \cdot \phi}} + \left(\frac{I_{0,p6}}{I_{0,p1}}\right)^2 \cdot \frac{1}{\left(1 + \frac{I_{0,p6}}{I_{0,p5}} \cdot e^{\frac{V_p}{n \cdot \phi}}\right)^2}} - \frac{I_{0,p6}}{I_{0,p1}} \cdot \frac{1}{1 + \frac{I_{0,p6}}{I_{0,p5}} \cdot e^{\frac{V_p}{n \cdot \phi}}}\right)\right] \tag{16}$$

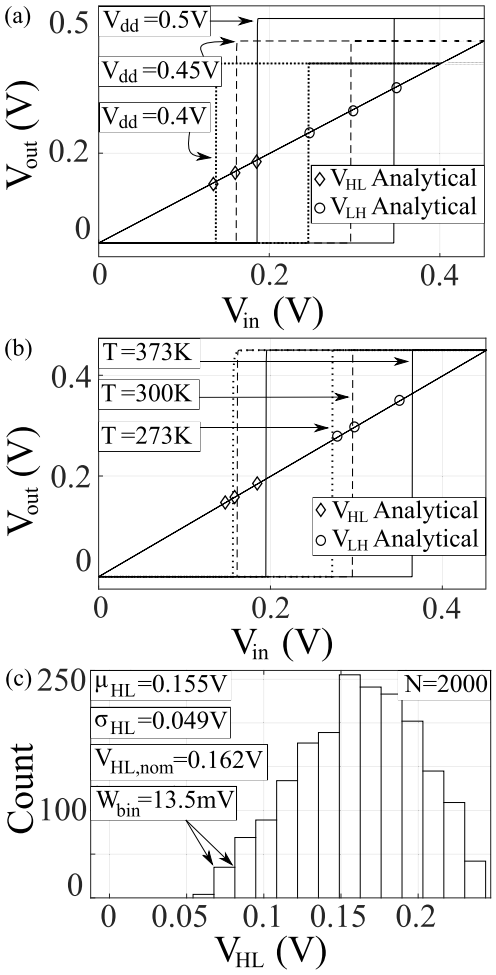

FIGURE 4. Simulated V_{out} vs V_{in} for: (a) different V_{dd} and $T = 300K$; (b) different T and $V_{dd} = 0.45V$. (c) Histogram associated to the Monte Carlo simulations for V_{HL} ($V_{DD} = 0.45V$).

A. SUPPLY VOLTAGE, TEMPERATURE AND PROCESS VARIATIONS

To verify the accuracy of the model, different simulations have been performed by considering supply voltage, temperature and process variations. In Figs. 3(a) and (b), the maximum error occurs when $V_{n(p)} = 0V$. Therefore, in the following the tuning voltages have been fixed to zero volts. In Fig. 4(a), the ST transfer characteristics are depicted for different supply voltages. The error associated to V_{HL} is maximum for $V_{dd} = 0.4V$, while that associated to V_{LH} for $V_{dd} = 0.5V$. Nevertheless, the maximum error relative to V_{dd} is below 3% in the analyzed V_{dd} range. The simulations have been performed with steps of $50mV$ in V_{dd}, but only the extrema are reported, where the error is maximum. For supply voltages below $0.4V$, the circuit does not toggle correctly for certain tuning voltages. In Fig. 4(b), the ST transfer characteristics are depicted for different temperatures ($V_{dd} = 0.45V$). The circuit is sensitive to temperature variations, and for both transition points the maximum error occurs at $T = 373K$. Nevertheless, the relative errors are 4.8% and 3.7% for V_{HL} and V_{LH}, respectively. Finally, Monte Carlo simulations have been performed in order to observe the deviation of the analytical transition voltages from the simulated ones, when considering both process and mismatch variations. The number of iterations was set to $N = 2000$. The histogram associated to V_{HL} is shown in Fig. 4(c). The nominal V_{HL} is $0.162V$. The mean and standard deviation are $0.155V$ and $0.049V$, respectively. Regarding V_{LH}, its nominal value is $0.294V$, while the mean and standard deviation are $0.278V$ and $0.097V$, respectively. The analytical V_{HL} and V_{LH} are within one standard deviation.

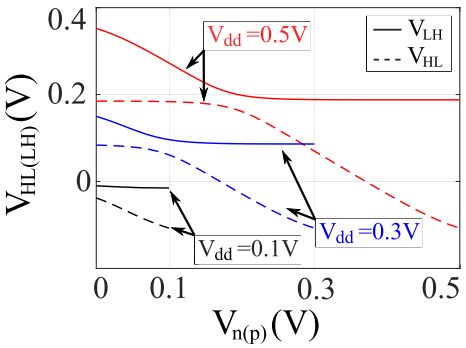

FIGURE 5. Analysis of the minimum supply voltage for which hysteresis occurs. Analytical $V_{HL(LH)}$ vs $V_{n(p)}$ for different supply voltages. No transition occurs when the curves become negative.

B. MINIMUM SUPPLY VOLTAGE AND HYSTERESIS

The proposed analytical model can be used to estimate the minimum supply voltage for which hysteresis occurs. As can be observed in Fig. 4(a), when the supply voltage is decreased, both transition voltages decrease as well. Eventually, when the supply voltage is decreased to a certain value, the high-to-low transition will not occur. However, the low-to-high transition will still occur. In Fig. 5, the analytical high-to-low (V_{HL}) and low-to-high (V_{LH}) transition voltages are plotted as a function of the tuning voltages, for different supply voltages. When $V_{DD} = 0.5V$, a hysteretic behavior is guaranteed only for $V_n < 0.37V$, because for higher tuning voltage the analytical V_{HL} becomes negative, i.e. it is not defined. This means that when sweeping the input voltage from high to low, no transition in the output voltage is observed. When the supply voltage is $0.3V$, the high-to-low voltage is above zero volts until $V_n \approx 0.17V$. When $V_{dd} = 0.1V$, both analytical curves are below zero volts, i.e. no transition is observed for whatever combination of V_n and V_p. It should be remarked that the minimum supply voltage for which hysteresis occurs also depends on transistors' dimensions. For the given design, the minimum supply voltage for which hysteresis occurs is approximately $0.15V$, i.e. when $V_{dd} = 0.15V$, V_{LH} is defined but V_{HL} is below zero volts for whatever V_n. All the presented analysis has been verified through simulations.

IV. EXPERIMENTAL RESULTS

An ASIC in AMS 0.35μm CMOS process has been fabricated through EUROPRACTICE MPW to experimentally validate

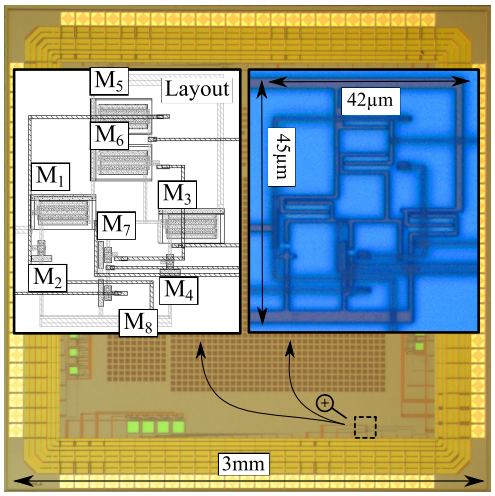

FIGURE 6. Layout and micrograph of the ST (AMS 0.35μm CMOS process).

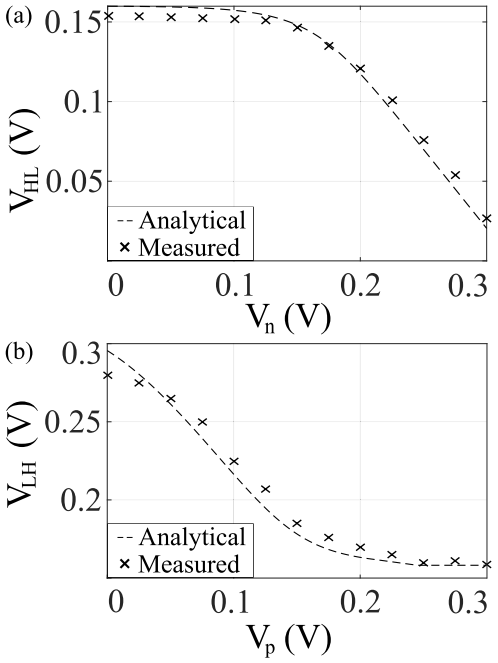

FIGURE 7. Analytical and measured (a) V_{HL} vs V_n and (b) V_{LH} vs V_p ($V_{DD} = 0.45V$).

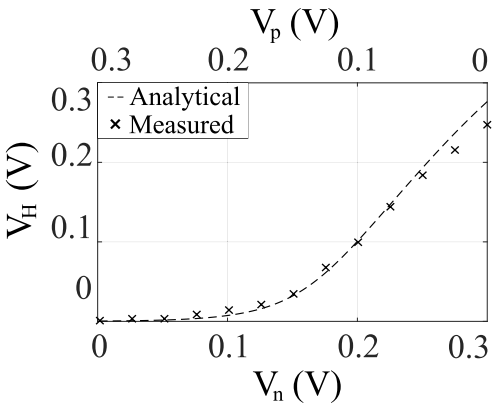

FIGURE 8. Analytical and measured hysteresis width V_H as a function of the tuning voltages $V_{n(p)}$ ($V_{DD} = 0.45V$).

the proposed analytical model. The ST circuit occupies an area of $42\mu m \times 45\mu m$. The PMOS transistors are sized 20/1, while the NMOS 1/1, i.e. same dimensions associated to the curves in Figs. 3(a) and (b). The layout and the micrograph of the circuit are shown in Fig. 6. Due to technology rules, the PMOS transistors are fabricated with two gates, each with a $10u$ width stripe. The voltages have been measured through a KEYSIGHT InfiniiVision DSOX3024T, by applying a $1Hz$ triangular wave at the input of the circuit. The analytical and measured V_{HL} as a function of V_n are shown in Fig. 7(a). The model resembles the measured behavior, although for increasing V_n, the measured V_{HL} is less linear. The same holds for the low-to-high transition point, shown in Fig. 7(b). For small V_p the measured V_{LH} is less linear than the analytical one. The maximum absolute error ($\Delta_{HL,meas} = |V_{HL,meas} - V_{HL}|$) between the analytical and measured V_{HL} is $5mV$, while the relative one ($\delta_{HL,meas} = |\Delta_{HL,meas}/V_{HL}|$) is 3.1%. Regarding the low-to-high transition point, the maximum absolute error is $16mV$, while the relative one is 5%. The difference between the analytical and measured transition points is attributed to circuit parasitics and process variations (e.g. change in the slope factor). As can be observed in Figs. 7(a) and (b), both V_{HL} and V_{LH} are maximum for $V_{n(p)} = 0V$ and minimum for $V_{n(p)} = 300mV$. The maximum hysteresis width ($V_{H,max}$) occurs when $V_n = 0.3V$, and $V_p = 0V$, as can be observed in Fig. 8. $V_{H,max,meas}$ is $253mV$, while the analytical one is $276mV$, i.e. the maximum error between the measured and analytical hysteresis voltages is $23mV$. It has been verified through measurements that the hysteresis transition voltages are strongly independent of each other, i.e. $V_{HL(LH)}$ does not vary with $V_{p(n)}$, in agreement with the analytical model assumptions. The maximum operating frequency is $20Hz$ for the implemented design. Therefore, the circuit is suitable for low frequency applications, e.g. low frequency waveform generators. The circuit power consumption is mainly due to the switching currents during the transitions. Due to the very small amplitude of these currents, they could not be measured precisely. Therefore, the circuit power consumption has been analyzed through simulations only. When switching from low-to-high, the maximum power consumption occurs when $V_p = 0V$ (i.e. M_5 is on), and the switching current has a peak value of $416pA$. Instead, when switching from high-to-low, the maximum power consumption occurs when $V_n = 0.3V$ (i.e. M_3 is on), and the switching current has a peak value of $423pA$. When the same circuit is simulated with the nominal supply voltage for the considered CMOS process ($3.3V$), the maximum peak current has a value of $259\mu A$ and $287\mu A$, during the low-to-high and high-to-low transitions, respectively. Therefore, when the circuit is operated in subthreshold region, the power consumption improves by five orders of magnitude with respect to the case in which the transistors are biased in strong inversion.

V. CONCLUSION

In this article, the subthreshold characteristics of a tunable CMOS Schmitt trigger have been modeled for the first time. The analytical model relates the hysteresis transition voltages to the transistors' geometrical parameters and tuning voltages, allowing the design of the circuit with desired hysteresis width in subthreshold region. Furthermore, it allows optimization of the circuit operation by including the supply voltage and the temperature dependencies in its formulation. The proposed analytical model is based on the assumption that the high-to-low and low-to-high hysteresis transition points are strongly independent of each other. This assumption has been verified both at simulation and experimental level. Supply voltage, temperature and process variations have been considered. Moreover, a simple method for the estimation of the minimum supply voltage for which hysteresis occurs is reported. The maximum error between the analytical and simulated transition points resulted to be less than 5%. The model has also been experimentally validated with an ASIC in AMS 0.35μm CMOS process fabricated through EUROPRACTICE MPW. The maximum error between the analytical and measured transition points is below 6%. The power consumption has an improvement of five orders of magnitude, while the maximum operating frequency is limited to 20Hz, for the given design. Overall, the proposed analytical model provides a deeper understanding of the circuit subthreshold operation for low power and low frequency applications.

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REFERENCES

[1] O. H. Schmitt, "A thermionic trigger," *J. Sci. Instrum.*, vol. 15, no. 1, p. 24, 1938.

[2] M. E. Valentinuzzi, "Otto Herbert Arnold Schmitt (1913–1998), a pioneer (an overview of Schmitt's scientific production)," *IEEE Eng. Med. Biol. Mag.*, vol. 23, no. 6, pp. 42–46, Nov. 2004.

[3] H. A. Alzaher, "Novel Schmitt trigger and square-wave generator using single current amplifier," *IEEE Access*, vol. 7, pp. 186175–186181, 2019.

[4] A. Panda, A. K. Singh, R. Tirupathi, and S. K. Kar, "A low-power tunable square-wave generator for instrumentation applications," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 7, pp. 5051–5057, Jul. 2020.

[5] W. S. Chung, H. Kim, W.-H. Cha, and H.-J. Kim, "Triangular/square-wave generator with independently controllable frequency and amplitude," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 1, pp. 105–109, Feb. 2005.

[6] A. De Marcellis, G. Ferri, and P. Mantenuto, "A CCII-based non-inverting Schmitt trigger and its application as astable multivibrator for capacitive sensor interfacing," *Int. J. Circuit Theory Appl.*, vol. 45, no. 8, pp. 1060–1076, 2017.

[7] H. Kim, W.-S. Chung, H.-J. Kim, and S.-H. Son, "A resistance deviation-to-pulsewidth converter for resistive sensors," *IEEE Trans. Instrum. Meas*, vol. 58, no. 2, pp. 397–400, Feb. 2009.

[8] A. Bonanno, M. Crepaldi, I. Rattalino, P. Motto, D. Demarchi, and P. Civera, "A 0.13 μm CMOS operational Schmitt trigger R-to-F converter for nanogap-based nanosensors read-out," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 975–988, Apr. 2013.

[9] E. D. Kyriakis-Bitzaros, N. A. Stathopoulos, S. Pavlos, D. Goustouridis, and S. Chatzandroulis, "A reconfigurable multichannel capacitive sensor array interface," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 9, pp. 3214–3221, Sep. 2011.

[10] H. Kim, H. J. Kim, and W. S. Chung, "Pulsewidth modulation circuits using CMOS OTAs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 7, pp. 1869–1878, Sep. 2007.

[11] T. Matic, T. Svedek, and M. Herceg, "A method for the Schmitt-trigger propagation-delay compensation in asynchronous sigma–delta modulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 7, pp. 404–408, Jul. 2012.

[12] S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, "Single-ended Schmitt-trigger-based robust low-power SRAM cell," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 8, pp. 2634–2642, Aug. 2016.

[13] E. Abbasian, F. Izadinasab, and M. Gholipour, "A reliable low standby power 10T SRAM cell with expanded static noise margins," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 4, pp. 1606–1616, Apr. 2022.

[14] M. Moghaddam, M. H. Moaiyeri, and M. Eshghi, "Design and evaluation of an efficient Schmitt trigger-based hardened latch in CNTFET technology," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 267–277, Mar. 2017.

[15] B. Ando and S. Graziani, "An instrument for the detection of optimal working conditions in stochastic systems," *IEEE Trans. Instrum. Meas.*, vol. 52, no. 3, pp. 815–821, Jun. 2003.

[16] Y. C. Lai and S. Y. Huang, "A resilient and power-efficient automatic-power-down sense amplifier for SRAM design," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 10, pp. 1031–1035, Oct. 2008.

[17] J. Hu, B. Liu, R. Ma, M. Liu, and Z. Zhu, "A 32 × 32-pixel flash LiDAR sensor with noise filtering for high-background noise applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 2, pp. 645–656, Feb. 2022.

[18] Y. Xu, W. Zhong, B. Li, S. Deng, H. Fan, Z. Wu, L. Lu, F. S. Y. Yeung, H. S. Kwok, and R. Chen, "An integrator and Schmitt trigger based voltage-to-frequency converter using unipolar metal-oxide thin film transistors," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 144–150, 2021.

[19] Z. Tang, Y. Fang, Z. Shi, X.-P. Yu, N. N. Tan, and W. Pan, "A 1770-μm^2 leakage-based digital temperature sensor with supply sensitivity suppression in 55-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 781–793, Mar. 2020.

[20] P.-R. Chang, B.-C. Wang, and H. M. Gong, "A triangular connection Hopfield neural network approach to analog-to-digital conversion," *IEEE Trans. Instrum. Meas.*, vol. 43, no. 6, pp. 882–888, Dec. 1994.

[21] S. L. Tesic, "Simple time-delay circuit with very high duty cycle," *IEEE Trans. Instrum. Meas.*, vol. IM-19, no. 3, pp. 152–156, Aug. 1970.

[22] E. S. Yang, "A probability density analyzer," *IEEE Trans. Instrum. Meas.*, vol. IM-18, no. 1, pp. 15–18, Mar. 1969.

[23] M. R. Elmezayen, W. Hu, A. M. Maghraby, I. T. Abougindia, and S. U. Ay, "Accurate analysis and design of integrated single input Schmitt trigger circuits," *J. Low Power Electron. Appl.*, vol. 10, no. 3, p. 21, Jun. 2020.

[24] L. A. P. Melek, A. L. da Silva, M. C. Schneider, and C. Galup-Montoro, "Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 869–878, Apr. 2016.

[25] T. D. Fernandes, C. Galup-Montoro, and M. C. Schneider, "Analysis and design of the three-inverter Schmitt trigger for supply voltages down to 50 mV," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 7, pp. 2302–2306, Jul. 2021.

[26] L. A. P. Melek, M. C. Schneider, and C. Galup-Montoro., "Operation of the classical CMOS Schmitt trigger as an ultra-low-voltage amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 9, pp. 1239–1243, Sep. 2018.

[27] A. Nowbahari, L. Marchetti, and M. Azadmehr, "Weak inversion model of an inverting CMOS Schmitt trigger," in *Proc. 11th Int. Conf. Commun., Circuits Syst. (ICCCAS)*, May 2022, pp. 1–5.

[28] S. Radfar, A. Nejati, Y. Bastan, P. Amiri, M. H. Maghami, M. Nasrollahpour, and S. Hamedi-Hagh, "A sub-threshold differential CMOS Schmitt trigger with adjustable hysteresis based on body bias technique," *Electronics*, vol. 9, no. 5, p. 806, May 2020.

[29] A. Nejati, S. Radfar, P. Amiri, and M. H. Maghami, "A bulk-driven differential CMOS Schmitt trigger with adjustable hysteresis for ultra-low-voltage operation," *Microelectron. J.*, vol. 114, Aug. 2021, Art. no. 105129.

[30] R. Gonzalez, B. M. Gordon, and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1210–1216, Aug. 1997.

[31] N. Lotze and Y. Manoli, "Ultra-sub-threshold operation of always-on digital circuits for IoT applications by use of Schmitt trigger gates," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 11, pp. 2920–2933, Nov. 2017.
[32] *Ericsson Mobility Report*, Ericsson, Stockholm, Sweden, Nov. 2021.
[33] C. C. Enz and E. A. Vittoz, "CMOS low-power analog circuit design," in *Proc. Emerg. Technol., Designing Low Power Digit. Syst.*, May 1996, pp. 79–133.
[34] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
[35] N. Lotze and Y. Manoli, "A 62 mV 0.13 μm CMOS standard-cell-based design technique using Schmitt-trigger logic," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, Jan. 2012.
[36] Y. Bastan, A. Nejati, S. Radfar, P. Amiri, M. Nasrollahpour, and S. Hamedi-Hagh, "An ultra-low-voltage sub-threshold pseudo-differential CMOS Schmitt trigger," in *Proc. 31st IEEE Int. Syst.-Chip Conf. (SOCC)*, Sep. 2018, pp. 1–5.
[37] R. Sandiri, Y. Chimata, Y. Nalamasa, and P. Arra, "Design of noise immune subthreshold circuits using dynamic threshold Schmitt trigger logic," in *Proc. IEEE Region 10 Symp. (TENSYMP)*, Jul. 2022, pp. 1–6.
[38] A. Nowbahari, L. Marchetti, and M. Azadmehr, "Analysis of a low power inverting CMOS Schmitt trigger operating in weak inversion," *Int. J. Electr. Electron. Eng. Telecommun.*, vol. 11, pp. 392–397, Nov. 2022. [Online]. Available: http://www.ijeetc.com/uploadfile/2022/1014/20221014033458167.pdf
[39] S. F. Al-Sarawi, "Low power Schmitt trigger circuit," *Electron. Lett.*, vol. 38, no. 18, pp. 1009–1010, Aug. 2002.
[40] Z. Wang, "CMOS adjustable Schmitt triggers," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 3, pp. 601–605, Jun. 1991.
[41] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, Jul. 1995.
[42] Y. Zhou, J. Mercier, and F. Yuan, "A comparative study of injection locked frequency divider using harmonic mixer in weak and strong inversion," in *Proc. IEEE 61st Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2018, pp. 97–100.
[43] S. M. Sharroush, "Analysis of the subthreshold CMOS logic inverter," *Ain Shams Eng. J.*, vol. 9, no. 4, pp. 1001–1017, Dec. 2018.
[44] M. A. Eldeeb, Y. H. Ghallab, Y. Ismail, and H. Elghitani, "Low-voltage subthreshold CMOS current mode circuits: Design and applications," *AEU-Int. J. Electron. Commun.*, vol. 82, pp. 251–264, Dec. 2017.
[45] M. Alioto, "Understanding DC behavior of subthreshold CMOS logic through closed-form analysis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 7, pp. 1597–1607, Jul. 2012.

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