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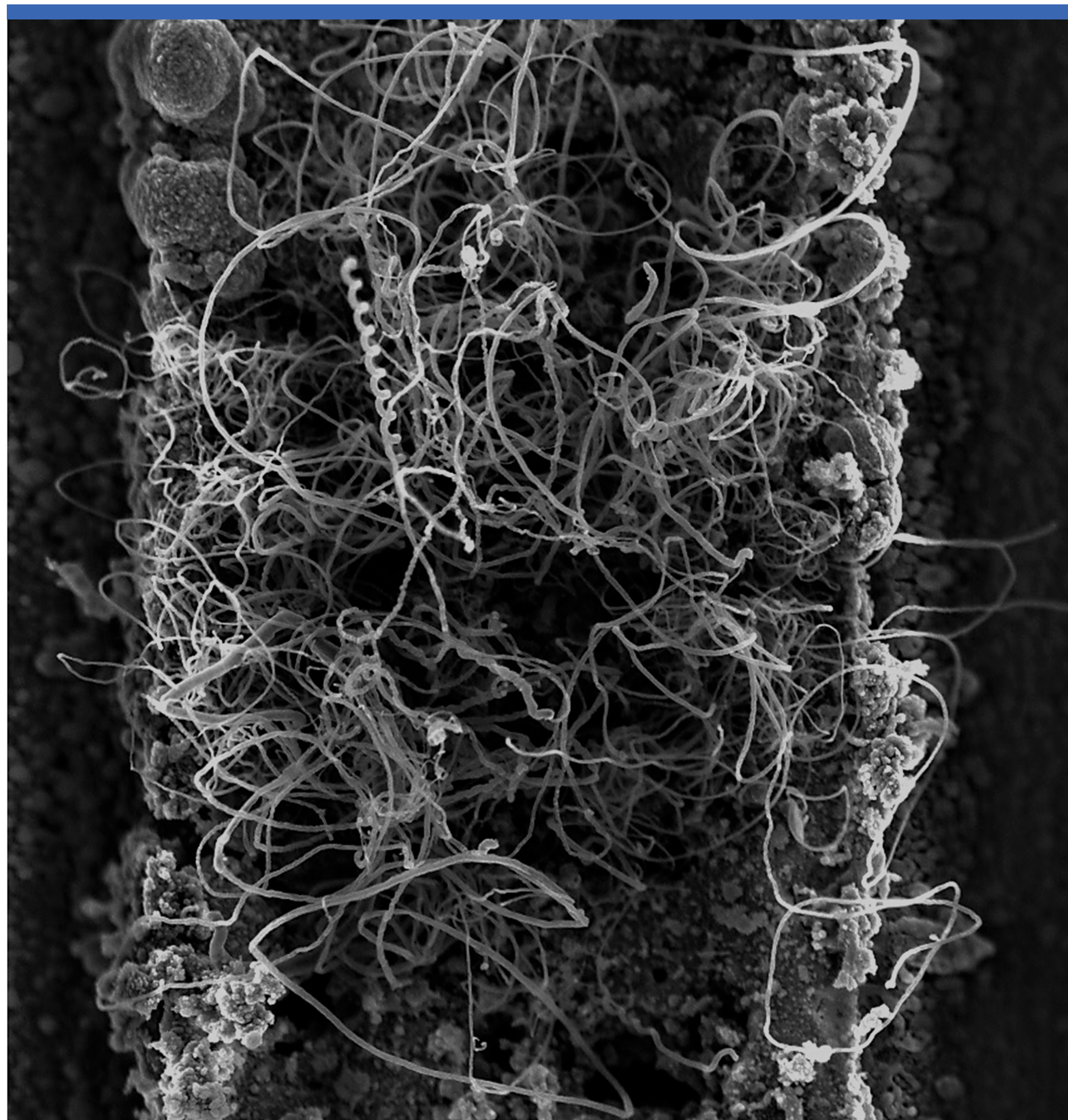
2020

Avisek Roy

Local Synthesis of Carbon Nanotubes on CMOS-MEMS Microheaters for Sensing Applications



Avisek Roy

Local Synthesis of Carbon Nanotubes on CMOS-MEMS Microheaters for Sensing Applications

A PhD dissertation in
Applied micro- and nanosystems

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To my loving family

Preface

This thesis is submitted in partial fulfilment of the requirements for the degree of Philosophiae Doctor (Ph.D.) from the Department of Microsystems, at the University of South-Eastern Norway (USN). This doctoral work has mainly been conducted at the Department of Microsystems (IMS), Faculty of Technology, Natural Sciences and Maritime Sciences, University of South-Eastern Norway (USN) in Borre, Norway. Experiments have also been carried out at the University of Illinois at Chicago (UIC) in Chicago, USA. The work has been done under the supervision of Professor Knut E. Aasmundtveit at USN, Associate Professor Mehdi Azadmehr at USN, and Professor Philipp D. Häfliger at University of Oslo (UiO).

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A special thanks to Asc. Professor Bao Q. Ta and Dr. Luca Marchetti for their support in experiments, helpful suggestions, and fruitful discussions throughout my PhD work. I would also like to thank Donatus L. Dress, Fredrik Holst and Blendian Mujaj for their support in laboratory work and for the insightful discussions we had.

For successful experimental works, support of the laboratory engineers is essential. I am thankful to Zekija Ramic, Thomas Martinsen, Dr. Muhammad Tayyib and Dr. Thai Anh Tuan Nguyen for providing that support on different stages of the research. I am also thankful to Asc. Professor Igor Paprotny, John Sabino and Tejumade Durowade for their support during my research visit at the University of Illinois at Chicago (UIC) in USA.

I would like to thank the Norwegian research council, our Department of Microsystem, and Nano-Network for providing the financial support and necessary facilities for the research work. Thanks to the PhD coordinators, Kristin Skjold Granerød and Aina Enstad for their support with the administrative works. Also, I wish to thank the members of the thesis assessment committee for taking the time to evaluate the doctoral thesis and for providing valuable comments and recommendations to further improve it.

PhD work can be very demanding. I am grateful to have an excellent group of colleagues at USN during this time. Thank you for the technical discussions, relaxing chats and the boardgame nights! Finally, my sincere gratitude goes to my closest family and my girlfriend for their unparalleled support, patience, and encouragement throughout the time of my PhD.

Abstract

Research on nanomaterials is growing rapidly due to their extraordinary properties, which can significantly differ from their bulk form. The physicochemical properties of nanoscale materials are diverse and can be engineered for utilizing them in numerous applications to advance our technology. Among the nanomaterials, carbon nanotube (CNT) is a popular candidate as a sensing material, which demonstrated promising results for potential commercial applications. A monolithic CMOS-CNT integration can provide sensing features through the CNTs on the top and read-out integrated circuits (ROICs) based on CMOS transistors in the bottom.

CNTs can be locally grown on custom-designed CMOS microstructures to utilize their sensing capabilities in emerging micro and nanotechnology applications. The main goal of this PhD project was to develop a CMOS-compatible CNT synthesis process on microheaters designed and fabricated in commercial CMOS chips with the vision of enabling the pathway for mass production of CNT-based sensors. Prior to designing a dedicated CMOS chip for CNT growth, thermal-mechanical simulations were performed on CMOS material layers that can generate the required CNT synthesis temperature (~650-900 ˚C) by joule heating. The simulated microheaters showed promising results with high thermal isolation to keep low ambient temperatures for CMOS-compatibility. Among the investigated CMOS materials, polysilicon is most suitable as heaters for high-temperature applications, while the metal options (i.e., Al, Cu) need alloying with Ni.

A CMOS chip with various polysilicon and aluminium microheaters was designed and fabricated in a commercial AMS 350 nm CMOS technology. Different designs also incorporate various features for realizing CMOS-MEMS heaters with varied post-processing results. A key contribution to the CMOS-CNT integration was the developed post-processing of CMOS chips for fabricating CMOS-MEMS heaters. In this post-CMOS processing, subtractive microfabrication technique was used for micromachining the heaters, where the passivation layers in CMOS were used as mask to protect the electronics. For the dielectric etching, high selectivity, uniform etching and good etch rate was required to fully expose the polysilicon layers without causing damages. It was

achieved by developing two-step reactive ion etching (RIE) of SiO_2 dielectric layer and making design improvements on a second-generation CMOS chip. Partial and fully suspended CMOS-MEMS microheaters were also fabricated by SiO_2 wet etching with minimum damage to the exposed aluminium layers.

CNTs were successfully synthesized on the polysilicon CMOS-MEMS heaters in a local thermal CVD process. The heaters had low CNT growth temperatures (~650 – 750 ˚C) before a breakdown, resulting in low yield with Fe catalyst. Growth with Ni provided higher yield with relatively lower diameter (< 20 nm). CNT growth was investigated on various non-suspended and suspended microheaters. Adding H_2 reduction gas improved growth quality. The growth process needs further development to grow longer CNTs within the obtained temperatures. Thermal instability issues of thin polysilicon layers were addressed, which made the CNT growth process challenging. Synthesized CNTs on two neighbouring heaters established a connection through the Si substrate; one of which was utilized to demonstrate gas and pressure sensing. To the author's knowledge, this is the first demonstration report for sensing applications using locally synthesized CNTs on the polysilicon layers of a commercial low-cost bulk CMOS technology.

Two CMOS microstructures were calibrated for on-chip temperature sensing. Results show that chip temperature ranging from room-temperature to 200 ˚C can be estimated with a deviation below 2 ˚C between the two sensors, while the deviation increases with higher temperature. Two on-chip transistors were also characterized upon heat exposure from different polysilicon microheaters that were used for CNT synthesis. Apart from one case, behaviour of the transistors did not change. Hence, CMOS-compatibility was confirmed for majority of the non-suspended CMOS-MEMS CNT growth structures. Our developed process for heterogenous monolithic integration of CMOS-CNT shows the promise of wafer-level manufacturing of CNT-based sensors by incorporating additional steps in an already existing foundry CMOS process.

Keywords: carbon nanotube, local CNT synthesis, CMOS-CNT integration, CMOS microheater, polysilicon microheater, CNT growth on CMOS, CNT-based sensor, gas sensor, pressure sensor, on-chip temperature sensor, thermal analysis

List of Papers

Paper 1 & 3–7 omitted due to publisher's restrictions

Article 1

A. Roy, F. Ender, M. Azadmehr, and K. E. Aasmundtveit, "CMOS micro-heater design for direct integration of carbon nanotubes," Microelectronics Reliability, 2017.
https://doi.org/10.1016/j.microrel.2017.05.031

Article 2

A. Roy, M. Azadmehr, B. Q. Ta, P. Häfliger, and K. E. Aasmundtveit, "Design and Fabrication of CMOS Microstructures to Locally Synthesize Carbon Nanotubes for Gas Sensing," Sensors, 2019.
https://doi.org/10.3390/s19194340

Article 3

A. Roy, B. Q. Ta, M. Azadmehr, and K. E. Aasmundtveit, "Post-processing challenges and design improvements of CMOS-MEMS microheaters for local CNT synthesis," *To be submitted*.

Article 4

K. E. Aasmundtveit, **A. Roy**, and B. Q. Ta, "Direct Integration of Carbon Nanotubes in CMOS – Towards an Industrially Feasible Process," IEEE Transactions on Nanotechnology, 2020.
https://doi.org/10.1109/TNANO.2019.2961415

My contributions: All results and most writings in Section IV (CNT growth structures in CMOS), contributions in writing and reviewing some parts of the other sections.

Article 5

A. Roy, F. Ender, M. Azadmehr, B. Q. Ta, and K. E. Aasmundtveit, "Design considerations of CMOS micro-heaters to directly synthesize carbon nanotubes for gas sensing applications," IEEE-NANO conference, 2017.
https://doi.org/10.1109/NANO.2017.8117447

Article 6

A. Roy, M. Azadmehr, P. Häfliger, B. Q. Ta, and K. E. Aasmundtveit, "Direct Synthesis of Carbon Nanotubes in CMOS – Layout of Micro-heaters," IEEE-NANO conference, 2018. https://doi.org/10.1109/NANO.2018.8626363

Article 7

A. Roy, L. Marchetti, M. Azadmehr, P. Häfliger, B. Q. Ta, and K. E. Aasmundtveit, "Characterization of Polysilicon Microstructures to Estimate Local Temperature on CMOS Chips," IEEE-ESTC conference, 2020.
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Papers not enclosed in the thesis

Article 8

K. E. Aasmundtveit, **A. Roy**, & B. Q. Ta, "Carbon Nanotubes Directly Integrated in CMOS by Local Synthesis – Towards a Wafer-Level Process," IEEE-NMDC conference, 2018. https://doi.org/10.1109/NMDC.2018.8605926

Article 9

A. Roy et al., "Local Synthesis of Carbon Nanotubes on CMOS Microstructures for Gas Sensing," *In preparation*.

Further, six more articles are planned for publication based on the contents from chapter 3 to 8.

List of Co-supervised Projects

1. Iqbol Adahamjonov, “Analysis of Test Structures for Ni-Al alloy Microheaters with Reduced Heat Transfer”, *Master Thesis*, USN, 2018.

2. Nuk Damys, “Design and Fabrication Challenges of MEMS Resonating Gas Sensor”, *Master Thesis*, USN, 2018.

3. Benjamin C. Figved, Hermon A. Gebrekidan, Arthur W. Haugen and Thomas A. Gabrielsen, “Design, Simulation and Fabrication of MEMS resonating sensors”, *Bachelor Thesis*, USN, 2019.

4. Bishwojit Konsam, “Fabrication of SOI Wafer and Mask for an FD-SOI Junctionless Transistor in a MEMS Cleanroom”, *Master Thesis*, USN, 2019.

5. Arian Nowbahari, “Design of a Low-cost Single Gate Planar Junctionless Transistor”, *Master Thesis*, USN, 2019.

6. Donatus Leonhard Dress, “Design and Fabrication of Microheaters with SOI Wafers for CNT Synthesis”, *Master Thesis*, USN, 2020.

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Chapter 1

Introduction

1.1 The world of macro, micro and nano

We measure the size of objects and distances based on a standard reference size defined by us. In the International System of Units (SI), we defined the unit of length as 'metre' through the fundamental constant of the speed of light and another fixed value, natural resonance frequency of the Caesium atom. Conveniently, this standard reference size is very much comparable to an average human size. We can then scale up or down, preferably in the order of thousands, to express the distance or size of something. However, it is easy to lose the grasp over the size of a thing as it starts to get smaller or larger relative to the world around us. We can certainly express the size of something in numbers, but it often becomes difficult to comprehend such values with our human senses. The illustration in *Figure 1.1* is an attempt to comprehend the relative sizes of different natural and artificial things at various scales.

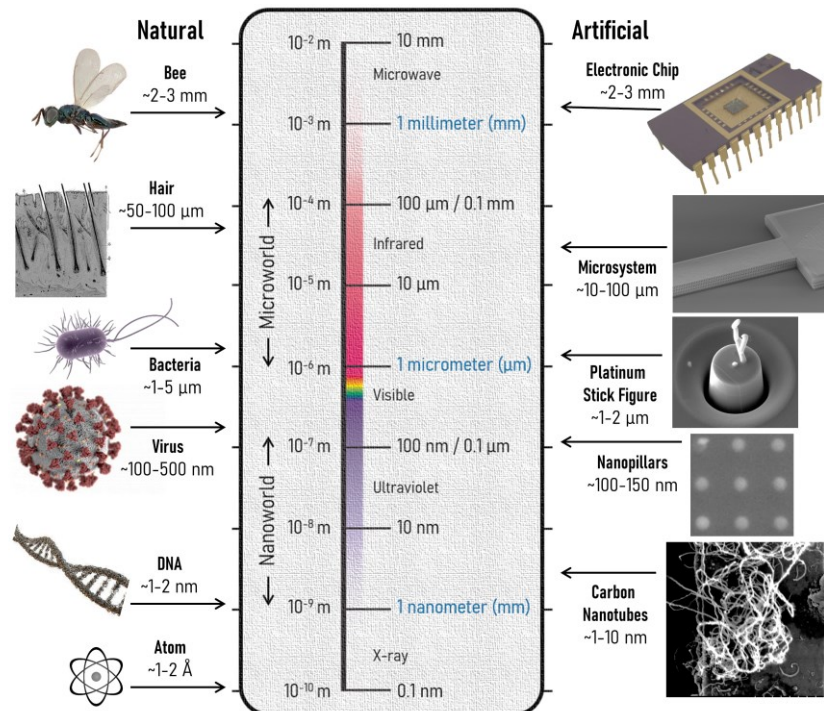


Figure 1.1: Relative sizes of various natural and artificial things in macro, micro and nanoscale.

Macroworld can be defined in terms of the sizes in human scale, where we can see the things with the naked eye and handle them with ease. Through our regular interaction with the macroworld, the immensity of space around us at the large scale is apparent, whereas the abundance of space at the small scale is not often perceived due to the relative nature of size. To express the vastness of space in small scale, German physicist Emil Wiechert mentioned in 1897 that the universe can be infinite in all directions, not only above us in the large but also below us in the small, as quoted by physicist Freeman Dyson in his book *"Infinite in All Directions"* [1].

How large is the world of micro? If we see from the perspective of nanostructures, it is as large as kilometres to us. With the envision of utilizing the space at the molecular level to manufacture nanoscale machines, a renowned physicist once stated:

"There is plenty of room at the bottom."

– Richard Feynman, 1959

Shrinking in size can provide us a lot of room to build micro or nanomachines apart from other advantages, but we also need to make a link with our macroworld to interact with the system. Therefore, we aim to establish our connection from the world of macro to nano through the world of micro.

1.2 Background and motivation

Miniaturized systems such as microdevices bring numerous benefits over its macro counterpart, being small and lightweight is only a part of it. The microdevices have high resistance to shock and vibration [2,3], thus ensure high robustness and reliability. Moreover, a large array of microdevices can be fabricated parallelly in batch by photolithography, which corresponds to low manufacturing cost. A microsystem can become even more interesting with the inclusion of nanomaterials.

Nanomaterials are simply materials sized in nanoscale, where at least one dimension of the material is typically considered less than 100 nm. Material at the small scale behaves differently than they do at the macroscopic level as many negligible effects at the macroscale become prominent at the micro and nanoscale, for example, surface tension

becomes a more dominant force than gravity [4–7]. Although properties of materials at microscale resembles macroscale, changes in material properties start to appear at nanoscale due to the domination of surface effects [4,8], making nanoworlds fundamentally different than the world at larger scale.

The unique and remarkable physical [9], electronic [10], thermal [11], optical [12], mechanical [13], chemical [14] properties of nanomaterials can be harnessed in numerous innovative applications [15–21]. The nanomaterials can also be engineered for modifying their physicochemical properties to enhance performance in desired utilization [22–26]. Nanomaterials with their reduced size have huge surface area relative to their volume (*Figure 1.2a*). As the particle size of a material reduces, the surface area of the nanoparticle increases exponentially with respect to its volume; below a certain particle size, the number of atoms at the surface of the nanoparticle exceeds the amount inside it (*Figure 1.2b*). Surface effects of a nanoparticle starts to dominate with the increase in surface-to-volume ratio, influencing drastic changes in its material properties [15,16,27–29], which in turn facilitates nanotechnology.

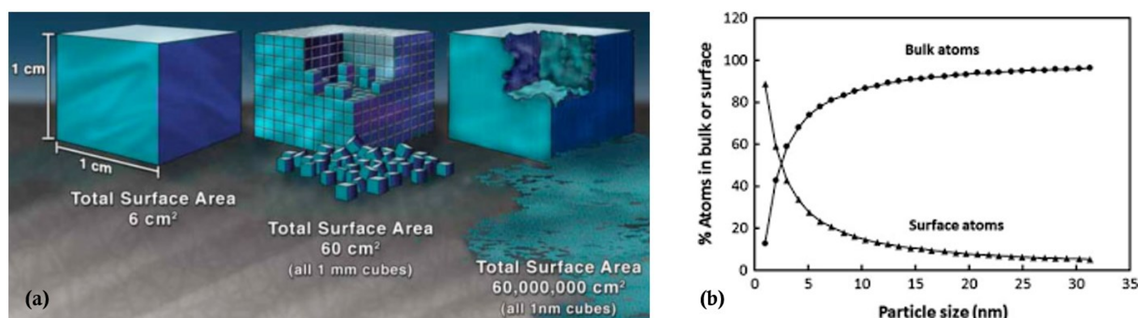


Figure 1.2: Effect of miniaturization. (a) Increase in surface area with decrease in cube size [30], (b) Variation in surface and bulk atom ratio with nanoparticle size [15,28].

Based on the composition, nanomaterials can be organic (e.g., carbon-based, dendrimers, polymers), inorganic (e.g., metals, metal oxides, quantum dots) and composites (e.g., organic-inorganic, organic-organic, inorganic-inorganic) [15,25,31]. Among them, carbon-based nanomaterials such as fullerenes, carbon nanotubes, graphene, and carbon quantum dots are very attractive in fundamental research due to their exceptional material properties and scope for various potential applications in

different technological fields [32–43]. One-dimensional (1D) carbon nanomaterial, carbon nanotubes (CNTs) have been in limelight of extensive research [44–46] due to their impressive material and structural properties, which can be exploited in various manner including smart sensing applications as detailed in *section 1.3*. With their sensing potentials in mind, CNTs became the choice of nanomaterial in our research.

CNTs need to be integrated in a microsystem for utilizing their sensing capabilities. Apart from being a platform for the CNTs and a bridge to the macroscopic world, a microsystem can contribute by providing electrical signal across the CNTs and process the acquired signal variations from these sensing nanomaterials to realize a smart system integration. A microelectromechanical system (MEMS) is a typical choice for micro and nanoscale integration due to its flexible fabrication process and material choice. However, a low-cost compact system with integrated circuits (ICs) for on-chip signal processing is important to commercially manufacture CNT-based sensors [47–49]. Such a microsystem platform can be provided by complementary metal–oxide–semiconductor (CMOS) technology, where the sensors will also benefit from short interconnects, less parasitic elements, low power consumption and better signal to noise ratio (SNR) with the built-in electronics [49–51]. Therefore, an attractive but challenging approach is directly integrating CNTs into CMOS. Potential integration methods and involved challenges are discussed in *section 1.4*.

There has been substantial amount of work on CNTs to explore its potential as a sensing material, but commercial CNT-based sensors are still not available [52]. It is mainly due to the absence of a standard process for integrating CNTs in a low-cost industrial CMOS technology with minimum modifications to the foundry fabrication process. Different literatures demonstrated CMOS-compatible integration process through MEMS implementations or extensive CMOS post-processing, which are not easily transferrable to current inexpensive CMOS technologies. Economical sensors with low-power and portability have many commercial applications, especially in this era of networked technologies that induces an increasing demand of sensors for the internet of things (IoT) [53]. This work aims to pave the way for realizing CNT-based commercial sensors.

1.3 Carbon Nanotubes

Carbon nanotubes are an allotrope of carbon, similar to the other carbon forms such as diamond, graphite, amorphous carbon and fullerenes. Based on the bonding formation of the atoms in carbon lattices, properties of these allotropes vary. For example, diamond is a very hard, electrically non-conductive, brittle material with the ability of light dispersion, which makes it useful in industrial applications such as cutting and drilling, while also commonly being used as jewellery mostly owing to its latter property. In contrast, graphite is soft and conductive (both electrically & thermally), thus utilized as pencil leads and electrodes due to the respective properties. A single atomic layer of graphite is known as graphene, properties of which [54–56] vastly varies from its bulk form. CNTs can be visualized as a two-dimensional (2D) rolled-up graphene sheet into a 1D cylindrical or tube shape as illustrated in *Figure 1.3*.

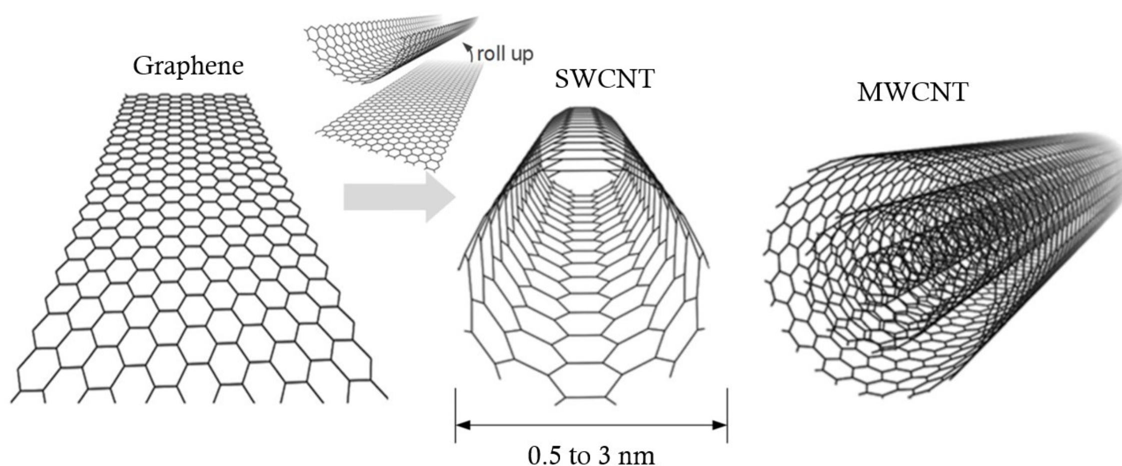


Figure 1.3: Schematics of graphene sheet, SWCNT and MWCNT. Adapted from [57].

1.3.1 Classifications

CNTs with one graphene sheet or wall is called single-walled carbon nanotube (SWCNT), while CNTs consisting multiple concentric layers of graphene sheets or walls are referred as multi-walled carbon nanotube (SWCNT). Sumio Iijima discovered MWCNTs in 1991 [58] and SWCNTs in 1993 [59]. MWCNTs can be as thin as 4-5 nm [60] and as long as 65 cm [61], resulting in extremely high aspect ratio. Each layer of MWCNTs can be considered as a SWCNT. MWCNTs will show metallic behaviour if one of its layers is

metallic [62–64]. In majority of the cases, MWCNTs show metallic characteristics [65,66], even if the individual SWCNT layers of a double-walled CNTs (DWCNTs) are semiconducting [66–68]. It has also been reported that metallic MWCNTs can be converted to semiconducting MWCNTs [69]. Rolling up a graphene sheet in a certain angles and curvatures is known as chirality of the CNTs, which has a significant impact on the properties of this nanomaterial [70–73]. SWCNTs can have either semiconducting or metallic behaviour based on their chirality [74–76].

CNTs often have structural disorders and form various types of defects such as voids, branching, bamboo-like structures, flakes [77–79]. These defects can influence the properties of the CNTs [78–83], which may also be useful in some applications [84–87]. Carbon nanofibers are another form of defective structures, which are often larger in diameter and unlike CNTs, their graphene layers are not concentric [88]. CNTs have improved structural orders with less defects at high temperatures [89–91]. Quality of the CNTs can be relatively determined through transmission electron microscopy (TEM) and Raman spectroscopy [90,91]. Since our process does not rely on a specific structure or chirality of the CNTs, these analyses were not considered for characterization.

1.3.2 Properties and applications

CNTs have earned their place as one of most researched nanomaterials [7,44–46,92] due to their extraordinary structural [93], electrical [94], electronic [95], optical [96], chemical [97], thermal [98], and mechanical [99] properties which can be exploited through a numerous range of applications in various fields of nanotechnology. CNTs can be 50,000 times thinner than average human hair, while being more than 100 times stronger than steel. One-dimensional structure of the CNTs enable them to have high aspect ratio. CNTs with their large surface area in proportion to the volume ensures enhanced chemical reactivity to certain gases while having good thermodynamic stability [100–102], which makes them an excellent sensing material. Metallic CNTs can withstand very high current density (> 10^9 A/cm^2) [103,104] which is ~3 orders of magnitude higher than the capacity of copper, while their room temperature thermal conductivity of 3500 W/m-K [105] is near 10 times higher than that of copper. Thus,

CNTs are a potential candidate to replace current interconnecting metals and vias in future IC technology [106]. Semiconducting CNTs with their higher mobility than any known semiconductors [107] hold the promise of succeeding silicon as the transistor channel [108]. CNTs are also ideal absorbers of infrared (IR) radiation and show enhanced photoresponse in the electrical conductivity of suspended SWCNTs, which is fitting characteristics for a sensitive material in bolometers [109,110].

CNTs have been attracting significant interests in different research fields including biomedical [35,111,112], chemical [97,113,114], electronics [53,115,116] and many other innovative technologies [45,52,117,118]. For biomedical applications, CNTs are mainly used in biosensors [119], targeted drug delivery systems [120], cancer diagnosis and therapy [121]. Most typical utilization of CNTs are in chemical fields that includes enormous amount of diverse sensing applications [122–133]. In microelectronics, recent developments of CNT field effect transistors (CNTFETs) [108,134–136] show promise to realize beyond-silicon integrated circuits. Among the other emerging CNT-based applications, water treatment [137] and energy conversion & storage [138] are notable. A few prominent CNT-based applications are presented in *Figure 1.4*.

The inherited properties of CNTs are effectively utilized in gas sensing applications [139–141]. Their large surface-to-volume ratio plays an important role in such applications as more gas molecules can come in contact with the surface of the CNTs, resulting in enhanced reactivity [142]. Moreover, CNTs offer room-temperature operation and the option for functionalization with metal or metal oxide nanoparticles to deliver enhanced sensitivity, selectivity, chemical stability, fast response [143–145] along with the promises of a wireless, low-cost, power efficient system upon CMOS integration [47–49]. There is a high demand for gas sensors of such qualities to utilize them in various domestic and industrial applications such as monitoring air quality of indoor (e.g., CO_2, H_2, odor) [146] and outdoor (SO_2, NO_2, CO_2) [147] for health and environmental concerns, detecting quality of perishable food [148], breath analysis through volatile organic compounds for medical diagnosis [149], and detecting pesticides and pathogens in agricultural production [97].

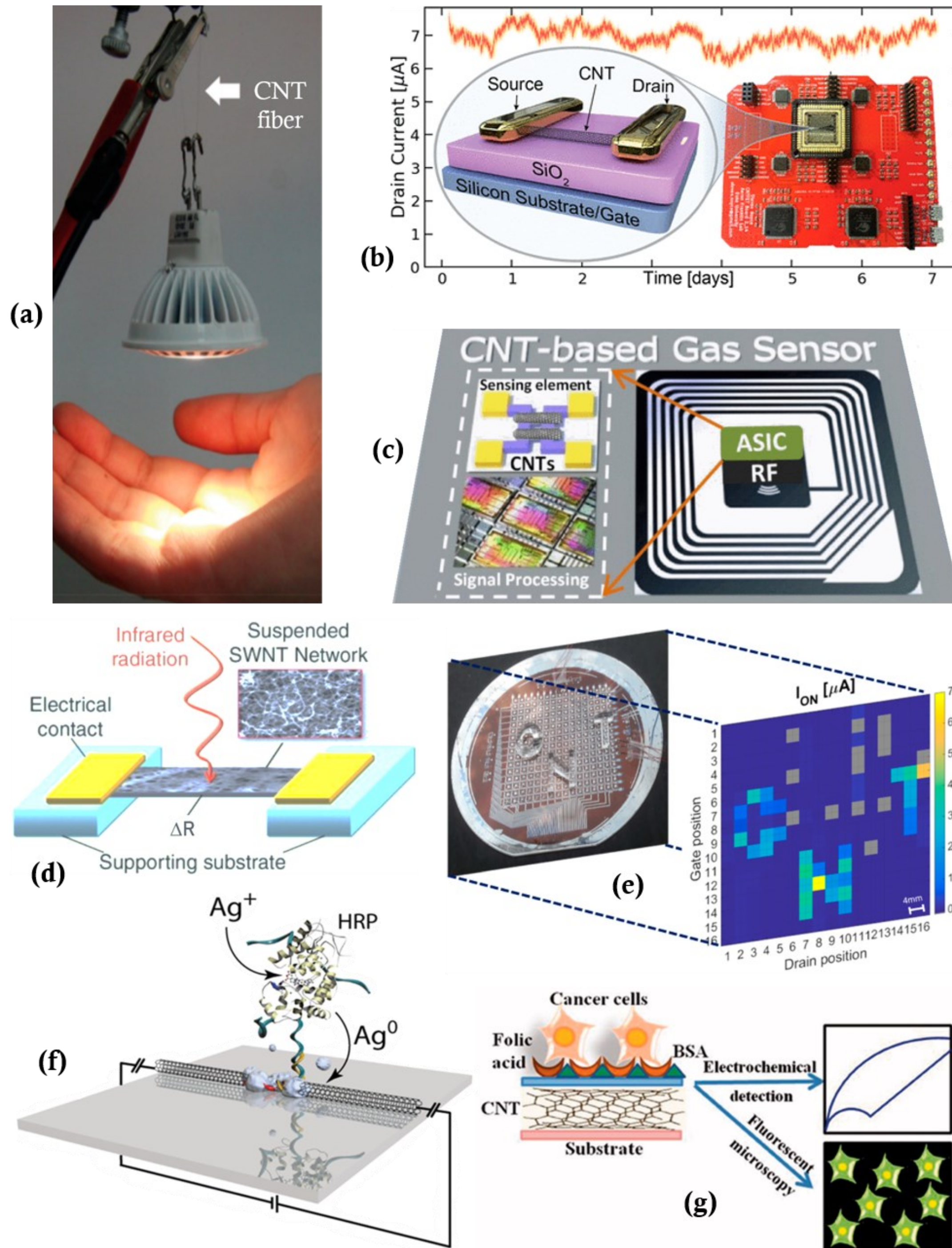


Figure 1.4: An overview of CNT-based applications. (a) A 46 g light-emitting diode lit and suspended by two 24 µm-thick CNT fibers [150]. (b) CNTFET schematic with source/drain contacts and SiO_2 dielectric [151]. (c) Conceptual illustration of a CNT-based gas sensor implanted directly into a MEMS/CMOS chip with RF circuitry [152]. (d) Diagram of a SWCNT network suspended between two electrodes in an IR bolometric detector [110]. (e) Current mapping for the pressure sensing word "CNT" made by PDMS [153]. (f) Visual representation of a DNA detection scheme with CNT network [97]. (g) Illustration of folic acid-targeted cytosensing strategy for an enhanced electrochemical detection of cancer cells [119].

1.3.3 Synthesis methods

Arc-discharge [154], laser ablation [155] and chemical vapor deposition (CVD) [156] are the primary synthesis methods for CNTs. Among others, spray pyrolysis (modified CVD) [157] and gas-phase flame synthesis [158] methods are notable. CNTs were discovered by arc-discharge method. This method as well as laser ablation method need high temperatures, extensive processing for purification and sorting, which makes this low-throughput method very expensive for mass production. Moreover, these methods lack control over CNT characteristics and growth location. CVD method is the most preferred CNT synthesis method for high volume production as it does not have the limitations of the previous methods. CVD is also compatible with microfabrication process as it allows direct CNT growth on preferred substrates with certain control over the characteristics (e.g., structure, diameter, orientation) of the CNTs at relatively lower temperatures.

Thermal CVD is the most conventional CVD method, where CNTs are typically synthesized by thermal decomposition of a hydrocarbon gas on catalyst nanoparticles at 650-900 °C in a wide range of pressures, varying from a few millibars (mbar) to atmospheric pressure. CNTs are also grown at lower temperatures [159] with low pressure CVD (LPCVD), where the process is generally operated below 1 mbar. Another approach to lower the synthesis temperature is by using plasma enhanced CVD (PECVD), where the generated plasma facilitates gas decomposition, however, the incoming energetic ions also damage the synthesized CNTs during the process [160]. Also, overall quality of the resultant CNTs are compromised when they are grown at lower temperatures [161].

1.4 CNT integration in microsystems

CNTs require integration with a microsystem to utilize their potential as a sensing material in small and low-cost sensors. To demonstrate a sensing concept or for the performance development of a sensor, CNTs are often integrated in MEMS. However, a commercial smart sensor also demands on-chip integrated circuits for signal processing, which can be fulfilled by the matured and low-cost Si technology, CMOS. Therefore, a standard process for monolithic integration of CNTs and CMOS becomes important.

1.4.1 Different integration approaches

There are various approaches of integrating CNTs in a microsystem. Different methods of integration have their own benefits and challenges. Certain methods can be more suitable than others for specific applications. Therefore, the choice of integration method can depend on the intended application. For microsystem integration, CNTs can be grown separately at high temperatures and then transferred and assembled. The advantage of the post-growth processes is desired chemical modifications of the CNTs before deposition on CMOS at low temperatures. The typical method of transferring CNTs is based on wet process, where the two most used techniques are dielectrophoresis (DEP) [162–165] and solution-based deposition [108,166–168]. Process flow of these techniques are shown in *Figure 1.5*.

Deposited CNTs in these liquid suspension techniques often have poor bonding with the electrodes in addition to the risk of contamination during the extended process steps [169]. They also often suffer from issues related to non-uniform CNT assembly and misalignment [164,170]. Another challenge is to ensure uniform CNT dispersion in the solvent since CNTs tend to bundle together in the solution due strong interaction between them, formed due to van der Waals forces [52], which results in aggregation of the deposited CNTs that may cause system failure [108,171]. In addition, solution-based CNT deposition may require purchasing CNTs, which can be very expensive [172].

In a recent breakthrough on CNTFETs, Hills et al. [108] proposed a manufacturing methodology for CNTs which combines processing and circuit design techniques to overcome the major challenges related to liquid deposition methods for CNT integration in CMOS. However, the complex nature of this work on CNFET-based digital circuits requires defining a dedicated CMOS fabrication process involving materials such as Pt for metal contacts and HfO_x for passivation layers [108], which are not common in standard low-cost bulk CMOS processes. In the case of the DEP process, it provides better alignment and uniformity, but usually has low throughput and requires complex metallization processes to establish good contact between the CNTs and the electrodes [49]. Seichepine et al. [164] developed CNT integration in CMOS by DEP method with

high yield, where 80% of the electrode pairs in the 1024 array of devices only have 1–5 CNT connections per electrode pair; however, these CMOS chips still required extensive metallization post-processing [173].

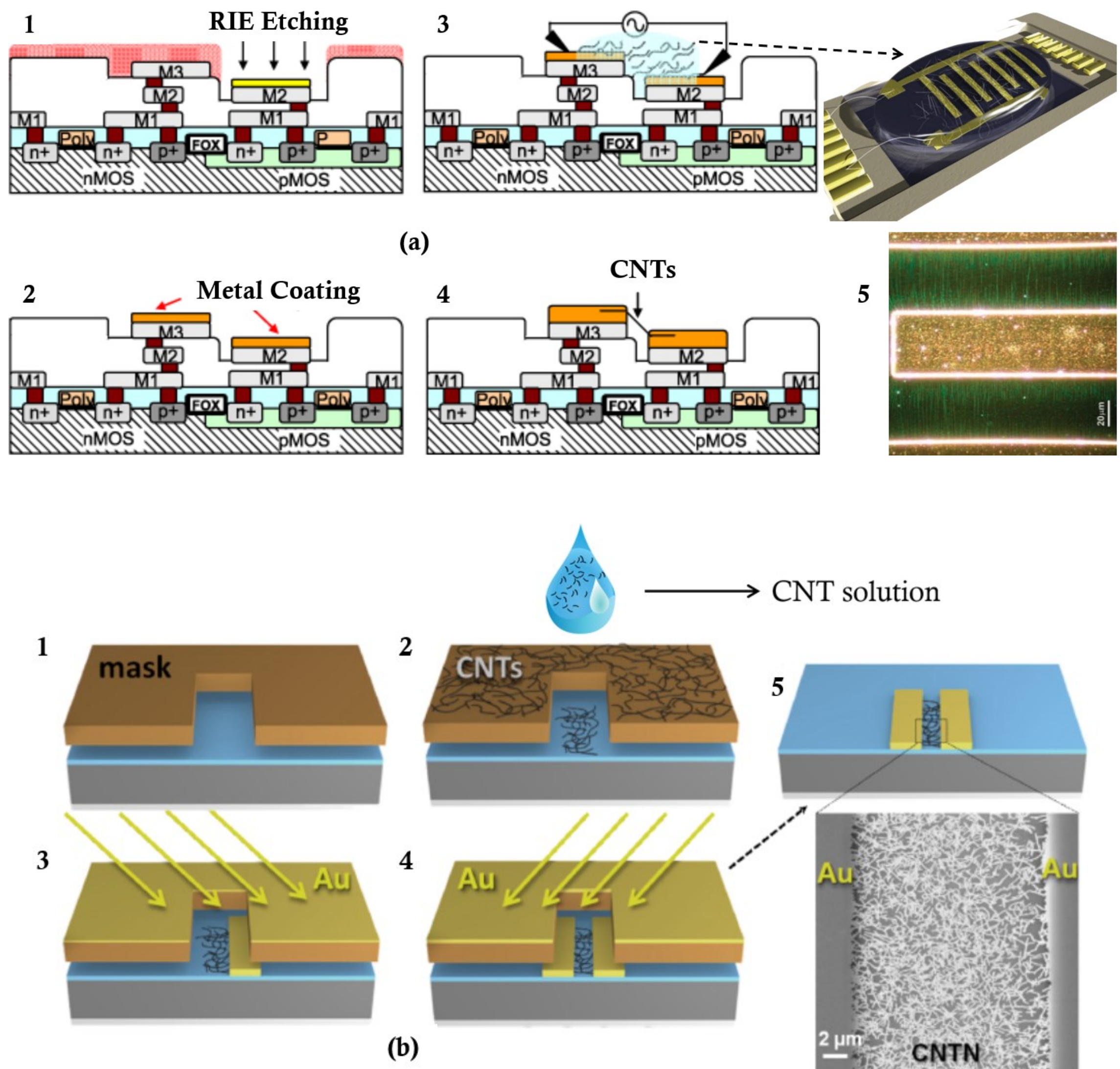


Figure 1.5: Liquid deposition methods. (a) A typical dielectrophoresis (DEP) process: (1) RIE etching to remove passivation layer on CMOS die, (2) electroless zincation process to remove aluminium oxide and to form a thin metal layer on top of the electrodes, (3) dielectrophoretic assembly to incorporate SWNTs onto CMOS circuitry, (4) the second electroless zincation process to improve the contacts between the CNTs and the metal electrodes, (5) deposited CNTs in between electrodes. Adapted from [165,174,175]. (b) A solution-based CNT deposition process: (1) application of a single shadow mask, (2) deposition by immersion in a solution containing dispersed CNTs, (3) & (4) defining source and drain electrodes by adjusting the metal deposition angle, (5) fabricated bottom-gate of CNT transistor and scanning electron micrograph of the CNT channel. Adapted from [169].

Another approach for CNT integration in a microsystem is by local CNT synthesis on desired microstructures. In this method, CNTs are grown by CVD process where only the growth region is heated. This process does not have the limitations of the wet deposition methods and ensures good structural quality of the synthesized CNTs, but the high growth temperature is the main restriction to obtain CMOS-compatibility in this process. And that is what we aim to solve in our approach of CMOS–CNT integration.

1.4.2 Local CNT synthesis on microstructures

CVD is the best approach for local CNT growth on microstructures, where only the microstructure is heated while the CVD chamber remains at room temperature. CNTs were directly synthesized on MEMS structures back in 2003 [176]. A process flow for locally growing CNTs on microstructures is presented in *Figure 1.6*. In this process, the fabricated microstructure (or microheater) is locally heated by joule heating to generate temperatures in the region of 650-900 ◦C. A pre-deposited thin catalyst layer (such as Fe, Ni, Co) on the microheater breaks into nanoparticles at such high temperatures, while a carbon-containing precursor gas enters the CVD chamber. CNTs start to grow on the microheater when the precursor gas interacts with the catalyst nanoparticles.

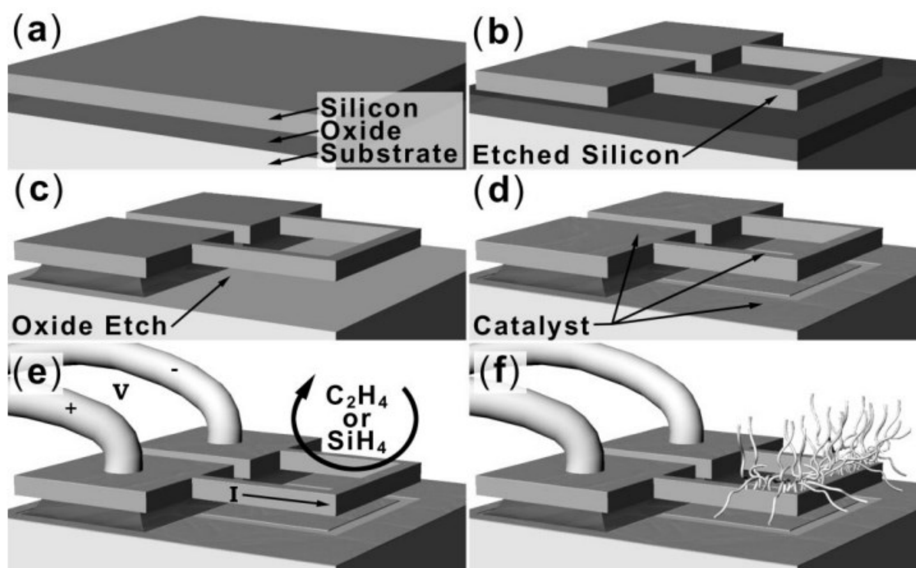


Figure 1.6: Process flow for CNT growth on MEMS. (a) Layers of wafer, (b) microstructure layer patterning and etching, (c) sacrificial oxide layer etching, (d) maskless catalyst deposition, (e) wire bonding on contact pads and joule heating in relevant gaseous ambient, (f) resulting carbon nanotubes. Adapted from [176].

In the CVD growth process, a catalyst is essential as CNT growth takes place on catalyst nanoparticles, the size of which mostly defines the diameter of the synthesized CNTs [177,178]. The catalyst can be deposited as a thin film, which breaks into nanoparticles on top of the microheater when local heat is applied. The deposited thin films are metastable and will spontaneously dewet (or agglomerate) to form small islands when heated at certain high temperatures (*Figure 1.7a*) due to surface energy minimization [179]. As the thickness of the film decreases, lower temperature is need for dewetting due to the acceleration in dewetting rate with reduction in film thickness [179], hence catalyst layer thickness can also impact diameter of the CNTs. Preformed catalyst nanoparticles can also be deposited to grow CNTs [180], but the process can be costly.

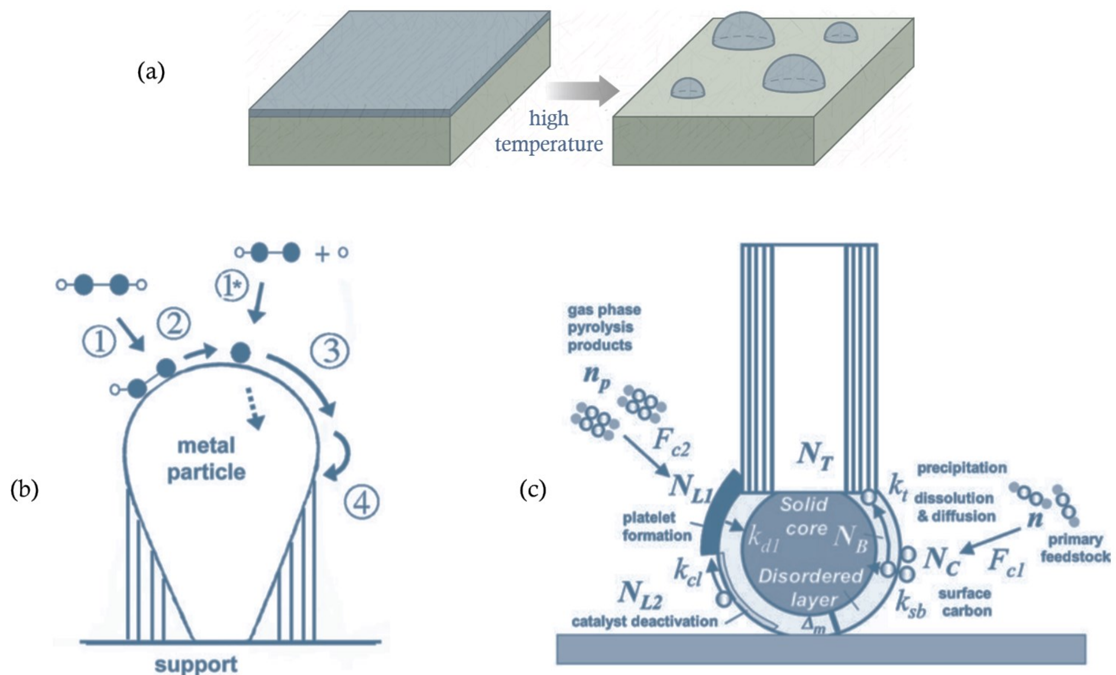


Figure 1.7: Dewetting of catalyst layer and CNT growth mechanisms. (a) Small island formation due to dewetting of thin film at high temperatures [179]. (b) Schematic of CNT tip-growth process: (1) adsorption of the gas precursor molecule on the catalyst surface, (2) dissociation of the precursor molecule, (3) diffusion of the carbon atoms in or on the catalyst particle, and (4) nucleation and incorporation of carbon into the growing structure [181]. (c) Schematic of a more complex mechanism of CNT base-growth process, explained in [182].

Apart from transforming catalyst thin film to nanoparticles, high temperature on the microheaters is required to provide essential thermal energy for the dissociation of

hydrocarbon gas molecules and the nucleation & growth of CNTs. Acetylene (C_2H_2) and ethylene (C_2H_4) are the most common carbon-containing precursor gas used for CNT synthesis in thermal CVD. The synthesis process starts with thermal decomposition of the precursor gas when the catalyst nanoparticles adsorb the gas molecules. The catalyst nanoparticles are the nucleation sites where carbon atoms diffuse and CNTs begin to grow with the thermal energy locally provided by the microheater. Typical activation energy for CNT nucleation in thermal CVD with C_2H_2 as precursor gas is 1.2–1.5 eV, although a significantly lower value of 0.9 eV is recently reported [183]. CNTs can nucleate and grow either from below (tip-growth) or above (base-growth) the catalyst nanoparticles depending on the interaction between the catalyst and the support layer [184]. Both CNT growth mechanisms are illustrated in *Figure 1.7b* and *1.7c*.

The growth process can be improved with inclusion of supporting gases such as Ar and H_2. There are numerous parameters that can affect the CNT synthesis process, which contributes to the fact that the underlying mechanisms of CNT growth are extremely complex and still not completely understood [184,185]. Catalyst material, support layer material, precursor gas, supporting gas, etching gas, concentration or mixing ratio of the gases, flow rates, temperature of growth location, thermal profile, annealing, pre-treatment of the catalyst layer, reactor type, process duration are the notable parameters that influence the CNT diameter, chirality, properties, quality, *etc*. Further details on some of these parameters are discussed in *chapter 5*.

1.4.3 Challenges of direct CNT growth on CMOS

Monolithic integration can be achieved if CNTs are directly synthesized on CMOS chips. However, a CMOS-compatible CNT synthesis process is very challenging. The major obstacles are limited material options, temperature restrictions, and microfabrication inflexibility in a standard CMOS process. In an industrial low-cost CMOS process, the material choices are often limited to silicon, silicon dioxide, silicon nitride, polysilicon, and metal interconnect layers such as Al or Cu; the conductive layer needed for localized heating is only provided by polysilicon and the metallization layers apart from the bulk silicon substrate. Thickness of these layers are also fixed for a certain CMOS technology;

hence, the sheet resistance of the polysilicon layers is already defined by the doping levels used in that process. Temperature limitations in CMOS is a major issue for directly growing CNTs, where the electronics cannot sustain temperatures above 300-400 ˚C for prolonged duration [186–188]. High temperature exposure may result in dopant re-diffusion in the active transistor regions and can cause electromigration in aluminium interconnects [189], triggering reliability issues and possible failure in the CMOS device. Growing CNTs (or nanomaterials in general) on chip at 650-900 ˚C, while keeping post-processing CMOS temperatures below 300 ˚C is very challenging [47,48,190]. In a dedicated MEMS process, microheaters can be thermally isolated by fabricating fully suspended heaters. However, fabrication processes in CMOS are stricter, where the process steps should not include any harsh chemicals or environment to keep the electronic interface safe. The challenges are further highlighted in [47,48,190].

CNTs have also been synthesized at low temperatures, mostly using PECVD and LPCVD methods [159,161,191]. However, reduction in temperature also lowers the CNT quality, growth rate and yield [161,190,191]. SWCNT growth is more challenging than MWCNTs at reduced temperatures [161]. A process development to overcome the limitations for low-temperature CNT growth is certainly an option for CMOS integration. For high temperature CNT synthesis, the local resistive heating method discussed in *section 1.4.2* is an excellent option, which is more suited for MEMS structures. Therefore, in our approach of monolithic CMOS-CNT integration, we aim to adapt the MEMS techniques by fabricating CMOS-MEMS microheaters, where CNT synthesis temperatures can be isolated to the local growth region.

1.4.4 CMOS-MEMS micromachined systems

There are numerous approaches of integrating MEMS and CMOS, which can mainly be classified into hybrid multi-chip and system-on-chip (SoC) integration solutions [192]. Hybrid multi-chip integration approach such as system-in-package (SiP) refers to the process where MEMS & CMOS chips are manufactured separately in their dedicated processes before the heterogeneous integration. In SiP, CNTs can be synthesized on MEMS chips and vertically stack them on chips containing ASICs to avoid direct CNT

growth on CMOS. However, additional time and cost for independent manufacturing of MEMS and CMOS chips together with their separate testing and hybrid packaging will cause hindrance for the commercial production of economically viable sensors. MEMS and CMOS structures are fabricated on the same substrate in SoC integration processes. SoC solutions are compact in size, cost-effective due to possible wafer-level packaging with low testing costs and provide high integration densities; however, the fabrication processes of these techniques can be challenging because of high complexity and low flexibility [192]. Considering the mentioned benefits and drawbacks of the integration approaches, SoC solution was preferred over SiP for our application.

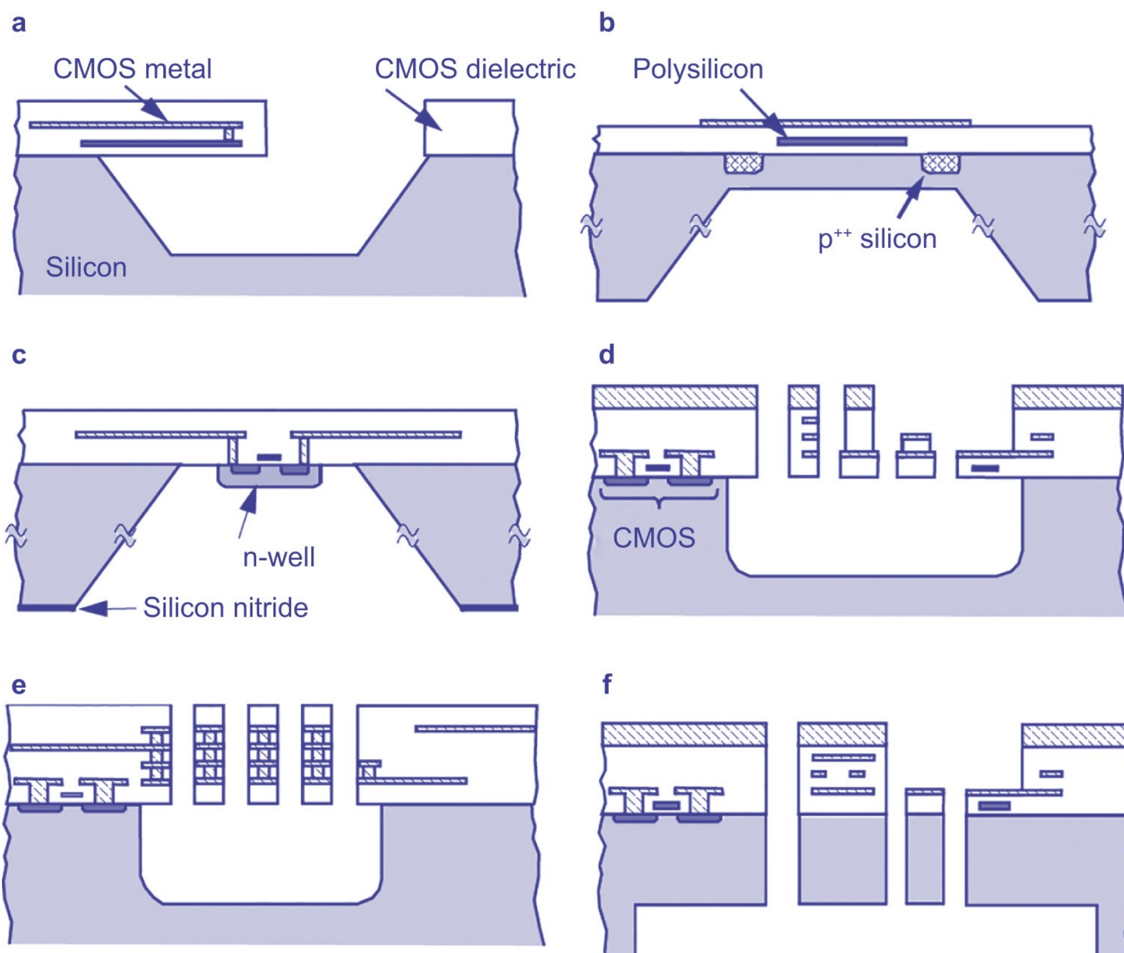


Figure 1.8: Various approaches of realizing CMOS-MEMS micromachined systems. (a) Frontside wet etching, (b) backside wet etching, (c) backside wet etching using an electrochemical etch stop, (d) frontside dry etching using a metal hard CMOS mask, (e) frontside dry etching using a photoresist mask, (f) front-and backside anisotropic deep-reactive ion etching (DRIE) [192].

Among the SoC solutions, monolithic integration of CMOS MEMS can be classified into pre-CMOS, intra-CMOS and post-CMOS approaches based on the formation order of the MEMS structures [193]. The latter approach is also known as CMOS-MEMS and has advantages over the other two approaches based on CMOS-compatibility, manufacturing costs and flexibility in design due to the convenience of choosing appropriate CMOS technology and foundry [192,193]. Therefore, we selected the CMOS-MEMS technique to fabricate microheaters in industrially manufactured CMOS chips for local CNT synthesis.

CMOS-MEMS structures are realized by bulk micromachining of an already fabricated IC substrate. Various approaches are used for necessary post-processing of the CMOS as illustrated in *Figure 1.8*. The CMOS-MEMS monolithic integration approaches allow compact chip design with high integration density and improved performance at a low cost. Another important benefit of this technique is that the devices can be implemented by the existing infrastructure of CMOS foundries with the current IC design tools. With the developments of IC and microfabrication technologies, CMOS-MEMS micromachined systems are gaining attention for developing various devices for numerous applications including commercial implementations [194–209]. A range of other recent works with this integration approach have been compiled in [210].

Many challenges can arise during the post-processing of the CMOS chips in the selected SoC CMOS-MEMS integration method, the challenges in our process development have been detailed in *chapter 4*. This integration solution has several mentioned benefits, but the process development takes longer time due to the involved complexity and low flexibility [192]. Although it is common to use bulk etching in this approach (*Figure 1.8*), we avoided that in our process to facilitate a simpler and cost-effective integration with minimum modification of an already operational CMOS foundry process flow.

1.4.5 Direct CMOS-CNT integration for sensing applications

A standard CMOS chip has polysilicon layers for constructing gates of the transistors and metal layers for routing electrical signals. Both of these layers can be used as heaters. However, based on the material properties suitable for efficient resistive heating along

with the temperature requirements in CNT synthesis, polysilicon is the better material option for the CMOS-MEMS microheater as detailed in *section 2.2*. The polysilicon layers in CMOS are covered with dielectric and passivation layers, which need to be selectively removed by the subtractive CMOS-MEMS microfabrication approach to make the polysilicon microheaters accessible for growing CNTs over them. The polysilicon CMOS-MEMS heaters may be fully or partially released by under-etching the dielectric layer beneath them. By generating the required high CNT synthesis temperature only at the growth location, low ambient temperature can be achieved. The concept is illustrated in *Figure 1.9*, where the exposed polysilicon microheater is heated through the wire bonded contact pads, while the CMOS circuits stay in a CMOS-compatible region.

CNTs can be locally synthesized on CMOS-MEMS microheater by thermal chemical vapor deposition (CVD) process, where the chamber remains at room temperature. During the CNT growth process, a local electric field can be generated between the growth structure and an adjacent microstructure to guide some synthesized CNTs towards that second microstructure for establishing connections [211]. A statistical analysis shows CNTs with small diameter (< 10 nm) are influenced more by the electric field [212]. Therefore, higher electric field between the microheater and the secondary electrode can influence the horizontal CNT growth to obtain more CNT connections between the electrodes (*Figure 1.9*). Once the CNTs are connected between the microstructures (or electrodes), a polysilicon-CNT-polysilicon network is formed, thus implementing a monolithic CMOS-CNT integration. The resistance of the connected CNTs can be monitored through the already bonded electrical wires on the contact pads of the electrodes. This configuration can be used for gas sensing due to their change in resistivity upon exposure to various gases. The synthesized CNTs can be functionalized to improve sensitivity and selectivity for target gases, where surface chemistry of the CNTs are influenced by coating them with nanoparticles [143–145]. Different metal (e.g., Pd, Pt, Sn) [213] and metal oxide (e.g., ZnO, TiO_2, Co_3O_4) [214] nanoparticles are the most common functionalization materials, which are typically deposited by thermal evaporation [215] and atomic layer deposition (ALD) [214] for locally grown suspended CNTs to detect various gas molecules [213].

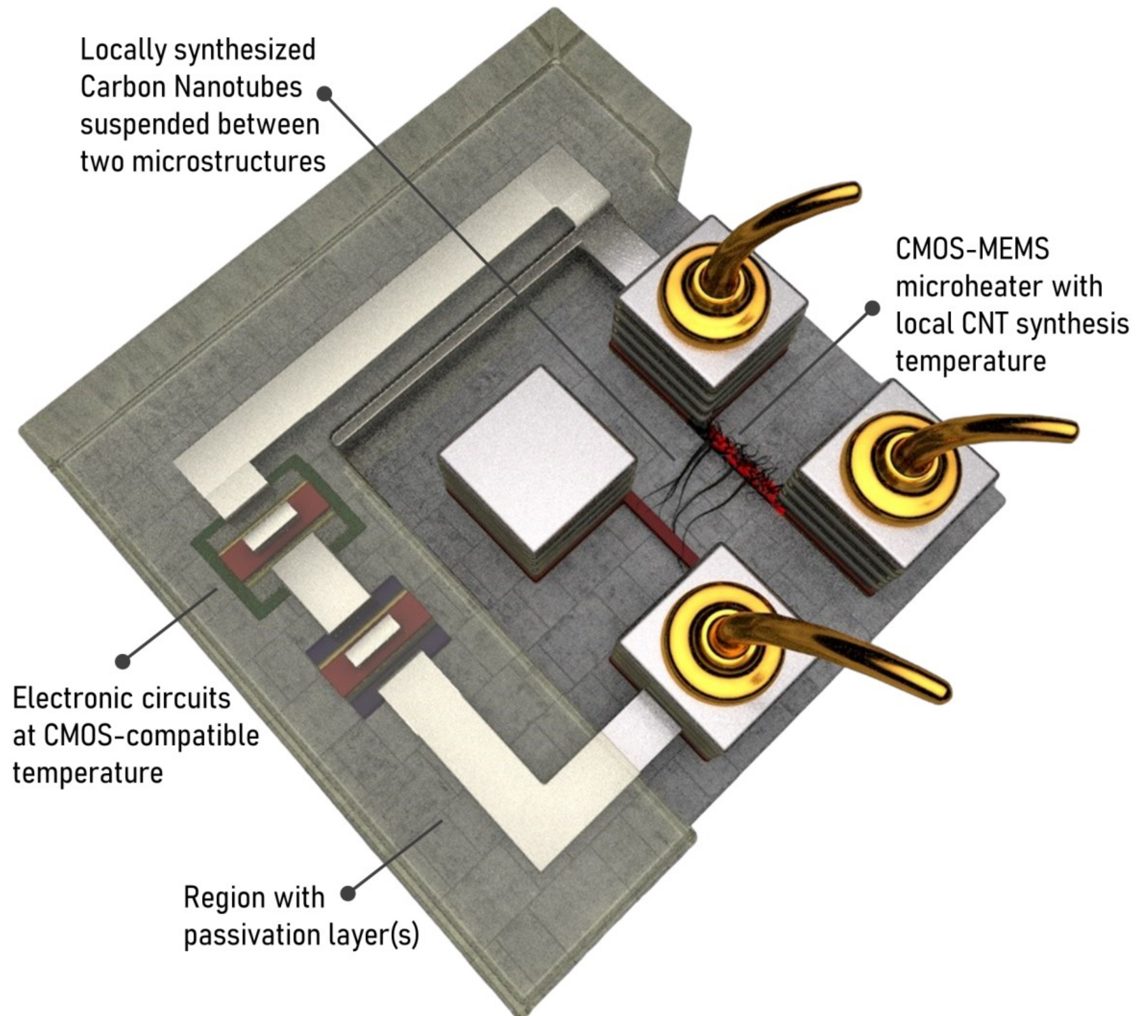


Figure 1.9: Concept of local CNT synthesis on CMOS-MEMS microheater at high temperatures with ICs at low ambient temperature.

1.4.6 Towards CNT-based commercial sensors

Extensive amount of work has been done on CNTs by M. S. Dresselhaus (earning her the title “Queen of Carbon”) and R. Saito [93,216–218] since its discovery. Due to its newly founded potentials, a group of H. Dai at Stanford University synthesized CNTs on micro catalytic islands by CVD method in 1998 with the vision of integrating them in conventional microstructures [219]. After a few years, another group of H. Dai also synthesized suspended CNTs on microstructures aligned by electric fields in MEMS [211] and a N-type MOS (NMOS) technology [220]. Although the process involved CMOS-incompatible substrate heating in a CVD furnace at near 900 ˚C, these works were the first to demonstrate monolithic integration of CNT with MEMS and MOS technology. In

2003, O. Englander, D. Christensen and L. Lin first demonstrated local CNT growth on MEMS structures by resistive heating [176]. E. Campbell's group have been contributing in CNT-related studies since 1999 [221], which involved local CNT growth on MEMS from 2006 by S. Dittmer et al. [222–224], indicating CMOS-compatibility. Another group from ETH Zurich, led by C. Hierold, has significant work related to suspended CNTs on MEMS [225–227]. At the University of South-Eastern Norway (USN), group of K. Aasmundtveit have numerous works on CNT integration in microsystems as summarized in a review, presented in *Article 4*, where B. Ta has contributed in the development of CNT synthesis in MEMS [89,212,228]. Some of these MEMS heaters were fabricated in SOI process, which allowed the design of a hole in the chip for S(T)EM (scanning electron microscopy, in transmission mode) imaging of CNTs as shown in *Figure 1.10*, revealing far more details than more common Secondary Electron SEM imaging.

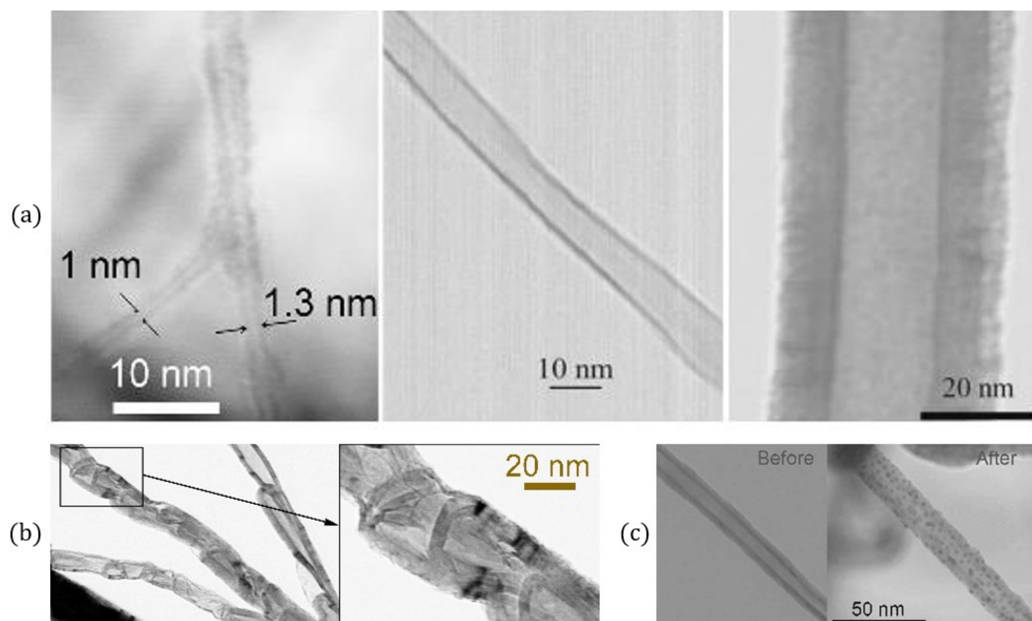


Figure 1.10: High-magnification CNT micrographs with S(T)EM in transmission mode: (a) individual CNTs [89,229], (b) bamboo-like CNTs [89], and (c) a pristine CNT (before) & a decorated CNT with Pd nanoparticles (after) [215].

To the best of the author's knowledge, only two groups have previously shown CMOS-compatible local CNT synthesis on CMOS structures. A group from the University of Cambridge are the first one to grow CNTs in a silicon-on-insulator (SOI) CMOS technology with tungsten microheaters as presented by F. Udrea et al. [230], which was

also the only resistive gas sensing demonstration of a CMOS-based sensor with locally grown CNTs. They also showed spectroscopic gas sensing in CMOS with locally grown CNTs as IR absorption layer [231]. This approach is a very good demonstration of local CNT synthesis for monolithic integration with CMOS, however, it is limited to more expensive SOI CMOS process [232] with tungsten metallization and involves complex bulk micromachining. The use of a refractory metal like tungsten is beneficial for high temperature CNT growth, but its utilization as interconnects (horizontal) is not common in foundry CMOS processes (especially in mixed-signal ICs) [49,190,233], where aluminium and copper are preferred, mostly due to their low resistivities. Moreover, the process involves selective backside bulk etching through a separate MEMS foundry [234,235], which reduces integration density and restricts the process to SOI CMOS substrates [49,190] beside adding cost and complexity. SOI CMOS process limits the scope for manufacturing low-cost CNT-based sensors, which is more desirable in an affordable bulk CMOS process.

H. Xie's group at University of Florida were the only one to locally grow CNTs on polysilicon microheaters, fabricated in a bulk CMOS process [236]. However, it involves various protracted post-CMOS processing steps before growing CNTs. In this approach, top metal layers made of Al were used as etching mask to protect CMOS circuits and the microheaters, which was then required to be etched by RIE. The process also includes two step frontside bulk silicon substrate etching involving both DRIE and RIE technique for anisotropic and isotropic etching to form cavities around microheaters. In addition, wet SiO_2 etching using buffered oxide etchant was performed, which can also etch any newly exposed aluminium layer during this dielectric etching step. Such extensive post-processing is difficult to accommodate in an already developed CMOS foundry process. Moreover, ICs need contact pads for establishing electrical connections by wire bonding, and these contact pads are made of the exposed metal layers (typically top metal); as the post-processing involves a step of etching the exposed metal layers, the contact pads will also be etched. The process does not use any external mask to pattern and protect the metal exposed layers. In the paper, it is unclear how the transistors were wire bonded (as illustrated in a schematic) for testing after the post-processing steps.

The scope for commercializing CNT-based sensors is high if a standard process can be developed to integrate CNTs with an existing low-cost IC manufacturing process [44,47,48,52,117]. We envision to incorporate the local CNT synthesis process in a low-cost industrial CMOS technology at the wafer-level. The direct CNT integration process would not be viable for mass production if extensive modifications are needed in an already developed foundry CMOS process. Therefore, our goal was to develop a simple post-processing method for fabricating CMOS-MEMS microheaters, where CNTs can be locally synthesized while maintaining low ambient temperature for CMOS-compatibility. The process steps should be compatible for transferring to the wafer-level, where CMOS, MEMS and CNTs are monolithically integrated, as illustrated in *Figure 1.11*.

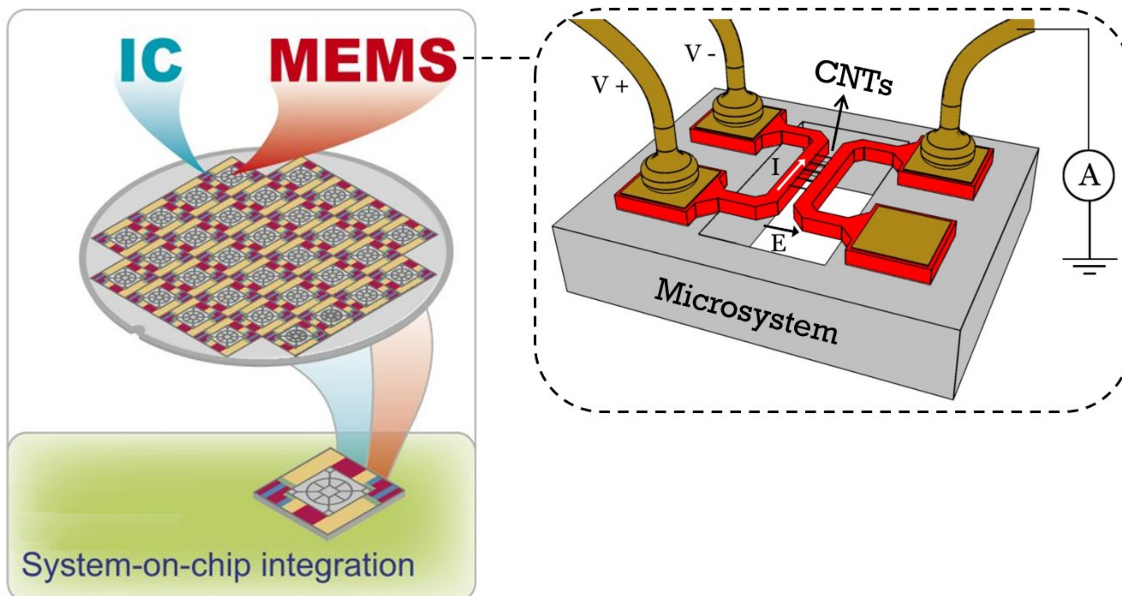


Figure 1.11: A concept for monolithic integration of CMOS, MEMS and CNTs at the wafer-level. Adapted from [192,237].

1.5 Research objectives and dissertation outline

The main goal of this project is to develop a process for locally growing CNTs on a low-cost industrial CMOS technology with the vision of enabling the pathway for commercial production of CNT-based sensors. Based on the objectives, the project can be divided into four significant stages. The first stage of the project involved feasibility analysis for realizing microheaters with CMOS materials that can locally generate up to 900 °C for

CNT synthesis, while the surrounding chip area remains at temperatures below 300 °C for CMOS-compatibility. It was done by analytical modelling and thermo-mechanical simulations, where suitable microheater dimensions were also analysed. This stage has been discussed in *chapter 2*. In the second stage, a CMOS chip was designed that contains several metal and polysilicon microheaters with various features to facilitate post-processing and CNT synthesis. The chip was designed in Cadence Virtuoso IC design tool and fabricated in a standard AMS 350 nm CMOS technology; details are presented in *chapter 3*. Focus of the stage three was realizing the CMOS-MEMS microheaters by necessary post-processing. Developing a suitable method of micromachining CMOS-MEMS heaters for high temperature applications was a crucial part of the project and a key step towards CNT synthesis in CMOS. The post-processing stage was challenging and most time-demanding part of the project, which is typical for SoC integration approaches [192]. An improved second chip was also designed and fabricated to facilitate the post-processing. Details of this stage is summarized in *chapter 4*, while some selective heaters from the new chip are presented in *section 3.3*. Fourth stage of the project was to locally grow CNTs on different CMOS-MEMS microheaters by thermal CVD process. The growth process itself was adapted from the earlier work of our group on MEMS-CNT integration (as introduced in *section 1.4.6*), while preliminary process developments were made for the CMOS-MEMS heaters to grow CNTs at lower temperatures, as discussed in *chapter 5*. As the objective was to directly transfer the developed growth settings for the MEMS heaters to the CMOS heaters without extensive development in growth process, in-depth characterization of the synthesized CNTs were not performed.

Beside the main objectives, CNT-based sensors were realized with the synthesized CNTs to demonstrate sensing applications, primarily for the purpose of gas sensing. To the best of the author's knowledge, this is the first reported demonstration of sensing applications (gas and pressure) with locally grown CNTs on the polysilicon layers of a bulk CMOS technology; results are shown in *chapter 6*. Synthesizing CNTs on CMOS layers is challenging and further developments are needed. The challenges and potential paths of resolving them to move towards wafer-level manufacturing are discussed in

chapter 7. Finally, on-chip temperature sensors are realized with the CMOS layers to estimate surrounding temperature of an active microheater when it is resistively heated to the maximum. Transistors are also characterized before and after operating some non-suspended polysilicon microheaters to CNT synthesis temperature for ensuring CMOS-compatibility. These results are presented in *chapter 8*.

Research contributions are made by publishing several articles on the obtained results. Some articles are in preparation phase, while some others are planned to be written. Significant results from these unpublished articles are also presented in this thesis. A list of the articles is provided in the thesis and the correlation of the articles with the thesis sections are shown in *Table 1.1*.

Table 1.1: Correlation between the thesis sections and relevant articles.

Summary of Thesis Sections	Relevant Articles
2. Feasibility Analysis for CNT Growth on CMOS	
2.2 CMOS materials for microheater design	Article 1 & 2
2.3 Microheater design considerations	Article 1 & 5
2.4 Thermo-mechanical analysis of microheaters	Article 1, 2 & 5
3. CMOS Chip Design	
3.2 Layout and micrographs	Article 2 & 6
3.3 Various microheater features	*Planned Article*
3.4 Microheater characterizations	*Planned Article*
3.5 IR microscopy	Article 2
4. Post-processing of CMOS-MEMS Microheaters	
4.2 Polysilicon microheater design layers	Article 3
4.3 Fabrication process of CMOS-MEMS heaters	Article 3
4.4 Post-processing challenges and heater design limitations	Article 3
4.5 Improved designs and post-processing	Article 3

Section	Article
4.6 RIE recipe development	Article 3 & *Planned Articles*
4.7 Microheater suspension	Article 3 & *Planned Articles*
4.8 Nickel electroplating on metal heaters	
5. CNT Synthesis on CMOS	
5.2 CNT growth process	Article 3 & 9
5.3 Effect of catalysts	*Planned Article*
5.4 Growth on different polysilicon microheaters	*Planned Article*
5.5 Growth on suspended microheaters	*Planned Article*
5.6 Effect of H2 in CNT synthesis	*Planned Article*
5.7 Resultant CNTs and defects	*Planned Article*
6. Sensing Applications	
6.2 CNT growth towards adjacent heater	Article 9
6.3 CNT connections and I-V curves	Article 9
6.4 Gas sensing	Article 9
6.5 Pressure response	*Planned Article*
7. CMOS Microheater Challenges and Wafer-level Scaling	
7.2 Electrical control and temperature limitations	*Planned Article*
7.3 Heater damages	*Planned Articles*
7.4 CNT growth development	*Planned Articles*
7.5 Towards wafer-level process for mass production	*Planned Article*
8. On-chip Temperature Sensing & Transistor Characterization	
8.2 Characterization of reference microstructures	Article 7
8.3 Sensor testing with on-chip microheaters	Article 7
8.4 Effect of convection	*Planned Article*
8.5 Effect of partially broken microheaters	*Planned Article*
8.6 Effect of CMOS microheaters on transistor characteristics	Article 9

N.B.: Article 4 and 8 are review papers.

Chapter 2

Feasibility Analysis for CNT Growth on CMOS

2.1 Introduction

Direct CNT synthesis on CMOS chips are much more challenging than on MEMS. Local CNT growth on a microsystem using CVD technique requires a microheater to generate a hotspot with temperature up to 900 ˚C. In a dedicated MEMS process, a material with desired properties can be deposited to fabricate the microheater. Furthermore, the microheater can be fully suspended to thermally isolate the heating region. However, this is not the case for CMOS since standard IC fabrication processes are not intended for implementing mechanical structures. In CMOS, the material options are limited, while the typical IC foundry processes do not offer suspension of microstructures. One key requirement in CMOS is the temperature compatibility that indicates the transistor regions should be below 300 ˚C during any post-CMOS processing. As a result, any microheater that generates high temperatures in CMOS need to ensure high thermal gradient around it for CMOS-compatible ambient temperature. Therefore, it is important to check the feasibility of using CMOS layers as microheaters for high temperature applications like CNT synthesis. Thus, suitable material options in CMOS were investigated, analytical models were made to specify the desired material properties and dimensions of the microheaters, and thermo-mechanical simulations were performed. Results from this chapter are published in *Article 1, 2* and *5*.

2.2 CMOS materials for microheater design

A standard CMOS process offers polysilicon and metal interconnecting layers that can be used to realize microheaters. Aluminium and copper are commonly used for metallization in typical CMOS technologies. These metals, however, are not suitable to serve as microheaters (for CNT growth) in their original form due to low electrical resistivity and high thermal conductivity. Moreover, Al melts at ~660 ˚C, which is far less

than the required 900 ˚C CNT synthesis temperature. Therefore, beside the polysilicon option, different binary alloys containing Al or Cu with suitable material properties were investigated.

An analytical model was established to obtain a better perspective of the material properties required for an efficient microheater. According to Fourier's law of thermal conduction, one-dimensional conductive heat transfer (Q_x) is defined as:

$$Q_x = -\,kA(\frac{dT}{dx}) \tag{1}$$

where k is the thermal conductivity of the material, A is the cross-sectional area (normal to the heat flow direction), and dT/dx is the temperature gradient in the direction of heat flow (along the microheater length in this case). The negative sign indicates that the heat flow is in the opposite direction of the thermal gradient.

The local CNT synthesis temperature was generated by joule heating, where an electrical current is passed through a conductor to produce the heat. Electrical power (P) dissipation for heating a considered length (l_x) of the microheater can be expressed as:

$$P = \frac{\rho I^2 l_x}{A} \tag{2}$$

where I is the applied current to the microheater, ρ is the microheater electrical resistivity, and A is the microheater cross-sectional area.

In this study, only conductive heat transfer was considered, neglecting convection and radiation due their minimal effect in micro scale compared to conduction. The nature of convection can be realized by Rayleigh number (Ra), where higher value of Ra indicates more influence of convective heat transfer, and it was shown that Ra decreases significantly for microscopic structures compared to macroscopic structures; thereby, the effect of convection becomes negligible at the micro level [238]. It was also derived that the heat loss on microstructures due to thermal radiation is less than 1%, even for temperature as high as 1000 ˚C [238]. Therefore, the dissipated electrical power in

resistive heating can be converted to heat by Fourier's law of heat conduction, and the following expression can be deduced from equation *(1)* and *(2)*:

$$dT = \frac{\rho I^2 l_x}{kA^2} dx \tag{3}$$

For a rectangular microheater, maximum temperature is generated at the centre of the heater and gradually reduces along its length. An expression for the maximum microheater temperature (T) can be derived by considering $l_x = l/2 - x$, where l is the total microheater length. For this condition, following expressions can be written:

$$\int_{T_0}^{T} dT = \frac{I^2 \rho}{kw^2 t^2} \int_0^{l/2} (\frac{l}{2} - x)\, dx \tag{4}$$

$$T = T_0 + \frac{I^2 l^2 \rho}{8w^2 t^2 k} \tag{5}$$

where T_0 is ambient temperature and w & t are heater width & thickness, respectively.

Materials for the microheaters should have high electrical resistivity (ρ) for efficient heating and low thermal conductivity (k) to reduce heat loss in the surroundings. In terms of material parameters, the ratio ρ/k is an important factor to effectively obtain high temperatures on the microheaters by resistive heating. This ratio is proportional to the maximum temperature on the microheater, as shown in Equation (5); hence, a high value of this ratio is desirable.

Alloys provide higher electrical resistivity and lower thermal conductivity than the native form of the involved metals, so higher ρ/k ratio can be obtained. Based on this ratio, nickel turned out to be the most suitable alloying material for both Cu and Al, as detailed in *Article 1* and *Article 2*, respectively. Different Cu–Ni and Al–Ni alloys were investigated; the most suitable options are compared in *Table 2.1* and *Table 2.2*.

In equation *(5)*, length (l) and width (w) of the microheater are defined by the design; current (I) is a variable during the joule heating process, and the heater thickness (t) and material properties (ρ, k) are CMOS-process-dependent parameters. The ratio ρ/t^2k

from the equation is directly proportional to the maximum microheater temperature. Although the value of this ratio depends on the CMOS process, it is modified for the metal microheaters when they are transformed into alloys. Also, the final thickness of the metal microheaters depend on the alloy composition. Therefore, this ratio is plotted in *Figure 2.1* for five different potential materials from *Table 2.1* and *Table 2.2*. The corresponding values of ρ and k are at CNT synthesis temperature (~900 ˚C). Thickness of the alloys are calculated based on a 0.6 µm thick Al or Cu layer, where atomic weights and mass densities of the associated materials are taken into account. A higher value of the ratio ρ/t^2k corresponds to a more efficient microheater, allowing room for reducing the l/w ratio to achieve mechanically more robust designs for suspended heaters. Based on the plot in *Figure 2.1*, Cu (70%)–Ni (30%) and Ni_3Al alloys are the most suitable metal microheater materials among the available options in CMOS for CNT synthesis. Alloys give better performance in this application but require post-processing such as metal deposition and annealing.

Table 2.1: Comparison between material properties of Cu and relevant Cu–Ni alloys [239,240].

Metal Alloy (composition, at.%)	Melting Point (°C)	Electrical Resistivity, ρ ($\times10^{-8}$ Ωm)	Thermal Conductivity, k ($Wm^{-1}K^{-1}$)	Ratio, ρ/k ($\times10^{-8}$ Ωm^2W^{-1} K)
Cu	1080	8.5	340	0.025
Cu–Ni (40%/60%)	1200	54.5	49.3	1.105
Cu–Ni (70%/30%)	1150	39	60.5	0.645

Table 2.2: Comparison between material properties of Al and relevant Al–Ni alloys [239–242].

Metal Alloy (composition, at.%)	Melting Point (°C)	Electrical Resistivity, ρ ($\times10^{-8}$ Ωm)	Thermal Conductivity, k ($Wm^{-1}K^{-1}$)	Ratio, ρ/k ($\times10^{-8}$ Ωm^2W^{-1} K)
Al	650	10.5	200	0.053
Al–Ni (50%/50%)	1680	10	72	0.139
Ni_3Al (75%/25%)	1400	73	36	2.028

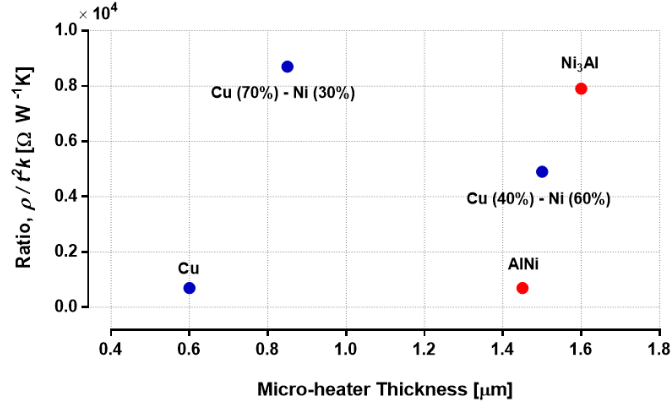


Figure 2.1: Influential ratio (ρ/t^2k) for maximum microheater temperature plotted against total microheater thickness associated with the material.

Polysilicon has a very high melting point (> 1400 ˚C). Since the polysilicon layers in CMOS are doped, the sheet resistance will depend on the specific process. However, typical ρ/k ratio of polysilicon is much higher than the metal options, making it the most suitable material in CMOS for the microheater application of local CNT synthesis. However, the choice between metal and polysilicon microheaters should be based on suitability in CMOS post-processing.

2.3 Microheater design considerations

The microheaters should have high resistance and minimized power consumption. Beside the material properties, dimensions of the microheaters are important parameters that define its performance. Thickness of the CMOS layers is process-dependent, hence fixed for each CMOS technology, which contributes to the challenges of implementing an effective microheater. To obtain high thermal gradient around a microheater, it may require to be fully or partially suspended. Therefore, microheater design considerations should include maintaining CMOS compatible temperature in the circuit region and ensuring mechanical stability of the suspended designs.

Suspended microheater designs may suffer from thermomechanical stress, which can lead to the heater deformation due to stiction and buckling. Vertically deformed microheaters may touch the substrate and directly conduct heat to the microsystem. Horizontally deformed microheaters may cause stress on the connected CNTs and

connections can break off. Therefore, minimizing the effect of stiction and buckling is important to avoid significant microheater deformation in any direction.

Stiction would mainly depend on the wet dielectric etching process. To release the microheaters, thin dielectric layer in between the microheater and substrate needs to be etched by wet etching. Hence, there can be a solid-liquid-solid interface because of residual etchant from the process, which may result in stiction due to capillary forces [243]. This adhesion force, F_c can be expressed as:

$$F_c = \frac{2\, A\, \gamma_{la}\, cos\theta_c}{d} \tag{6}$$

where A is the wetted surface area, γ_{la} is surface tension at liquid-air interface, θ_c is the contact angle at liquid-solid interface and d is the thickness of the liquid layer.

At any contact angle less than 90° between the wet etchant and the microheater, stiction may take place due to the adhesion force on the microheater. Thinner dielectric layer beneath the microheater, which is required to be etched for realizing suspended designs, will increase this force. In CMOS, typical dielectric layer underneath the metal layers are significantly thicker compared to that of the polysilicon layers. Therefore, metal microheaters should have lower chance of stiction. From design viewpoint, microheater length and width should be minimized to reduce the wetted surface area, thus reducing the possibility of stiction during the wet dielectric etching process.

High coefficient of thermal expansion (CTE) of the microheater materials facilitates buckling. Temperature for CNT synthesis will cause thermal stress on the microheaters, mostly due to longitudinal thermal expansion. Following expression for the induced load (F_{TL}) due to such stress is found from the relationship between stress and strain in the elastic region (Hooke's law) and their basic definitions:

$$F_{TL} = \mathrm{E}\frac{\Delta L}{L}\mathrm{wt} \tag{7}$$

where E is the Young's modulus, ΔL is change in length due to thermal expansion, L is initial microheater length and w, t are the width and thickness, respectively.

The linear thermal expansion coefficient (α) along the length due to change in temperature *(ΔT)* is defined as:

$$\alpha = \frac{\Delta L}{L} / \Delta T \tag{8}$$

From equation *(7)* and *(8)*, load on the microheater due to longitudinal thermal expansion can be expressed by the following equation:

$$F_{TL} = Ewt\alpha\Delta T \tag{9}$$

Euler's formula for critical buckling load (F_{CR}) provides the maximum axial load that an ideal beam can endure without buckling. The formula is expressed as:

$$F_{CR} = \frac{\pi^2 EI}{(KL)^2} \tag{10}$$

where I is moment of inertia of the cross-sectional area of the microheater, K is column effective length factor and other symbols indicate previously mentioned meanings.

For a rectangular shaped structure with a width larger than thickness, the area moment of inertia is $wt^3/12$ and for a structure with both ends fixed, the column effective length factor is 0.5. Therefore, for the rectangular microheater, equation *(10)* becomes:

$$F_{CR} = \frac{\pi^2 Ewt^3}{3L^2} \tag{11}$$

Since the microheater load is caused by thermal stress, the induced load due to thermal stress (F_{TL}) is equal to the critical buckling load (F_{CR}). Therefore, the following equation for critical buckling length (L_{CR}) can be derived by equating equation *(9)* & *(11)*:

$$L_{CR} = \sqrt{\frac{\pi^2 t^2}{3\alpha\Delta T}} \tag{12}$$

Critical buckling lengths have been calculated using equation *(12)* and under-etched length of the suspended microheaters have been kept below the critical buckling lengths to reduce the effect of buckling.

Maximum thermal gradient around the microheaters can be reached by completely etching the dielectric layer underneath those growth structures; however, the microheaters would suffer from undesirable mechanical deformation. Therefore, it is beneficial to keep some dielectric layer underneath the microheaters as a mechanical support. Having dielectric support underneath also means a heat conduction path to the bulk of the chip. It is trade-off between achieving a high thermal gradient and the keeping mechanical integrity of the microheater. So, the goal is to under-etch a sufficient amount of dielectric to get the required thermal isolation for maintaining CMOS-compatible temperatures, while avoiding destructive microheater deformation. Depending on the heater dimension, microheaters can also be kept non-suspended. The non-suspended microheaters will have lower thermal isolation, but mechanical stability will not be a concern for them.

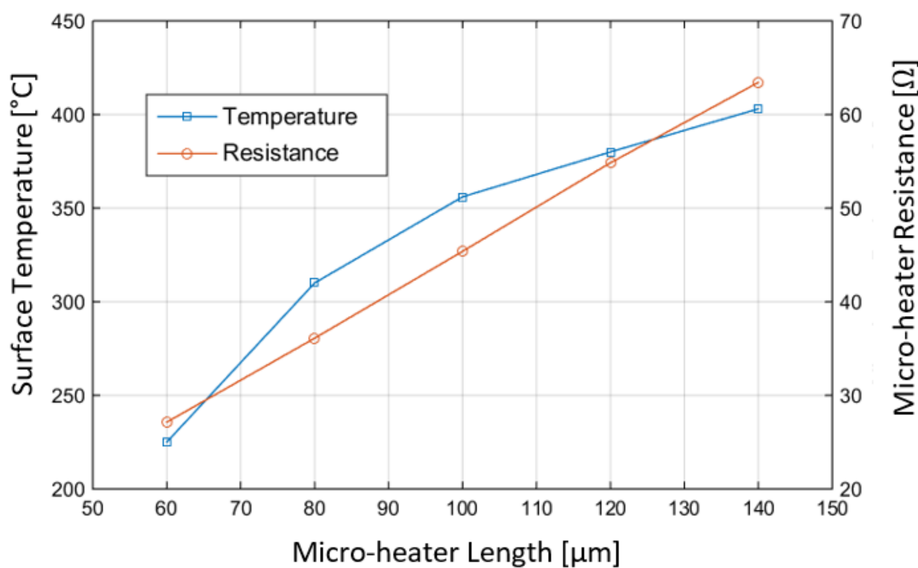


Figure 2.2: Effect of length variation for non-suspended Cu-Ni microheater.

The microheater surface area is directly proportional to the amount of conductive heat transfer in the surroundings, as specified in equation *(1)*. Hence, length and width of the non-suspended microheaters should be minimized from the heat conduction perspective. Minimum microheater length is the distance between two contact pads, which is considered 30 µm to keep sufficient space for wire bonding. Minimum width in CMOS is process-dependent, and typically can be below 1 µm. So, minimum microheater

width of 1 μm is considered. Optimum power consumption can be achieved by keeping the microheater dimensions minimum. Meanwhile, the microheater resistance should be sufficiently high so that maximum power is consumed by the heater during the joule heating, with low power loss at the remaining of the heater circuit. It should be noted that metal heaters such as cupronickel has low resistivity compared to polysilicon; hence, the microheater resistance may need to be increased by length extension. Length extension will rise heat conduction in the microchip, especially for non-suspended designs. *Figure 2.2* shows the variation of microheater resistance and CMOS surface temperature with the length variation of non-suspended cupronickel microheater.

2.4 Thermo-mechanical analysis of microheaters

We designed several microstructures suitable for CNT synthesis, using the compatible materials (polysilicon, Al–Ni, and Cu–Ni alloys) in CMOS and performed thermomechanical analyses with the Multiphysics simulation software, ANSYS. The tables in *Article 1* provide a range of simulation parameters. Most of these designs involve partially suspended microstructures (PSMs) to balance mechanical stability and high thermal isolation. A few designs involve fully suspended microstructures or no suspension at all.

The polysilicon microheaters are designed with two different layers: poly-1 and poly-2. In the simulations, the considered sheet resistances of poly-1 and poly-2 are ~6 Ω/sq and ~18 Ω/sq, respectively. All polysilicon heaters are simulated with 0.85 μm thickness, even though their actual thickness in a CMOS process will be 3–4 times lower. Therefore, the polysilicon heaters will have higher resistance in practice, which is beneficial for resistive heating. In the finite element method (FEM) simulations, higher polysilicon thickness helps to reduce the number of elements for meshing and, consequently, limits the processing time of each simulation.

The microheaters can be partially suspended along their entire length; *Figure 2.3* reveals the suspended and non-suspended areas. *Figure 2.3a* illustrates the microheater surface area, which was divided into three regions. Two PSM designs are presented, where

region C is non-suspended and region B is suspended in both designs. A cross-sectional illustration of non-suspended and suspended microheater areas is shown in *Figure 2.3b* and *Figure 2.3c*, respectively. The non-suspended regions have a dielectric layer underneath that mechanically supports the microheater.

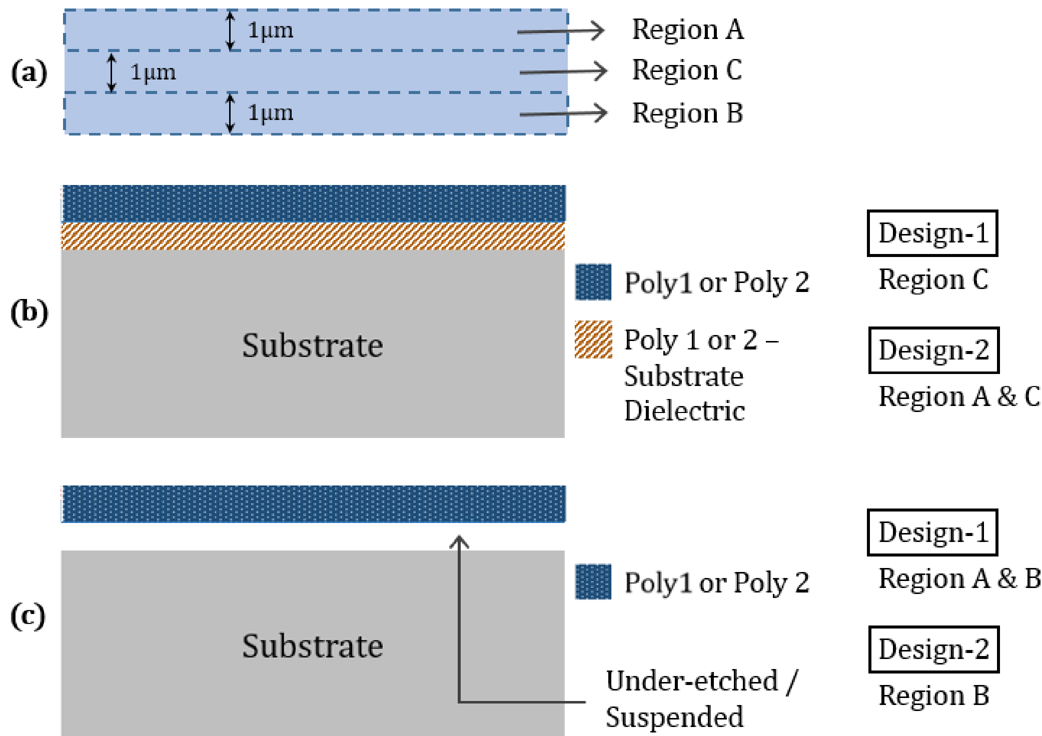


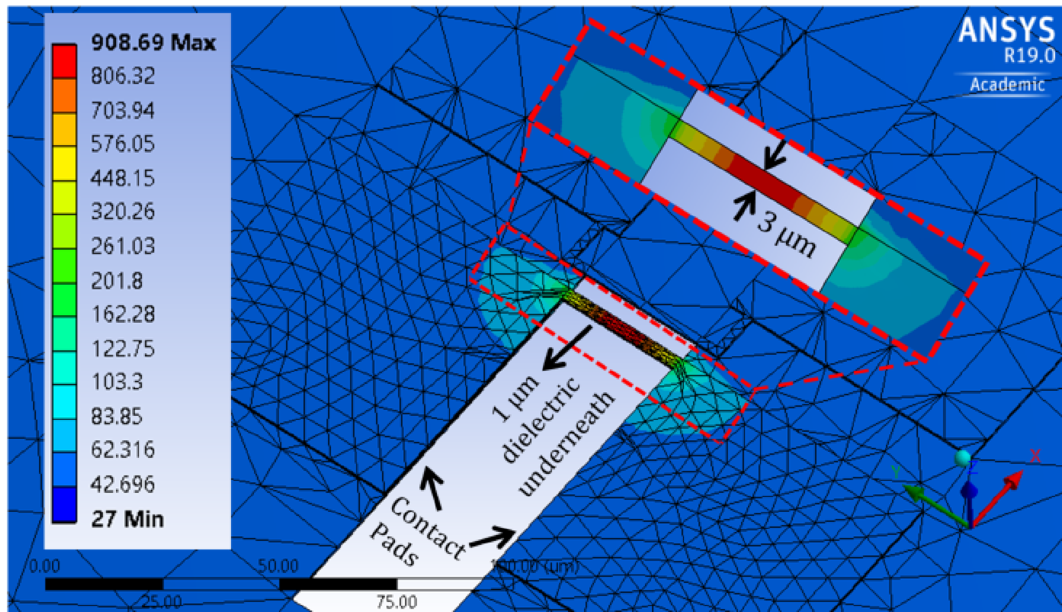
Figure 2.3: Partially suspended polysilicon microheater design illustrations. (a) Microheater surface area; (b) cross-sectional view of non-suspended region, and (c) cross-sectional view of suspended region.

2.4.1 Polysilicon microheaters

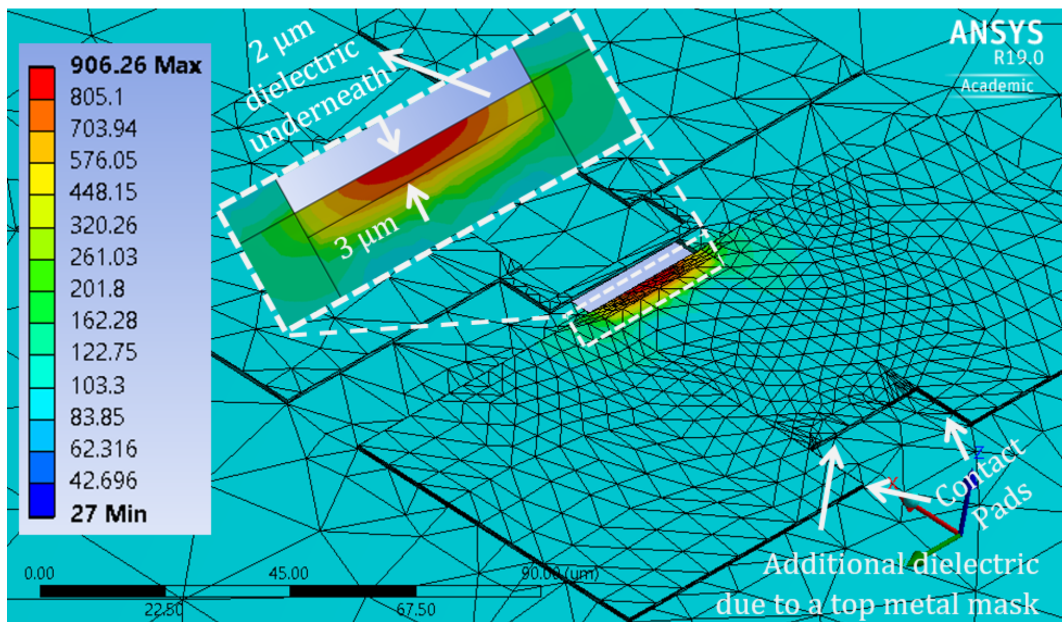
The designed polysilicon PSMs are 30 µm long and 3 µm wide, giving around 60 Ω and 180 Ω resistance to poly-1 and poly-2 heaters, respectively, when they reach the CNT synthesis temperature. In these models, both region A and B are suspended, keeping dielectric support in region C for design-1, while only region A is suspended for design-2. In design-2, region B can be blocked from under-etching by putting a mask using the top metal layers of the CMOS design on one side of the microheater.

Figure 2.4 shows the thermal simulation results for both designs, where poly-1 was used as the heater material. The microheaters locally generate the required CNT synthesis

temperature in their centres. Design-1 (*Figure 2.4a*) achieves a high thermal gradient around the heater due to the 1 µm dielectric etching on both sides (region A & B) of the 3 µm wide heater, leaving 1 µm wide dielectric layer in the middle (region C). Design-2



(a)



(b)

Figure 2.4: Thermal–electric simulation results of poly-1 partially suspended microheater (PSM) designs: (a) design-1 and (b) design-2.

(*Figure 2.4b*) has a 1 µm wide suspension on one side of the heater (region B), leaving a 2 µm wide dielectric layer (region A and C) underneath the heater. Suspended microheater regions produce a higher thermal gradient around them. Therefore, the microheater in design-2 has lower thermal isolation than the microheater in design-1. Moreover, since a top metal layer blocks heater under-etching on one side (region A), the dielectric layer will remain in the blocked region near that side of the heater, as indicated in *Figure 2.4b*, creating more heat-conduction paths. Even with lower thermal isolation of the heater, the average surrounding surface temperature in design-2 is near 100 °C. Therefore, both poly-1 PSM designs maintain the CMOS-compatible temperature in the chip, while producing a local hotspot for CNT synthesis. From a mechanical viewpoint, design-2 is preferable over design-1, as it involves less dielectric etching underneath the heater. In terms of power consumption, design-1 (~35 mW) is more efficient than design-2 (~80 mW).

The plots in *Figure 2.5* show the thermal-simulation results of poly-2 microheaters for both design-1 and design-2. Temperatures along the length of the heaters are plotted in *Figure 2.5a*. The graphs form parabolic shapes, as predicted by equation *(5)*, with the maximum temperature (~900 °C) at the centre of the heaters, while CMOS-compatible temperatures are reached even at both ends of the heaters. The power requirements for these heaters are similar to the corresponding poly-1 designs. Plots in *Figure 2.5b* indicate the temperature drops when moving away from the heaters. High thermal gradient around the heaters is apparent in the plots. Surface temperature in design-1 reaches ~50 °C, within 2 µm away from the heater, achieving an average thermal gradient of 425 °C per micrometre around the heater. In design-2, the surface temperature becomes ~100 °C, within 8 µm away from the heater, indicating an average thermal gradient of 100 °C per micrometre around the heater.

Two polysilicon microheaters were modelled with a reduced length of 6 µm for simulating non-suspended and fully suspended designs. The widths of the non-suspended and fully suspended designs are 1 and 2 µm, respectively. The reduced length for a fully suspended microheater offers lower risk of deformation. Although it may still

suffer from buckling and stiction, the width of this design was extended to 2 µm for improving mechanical steadiness. At around 900 °C, resistances of fully suspended and non-suspended designs are ~55 Ω and ~110 Ω, respectively.

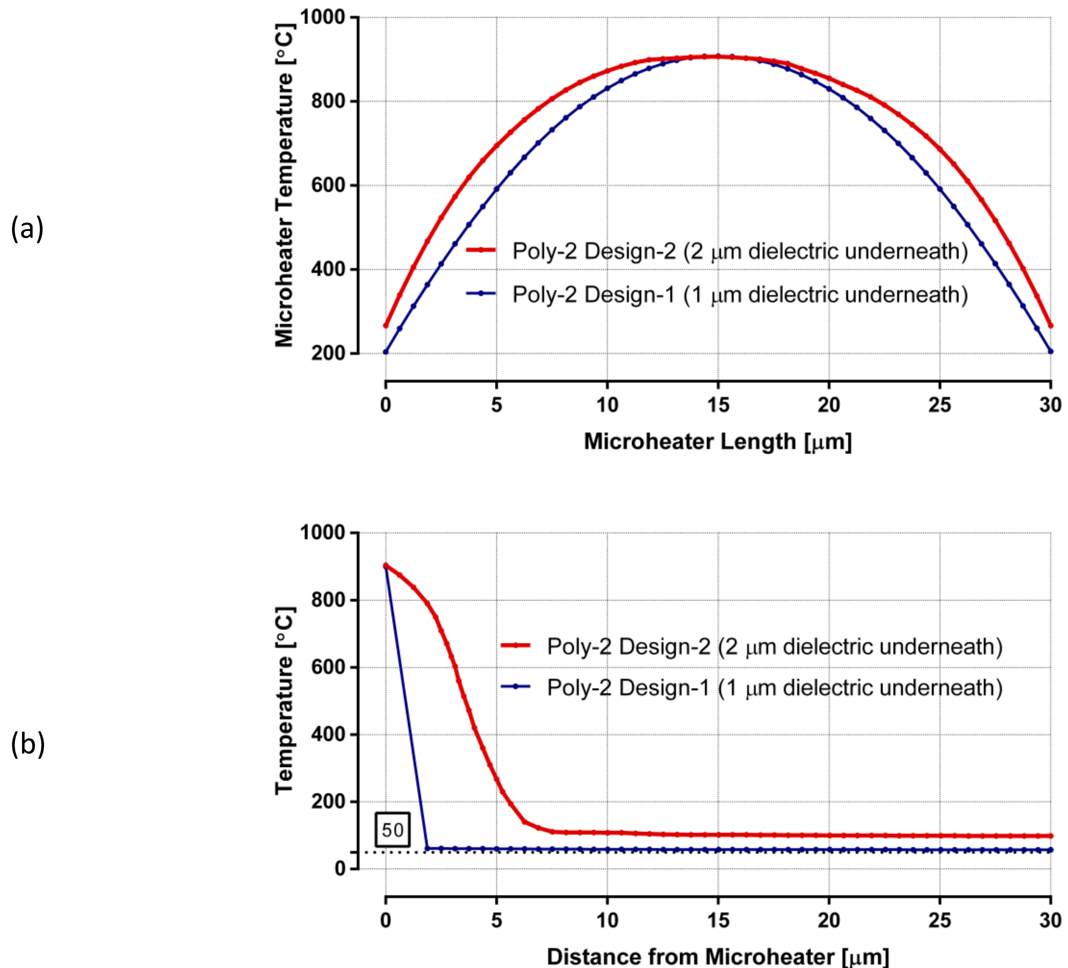


Figure 2.5: Thermal analysis of partially suspended poly-2 designs: (a) microheater temperature along its length; (b) temperature distribution from the centre of the heater to the surrounding surface.

These microheaters are only designed with poly-2 layer since it has higher electrical resistivity among the polysilicon options. Thermal responses of both non-suspended and fully suspended designs are plotted in *Figure 2.6*. Plots in *Figure 2.6a* present the temperatures of the heaters, both having a 2 µm long region in the centre, where the heaters reach more than 800 °C, an optimum region to grow low-diameter CNTs. Plots in *Figure 2.6b* show that the average surrounding chip temperature reaches far below CMOS-compatible temperature for both designs. Both designs have a very high thermal

gradient around the heaters, indicated by the sharp temperature decrease. They also have a similar power requirement of ~20 mW. The non-suspended heater is a clear favourite among these designs, as it avoids mechanical deformation and does not require any dielectric under-etching steps during the CMOS post-processing.

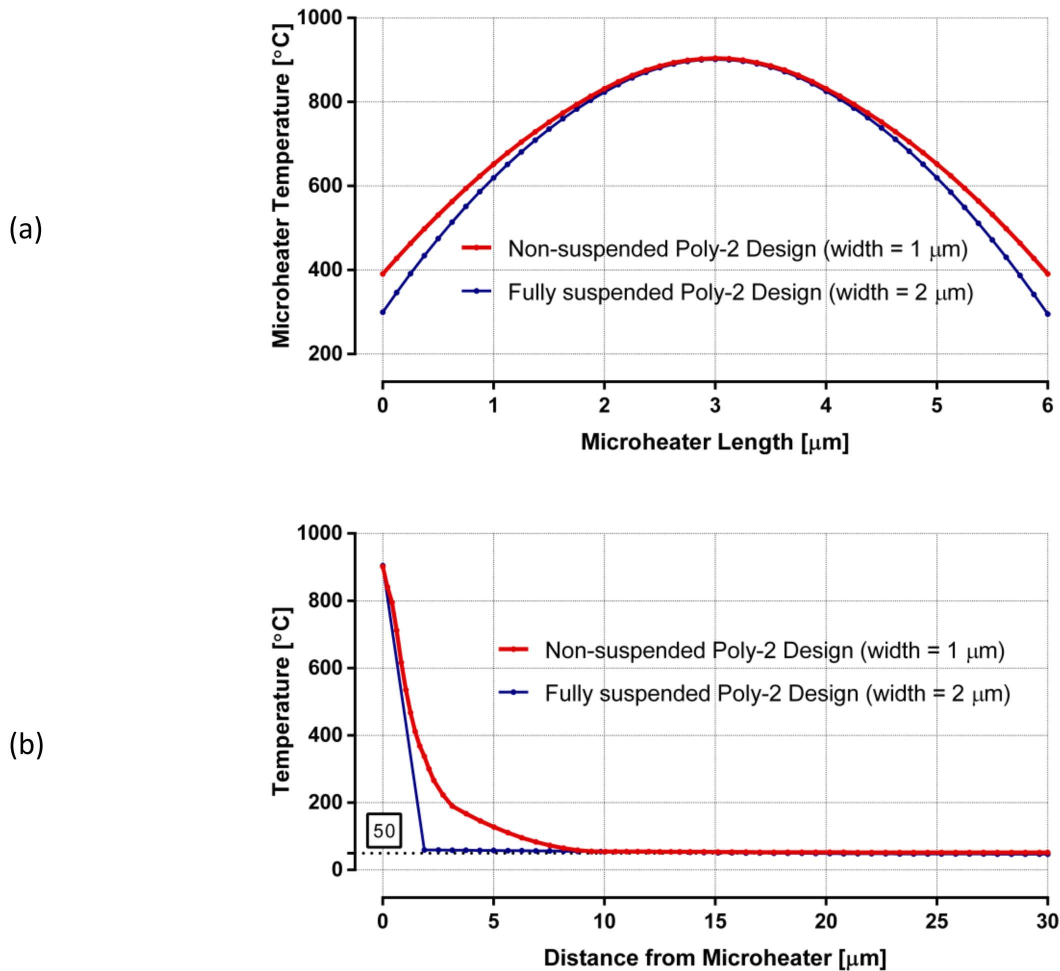


Figure 2.6: Thermal analysis of non-suspended and fully suspended poly-2 designs: (a) microheater temperature along its length; (b) temperature distribution from the centre of the heater to the surrounding surface.

2.4.2 Poly-1 & Poly-2 stacked microheaters

PSMs can also be designed using two polysilicon layers, which would increase microheater thickness and can improve mechanical stability. In addition, the dielectric layer in between the polysilicon layers has low CTE and thermal conductivity, thus, less heat is conducted to bottom polysilicon layer (Poly-2) when the top polysilicon layer

(Poly-1) undergoes resistive heating. Therefore, bottom polysilicon layer has less thermal expansion, improving overall integrity of the microheater. An illustration of poly1-poly2 PSM design is presented in *Figure 2.7*, where the dielectric etching regions beneath the Poly-2 layer have been indicated.

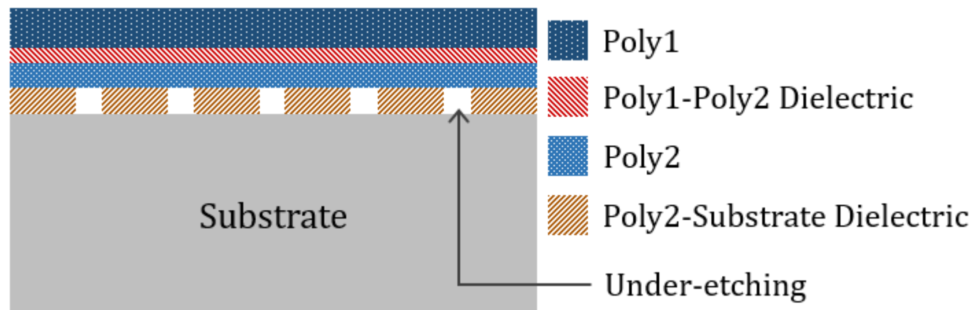


Figure 2.7: Cross-sectional view of partially suspended Poly1-Poly2 microheater design.

Temperature distribution across the length of partially suspended and non-suspended Poly1-Poly2 microheaters are shown in *Figure 2.8a* and *2.8b*, respectively. Poly-1 provides necessary CNT synthesis temperature, while Poly2 has lower temperature due to the Poly1-Poly2 dielectric layer. For the PSM design (*Figure 2.8a*), the oscillations in Poly-2 temperature are due to the five under-etched regions. For the non-suspended design (*Figure 2.8b*), the non-symmetry in temperature along the microheater length is a simulation artefact. In this Poly1-Poly2 microheater design, apart from the improvement in mechanical stability, lower temperature of Poly2 also enables lower CMOS surface temperature.

2.4.3 Al–Ni microheaters

For the standard CMOS process with Al metallization, microheaters were designed and simulated using tri-nickel aluminide (Ni_3Al). *Figure 2.9* shows the thermal simulation results for both non-suspended and partially suspended designs. Around a 1 µm thick layer of Ni needs to be deposited on a 0.6 µm thick Al layer to obtain the Ni3Al phase, considering the atomic weights and mass densities of Ni, Al, and Ni_3Al. Therefore, these microheaters are designed with a 1.6 µm thickness. The width of non-suspended design in *Figure 2.9a* is 1 µm, whereas PSM (with limited under-etching along the length, similar

to design-1 from previous section) in *Figure 2.9b* has a 3 µm width. PSMs with a greater width would yield higher mechanical stability in the under-etched design, while lower width of the non-suspended design results in less heat conduction on the substrate.

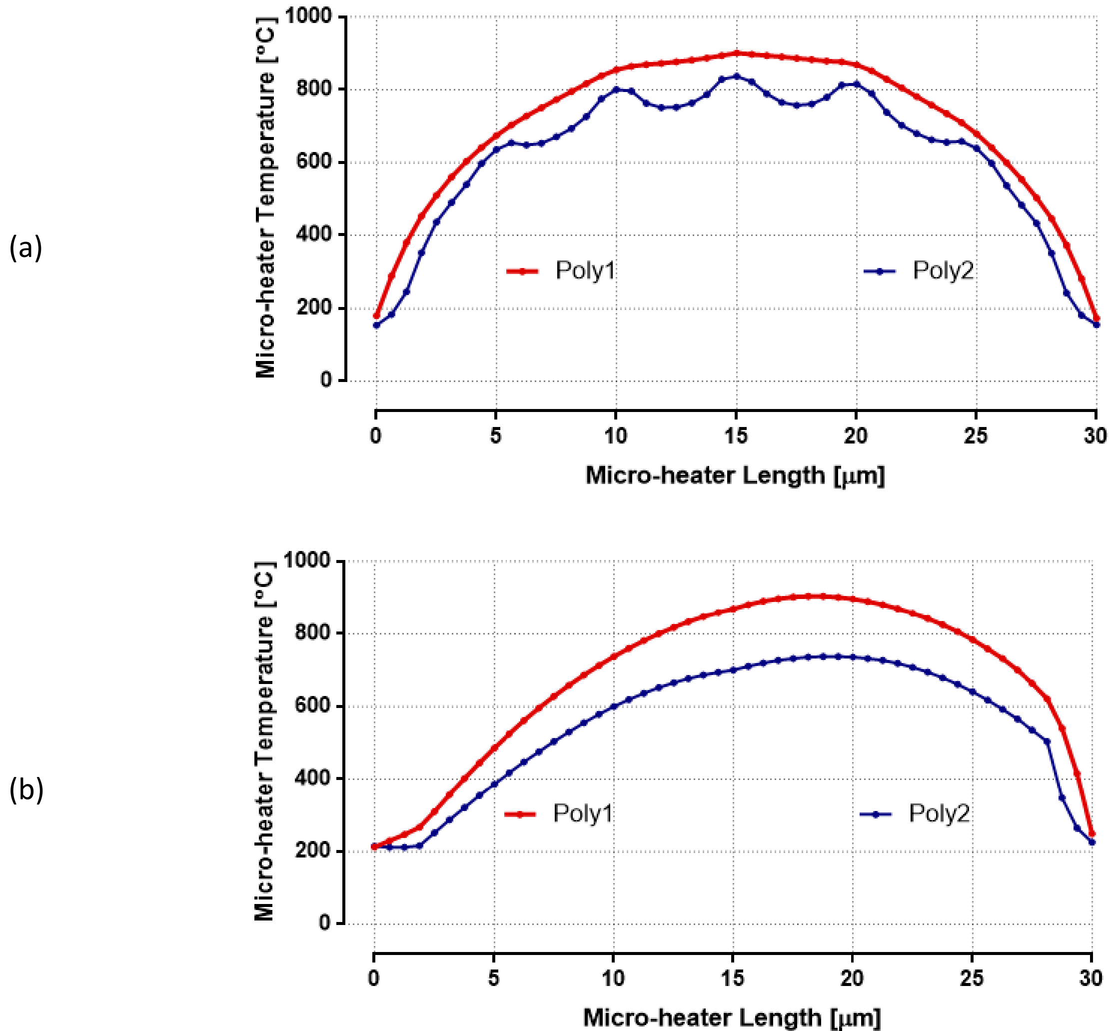
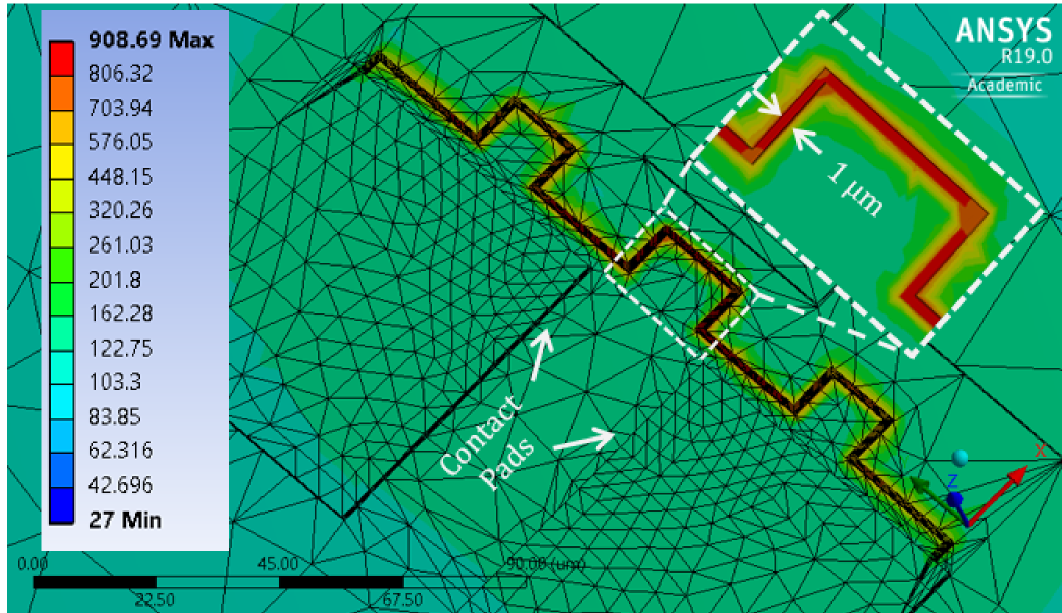
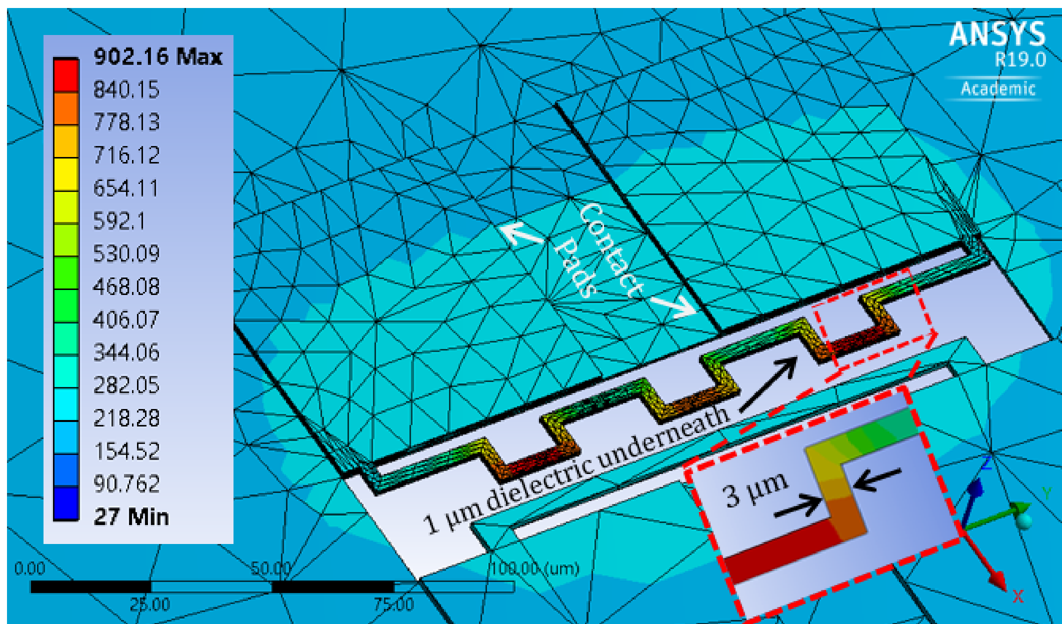


Figure 2.8: Temperature distribution across the length (a) partially suspended and (b) non-suspended Poly1-Poly2 microheaters.

For efficient resistive heating, the microheaters need sufficiently high resistance. Hence, the length of the metal heater designs was extended to ~240 µm for increasing heater resistance. The PSM design had ~15 Ω room temperature resistance, which goes above 35 Ω at the CNT synthesis temperature due to increase in Ni_3Al resistivity at the elevated temperature. The non-suspended design has a 3-times-higher heater resistance due to



(a)



(b)

Figure 2.9: Thermal–electric simulation of Ni_3Al designs: (a) non-suspended and (b) partially suspended.

a 3-times-lower width. The non-suspended design (*Figure 2.9a*) produces a chip surface temperature above 300 °C, due to lack of thermal isolation of the heater. This post-processing temperature is not suitable for CMOS circuits. However, the partially suspended design (*Figure 2.9b*) has sufficient thermal isolation for the heater, resulting

in a CMOS-compatible surrounding temperature of ~200 °C. It requires around 350 and 150 mW power for the non-suspended and partially suspended microheaters, respectively, to generate the CNT synthesis temperature.

2.4.4 Cu–Ni microheaters

Cupronickel microheaters were designed and simulated for the CMOS processes that use Cu as interconnecting metal. Material properties of 70% Cu – 30% Ni alloy composition is used for the heaters. Considering the atomic weights and mass densities of Cu and Ni, the heaters are modelled with 0.85 µm thickness. Depositing 0.25 µm thick Ni on top of a 0.6 µm thick Cu layer is suitable for achieving 70% Cu – 30% Ni binary alloy composition upon annealing. The length and width of the microheaters in both non-suspended and partially suspended designs are kept same as the Ni_3Al microheater designs. Heater resistances of Cu–Ni designs are also similar to the Ni_3Al heaters, as sheet resistances for both of these heaters are alike at near CNT synthesis temperature.

Microheater temperatures, along with the surrounding surface temperatures, are plotted for non-suspended, partially suspended, and fully suspended Cu-Ni designs in *Figure 2.10*. All these heaters have a local hot region of ~900 °C for growing CNTs, and the temperature starts to drop when moving away from the heaters. The non-suspended design reaches a CMOS-incompatible surface temperature of ~350 °C, while the PSM design manages to achieve a CMOS-compatible chip surface temperature of ~200 °C. Average surrounding temperature of the fully suspended Cu–Ni design drops down to near room temperature. At 4 µm away from the heaters, the average thermal gradients around the non-suspended, partially suspended, and fully suspended Cu–Ni microheaters are 137, 175, and 219 °C per micrometre, respectively. The power requirements of non-suspended and partially suspended designs are similar to the respective Ni_3Al designs, while the fully suspended heater consumes less than 5 mW of power. Even though the fully suspended heater has the maximum thermal isolation and lowest power consumption, the design is not practically feasible as it is prone to mechanical deformation. Therefore, PSM is the most suitable among the Cu–Ni designs for our application.

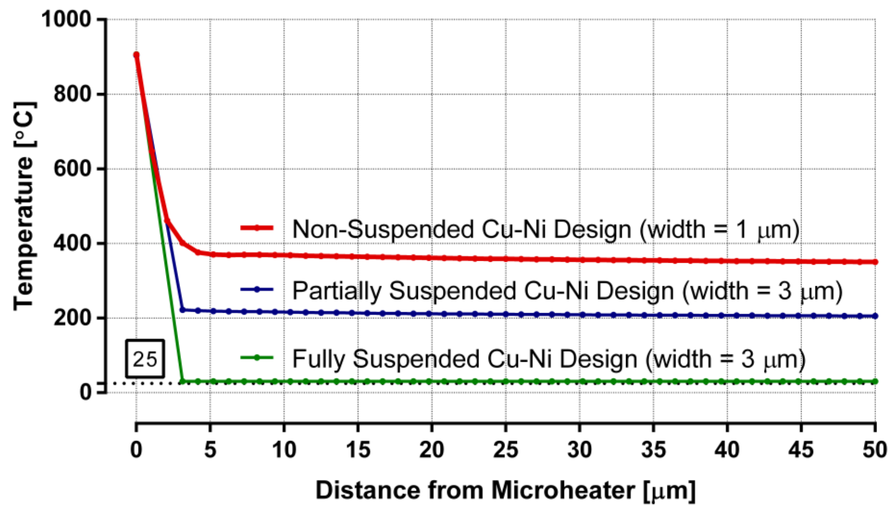


Figure 2.10: Temperature distribution from the centre of different cupronickel microheaters to the surrounding surface.

2.5 Conclusion

CMOS-compatible materials suitable for resistive heating were investigated. The role of material properties for effectively generating high temperatures were determined based on analytical model. Along with polysilicon layers, alloys made from metal interconnects in CMOS were considered. For Al and Cu interconnect metal layers, Tri-nickel aluminide (Ni_3Al) and cupronickel (70% Cu–30% Ni) were respectively selected on the basis of their material properties. Design considerations were made based on potential deformation caused by stiction and buckling. Results of thermo-mechanical simulation on non-suspended, partially suspended and fully suspended microheaters showed that CMOS-compatible ambient temperature (< 300 ˚C) can be achieved when a heater generates CNT synthesis temperature (~ 900 ˚C).

Chapter 3

CMOS Chip Design

3.1 Introduction

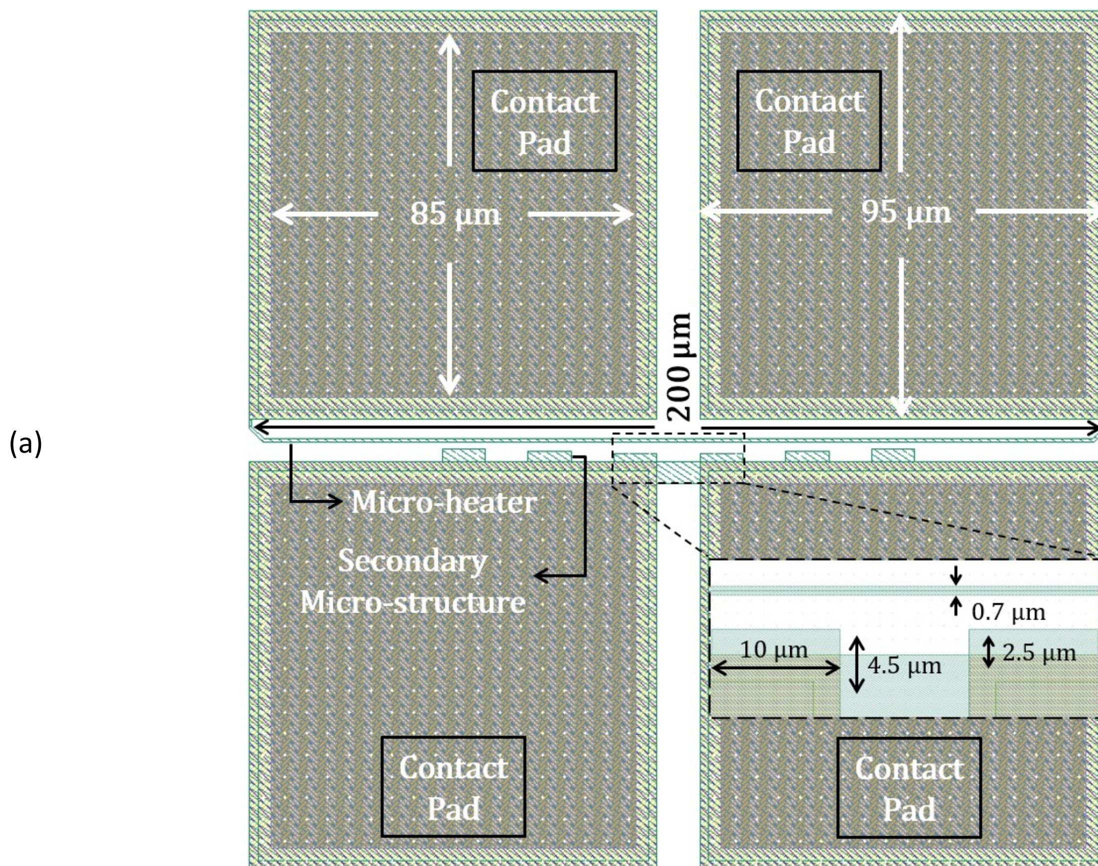
The promising thermo-mechanical simulation results showed that it can be possible to generate CNT synthesis temperatures on CMOS microheaters with safe ambient temperature for the electronics. With the successful feasibility analysis, a commercial AMS 350 nm CMOS process was chosen to design and fabricate microheaters. Although simulations were performed with AMS 180 nm and AMS 350 nm CMOS technologies, the latter was chosen for realizing the chips on the basis of cost considerations. The fabrication process was carried out through the EUROPRACTICE IC service, which offers Multi Project Wafer (MPW) option for reducing the production costs to facilitate low-volume device prototyping. The selected 350 nm CMOS technology was AMS C35B4C3; it provides two different polysilicon layers (Poly-1 & Poly-2) and four interconnecting metal layers made of aluminium. Among the CMOS microheater materials for CNT synthesis, polysilicon was considered as the best option due to its material properties. In addition, alloying is not required for polysilicon microheaters. A CMOS process using Cu for metallization is preferred over the one using Al based on both alloy formation challenges and material efficiency as a microheater. However, Cu interconnects are more commonly used from 180 nm CMOS technology, whereas the older and less costly 350 nm technology typically uses Al. Since polysilicon was the preferred microheater material for the CNT synthesis application and are available in both processes, the older CMOS technology was chosen for the research work based on the fabrication cost. A variety of microstructures were designed in a 3 mm × 3 mm CMOS chip using the aluminium and polysilicon layers. The IC service provided 40 fabricated CMOS chips. Most results from this chapter are published in *Article 2* and *6*, while contents from *section 3.3 & 3.4* are planned for publication.

3.2 Layouts and micrographs

The IC design tool, Cadence Virtuoso was used for the layout design. Associated AMS 350 nm design library was used to access the available device layers along with performing the design rule checking (DRC) and other verifications. The chip design involved custom-designed microstructures including contact pads for electrically accessing those structures. Since the CMOS chip was not designed for conventional application specific integrated circuits (ASICs) and was focused to realize CMOS-MEMS structures, it was possible to avoid several relatively less significant design rules.

3.2.1 Aluminium designs

Four Al microheater layouts are illustrated in *Figure 3.1*, with an overview of the system including the contact pads (*Figure 3.1a*). In design-1, the microheater is 200 µm long with uniform width of 0.7 µm. In design-2 (*Figure 3.1b*), the central region (10 µm long)



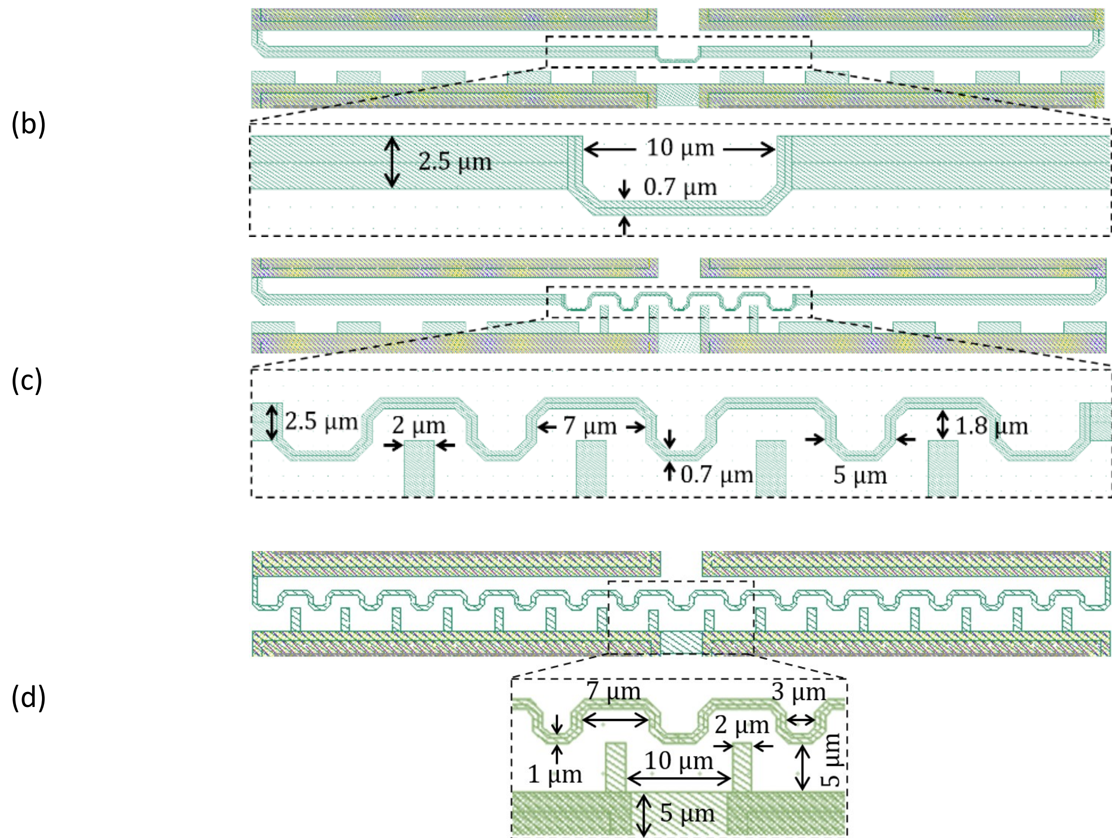


Figure 3.1: Top view of aluminium microheater layout designs. (a) Design-1, microheater configuration including contact pads; (b) Design-2 & (c) Design-3, reduced microheater effective length; (d) Design-4, wave-shaped microheater with increased length.

of the microheater has a width of 0.7 µm while the width of the remaining region is 2.5 µm. This is to obtain higher temperature in the central region. In design-3 (*Figure 3.1c*), the central region has a rectangular wave shape to achieve a greater effective length compared to design-2. The length of the wave-shaped microheater in design-4 (*Figure 3.1d*) is efficiently increased to over 350 µm, with width of 1 µm.

The contact pads for the microstructures have a surface area of 95 µm × 95 µm, providing sufficient area for wire bonding. Layout of the contact pads are only shown in *Figure 3.1a*. Spacing between the electrodes has been changed in different designs to vary the local electric field. Shapes of the secondary electrodes were also varied; they are narrower in design-3 and design-4 than the secondary electrodes of other two Al designs.

(a)

(b)

(c)

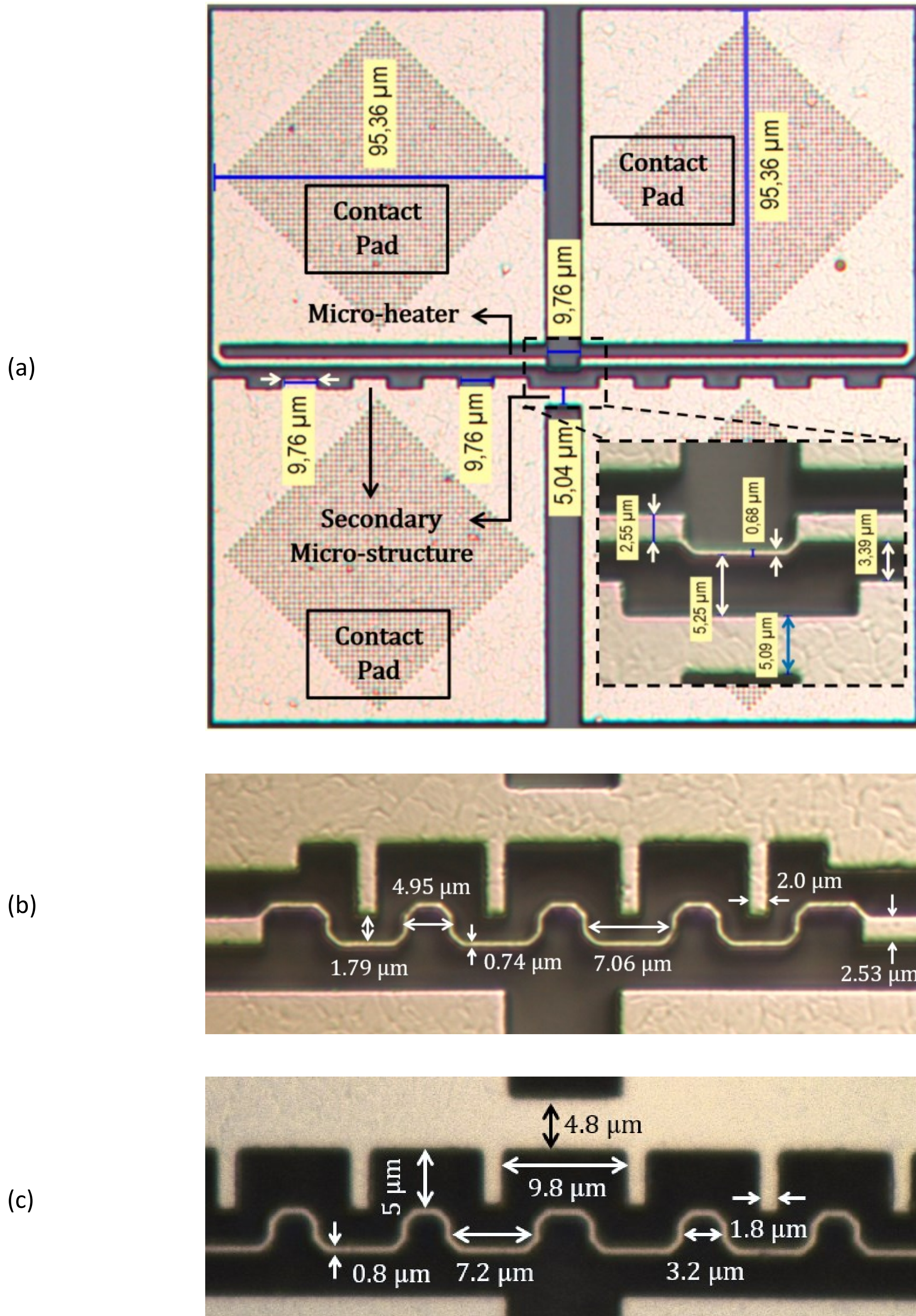


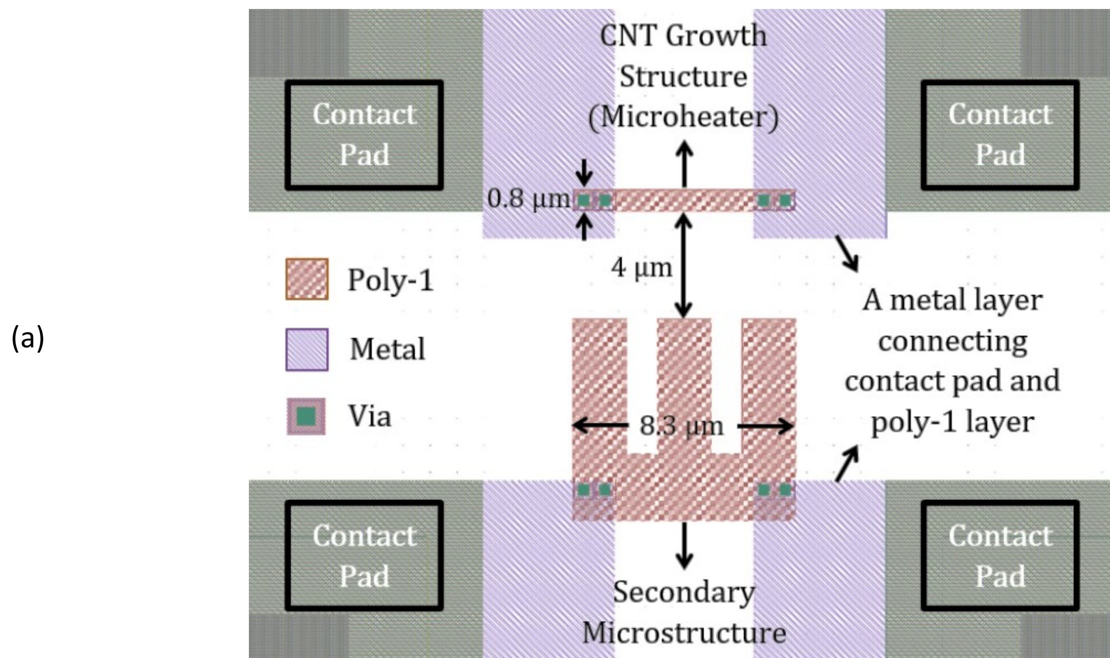
Figure 3.2: Optical micrographs of fabricated aluminium microheaters. (a) Overview of Design-2 including contact pads; (b) Design-3 and (c) Design-4 metal microstructures.

Optical micrographs of some fabricated metal microheaters are shown in *Figure 3.2*. The microstructures are made of the top Al metal layer. In these designs, the top metal layer is not covered by any CMOS passivation layer. In CMOS chip design, a 'PAD opening' layer can be used to define selected regions where the passivation layer(s) are etched during the wafer-level fabrication process, which enables an exposed top metal layer. Bottom surface of this metal layer is covered by a dielectric layer. Dimensions measured from the optical micrographs of the fabricated Al microstructures reflect the corresponding dimensions of the layout designs. The rhombus structure in the middle of the contact pads (*Figure 3.2a*) consists of an array of vias. The Al microheater with longest length (*Figure 3.2c*) has a measured resistance of ~50 Ω.

3.2.2 Polysilicon designs

A poly-1 microheater design with secondary structure is presented in *Figure 3.3*. The CMOS layout design in *Figure 3.3a* illustrates all the comprised layers where the vias provide access to metal layers for the polysilicon structures. The extended metal layer aids in designing an 8.3 µm long heater, while keeping a 15 µm distance between the contact pads. The microheater is 0.8 µm wide and has a measured resistance of ~100 Ω.

(a)



(b)

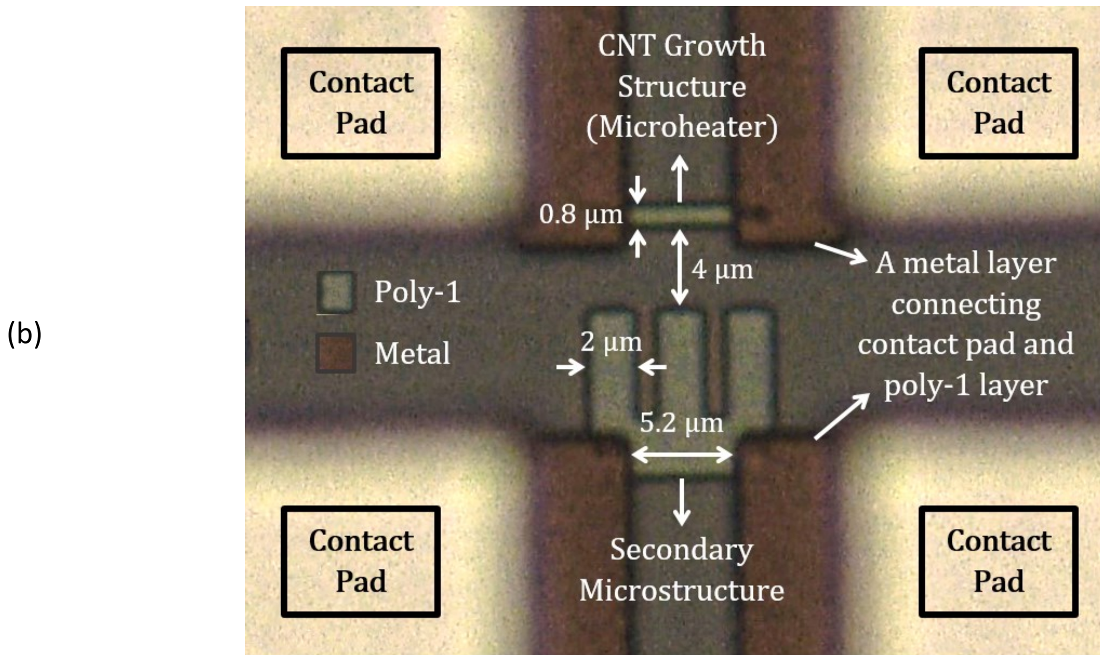


Figure 3.3: Poly-1 CNT growth structures. (a) layout design and (b) optical micrograph.

The heater and secondary structures are 4 µm apart. Dimensions of the microstructure layouts are properly translated to the fabricated polysilicon structures, as seen in the optical micrograph in *Figure 3.3b*.

Figure 3.4a shows the layout of a poly-2 design, and *Figure 3.4b* shows the corresponding optical micrograph of the fabricated CMOS microstructures. The design involves a poly-2 layer, two different metal layers, and vias for electrical connection between layers. Some additional vias are purposely placed in front of the microheater to limit dielectric etching in those regions. In this design, a top metal layer (metal-2) was used as an etch protection mask; hence, the dielectric layer underneath that metal layer is not etched.

This poly-2 design resembles a simulated model (design-2) from *Figure 2.3 & 2.4b*, where the heater is only under-etched from the side facing secondary microstructures. The heater is ~25 µm long and 1.5 µm wide. It has a high measured resistance of ~1 KΩ due to high poly-2 resistivity. The optical micrograph shows the fabricated microstructures, which were rendered well from the designed CMOS layout.

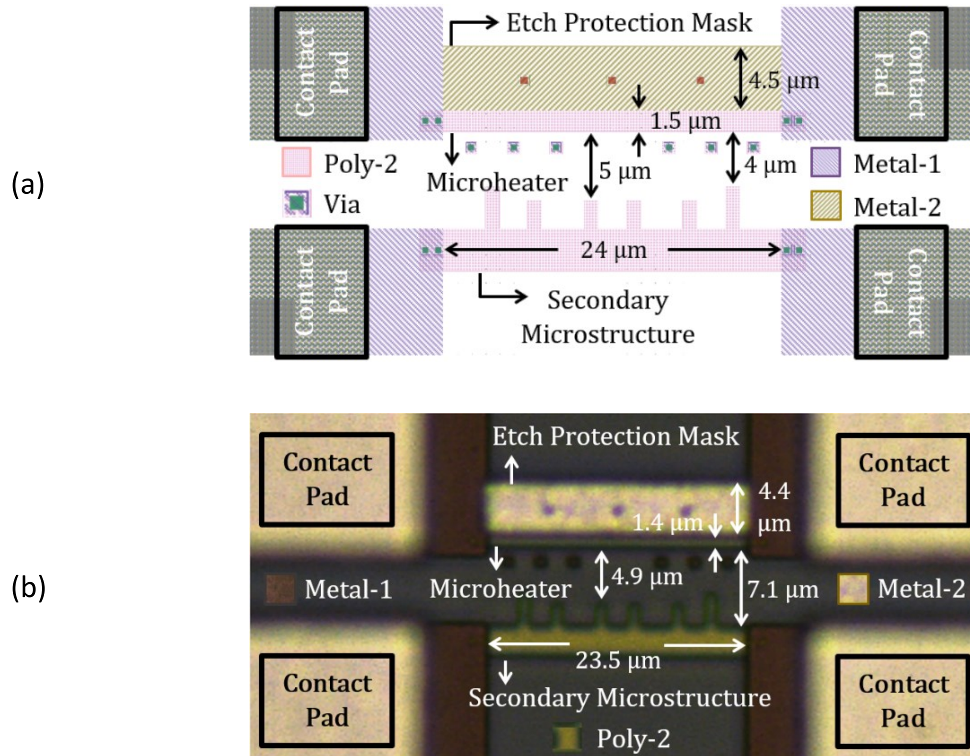


Figure 3.4: Poly-2 CNT growth structures. (a) layout design and (b) optical micrograph.

3.3 Various microheater features

Different microheaters are designed with different features, mainly to facilitate post-processing for realizing CMOS-MEMS heaters. Apart from CNT synthesis, on-chip CMOS microheaters can be useful in numerous applications [244–255]. In all these high-temperature applications, the electronic circuitries should be kept within the CMOS-compatible temperatures. Since the microheaters designed for our application are targeted for very high CNT synthesis temperatures, they could cover a high temperature range. Hence, the designed CMOS heaters can also be beneficial for other applications.

In this project, an improved second-generation CMOS chip was designed based on the experiences from the post-processing of the initial first-generation CMOS chip design; the details are discussed in *section 4.5*. The heater features from both of these designed chips are presented in this section. The features are discussed with the associated heater layout designs and micrographs. The secondary microstructures were designed as the neighbouring electrode to guide the growing CNTs from the microheater by local electric field, but they can also be used as microheaters.

3.3.1 Metal layer as etching mask

Top interconnecting metal layers can be used as *in-situ* mask to avoid dielectric layer etching from the regions where the metal structures are placed. They can be utilized to limit or prevent from under-etching polysilicon microheaters as shown in *Figure 3.5*. Depending on the gap between the metal mask and microheater (*Figure 3.5a & 3.5b*), amount of under-etching can be reduced compared to the fully exposed side of the heater during an isotropic etching. Therefore, the fully exposed side will have higher dielectric etching underneath the heater than the side with the metal mask. The partially suspended microheaters fabricated in this approach will have higher suspension in one side, which will result in higher temperature in that side compared to the less suspended side during joule heating due to lower heat loss through the dielectric layer.

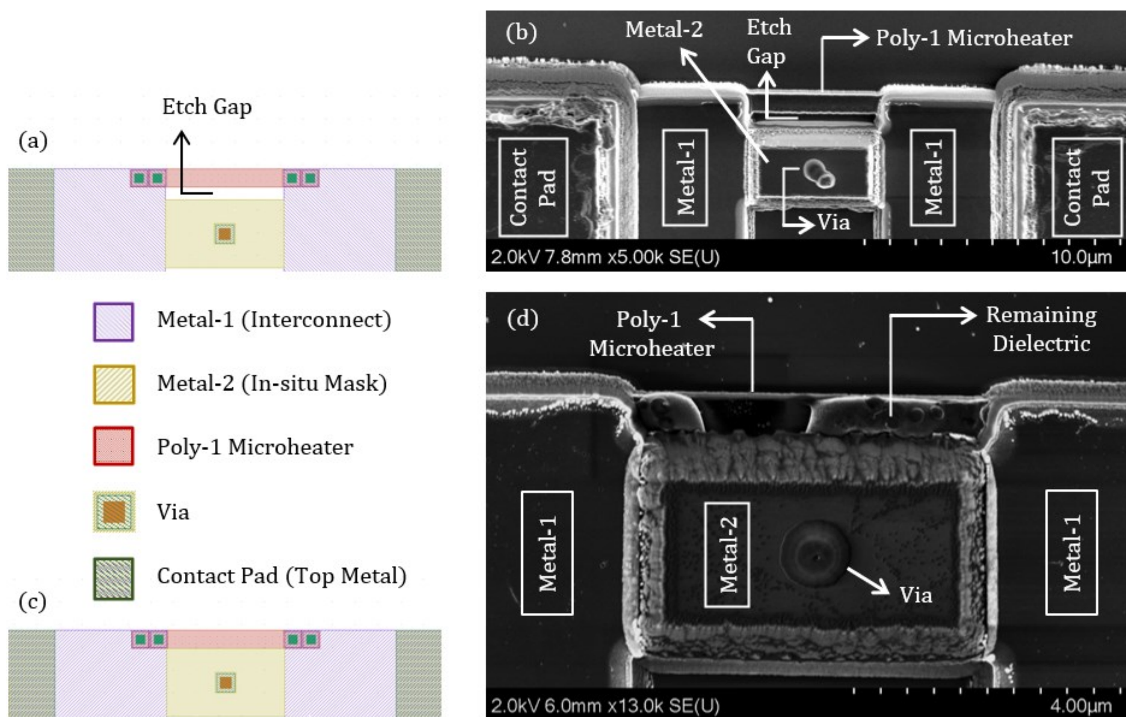


Figure 3.5: *In-situ* metal masks for polysilicon microheaters. (a) Layout design and (b) electron micrograph of a microheater and metal mask with an etch gap (after dry etching); (c) Layout design and (d) electron micrograph of a microheater with directly adjacent metal mask on one side (after dry etching).

Microheater under-etching can also be prevented by placing the metal mask directly adjacent to the heater as shown in *Figure 3.5c & 3.5d*; this design is similar to the simulated model (design-2) in *Figure 2.3 & 2.4b*. However, the mask also hindered in

completely removing the dielectric layer above the microheater after dry etching, as observed in *Figure 3.5d*. The metal mask here is made of metal-2, which is the second metal layer from the bottom in this four metal layer CMOS process. Due to the height differences between the metal layers, designing this mask with the lower metal layer (i.e., metal-1) will reduce the remaining dielectric over the microheater, while a mask made of a higher metal layer (e.g., metal-3) will result in a microheater covered with more dielectric layer after dry etching. The remaining dielectric layer over the microheater will be removed during the under-etching process by wet etching.

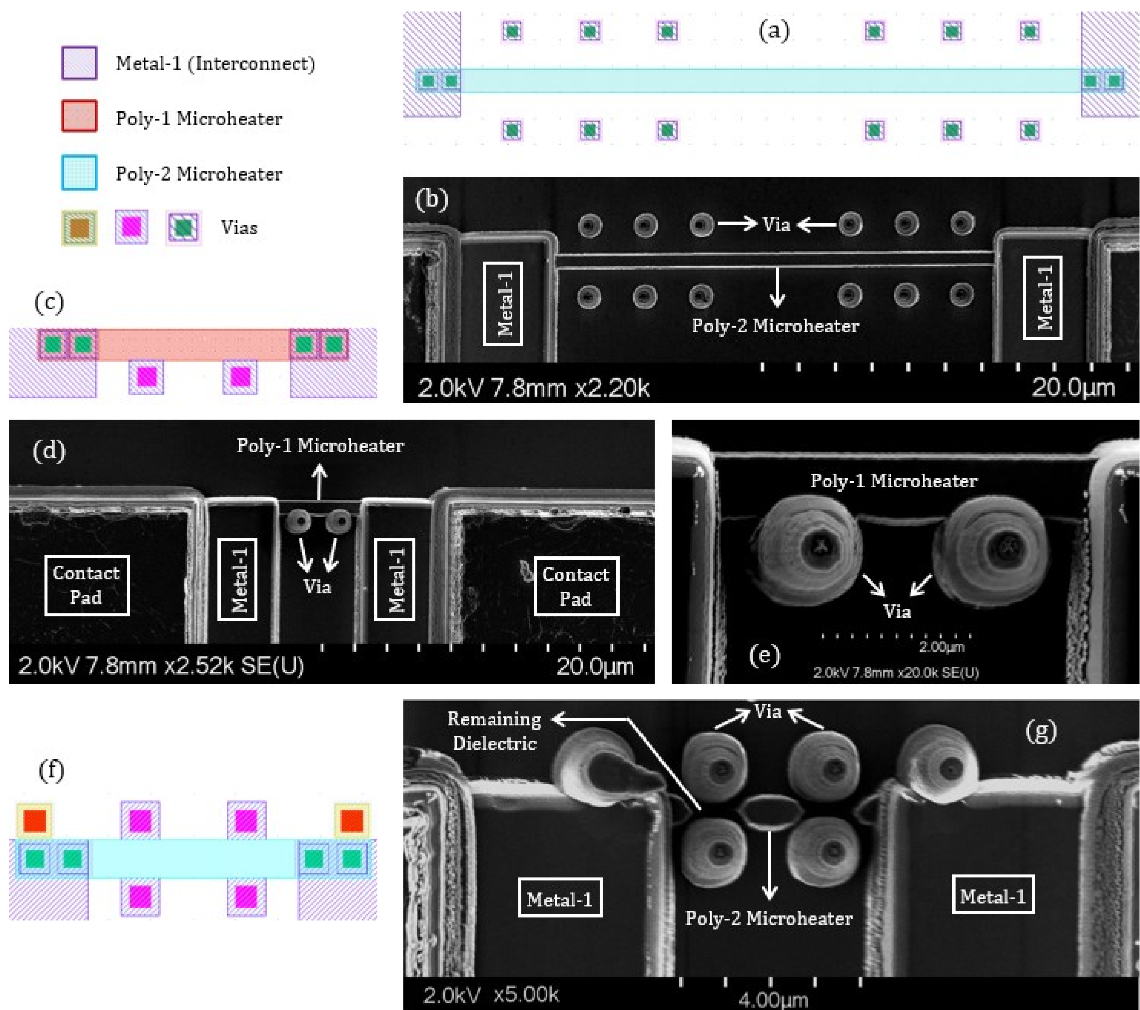


Figure 3.6: *In-situ* via masks for polysilicon microheaters. (a) Layout design and (b) electron micrograph of a microheater and via masks with etch gaps; (c) Layout design and (d) electron micrograph of a microheater with directly adjacent vias on one side, (e) close-up of the heater with two vias; (f) Layout design and (g) electron micrograph of a microheater with via masks for patterned under-etching.

3.3.2 Via as etching mask

Similar to the metal layers, the vias in the CMOS process can be used as the *in-situ* etch protection masks as shown in *Figure 3.6*. Due to small dimensions of the microheaters, ~1 µm × 1 µm vias were placed near some heaters to employ them as the etching masks. Only two vias can sufficiently be utilized to prevent under-etching selective regions of a microheater for partial suspension as demonstrated in *Figure 3.6c, 3.6d & 3.6e*. The under-etching pattern illustrated in *Figure 2.7* is achieved with the via mask arrangements from *Figure 3.6f & 3.6g*. In this approach, the centre of the microheater can be fully suspended, which generates the maximum temperature along the heater during the resistive heating. Figure 3.7 shows a cross-sectional sketch of partially suspended heater from the design presented in *Figure 3.6c & 3.6d* after under-etching the dielectric layer. The via / metal mask prevents under-etching a region of the microheater.

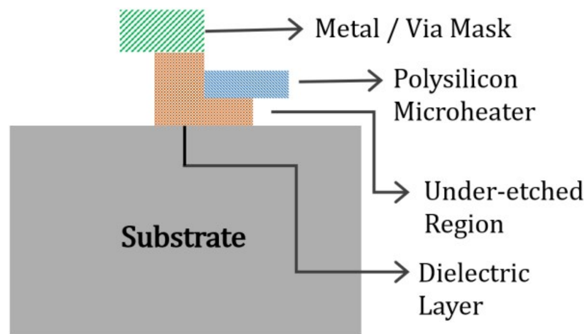


Figure 3.7: Cross-sectional sketch of an under-etched polysilicon microheater with via / metal mask.

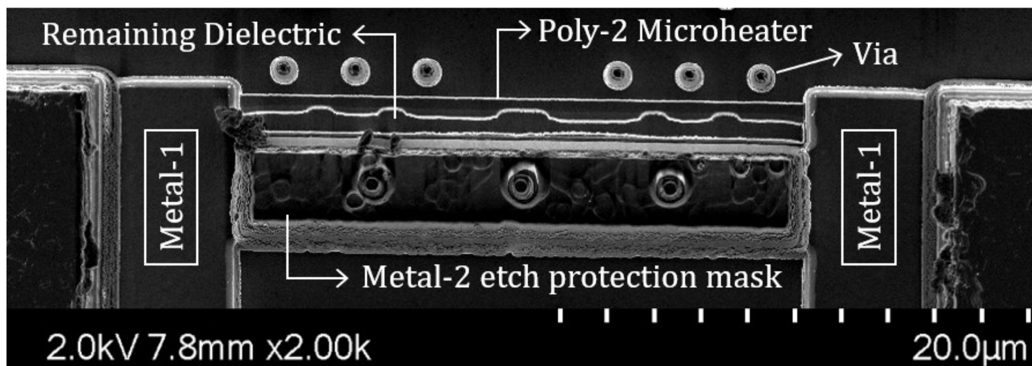


Figure 3.8: Scanning electron microscope (SEM) image of a polysilicon microheater with *in-situ* metal and via masks (after polysilicon exposure with dry etching).

A polysilicon microheater with both metal and via masks are presented in *Figure 3.8*, the layout design of which has been illustrated in *Figure 3.4a*. As the metal mask was directly placed beside the microheater, the dielectric layer residue remains in that side of the heater after the dry etching, which was also observed in *Figure 3.5d*.

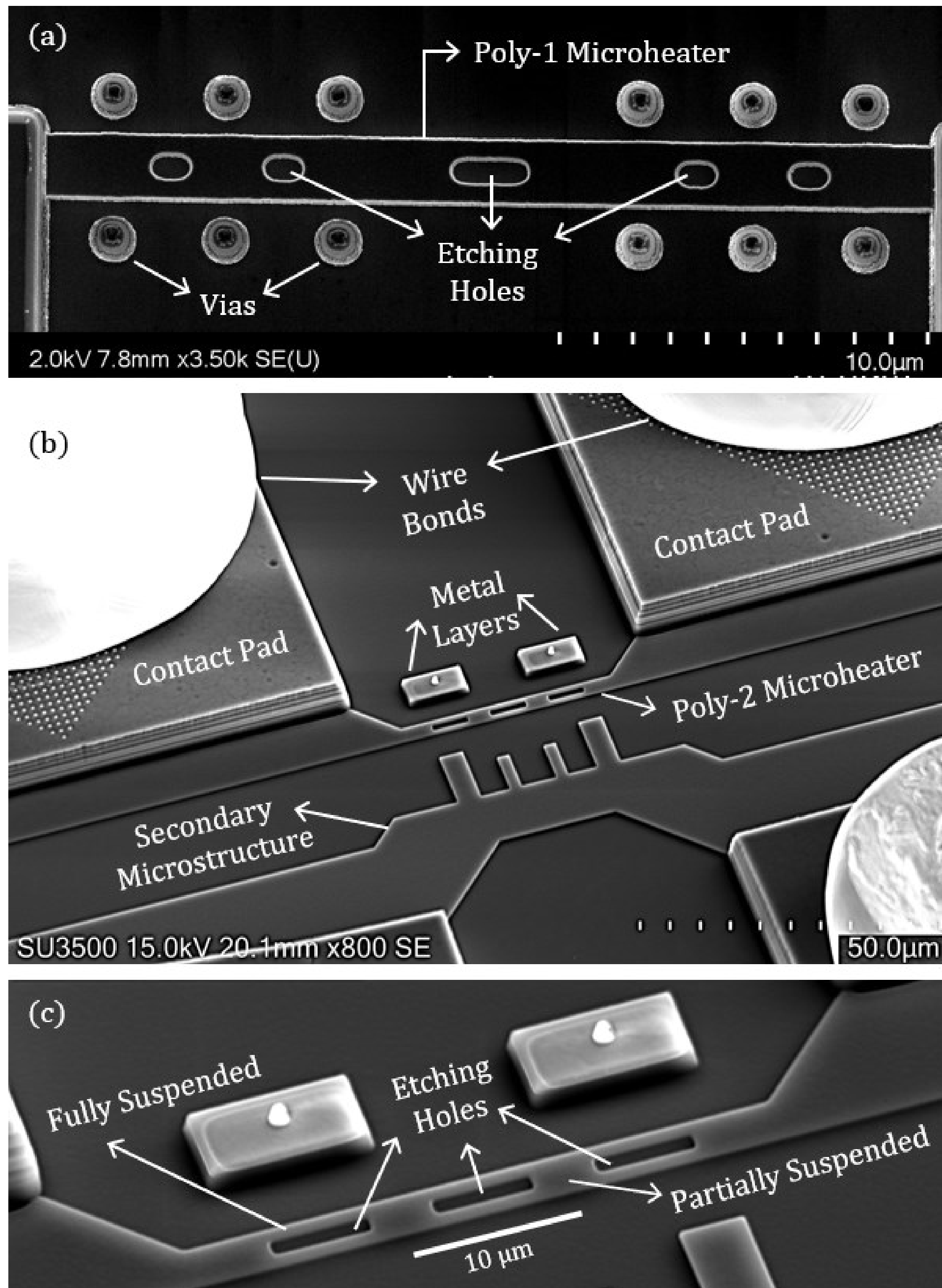


Figure 3.9: Polysilicon microheaters with etching holes. Electron micrographs of (a) microheater with holes and via masks, (b) microheater with partially and fully suspended regions due to the etching holes, and (c) close-up of the poly-2 heater.

3.3.3 Microheaters with etching holes

Several polysilicon microheaters were fabricated with some holes to facilitate under-etching and releasing the heaters as shown in *Figure 3.9*. Forming holes of different sizes and shapes in the polysilicon layers (*Figure 3.9a & 3.9b*) were allowed in the CMOS design. In *Figure 3.9a*, the microheater will have maximum suspension in the centre, where heater reaches maximum temperature. The micrograph in *Figure 3.9c* shows fully released microheater regions around the etching holes, while the other regions still have dielectric layer beneath the heater. This approach also resembles the patterned heater under-etching as shown in the cross-sectional illustration in *Figure 2.7*. The wet etching results to suspend the microheaters are detailed in *section 4.7*.

3.3.4 Microheaters covered with passivation layers

The surfaces of CMOS chips are normally covered with passivation layer(s) to protect the ICs. For the contact pads, the passivation / protection layer(s) are selectively removed during the IC fabrication process to expose the top metal layer in those regions for establishing electrical connections by means of wire bonding or similar methods to form electrical access with the device layers. The contact pad regions are defined by a ‘pad opening’ design layer during the IC design phase. In our CMOS chips, this design layer was used on most part of the chips that contain microheaters. In this way, the passivation layers are avoided on the microheater regions. This eliminates the post-processing step of etching the passivation layers. Further details on post-processing of the CMOS chips are in *chapter 4*. In a few microheater designs, the ‘pad opening’ design layer was not used over the polysilicon layer of the effective microheater region; therefore, such a region is covered with passivation layers as shown in *Figure 3.10a*. The purpose of this design was to check if a heater can be protected or covered, while the dielectric layer in the surrounding areas are etched. *Figure 3.10b* & *3.10c* demonstrate the microheater covered by dielectric after preforming RIE to remove surrounding dielectric layer and expose the silicon substrate. During the dry etching process, the passivation layers were also etched at a slower rate; thus leaving ~2.5 µm thick dielectric layer over the heater region while the neighbouring areas are fully exposed.

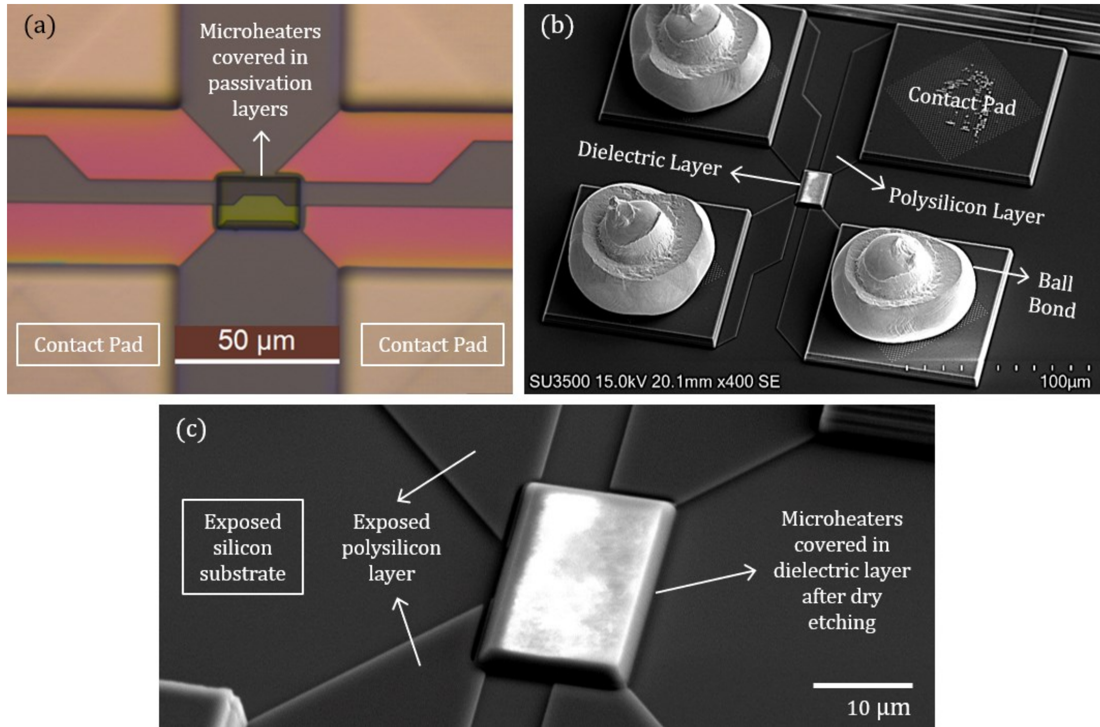


Figure 3.10: Polysilicon microheater with protective layer. (a) Optical micrograph of the heater covered with passivation layers, (b) SEM image after dry etching, and (c) heater region in higher magnification.

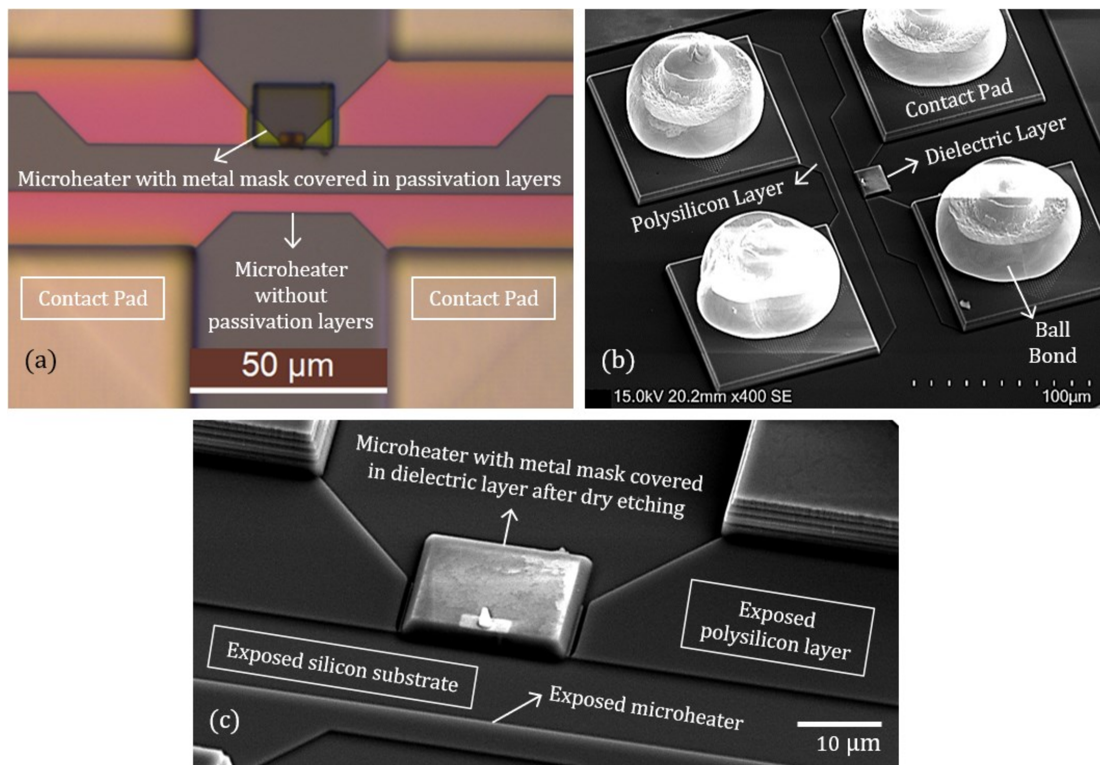
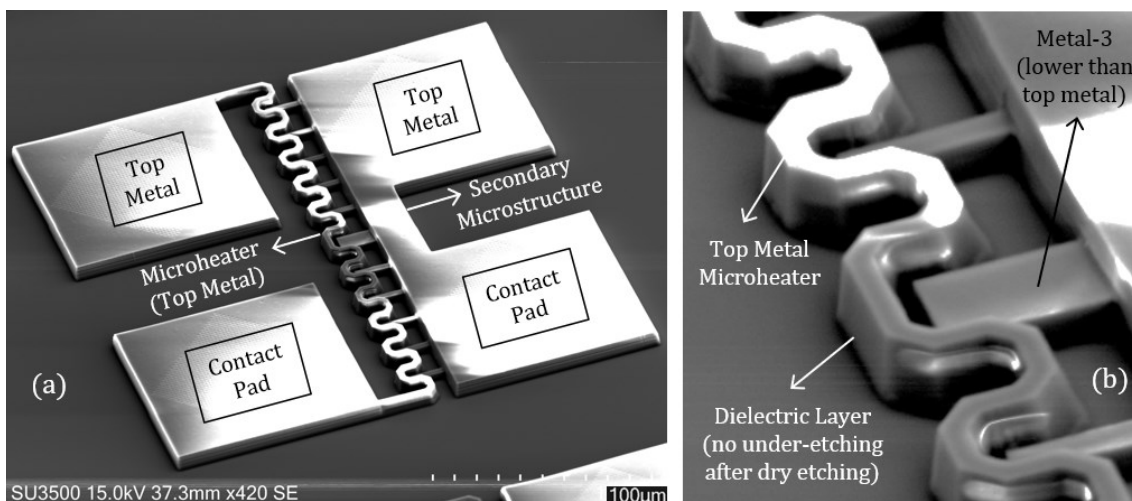


Figure 3.11: Polysilicon microheaters covered with and without protective layer. (a) Optical micrograph of the heaters, (b) SEM image after dry etching, and (c) heater region in higher magnification.

Figure 3.11a shows a polysilicon microheater with metal mask covered in passivation layers, while the adjacent polysilicon heater does not have such a layer. SEM images of the design after the dielectric RIE process are shown in *Figure 3.11b & 3.11c*. The three-dimensional perspective with high magnification in *Figure 3.11c* reveals the thick dielectric layer covering a microheater with exposed polysilicon layers and silicon substrate in the surroundings. It demonstrates that only a small region can be covered by protective layer through the utilization of 'pad opening' design layer during the IC design process. This approach can also be used to under-etch a microheater while covering its surface with a protective layer.

3.3.5 Wave-shaped microheaters

In this microheater design, the length of the heaters is efficiently extended by making the rectangular wave-shape structures. Such spring-like shapes can also support to counteract thermal expansion of the heater when operated at high temperatures. Micrographs of such heaters are presented in *Figure 3.12*. For the metal heaters, extended length is beneficial to increase the resistance for effective resistive heating. Several rectangular beams are used as secondary microstructures, which go in between the waves of the microheater (*Figure 3.12a & 3.12b*) for producing a concentrated electric field at the beam tips. The beams are made by a lower metal layer than the microheater metal layer (*Figure 3.12b*) to create a height difference. Similar structures are also fabricated with a polysilicon layer as presented in *Figure 3.12c*.



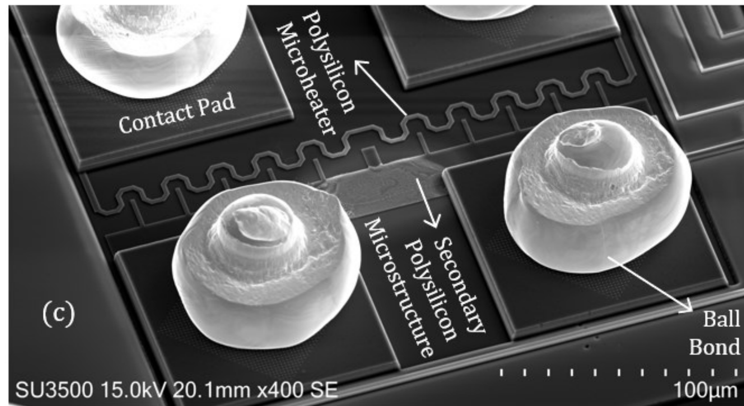


Figure 3.12: SEM images of wave-shaped microheaters. (a) Top metal heater with rectangular beams as secondary microstructures, (b) close-up of the metal structures, (c) similar design with polysilicon layer.

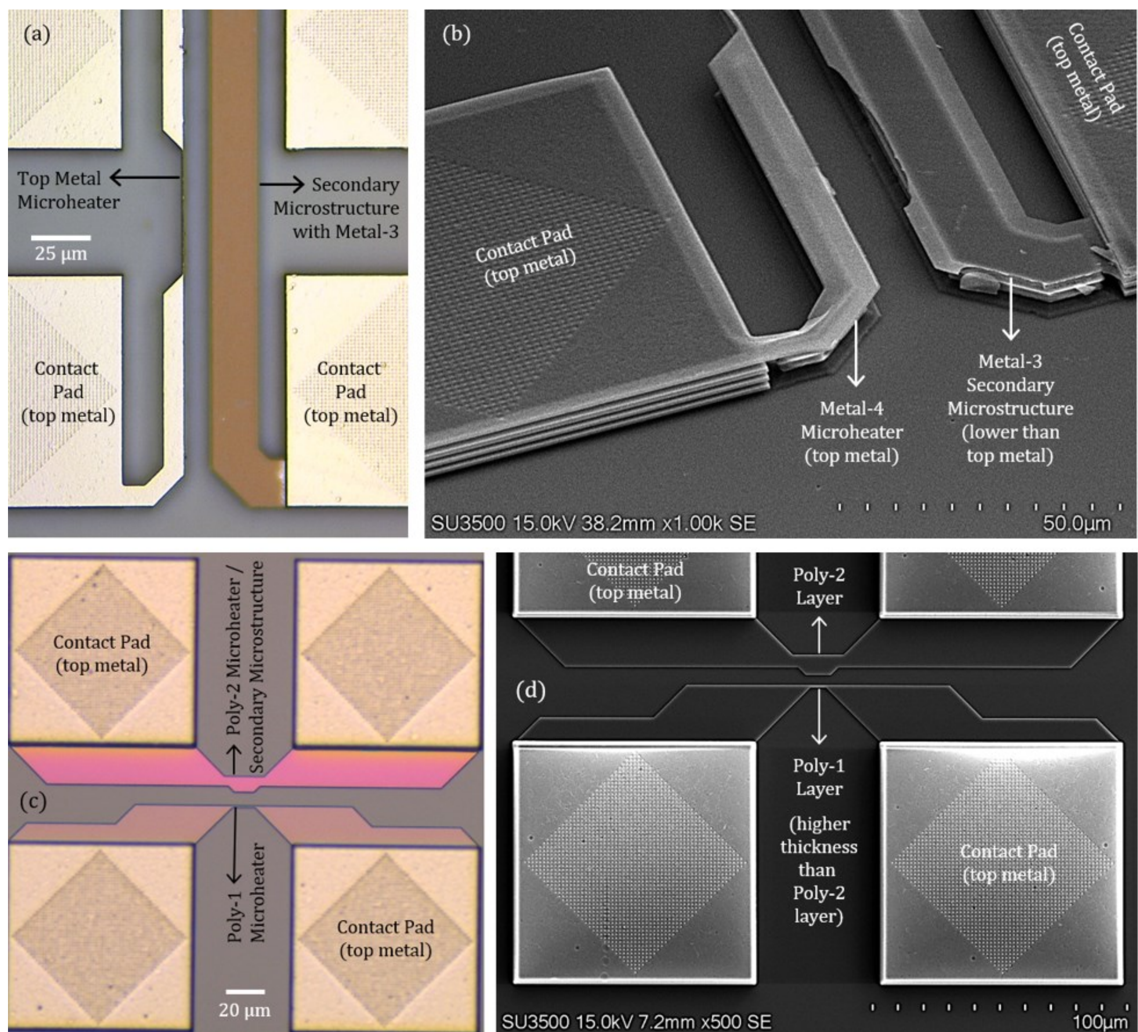
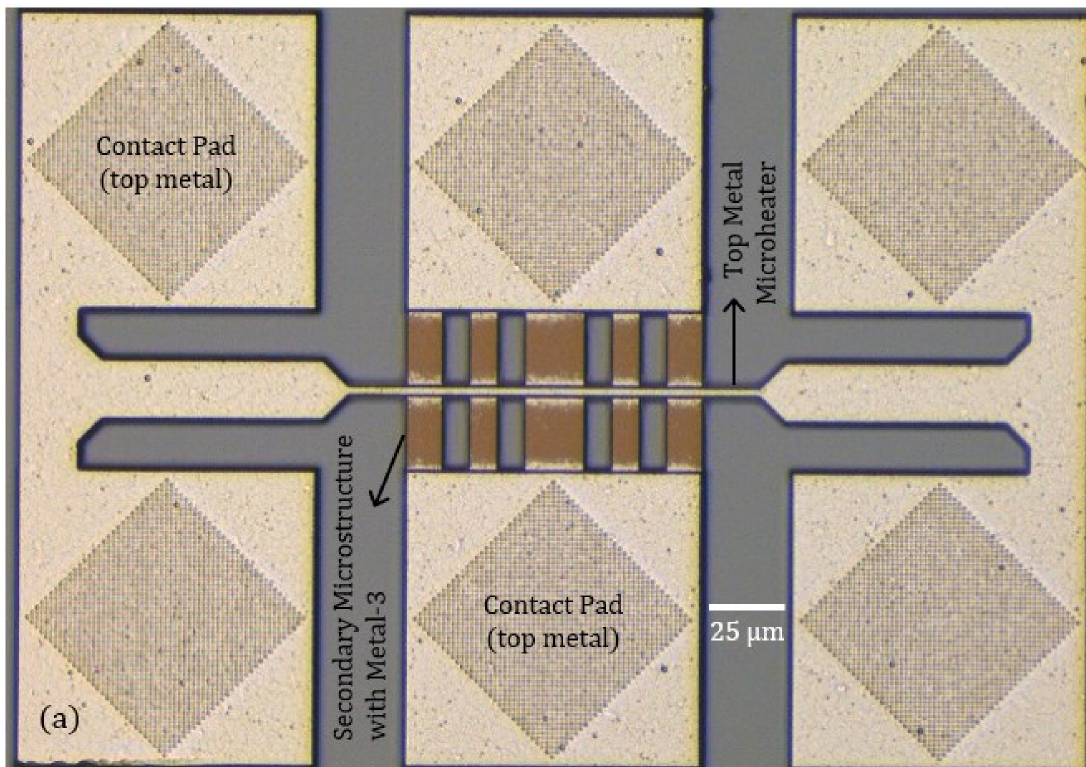


Figure 3.13: Microheaters with CMOS layers at different heights. (a) Optical and (b) electron micrograph of metal heaters; (c) Optical and (d) electron micrograph of polysilicon heaters with height variation.

3.3.6 Microheaters with height variation

CMOS microheaters can be fabricated using different layers available in the technology. In AMS 350 nm CMOS process, four Al interconnection layers are available. These layers are at different heights from the substrate, and heaters can be fabricated using any of them. By designing microheater using the top metal, the heater can be readily exposed in the fabricated CMOS chips using 'pad opening' design layer; thus, no post-processing is needed to obtain such exposed heaters. Dielectric layer is needed to be etched for exposing heaters made of other layers. Heaters buried with the dielectric layer can also be useful for some applications, one of which is demonstrated in *chapter 8*. In terms of CNT synthesis, the idea was to explore the possibility of 3D CNT integration with the two electrodes (i.e., the heaters) situated at two different heights. *Figure 3.13* shows metal and polysilicon microheaters at different heights. The height difference between the metal heaters (~ 1.5 µm) can be observed in the tilted view of *Figure 3.13b*. The polysilicon heaters (*Figure 3.13c & 3.13d*) also have a height variation of ~50 nm.

Metal microheaters can also be fabricated overlapping another metal microstructure as shown in *Figure 3.14*. The secondary microstructure is below the top metal microheater



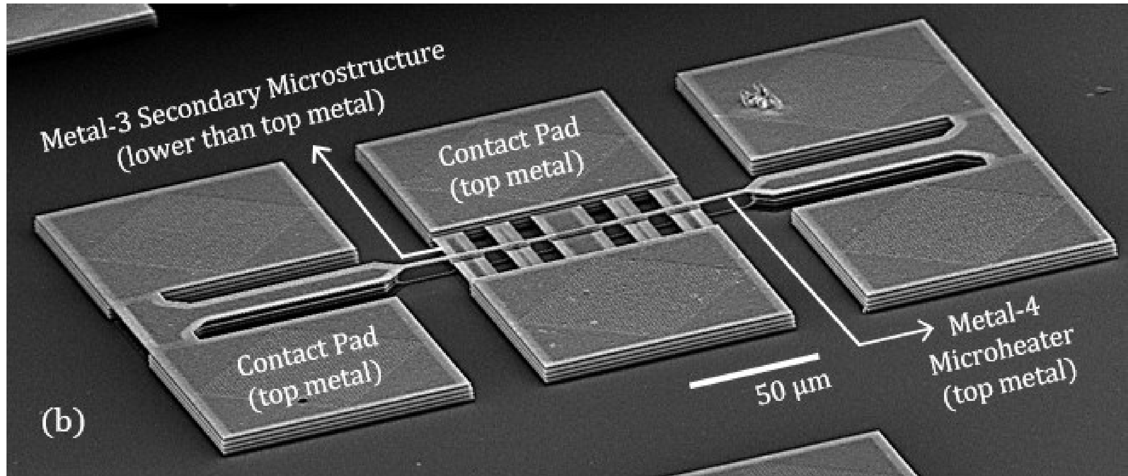


Figure 3.14: Vertical configuration of metal microheaters. (a) Optical and (b) electron micrograph of a four-terminal top metal heater fabricated over a secondary microstructure made of a bottom metal layer.

in this arrangement. The 3D micrograph in *Figure 3.14b* shows the height variation between the fabricated metal structures. The heater made of top metal has four terminals to facilitate four-point resistance measurement.

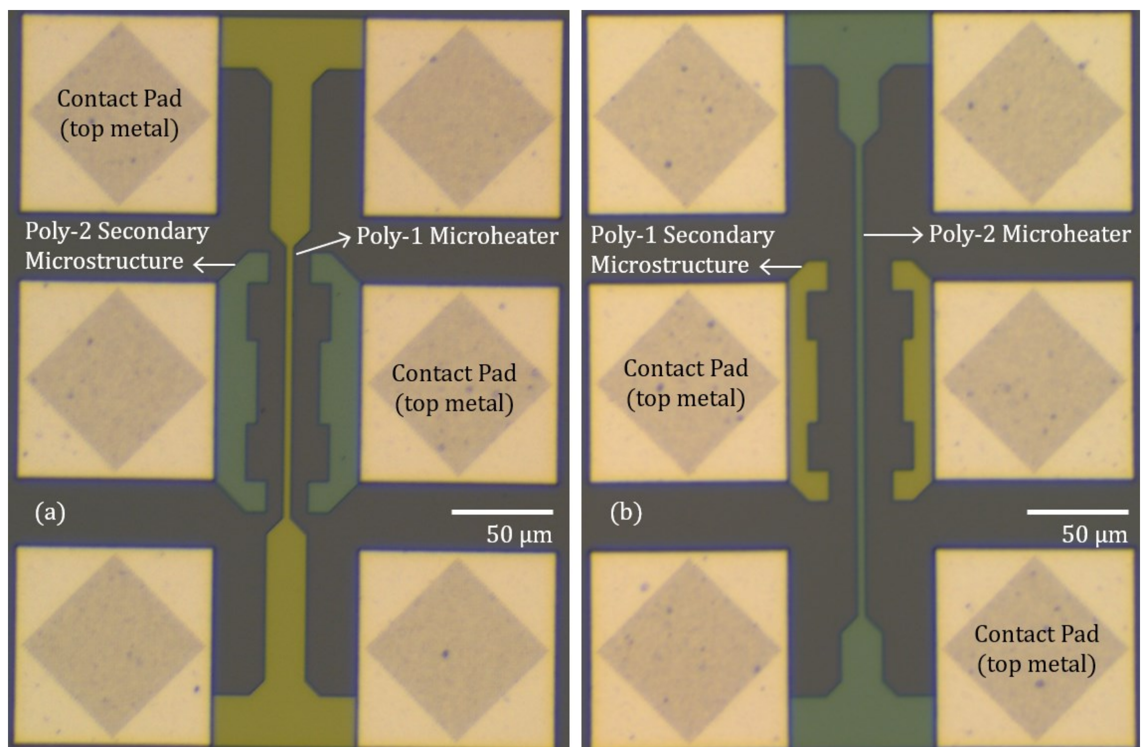


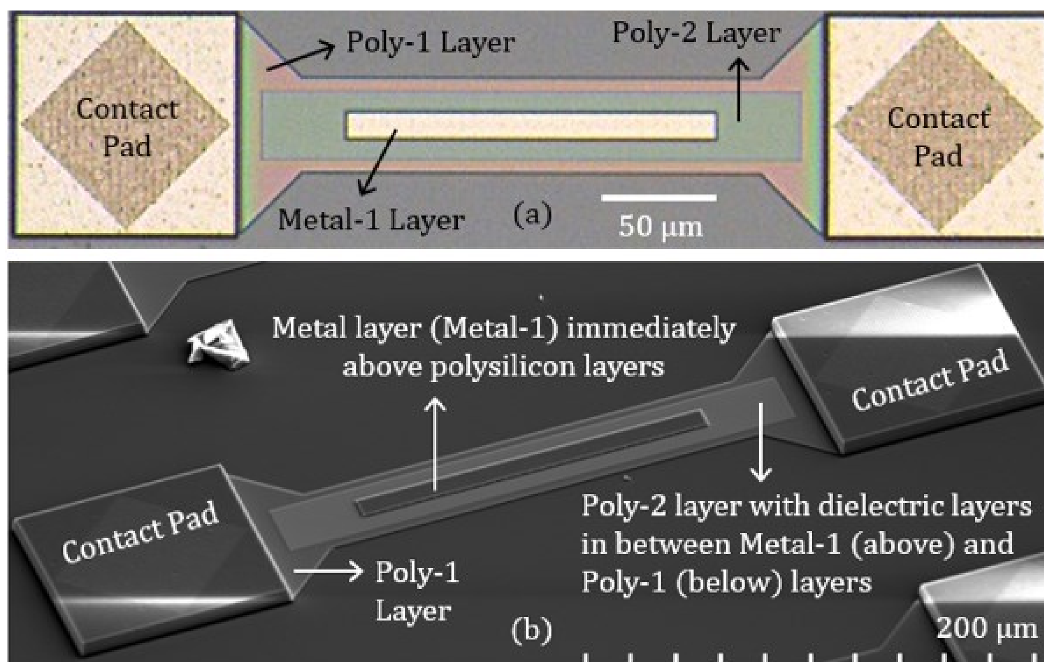
Figure 3.15: Four-terminal polysilicon heaters with two separate secondary microstructures. Optical micrographs of (a) poly-1 heater with poly-2 secondary structures and (b) poly-2 heater with poly-1 secondary structures.

3.3.7 Microheaters with four terminals

Two polysilicon microheaters were also fabricated with four terminals as shown in *Figure 3.15*. This arrangement was useful for the application of temperature sensing as detailed in *section 8.2*, where accurate resistance measurements were important. The configuration also has two secondary microstructures, which were included with the intension to increase possibility for CNT connection.

3.3.8 Microheaters with stacked polysilicon layers

The two polysilicon layers can be stacked to form thicker microheaters. Cross-sectional illustration of such a microheater is presented in *Figure 2.7*. The typical polysilicon layers in a CMOS process are very thin (~200-300 nm). In applications as heaters, thicker polysilicon layers are preferred for enhanced mechanical stability at high temperatures. Therefore, the heaters in *Figure 3.16* were fabricated with both poly-1 and poly-2 layers, where the latter is stacked over the prior layer with a dielectric layer in between them. In a larger heater design, the bottom metal layer was also stacked (*Figure 3.16a & 3.16b*) for experimental purpose; the layers can be distinguished in the 3D view of *Figure 3.16b*. Heaters stacked only with poly-1 & poly-2 layers are shown in *Figure 3.16c, 3.16d & 3.16e*; the via was placed in these designs to fulfil the required IC design rules.



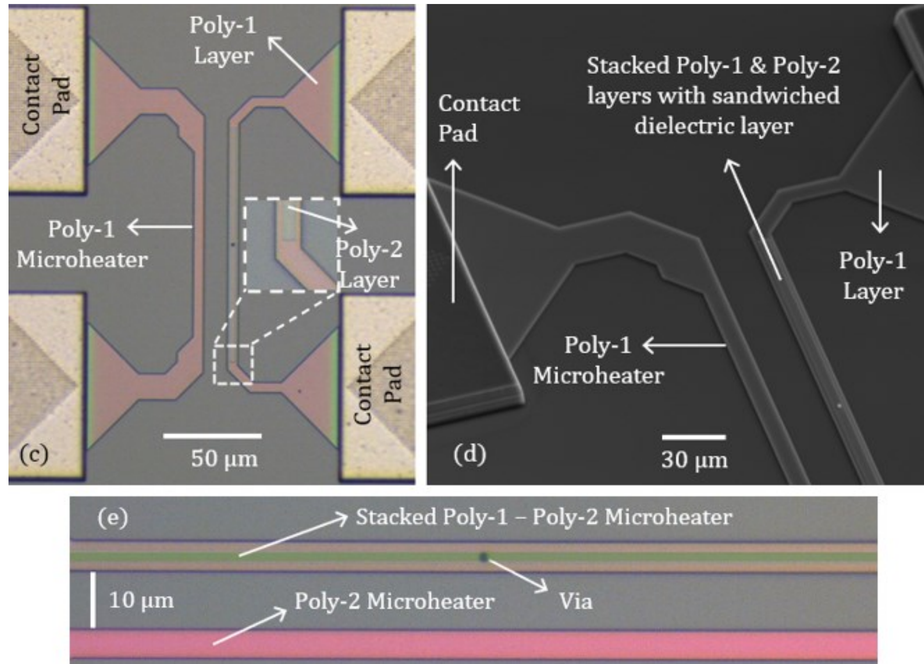
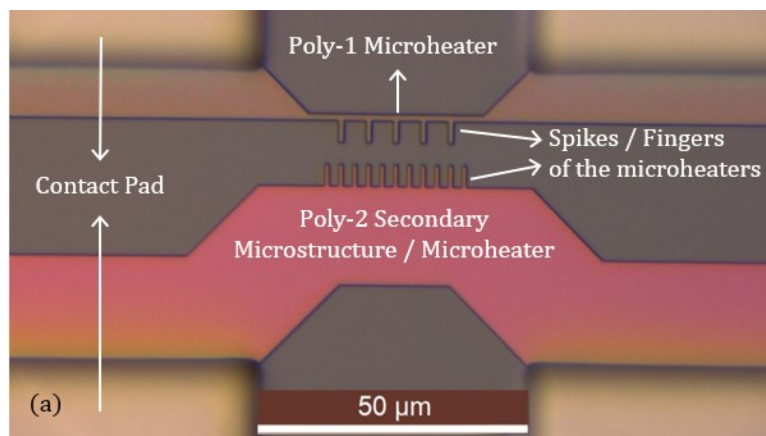


Figure 3.16: Microheaters with stacked poly-1 & poly-2 layers. (a) Optical and (b) electron micrograph of a heater with stacked bottom metal above the polysilicon layers; (c) Optical and (b) electron micrograph of a stacked Poly-1 – Poly-2 microheater, (e) close-up of a similar heater design.

3.3.9 Microheaters with spikes

In this design, the polysilicon microheaters have spikes or fingers in one of the sides as demonstrated in *Figure 3.17*. This resembles a comb-drive like configuration. A local electric field can be applied between the two heaters by supplying a voltage across them. The finger structures of the heaters are intended to focus such electric field on their tips. For application of CNT integration, it can be beneficial to guide the growing CNTs towards the spikes.



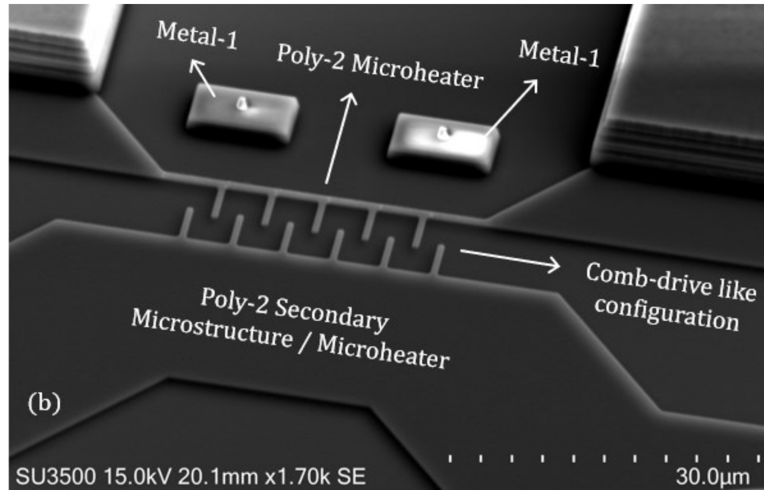


Figure 3.17: Polysilicon microheaters with spikes or fingers. (a) Optical micrograph of poly-1 and poly-2 heaters; (b) Electron micrograph of poly-2 heaters that resemble a comb-drive like configuration.

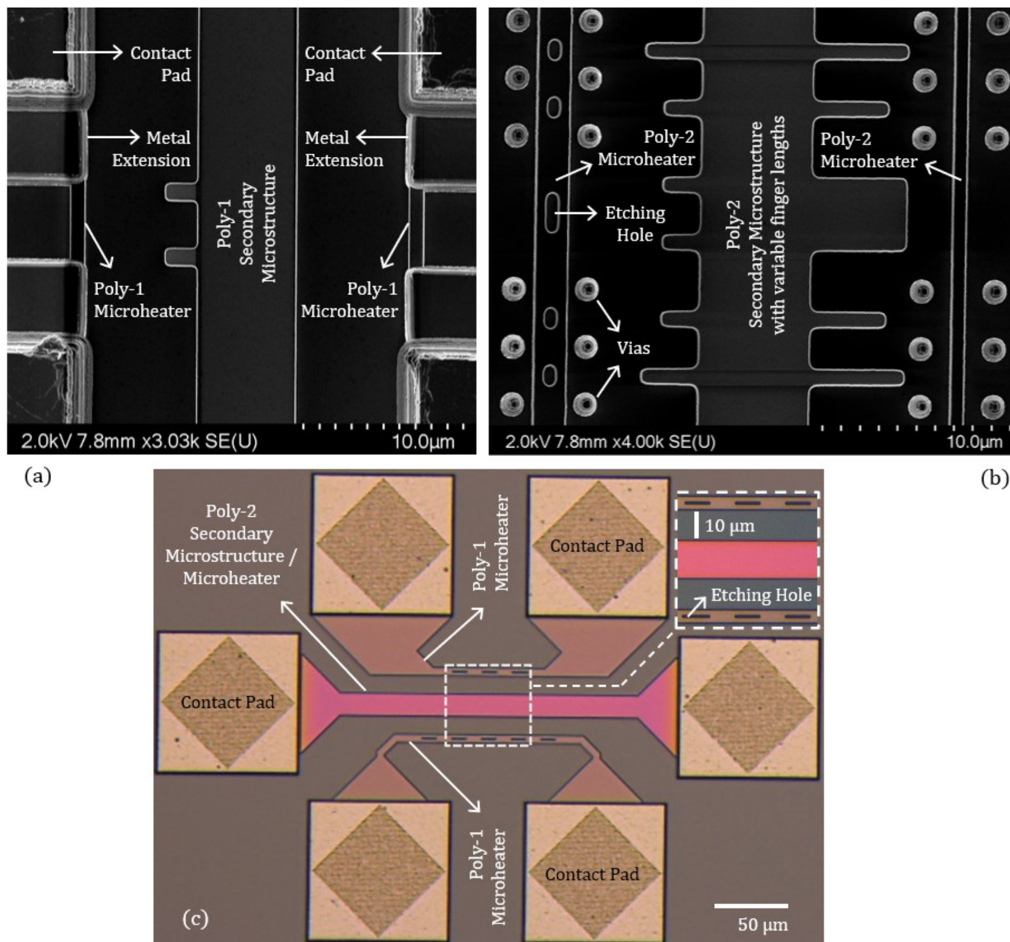


Figure 3.18: Arrangement of a larger polysilicon heater with two smaller microheaters on the opposite sides. SEM images of various (a) poly-1 and (b) poly-2 microheaters; (c) Optical micrograph of two poly-1 microheaters on two sides of a poly-2 heater.

3.3.10 Three-microheater configuration

In this approach, three microheaters are placed in parallel. Two smaller microheaters are situated on two sides of a larger heater in the middle as shown in *Figure 3.18*. The two smaller heaters on the sides are designed for synthesizing CNTs, while the middle heater is intended as a secondary structure. This design allows experimenting with different microheaters in the same configuration. *Figure 3.18a* and *Figure 3.18b* are arrangements of poly-1 and poly-2 heaters, respectively. *Figure 3.18c* shows a combination of two poly-1 heaters with a poly-2 heater / secondary structure.

3.3.11 Rectangular arrangement of microheaters

The purpose of this design is to fabricate microheaters with increased resistance by length extension while properly utilizing the valuable space of the CMOS chips. *Figure 3.19* shows long poly-1 and poly-2 microheaters with corresponding secondary heaters / structures placed in between the contact pads of the long heaters. The polysilicon heaters with the extended lengths (> 600 µm) are the longest fabricated heaters in our CMOS chips. The longest poly-2 heater with ~ 1 µm width has the maximum resistance (~ 18.5 kΩ) among all the designed microheaters.

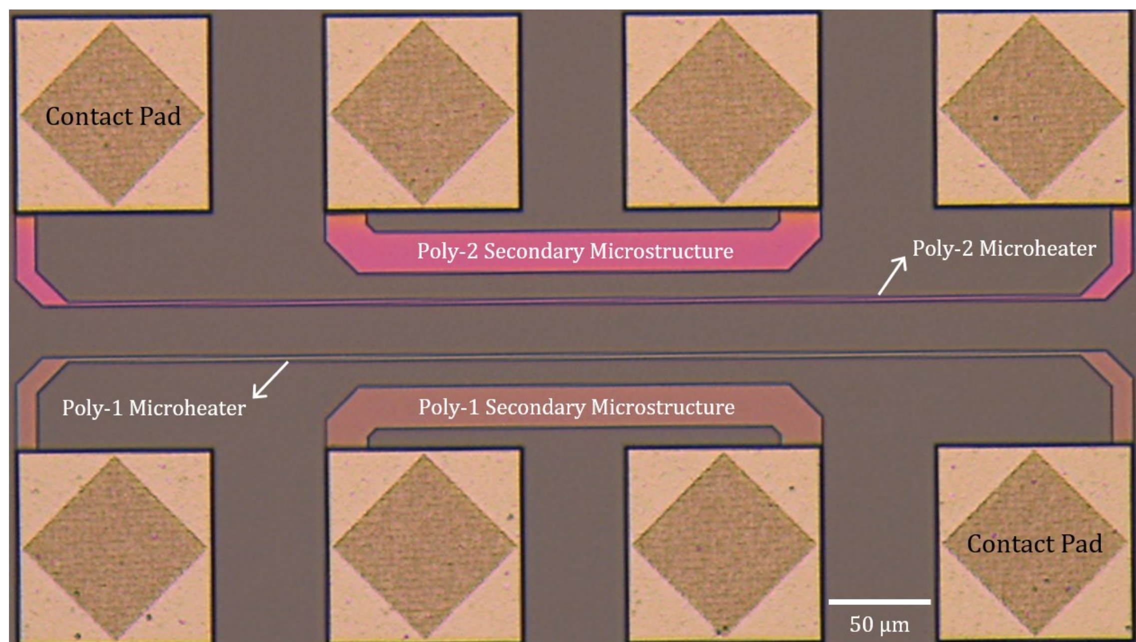


Figure 3.19: Optical micrograph of polysilicon microheaters with rectangular configuration.

3.3.12 Microheaters with small and large surface area

For non-suspended microheaters, larger surface area corresponds to higher heat loss by thermal conduction through the underneath dielectric layer, which results in higher surrounding temperature on the CMOS chip. For the suspended heaters, wider structure can be beneficial for mechanical stability. Microheaters with various surface areas were

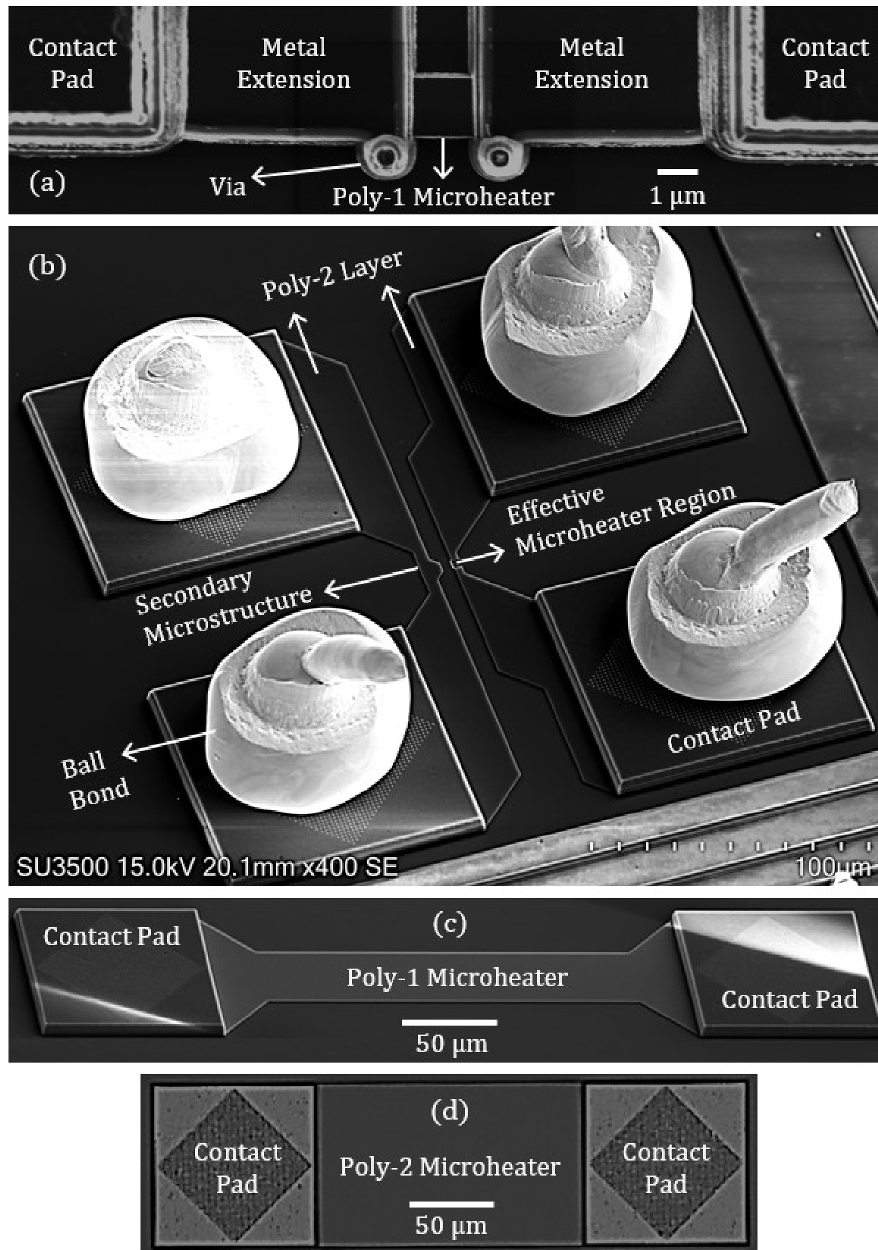


Figure 3.20: Polysilicon microheaters with small and large surface areas. Micrograph of (a) poly-1 heater with the smallest surface area, (b) poly-2 heater with a small effective heating region, (c) poly-1 heater with a large surface area, and (d) poly-2 heater with the largest surface area.

fabricated in our CMOS chips. Among them, the heaters with small and large surface areas are presented in *Figure 3.20*. The microheater with ~2 × 1.5 µm surface area (*Figure 3.20a*) was the smallest heater fabricated in the CMOS chips. This microheater is a reliable choice as a non-suspended heater to obtain local high temperatures without significant increase in ambient temperature due to its low heat-conduction path. It also offers lower risk of deformation when fully suspended due to the reduced length. Another heater with small surface area in the effective heating region is shown in *Figure 3.20*b. *Figure 3.20c & 3.20d* presents two heaters with large surface areas; the latter has the maximum surface area (95 µm × 155 µm) among all fabricated heaters. It has been verified that the ambient temperature become CMOS-incompatible when these two heaters are operated at maximum sustainable temperatures; details are in *section 8.3*.

3.4 Microheater characterizations

The CMOS layers used for the fabrication of microheaters have different thickness. The polysilicon layers are ~200-300 nm thick; the poly-1 layer is ~1.5 times thicker than the poly-2 layer [256–258]. The stacked poly-1 and poly-2 layers have ~40 nm thick dielectric layer in between them [256–258]. Electrical resistivities of the structures are calculated

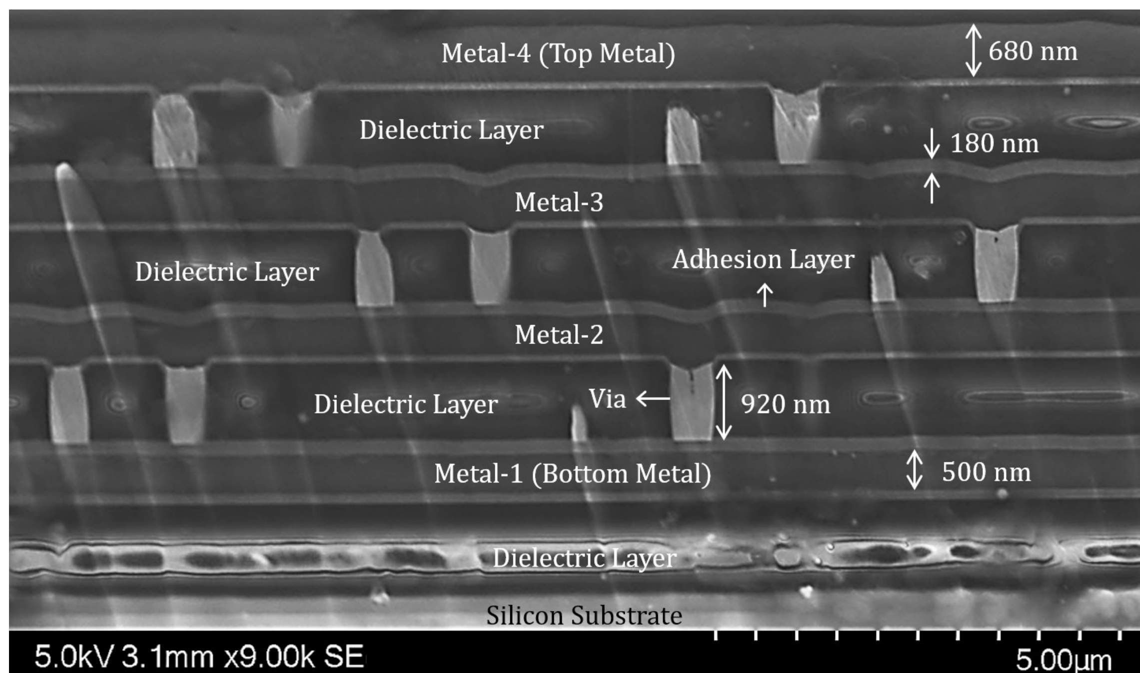


Figure 3.21: Electron micrograph of a custom-designed contact pad cross-section.

through their dimensions; poly-2 has around 4-times higher resistivity than poly-1. The sheet resistance of poly-2 is ~5-6 time higher than that of poly-1. A cross-sectional micrograph of a custom-designed contact pad is shown in *Figure 3.21*; it shows thickness of the four aluminium layers along with vias and dielectric layers. The metal microheaters are mostly designed with Metal-3 and Metal-4 layers. For the initially designed CMOS chip, Metal-1 was used for the extension from contact pads to connect with the polysilicon layers. Both Metal-1 and Metal-2 layers have been used as etching masks along with vias for different polysilicon microheater designs as demonstrated in *section 3.3.1 & 3.3.2*.

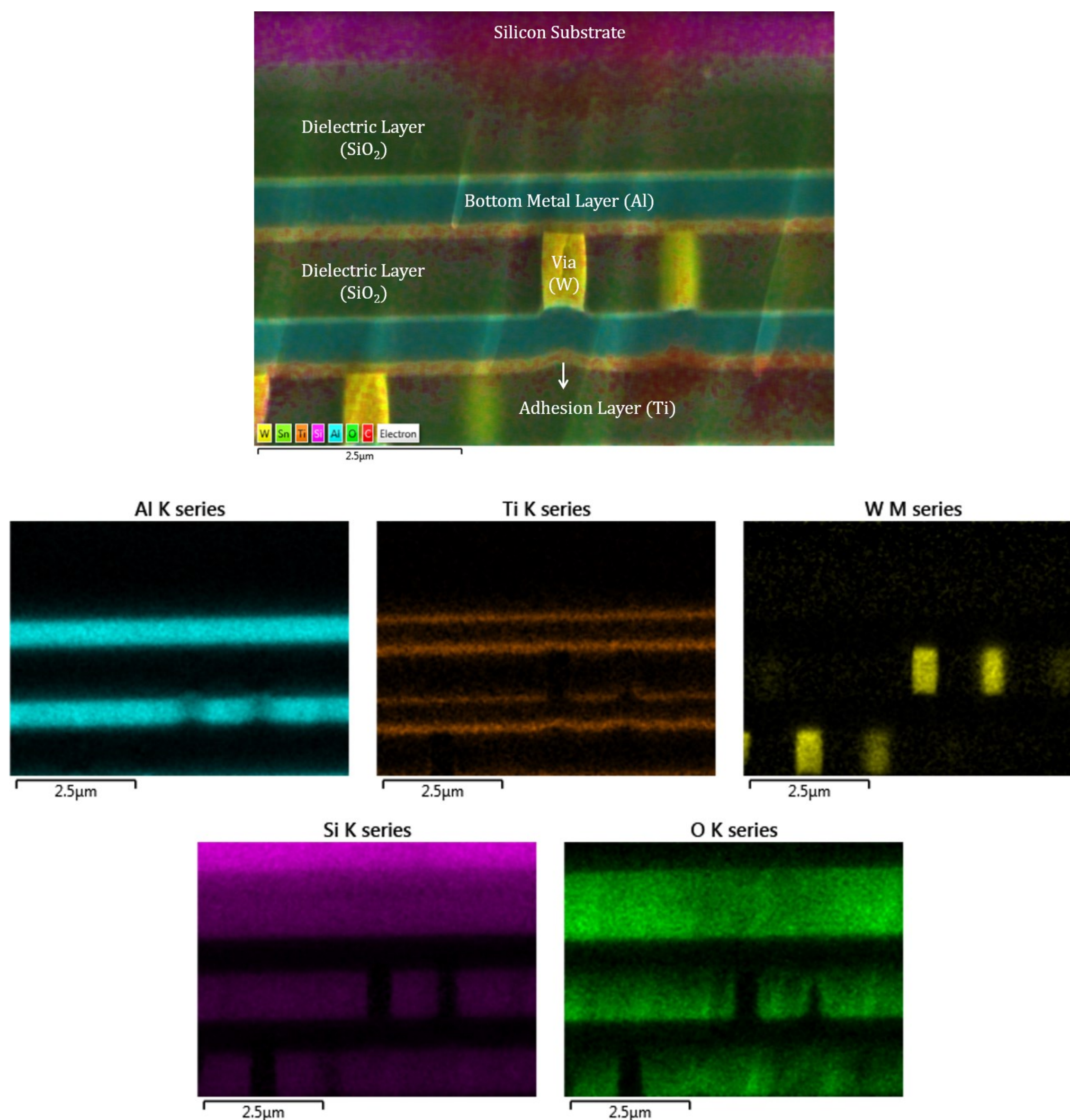


Figure 3.22: EDX analysis of a region in contact pad cross-section.

Apart from the top metal, the other aluminium layers are sandwiched between thin titanium nitride (TiN) layers, which act as adhesion layers for connecting with the tungsten vias [259,260]. The top aluminium layer only has TiN layer in the bottom surface. Energy dispersive x-ray spectroscopy (EDX) analysis of a cross-section in *Figure 3.22* confirms the involved materials of the relevant layers; since the chip was upside down during the analysis, the silicon substrate can be seen on the top. The dielectric layer is made of SiO_2.

Table 3.1: Characterizations of different metal and polysilicon microheaters.

Heater	Surface area* (μm × μm)	Design	R (Ω)	V_{max} (V)	P_{max} (mW)
Top metal	~10 × 0.7 (c); ~210 × 2.5 (s)	Figure 3.2a	~12.5	1.2	~100
Poly-1	8.2 × 0.8	Figure 3.5a, 3.5b	~112	2.1	~10
	8.3 × 2.5 (e)	Figure 3.3	~36.5	1.7	~45
Poly-2	~27 × 1.5	Figure 3.4, 3.8	~2500	19	~110
	~4.7 × 0.7 (e)	Similar to Figure 3.20b	~1425	4.2	~11
Poly-1 – Poly2	~8.8 × 3.7	Poly-2 on Poly-1	~25	1.9	~80
Top metal	~220 × 5	Similar to Figure 3.1a	~5.25	1.7	~335
Poly-1	~400 × 2 (e)	Figure 3.12c	~2500	40**	~540
	~32 × 1 (e)	Figure 3.17a	~430	10	~140
Poly-2	~36 × 3 (e, h)	Figure 3.9b, 3.9c	~1650	25	~290
	~20 × 6.2 (a)	Figure 3.13c, 3.13d	~625	21.5	~600
Poly-1 – Poly2	~185 × 5 (e)	Figure 3.16c, 3.16d	~350	29	~1370

***** c: centre region, s: side regions, e: effective heating region, h: has etching holes, a: average width

****** Max voltage of the power supply reached, but the microheater was not broken.

The microheaters have been characterized in different approaches throughout the CMOS post-processing and CNT synthesis process. Initial characterizations of some the heaters with different features are summarized in *Table 3.1*. Other characterizations of

various microheaters can be found in *section 4.7, 4.8, 5.4, 5.5, 7.2, 7.3, 8.2 & 8.5*. The room-temperature resistance values of the microheaters can differ by tens of ohms from chip to chip, mostly due to thickness variations in the layers. However, electrical resistivity values of the layers are considered to be similar over the manufactured CMOS chips. The first 6 heaters are from the initially designed CMOS chip. There are some fundament design changes between the microheaters in initial and final CMOS chip, which are detailed in *section 4.5*. Maximum voltage (V_{max}) and power (P_{max}) of the heaters were taken before their breaking point.

3.5 IR microscopy

Thermal microscopy of the microheaters from initially designed (previous generation) CMOS chip was attempted using a high-performance infrared camera, FLIR A6750sc MWIR (Mid-wave IR) with a 4X microscopic lens. An uncalibrated camera was rented; hence, it was calibrated by the author. It is ideal to use a black body for the calibration. Due to unavailability of black body, a hot plate was used with Kapton tape applied on the centre of the surface to increase the emissivity. Kapton tape has an emissivity of around 0.95. For measuring reference temperatures, both IR thermometers and thermocouples were used. A range of calibration points were added using the software 'ResearchIR' for increased hot plate temperatures; the fitted plot was linear.

The experimental setup is shown in *Figure 3.23*. A probe station was used for supplying current to the microheaters in the CMOS chips; inset of *Figure 3.23* shows probe tips connected to the contact pads of a microheater. The probe tips were placed using the mechanical probe positioners with the help of optical microscope. Then the optical microscope was moved, and the thermal camera was positioned on top of a CMOS chip. While the surface temperatures of the CMOS chips can be measured easily, accurate microheater temperatures were not determined due to fundamental resolution limitations. The camera operates at 3–5 µm wavelengths, with the minimum spot pixel size of 3 µm × 3 µm. The camera also needs an array of 3 × 3 pixels for an adequate thermal measurement. Hence, the narrowest microstructure dimension needs to be at least ~9 µm to obtain acceptable measurements, while most of our microheaters only

have a ~1 µm widths. Therefore, accurate temperature data for the microheaters was not achieved, as the obtained temperature values from the microheaters have an average of the heater temperature and surrounding area temperature of the heater.

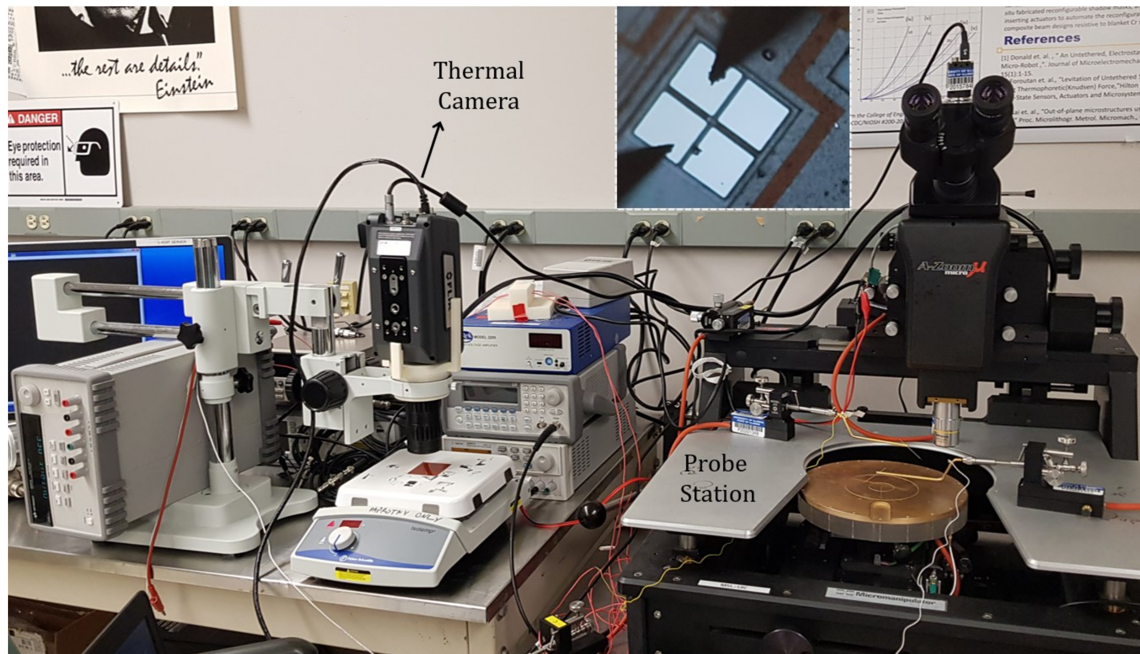


Figure 3.23: Setup for thermal microscopy of microheaters; hotplate with Kapton tape for calibration, and probe station with optical microscope for establishing electrical connections to the contact pads (inset).

Figure 3.24 shows an infrared image of the Al microheater presented in *Figure 3.1d & 3.2c*. Although maximum temperature on the microheater appears to be ~170 °C in *Figure 3.24*, the actual heater temperature was much higher. This was confirmed since the Al microheater was melted at the region of maximum temperature when the electrical current through the heater was slightly increased. Therefore, we could estimate that the actual temperature on that hottest spot of the Al microheater was ~660 °C (melting temperature of Al).

The thermal measurement of the surface surrounding the microheater was accurate, which shows a temperature of ~30 °C. Although the temperature measurement on the microheater was not accurate, due to resolution limitation, it is still a positive indication that the surrounding CMOS chip area remains at near room temperature while the Al heater reaches near melting temperature. This showed a convincing sign towards

agreement with the thermal simulation results and maintaining CMOS-compatible temperatures at high microheater temperatures.

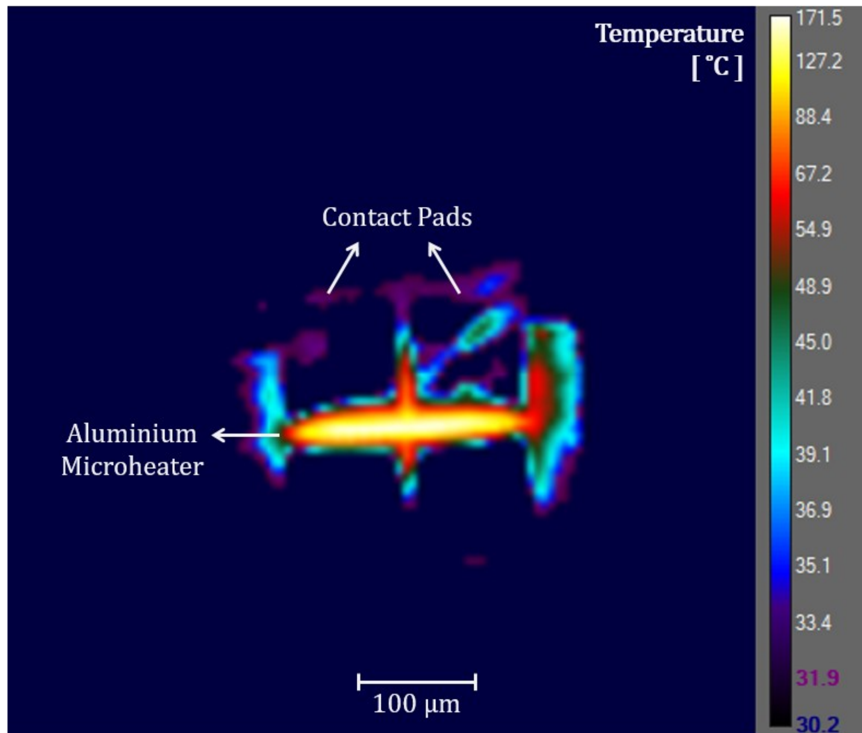


Figure 3.24: Thermal micrograph of an aluminium microheater on a CMOS chip.

IR image of the CMOS chip while resistively heating a polysilicon microheater is shown in *Figure 3.25*. It demonstrates the low ambient temperature in the chip with local microheater temperature. As the microheater temperature is much higher than the indicted value, a high thermal gradient around the heater is obtained, which agrees with the thermal simulation results of polysilicon microheaters.

Polysilicon microheaters of the previous generation CMOS chips were very small. Even though they generated higher temperatures than the aluminium heaters, it was not reflected by the measurement values due to the resolution limitations. *Figure 3.26a* shows hot probe tips during the joule heating process. Due to the small dimensions of the polysilicon microheaters, single pixel IR measurement was attempted (*Figure 3.26b*). In the latest generation CMOS chips, some larger microheaters (such as *Figure 3.16a, 3.20c, 3.20d*) were fabricated to ensure compatibility with IR microscopy, however, IR measurements were not performed on those chips.

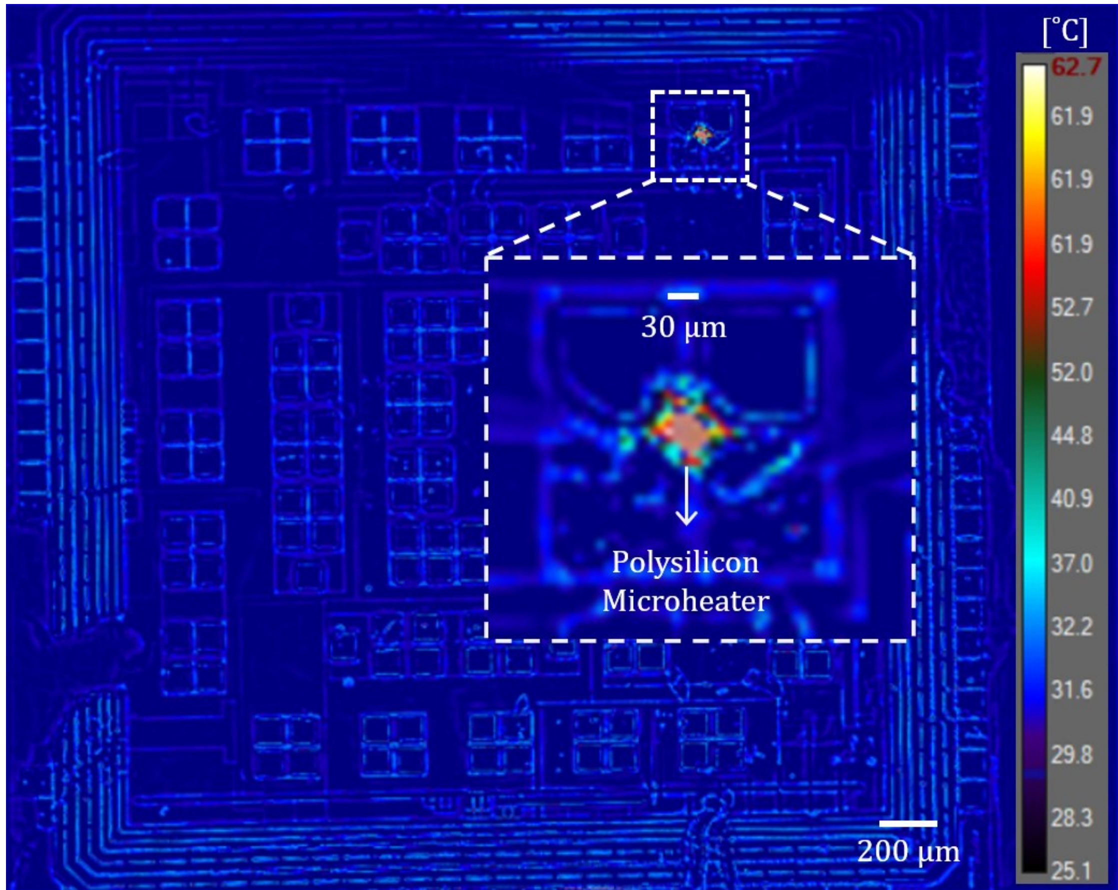


Figure 3.25: Thermal image of a CMOS chip during the local heating of a polysilicon microheater.

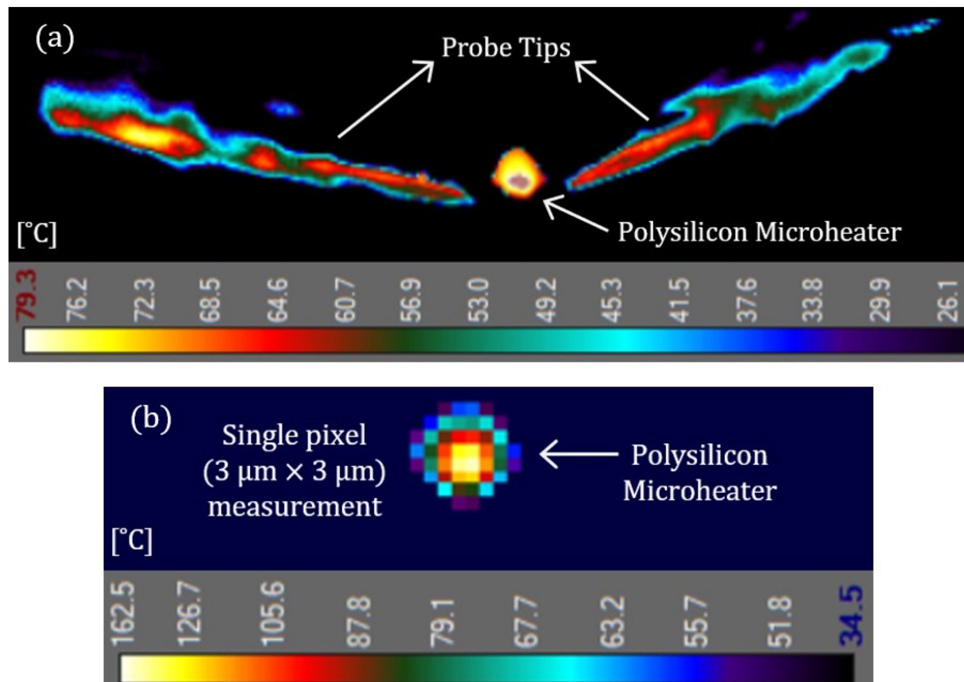


Figure 3.26: Thermal microscopy of polysilicon microheaters. (a) Hot probe tips; (b) Single pixel.

3.6 Conclusion

CMOS chips with various metal and polysilicon microheaters were designed and fabricated in a standard AMS 350 nm CMOS technology. Layout and micrographs of different microheaters made of poly-1, poly-2 and Al were presented. The designed chips have microheaters with various features including via or top metal layer as etching mask, heaters with etching holes, heaters with different shapes and sizes, heaters with stacked polysilicon layers. Initial characterization of different microheaters were presented. Results from IR microscopy were shown and the resolution limitations for the microheaters were addressed.

Chapter 4

Post-processing of CMOS-MEMS Microheaters

4.1 Introduction

Developing the post-processing of CMOS-MEMS microheaters has been challenging and time-demanding, which is typical in the SoC integration approaches due to lower fabrication flexibility [192]. During any post-CMOS MEMS integration process, it is necessary to ensure that the on-chip CMOS electronics are not affected. Therefore, a carefully conceived post-CMOS microfabrication process is required along with thoughtful design of the CMOS chip. Successful post-processing of CMOS chips to realize CMOS-MEMS heaters is the key for locally growing CNTs in CMOS, which can potentially lead towards commercial production of low-cost CNT-based sensors. Two generations of CMOS chips were designed and fabricated in an industrial CMOS process to grow CNTs on the CMOS-MEMS heaters. Based on post-processing results of the older generation CMOS chips, design improvements were made on the succeeding generation, and post-processing approaches were modified accordingly. We experienced that proper design of the microstructures plays a very important role in realizing the CMOS-MEMS structures along with the selection of appropriate post-processing approaches. In this section, the development of post-CMOS processing is discussed along with the encountered post-processing challenges. The incorporated design upgrades in the latest generation CMOS chip to successfully fabricate CMOS-MEMS microheaters is also presented. Most results from this chapter are presented in *Article 3 (to be submitted – manuscript enclosed in the thesis)*, while contents from *section 4.6 & 4.7* will be included in planned publications. The results in *section 4.8* is preliminary work, where the feasibility of Ni electroplating on Al microheaters was checked.

4.2 Polysilicon microheater design layers

A CMOS chip with various metal and polysilicon microheaters was designed and fabricated in a standard AMS 350 nm process. For local synthesis of CNTs, the polysilicon

heaters were the primary preference due to their material properties. Numerous microstructures of the two polysilicon layers (poly-1 and poly-2) have been presented in *section 3.3*. The polysilicon microheaters are connected to custom designed contact pads made of stacked inter-connecting aluminium layers, where the electrical connection can be established on the exposed top metal layer. In the tilted cross-sectional view (*Figure 4.1*), a contact pad with all metal layers is presented. The electron micrograph was taken after removing the dielectric layer, which resulted in a clear view of the layers including the vias (inset).

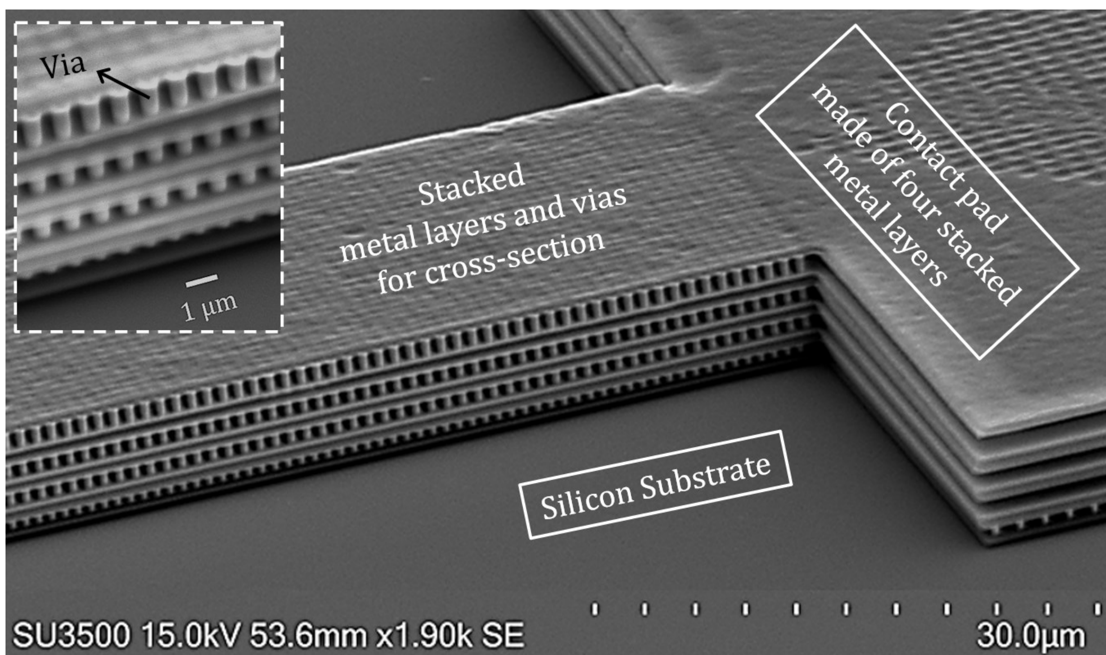


Figure 4.1: SEM image of a contact pad and stacked metal layers with vias in a 3D cross-sectional view.

From the first-generation CMOS chip, a typical design containing polysilicon microheaters and associated contact pads have been presented in *Figure 3.1*. In the microheater designs, the objective was to make polysilicon resistors that can efficiently generate CNT synthesis temperature by local resistive heating at low power and minimum heat loss. Reduction in the microheater surface area is beneficial in limiting conductive heat loss. Therefore, widths of the designed polysilicon heaters were mostly kept within the range of 0.7 µm to 1 µm, 0.7 µm being the lowest valid dimension for poly layers in the used CMOS technology. For efficient heating, a designed microheater should have the dominant resistance within the joule heating circuitry to avoid heat loss.

Considering the boundary conditions, the heaters were designed within a varied length ranging mostly from 6 - 15 µm. A minimum distance of 15 µm is considered between two contact pads for the ease of wire bonding. To ensure this distance, only the bottom metal layer is extended to connect with the polysilicon layer as seen in *Figure 3.3*.

A cross-sectional illustration in *Figure 4.2* reveals all the layers in a CMOS polysilicon microheater design. The heater is surrounded by SiO_2 dielectric layers and connected with the extended bottom metal layer through a few vias. The top contact pad connects to the bottom metal layer through two more metal layers and corresponding arrays of vias. The surface of the dielectric layer is normally covered with passivation / protection layers in typical CMOS chips. Our chips need post-processing steps to expose the poly layers for the purpose of CNT synthesis. Therefore, through the selective placement of a design layer, the passivation layers are avoided over the microheaters. In this way, the passivation layers are only removed on the indicated regions during the CMOS fabrication process, while the regions over the CMOS circuits are still protected by the passivation layers made of silicon nitride [261,262]. As a result, we can avoid several post-processing steps needed for selective removal of the passivation layers.

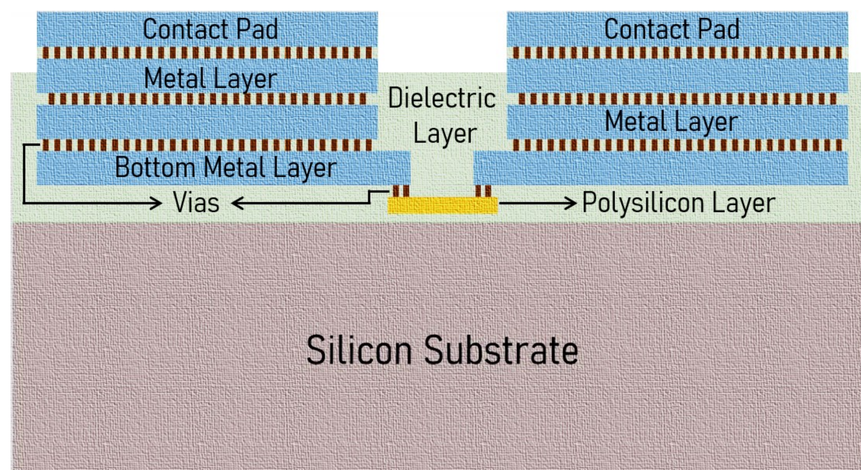


Figure 4.2: Cross-sectional illustration of a polysilicon microheater with associated layers, designed in the first-generation CMOS chips.

Figure 4.3 shows the surface profile of different CMOS layers in a first-generation chip before any post-CMOS fabrication / etching. The height difference between the regions with passivation layer and top metal layer is ~0.9 µm. The dielectric layer is ~2 µm lower

than the top aluminium layer in the non-passivated regions. There is no significant surface roughness on the layers.

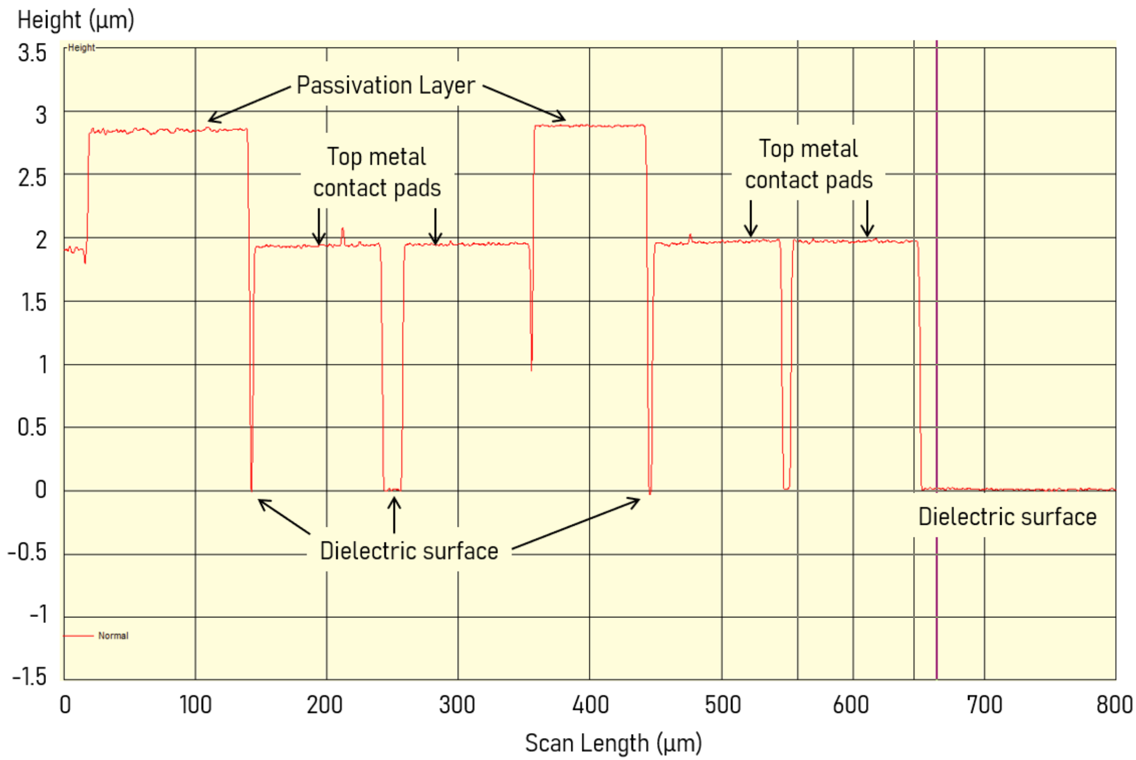


Figure 4.3: Surface profile of a CMOS chip before any post-CMOS processing.

4.3 Fabrication process of CMOS-MEMS heaters

In the subtractive post-CMOS processing technique, the thick dielectric layer needs to be removed to realize CMOS-MEMS microstructures. The cross-sectional illustrations in *Figure 4.4* indicate the process steps. *Figure 4.4a* shows the view of a fabricated chip after receiving from the foundry, where the microheater region has no passivation layer. The polysilicon microstructures are exposed by etching SiO_2 layer. It is essential that the selectivity between SiO_2 and polysilicon is very high to keep the polysilicon structures intact during the dielectric etching. For SiO_2 etching, buffered oxide etch (BOE) is commonly used. Although this wet etching process provides high selectivity between SiO_2 and polysilicon, aluminium metal layer is highly affected in this etching process. Also, a wet etching process carries the risk of contaminating the delicate CMOS chip surface. Therefore, a highly selective dry etching process is more suitable for this step.

The substrate temperature of the sample holder must not exceed CMOS-compatible temperature during the dry etching process. It is also important to maintain CMOS-compatible temperature during the CNT synthesis process.

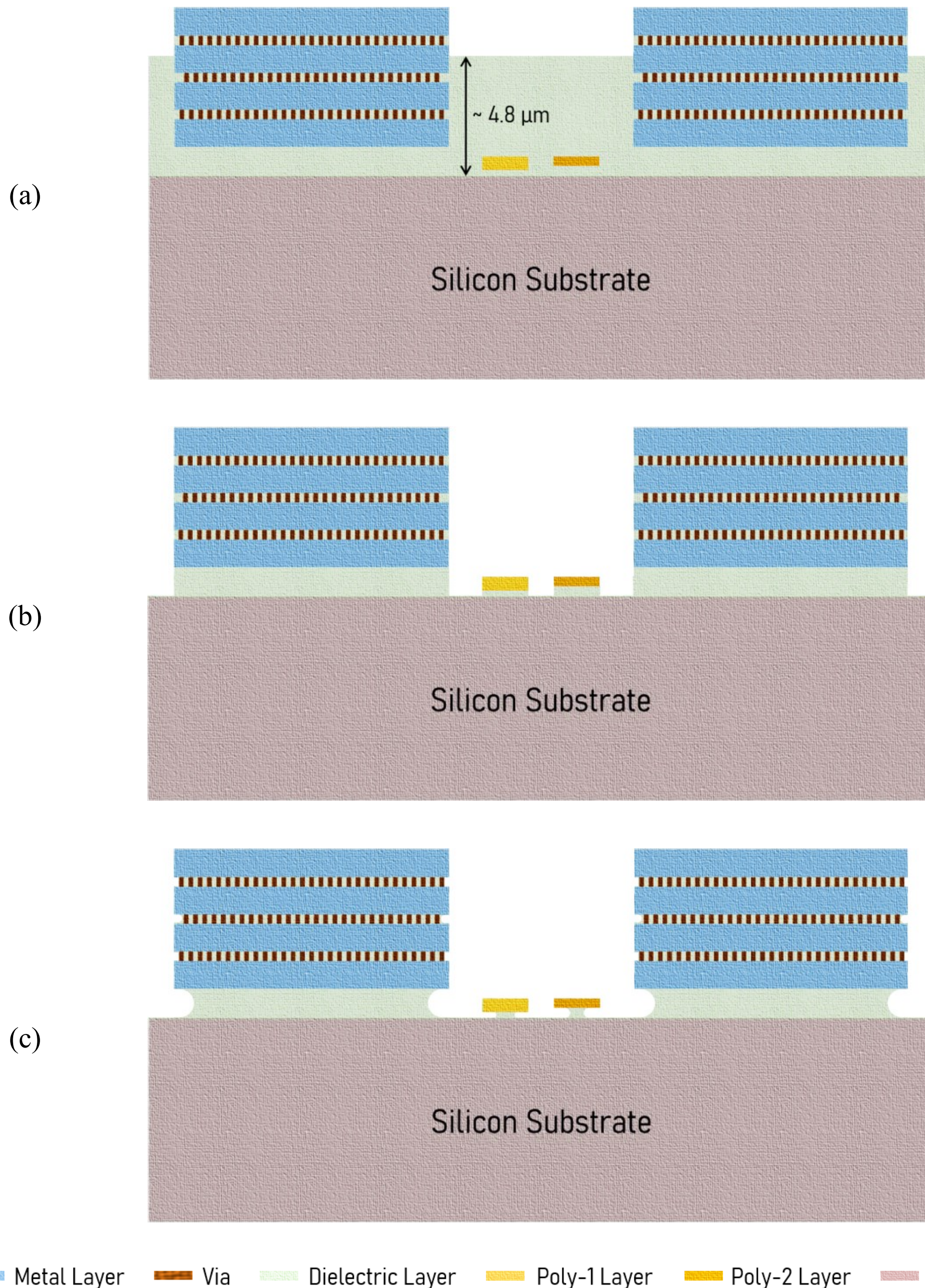


Figure 4.4: Required steps of post-CMOS processing for realizing CMOS-MEMS polysilicon microheater. (a) Initial view after receiving the chips from CMOS foundry, (b) dry etching of the exposed dielectric layer, and (c) wet etching for limited duration to partially or fully suspend the microheaters.

The high temperature on the microheater during the CNT growth process should be highly localized. The CMOS microheaters can be partially or fully suspended by etching the dielectric layer underneath the heaters to reduce or remove the heat conduction path from the heater to the Si bulk. As the width of microheaters are within 1 um, dry etching can suffice to partially release the heaters unless the etching process is completely anisotropic. To fully release the microheaters, a time-controlled wet etching process can be performed, where the risk of stiction should be taken into consideration.

4.4 Post-processing challenges and heater design limitations

To expose the polysilicon layers, etching of ~4.2 µm thick SiO_2 layer is required. As the opening over the microheater region is small, deep reactive ion etching (DRIE) becomes an initial preference. The used recipe for the SiO_2 DRIE (named as dry etching recipe, DER-1) provided high etch rate and high aspect ratio. The etching profile, as obtained by profilometry, in *Figure 4.5a* shows that the etched depth in the regions of small openings were similar to the regions with large openings. However, the selectivity of DER-1 was very poor, resulting in significant etching of the polysilicon layers once they become exposed. Therefore, a new SiO_2 etching recipe (DER-2) was chosen in a RIE system with inductively coupled plasma (ICP) source, which facilitated a wider range of gases. Details of all the applied etching recipes are presented in *section 4.6*.

Etching with DER-2 ensured decent selectivity between polysilicon and SiO_2, however, it also resulted in non-uniform etching due to low aspect ratio. The surface profile in *Figure 4.5b* shows the lower etching depth in the regions with small opening. The passivation layer etched at a slower rate in both recipes, resulting in thick dielectric in those regions as seen in *Figure 4.5a* and *Figure 4.5b*. It can also be noticed that the surface roughness of the structures in *Figure 4.5b* is higher compared to the results in *Figure 4.5a*. The temperature of the sample holding substrate was not controllable in the used RIE system, hence, the samples were at an elevated temperature during the RIE process, which can be the reason for the higher surface roughness. Introduction of a cooling cycle (using argon) in between short etching cycles helped in improving the surface profile, as well as reduced etching of the passivation layer.

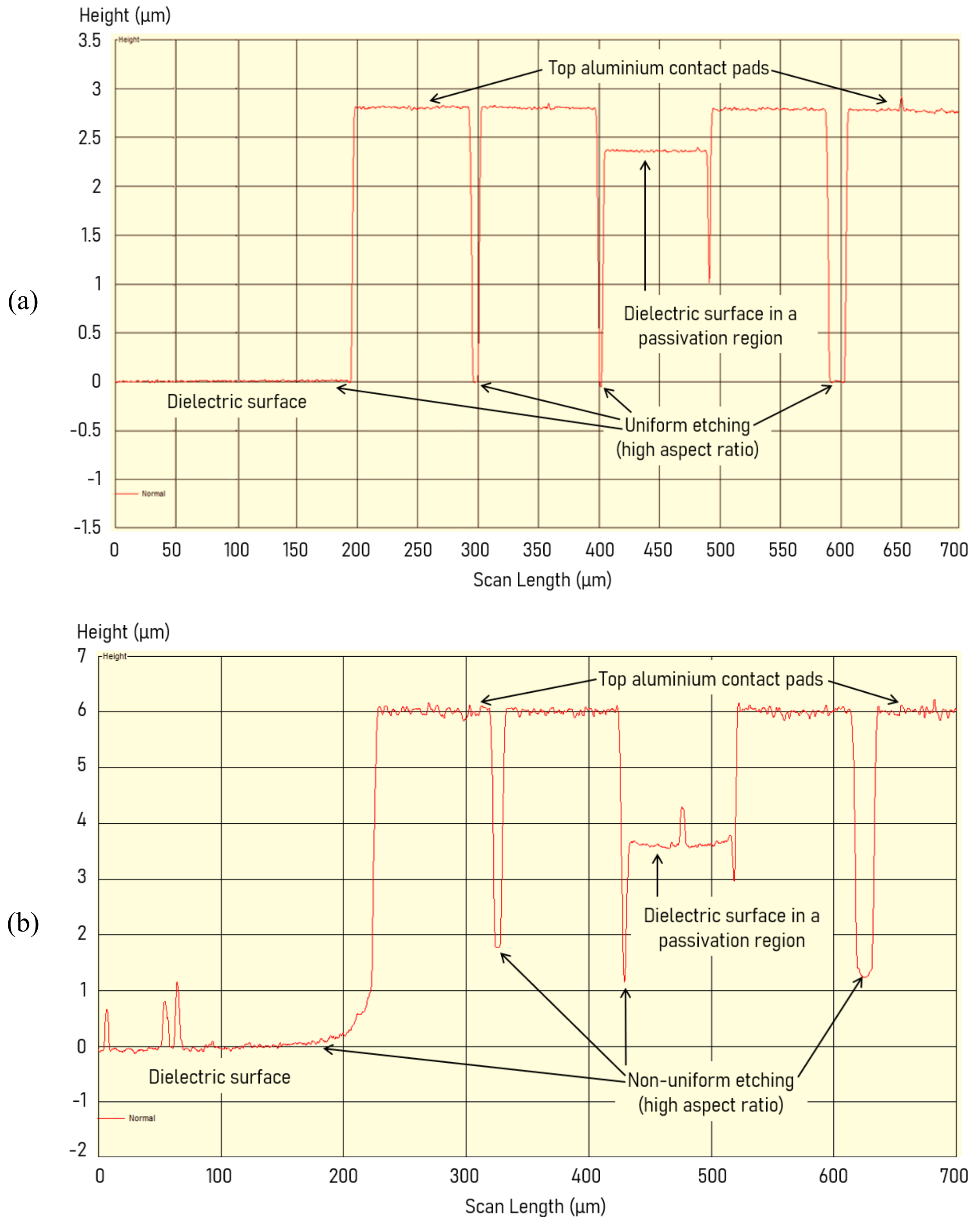


Figure 4.5: Etching profile after (a) DRIE using DER-1 and (b) RIE with ICP source using DER-2 recipe.

It is important to achieve a more uniform etching profile. The CMOS chip has regions with small and large openings or etching windows as presented in the entire chip layout (*Figure 4.6*); the microheater regions have the smallest window for dielectric etching. The gray regions in the CMOS chip has no passivation layer, while the regions with electronics in white background is protected by the passivation layer.

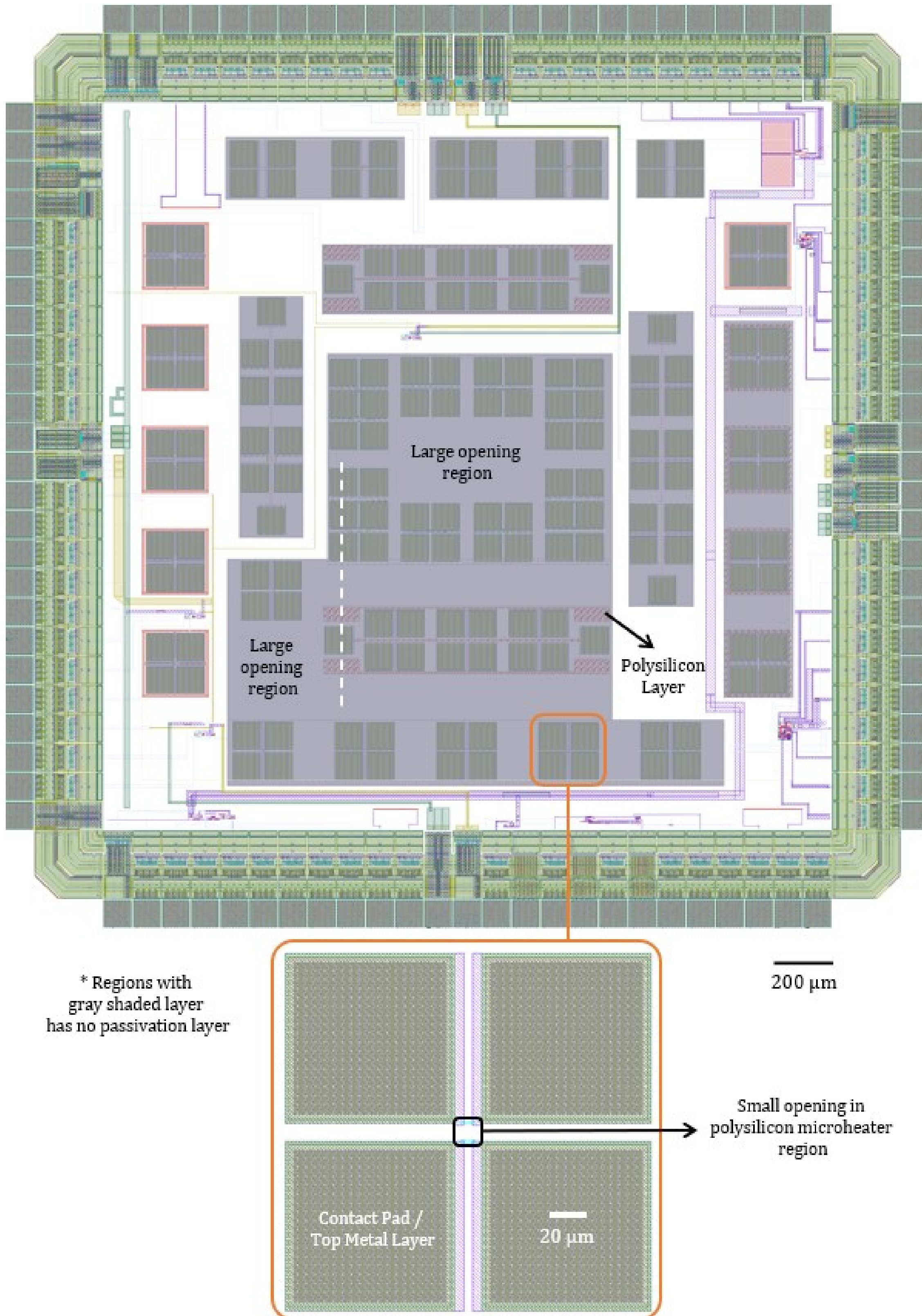


Figure 4.6: Layout design of the first-generation CMOS chip with small opening for the polysilicon microheater region.

As the opening area over different microheater designs are not the same, a variable etching depth due to lower aspect ratio means some microheaters will be exposed earlier than the others. As a result, if etching duration is increased for exposing the heaters with smaller opening area, the already exposed heaters will be at risk of getting etched since the etching selectivity is not extremely high.

The issue of low aspect ratio is also relevant in the microheater characterization. It is challenging to identify weather the microheaters are exposed. An optical method of characterization (such as interferometry) is not useful as the heaters are covered by transparent SiO_2. Due to the small opening area and dimensions of the heaters, measuring with a profilometer is challenging, and the measurements are also limited by the diameter of the probe tip. Observing cross-sections is an effective method for this characterization, but this destructive method is not reasonable in our case due to the limited number of samples (CMOS chips). A suitable method for this purpose is using a probe station, where the microprobes can be placed on the sample to measure conductivity (*Figure 4.7*).

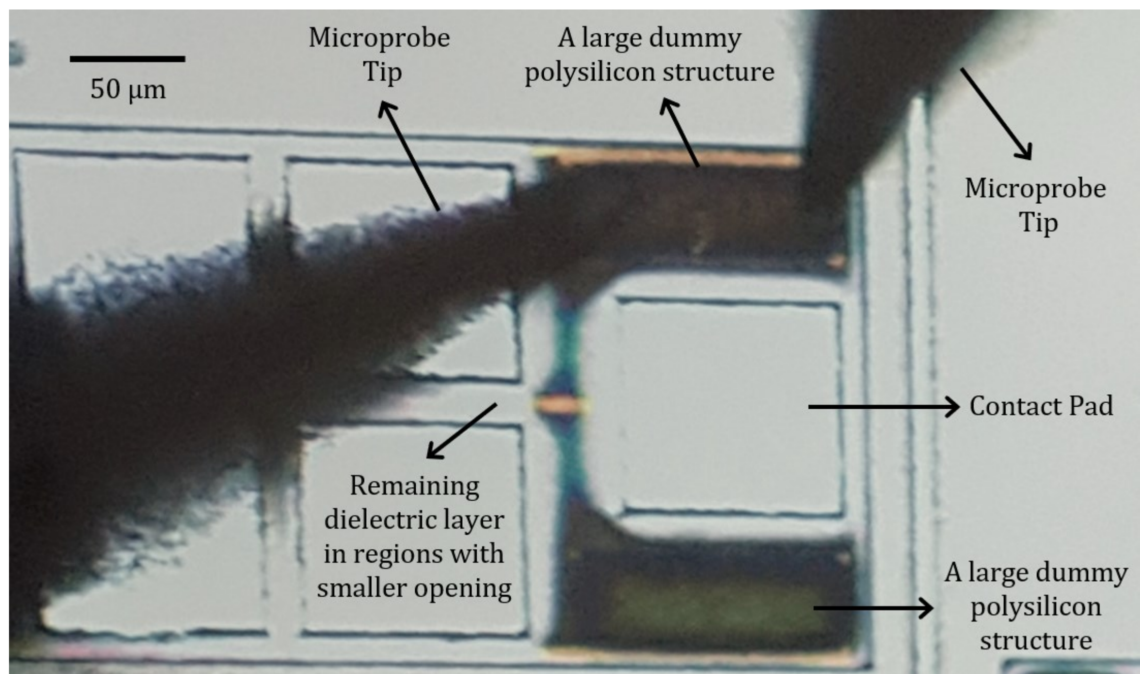
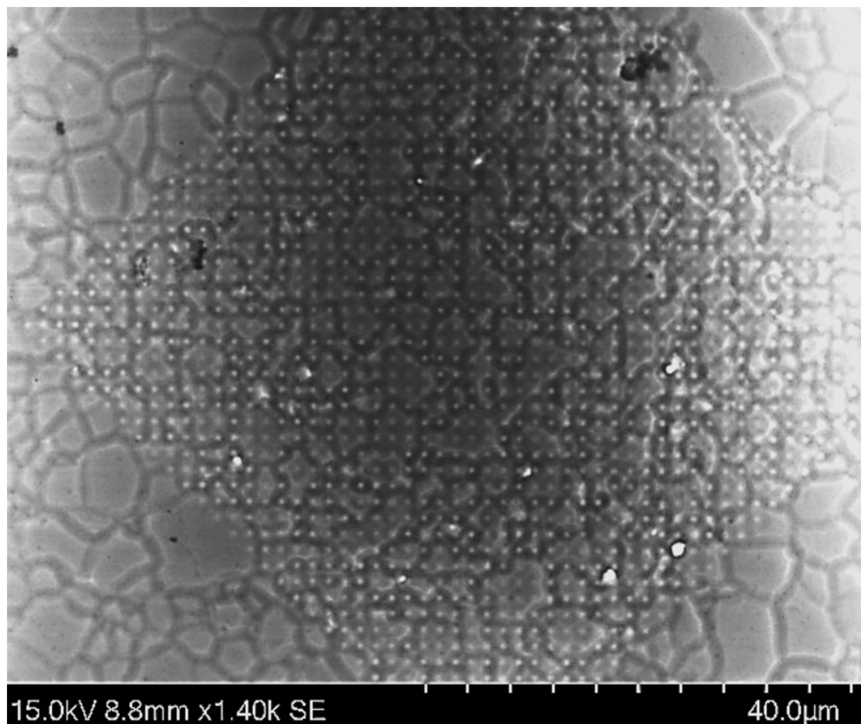


Figure 4.7: Conductivity measurement on an exposed polysilicon structure using microprobes to confirm the removal of dielectric layer.

A conductive surface means SiO_2 is removed, and polysilicon or bulk silicon is exposed in the measured region. This method can only be used in the areas with large opening, similar to the regions with the large dummy polysilicon structure in *Figure 4.7*. The dielectric layer remains in the regions with smaller opening, and such a size of the opening represents the etching window for most of the polysilicon microheaters from the first-generation designs. It signifies that higher aspect ratio is needed during the SiO_2 etching. With equal etching depths for small and large openings (similar to *Figure 4.5a*), confirming conductive surface on a larger region like the dummy polysilicon structure will also ensure exposure of the microheaters.

Initially the chips were etched without enabling the ICP source. After providing some power to the ICP source, a higher aspect ratio is obtained. Although very narrow opening areas still had residues, an opening window wider than 35 µm had adequate etching. Higher ICP power indeed helps in improving the aspect ratio, however, increasing it above 200 W resulted in higher substrate temperature during the ICP-RIE process. As a result, the exposed aluminium surfaces were highly damaged (*Figure 4.8*) due to enhanced physical etching at high temperatures.

(a)



(b)

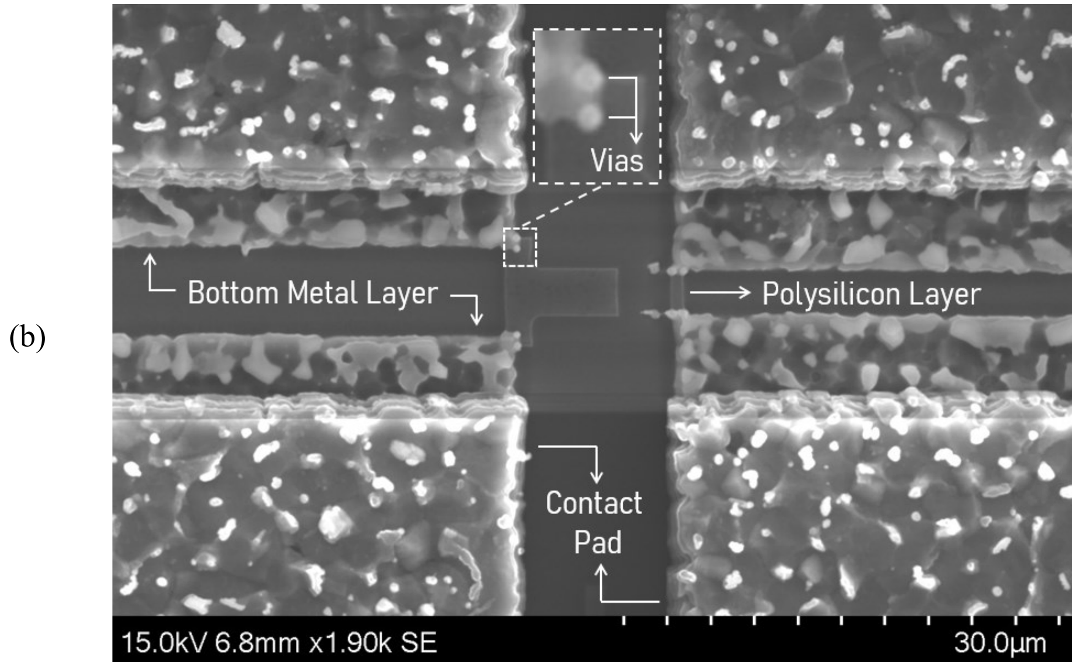


Figure 4.8: Damages on aluminium layers after RIE with high ICP power. (a) Surface of a contact pad and (b) possible disconnections of the extended bottom metal layers and vias that link the polysilicon heaters.

The damaged aluminium contact pads (*Figure 4.8a*) are problematic for wire bonding. In *Figure 4.8b*, it can be seen that the bottom extended metal layer connected to the polysilicon microstructures is also exposed and damaged. Due to the metal damages, the vias in between the bottom metal layer and polysilicon layer can be clearly seen in the magnified inset of *Figure 4.8b*. As a consequence of these damages, the polysilicon heaters were getting disconnected from the bottom metal layer due to the barely connected vias. Therefore, to limit the extensive damages of the exposed aluminium layers while obtaining a high aspect ratio (uniform etching), the power of the ICP source was limited to 200 W during the ICP-RIE process. Settling for the low ICP power is a shortcoming of the RIE system which lacks a thermal management system for the sample placement substrate.

Apart from the post-processing challenges of the initially designed CMOS chips, some design limitations also became apparent during the experiments. An important one among them is the small amount of vias used for connecting the polysilicon heaters with the bottom metal layer. For most of the microheaters, only two vias were used to connect each side of the polysilicon heaters with the metal layer. As a result, the vias

were subjected to high current density during the joule heating process when the required current to attain the high-temperature CNT synthesis condition exceeded the standard CMOS operation limits. During this process, the heaters were getting disconnected at the vias before reaching the CNT growth temperature in majority of the cases. Measuring the microheater temperature during joule heating was another challenge. The width of the microheaters is too small to get reliable thermal measurements as discussed in *section 3.5*. The operating wavelength used in the high-performance IR microscope was 3-5 times larger than the width of the microheaters.

4.5 Improved designs and post-processing

The challenges encountered during the post-processing of the first-generation CMOS chips revealed the necessity of design improvements for the microheaters as well as improving the post-processing approaches. Therefore, a new set of microheaters were designed and fabricated in the same AMS 350 nm CMOS technology; some micrographs of the improved polysilicon designs are in *Figure 3.13c, 3.13d, 3.17, 3.20b*. Layout of this second-generation chip is presented in *Figure 4.9*. Compared to the designs from first-generation polysilicon heaters (*Figure 3.3*), the bottom metal extension is eliminated here to avoid the metal damage and consequent disconnection from the polysilicon layers as experienced during the ICP-RIE at higher powers. The purpose of the metal extension was to keep the microheater length short and maintain a certain distance between the contact pads at the same time. In this new design, the polysilicon layer is extended instead. The gradual shortening of the heater width ensures that the effecting heating region remains in a small area at the centre of the structure (*Figure 4.9*).

Distances between all the contact pads were also expanded in the new designs. It was measured from the previous designs that a uniform SiO_2 etching over the entire CMOS chip can be obtained if the minimum opening window is wider than 35 µm. Therefore, on the improved heater designs, the minimum opening area over the polysilicon microstructures surrounded by the four contact pads is set to 50 µm × 50 µm (*Figure 4.9*). This design improvement resolves all aspect ratio related challenges experienced from the post-processing of the previous CMOS chips.

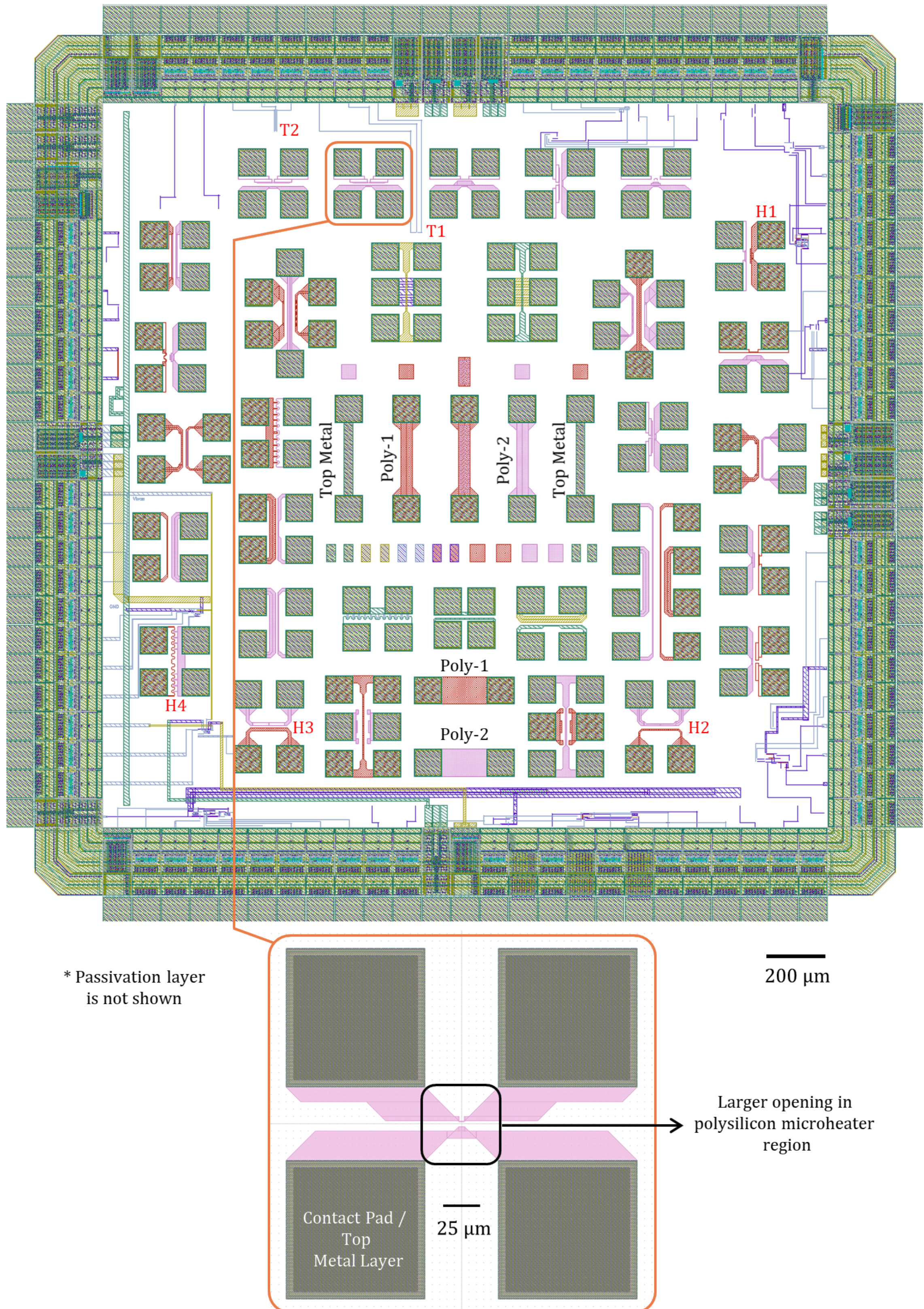


Figure 4.9: Layout design of the second-generation CMOS chip with large opening for the polysilicon microheater region.

Another design improvement was increasing the number of vias connecting the bottom metal layer and polysilicon layer. The cross-sectional illustration of the new design in *Figure 4.10* shows that the via array is extended to the entire contact pads. Here, the polysilicon layer covers the entire surface area underneath the contact pad and a large array of vias over that polysilicon area establishes connection to the metal layer above. This solves the high current density issue during the joule heating caused by the mere number of vias used in the preceding design (*Figure 4.2*). Finally, in the new CMOS chip design, a few large polysilicon heaters (such as *Figure 3.2c, 3.2d*) were placed to make them suitable for a potential IR microscopy during joule heating. The larger microheaters are at least ~30 µm wide, hence, the thermal measurements on these heaters will not be limited by resolution.

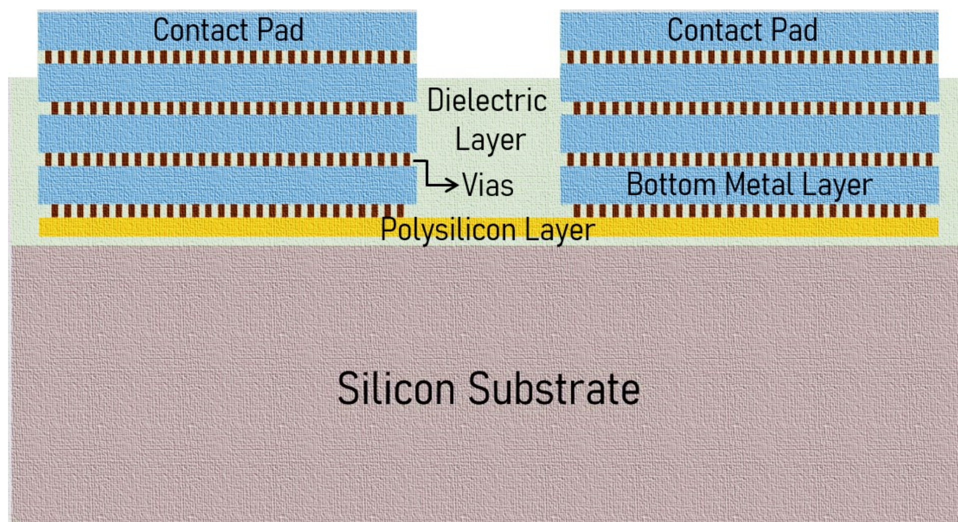


Figure 4.10: Cross-sectional illustration of a polysilicon microheater with associated layers, designed in the latest generation CMOS chips.

The post-processing approach was also improved by developing two SiO_2 etching recipes in a new ICP-RIE system. One recipe (DER-3) involves high ICP power and the other one (DER-4) without any ICP power. DER-3 has faster SiO_2 etching rate and ensures high aspect ratio for uniform etching in both small and large opening regions. As this new ICP-RIE system has excellent thermal control with the option of below 0 ˚C temperature on the sample holding substrate during etching, we overcame the metal damage and surface roughness issues occurred in the previous ICP-RIE system at higher ICP powers.

Figure 4.11 shows the surface of contact pads after SiO_2 etching in the new system with DER-3, which does not show any visible damage on the metal surfaces unlike previous results in *Figure 4.8*.

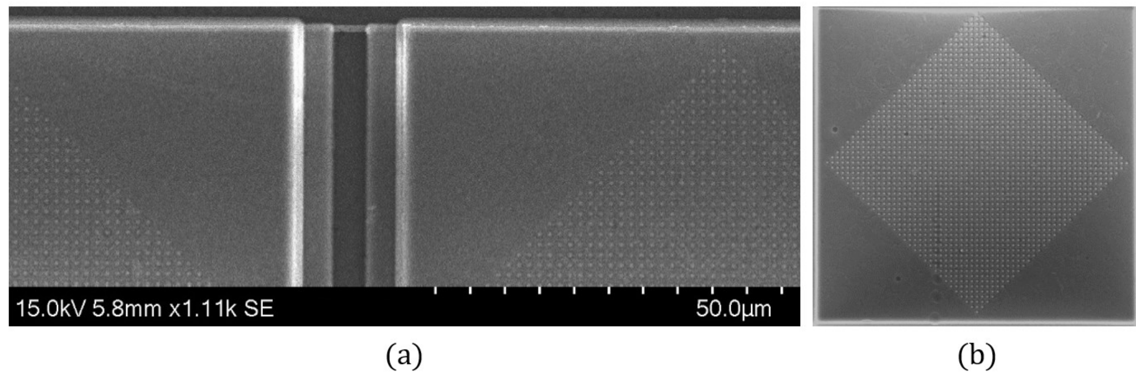
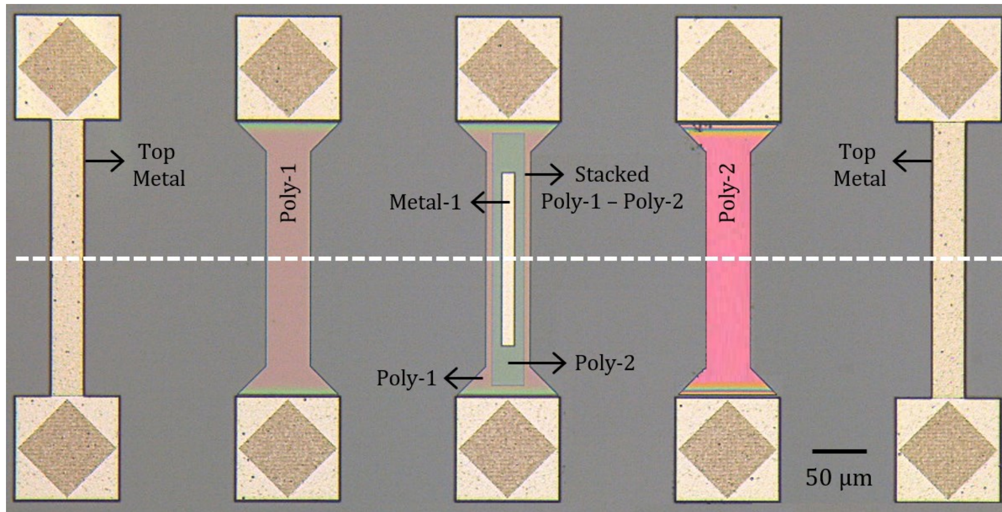
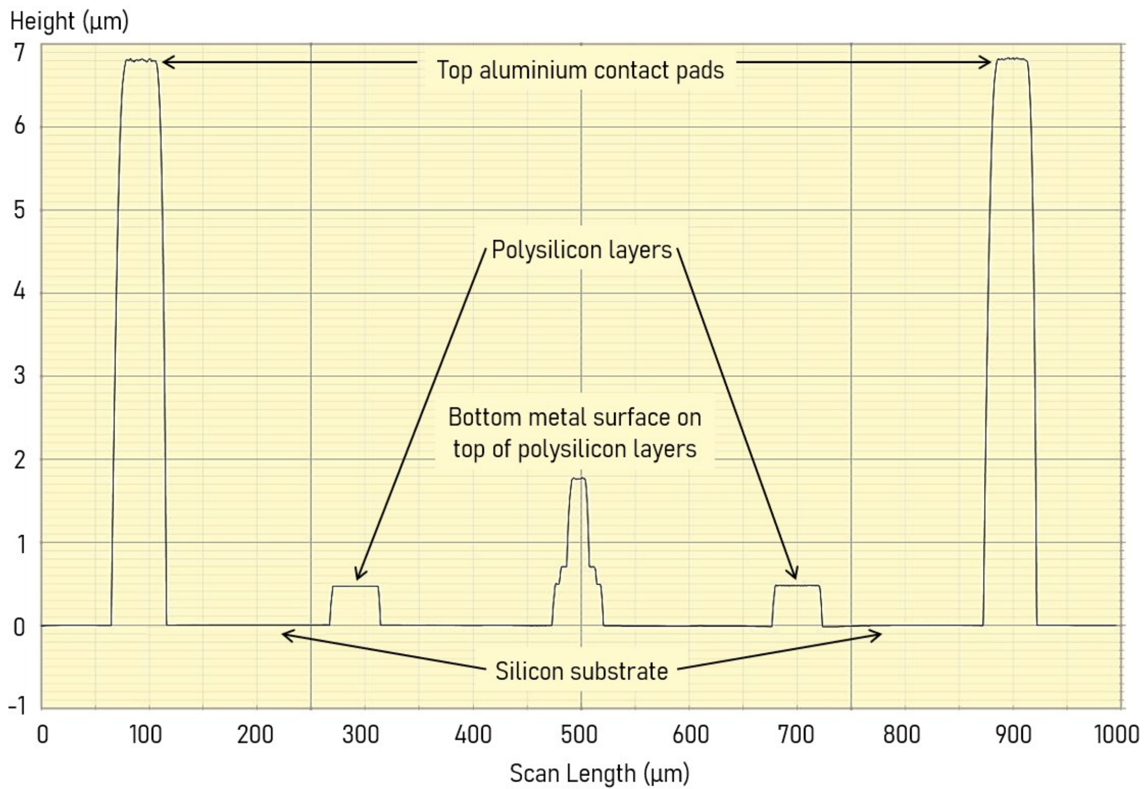


Figure 4.11: Aluminium surface after dry etching with DER-3 in the new ICP-RIE system. (a) Top and bottom metal surface of the first-generation design; (b) Entire contact pad without damage.

The only drawback of the new ICP-RIE recipe, DER-3 has somewhat low selectivity between SiO_2 and polysilicon. Therefore, it cannot be used once the polysilicon layers are exposed, a challenge solved by the other newly developed recipe, DER-4. DER-4 has excellent selectivity and does not etch polysilicon layers while etching surrounding SiO_2. As the ICP source is disabled in DER-4, the etch rate and aspect ratio however is lower than for DER-3. To get the benefits of both recipes without damaging the polysilicon layers, both of them were used for their specific purposes. The SiO_2 etching started with DER-3 and stopped before the polysilicon layer is uncovered, then the remaining exposed SiO_2 is etched by DER-4. DER-3 provided fast etching with high aspect ratio for removing SiO_2, while DER-4 ensured high selectivity for fully and safely exposing the poly layers as shown by the surface profile in *Figure 4.12*. It should be noticed that the thicknesses of the polysilicon layers, as well as the SiO_2 layers are not consistent for the CMOS chips, and the latter can vary by several tens of nanometres. Therefore, it is important to be cautious with the etch duration when using DER-3 due to the selectivity issue. Over-etching with DER-3 can result in thinner polysilicon layers after exposure, making their resistance too high for useful operation. To avoid such situations, a safe margin is considered for stopping the etch with DER-3 and continuing with DER-4.



(a)



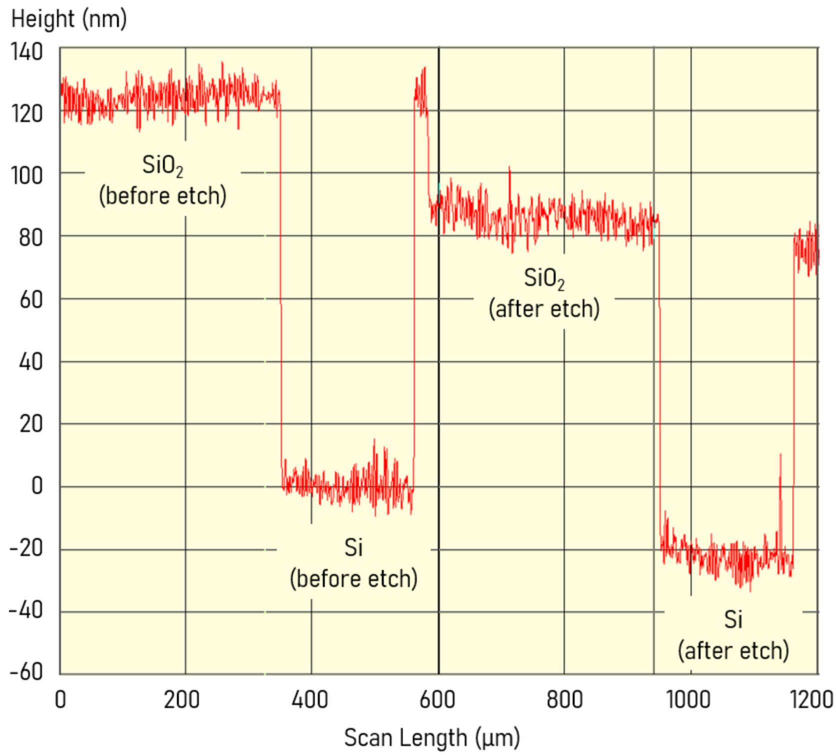
(b)

Figure 4.12: Etch profile after dry etching with DER-3 & DER-4. (a) Optical micrograph of the scanned region with large metal and polysilicon layers; (b) Profilometer measurement scanned across the white dashed line from the previous image.

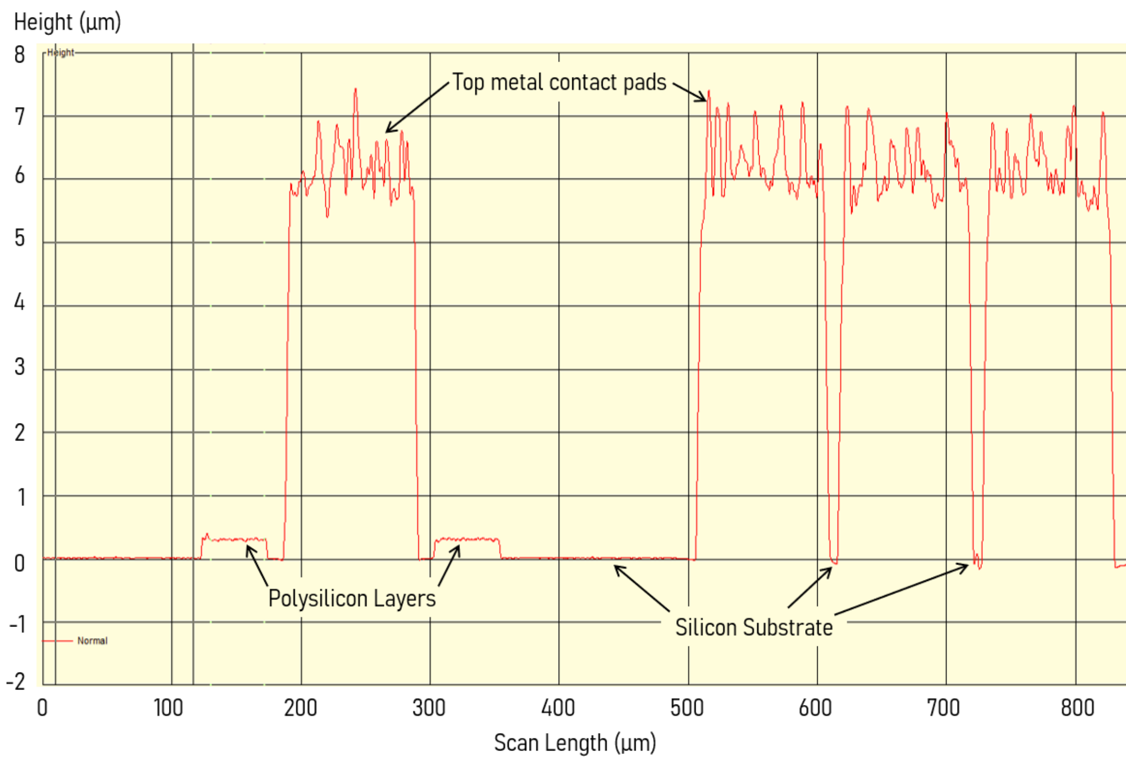
4.6 RIE recipe development

The post-processing starts with dry etching of the dielectric layer. For the initially designed CMOS chips, the DER-1 and DER-2 etching recipes were used for SiO_2 etching. DER-1 was performed using a DRIE system (Plasmalab System 100, Oxford Instruments, UK). In DER-1, sulphur hexafluoride (SF_6) was used for the SiO_2 etching in a Bosch process. In this process, duration of each etching cycle was 1 minute followed by 2 minutes of cooling cycle using 50 sccm Ar at 30 mTorr chamber pressure. Depending on the desired etching thickness, the number of cycles of this loop was decided. The recipe ends with a final 10-minutes long cooling cycle using 50 sccm O_2. It was a pre-configured recipe in the DRIE system for etching SiO_2. The recipe provided high aspect ratio with uniform etching even at small opening regions (*Figure 4.5a*), but the selectivity between Si and SiO_2 was poor.

DER-2 was performed in an ICP-RIE system (Mini-lock Phantom III, Trion Technology, USA). In this system, CHF_3 and CF_4 were used for the etching instead of SF_6-based chemistry. The ICP source was enabled with 200 W power and added in a SiO_2 RIE recipe [263] together with an introduction of 50 sccm Ar cooling cycle to form DER-2. Each etching cycle was 10 minutes long followed by 5 minutes of cooling. Similar to DER-1, O_2 was initially included in DER-2 to increase the etch rate [264], however, it was later removed as introducing O_2 also increases silicon etching thus reduces selectivity. Numerous experiments were carried out on SiO_2 patterned silicon pieces to improve the selectivity between Si and SiO_2. With high ICP power, DER-2 provided a selectivity ratio of ~ 1:2, etching the SiO_2 layer at a double rate than the silicon layer (*Figure 4.13a*). Another recipe with 45 sccm CHF_3 and 15 sccm 0_2 was also attempted, which has better selectivity, but the etch rate is very low (~1-3 nm /min) for practical use in removing thick SiO_2 layer. In addition, the O_2 gas flow control was not adjustable in the ICP-RIE system, hence the gas ratio between CHF_3 and 0_2 was not properly measured. The polysilicon layers of the first-generation CMOS chips were exposed using DER-2, as shown in *Figure 4.13b*; the scan was performed across the white dashed line in *Figure 4.6*. ICP power of 500 W was used in this case, resulting in rough metal surface as also observed in *Figure 4.8*.



(a)



(b)

Figure 4.13: Etching profile after ICP-RIE using DER-2. (a) Selectivity test on a SiO_2 patterned Si sample; (b) Polysilicon layer exposure on first-generation CMOS chip.

For the succeeding CMOS chips with improved designs, all dry etchings were performed in another ICP-RIE system (PlasmaPro 100 Estrelas, Oxford Instruments). The developed recipes for this system, DER-3 & DER-4, use CHF_3 as the primary reactive gas; it provides better selectivity between Si and SiO_2 than CF_4 based etching [265]. In these recipes, the RF power is balanced by keeping etch rate, selectivity, and etched surface profile into consideration. Higher RF power contributes in raising ion energy of the gases, which increases the etch rate but can cause damages on the etched surface due to induced physical etching [266] and reduced selectivity. Higher ICP power corresponds to higher etch rate due to the increase in ion density of the plasma [267] and improve etching with high aspect ratio [268]. In ICP-RIE, high aspect ratio and etch rate is achieved without significant surface damages due to decoupled plasma density and energy [266]; reduced RF and high ICP power was used in DER-3 to ensure that. As uniform etching was achieved with high aspect ratio at 800 W, the ICP power was not increased further. Moreover, too high ICP power, hence too high plasma density can decrease etch rate due to reduced mean free path causing higher ion collisions in the plasma [267].

Duration of each etching cycle in DER-3 is 5 minutes, followed by 38 sccm Ar cooling cycle for 2 minutes. The loop was repeated 8 times for 40 minutes etching. As DER-3 has less selectivity, further etching was continued with DER-4. The ICP source is disabled in DER-4, while higher RF power is used. Without the ICP power, ion density of plasma reduces and results in lower etch rate and higher selectivity. Although DER-4 produces significantly lower etch rate, it has the best selectivity among the four recipes. Ar flow rate is increased in this recipe to somewhat improve the etch rate. In this ICP-RIE system, the substrate temperature of 0 ˚C and 20 ˚C was used; the etching results in both temperatures were similar beside minor deviation in etch rates. Low chamber pressures used in the recipes ensure less ion collisions and high directionality. Etching and cooling duration of each cycle in DER-4 is the same as for DER-3. Total required etch period using DER-4 varied from chip to chip as thickness of the dielectric and polysilicon layers in the CMOS chips differ by tens of nanometres. In most cases, 20-25 minutes of etching with DER-4 was enough for removing the oxide layers to reveal the polysilicon layers and silicon substrate. All used SiO_2 dry etching recipes are summarized in *Table 4.1*.

Table 4.1: Summary of the SiO_2 dry etching recipes.

Dry Etching Recipe	Gases with Flow Rates (sccm)	RF & ICP Power (W)	Pressure (mTorr)	Etch Rate (nm/min)
DER-1	H_2: 15, SF_6: 50, O_2: 5	RF: 50, ICP: 1500	30	~ 100
DER-2	Ar: 30, CHF_3: 30, CF_4: 30	RF: 500, ICP: 200	100	~ 90
DER-3	Ar: 38, CHF_3: 12	RF: 80, ICP: 800	10	~ 105
DER-4	Ar: 95, CHF_3: 15	RF: 300, ICP: 0	20	~ 30

Polysilicon microheaters from first- and second-generation CMOS chips after dielectric etching with DER-3 and DER-4 are shown in *Figure 4.14*; both chips were etched together for the same duration. The multi-coloured patterns on the polysilicon microstructures in *Figure 4.14a* indicate that some dielectric layer remained in the first-generation heater, which can be due to relatively shorter opening between the top and bottom contact pads. However, since DER-4 has excellent selectivity (not quantified due to very low Si etching), longer etching can fully expose the polysilicon layers. The second-generation heater with larger opening is fully exposed (*Figure 4.14b*). The dry etching with DER-3 has mostly been anisotropic (*Figure 3.12b*), but some amount of polysilicon under-etching can be obtained (*Figure 3.9c*) with DER-4 when etched for longer duration.

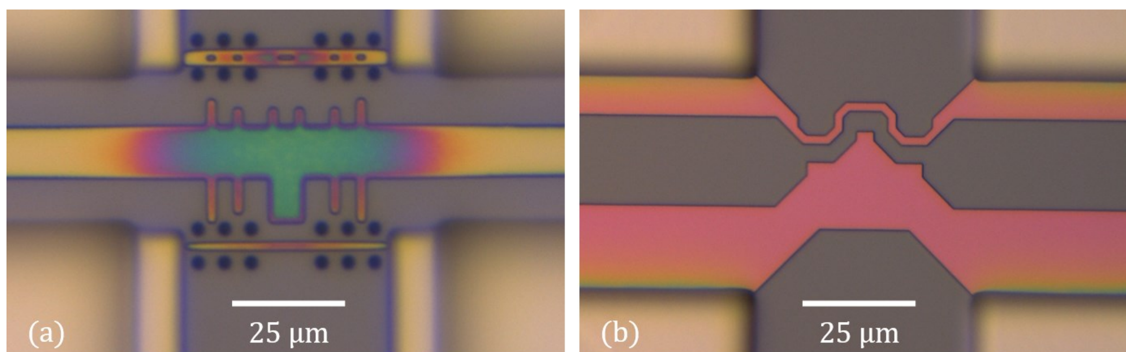


Figure 4.14: Optical micrographs of polysilicon microheaters in (a) first-generation and (b) second-generation CMOS chips after dielectric etching with DER-3 & DER-4.

EDX analysis was also performed around a metal microheater (*Figure 4.15*) after etching with DER-3 to confirm the anisotropy. The mass percent of the elements are summarized from the EDX spectrum in *Table 4.2*. Traces of SiO_2 are evident underneath the top metal layer, while the surrounding regions are mostly Si substrate.

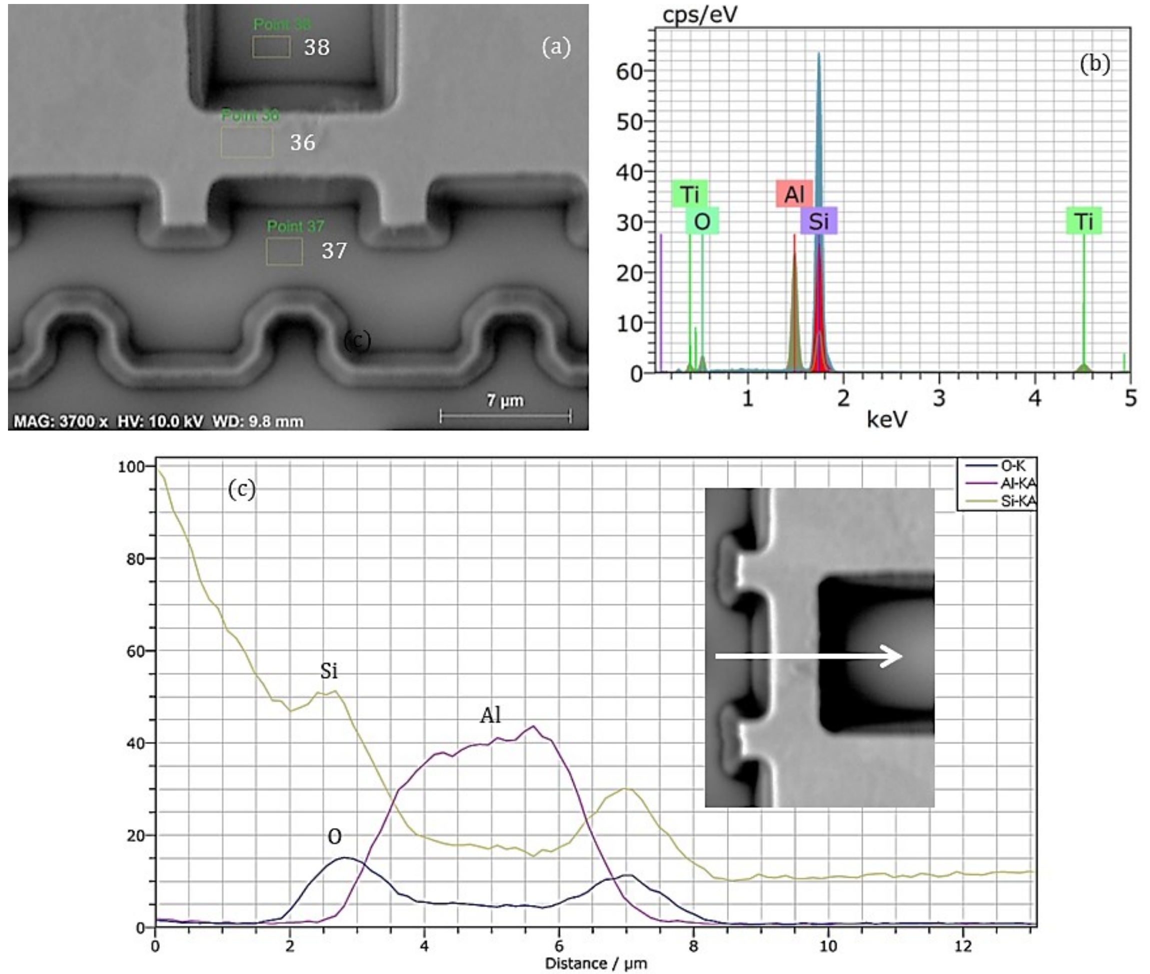


Figure 4.15: EDX analysis around a metal microheater after etching with DER-3. (a) Electron micrograph with scanned regions; (b) EDX spectrum (elemental mapping); (c) Line scan across the heater width.

Table 4.2: Atomic percent (%) on the scanned regions of the EDX analysis**.**

Spectrum	O	Al	Si	Ti
Point 36	12.47	37.28	22.63	27.62
Point 37	1.86	-	98.14	-
Point 38	2.84	-	97.16	-

4.7 Microheater suspension

The post-processing step of releasing microheaters is not essential for all heaters to achieve the CMOS-compatible ambient temperature. The primary motivation for microheater suspension is to thermally isolate the heaters when CNT synthesis temperatures are generated. Suspended heaters also require lower power consumption for generating the high temperatures. However, heater suspension introduces an additional risky process step of wet etching, which can result in mechanical deformation of the heaters due to stiction. Due to very thin dielectric layer (~ 250-300 nm) beneath the polysilicon layers, the capillary force in equation *(6)* becomes high, which indicates higher probability of stiction. Surface area of the microheaters also plays a significant role here; lower surface area reduces the possibility of stiction. Based on the trade-off between high thermal gradient and mechanical stability of the heaters, amount of heater suspension / under-etching can be considered.

For isotropic SiO_2 etching, a typical BOE recipe [269] was initially attempted before moving towards a more aluminium friendly etchant. For partial suspension of the polysilicon microheaters (*Figure 4.4c*), SiO_2 wet etching recipes were investigated that, unlike the BOE, do not etch aluminium. The most suitable etchant found for this task was Pad-etch [269,270], which is formulated for a similar purpose of protecting aluminium pads while etching dielectric layers as reflected by its name. Even though this etchant still mildly attacks aluminium, the damage is far less than BOE. It is important to fully expose the silicon substrate (*Figure 4.4b*) before proceeding to wet etching for reducing duration of exposure to the etchant. Optical microscopy can visually provide signs of remaining SiO_2 layer (*Figure 4.16*). In *Figure 4.16a*, Si substrate in the right diagonal half of the chip is exposed, whereas the other half has SiO_2 layer. From bluish towards golden colour indicates thinner to thicker SiO_2 layer. Chip in *Figure 4.16b* only has SiO_2 on top surface; both chips from *Figure 4.16a* & *4.16b* were dry etched together. Microheaters from regions with thin dielectric layer are shown in *Figure 4.16c* & *4.16d*; tan layer on the polysilicon indicates the thin SiO_2 layer. *Figure 4.16e* shows a heater from the bluish chip region with thicker SiO_2 layer, and *Figure 4.16f* presents a heater from the chip region with exposed silicon substrate.

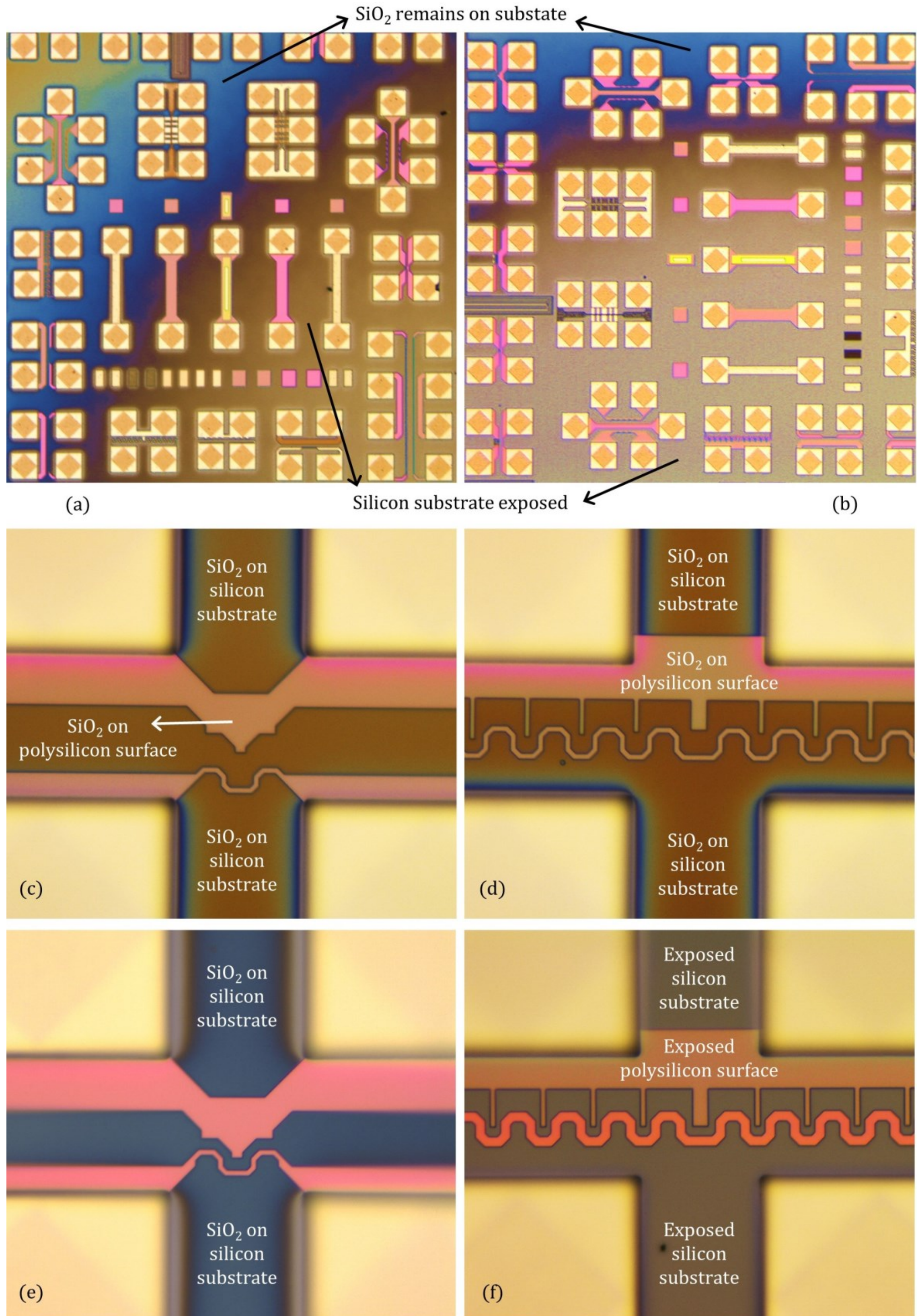


Figure 4.16: Optical micrographs after dry etching. (a), (b) Partially exposed Si substrate; (c), (d) Thin SiO_2 remained on polysilicon heaters; Heaters from (e) thicker SiO_2 region and (f) exposed Si substrate region.

Optical micrograph of a CMOS chip with fully exposed silicon substrate is shown in *Figure 4.17*. A probe station was used to confirm whether all exposed SiO_2 was etched by measuring electrical conductivity of the chip surface. A properly etched chip surface shows finite resistance, while even a thin remaining SiO_2 layer results in non-conducting surface in this measurement. Probe tips with ~20-25 µm diameter were used in this task. Microprobes with thinner tips (1 µm & 3.5 µm) were also tried to examine the smaller polysilicon structures, but those soft tips did not provide good contacts for proper measurement. The probe station was also handy for testing the resistance of some polysilicon heaters before wire bonding the sample in a chip carrier. Significantly higher heater resistance is found if the polysilicon layer is etched during the ICP-RIE process.

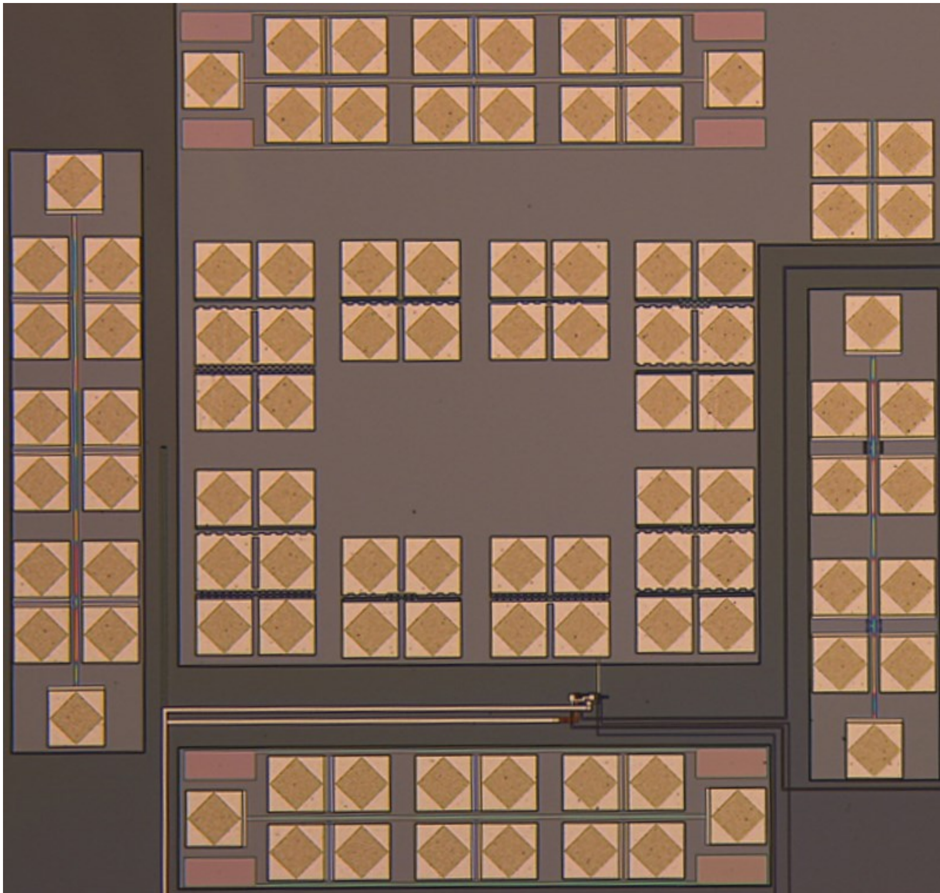


Figure 4.17: Part of a CMOS chip with fully exposed silicon substrate after dry etching.

For the isotropic etching of SiO_2, a variant of the 'Pad-etch' recipe was used. Pad-etch is an ammonium fluoride (NH_4F) based oxide etchant conventionally used to save aluminium pads, even though it still slowly etches aluminium and can make the metal

surface rough especially when the sample is exposed longer in the etching solvent. The aluminium surface is mostly attacked in the first few minutes before being passivated [270] by aluminium acetate salt [271] formed from the acetic acid (CH_3COOH) in the etchant that protects aluminium from further significant etching. The etchant solution is completed with propylene or ethylene glycol and water. Surfactants are also often used to lower surface tension and increase wetting [272] in the Pad-etch solution. In our version of the recipe, ethylene glycol was used without any surfactant. Duration of this wet etching depends on the required amount of partial microheater under-etching. From our experiments, around 30 minutes of etching with Pad-etch resulted in near 400 nm SiO_2 removal from underneath each side of the exposed polysilicon structures. The used SiO_2 wet etching recipes are summarized in *Table 4.3*.

Table 4.3: Summary of the SiO_2 wet etching recipes.

Etchant	NH_4F	Acetic Acid	Ethylene Glycol	Water	HF
Pad-etch	13.5%	31.8%	4.2%	50.5%	-
BOE	7 parts	-	-	-	1 part

It is important to note that etching with this etchant should be done in one step to avoid further damaging the aluminium surface. Cleaning the sample after taking it out from the etchant removes the passivation layer over the aluminium surface, hence, putting the sample back to the etchant for additional SiO_2 etching causes more harm to the unprotected metal; the chip in *Figure 4.18a* has been etched in this way. It has been etched for 30 minutes and cleaned before putting the chip back to the etchant for further 15 minutes of etching. As a result, the top aluminium layer has been etched in this chip. The aluminium layer (metal-3) beneath the top metal can be visible in all contact pads. It is possible to etch the newly exposed SiO_2 layer (which was beneath the top metal layer) over the metal-3 layer and use this layer as the contact pad for wire bonding. This can be done with an additional dry etching step if further wet etching is not desirable. *Figure 4.18a* also shows that a few 60 µm × 30 µm blocks of metal-3 and

metal-2 dummy structures were lifted off due to removal of the underneath SiO_2. However, the metal-1 blocks of same dimensions still remained. It is due to the dielectric thickness beneath the metal layers. Being the bottom aluminium layer, metal-1 has the least SiO_2 thickness underneath it, among all the metal layers; hence, the dielectric layer encounters less vertical exposure to the etchant. Result of the 30 minutes continuous etching with Pad-etch is shown is *Figure 4.18b*. The top metal was not etched in this case, none of the metal blocks were also lifted off.

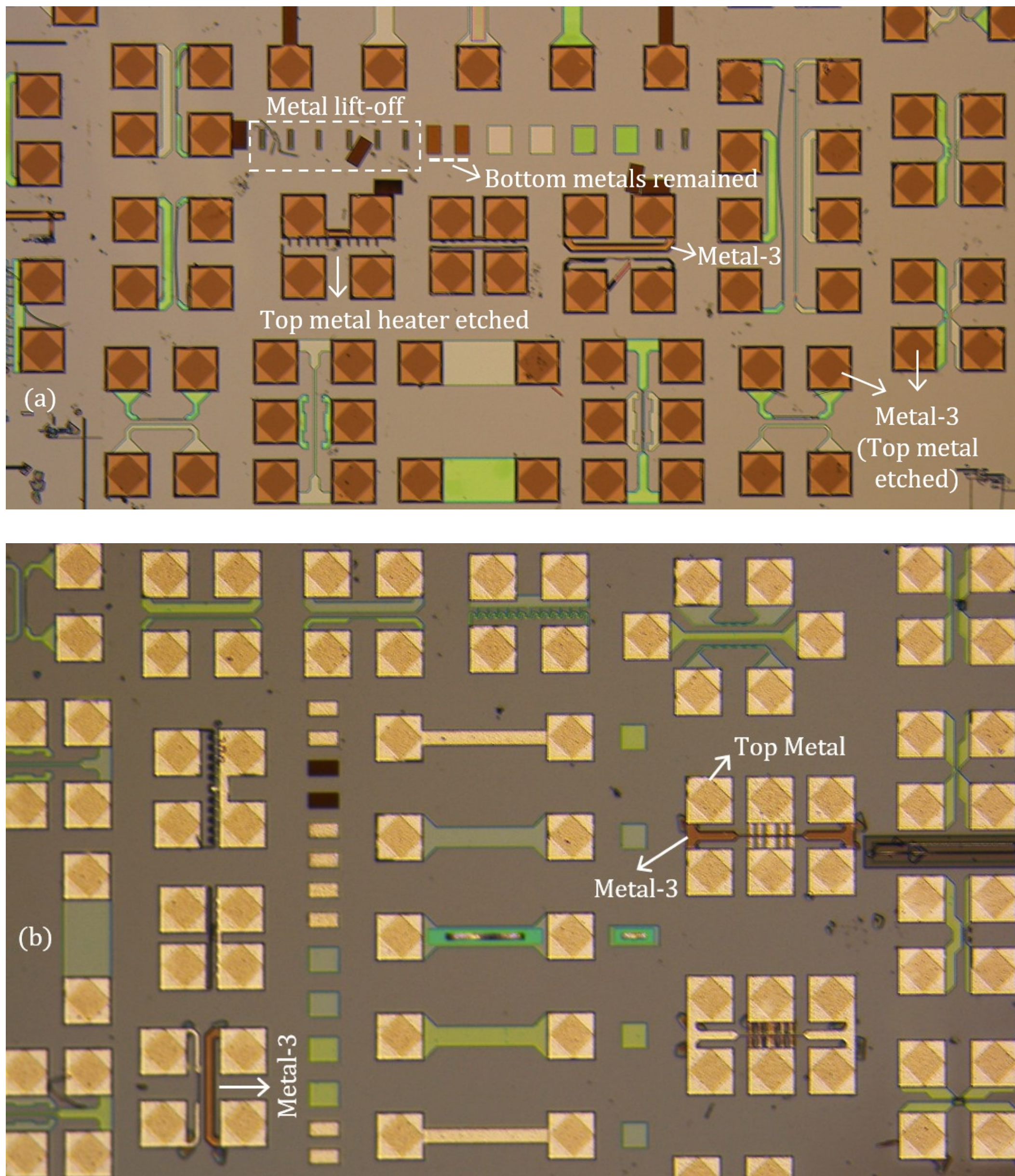


Figure 4.18: Optical micrographs of CMOS chips after wet etching with ‘Pad-etch’. (a) Wet etching in two steps (30 + 15 minutes) with an intermediate cleaning session; (b) Wet etching in one step (30 minutes).

Damages on the exposed aluminium layers due to the longer two-step wet etching is shown in *Figure 4.19*. It is also difficult to bond wires on the contact pads of the wet etched chips. It is particularly more challenging on the chips etched for longer duration since the wire bonding needs to be done on the metal-3, which is covered with a thin TiN adhesion layer. Wire bonding on this surface required higher bonding force, however, the contact pads can be broken if the force is too high (*Figure 4.19b & 4.19c*).

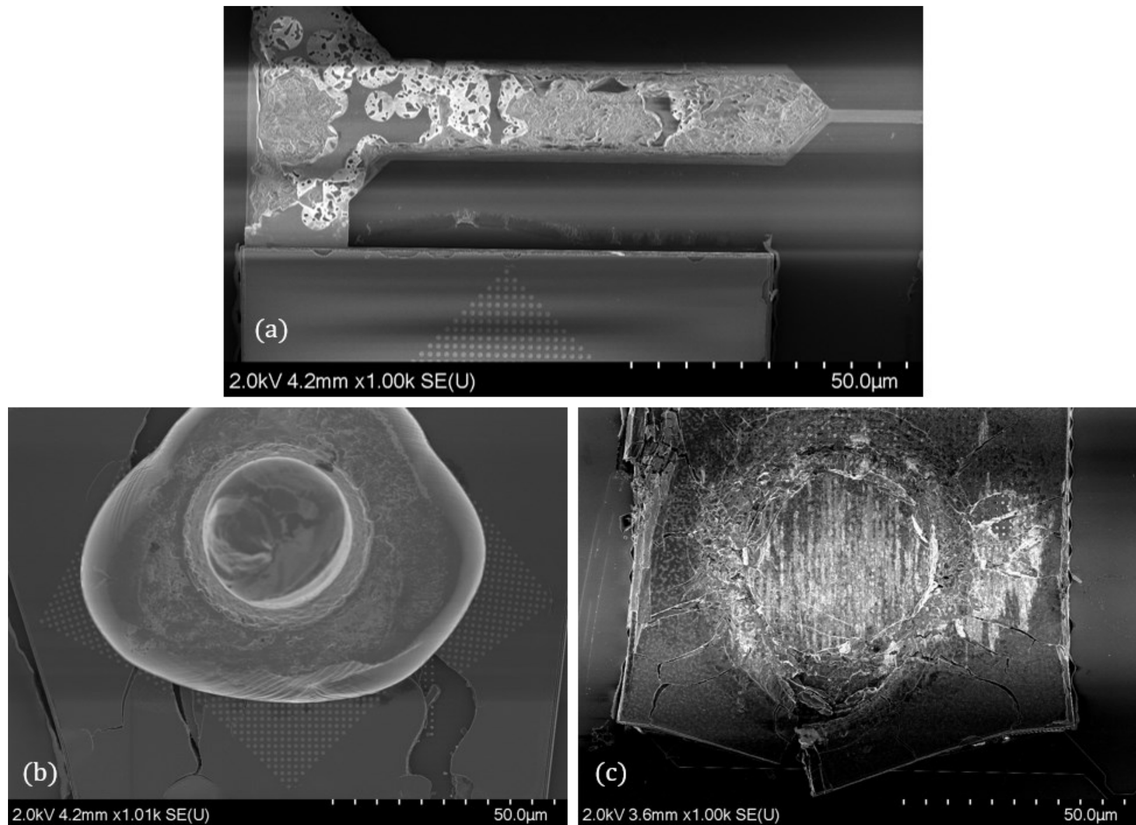


Figure 4.19: SEM images of damages on exposed aluminium layers due to the two-step 45 minutes wet etching. (a) Etched aluminium microheater; (b) Ball bonding with high bonding force needed on Metal-3, and (c) broken contact pad.

The optical micrographs in *Figure 4.20* provide an indication of the under-etching on polysilicon due to wet etching for longer (*Figure 4.20a & 4.20b*) and shorter (*Figure 4.20c & 4.20d*) durations. The suspended regions of the polysilicon may bend downwards, which can cause a height difference with the non-suspended regions, resulting in visually distinguishable regions in the optical microscope. The dielectric thickness beneath the polysilicon layers is even less than the bottom metal layer, thus the under-etching

amount on the polysilicon structures is lower than the metal structures. The metal blocks near poly-2 microheater (as seen in *Figure 3.9b & 3.9c*) are lifted off, and the underneath SiO_2 completely etched in *Figure 4.20b*. Among the polysilicon layers, poly-1 is thicker and has thinner dielectric layer underneath than the poly-2 layer; hence, the under-etching on poly-1 can also be less. Unlike the poly-2 layer, suspended regions of the poly-1 layer is not visually noticeable.

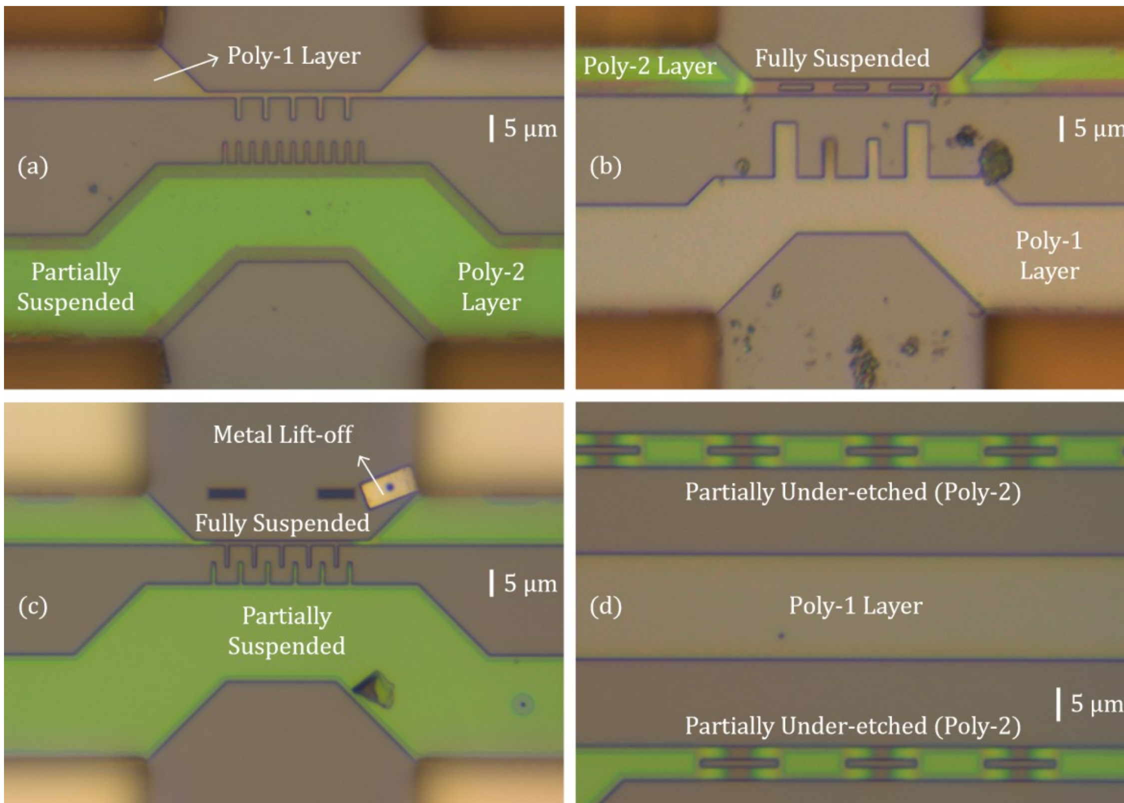


Figure 4.20: Optical micrographs of suspended polysilicon microstructures with time controlled etch-stop. After two-step long-duration wet etching: (a) partially suspended poly-2 microheater, (b) fully suspended microheater with etching holes; After single-step short-duration wet etching: (c) fully and partially suspended poly-2 microheaters, (d) partially suspended poly-2 microheaters with etching holes.

SEM images taken under 45˚ angle clearly show the suspended metal microheaters (*Figure 4.21*). *Figure 4.21a & 4.21b* show successfully released metal heaters, while, stiction also occurred in some of them (*Figure 4.21c & 4.21d*). Suspension of polysilicon heaters are difficult to capture, but the contrast of the suspended regions is visible (*Figure 4.22*). A high contrast image can highlight the under-etched / suspended regions of the polysilicon layers as shown in *Figure 4.22c*, even for poly-1 microheaters.

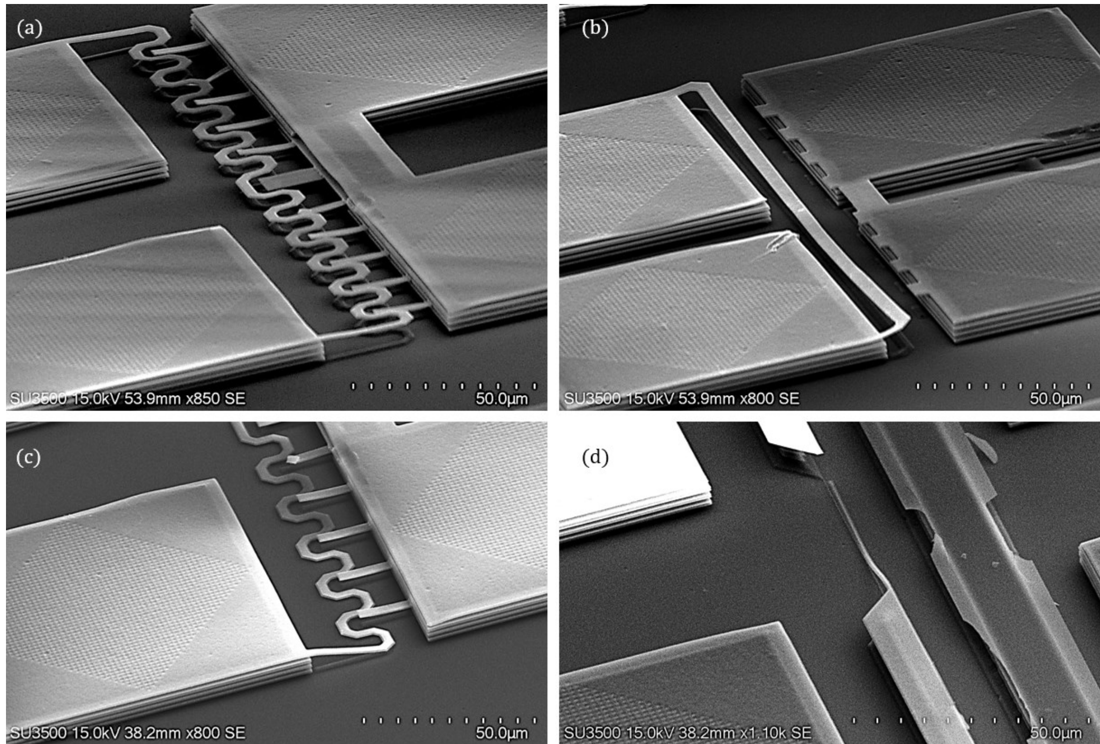


Figure 4.21: Fully suspended metal microheaters. Successfully released: (a) wave-shaped heater, (b) long bridge-shaped heater; Collapse due to stiction: (c) wave-shaped heater, (d) heater with narrow region.

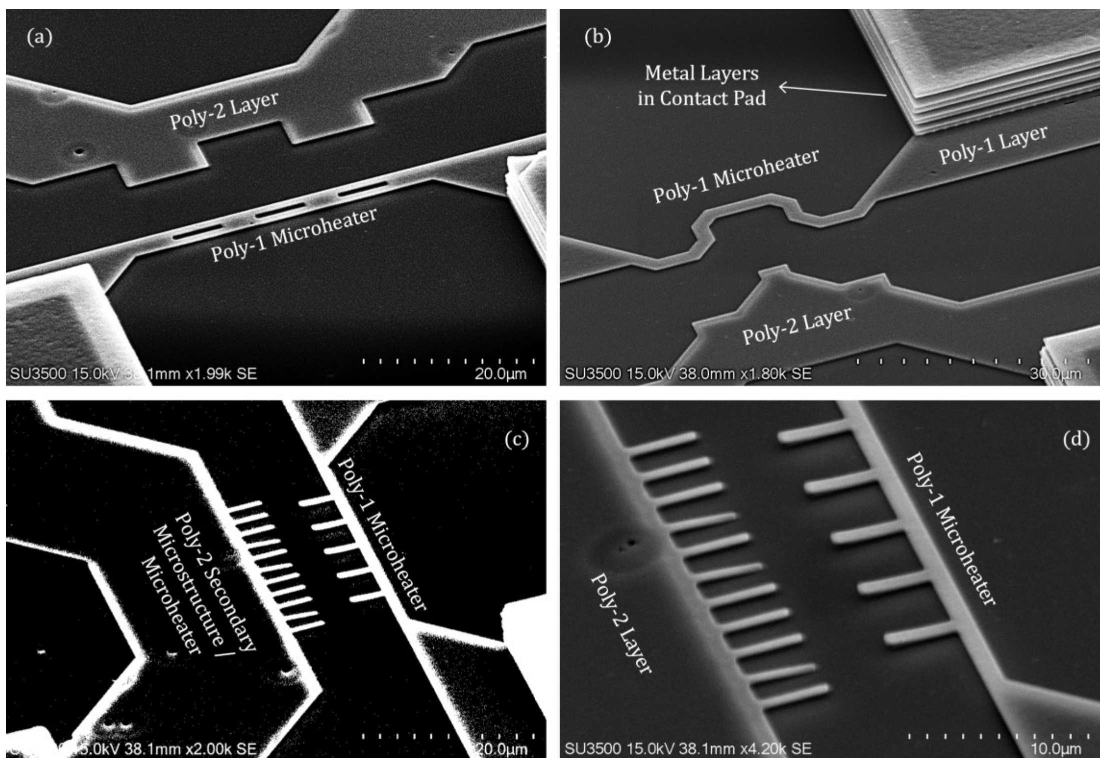


Figure 4.22: Tilted SEM images of suspended polysilicon heaters. (a) Poly-1 suspended near etching holes; (b) Contrast in metal, poly-1 and poly-2 suspension; (c) High contrast image; (d) Close-up at low contrast.

The usage of critical point drying can be beneficial for reducing or eliminating surface tension to overcome stiction [273]. This technique was not attempted during the post-processing of the CMOS chips as the number of the heaters with stiction problem was limited. Vapour HF etching is another alternative to the wet etching process for stiction-free suspension of the heaters [274].

The suspended microheaters were tested. Buckling was observed in some cases; a fully suspended buckled heater is shown in *Figure 4.23*. This is expected based on the critical buckling length from equation *(12)*. In the region with maximum deformation, the heater is shifted by ~1.3 μm (*Figure 4.23c*) from its original position. Performance of the suspended heaters are compared with the non-suspended ones in *section 5.5 & 7.3*.

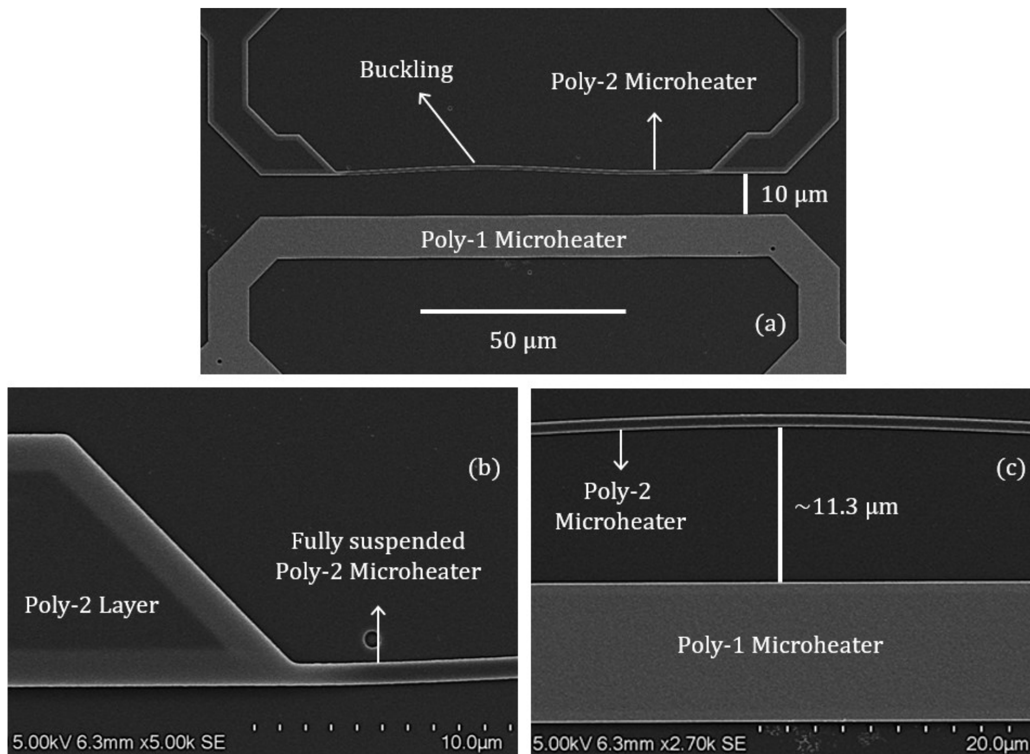


Figure 4.23: Effect of polysilicon microheater buckling. (a) Poly-2 heater buckling inwards; (b) Suspended poly-2 layer; (c) Maximum deformed region of the poly-2 heater.

An under-etching comparison between poly-1, poly-2 and the top metal layer after using 30-minutes long wet etching by pad-etch can be seen in *Figure 4.24a*. A break in the poly-1 microheater occurred after a high temperature operation, which provides a view on the underneath SiO_2 layer as presented in the inset of *Figure 4.24a*. A ~3.72 μm SiO_2

layer can be found under this 5 µm wide heater due to ~640 nm SiO_2 etch on each side of the heater. In the contrast-based under-etching measurements from the SEM image, this value was estimated to be ~800 nm. Therefore, the actual under-etched amount in the microheaters can be 20% less than the value estimated from the contrasts. Using the same method, the suspended width on each side of the poly-2 microheater is roughly ~1.58 µm, which is double than the value approximated for poly-1 heater. It indicates that the poly-2 layer with its thicker underneath SiO_2 layer is under-etched twice as fast as poly-1 layer. The contrast visible on the top metal is ~4.2 µm wide, that is ~2.65 times higher than the poly-2 layer. In case of only RIE (without any wet etching), the underneath SiO_2 in the broken region of an identical poly-1 microheater has no reduction, which indicates complete anisotropic etching by the RIE recipe, DER-4.

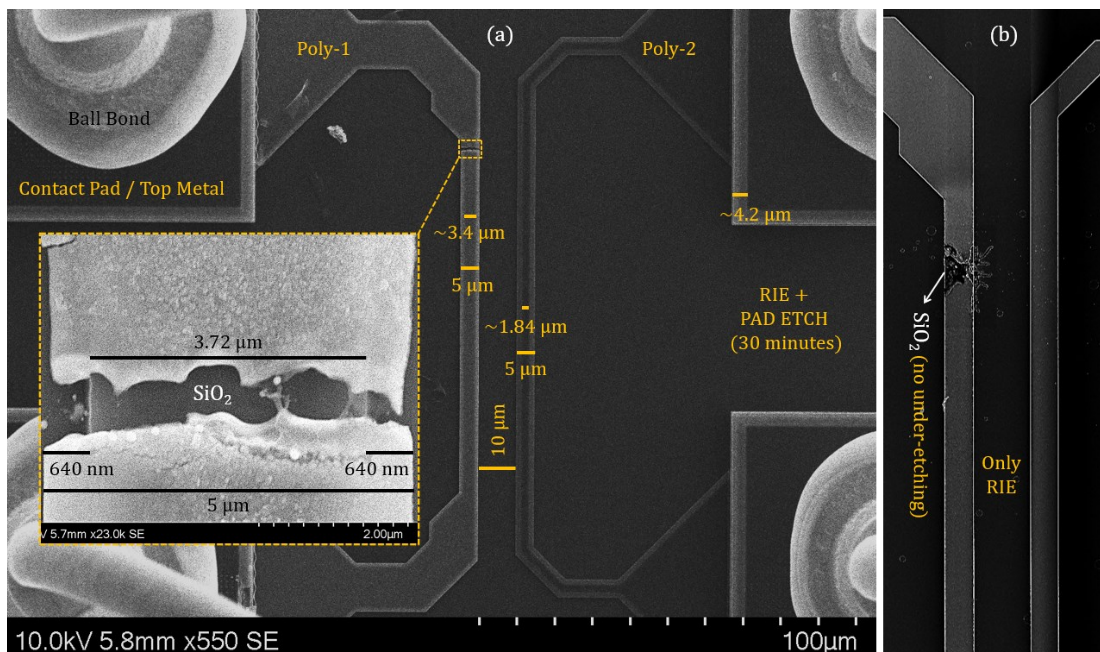


Figure 4.24: Under-etching comparison between different layers and etching approaches. (a) Under-etching in poly-1, poly-2 and top metal after RIE and wet etching; (b) No under-etching after only RIE.

4.8 Nickel electroplating on metal heaters

Electroplating attempts were made on some aluminium microheaters. It is challenging to electroplate on such microstructures, hence, relatively larger heaters were chosen for the experiment. The heaters were wire bonded on a chip carrier before submerging it to the electrolyte solution. Electrical connections from the chip carrier were carefully

routed to the power supply. EDX analysis on an electroplated aluminium microheater shows some Ni deposition (*Figure 4.25*).

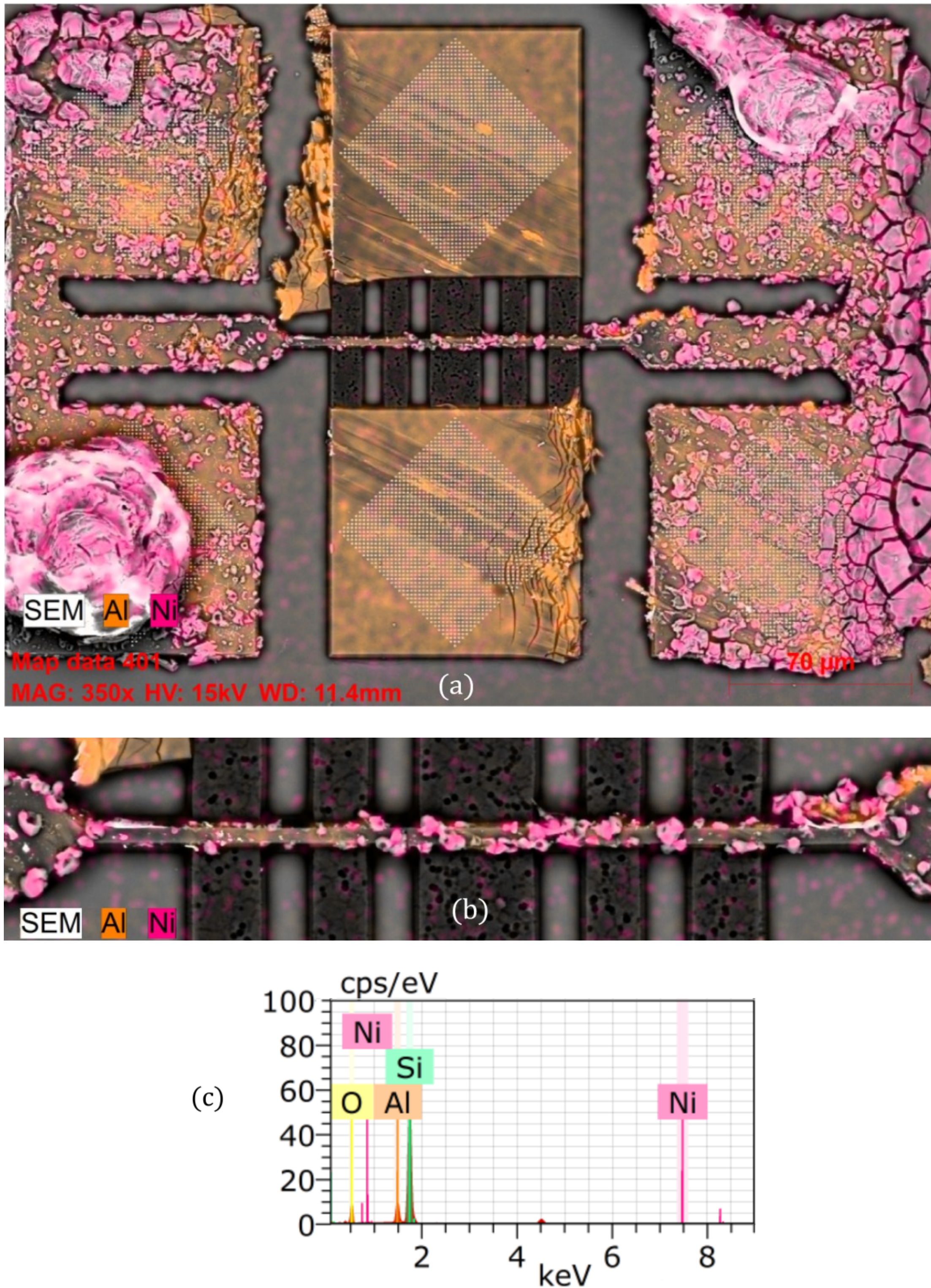


Figure 4.25: EDX analysis of a Ni electroplated Al microheater. (a) Traces of Al and Ni on the heater; (b) Narrow heater region in the middle with inconsistent Ni traces; (c) EDX spectrum (elemental mapping).

Figure 4.25a & 4.25b show non-uniform clusters of Ni deposited on the Al layer. More Ni deposited on the contact pads than the effective heater region. The results indicate that a well-developed electroplating process is required for uniform Ni deposition. In addition, Ni was also depositing on the bonded wire (*Figure 4.25a*), which made the bonding joints stiffer. Hence, they were easily broken during the cleaning process. Rewire bonding is also difficult due to the damages left on the contact pads (*Figure 4.26*). Due to time constraints and sample limitations, the electroplating process was not further developed.

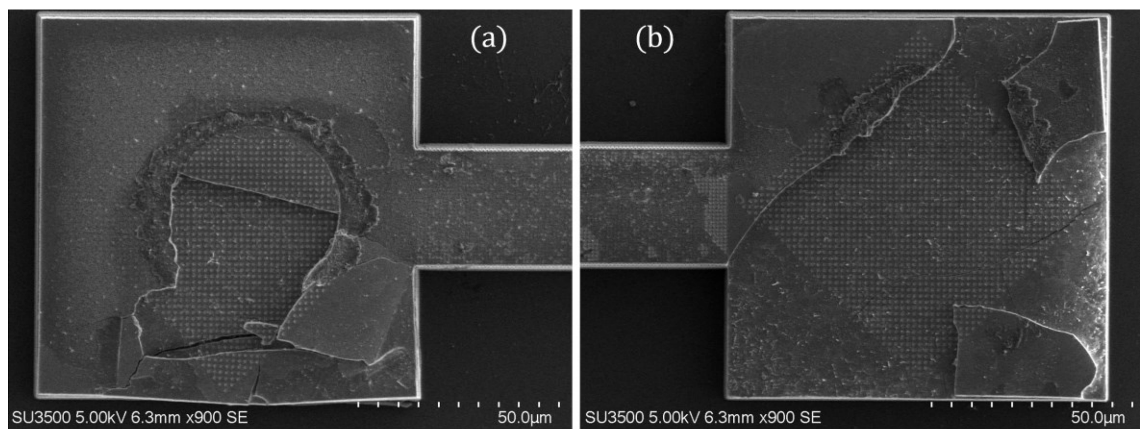


Figure 4.26: Contact pad damages after breaking of stiffer bonding joints. (a) Cracked surface; (b) Broken top metal surface.

4.9 Conclusion

The subtractive post-CMOS SoC integration technique was selected as the cost-effective and suitable method of fabricating the CMOS-MEMS microstructures for local CNT synthesis. Proper CMOS chip design and post-processing approaches held the key of successfully realizing the CMOS-MEMS microheaters. The previous generation chip revealed several design limitations during the post-processing. The challenges with dielectric etching include achieving high aspect ratio for uniform etching with high selectivity and good etch rate. A two-step dielectric RIE process was developed. Uniform etching is further facilitated by design improvements in the succeeding generation CMOS chip. Microheaters were partially or fully suspended by wet etching and Ni electroplating on Al heaters were attempted.

Chapter 5

CNT Synthesis on CMOS

5.1 Introduction

CNTs have previously been synthesized on MEMS heaters in the USN cleanroom facility using a custom-built CVD chamber, where vacuum can reach up to ~7 mbar. Acetylene (C_2H_2) has been used as the precursor gas with Ar as a supporting gas. It was estimated that the MEMS heaters locally reached ~850-900 °C during the CNT synthesis, which was monitored and adjusted by electrical control during the joule heating; the MEMS polysilicon heaters reached the desired CNT growth temperature when the heater resistance dropped down by ~10-20% after reaching its peak value [275,276]. However, this was not the case for the fabricated CMOS polysilicon microheaters. These heaters resemble the MEMS heaters, but the layer thicknesses are much smaller (~8-10 times) in CMOS. Apart from the heater thickness, material properties of the polysilicon layers are also different in the AMS 350 nm CMOS process compared to the MEMS polysilicon layer as their doping materials and concentrations can differ. The initial CNT growth settings were adapted from the previous work on MEMS to emulate the growth results on the CMOS microstructures. Since the CMOS-MEMS heaters did not reach the same growth temperatures as the MEMS heaters, similar growth results were not achieved. Growth quality of the CNTs improved upon changing some synthesis conditions (such as changing catalyst, adding etching gas), in-depth analysis on the resultant CNTs however was out of scope for this PhD work. The results from this chapter will be included in *Article 9 (in preparation)* and two other planned articles.

5.2 CNT growth process

On a post-processed CMOS chip with fabricated CMOS-MEMS polysilicon microheaters, a thin catalyst layer (~2-3 nm iron) is deposited on the CMOS chip by e-beam evaporation using a multi-technique thin film deposition system (ATC 2030-HY, AJA International, USA). In this maskless process, iron deposits all over the chip, however,

such a nanolayer is much thinner than the oxide layer (~250 nm) beneath the polysilicon layers, hence, there is no risk of forming short circuit between the polysilicon structures. In semiconductor processing, metal contaminants such as the CNT catalysts (e.g., Fe, Ni, Co) can cause p-n junction leakage as they can diffuse in the transistor regions [277], which can significantly influence the device characteristics. In our process, the thin metal catalysts are deposited during a post-CMOS fabrication step, where the regions with electronics are covered with thick dielectric and only the microheater regions are exposed. Hence, the metal catalyst exposure to the transistor regions is avoided.

Very low deposition rate (0.07 Å/s) is set for the catalyst deposition process to ensure good adhesion between Fe and the exposed polysilicon layers, which reduces Fe layer lift-offs during the CNT synthesis. The CMOS chip (3 mm × 3 mm) is then attached on a ceramic chip carrier using double-sided copper tape for wire bonding. The polysilicon microheaters are connected to custom designed aluminium contact pads through interconnecting metal layers and vias. A wire bonding system (5610, F&K Delvotec) is used to establish electrical connections between chip carrier bond pads and contact pads of the microheaters with 17 µm gold wires. The packaged chip (*Figure 5.1*) is then

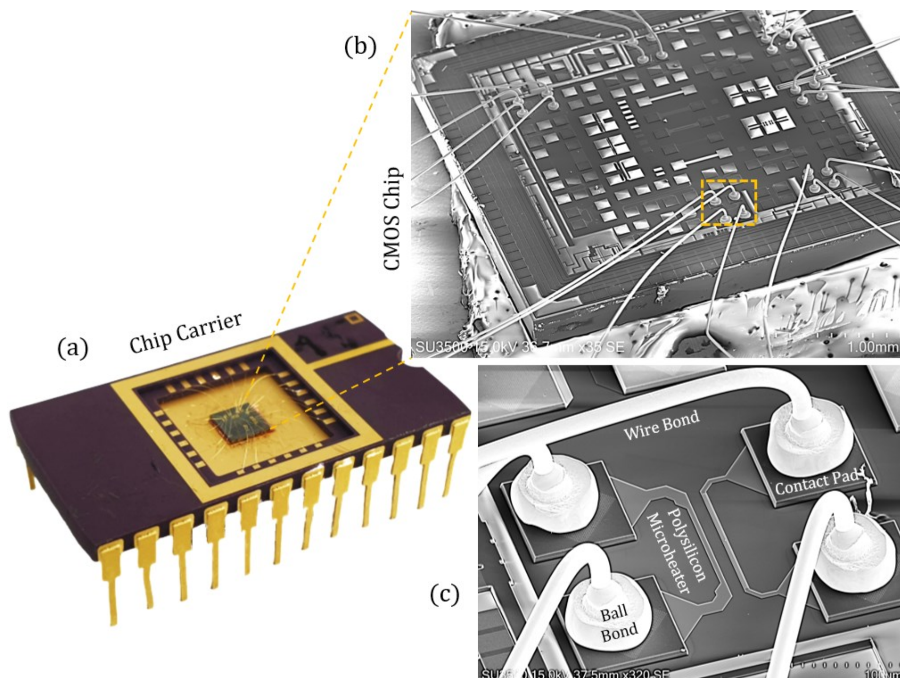


Figure 5.1: Packaged CMOS chip with CMOS microheaters. (a) CMOS chip wire bonded on a chip carrier; High magnification images of (b) bonded CMOS chip, and (c) a bonded polysilicon microheater.

placed inside a custom-built CVD chamber with a connector board, and a multi-pin vacuum feedthrough is used to transfer the electrical connections.

The experimental setup for the local CNT synthesis by thermal CVD process is shown in *Figure 5.2* along with a schematic diagram. The CVD chamber is connected to a digital pressure measurement system (VSC43 Vacuum Transducer & VD6 Vacuum Indicator Unit, Thyracont) for monitoring chamber pressure. The chamber is evacuated with the

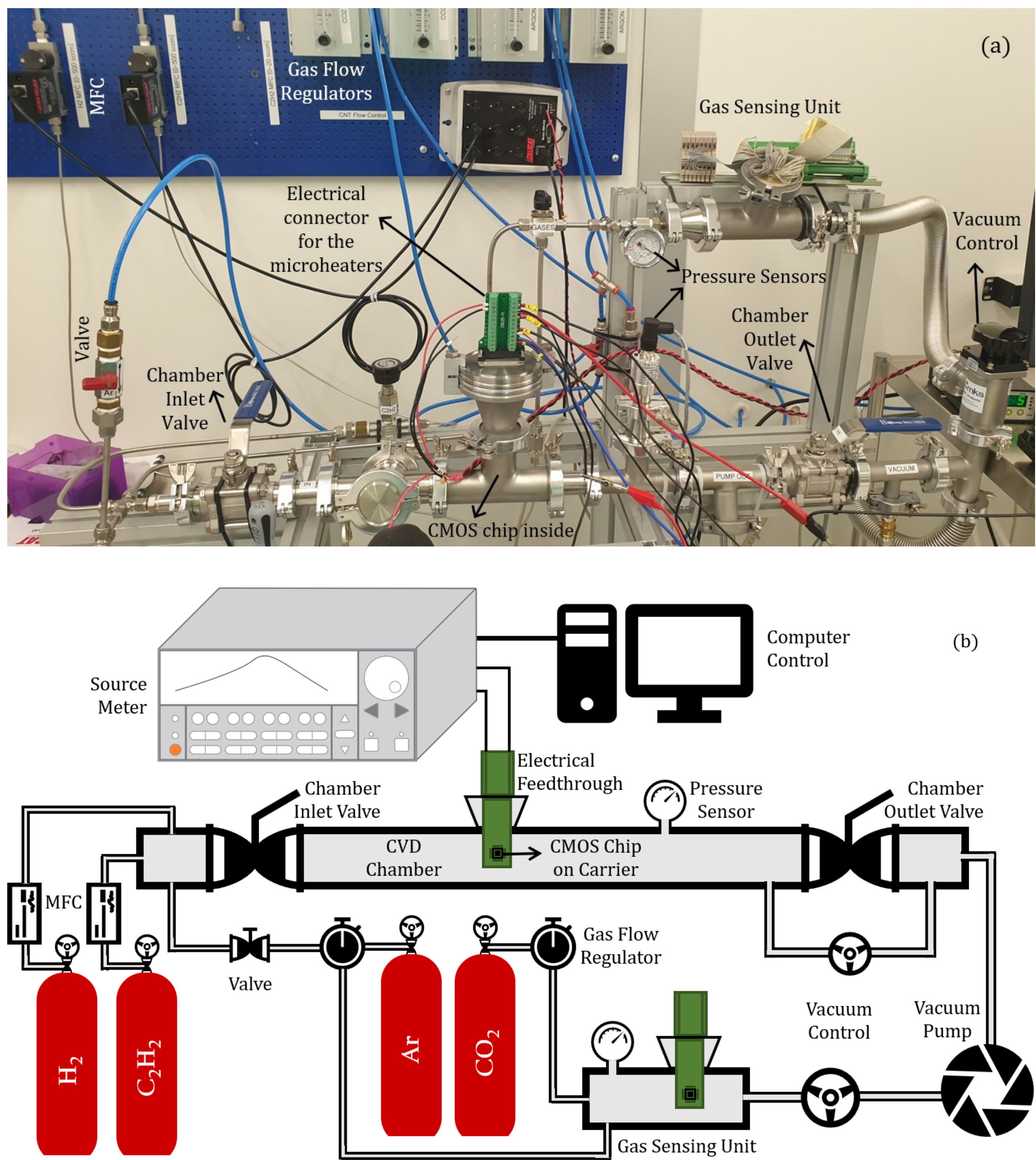


Figure 5.2: Experimental setup of CNT synthesis in CVD process. (a) Actual image, (b) Schematic diagram.

vacuum pump until the pressure is reduced to 6–7 mbar. 100 sccm Ar is introduced in the chamber, while the outflow vacuum controller is used to keep the chamber pressure near 400 mbar. A CMOS-MEMS microheater is then activated by joule heating, and the heater temperature is raised slowly by gradual voltage increase with a dual-channel source meter (2602 System SMU, Keithley). The source meter is controlled by a PC with LabVIEW program, which is also used for recording necessary experimental data. The microheater temperature is estimated by resistance measurement. The catalyst layer over the microheater breaks into metal nanoparticles at high heater temperatures. 50 sccm C_2H_2 is then introduced in the chamber using a mass flow controller (MFC). The hydrocarbon gas decomposes into hydrogen and carbon upon contact with catalyst nanoparticles at high temperatures (~650–900 ˚C). Carbon dissolves into metal nanoparticles and CNTs start to grow on the CMOS-MEMS microheater.

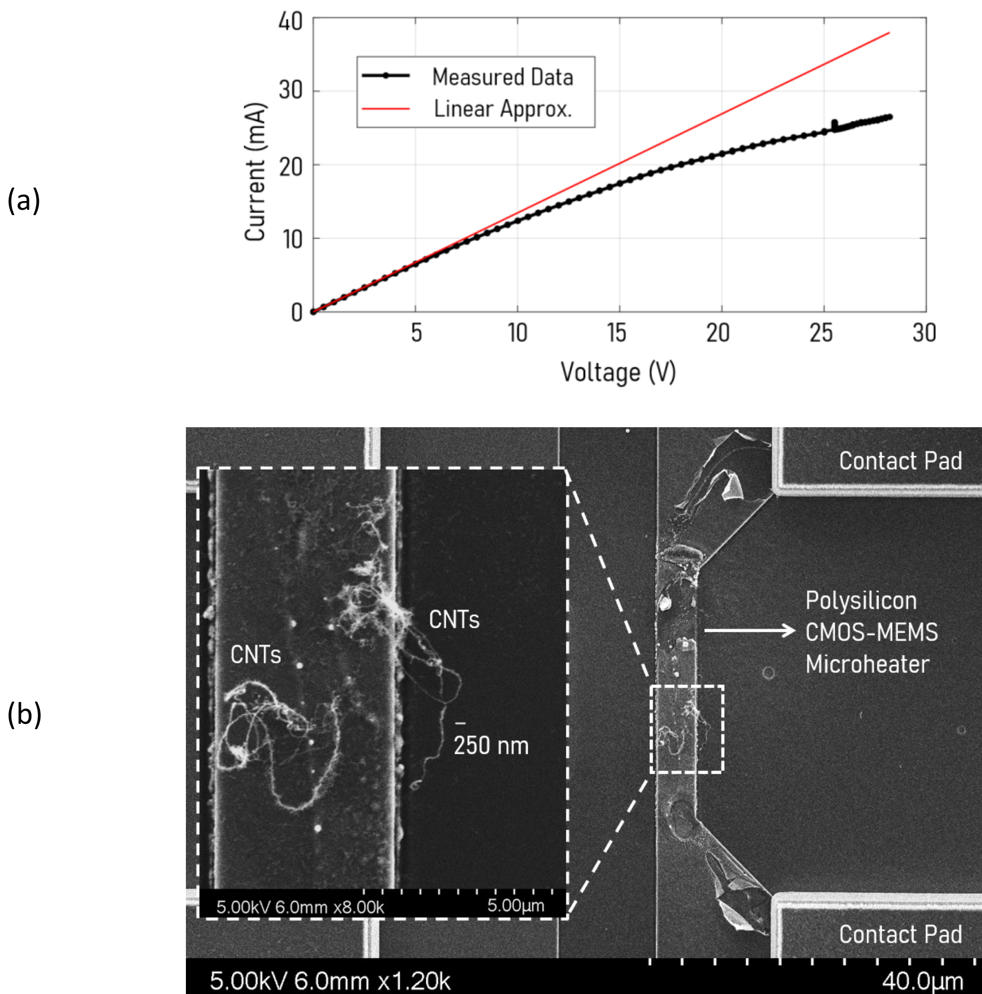


Figure 5.3: CNT synthesis on a polysilicon CMOS-MEMS microheater. (a) IV curve; (b) Synthesized CNTs.

Figure 5.3a shows the I-V curve of the resistive heating process. The CNT synthesis was attempted at different operating voltages of a heater to identify a suitable heater voltage range where the CNT synthesis temperature is obtained. Controlling the temperature was the most challenging part of the CNT growth process on the polysilicon CMOS-MEMS microheaters. The microheaters were breaking down before reaching temperatures in the region of 800-900 ˚C. Based on the heater characterizations, maximum temperature of 650-800 ˚C on the heater surface can be estimated. Details on the challenges of CMOS microheater temperature is provided in *section 7.2*. CNTs grow within 5-10 minutes at the synthesis condition inside the CVD chamber, then the heater temperature is gradually decreased to room temperature. SEM images of the synthesized CNTs on a CMOS-MEMS microheater are presented in *Figure 5.3b*.

5.3 Effect of catalysts

The major challenge of growing CNTs in the CMOS-MEMS microheaters was obtaining high temperature on the heater surface. The microheaters were mostly generating very local CNT synthesis temperature before mechanical breakdown as detailed in *section 7.2 & 7.3*. Therefore, CNTs were mostly growing in a local heater region, surrounded by potential CNFs and amorphous carbons (a-Cs). As the maximum temperature of the microheaters could not be increased significantly without changing some constraints on polysilicon layers defined by the foundry CMOS process, the CNT growth quality and density needed to be increased by modifying other synthesis parameters.

CNTs have mostly been grown with a developed recipe using Fe catalyst on MEMS heaters at USN [89,212,228,237]. It was attempted to reproduce those results of CNTs growth on the CMOS-MEMS heaters. Beside obtaining similar heater temperatures, other synthesis conditions were maintained. To obtain the growth quality from MEMS process, catalyst thickness was reduced from its initial 3 nm value for compensating the temperature. Apart from temperature and catalyst type, the catalyst layer dewetting rate and consequent coarsening depends on the layer thickness for a certain synthesis condition [184]. The agglomeration of Fe to form discrete islands is higher in thicker catalyst layer, resulting in larger islands for CNT growth after dewetting [278].

Experimental results of Chhowalla et al. [279] showed that CNT diameter, length and density depends on the initial catalyst layer thickness. In the synthesized CNTs, diameter decreases and length increases with reduction in the deposited catalyst layer thickness. The maximum density, however, was obtained at an optimum thickness of the catalyst layer, below which the density somewhat decreases and above which the decline in density is sharper. In the results of grown CNTs with 2 nm and 3 nm Fe (*Figure 5.4*), no significant difference was found. Diameter of the CNTs are also comparable in both cases. CNT growth was also attempted with 1 nm Fe, however, CNTs did not grow in most microheaters. This can be due to diffusion of such thin Fe into the microheater. To avoid microheater breakdown, temperature on the heaters were manually increased at a slow rate, thus the heaters were at high temperatures for extensive period (> 15 minutes). It can contribute in the diffusion of 1 nm Fe.

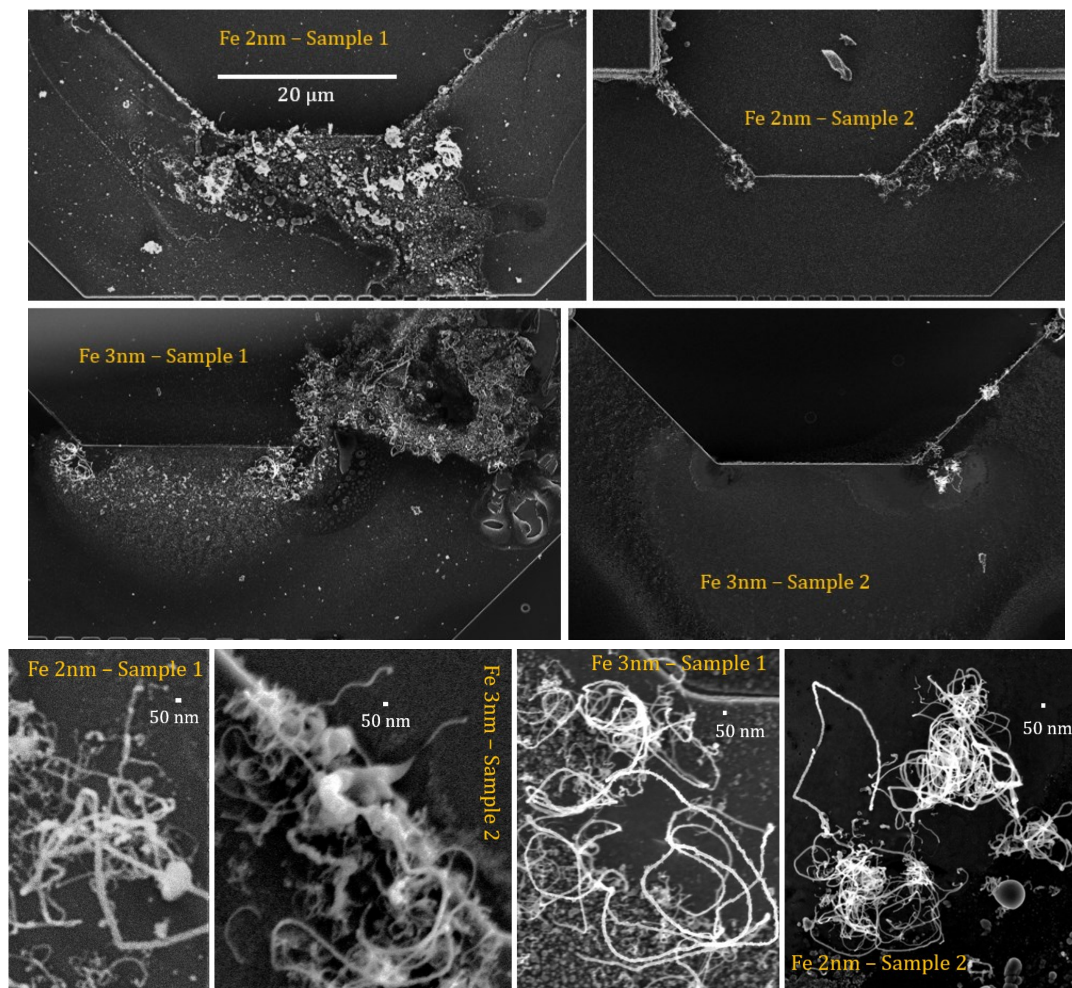
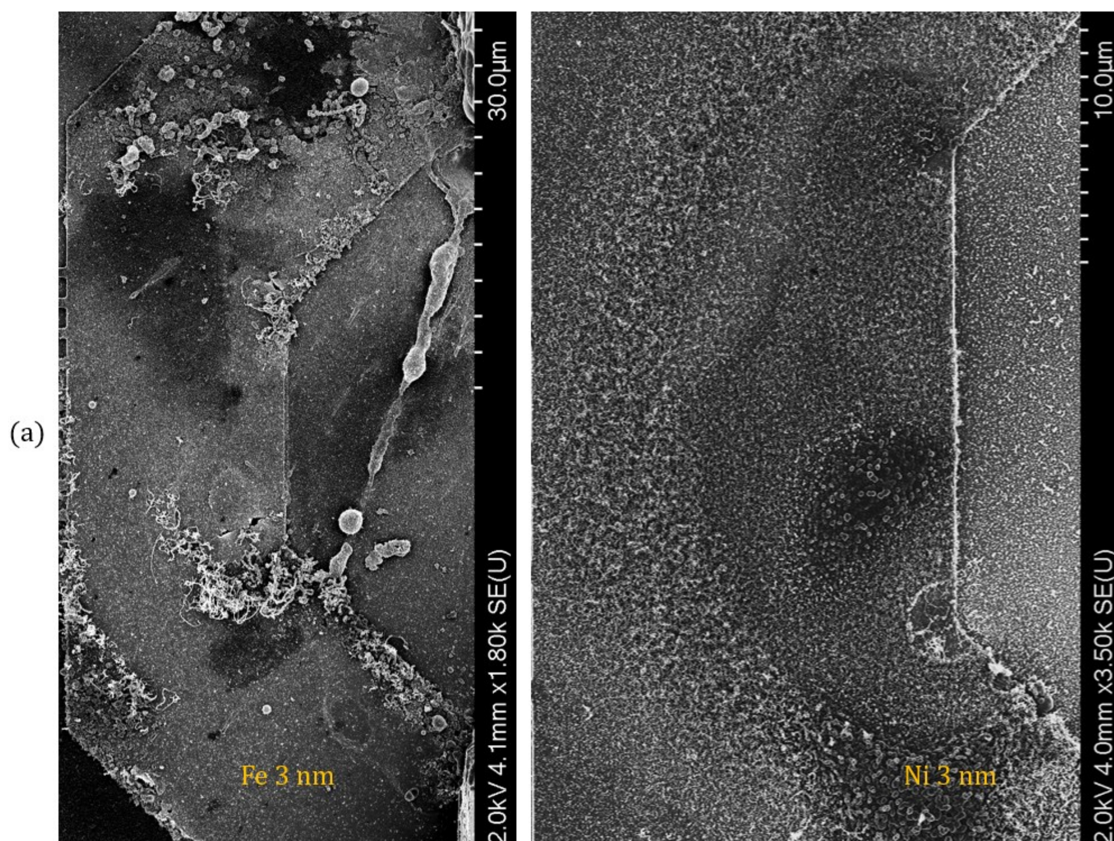


Figure 5.4: CNT synthesis using 2 nm and 3 nm Fe catalyst layers on identical polysilicon microheaters.

The most common catalysts for growing CNTs are Fe, Ni, Co transition metals. Carbon has high solubility and diffusion rate in these metals, which increases with temperature [280,281]. The resultant catalyst nanoparticles after high temperature exposure of the catalyst layer highly influence the diameter of the CNTs [177,178], while size and density of the catalyst nanoparticles can vary based on the catalyst layer interaction with the underlayer or support layer [184], which is polysilicon here. Therefore, outcome of the CNT growth will differ for different catalysts under a certain synthesis atmosphere.

The difference in growth yield is evident in *Figure 5.5*. Considering CNTs were grown on identical CMOS-MEMS microheaters without changing any other synthesis parameters, Ni as catalyst layer provided higher growth per unit area compared to Fe layer. While the CNTs from Fe are mostly in local regions on the microheater (*Figure 5.5b*), CNTs from Ni were grown all over the heater (*Figure 5.5c*). The nucleation efficiency appears to be better with the catalyst-substrate interactions of Ni-polysilicon than Fe-polysilicon under the used growth condition. Since the heater temperature is relatively low, it indicates that the activation energy required for the CNT synthesis with Ni catalyst layer



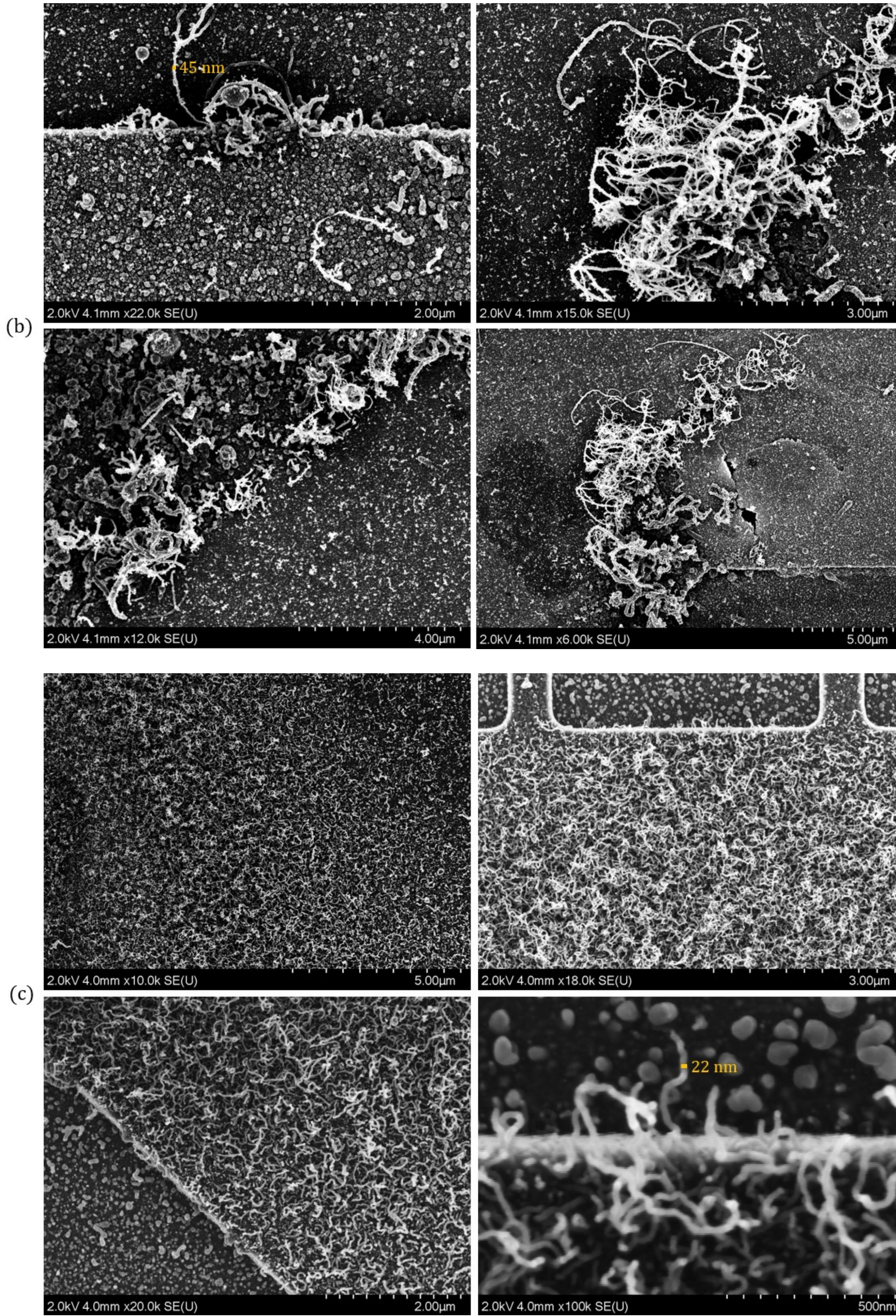
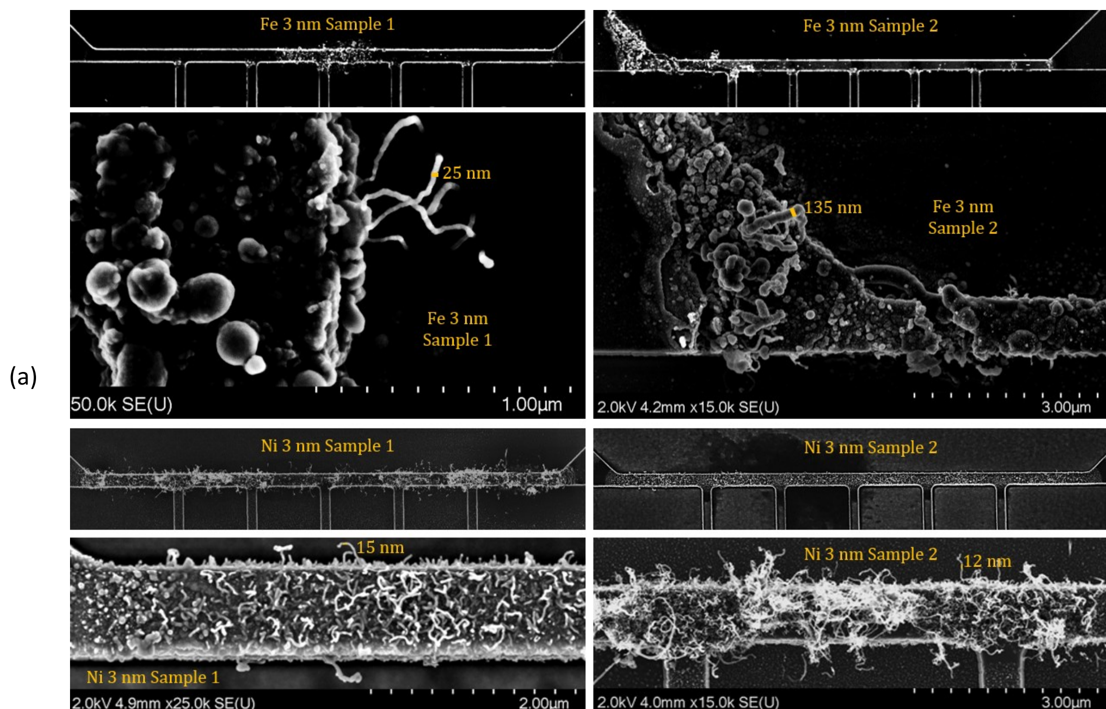


Figure 5.5: Contrast in yield of CNT synthesis with Fe and Ni catalyst. (a) Growth on identical polysilicon microheaters; Different growth regions of the heaters with (b) 3 nm Fe and (c) 3 nm Ni.

in the polysilicon microheater is lower than that of Fe. Chiang et al. [282] compared the activation energies of Fe, Ni and several combinations of Fe & Ni nanoparticles from experimental data, where the values found for Fe and Ni are 119 and 73 kJ/mol, respectively. This result is consistent with a theoretical estimation [283]. Therefore, the CNT nucleation is energetically more favourable to Ni than Fe.

CNT synthesis with 3 nm Fe and Ni has been repeated for identical growth structures in various microheater designs and similar growth results were found for other heaters (*Figure 5.6*). For the narrow microheater in *Figure 5.6a*, CNTs and CNFs were found in a local region for Fe samples where the heater temperature was high. In contrast, CNTs were found all over the narrow heater for the Ni samples. The difference in growth between samples with same catalyst layer can be due to some variations in heater temperature. A comparison between 2 nm Fe and 3 nm Ni is also shown for a wide heater in *Figure 5.6b*. Similar outcome is also evident here. While the Fe-based heater has visually interpreted a-C, CNFs, and defects along with small regions of good quality CNTs, the Ni-based heater has CNTs of similar quality all over its surface. On average, diameter of the Ni-based CNTs were also found to be smaller than the Fe-based CNTs.

(a)



(b)

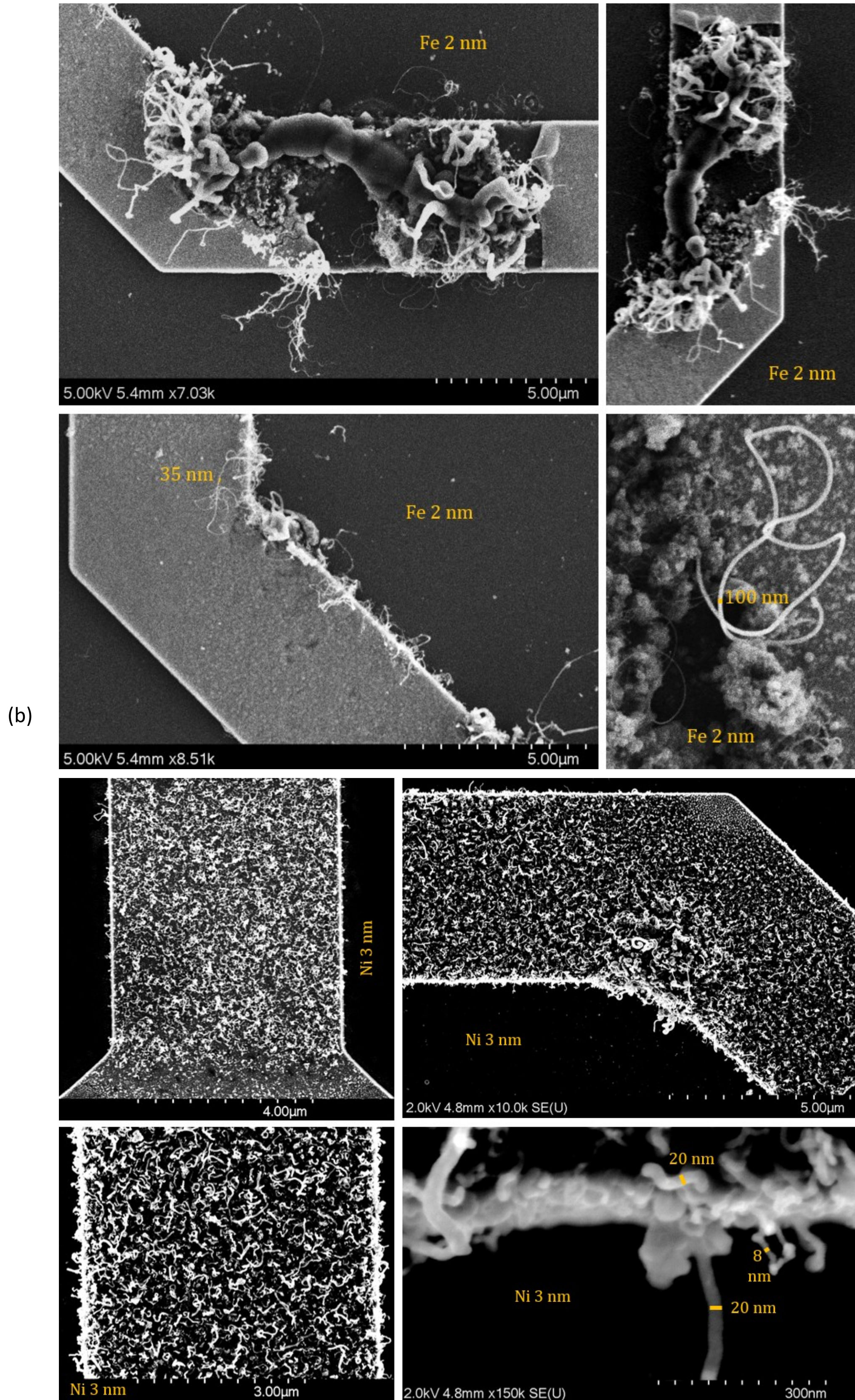


Figure 5.6: CNT synthesis with Fe and Ni catalysts. (a) Narrow microheaters with 3 nm catalyst layers; (b) Wide microheaters with 2 nm Fe and 3 nm Ni.

Figure 5.7 shows the growth results of the smallest microheater design in the second-generation chip. In most cases, CNTs were not synthesized on this heater with Fe catalyst, whereas, growth with Ni as catalyst was successful. Sample-1 of 3 nm Fe shows the best result with Fe, where no recognizable CNTs were found on the heater surface. Sample-2 of 3 nm Fe have dewetted catalyst layer, a phase before any growth took place. While Sample-1 of 3 nm Ni has some CNT growth on the heater centre, sample-2 did not quite reach the CNT synthesis temperature.

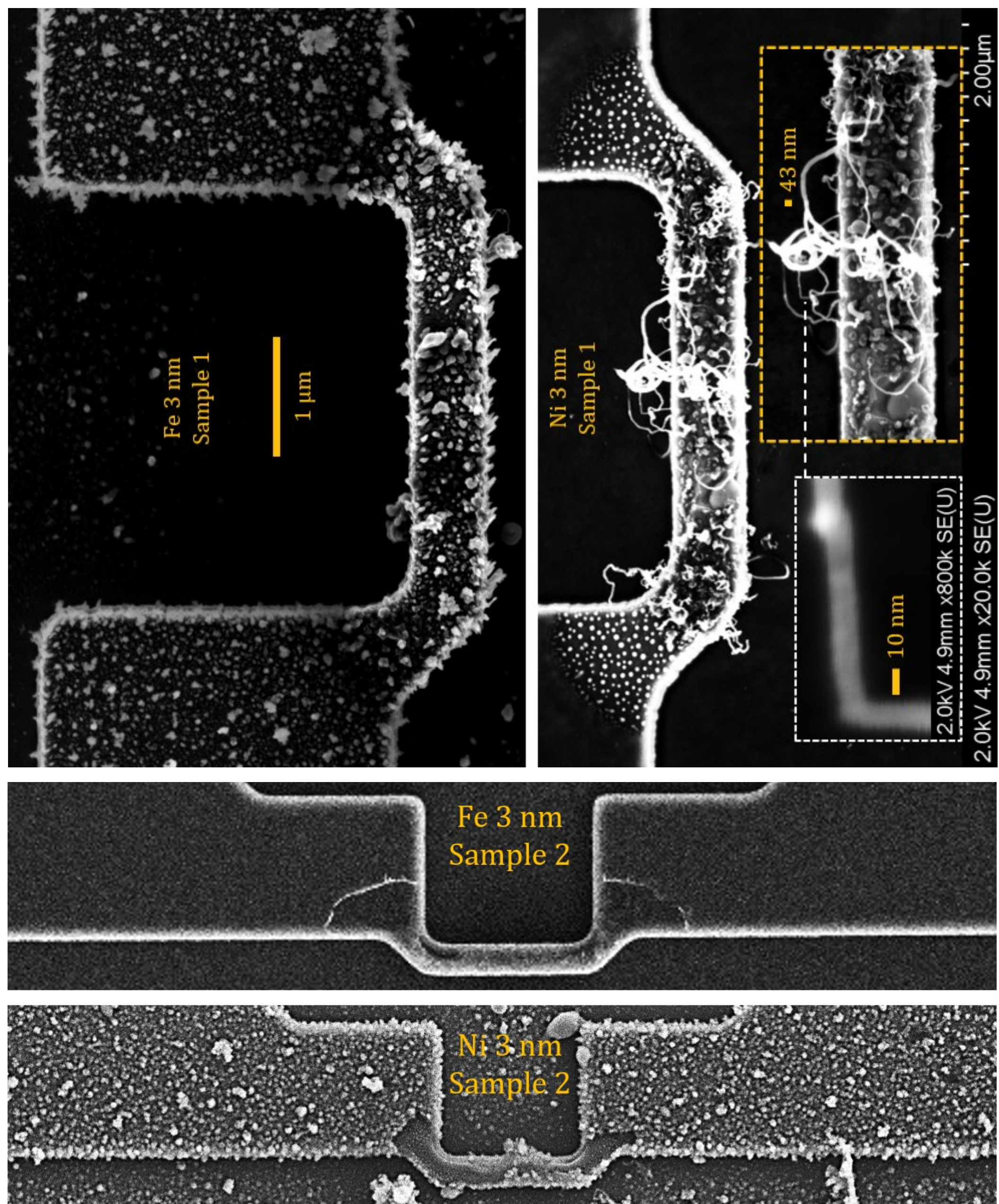


Figure 5.7: Small polysilicon microheater with no CNT growth with Fe and limited CNT growth with Ni.

Surface of identical polysilicon heaters with 3 nm Fe and Ni catalyst layers were analysed by atomic force microscopy (AFM) after surface energy minimization of the thin films upon joule heating. 3D plots of 1 µm × 1 µm surface area on the microheaters along with the line scans of the corresponding heaters presented in *Figure 5.8* reveals the size differences in Fe and Ni nanoparticles. This difference is comparable to the diameter of the Fe- & Ni-based CNTs. The difference in dewetting could be due to the catalyst layer

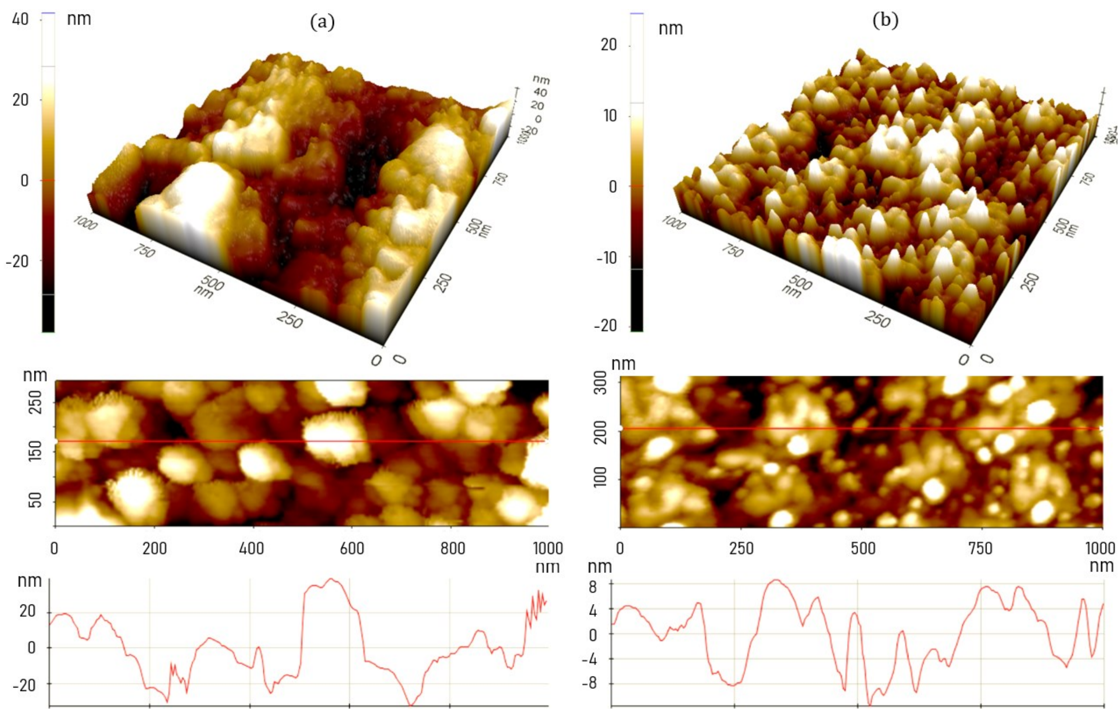
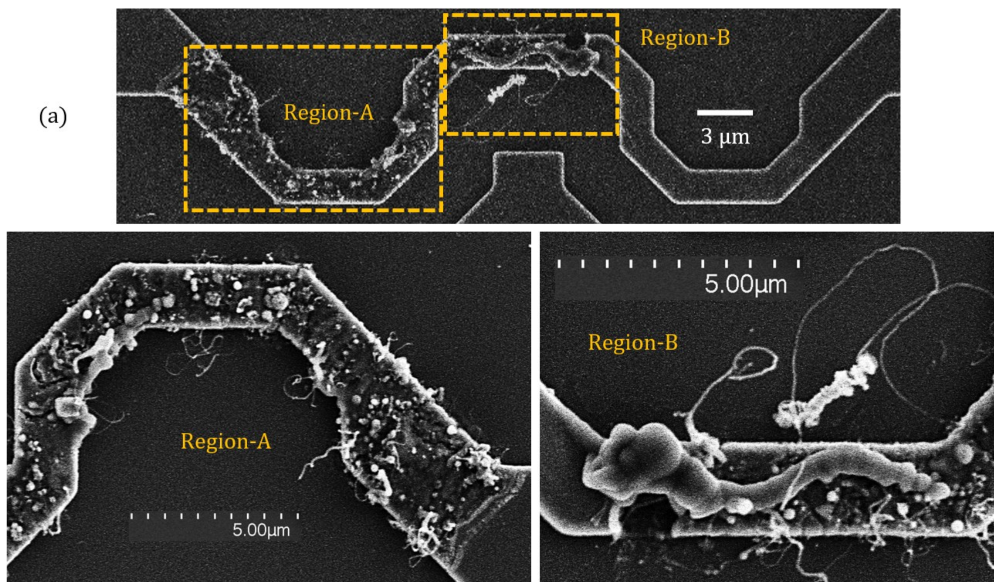


Figure 5.8: AFM characterization of identical polysilicon microheaters with (a) 3 nm Fe and (b) 3 nm Ni.



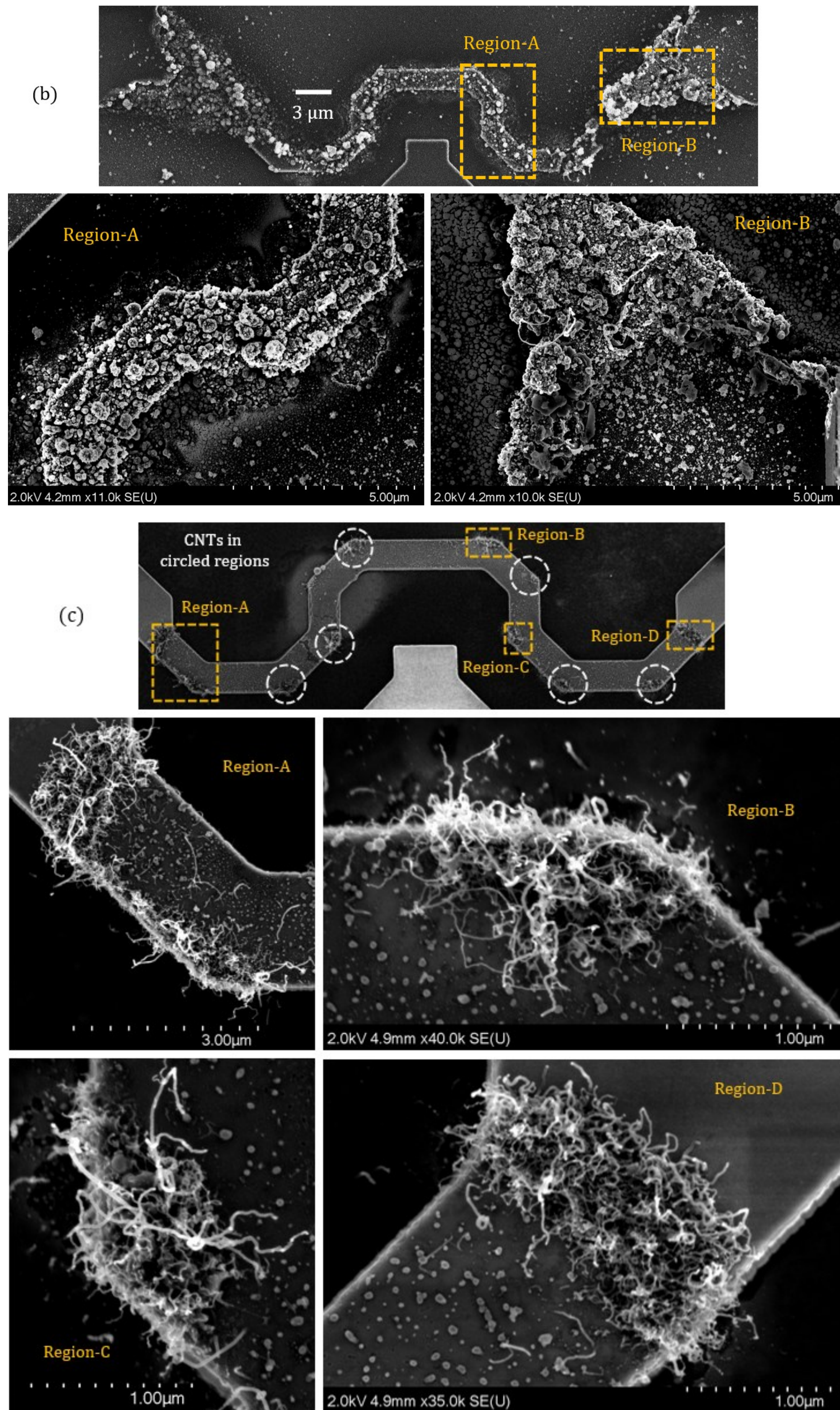


Figure 5.9: CNT synthesis on a wave-shaped polysilicon microheater with variations in catalyst; (a) 2 nm Fe; (b) 3 nm Fe; (c) 3 nm Ni.

interaction with the support layer (polysilicon). For a certain temperature, formation of the macroscopic islands from the thin film depends on the density and diffusion co-efficient of the catalyst [284].

Figure 5.9 shows the comparison between 2 nm Fe, 3 nm Fe and 3 nm Ni on identical wave-shaped polysilicon microheaters. The 2 nm Fe heater in *Figure 5.9a* has CNTs and visibly interpreted CNFs and a-Cs, mostly in one side of the heater. The growth result is similar for 3 nm Fe heater (*Figure 5.9b*), where the carbon structures are deposited on the entire heater. In contrast, 3 nm Ni heater (*Figure 5.9c*) produced good quality CNTs on several clustered regions. Although the heater is non-suspended, the DRIE process may not be completely anisotropic. In this heater, the regions with sharp corners are more likely to have under-etching and thus have lower conductive heat loss to the substrate resulting in higher local temperatures for CNT synthesis.

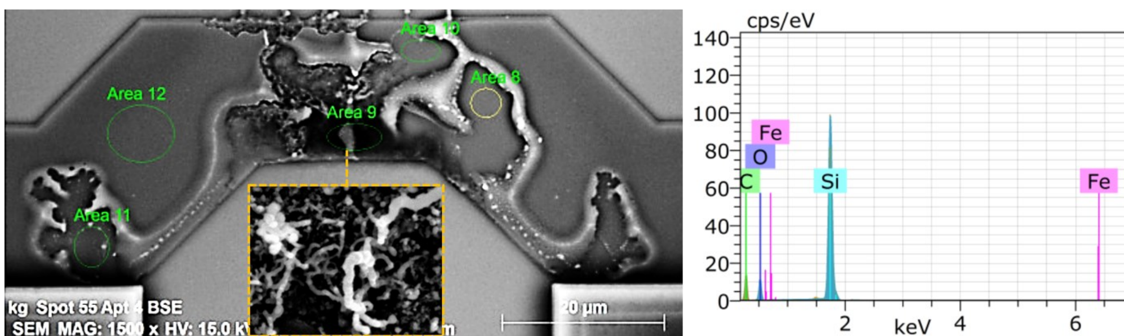


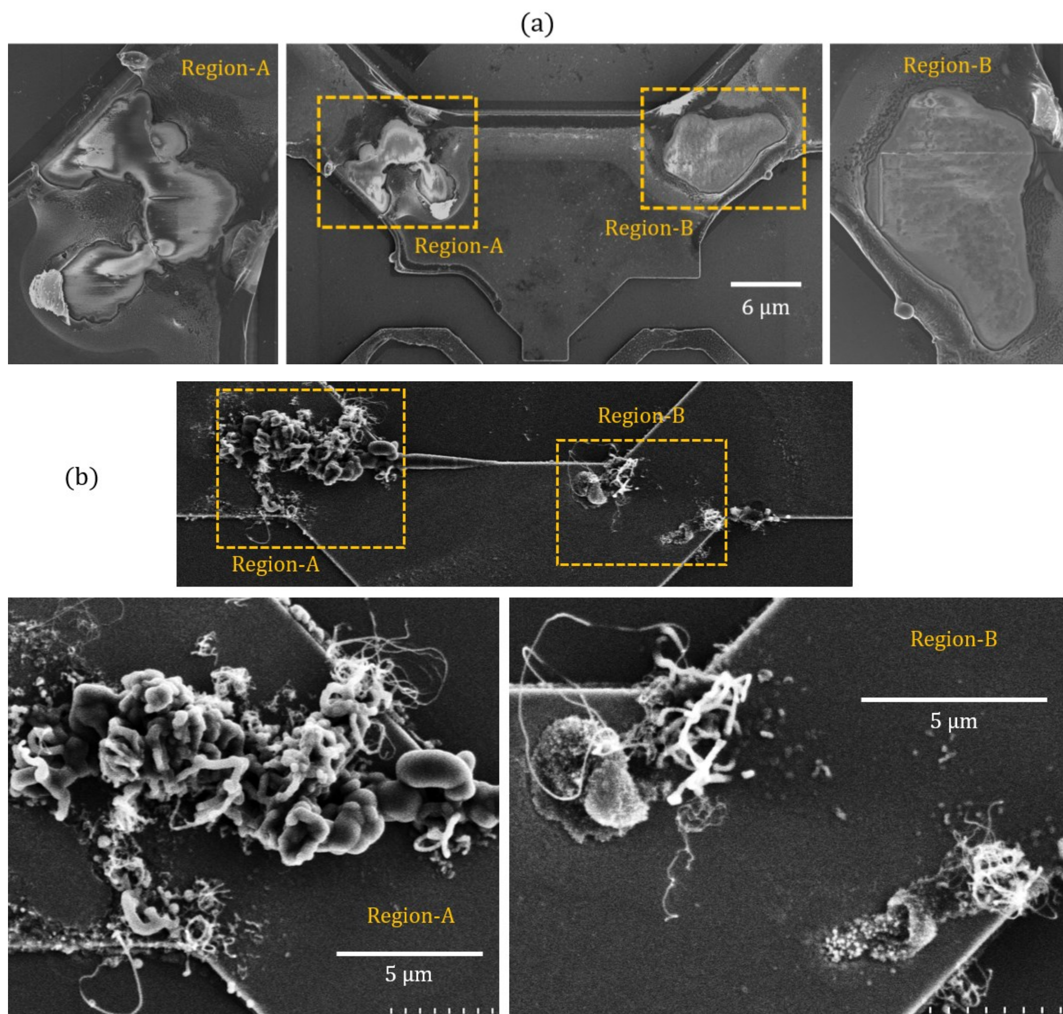
Figure 5.10: EDX analysis on different regions of a microheater.

Table 5.1: Atomic percent (%) on the different scanned regions of the EDX analysis**.**

Spectrum	C	O	Si	Fe
Area 8	8.19	31.99	59.82	-
Area 9	59.27	15.56	25.07	0.09
Area 10	8.39	31.26	60.35	-
Area 11	14.04	29.66	56.10	0.20
Area 12	10.69	27.16	61.70	0.45

In some microheaters with high surface area, dewetting of the catalyst layer is recognizable. *Figure 5.10* shows the EDX analysis on different regions of a heater and the obtained atomic percentage of different elements are summarized in *Table 5.1*. Area-9 has high carbon content, where CNTs are found (inset of *Figure 5.10*). The catalyst layer is depleted after dewetting in the visually recognizable area-8 & area-11, which is indicated in *Table 5.1*.

Figure 5.11 shows three different conditions on identical heaters with 2 nm Fe, 3 nm Fe and 3 nm Ni. Catalyst depletion can be seen on two corner regions of a 2 nm Fe heater in *Figure 5.11a*. CNTs can be found on the 3 nm Fe heater, surrounded by a-Cs and CNFs (*Figure 5.11b*) in the similar corner regions where catalyst layer was depleted on the 2 nm Fe heater. *Figure 5.11c* shows the Ni-deposited microheater with high density CNT synthesis on those high temperature heater regions. Pisana et al. [278] found that CNTs



(c)

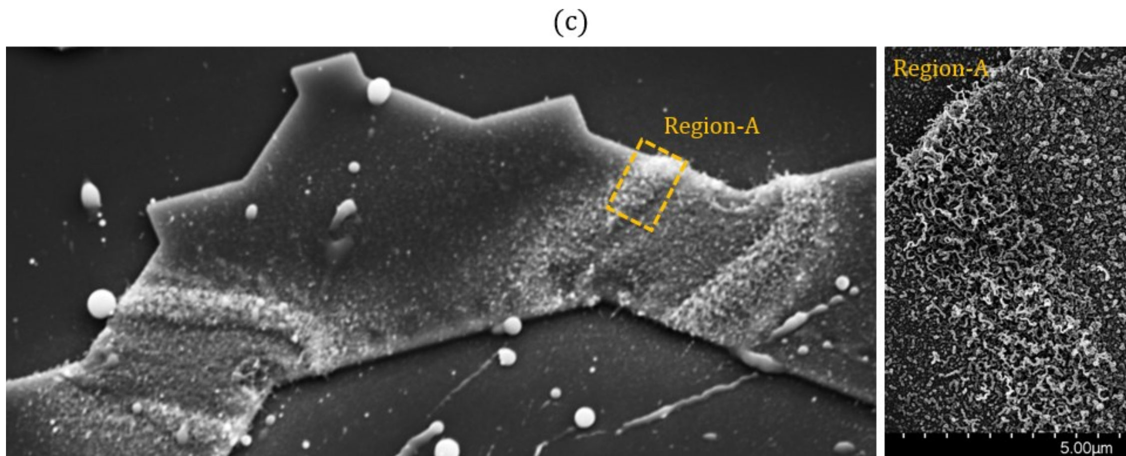


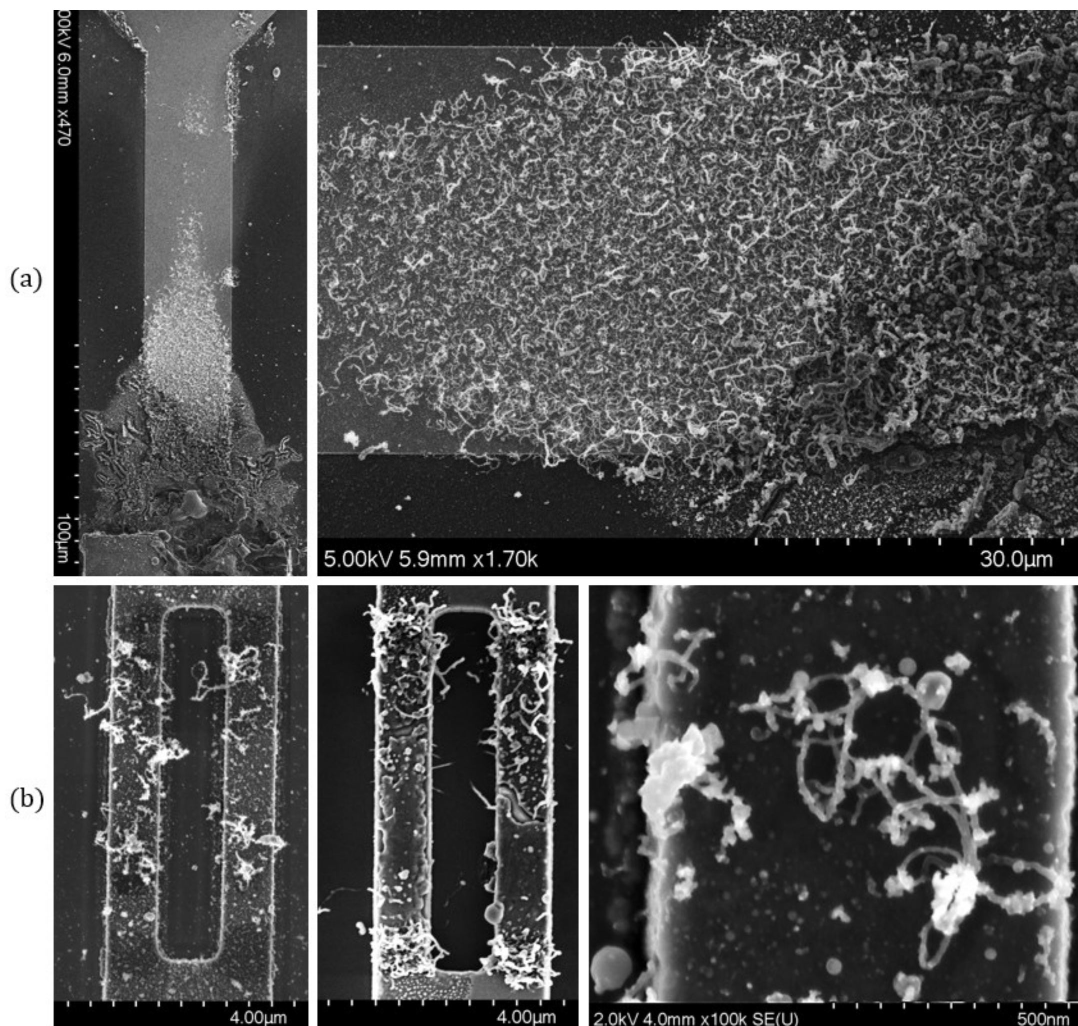
Figure 5.11: Dewetting of catalyst thin film on a polysilicon microheater and CNT synthesis. (a) Depleted catalyst in a heater with 2 nm Fe; (b) Synthesized CNTs and CNFs with 3 nm Fe on similar regions of catalyst agglomeration; (c) CNTs on similar regions of an identical non-suspended heater with 3 nm Ni.

grow in the regions where the catalyst layer thickness is thin, and the CNT density reaches peak in the thinnest catalyst region. This is consistent with the results in *Figure 5.11*, where the regions with thin catalyst layer due to high heater temperature are seen *Figure 5.11a*, while some CNT growth and high-density CNT growth are seen on similar heater regions in *Figure 5.11b* & *Figure 5.11c*, respectively.

Although CNT growth with Ni provided desired CNT quality, diameter, and yield, the CNTs were not growing long enough to establish a connection between the adjacent heaters. A comprehensive development process is required to successfully increase CNT length as suggested in *section 7.4*. CNT synthesis with Co was also attempted. Sugime et al. [285,286] reported low-temperature CNT growth using Co-Al-Mo multilayer catalyst. In this catalyst, Al acts as a diffusion barrier layer, without which interdiffusion occurs between Co and Mo due to their strong interaction [285]. Based on the results obtained in [285], 5 nm Mo followed by 0.5 nm Al and 2.5 nm Co layers were deposited on a CMOS chip. However, the low-pressure conditions (6.0×10^{-2} mbar base and 3 mbar synthesis pressure) could not be replicated in our custom-built CVD chamber. In addition, 40 nm Cu was used as the support layer in [285], whereas, we use polysilicon as the support layer. CNT synthesis was attempted on the CMOS-MEMS microheaters with 10 mbar chamber pressure, which did not result in any CNT growth. Due to time constraints and limited CMOS chips, this process was not further investigated.

5.4 Growth on different polysilicon microheaters

The fabricated CMOS chips have various polysilicon microheater designs as presented in *section 3.3*. CNTs were grown in most of these heaters. For some large microheaters, especially made of poly-2 layer, the CNT synthesis temperature could not be obtained as the source meter reached the maximum voltage of 40 V. The maximum obtained heater temperatures vary from one design to other, which is reflected by the quality and density of synthesized CNTs on them. Results of CNT synthesis on some of the microheaters with distinct features are presented in *Figure 5.12*. A large heater with high surface area is shown in *Figure 5.12a*, where CNTs were grown on one half of its surface. CNTs grown on the heaters with etching holes are shown in *Figure 5.12b*. CNTs are seen to be grown on narrow spikes of heaters (*Figure 5.12c*), while the synthesis temperature does not reach on the wide spike regions of some heaters (*Figure 5.12d*).



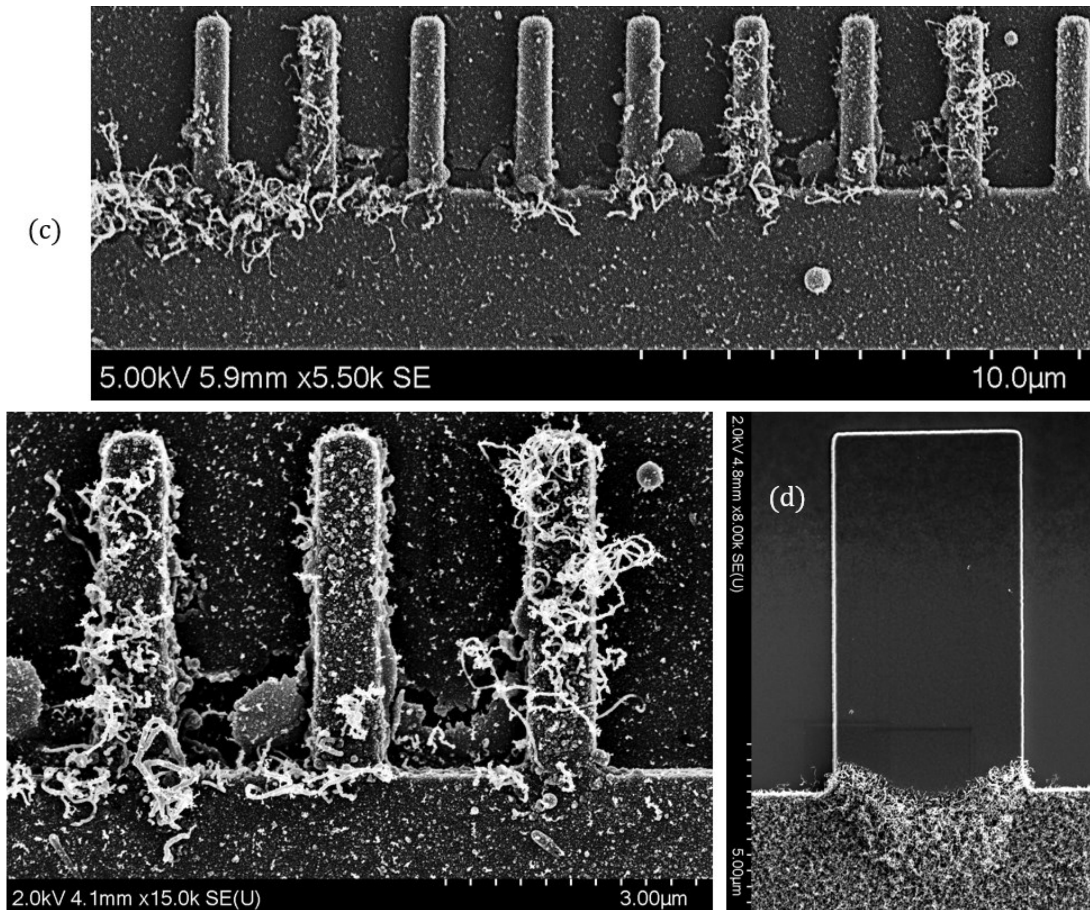


Figure 5.12: CNT synthesis on various polysilicon microheaters. (a) Large heater; (b) Growth around etching holes; Growth (c) on narrow spikes, and (d) below wide spikes.

CNTs have also been grown on microheaters with stacked poly-1 and poly-2 layers as shown in *Figure 5.13*. In this heater with Ni catalyst, CNTs are deposited on the entire heater surface, covering both poly-2 and exposed poly-1 regions. CNT density is normally found to be higher in heaters with high surface area, when compared among the Ni catalyst results. Heat is distributed on the large surface of these heaters, while the high temperatures of the narrow heaters are generated on local regions. Among the relatively narrow heaters (~5 µm wide), the stacked poly-1 – poly-2 heater in *Figure 5.13* produced the best growth results. These heaters are thicker in the stacked region, where the two polysilicon layers are also separated by a thin SiO_2 layer. Due to their thickness advantage, they should be able to obtain higher temperature before mechanical failure occurs, in comparison to the heaters made of individual polysilicon layers, and hence, they can grow CNTs more effectively.

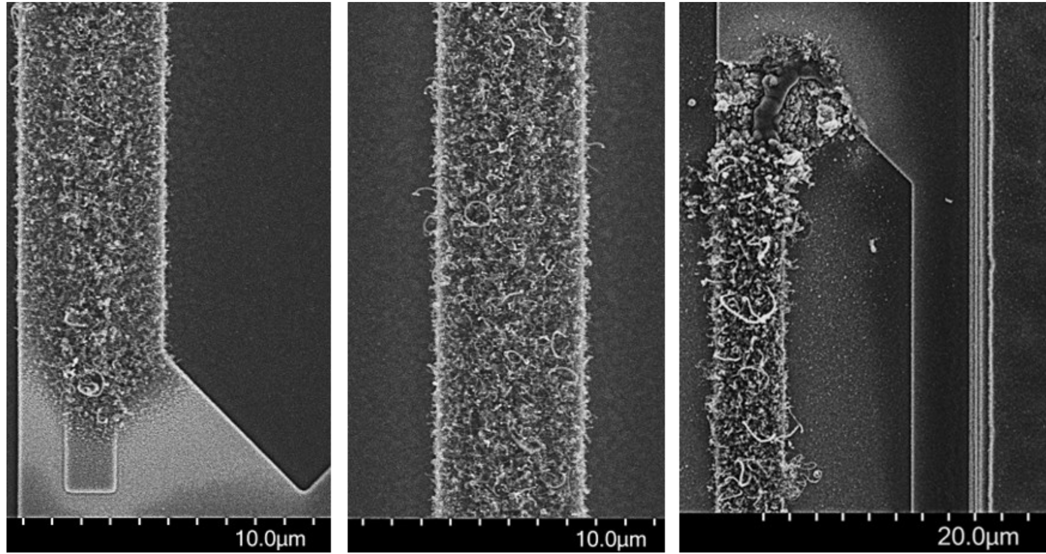
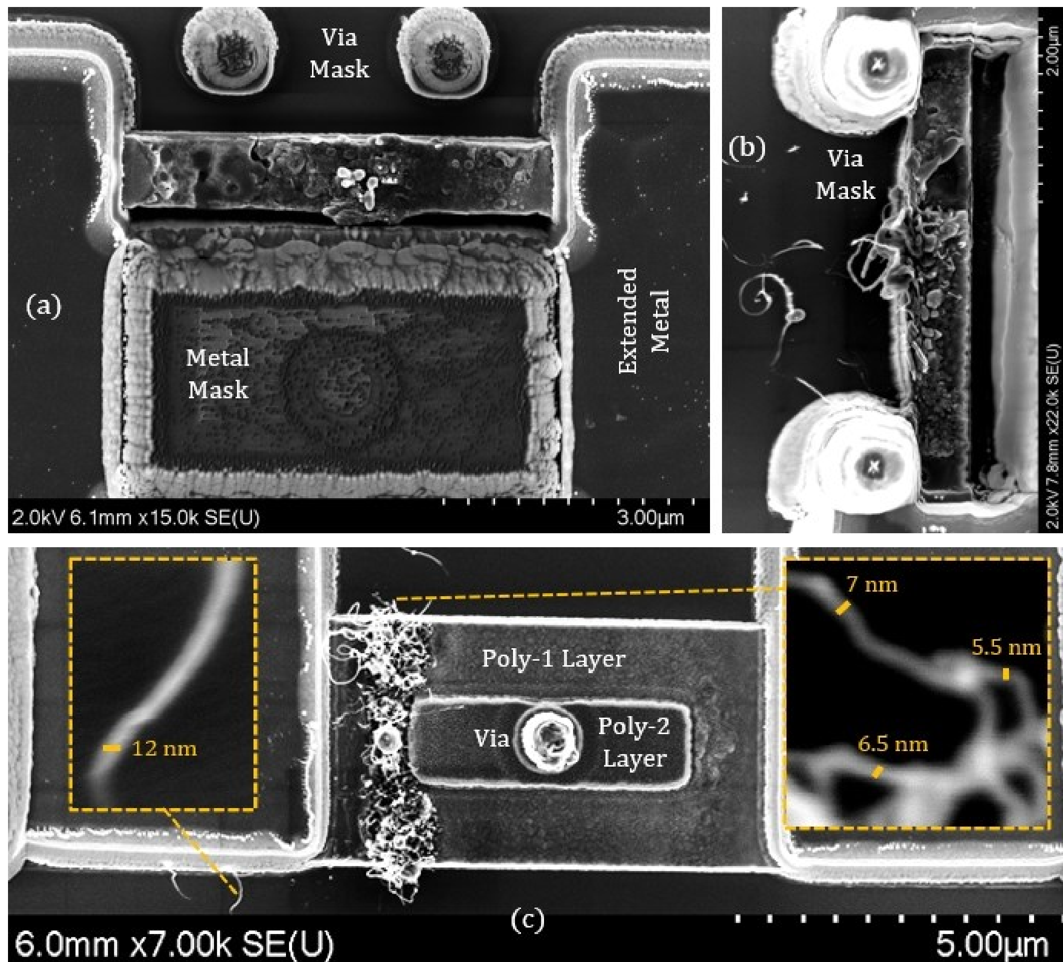


Figure 5.13: CNT growth on a stacked poly-1 – poly-2 microheater with Ni catalyst.

It was possible to grow CNTs or CNFs on some of the first-generation microheaters as shown in *Figure 5.14 & 5.15*. The microheater with metal and via masks in *Figure 5.14a*



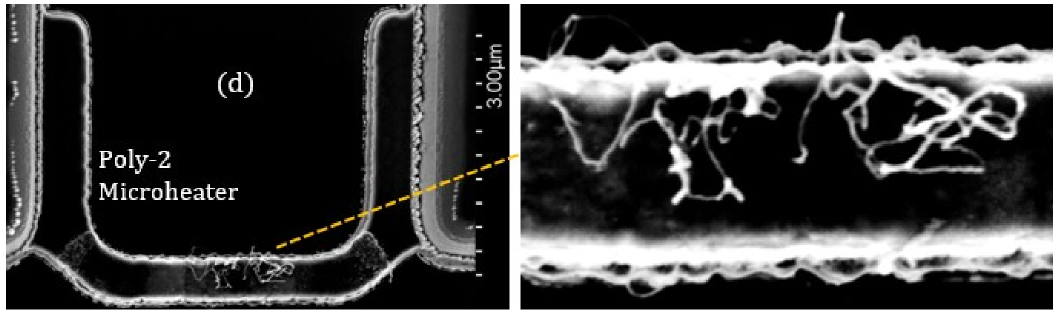


Figure 5.14: CNT synthesis on various polysilicon microheaters from the older generation CMOS chip. Growth on heater with (a) metal mask, (b) via mask, (c) stacked poly-1 – poly-2, and (d) small surface area.

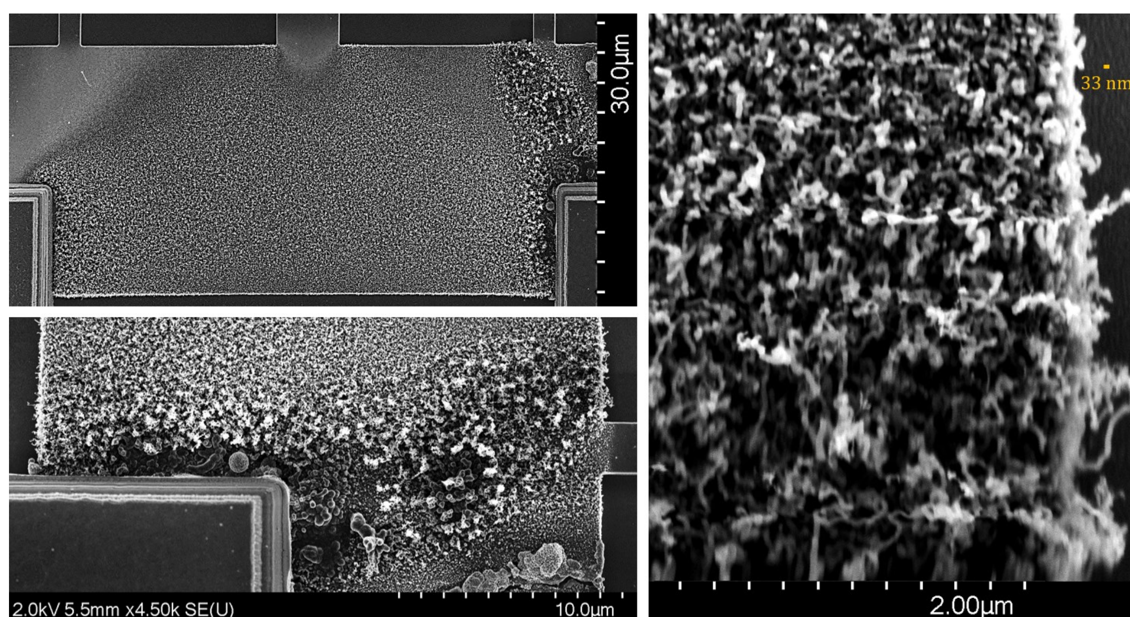
Figure 5.15: CNT synthesis on most effective polysilicon heaters from the older generation designs.

have fibre-like structures in the centre, while the heater with only via masks have very few CNT / CNF growth (*Figure 5.14b*). A stacked poly-1 – poly-2 microheater from the first-generation CMOS chip provided some CNT growth with CNTs below 10 nm diameter on one side of the poly-1 layer as shown in *Figure 5.14c*. The microheater with smallest surface area among all designs (both first and second generation) have few CNTs grown on the middle of the heater (*Figure 5.14d*).

Among the older microheater designs, the most effective CNT growth was observed in two adjacent heaters (*Figure 5.15)*. These CNTs were synthesized with 3 nm Fe catalyst. Region-B of *Figure 5.15* shows an unusual growth location in the metal contact pads. Since the Al layers would melt at ~660 °C, the CNTs with diameter mostly below 20 nm could have grown at a lower temperature, considering no deformation is seen on the contact pads.

CNT growth with Ni catalyst on two identical poly-1 and poly-2 heaters are compared in *Figure 5.16*. Density of CNTs in both heaters is similar. CNTs with smaller diameter in poly-2 heater indicates relatively higher heater temperature. I-V curves along with power consumption of these heaters are compared in *Figure 5.17*. Regardless of the initial resistance values of the heaters, they would consume similar power to generate

(a)



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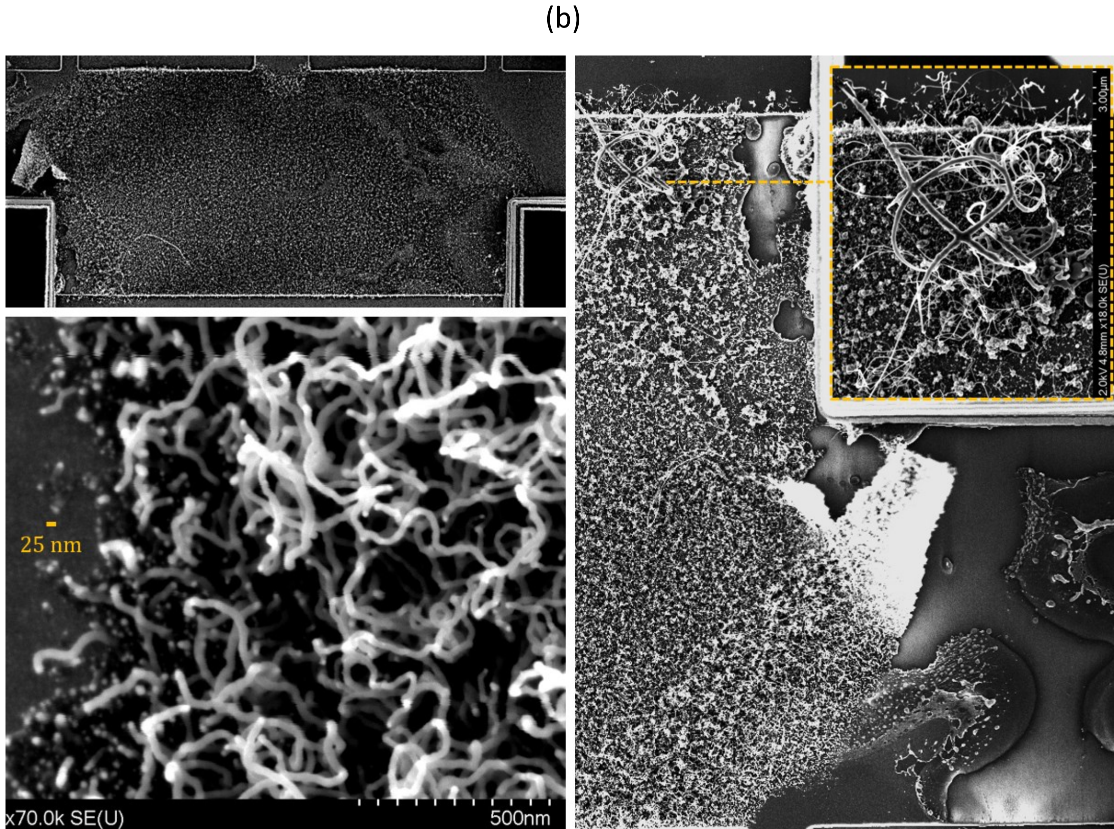


Figure 5.16: CNT synthesis on (a) poly-1 and (b) poly-2 microheaters with same surface area.

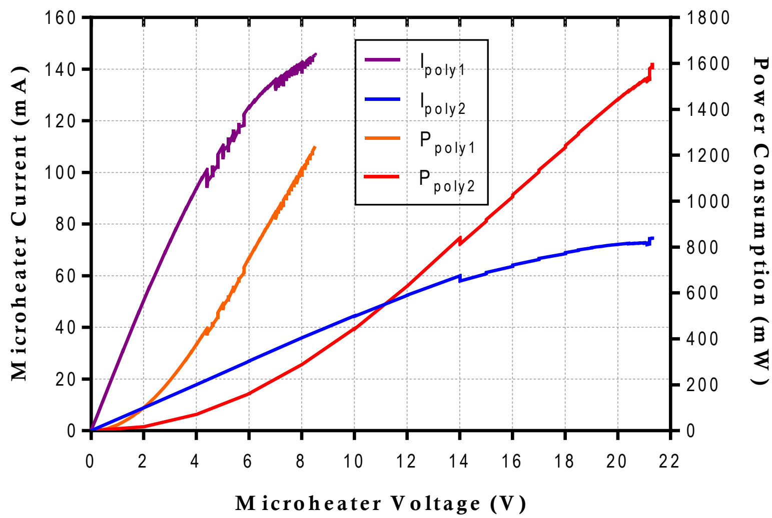


Figure 5.17: Electrical characterization of identical poly-1 and poly-2 heaters.

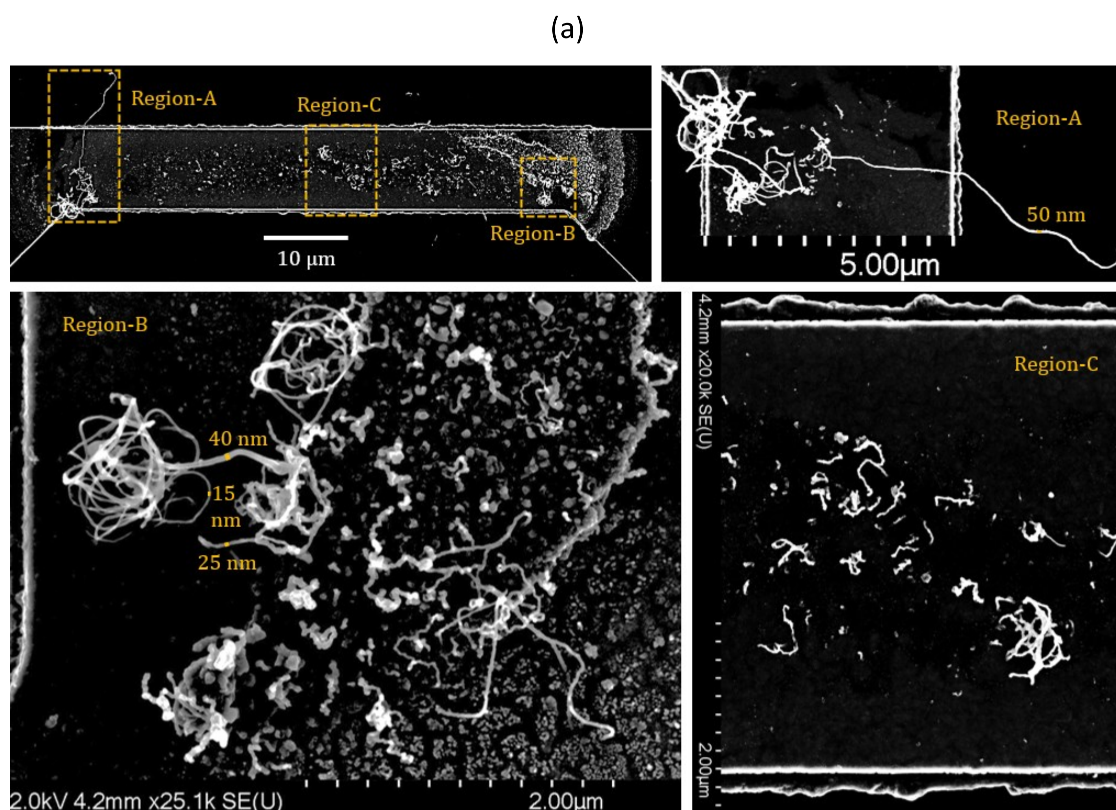
comparable temperatures. However, poly1 heater will have slightly higher heat loss due to its higher thickness (~100 nm) than poly2. The maximum power of the poly-2 heater (~1600 mW) reached during the CNT synthesis process was higher than that of poly-1

heater (~1250 mW). The 350 mW higher power in poly-2 microheater supports the claim of its higher temperature.

5.5 Growth on suspended microheaters

CNTs were synthesized on the partially or fully suspended microheaters. *Figure 5.18* shows the CNT synthesis results on identical non-suspended (with 3 nm Fe) and partially suspended (with 2 nm Fe) poly-2 microheaters. The overall CNT growth on the non-suspended heater (*Figure 5.18a*) appears to be better than the partially suspended heaters, which can be due to higher mechanical vulnerability of the latter ones. Among the partially suspended heaters, the one etched by pad-etch (*Figure 5.18b*) had less suspension and better growth in comparison to the one etched by BOE (*Figure 5.18c*). I-V curves and power consumption of the heaters are shown in *Figure 5.19*. Due to the under-etching, less heat was lost through the dielectric, thus the power consumption of the partially suspended heaters (~520 – 535 mW) was less compared to identical non-suspended heater (~700 mW) for reaching CNT synthesis temperature that results in CNTs with comparable diameters (*Figure 5.18a & 5.18c*).

(a)



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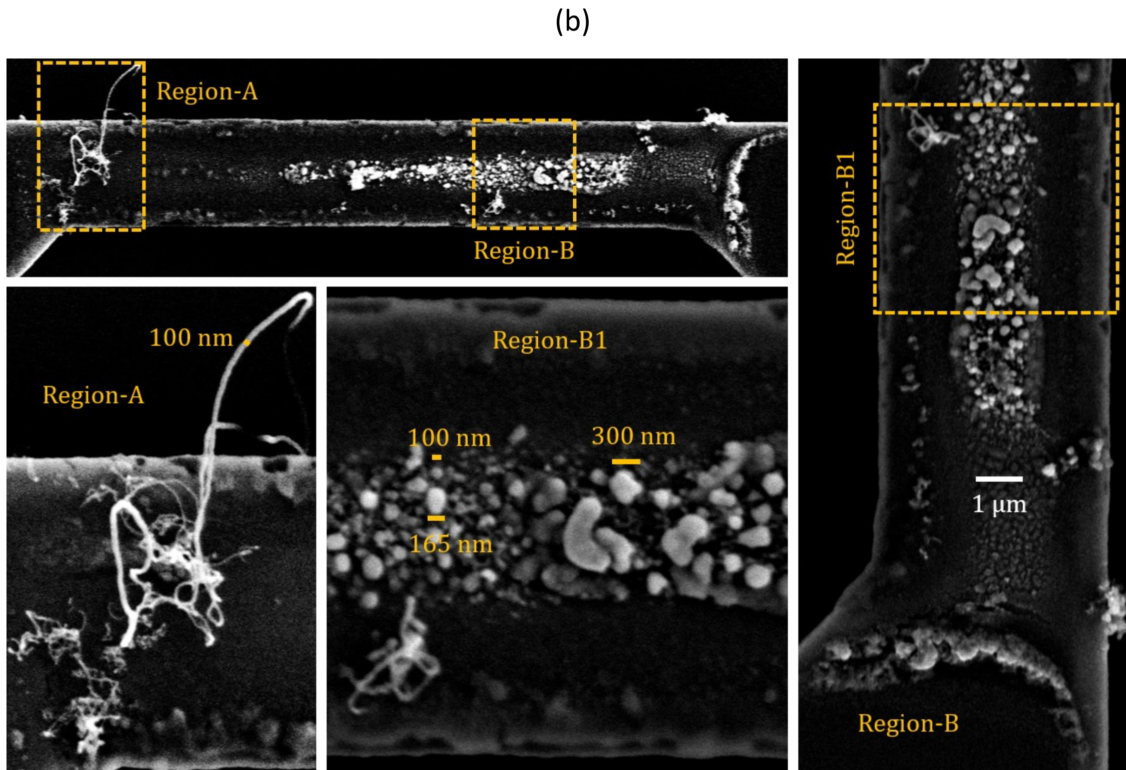

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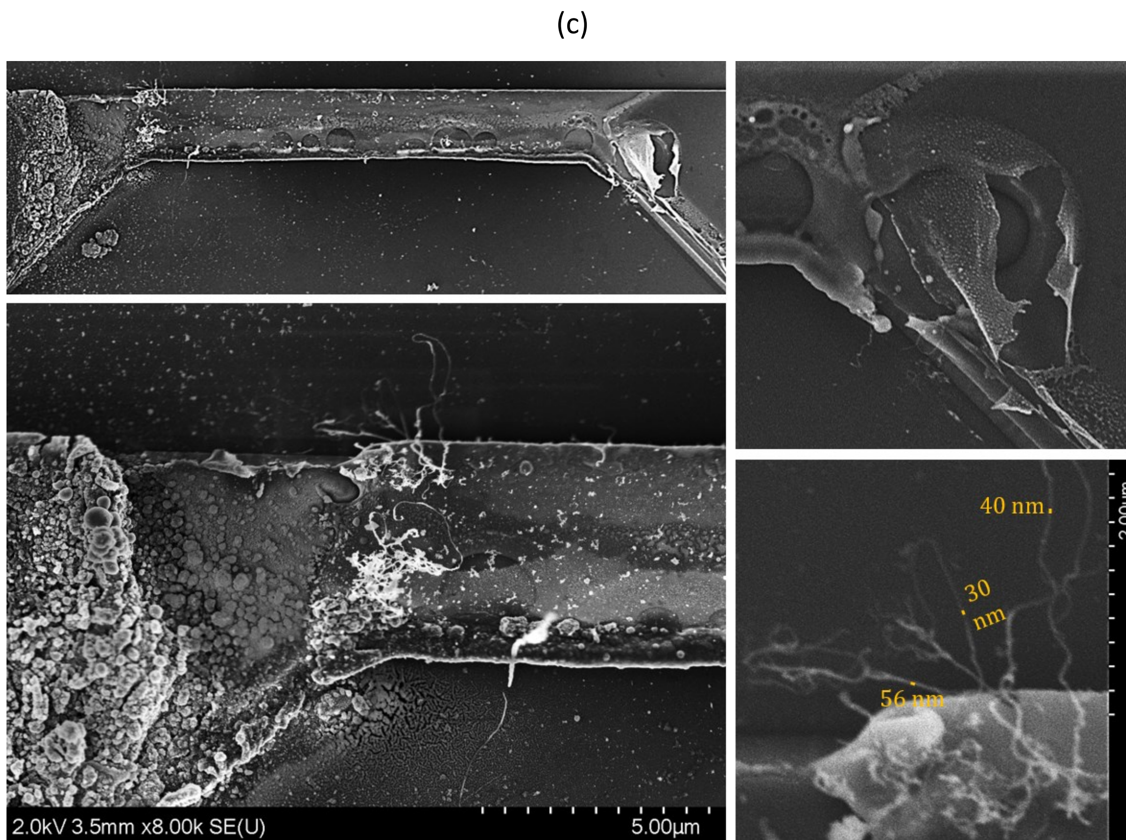


Figure 5.18: CNT synthesis on identical (a) non-suspended, (b) partially suspended (with pad-etch), and (c) partially suspended (with BOE) poly-2 microheaters.

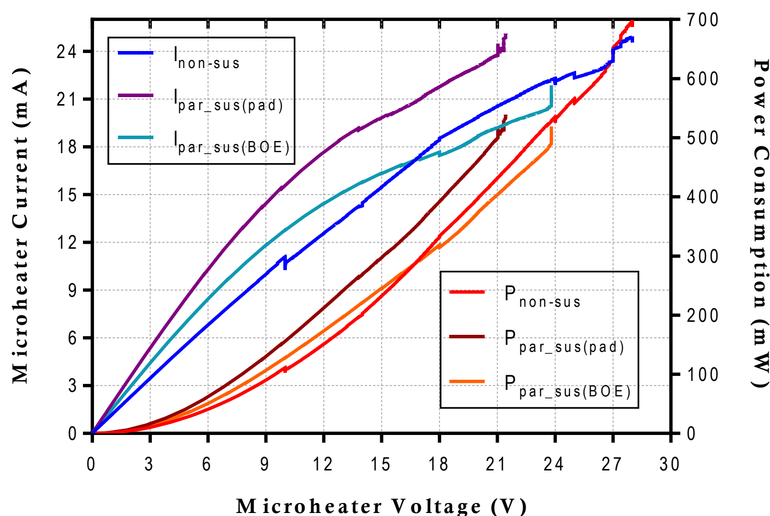
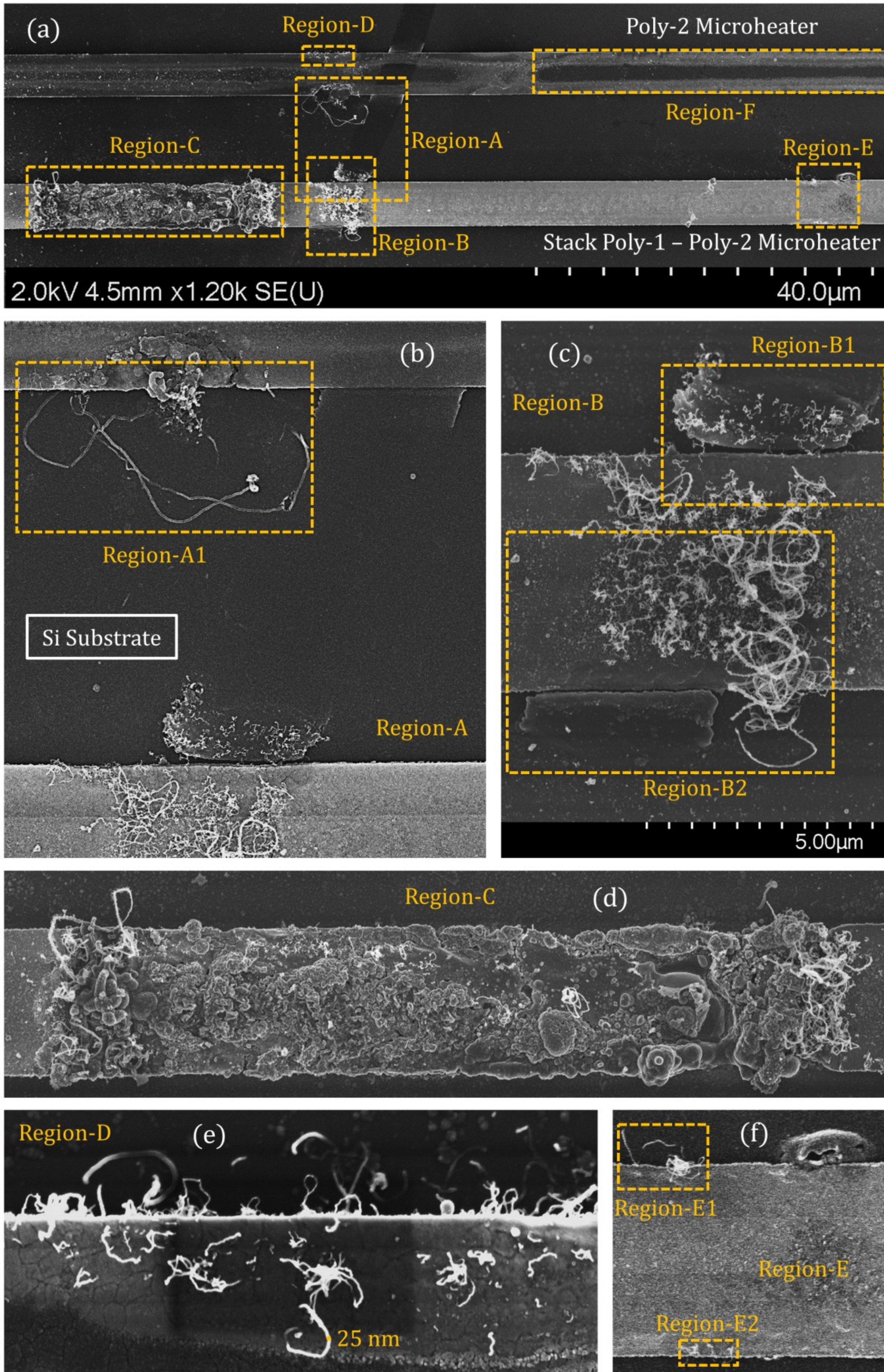


Figure 5.19: Electrical characterization of identical non-suspended and two partially suspended heaters.

The CNT synthesis results of partially suspended poly-2 and stacked poly-1 – poly-2 microheaters with identical surface area are shown *Figure 5.20*. As shown in *section 4.7*, poly-2 layer has higher under-etching than poly-1 due to thickness variation in underneath dielectric layer. Thus, the stacked poly-1 – poly-2 heater in *Figure 5.20* has less suspended regions than the poly-2 heater. Density of CNT growth is comparatively better in the stacked poly-1 – poly-2 heater. Multiple CNTs from both heaters can be seen to have connection to the silicon substrate. In addition, a pealed / broken layer can also be seen to have connection with the two microheaters through some synthesized CNTs. Although no direct CNT connection was found between the two heaters, a link was established through the CNTs connecting to the substrate. This link resulted in a finite current response between the heaters, where the CNT connections played an important part. This connection provided the best gas sensing results presented in *section 6.4*. It is difficult to recognize the exact connection path, which can be considered as a link of polysilicon – CNTs – (possible pealed layer) – silicon substrate – (possible pealed layer) – CNTs – polysilicon. Regardless of the complex nature of the connection, the role of CNTs in the established link is evident from the gas and pressure response. Multiple CNTs from both heaters were also in direct connection with the Si substrate. Region-A1 shows some longer CNTs that grown from a damaged part of the poly-2 heater and connect to the substrate. In the stacked heater, a web-like CNT bundle with low-diameter CNTs (Region-E1) formed connection with the bottom silicon surface.


(a)
Region-D
Poly-2 Microheater
Region-F
Region-C
Region-A
Region-E
Region-B
Stack Poly-1 – Poly-2 Microheater
2.0kV 4.5mm x1.20k SE(U)
40.0µm
(b)
Region-A1
Si Substrate
Region-A
(c)
Region-B1
Region-B
Region-B2
5.00µm
Region-C
(d)
Region-D
(e)
25 nm
(f)
Region-E1
Region-E
Region-E2

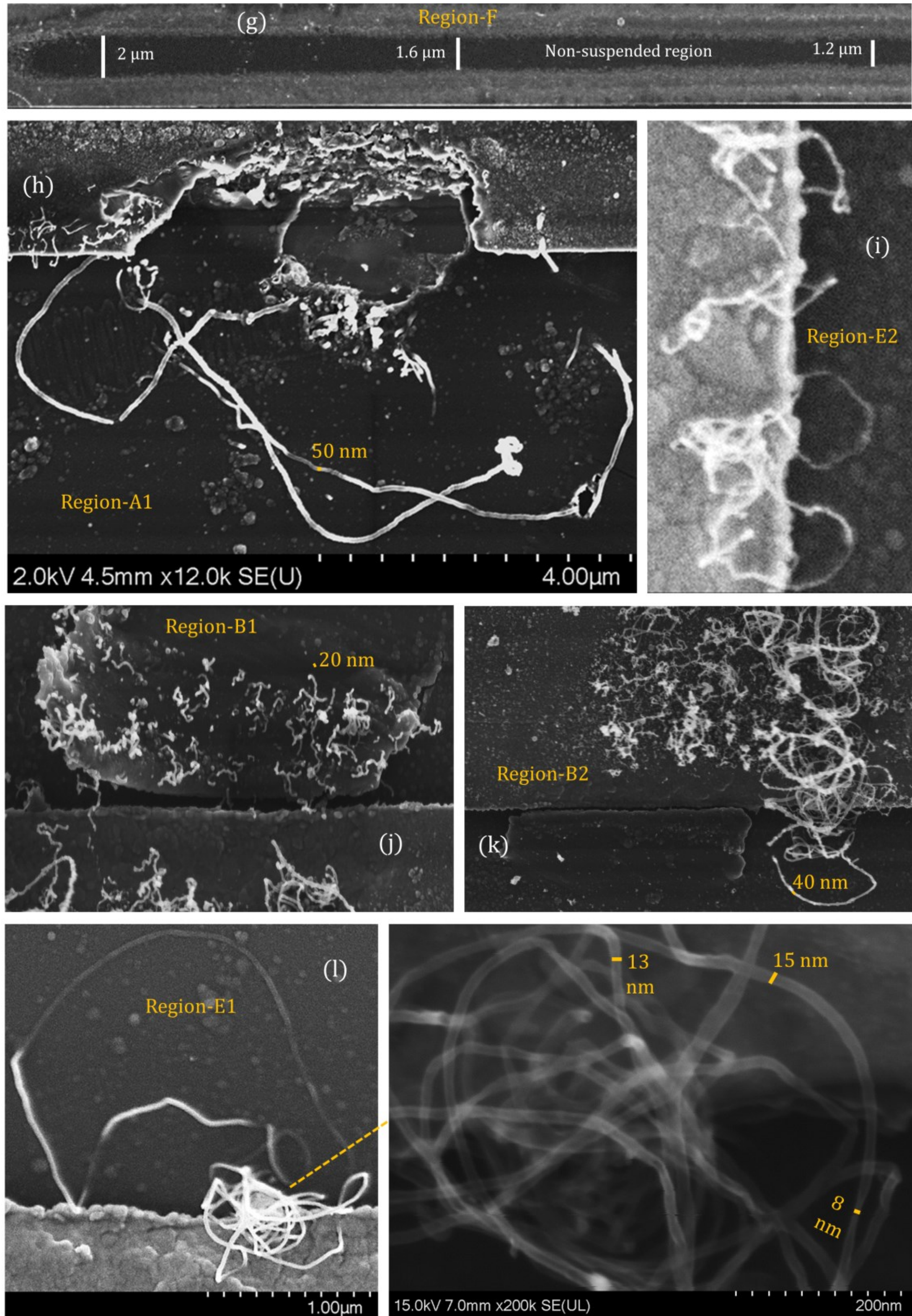


Figure 5.20: CNT synthesis on partially suspended identical poly-2 and stacked poly-1 – poly-2 microheaters with established connection through CNTs: (a) overview, (b) Region A, (c) Region B (poly-1 – poly-2), (d) Region C (poly-1 – poly-2), (e) Region D (poly-2), (f) Region E (poly-1 – poly-2), (g) Region F (poly-2), (h) Region A1 (poly-2), (i) Region E2, (j) Region B1, (k) Region B2, and (l) Region E1.

Electrical characteristics of the heaters are shown in *Figure 5.21*. The poly-2 heater was operated at near 40 V, which is the maximum value provided by the power supply. Obtaining the CNT growth temperature on the poly-2 heater was only possible as it was partially suspended. CNT growth temperature was not achieved in any of the non-suspended identical poly-2 heaters. The poly-2 and stacked heaters were operated at ~850 mW and ~1200 mW during the CNT synthesis. Although the two heaters have same surface area, the thickness is higher in the stacked one, hence, a direct power consumption comparison cannot be made.

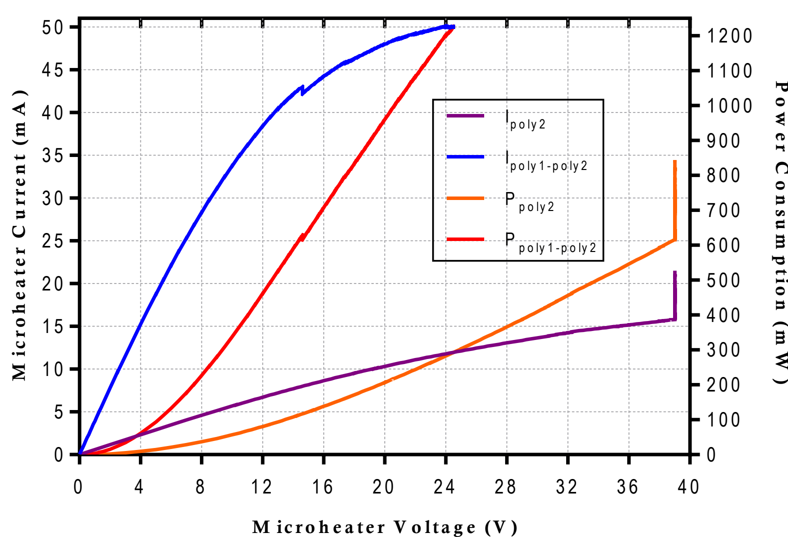


Figure 5.21: Electrical characterization of identical poly-2 and stacked poly-1 – poly-2 heaters.

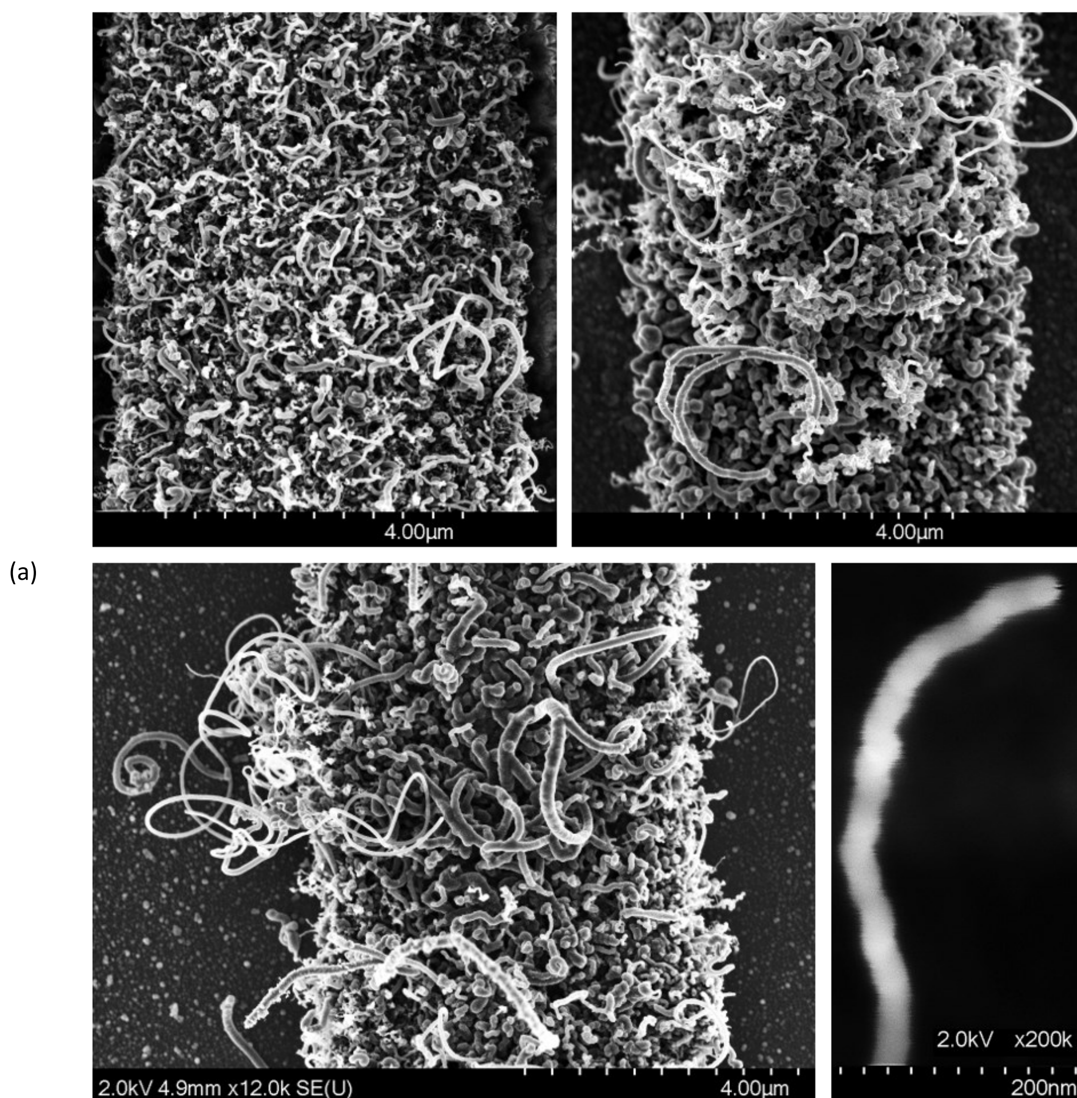
CNTs were synthesized on the stacked heater before growing on the poly-2 heater. The poly-2 heater was kept at 39 V during the CNT synthesis, where the current was relatively stable at ~ 16.5 mA before jumping to ~21 mA at a later stage. It may have happened when CNTs established connection with the stacked heater through the substrate or due to the damage occurred in the poly-2 heater. The current measured between the two microheaters that indicated the electrical connection is presented in *section 6.3*.

5.6 Effect of H_2 in CNT synthesis

An etching or reducing gas (such as H_2 or NH_3) can be added to the precursor hydrocarbon gas (e.g., C_2H_2) and supporting gas (e.g., Ar) for limiting the carbon content

on the catalyst. The etching gas can reduce oxidized metal catalyst (such as Fe or Ni), which results in improved catalyst activity and increased surface mobility of the catalyst atoms [287] as the mobility of oxidized metal becomes low [288]. Cantoro et al. [159] showed the effect of reducing gases in catalyst dewetting and activation.

The CNT growth yield on CMOS-MEMS microheaters was not sufficient when Fe catalyst was used, hence, no etching gas was introduced before. As high CNT density was obtained consistently on the Ni-deposited heaters, CNT synthesis was performed with H_2 on some of the microheaters. The results of CNT growth without and with H_2 introduction on identical stacked polysilicon microheaters are shown in *Figure 5.22a* and *5.22b*, respectively. Without the etching gas (H_2), dense CNTs and CNFs can be observed



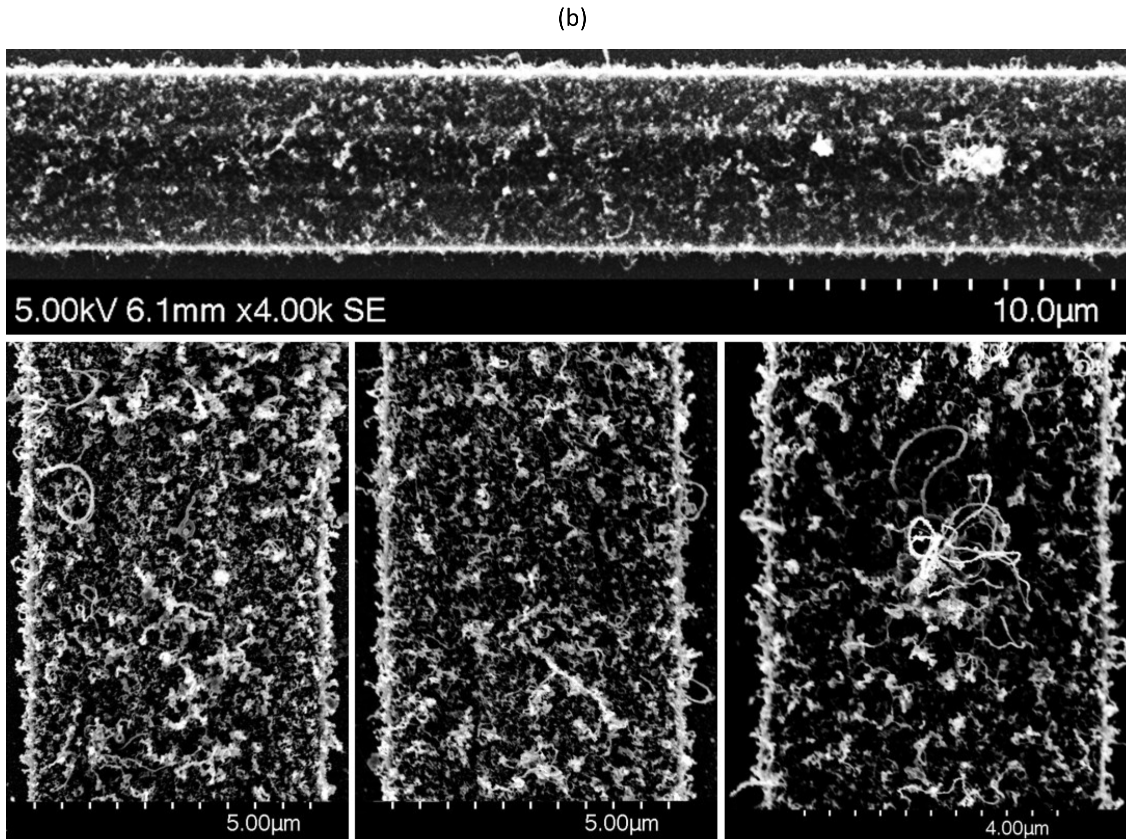


Figure 5.22: CNT synthesis on Ni catalyst (a) without and (b) with H_2 etching gas.

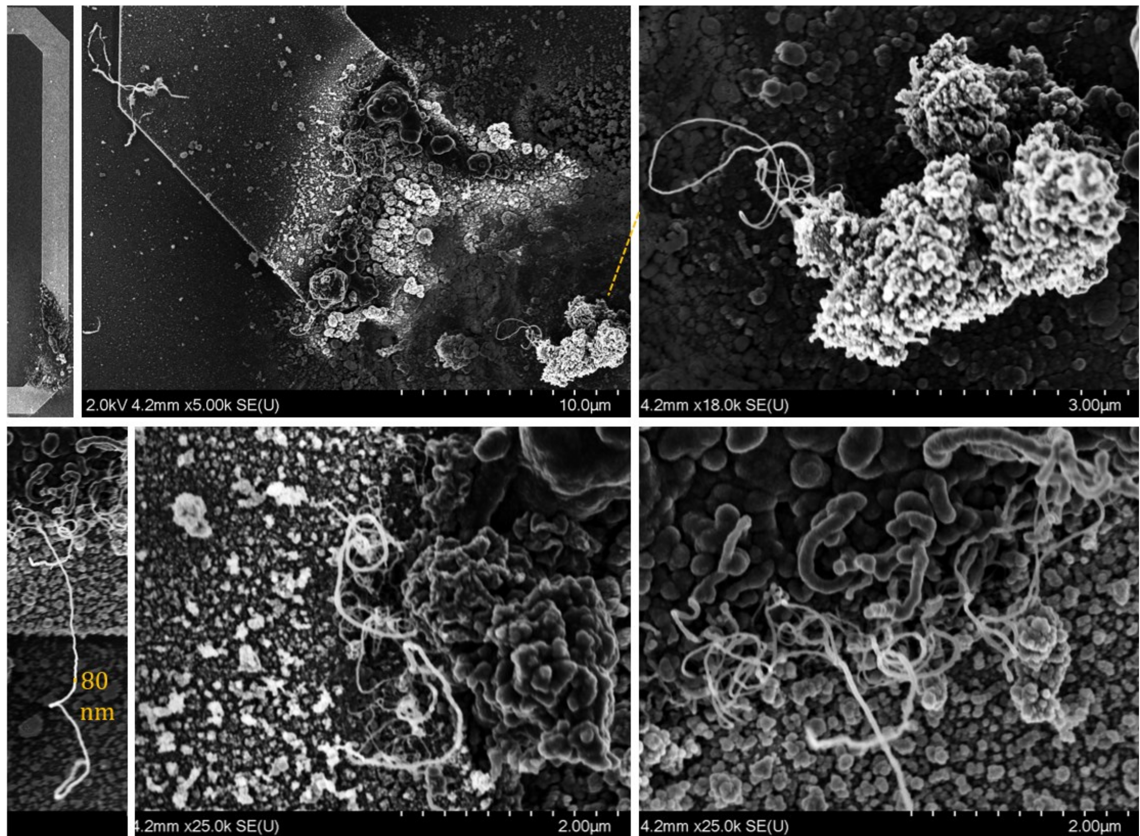
on the microheater in *Figure 5.22a*. In comparison, reduced number of CNFs are noticeable with less dense CNTs on the microheater surface (*Figure 5.22b*) when H_2 etching gas was included in the growth process.

It should be noted that the CNT growth parameters such as gas flow rates, gas ratios, chamber pressure were not optimized for growth with Ni catalyst, which is also the case for H_2 introduced CNT synthesis recipe. In this CNT growth process, 85 sccm Ar, 50 sccm C_2H_2 and 15 sccm H_2 gases were used, instead of 100 sccm Ar and 50 sccm C_2H_2 used in the previous synthesis process. It is essential to adjust the ratio between the involved gases for obtaining the optimum growth results [279,289,290]. Defects in growth can be reduced by increasing the etching gas content in the gas mixture, while excessive dosing of such gas can also result in highly defective growth [289]. Average growth rate can be increased to get longer CNTs with proper amount of H_2 introduction [290]. Therefore, a balance between the gases is needed to achieve the desired growth quality.

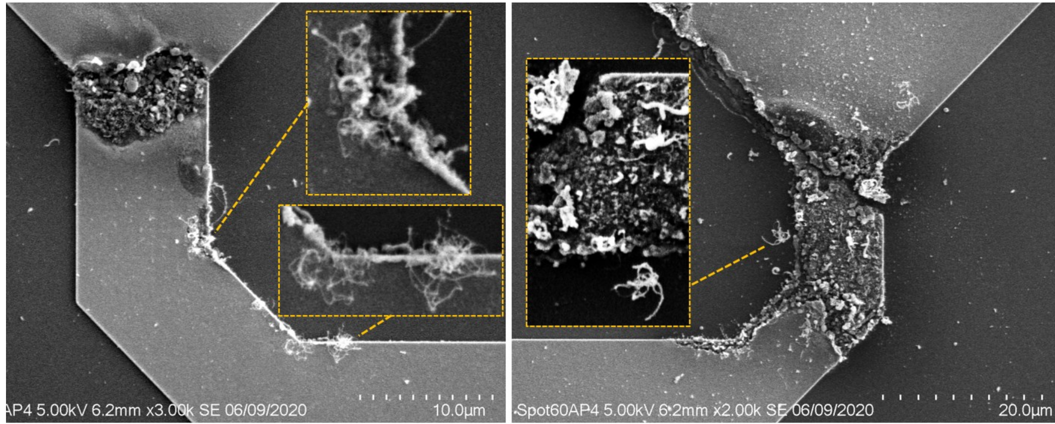
CNT synthesis with all varied parameters can be compared on the CMOS-MEMS microheater presented in *Figure 5.23*. All Fe-deposited heaters (*Figure 5.23a, 5.23b & 5.23c*) mostly have a-Cs and CNFs in local regions along with some CNTs. The growths have mostly been in visibly damaged microheater regions with estimated local high temperatures. The Ni-deposited microheaters are covered with CNTs (*Figure 5.23d & 5.23e*). The process involving H_2 etching gas provided relatively longer and less defects CNTs on average.

The heater in *Figure 5.23* is 10 µm wide. CNT synthesis on a similarly structured heater with half of its width have been presented in *Figure 5.6b*. CNT density is similar in the corresponding heaters with 2 nm Fe (*Figure 5.23b*) and 3 nm Ni (*Figure 5.23d*). It can be noticed that the inner corner edges of this heater design have better quality (for 2 nm Fe) or longer (for 3 nm Ni) CNTs then the rest of the heater surface, which can be due to high temperatures on those regions. It indicates that obtaining higher heater temperature can result in longer CNTs.

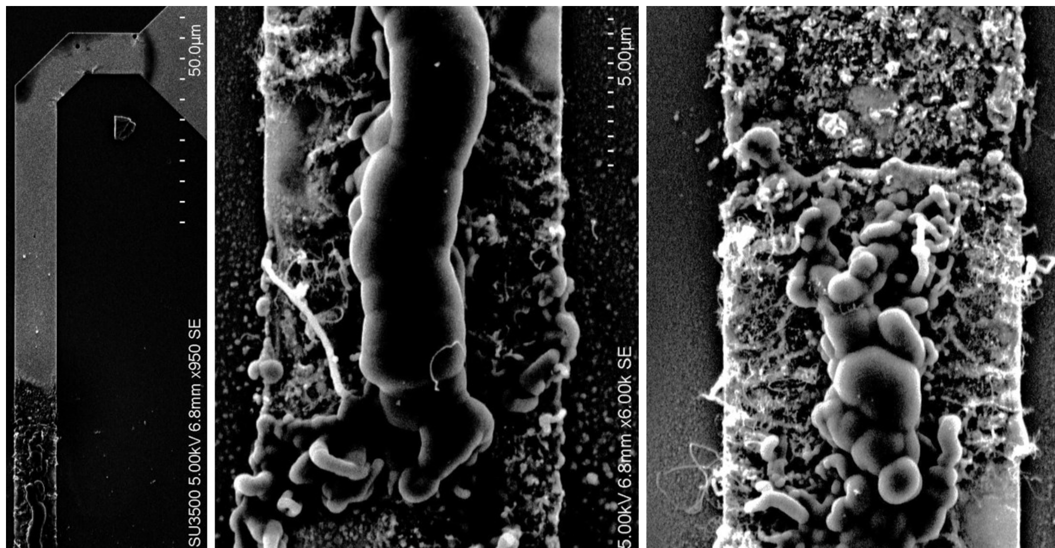
(a)



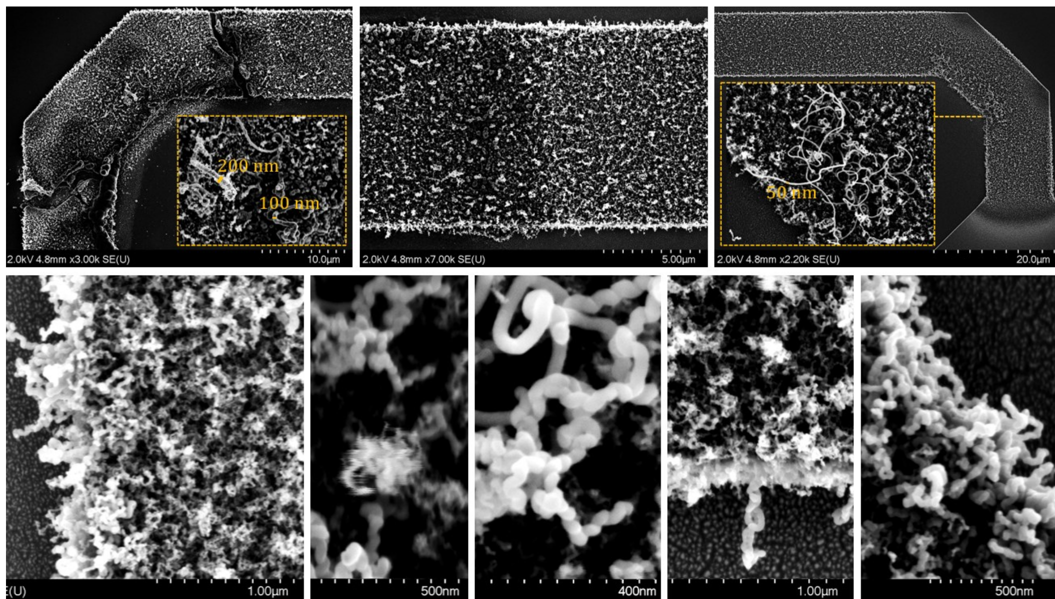
(b)



(c)



(d)



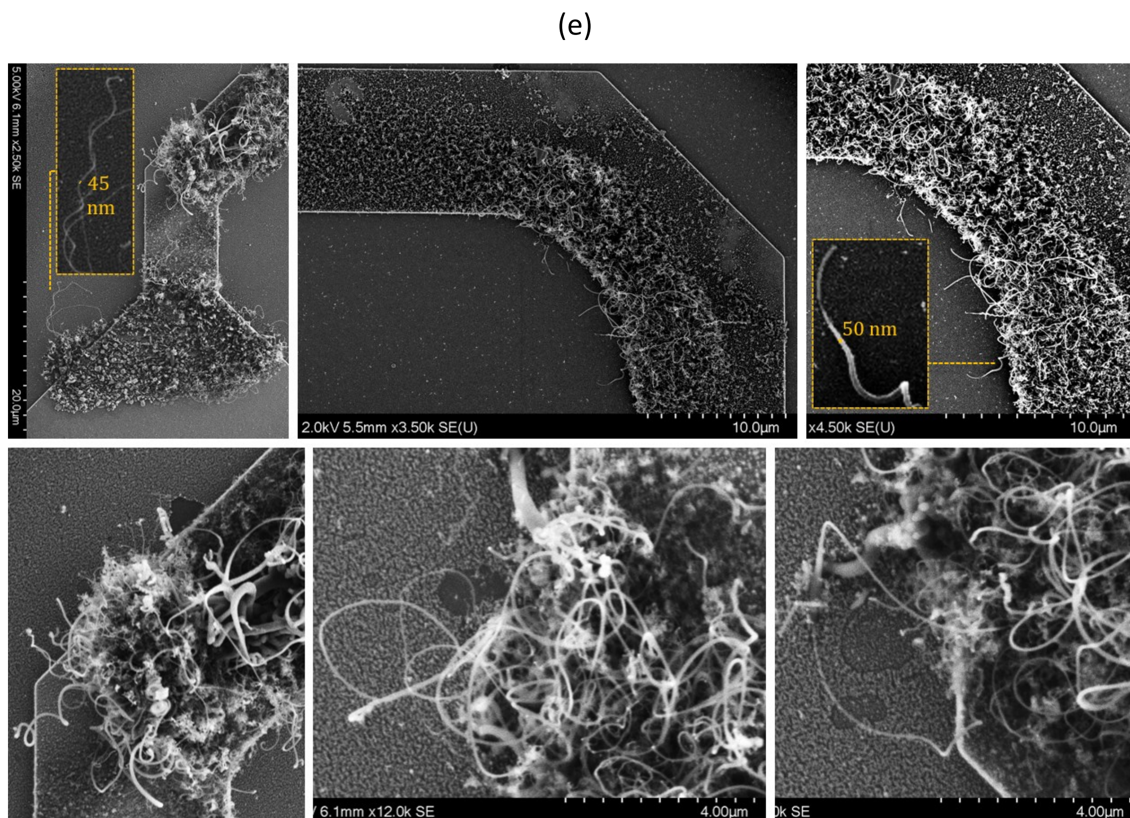
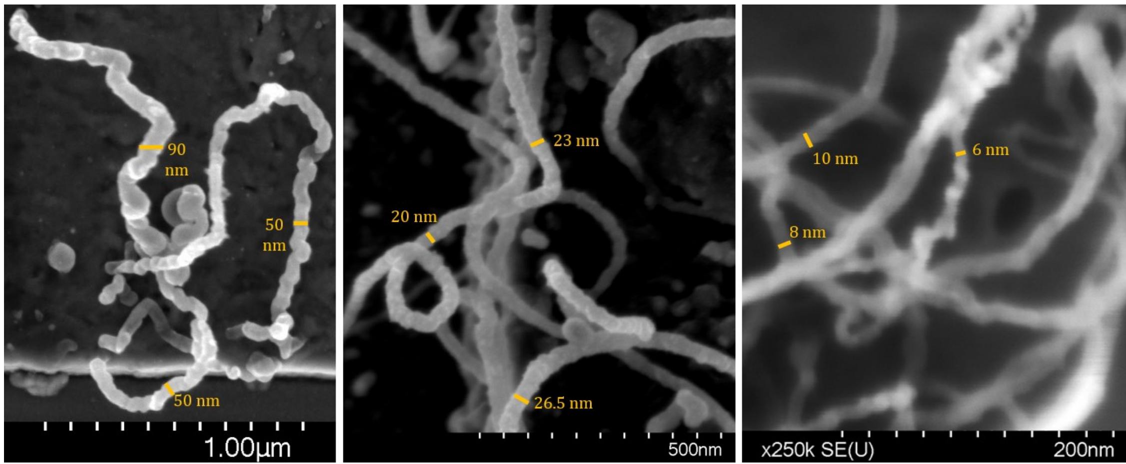


Figure 5.23: CNT synthesis on identical microheaters using (a) 3 nm Fe, (b) 2 nm Fe, (c) 2 nm Fe with partial heater suspension, (d) 3 nm Ni, and (e) 3 nm Ni with H_2 etching gas.

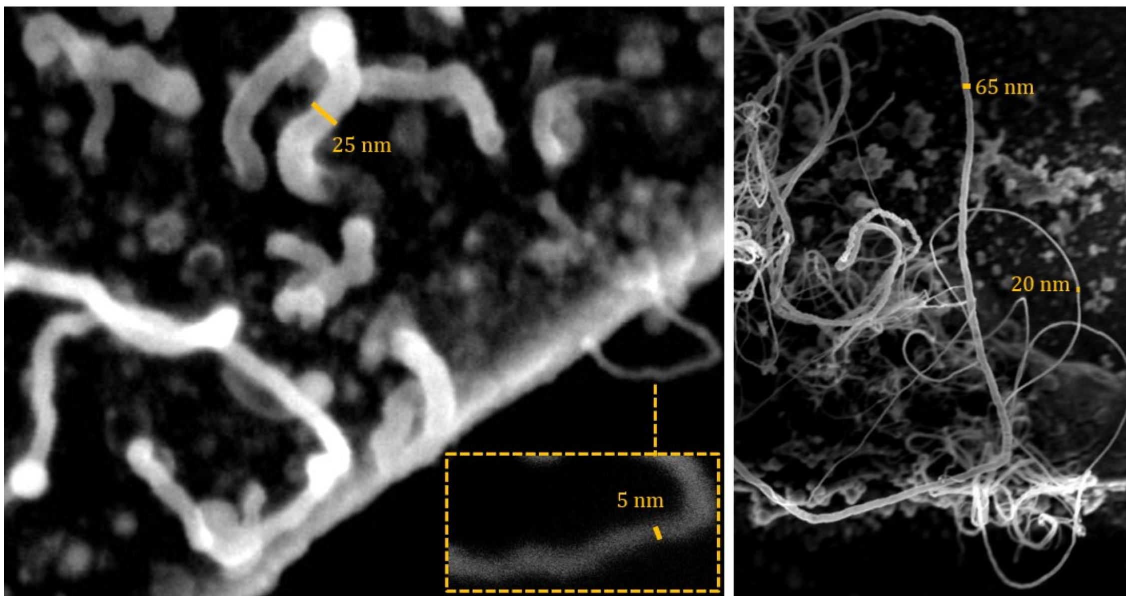
5.7 Resultant CNTs and defects

High magnification electron micrographs of the locally synthesized CNTs on CMOS-MEMS microheaters with different catalyst parameters are presented in *Figure 5.24*. Due to variation in the microheater temperatures, a wide range of CNT diameters were found even when same catalyst parameters were used. Diameter of the CNTs ranges within tens of nanometres, which indicates they can be considered multi-walled CNTs (MWCNTs) and metallic. CNTs with diameter lower than 10 nm were also found for all catalyst variations. Although SWCNTs with diameter as large as 11 nm have been grown [291], the small diameter CNTs grown around the larger CNTs on the CMOS-MEMS heaters are expected to be MWCNTs. On average Ni-based CNTs have smaller diameter than the Fe-based CNTs. For Fe catalyst, 20-50 nm CNTs are often found in most structures, while lower than 10 nm CNTs can be found in a few of them.

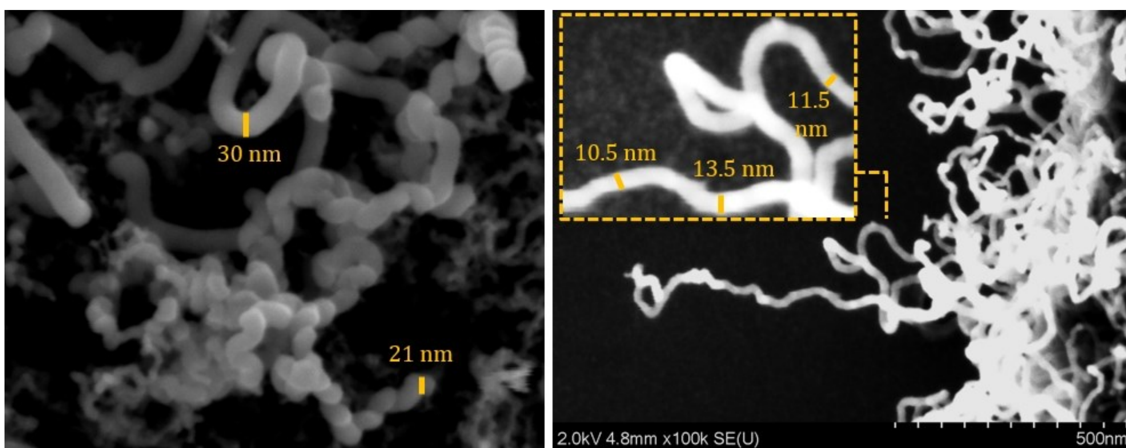
(a)



(b)



(c)



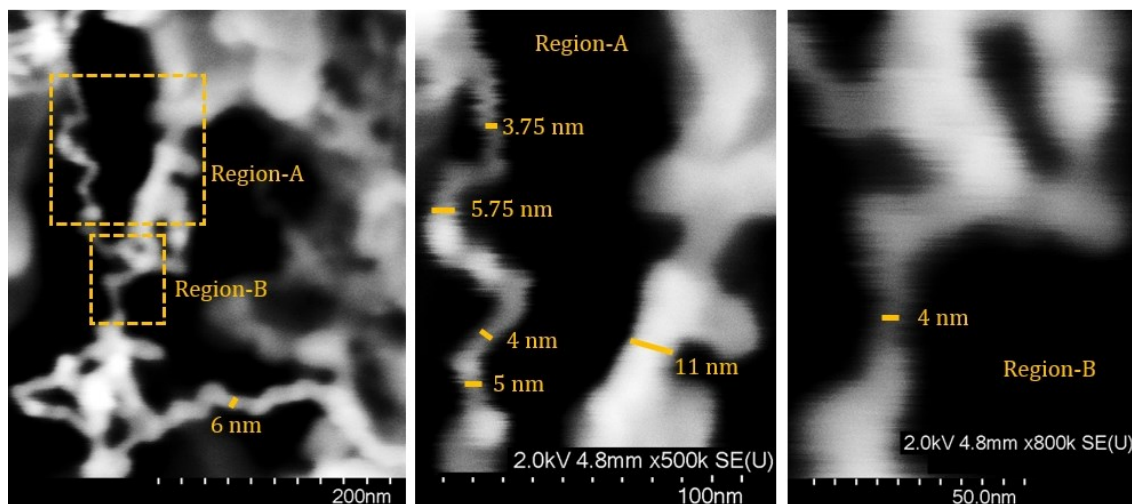


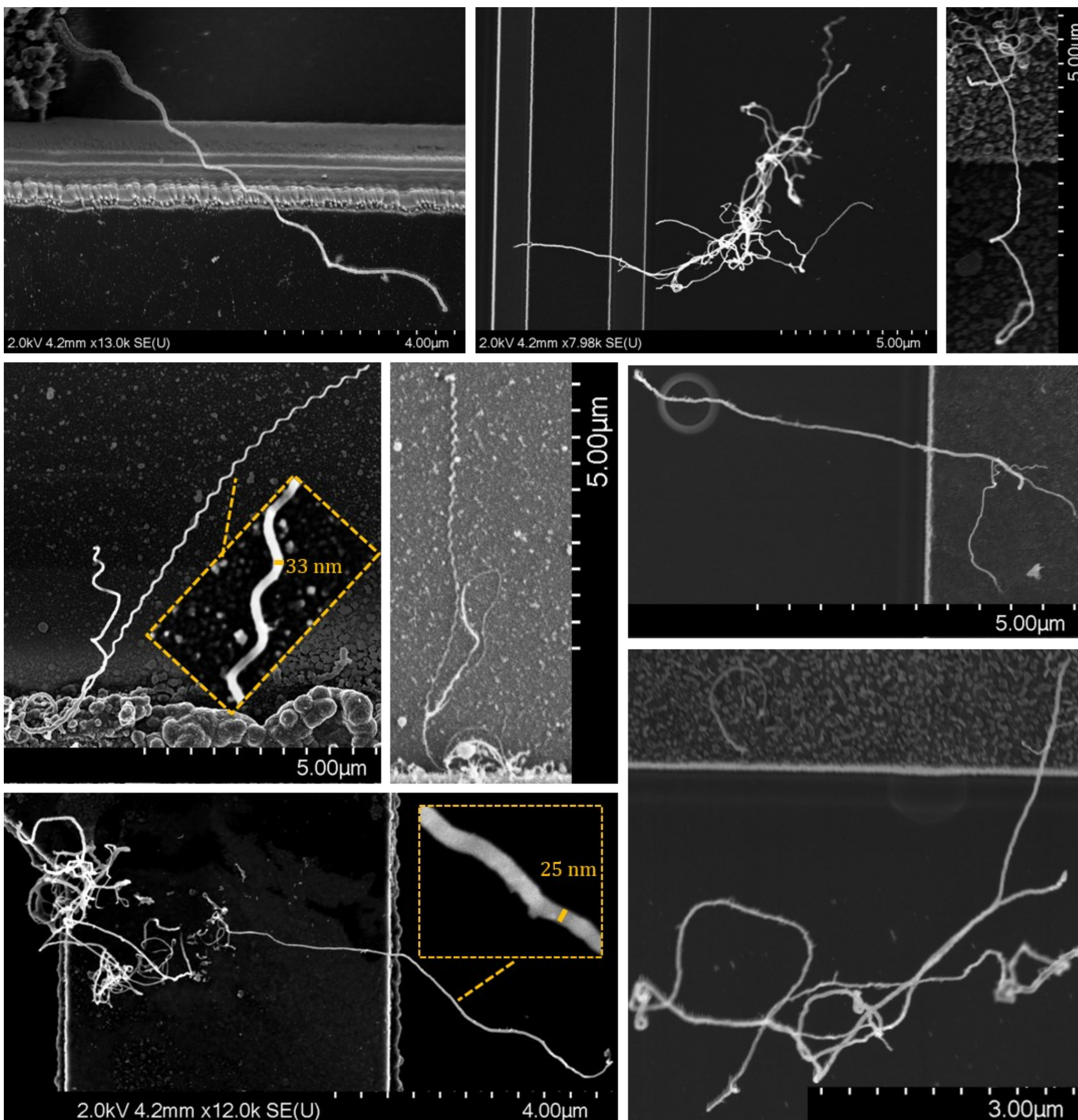
Figure 5.24: Characterization of CNTs synthesized using (a) 3 nm Fe, (b) 2 nm Fe with partial heater suspension, and (c) 3 nm Ni.

The main issue of the synthesized CNTs are their length. The CNTs were not growing long enough to bridge the gap between the electrodes. There are several reasons that can limit the length of the CNTs; in our case, the initial cause is the growth temperature. Longer CNTs have been synthesized on polysilicon MEMS heaters [89,212,228,237] at USN with similar recipes used for the CMOS-MEMS process. As the CMOS-MEMS heaters were not reaching similar temperature, CNTs were not growing longer. Growth rate can increase exponentially [292] up to a certain temperature. To increase growth rate at the obtained CMOS-MEMS heater temperatures, gas ratios need to be optimized. CNT growth can be terminated by the formation of a-C over them [281,293,294], especially when concentration of the carbon containing gas is high [293]. The a-C encapsulates the catalyst nanoparticles and thus blocks the access of precursor gas; as a result, the catalytic activity stops, and CNT growth terminates. This seems to be the reason for the short CNTs on the CMOS-MEMS heaters. The etching gas such as H_2 helps to remove a-C, but a proper balance with the hydrocarbon gas is needed to ensure optimum CNT growth, while avoiding catalyst poisoning [279,289,293]. Catalyst deactivation can mostly occur due to encapsulation by a disordered carbonaceous layer at low temperatures, while the CNT growth can be resumed if temperature is increased [281,295]. Since the CMOS-MEMS heaters are operated at near breaking voltage, increase in temperature is not an option. In the CMOS-MEMS microheaters, long-

duration (> 30 minutes) CNT synthesis process was tested, but no significant difference was found as growth terminated after a certain duration. The interaction between the synthesized CNTs and the support layer can also obstruct CNT growth [296].

The longer CNTs (> 5 µm) grown on the CMOS-MEMS heaters are shown in *Figure 5.25*. Among the long CNTs, most were grown on the 3 nm Fe catalyst layer (*Figure 5.25a*). However, the longest CNTs were found on the 3 nm Ni-deposited heaters when synthesized with H_2 (*Figure 5.25b*), which supports the issue of catalyst encapsulation. In most cases, long grown CNTs have more than 20 nm diameter.

(a)



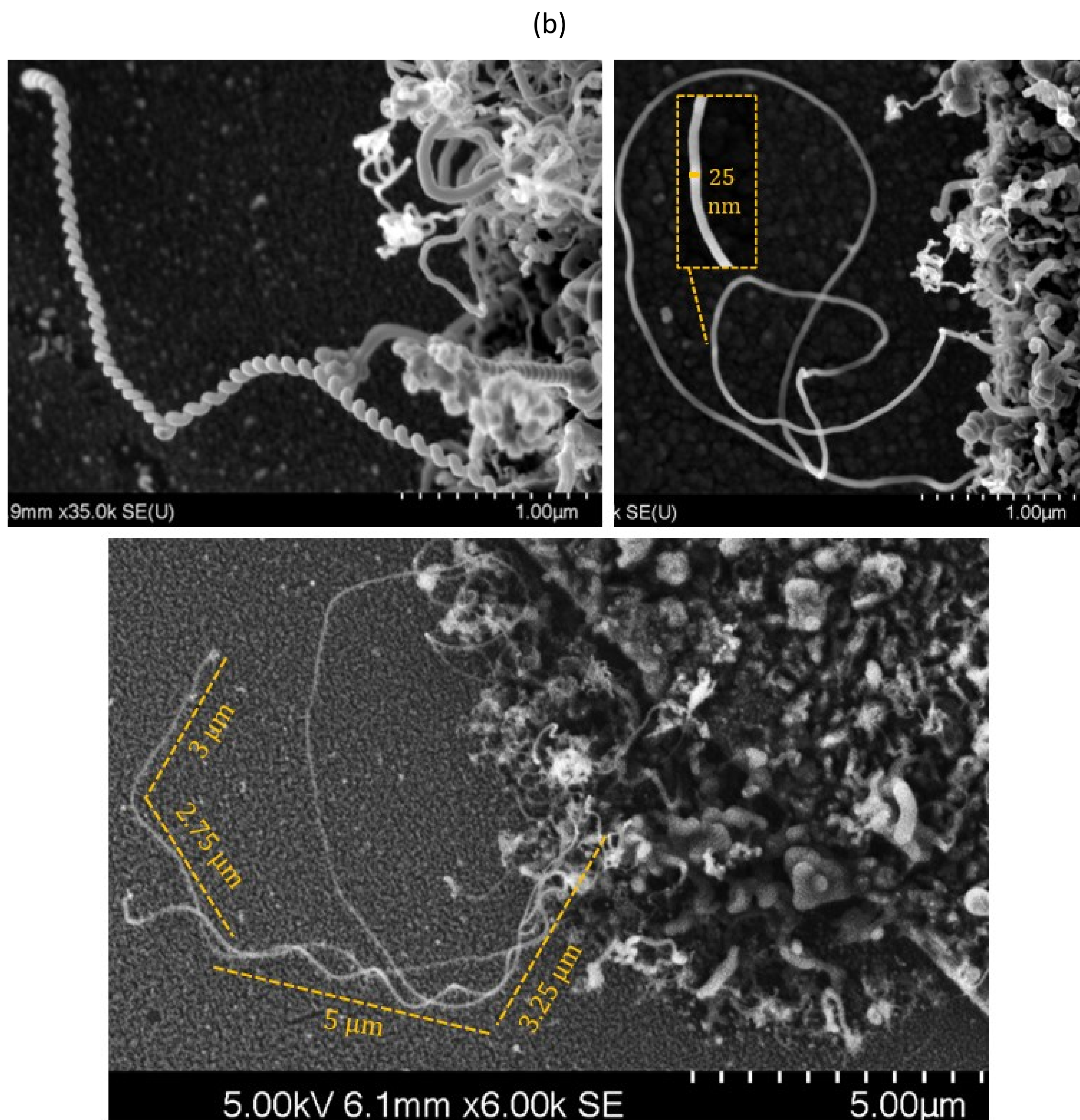
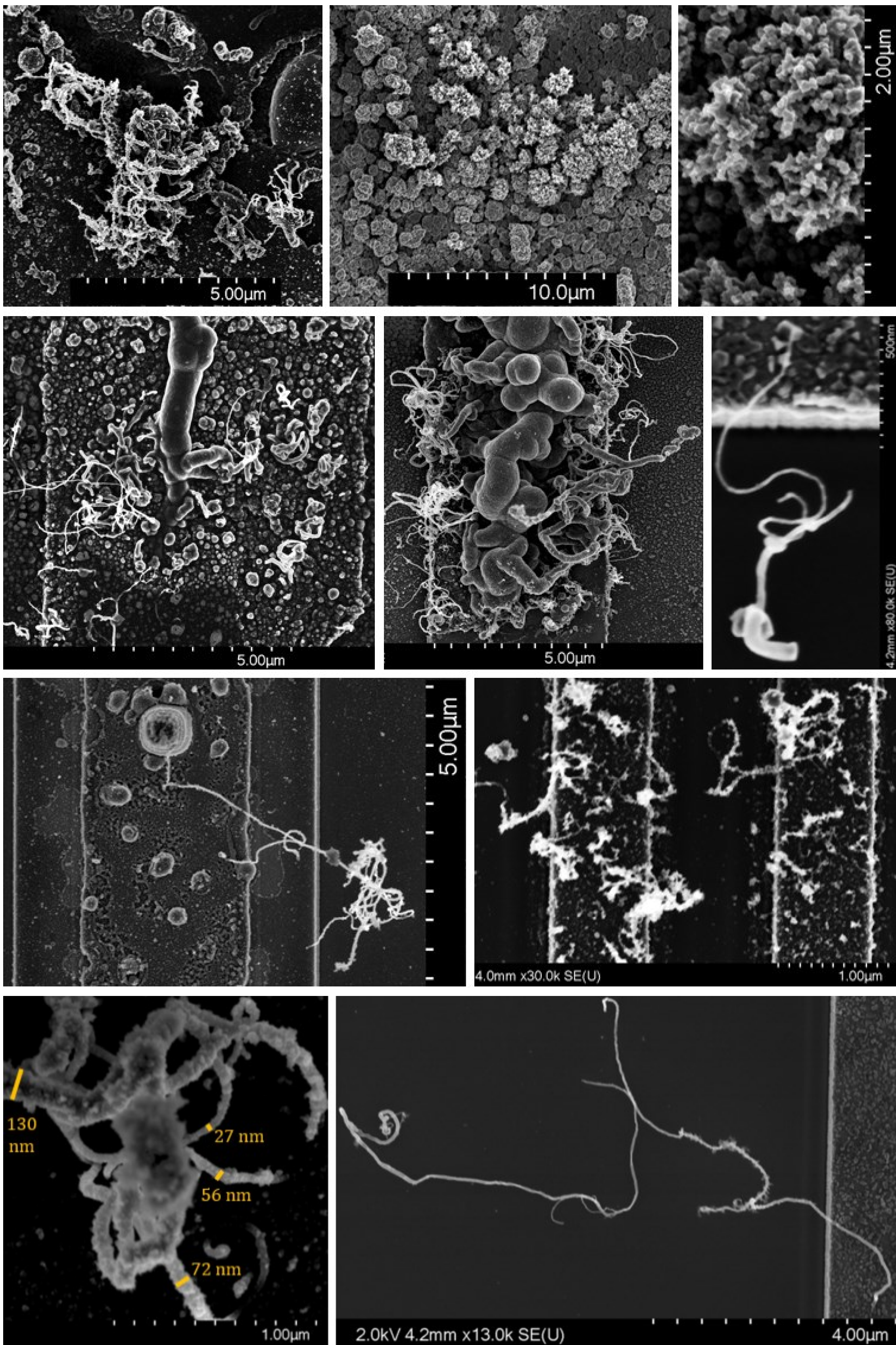
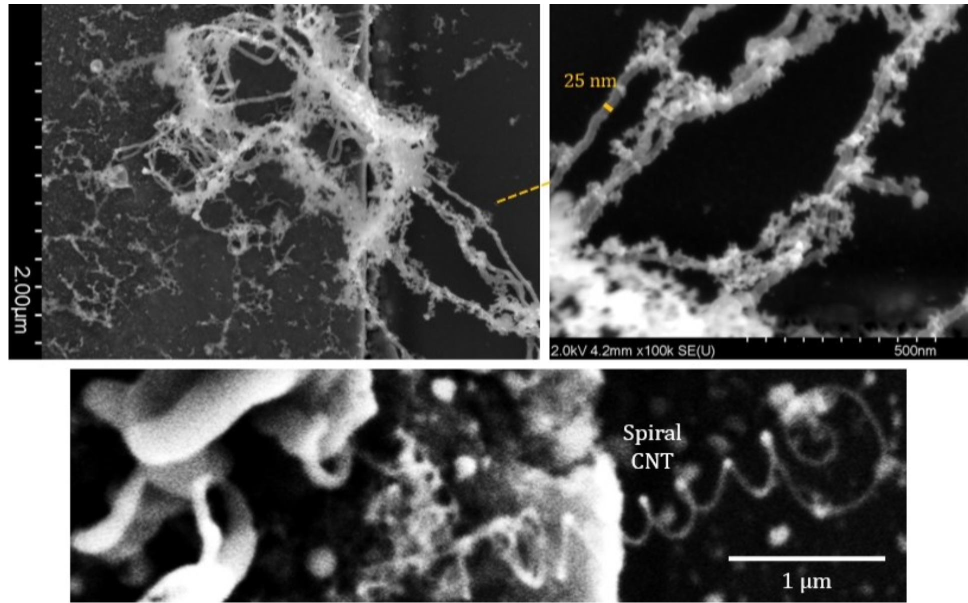


Figure 5.25: CNTs longer than 5 µm synthesized using (a) Fe and (b) Ni catalyst.

Different types of defects have been observed in the CNTs grown on the CMOS-MEMS microheaters. A variety of defects from Fe-based and Ni-based growth are presented in *Figure 5.26a* & *Figure 5.26b*. In comparison, more CNFs and defective CNTs were found in Fe-based growth. The synthesis temperature could be the main reason for the defective growths. Low temperature growth can result in larger catalyst particle sizes, which then facilitates the growth of a-C, CNFs and defective CNTs. Pre-treatment of the heaters along with an optimized synthesis recipe with the etching gas can reduce the number of defects.

(a)





(b)

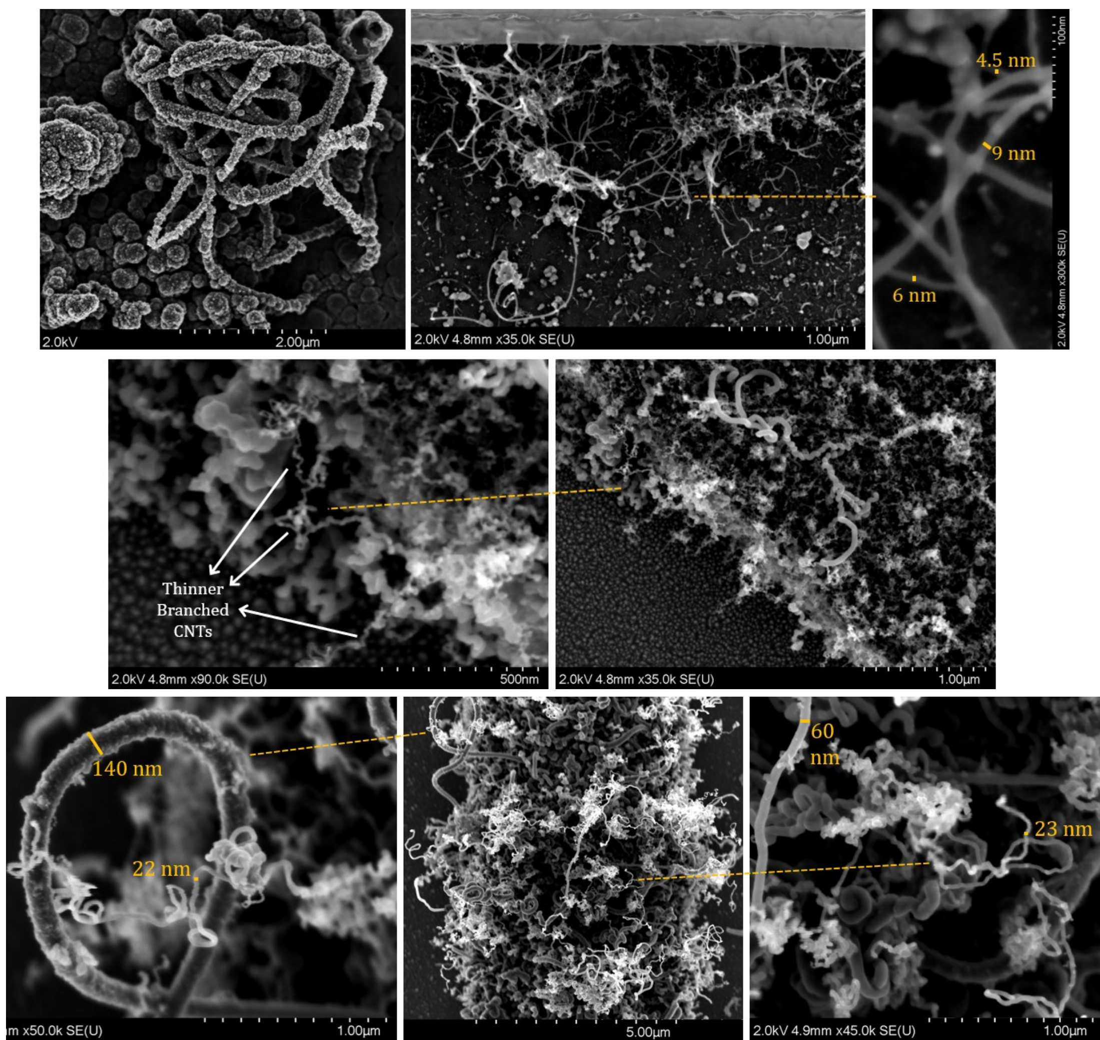


Figure 5.26: CNTs and CNFs with various defects synthesized using (a) Fe and (b) Ni catalysts.

5.8 Conclusion

CNTs were successfully synthesized on CMOS-MEMS microheaters in standard CMOS chips by local thermal CVD process. The obtained growth temperature however was much lower as the polysilicon microheaters were breaking down due to thermo-mechanical stress before reaching higher synthesis temperatures. As a result, the desired CNT growth results from the previously developed MEMS process were not successfully transferred to the CMOS process. To improve the growth in CMOS, Ni was attempted as catalyst layer, which resulted in better yield. With Ni, it was possible to grow CNTs in most polysilicon microheaters including suspended and non-suspended ones. Introduction of H_2 as an etching gas improved growth quality, the synthesized CNTs however remained short (mostly < 2 µm). Optimization of the gas ratios is a potential solution to obtain the preferred growth results.

Chapter 6

Sensing Applications

6.1 Introduction

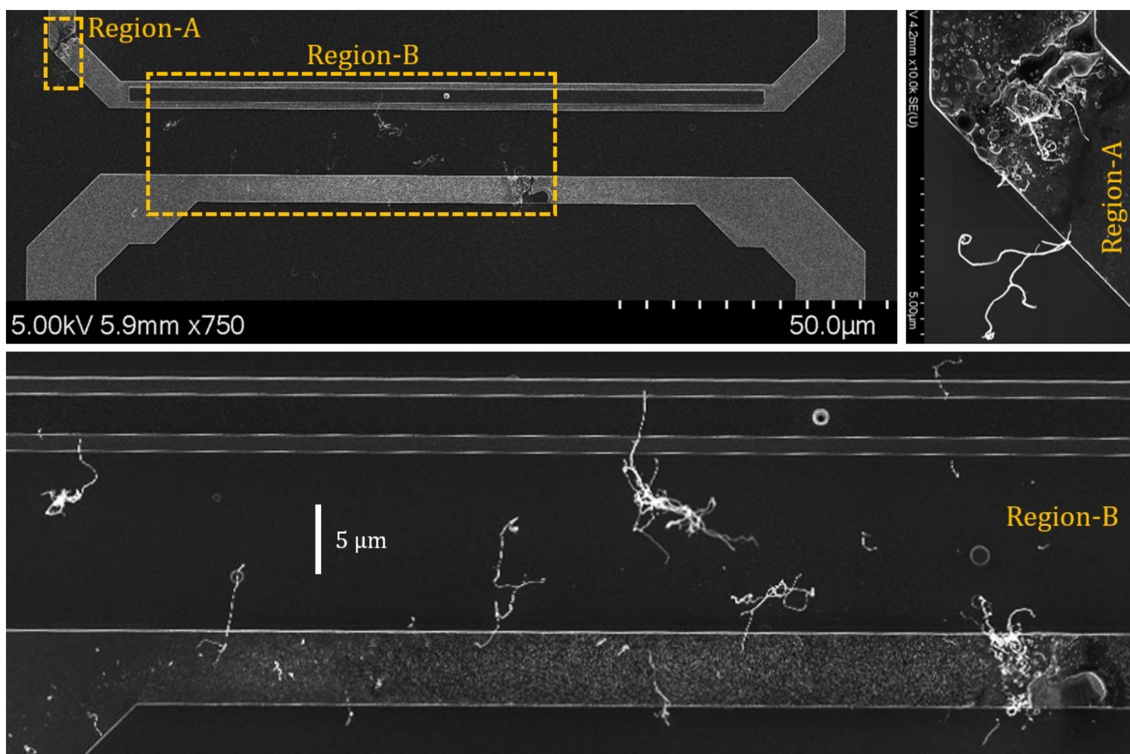
The motivation for growing carbon nanotubes in CMOS chips is to utilize the material properties of the nanomaterial in sensing applications. Numerous applications of CNT-based sensors have been demonstrated, mostly in MEMS platform. However, the sensing applications have not been shown with locally synthesized CNTs on the post-processed polysilicon microheaters of a commercial bulk CMOS technology. At USN, gas sensing have been shown with suspended CNTs between two MEMS electrodes [152,276]. CNTs need to grow horizontally for bridging the gap between the adjacent electrodes / microheaters and suspend between them. CNTs grown on the CMOS-MEMS heaters were not long enough to obtain suspended CNT connections. However, a lot of CNTs connected to the Si substrate from the CMOS-MEMS growth structures. When CNTs were grown on both adjacent microheaters, a finite current was found between the heaters on several occasions. However, inspection with SEM did not show any suspended CNT connections in those cases. Hence, it is interpreted that the synthesized CNTs established the electrical connections through the silicon substrate. Although I-V curve can be generated between the adjacent microheaters, most of these connections did not provide proper sensing response. A few of them showed moderate response, while one of the connections provided good response for both gas and pressure. The results from this chapter will be included in *Article 9 (in preparation)* and in a planned publication.

6.2 CNT growth towards adjacent heater

A local electric field was generated between the adjacent microheaters during the CNT synthesis process by supplying voltage across the heaters; the voltage value depended on the distance between them. The voltage was regulated based on the operating microheater voltage during CNT synthesis. In most cases, the electric field value was

kept within 1 V/µm. Although the intension was to direct the CNTs from the growth location towards the adjacent heater, the short CNTs may not have been impacted by the electric field. CNT connections have been electrically detected in several instances during the synthesis process, which were likely established through the Si substrate. As CNTs were grown on both adjacent microheaters, a good connection between the CNT and heaters was ensured; this can be a concern for suspended CNT connections, where CNTs grown from one microheater make relatively fragile contact with the adjacent electrode.

Figure 6.1 shows CNTs grown in the direction of adjacent heater, where the CNTs came closest towards each other. Relatively long CNTs were grown in both of these microheaters. The synthesized CNTs from such adjacent heaters make a connection through the conducting Si substrate. *Figure 6.2* shows an exceptional case when CNTs connected to the adjacent heater through a broken poly-2 beam. The connection that provided the best sensing response has been presented in *Figure 5.20.* Among the Ni-based growths, the heaters from *Figure 5.5* & *Figure 5.6a* had significant number of CNTs connected to the Si substrate that established a connection between them.



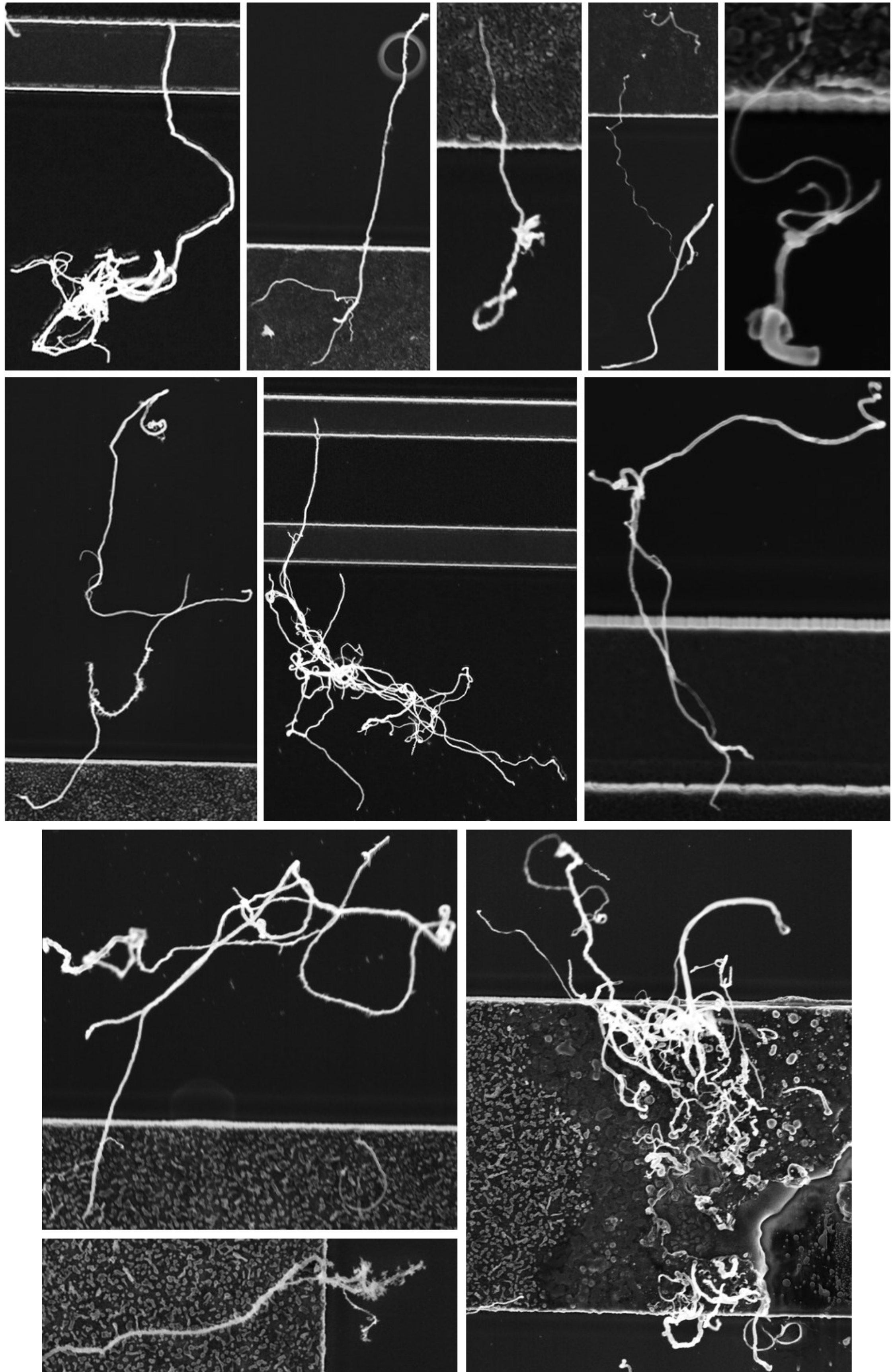


Figure 6.1: CNTs on two adjacent microheaters growing towards one another.

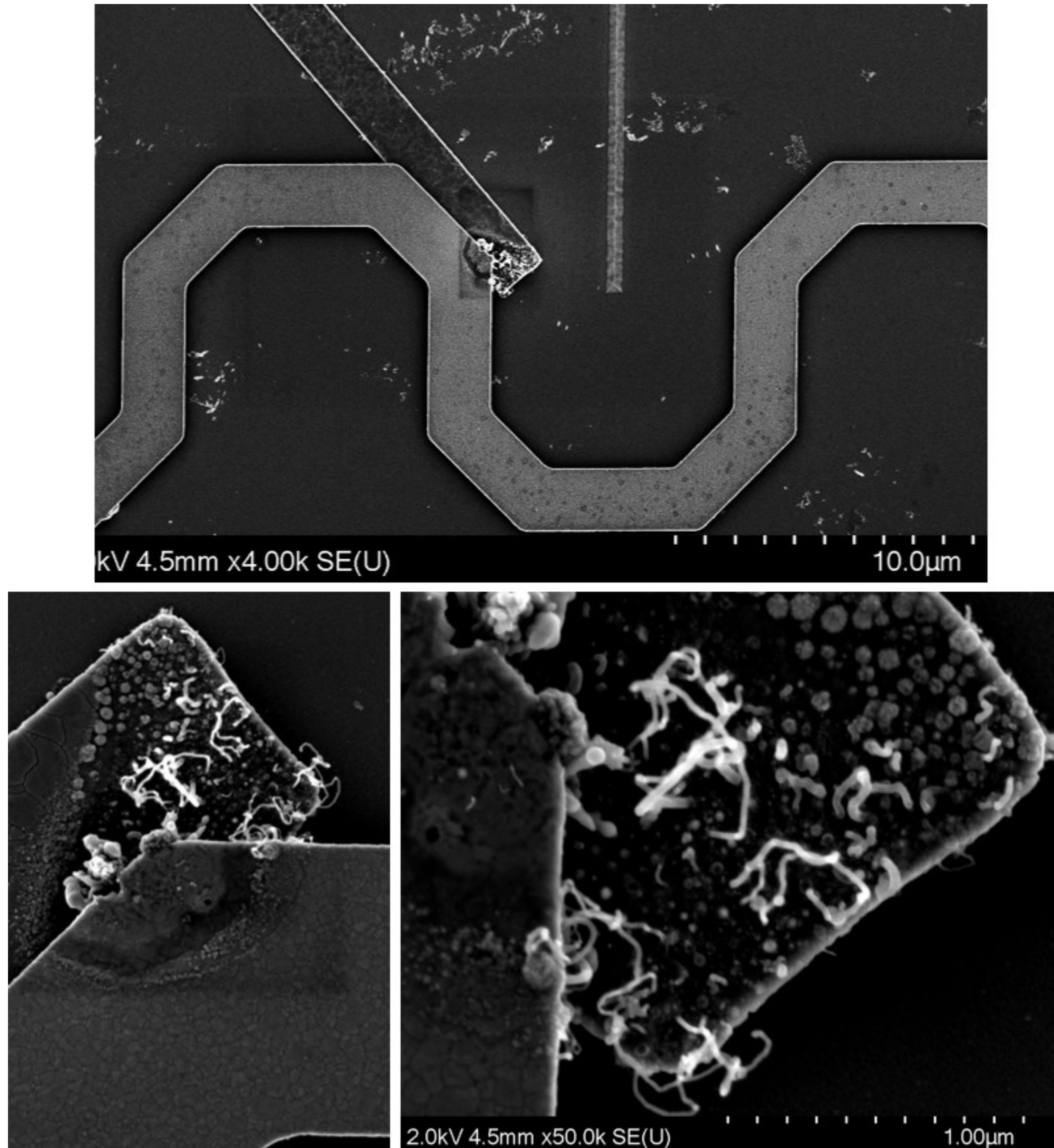
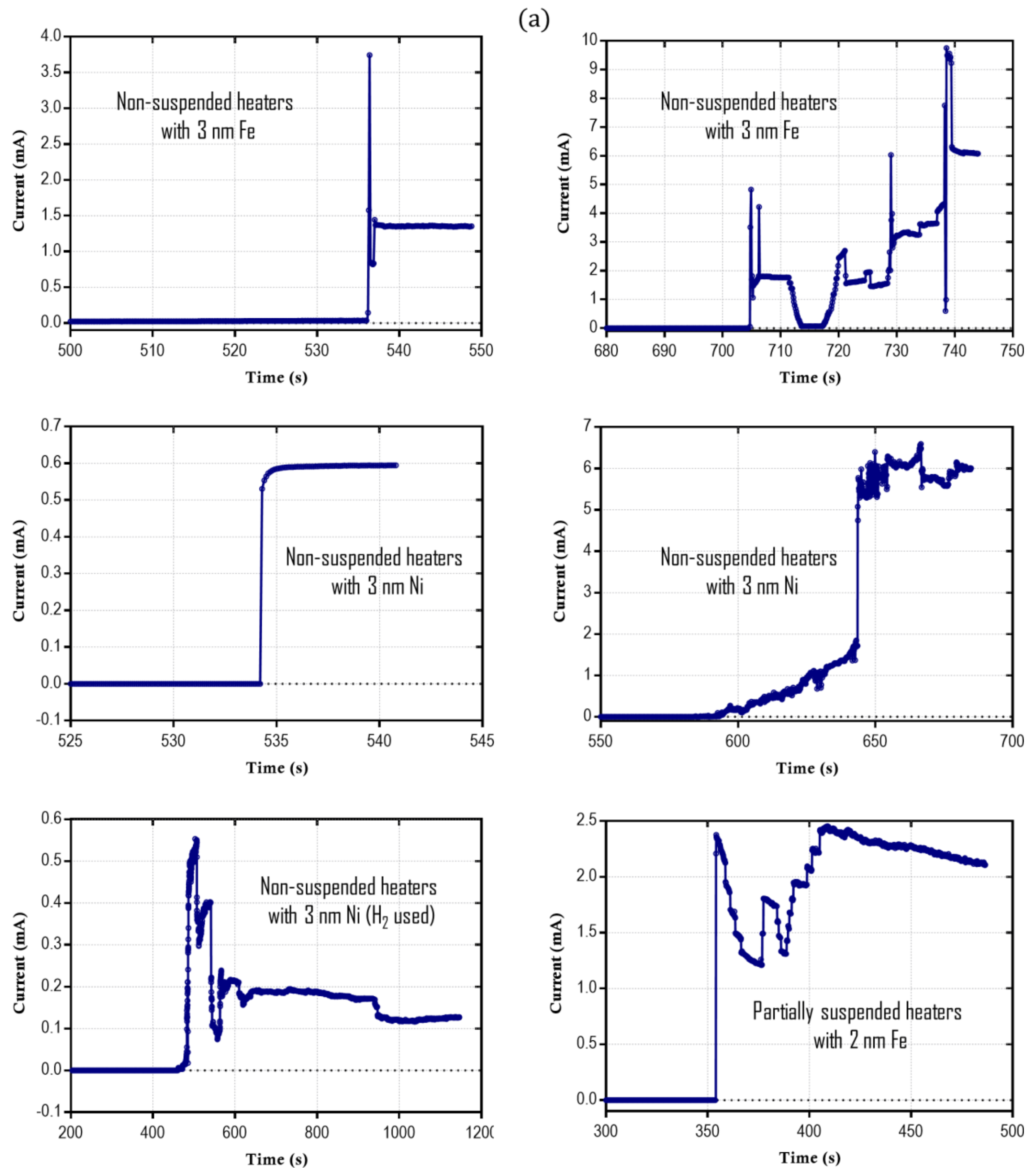


Figure 6.2: CNTs from a poly-1 heater connects through a broken poly-2 beam from the adjacent heater.

6.3 CNT connections and I-V curves

The connection between two adjacent heaters were monitored electrically during the CNT growth process. The voltage source used for generating electric field between the adjacent heaters also serves the purpose of detecting the connections. A significant increase in current can be detected when some locally grown CNTs establish a connection between the two microelectrodes. This jump in current from the previous open circuit state are shown in *Figure 6.3* for some microheaters with different catalysts. Current can also reduce if some connections get broken.

The bias voltage was varied with the increase in heater voltage to keep the local electric field value near 1 V/µm. Depending on the CNT connections, a range of current increase were found, mostly within 0.5 mA to 10 mA. The applied voltage across them also differed depending on the microheater designs, spacing between the adjacent heaters and growth conditions. Maximum current jump was seen in the most responsive sensor (*Figure 6.3b*).



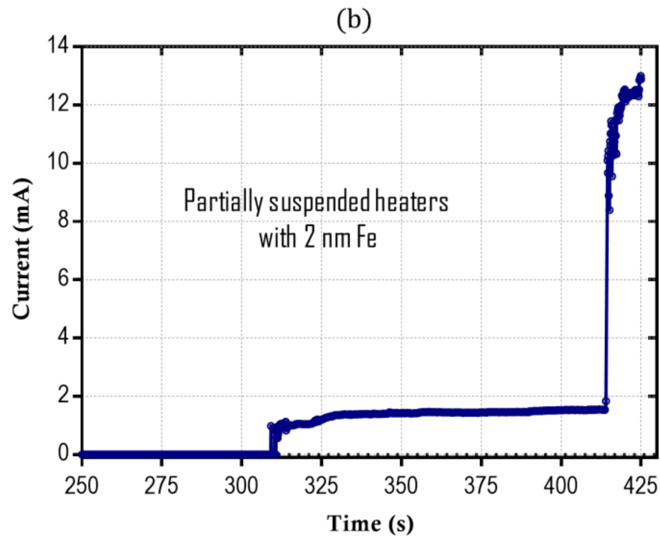
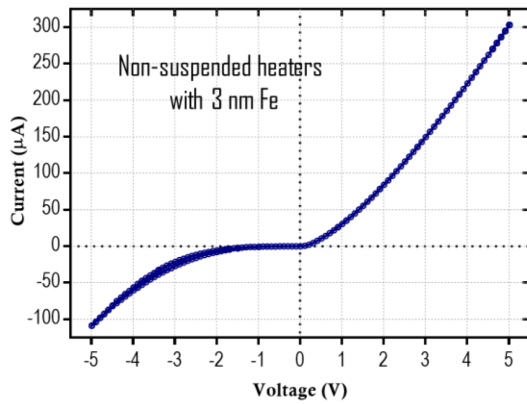


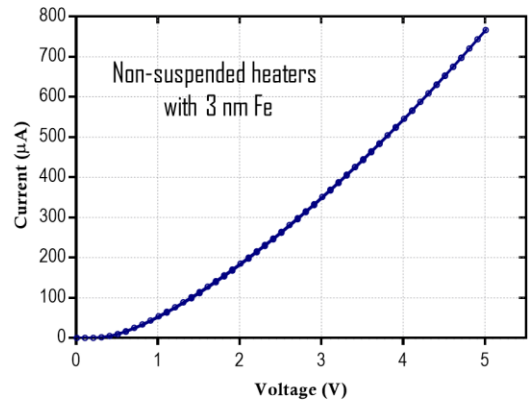
Figure 6.3: Electrical detection of established connections between two adjacent heaters through synthesized CNTs. (a) Heaters with growth variations; (b) Connection of the most responsive sensor.

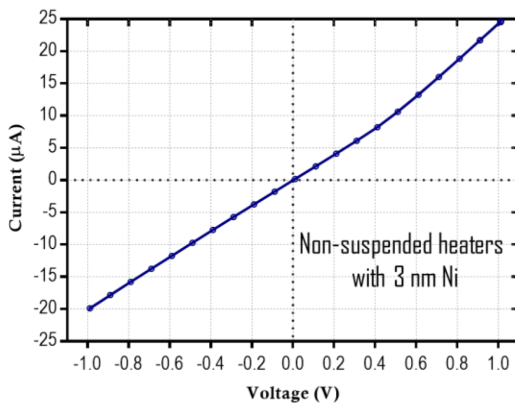
Electrical response of different microheaters with CNT connected network is shown in *Figure 6.4*. Near-ohmic behaviour can be seen for most of them within the operated range of voltage, while a few showed rectifying characteristics. Results of the I-V measurements have similarities with the Si-CNT-Si systems characterized on MEMS heaters [237]. The resistance of the connected networks has wide variations due to the number of connected CNTs and the actual nature of the connection. In most cases, the value ranges from 20 kΩ to 50 kΩ, while network resistance as low as ~5 kΩ and as high as ~2 MΩ was also found in the linear region. CNT-Si interface have high contact resistance that can dominate the total network resistance. For locally grown CNTs suspended on MEMS electrodes, a total network resistance of 400 kΩ was found [276]. However, a direct comparison cannot be made here, as the non-suspended CNTs on the CMOS-MEMS heaters formed a more complex network through the Si substrate.

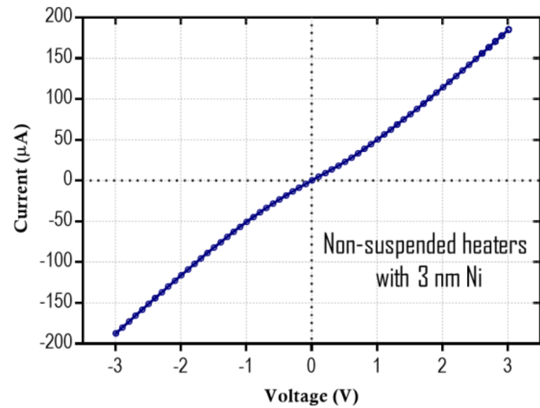
On average, higher number of connections were established in the heaters with Ni-deposited catalyst, which can be due to higher CNT growth yield obtained in Ni-based heaters. Since the distance from the polysilicon heater surface to the silicon substrate is small (~ 500 nm), the short synthesized CNTs are able to touch the substate. Hence, a higher synthesis yield results in higher possibility of establishing such a connection.

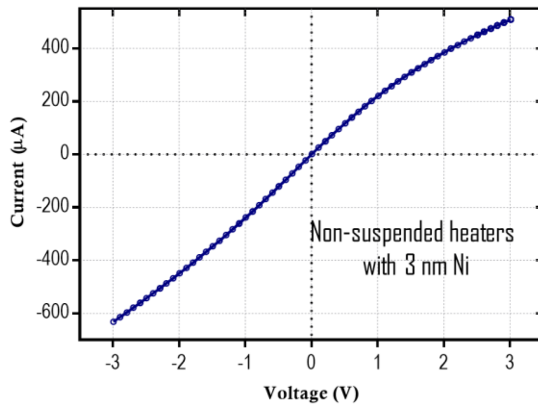
(a)

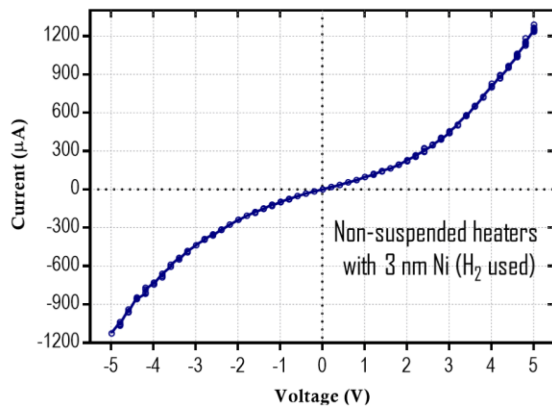


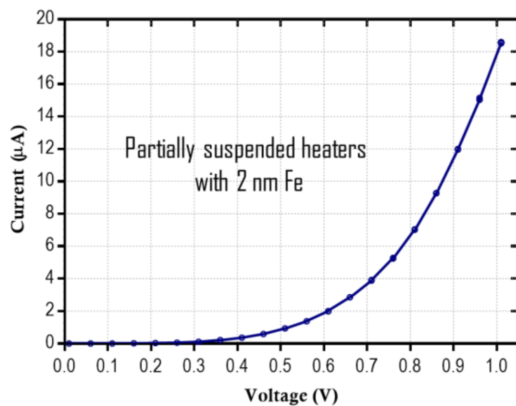


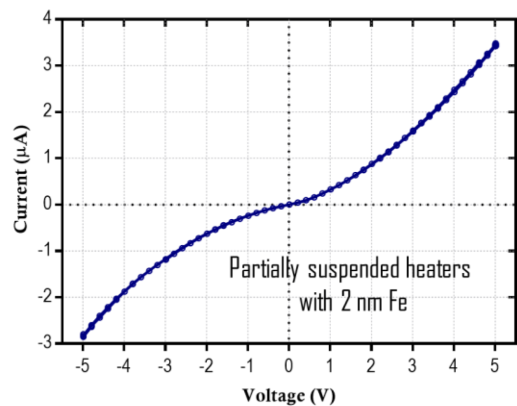












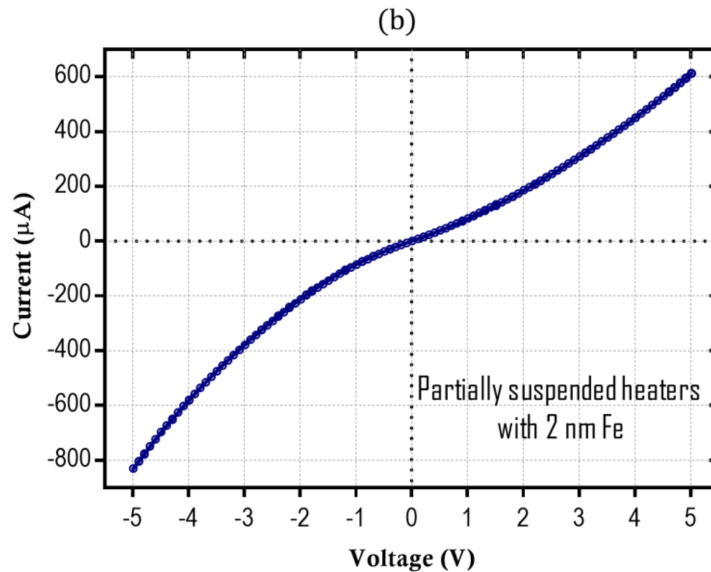


Figure 6.4: Electrical response of some connected network. (a) Established connection on various microheaters with variations in CNT growth; (b) I-V curve of the most responsive sensor.

6.4 Gas sensing

Gas responses of the CNT-based sensors were investigated in a smaller dedicated chamber (~650 cm^3) which is partially integrated with the main CVD chamber as shown in *Figure 5.2*. Pristine CNTs have a limited sensitivity and selectivity to gases and analytes such as NH_3, NO_2, and CO_2 at room temperature [152,297]. Adsorption of gas molecules on CNT surface leads to transfer of electrons between the materials, which results in a change of CNT resistance [298,299]. The electrical characteristics of the CNTs can be monitored to detect the gas response. CO_2 gas sensing with CNTs have been reported in [152,300]. Sensitivity of CNTs can be further enhanced by functionalizing them. Several functional materials such as Pd, Pt, ZnO, TiO_2 etc can be deposited on the CNTs. Functionalization of CNTs not only enhance sensitivity, but also improve selectivity and recovery of the CNTs in a gas sensor. The performed gas sensing for the CNTs on the CMOS-MEMS electrodes are, however, without any functionalization. CO_2 was chosen as the main target gas; a CO_2 detector can be utilized for different applications such as monitoring the degradation of perishable food [148,152] and breath analysis [97,140,149].

Figure 6.5 shows the sensor response to a mixture of Ar and CO_2, where the concentration of the gases was varied while keeping the total chamber pressure constant. The sensor was operated at 0.5 V bias voltage; the I-V characteristics of the sensor in *Figure 6.4b* shows linear behaviour in that region. A relatively significant change in current (~500 nA) can be seen when the gases were introduced from a vacuum condition. The current further dropped by ~100 nA when the CO_2 concentration was increased. For low-concentration CO_2 exposure, the sensor showed consistent recovery within relative short duration (~2 minutes).

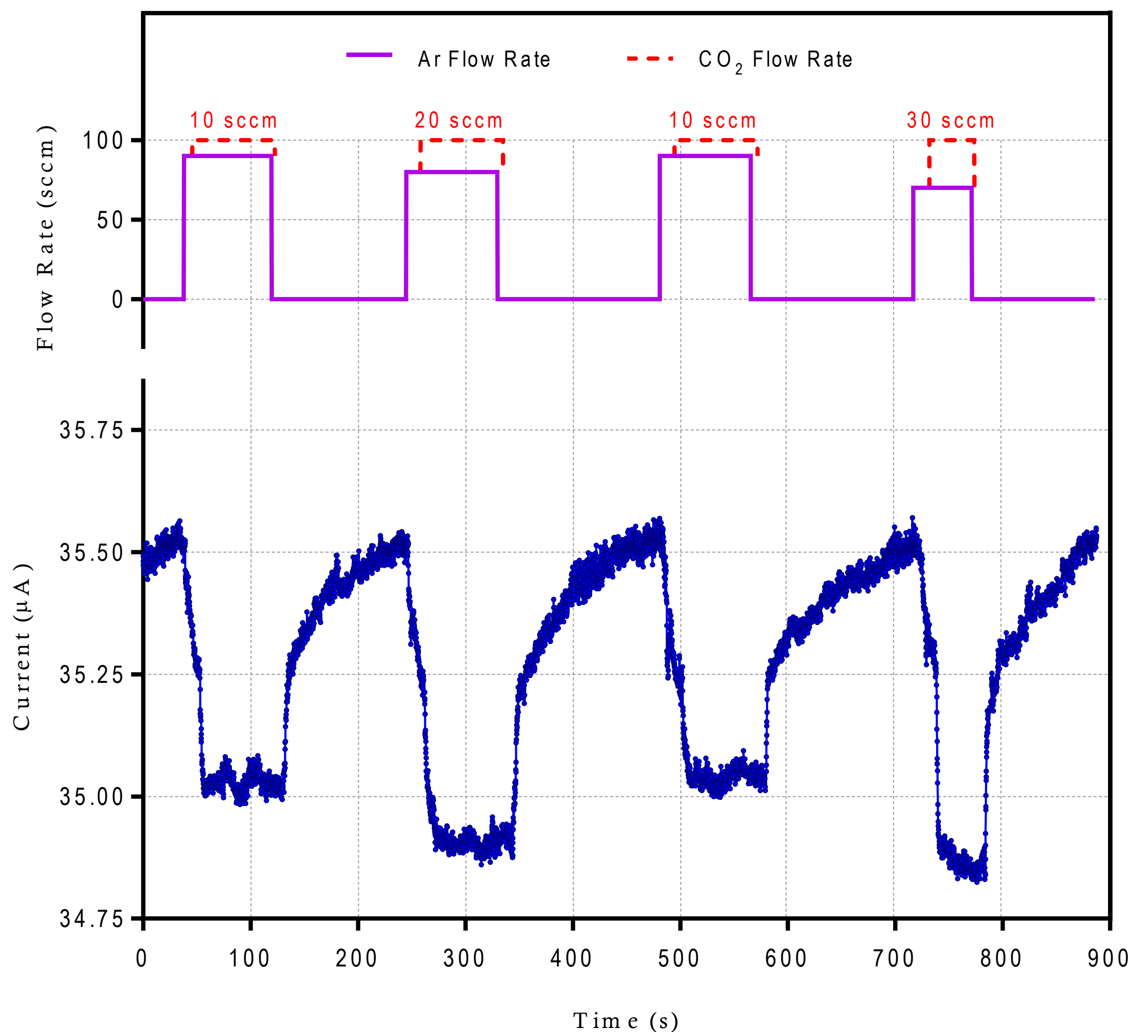


Figure 6.5: Sensor response to Ar and CO_2 mixture with varied concentration under constant pressure.

Although variation in the sensor response can be seen when CO_2 concentration is varied, the performed tests were aimed for qualitative rather than quantitative analysis. The

result is comparable to similar gas detection demonstrated in MEMS-CNT integrated sensors [152,276]. Apart from chemical response due to the interaction with the CO_2 gas molecules, the device also showed some sensitivity towards pressure. *Figure 6.5* shows some indication of the sensor response to pressure change when Ar was introduced a few tens of seconds earlier than CO_2; a variation in sensor response time is noticeable. The response time for the initial change in pressure caused by Ar introduction is higher than the sharp drop in current caused by CO_2 introduction; more evidence of this can be found in the follow-up results.

The measured response of the device for air and mixture of CO_2 with air is shown in *Figure 6.6*, where the chamber pressure was also varied. Filling the chamber with only air resulted in a rapid current drop (> 1000 nA). The sensor did not fully recover within

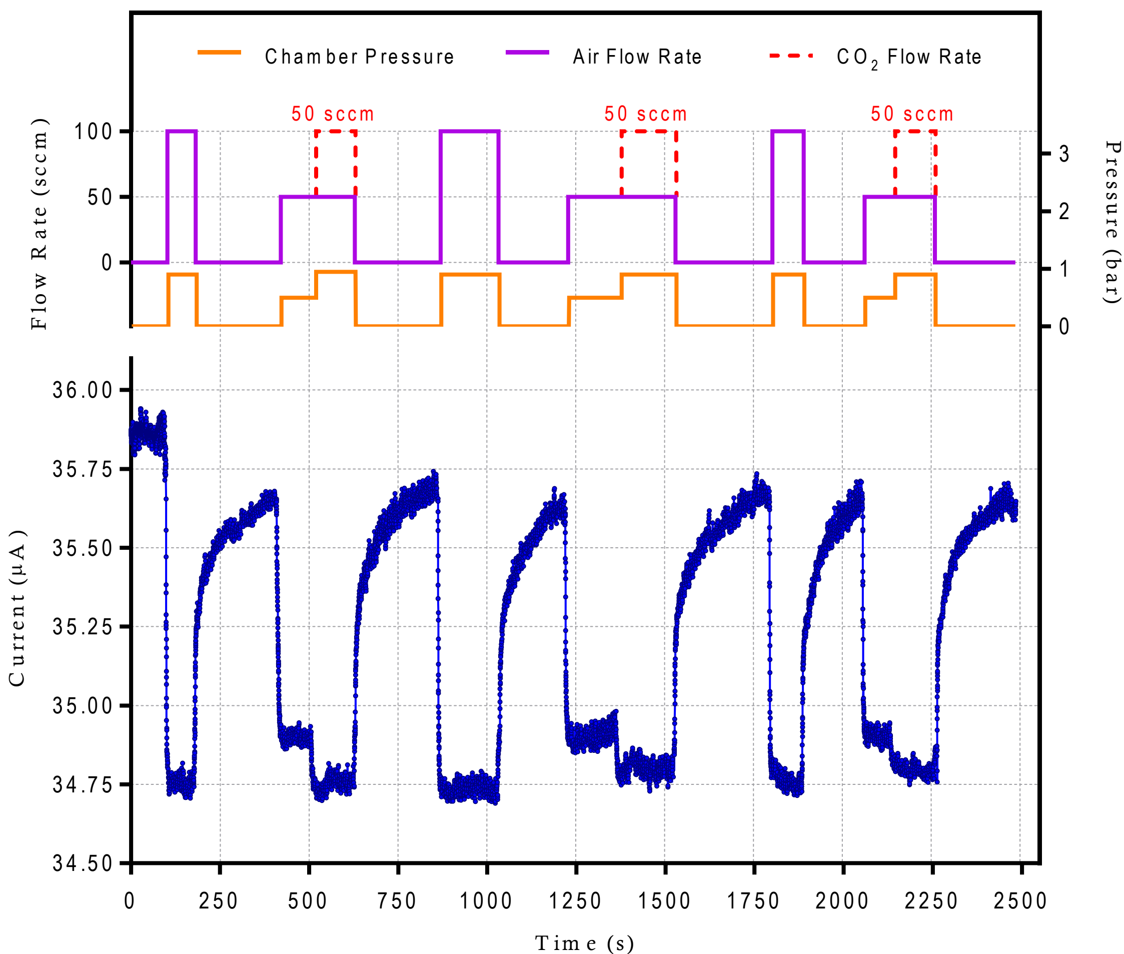


Figure 6.6: Sensor response to air, mixture of air & CO_2 along with change in chamber pressure.

the provided duration of ~4 minutes before the gas exposure was repeated. Adding pure CO_2 in an already existing air environment did not show significant current drop; the surface of the CNTs could already be fully adsorbed by the CO_2 in air molecules. Hence, the minor drop in current could be due to the increase in pressure to ~1 bar upon adding CO_2 from the state of 0.5 bar air. Response to different pressure level by Ar exposure has been evaluated in *section 6.5*. The overall response of the device was consistent over repeated cycles, including sensor recovery within the given period.

The sensor was also tested with pure air and CO_2 separately under same chamber pressure *(Figure 6.7)*. Although the sensor did not fully recover within the given time before introducing CO_2, a current difference of ~200 nA was found between the gases. Full recovery of the sensing element was achieved after ~8 minutes in vacuum. The required recovery time of the sensor depended on the CO_2 concentration and how long the CNTs were exposed to the gas. Heating the CNTs can be effective to improve the recovery time [301], which could be done by joule heating the connected CNTs.

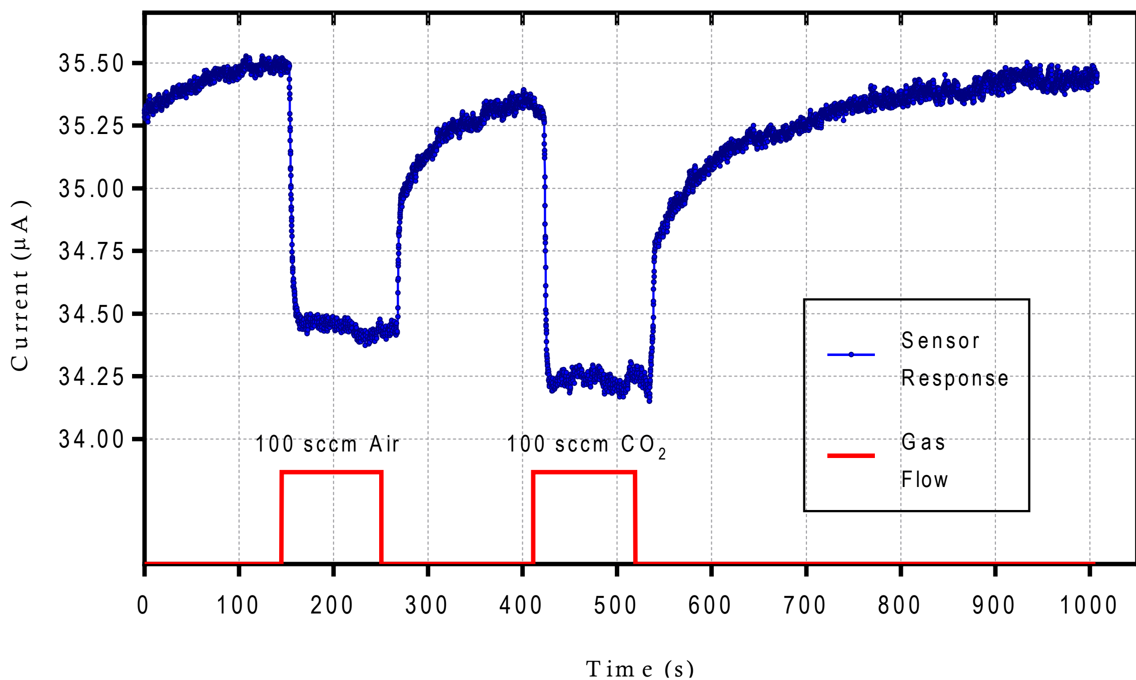
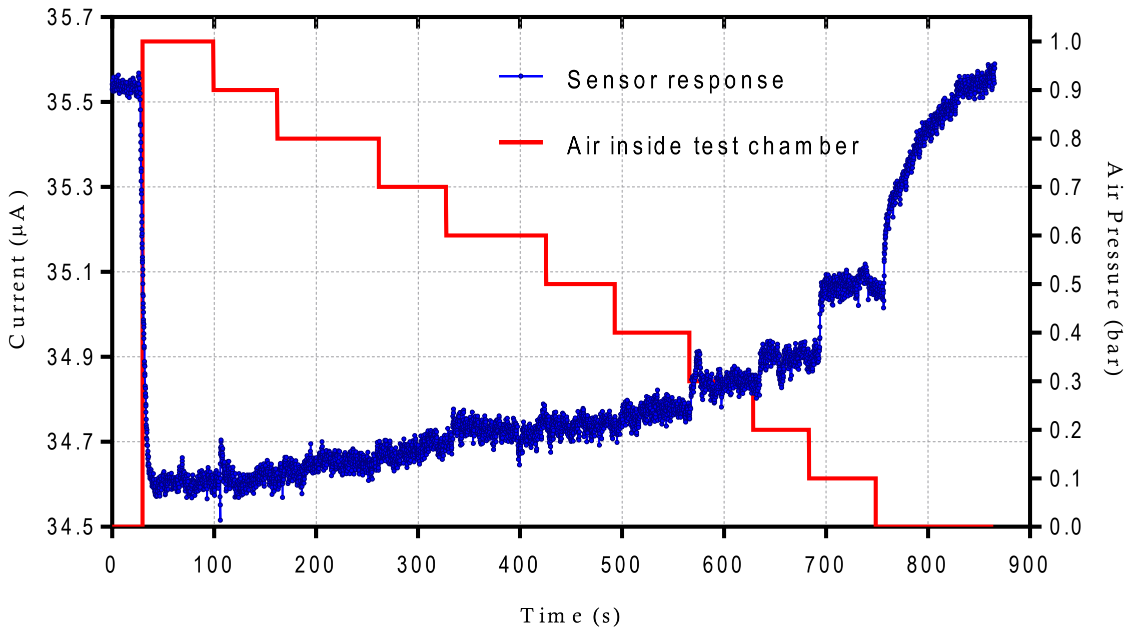


Figure 6.7: Comparison of sensor response between Air and CO_2 under constant pressure.

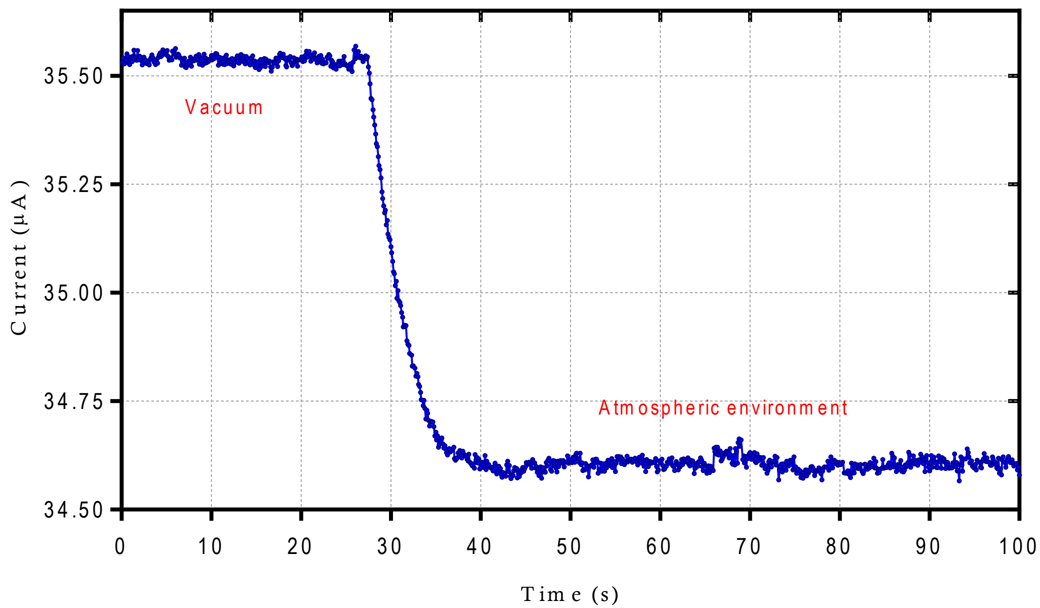
Figure 6.8 shows the result of variation in air concentration along with the chamber pressure. The sensor current dropped sharply when the chamber was brought to the

atmospheric environment from the vacuum state. However, the increase in current due to reducing pressure is not substantial as long as the chamber has some air molecules. The current changes become considerably higher again when the air concentration is very low or when air is removed from the chamber. It indicates that the change in current is mostly caused by the molecular interaction between the CNTs and air. Front-

(a)



(b)



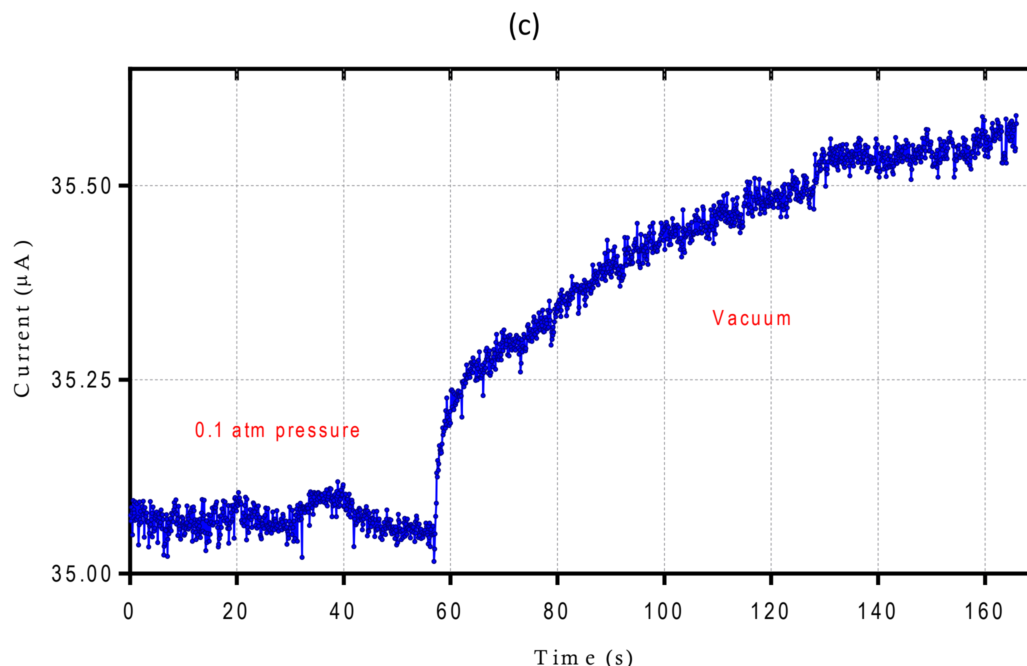


Figure 6.8: Sensor response with variation in air pressure; (a) Gradual decrease of air from test chamber; (b) Vacuum to atmospheric environment; (c) Low air concentration with 0.1 bar pressure to vacuum.

end circuits can be used in CMOS for better signal processing [302] and calibrating different sensors with variation in electrical characteristics caused by the lack of control in reproducing similar CNT-based connections between the microelectrodes.

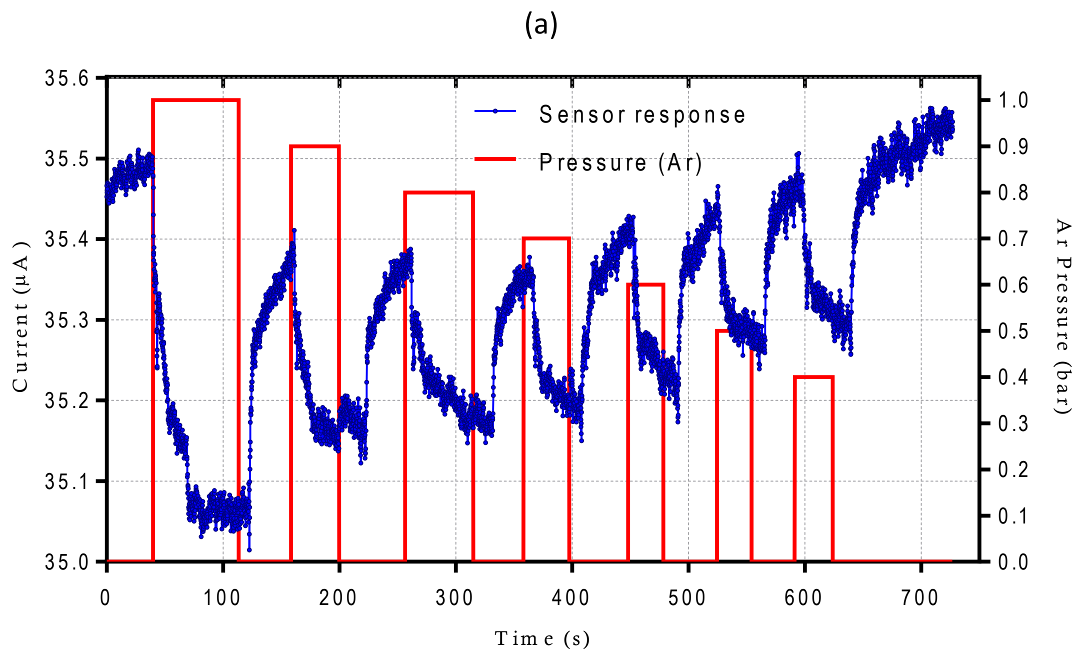
Response time of the sensor from vacuum to the atmospheric environment can be measured from *Figure 6.8b*. Around 1000 nA current dropped within less than 15 seconds. The current increase from low air concentration at 0.1 bar pressure to vacuum is highlighted in *Figure 6.8c*. While the reduction in similar pressure level (such as 1 bar to 0.9 bar air) did not produce considerable current increase, the removal of 0.1 bar air resulted in ~500 nA gradual raise in current. It took ~90 seconds for the sensor to reach its initial condition from the low-concentration air exposure.

6.5 Pressure response

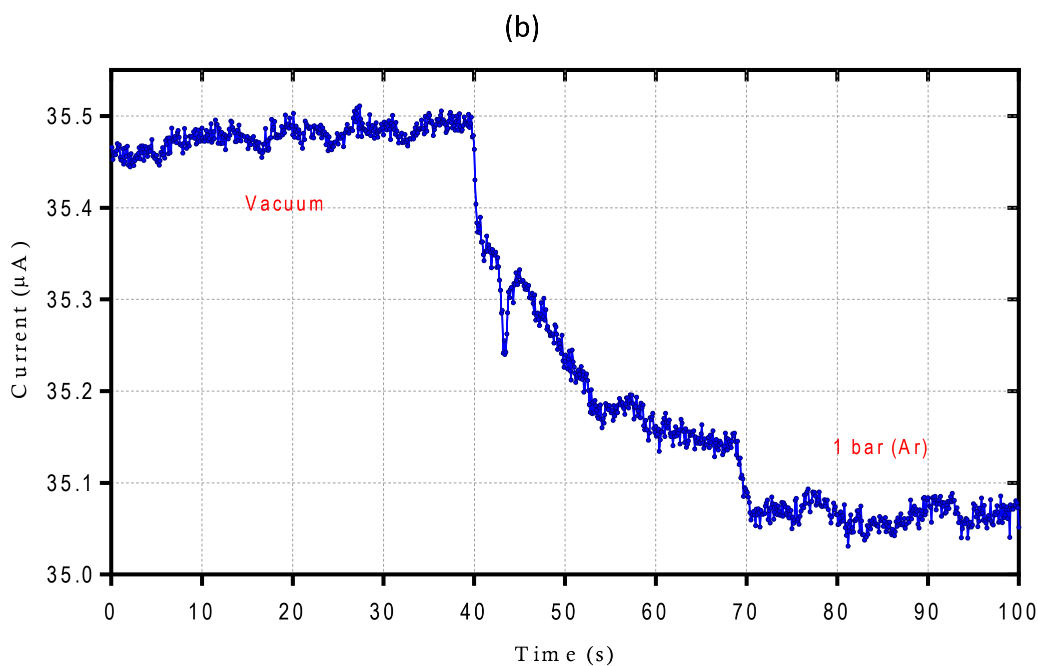
The pressure response of the sensor was tested (*Figure 6.9*) by introducing Ar in the chamber. The pressure was gradually decreased with a step of 0.1 bar from 1 bar down to 0.4 bar in between vacuum cycles. A maximum of 1 bar chamber pressure from the initial vacuum condition resulted in ~400 nA gradual drop in current.

It should be noted that the sensor response time due to change in pressure is not as rapid as gas sensing. With the same amount of chamber pressure, the sensor current dropped to a stable value in less than 15 seconds for air (*Figure 6.8a*), while the pressure response took over 30 seconds to stabilize. The drop in current of ~1000 nA is also high in gas sensing compared to the ~400 nA for pure pressure sensing. But in case of gas response, the current drop also includes changes due to pressure. Therefore, the sensor response based on only gas interaction should be ~600 nA for 1 bar chamber pressure.

(a)



(b)



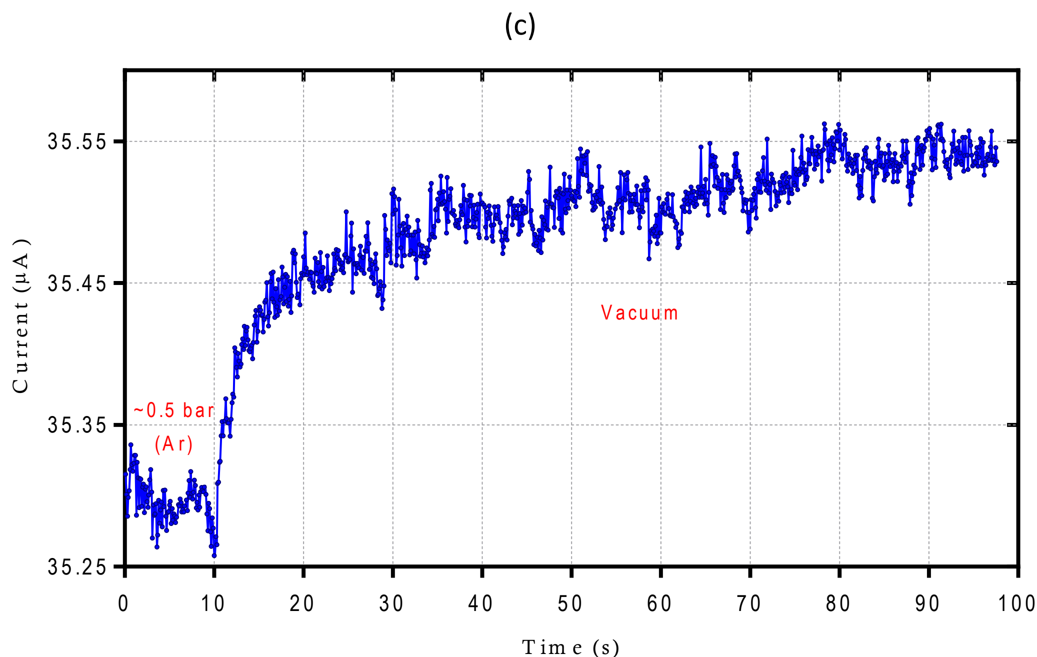


Figure 6.9: Sensor response at different chamber pressure; (a) Gradual removal of argon from the test chamber; (b) Vacuum to 1 bar argon; (c) 0.4 bar argon to vacuum.

In terms of recovery time, the response appears to be faster in pressure sensing, although a direct comparison cannot be made. The sensor took less than 30 seconds to retain the initial current value the chamber pressure was changed from 0.4 bar to vacuum (*Figure 6.8b*). In contrast, the sensor took ~8 minutes to fully recover in vacuum from 1 bar pure CO_2 exposure (*Figure 6.7*).

6.6 Conclusion

Although the synthesized CNTs were not long enough to suspended horizontally between the two electrodes, many CNTs grown from the CMOS-MEMS heaters could connect to the Si substrate. Electrical connections were detected when CNTs grown on two adjacent heaters established a link through the conductive bulk. I-V curves of CNT connections on different microheaters were presented. Both gas and pressure sensing were demonstrated on such a configuration. The gas and pressure response of the senor was distinguished through different experiments.

Chapter 7

CMOS Microheater Challenges and Wafer-level Scaling

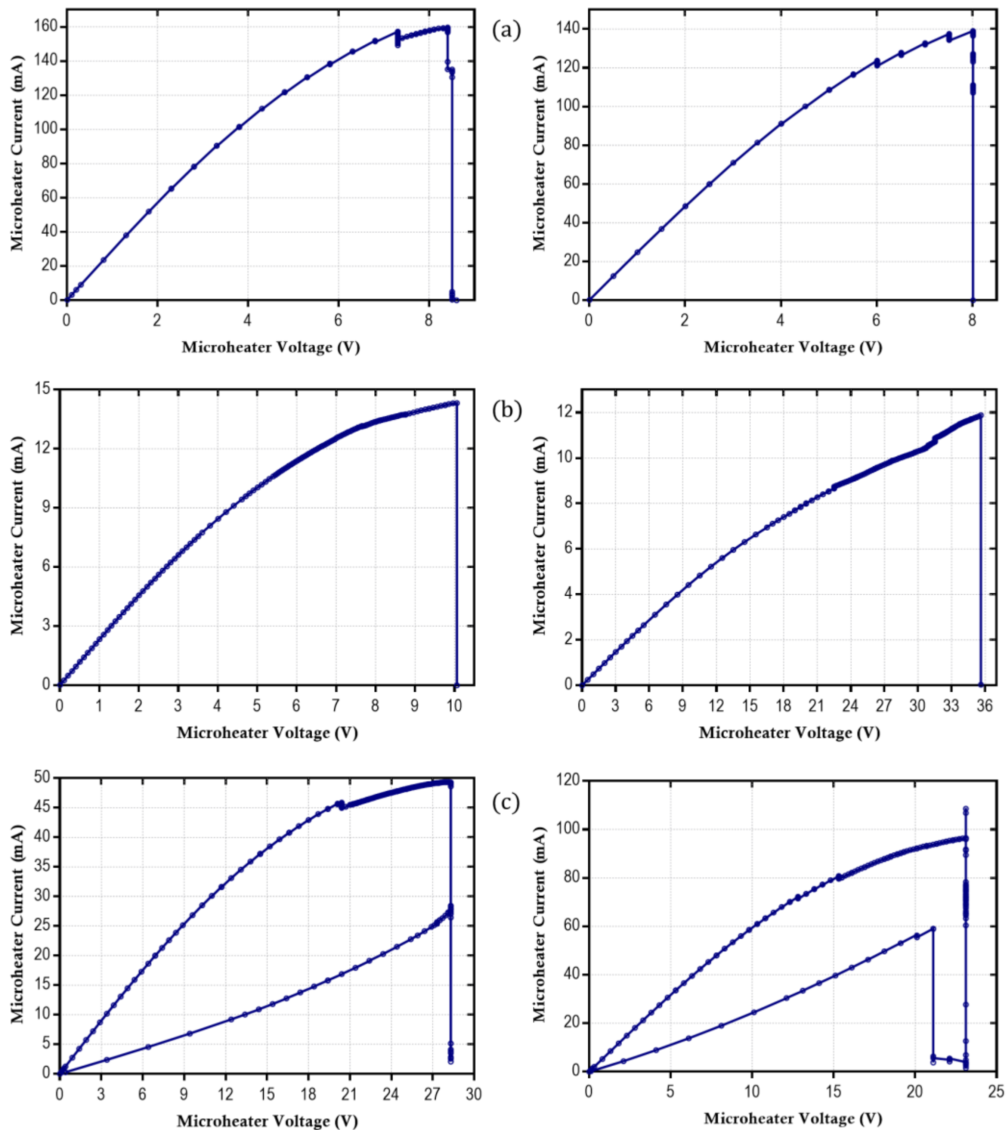
7.1 Introduction

The most challenging part of CNT growth on the polysilicon CMOS-MEMS microheaters has been controlling the temperature during joule heating based on the temperature dependant resistivity of polysilicon due to its thermal stability issues at high temperatures. Polysilicon is made of single crystal silicon grains with varied orientations and sizes. These grains are separated from each other by grain boundaries, which along with the grains determine the conduction in polysilicon [303]. Polysilicon suffers from unstable grain boundary; thermal stability issue of polysilicon due to highly reactive grain boundary causes resistance drift [190,303–307]. Temperature and doping concentration have high impact on the resistivity of individual grain [190,303,308]. Large difference in local grain temperatures on the polysilicon CMOS-MEMS heaters could be the reason for their breaking before reaching higher CNT synthesis temperature. Polysilicon thermal breakdown can occur due to local melting of grains or grain boundary layers at high currents during joule heating [190,309,310]. The grain boundaries of polycrystalline materials are also more susceptible to oxidation as molecular species have a preference to migrate there, which influences the resistivity of polysilicon [307]. This can be a potential reason why the exposed CMOS-MEMS heaters were breaking at lower temperatures, while the polysilicon microheaters passivated by the dielectric layer could reach melting temperature as shown in *section 8.3*. The results from this chapter will be included in some planned publications.

7.2 Electrical control and temperature limitations

Breakdown of the polysilicon CMOS-MEMS heaters was abrupt. *Figure 7.1* presents the I-V curves of different microheaters showing the nature of their breakdown. Based on

the CNT synthesis results and heater characterizations, thicker or wider heaters are more thermo-mechanically stable and generate higher temperature on a relatively consistent basis. The kink point(s) (a point where direction of a curve has sharp change) in wide heaters (*Figure 7.1a*) or thicker stacked heaters (*Figure 7.1e*) provide some indication of its mechanical stability before the breakdown occurs. The voltage / temperature control of the narrow heaters is more challenging, and such heaters can break very rapidly without providing any indication in the I-V curves (*Figure 7.1b*). Voltage is increased at a lower step or slower rate for these heaters to avoid increasing the heater current density too fast, which can result in a kink point for the narrow heaters (*Figure 7.1d*). Heaters can also become partially broken or their broken region can partially reconnect to form a conducting path again as shown in *Figure 7.1c*.



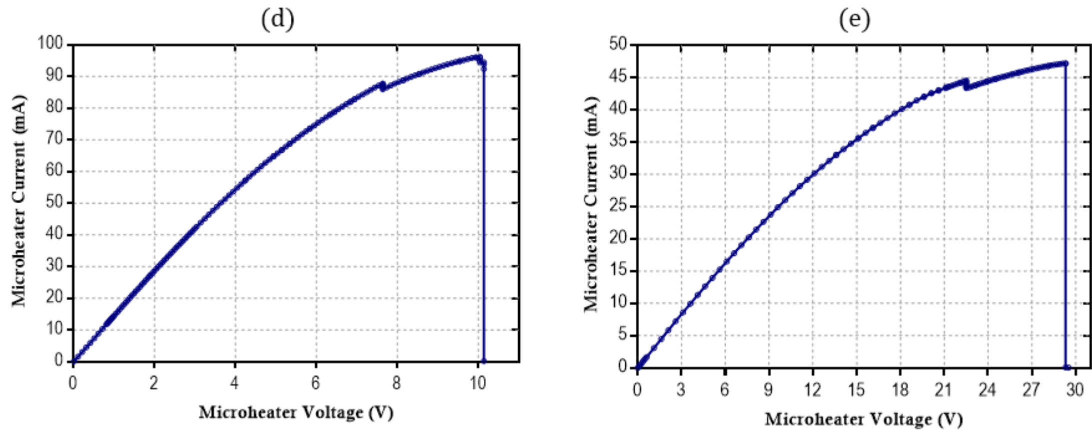


Figure 7.1: Electrical characterization of different broken CMOS-MEMS polysilicon heaters. I-V curves of (a) wide (≥ 20 µm), (b) narrow (≤ 2 µm), (c) half broken, (d) narrow with lower and slower voltage increment, and (e) stacked poly-1 – poly-2 microheaters.

The wider heaters with higher surface area require longer time to reach a relatively stable temperature during the joule heating. For these heaters, the voltage should only be increased after waiting sufficient duration when the heater resistance somewhat stabilizes. Increasing the voltage at a faster rate would create a local hotspot on the heater while most of the surrounding regions are at much lower temperature; it creates a high thermal gradient within the heater, resulting in a mechanical deformation due to the thermal stress. Xie et al. [190] reported the unstable behaviour of highly doped CMOS polysilicon microheaters like ours, when the heater temperature exceeds the polysilicon recrystallization temperature, which can be at ~600 ˚C [311].

To estimate temperature of the polysilicon CMOS-MEMS heaters, we operated some of them under an optical microscope. Most of the heaters became incandescent at local regions. Different stages during the joule heating of a non-suspended microheater is shown in *Figure 7.2*. Incandescence (thermal radiation) captured on heater can be seen in *Figure 7.2b & 7.2c*. With the increase of operating voltage, the heater showed mild red glow (*Figure 7.2b*), which turned brighter (*Figure 7.2c*) before breaking abruptly (*Figure 7.2d*). SEM images in *Figure 7.3* shows various conditions of several identical or similar microheaters when CNT synthesis was attempted. It shows the heaters were either broken, damaged or have grown CNTs / fibres in the similar regions where incandescence was seen in *Figure 7.2c*.

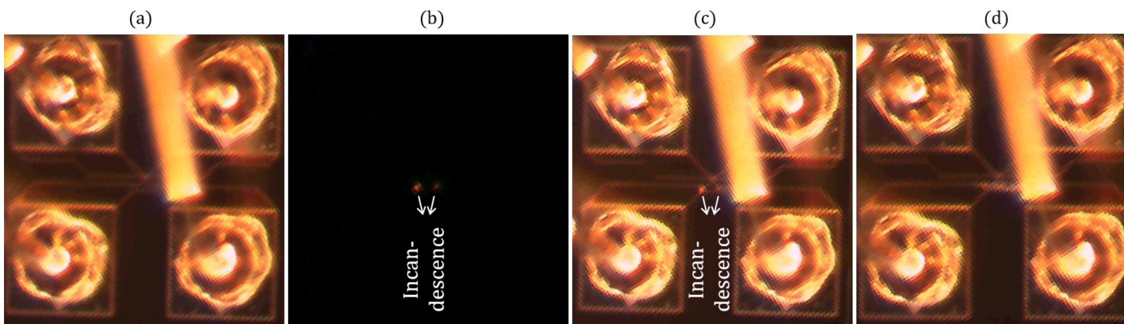


Figure 7.2: Optical micrographs of different stages during a polysilicon CMOS-MEMS microheater joule heating. (a) Initial stage; (b) Mild red glow; (c) Brighter red glow; (d) Heater broken.

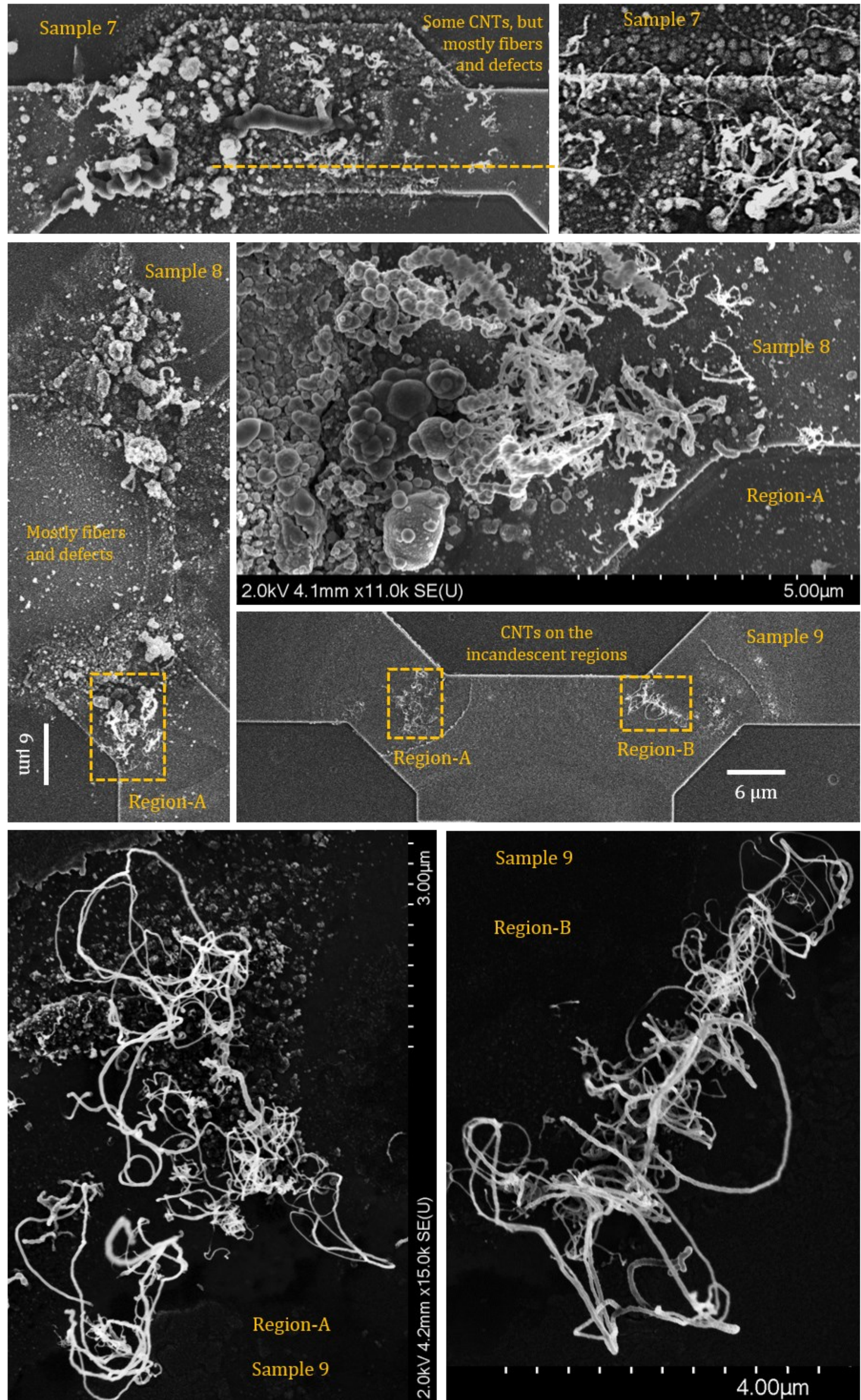


Figure 7.3: CNT growth attempts on several identical or similar microheaters in different CMOS chips.

Due to the difficulty in temperature control, not all heaters were successful to grow CNTs. Even for identical heaters, the resistance and breaking voltage can differ due to the thermal stability issue of polysilicon, as discussed earlier. Hence, the required electrical power of the heaters to generate similar temperature can vary. Since the heaters break abruptly, it is difficult to estimate when the precursor gas should be introduced. Therefore, instead of electrical control, a better indication to start the CNT synthesis process for the current CMOS-MEMS heaters would be when the electromagnetic radiation emitted from the microheater falls in the visible range, as observed in *Figure 7.2c*. With proper calibration, microheater temperature can be estimated based on incandescence [254,312]. CNT synthesis on microstructures have also been successfully done by rough estimation of the glow intensity [176,190].

An electron micrograph of the polysilicon heater from *Figure 5.18* was overlaid by an optical micrograph captured during the incandescence phase of an identical partially suspended microheater in *Figure 7.4*. Glow of this heater covered a relatively wider surface area compared to the non-suspended heaters. Effect on the hottest regions of identical heaters can be seen in *Figure 5.18*.

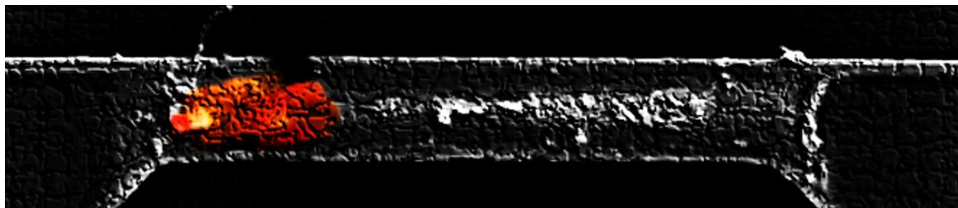


Figure 7.4: Electron micrograph of a partially suspended microheater overlaid with an optical micrograph of incandescence on the heater.

7.3 Heater damages

The microheaters were damaged in several manners. The most common form of damage is a small crack (*Figure 7.5a*), possibly at the hottest spot of the heaters. Different heater designs have different mechanically vulnerable regions. Regardless of their differences in thickness and material properties, the broken region was similar for heaters made of poly-1, poly-2 and metal with identical surface area (*Figure 7.5b*).

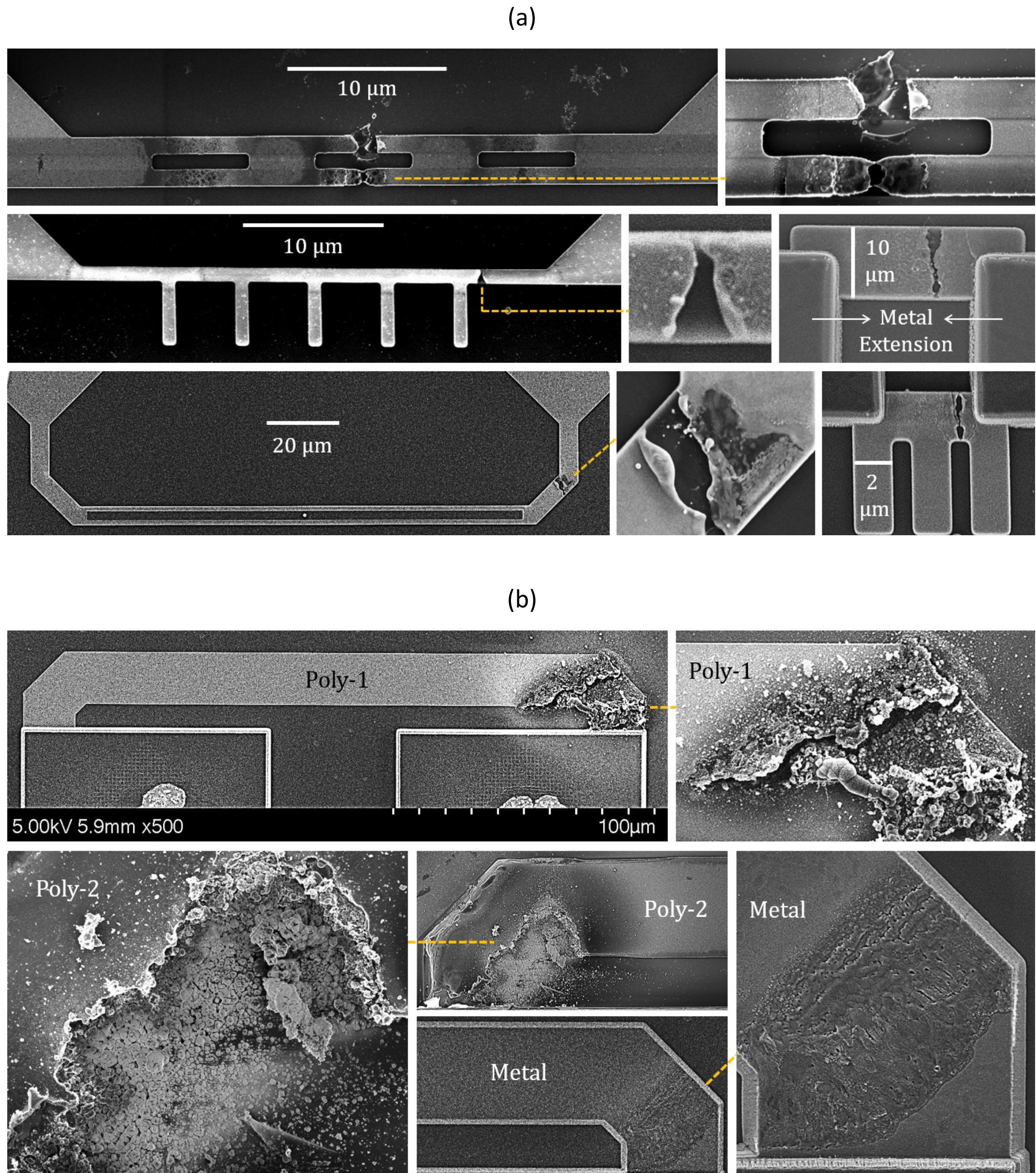


Figure 7.5: Broken microheaters after joule heating. (a) Cracked regions of different polysilicon heaters; (b) Breaking of identical heaters made of poly-1, poly-2 and metal layers.

Deformation has been observed in the fully or partially suspended microheaters as shown in *Figure 7.6a*. Buckling is a potential reason for such heater deformation. Among suspended (partially or fully) and non-suspended heaters, the latter reaches higher temperatures for most heaters, which can be due to their higher thermo-mechanical stability. Higher heater suspension means the required voltage (or power) to reach a

certain temperature will be lower than what is needed for its non-suspended counterpart due to reduced thermal loss through the substrate. Therefore, the voltage should be controlled more carefully for the suspended heaters as they will reach the maximum temperature at a lower voltage, depending upon the amount of suspension. Although poly-2 is thinner than poly-1, both heaters posed similar thermo-mechanical challenges among the non-suspended choices. However, since poly-1 heaters have lower resistance than poly-2 heaters with similar surface area, voltage should be increased at a slower rate or lower step during joule heating. For partially or fully suspended poly-1 and poly-2 heaters, poly-2 layer goes through faster under-etching than poly-1 due to its thicker dielectric layer underneath. Hence, their voltage should be adjusted accordingly in the resistive heating process. In some cases, microheaters with large surface area had excessive damage on some or entire region of the heater (*Figure 7.6b*).

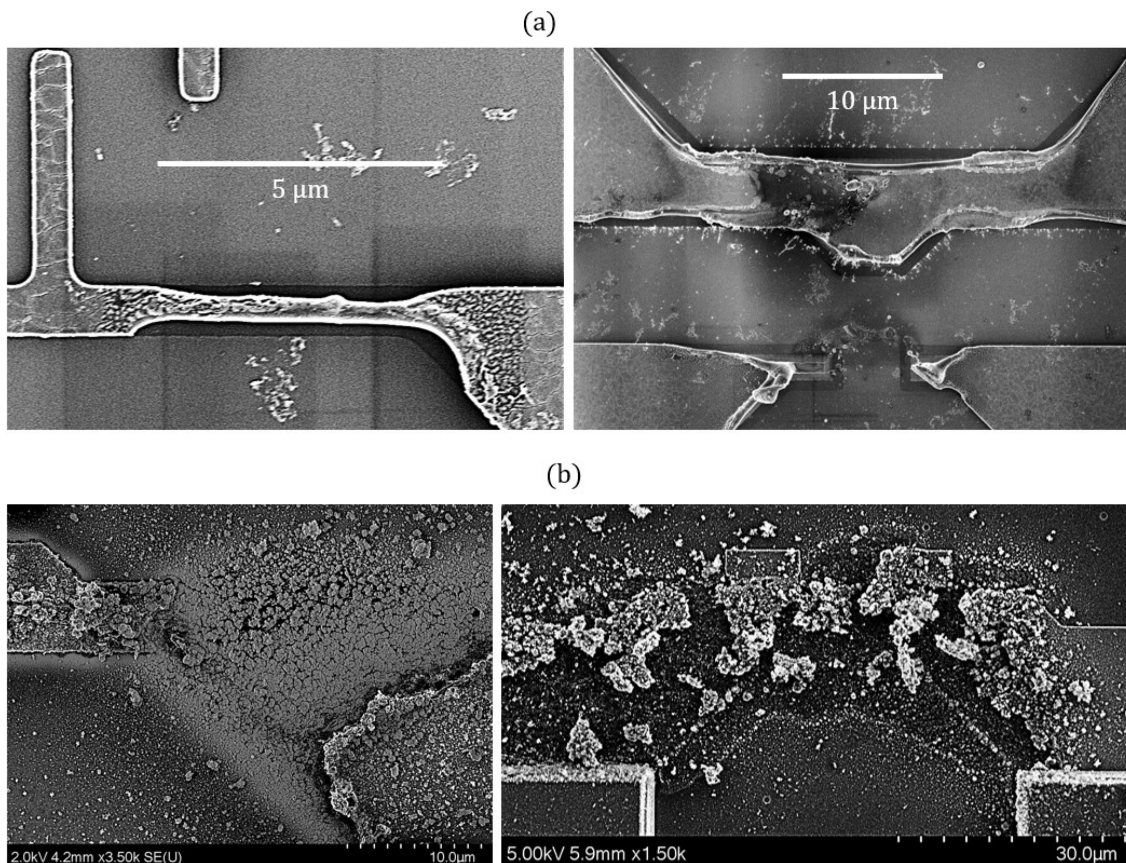


Figure 7.6: Damages in microheaters after joule heating. (a) Deformation in fully or partially suspended heaters; (b) Most damaged heaters.

Some microheaters with large surface area also caused partial melting and deformation in the neighbouring metal contact pads (*Figure 7.7*). Since the contact pads are made of Al, the temperature surrounding the heaters should be over Al melting temperature (~660 ˚C). The maximum temperature on the heater surface must be much higher.

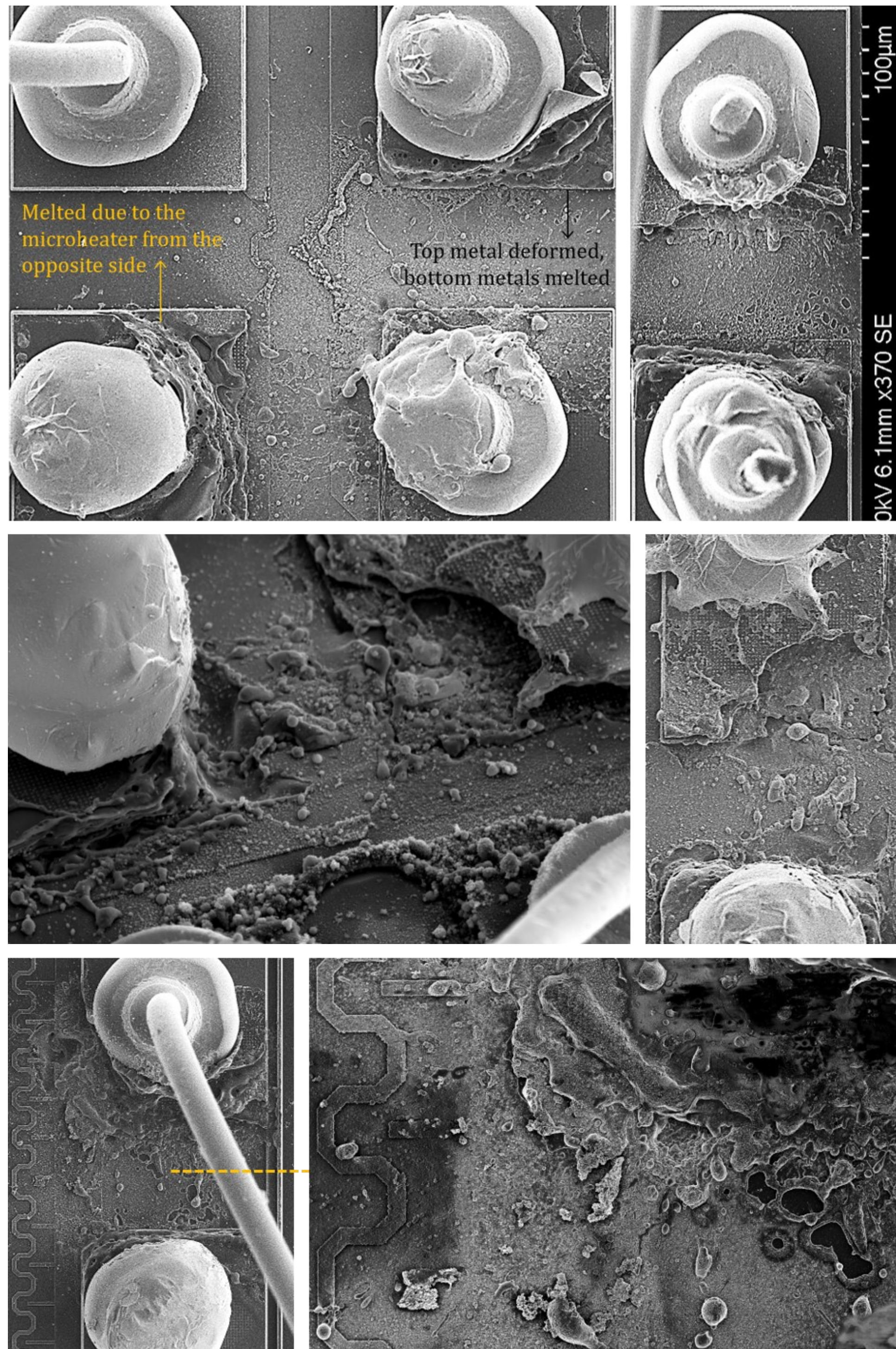
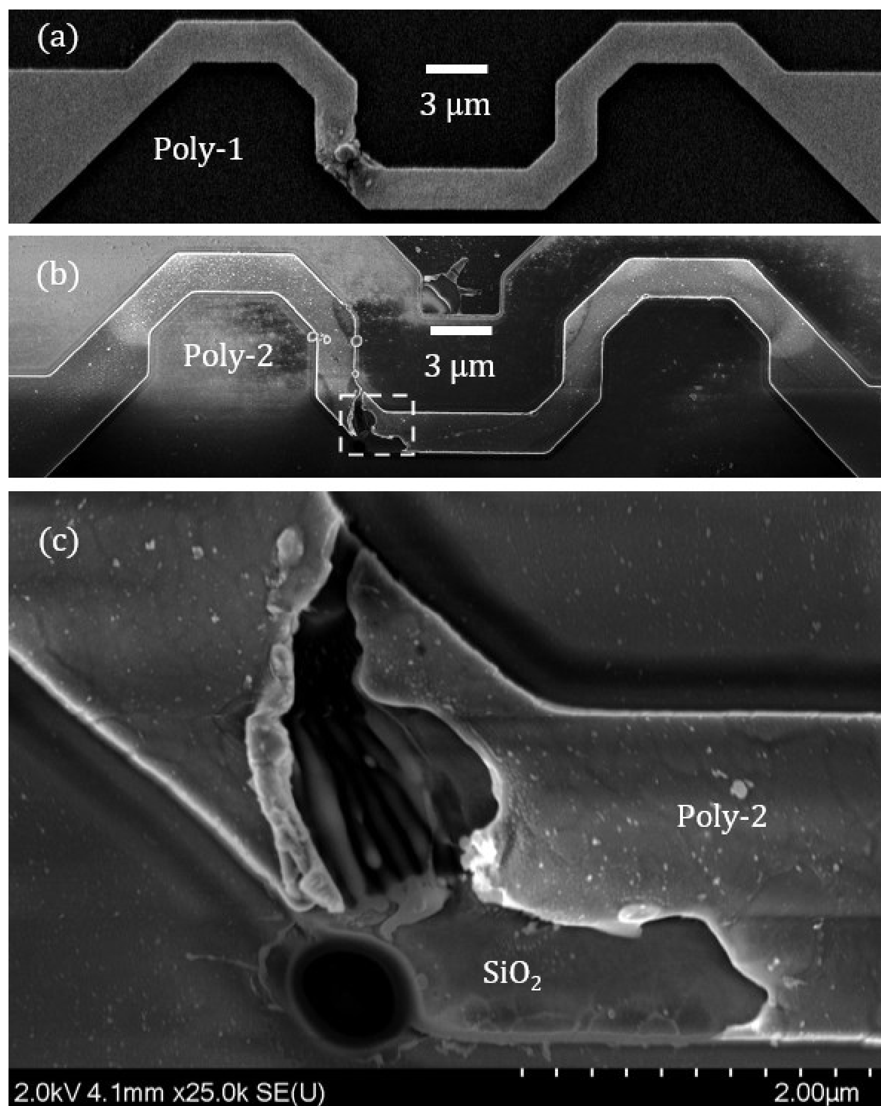


Figure 7.7: Melting in sections of aluminium contact pads for some heaters with low thermal gradient.

The breaking regions and mechanical deformation of similar wave-shaped poly-1 and poly-2 microheaters during the CNT synthesis are shown in *Figure 7.8*. Based on several testing, the broken region seen in *Figure 7.8a & 7.8b* is identified as the vulnerable spot for such non-suspended microheaters. *Figure 7.8c* shows the broken region of the non-suspended poly-2 heater that reveals the underneath dielectric layer. The suspended heaters in *Figure 7.8d & 7.8e* are from the same chip, which was wet etched for ~30 minutes by Pad-etch. The broken region in *Figure 7.8d* reveals the under-etched region of the poly-1 heater; SiO_2 was etched by ~0.5 µm on each side of the heater. The poly-2 heater with same width was, however, fully suspended due to the exposure of its thicker dielectric layer to the etchant. This heater shows deformation (*Figure 7.8e*) with a shrunken region, possibly caused by buckling during the high-temperature operation.



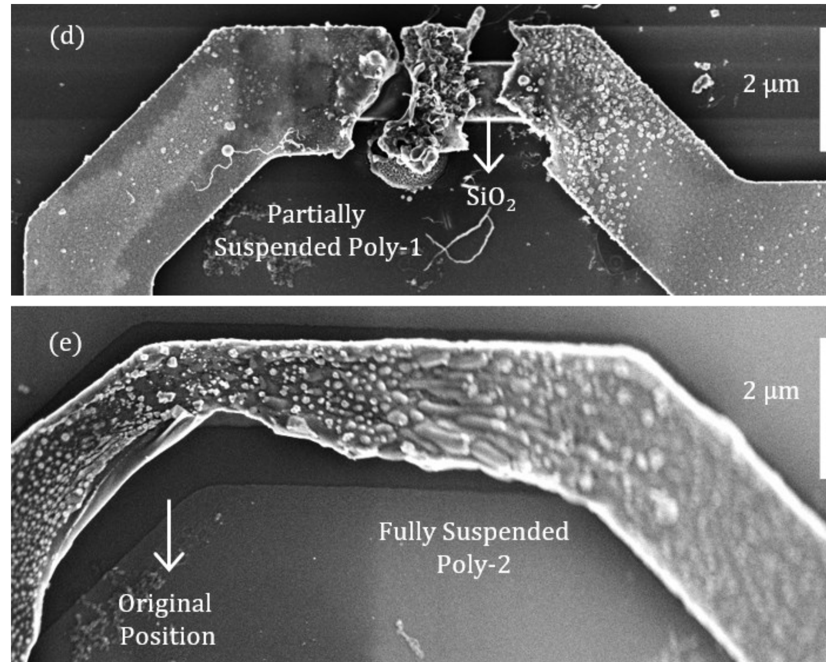


Figure 7.8: Broken wave-shaped polysilicon microheaters; (a) Poly-1; (b) Poly-2; (c) Close-up of poly-2 break; (d) Wet etched poly-1 revealing amount of under-etching; (e) Fully suspended poly-2 deformation.

The shift in breaking point of identical 10 µm × 1 µm rectangular microheaters are shown in *Figure 7.9a, 7.9b & 7.9c*. Equation (5) indicates that such a rectangular heater will have maximum temperature at its centre. Since the microheaters break in the region where the temperature is maximum, a shift in the maximum temperature can be inferred for the non-suspended poly-1 microheaters as the crack in them occurred ~1 µm away from the heater centre (*Figure 7.9a & 7.9b*). In case of the partially suspended heater, the crack appears very close to the centre (*Figure 7.9c*), indicating its maximum temperature. Similar temperature shifts have also been seen in simulations (*Figure 2.8*). The shift in temperature can be due to Thomson effect, which increases in small structures during joule heating [313,314]. While the non-suspended or partially suspended microheaters had cracks, a fully suspended poly-2 microheater with same design was broken and deformed (*Figure 7.9d*). It shows higher thermo-mechanical stress on the thin suspended heater.

The heater region with maximum temperature is a common place for both cracks and CNT growth. CNTs are often found inside or near a broken heater region as shown in *Figure 7.10*. It demonstrates the main challenge of CNT growth on the CMOS-MEMS

heaters. In order to grow CNTs on most of these heaters, they need to be operated very near to the breaking voltage of the heater. As a result, the heaters often get broken even before starting the synthesis process. The microheaters may also break during the growth process when operated for longer duration. In *Figure 7.11*, different outcomes can be seen for identical heaters when it was attempted to grow CNTs at the maximum obtained heater temperature. Four scenarios were commonly found; the heaters can break, catalyst dewetting can be observed without any growth, only CNFs and defective CNTs can grow or CNTs can be successfully synthesized.

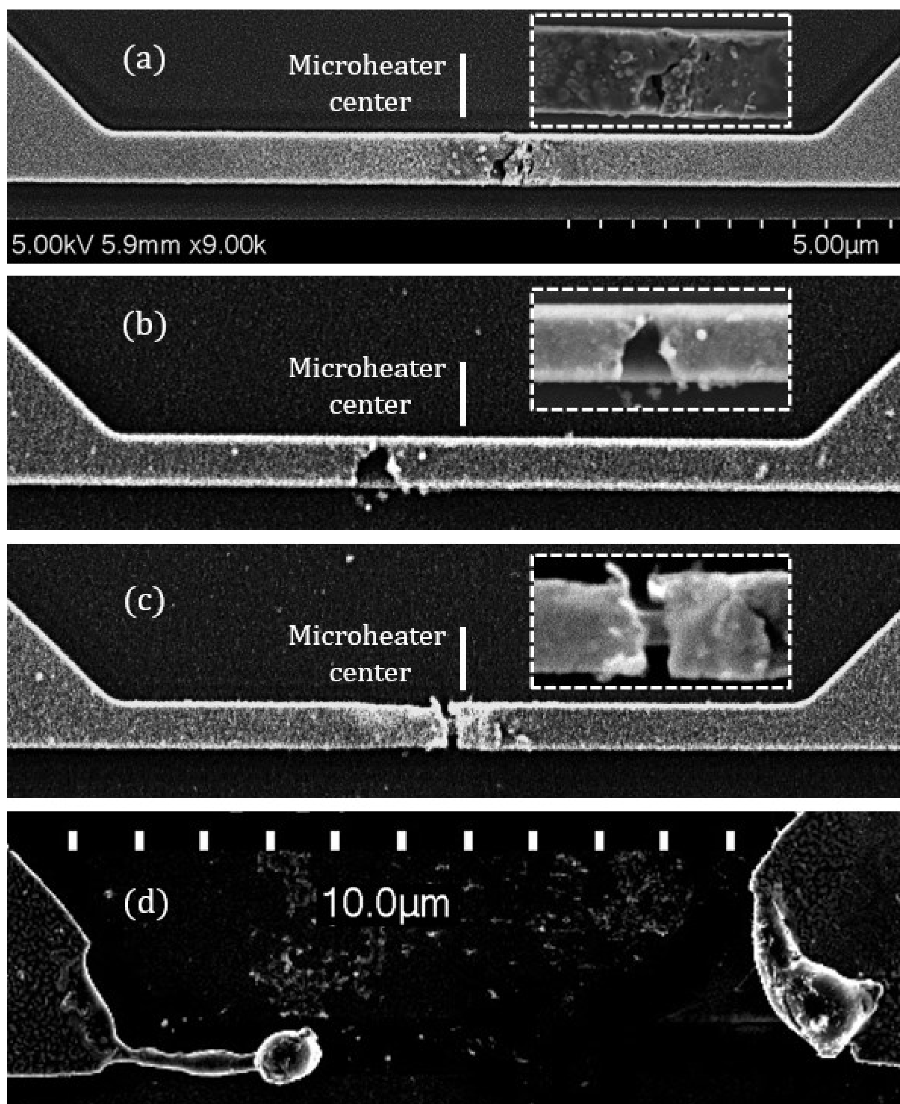


Figure 7.9: Breaking of rectangular polysilicon microheaters; Deviation of breaking points from poly-1 microheater centre: (a) non-suspended (< 1 μm), (b) non-suspended (> 1 μm), (c) partially suspended (at centre); (d) deformed fully suspended poly-2 heater of same design.

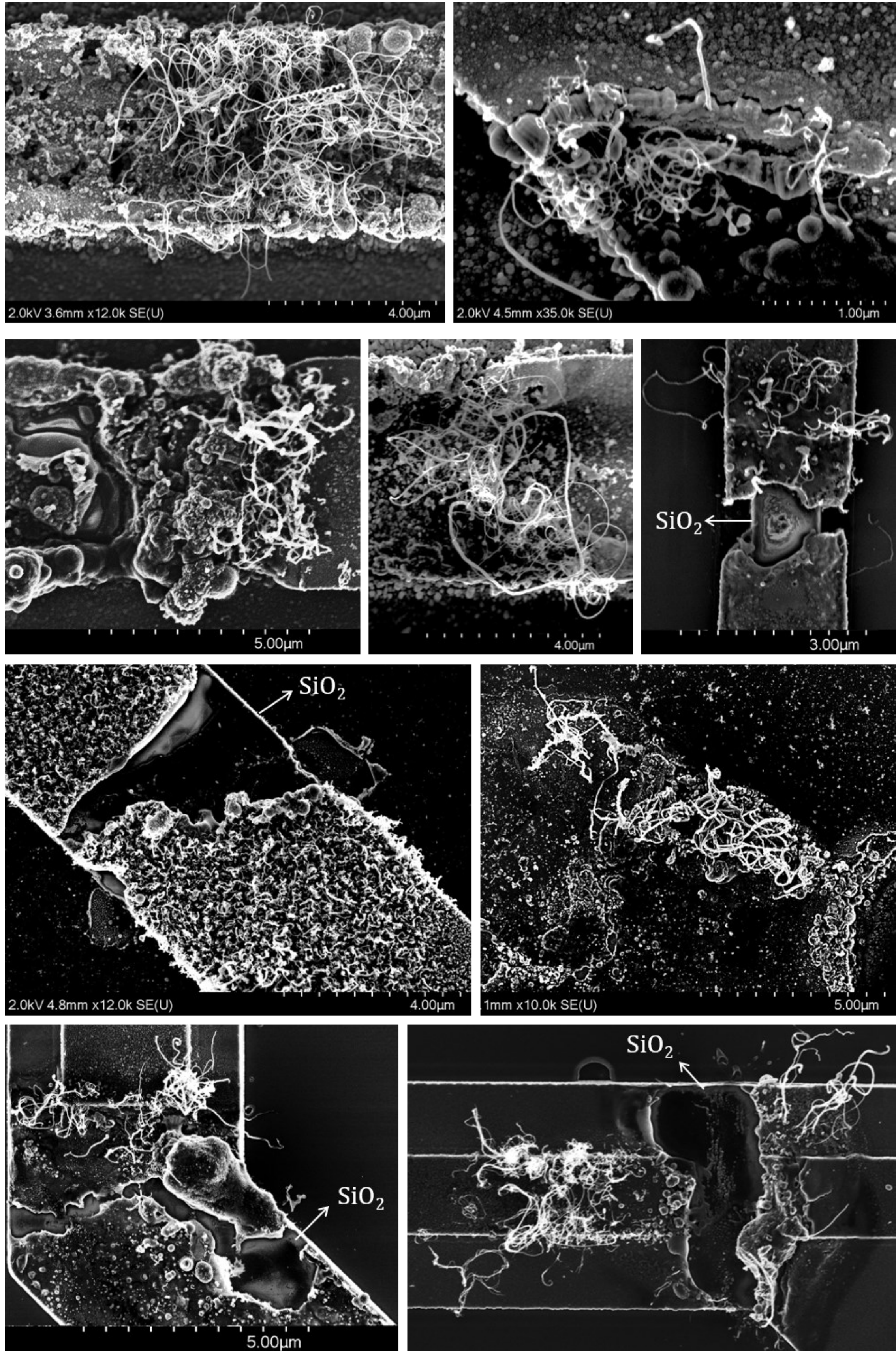


Figure 7.10: CNTs grown inside or around broken microheater regions.

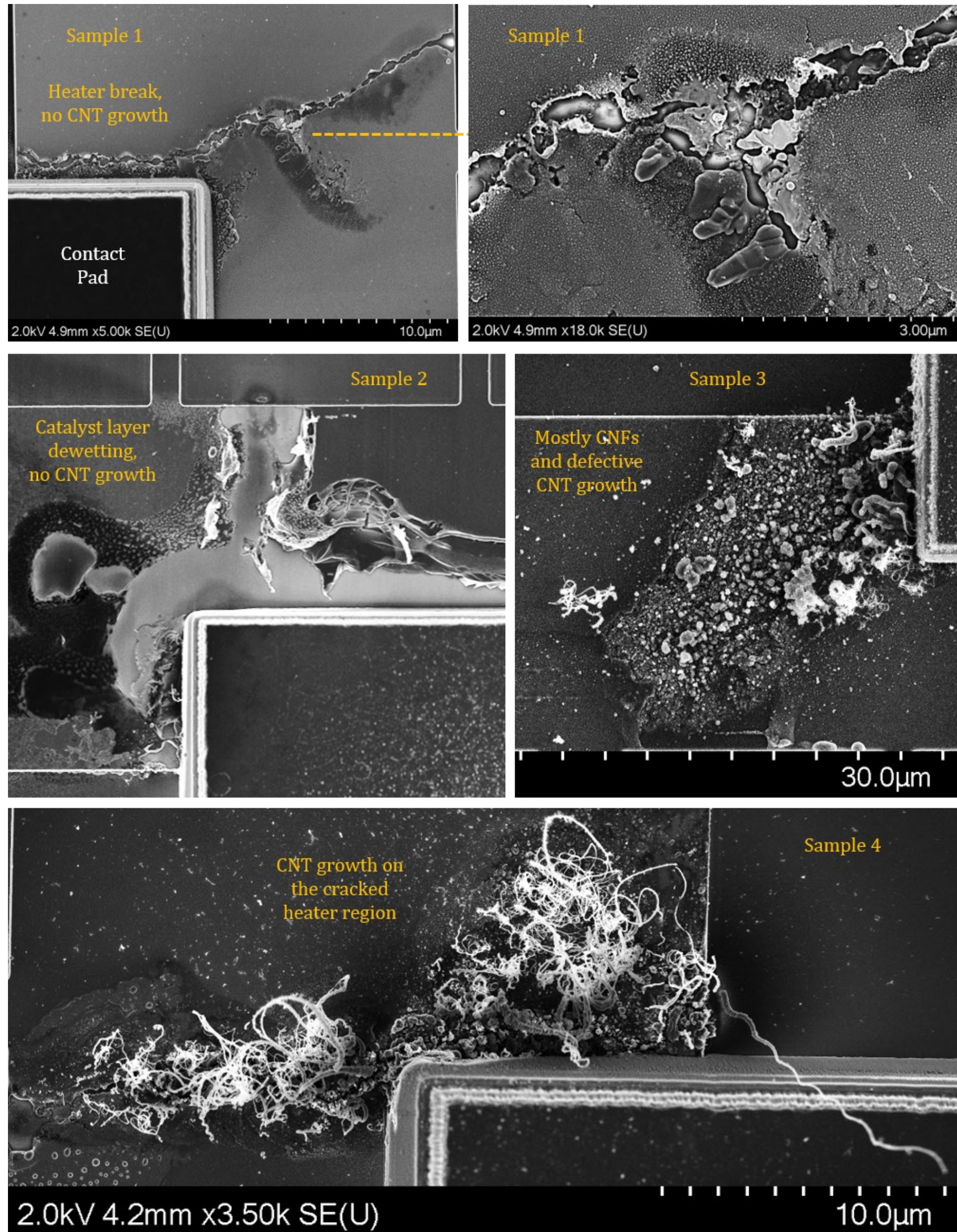


Figure 7.11: Different outcomes on the maximum temperature region of identical microheaters.

7.4 CNT growth development

The development of synthesis process to obtain desired range of CNTs can be complex due to the influence of numerous parameters. The insufficient understanding on the growth mechanism also adds complexity to the development process. The synthesized CNTs on CMOS-MEMS microheaters with 3 nm Fe provided CNTs with a wide range of diameters, including within the desired range of 5-10 nm. CNTs grown using 3 nm Ni provided narrower CNTs with most of them fall in the diameter below 20 nm. CNTs

below the diameter of 5 nm was also found with this catalyst layer. In addition, the number of CNTs per unit area increased significantly with Ni compared to Fe catalyst. Introduction of H_2 etching gas improved the overall quality of the CNTs grown from Ni nanoparticles, as well as relatively increased the CNT length. Although it was possible to get connection between the adjacent heaters with the shorter CNTs through the Si substrate by growing on both heaters, its reproducibility is challenging due to the nature of the connection. Therefore, further development is required to obtain desired CNT lengths in the range of 10-15 µm.

For CNT growth development, it is important to have good control over the process parameters so that only intended factors can be varied. The CMOS-MEMS microheaters are not suitable for CNT growth development due to the lack of temperature control over, as demonstrated in *Figure 7.3 & 7.11*, along with the limitations in number of samples obtained from the CMOS foundry. Therefore, the process should be developed on test structures under stable temperature, where the temperature needs to be similar to what was obtained by the CMOS-MEMS heaters. The goal is to ensure quality, yield, and small diameter of the synthesized CNTs, while extending their length sufficiently to suspend the CNTs between two adjacent microheaters / electrodes.

Based on the current CNT growth results, a good starting point for the growth development can be optimizing the gas flow ratio between the hydrocarbon precursor gas (C_2H_2) and reducing gas (H_2). A variation in this ratio can cause significant disparity [184], as demonstrated by the growth results in [279,289]. Without an optimized ratio of the involved gases, the catalyst can be deactivated causing hindrance in CNT growth [279,289]. The role of gas flow rate and duration is also important on the length, diameter and yield of the CNTs, as demonstrated by Tripathi et al. [315]. By fine tuning these two parameters, they obtained optimum CNT growth condition; parameter values beyond a narrow margin corresponds to shift from the desired CNT characteristics.

The total gas pressure with a fixed gas ratio can influence the resultant CNT length. It has been shown that increasing the pressure also increases the CNT length [279]. However, the results were obtained within a significantly low-pressure range (~0.65 to

~13.3 mbar) compared to the pressure (> 400 mbar) used in our process. Gas type also plays a role in the resultant CNTs [278]. Pre-heating the gas and lower catalyst layer thickness has also been effective for obtaining longer CNTs [316].

In CNT synthesis process, the catalyst layer dewetting and CNT nucleation mechanisms are complex and often occur at the same time; it can be decoupled by pre-heating the catalyst layer before introducing the hydrocarbon gas [184]. Microheater pre-treatment are often done with Ar, which can be influential for uniform coarsening of the catalyst thin film to nanoparticles [278]. Pre-treatment of the CMOS-MEMS heaters were attempted on a few occasions, but the results are not comparable due to the sample number of trials. The pre-treatment phase was mainly avoided because of microheater temperature limitations discussed in *section 7.2*. Low temperature CNT synthesis [161,183,285,317] processes and bi-metallic catalysts [282,316] can also be explored.

7.5 Towards wafer-level process for mass production

For commercialization of CNT-based sensors, low-cost manufacturing of the sensors is essential. In SiP integration approach, MEMS–CMOS assembly adds cost and processing steps, which are not compatible with low-cost mass production. The SoC integration approach is more cost-effective but requires CMOS-compatible post-processing steps. A microheater in CMOS with optimized dimensions can be as small as a few micrometres (*Figure 7.3*), hence, will not add to the expensive space of CMOS chips. The simulation results in *Figure 2.5, 2.6 & 2.10* indicate a very high thermal gradient around the microheaters, where the electronics can be at CMOS-compatible temperature within tens of micrometres. Therefore, a 1 mm × 1 mm CMOS chip could easily accommodate the required number of microheaters in a potential commercially produced sensor.

Successful CMOS post-processing has been demonstrated to locally grow CNTs on the CMOS-MEMS microheaters in our fabricated CNT-based prototype sensors. Our vision has been to incorporate the CNT synthesis process in a standard CMOS technology at wafer level. At the research level, the CMOS post-processing steps are performed on individual CMOS chips. However, those process steps may be included in a dedicated

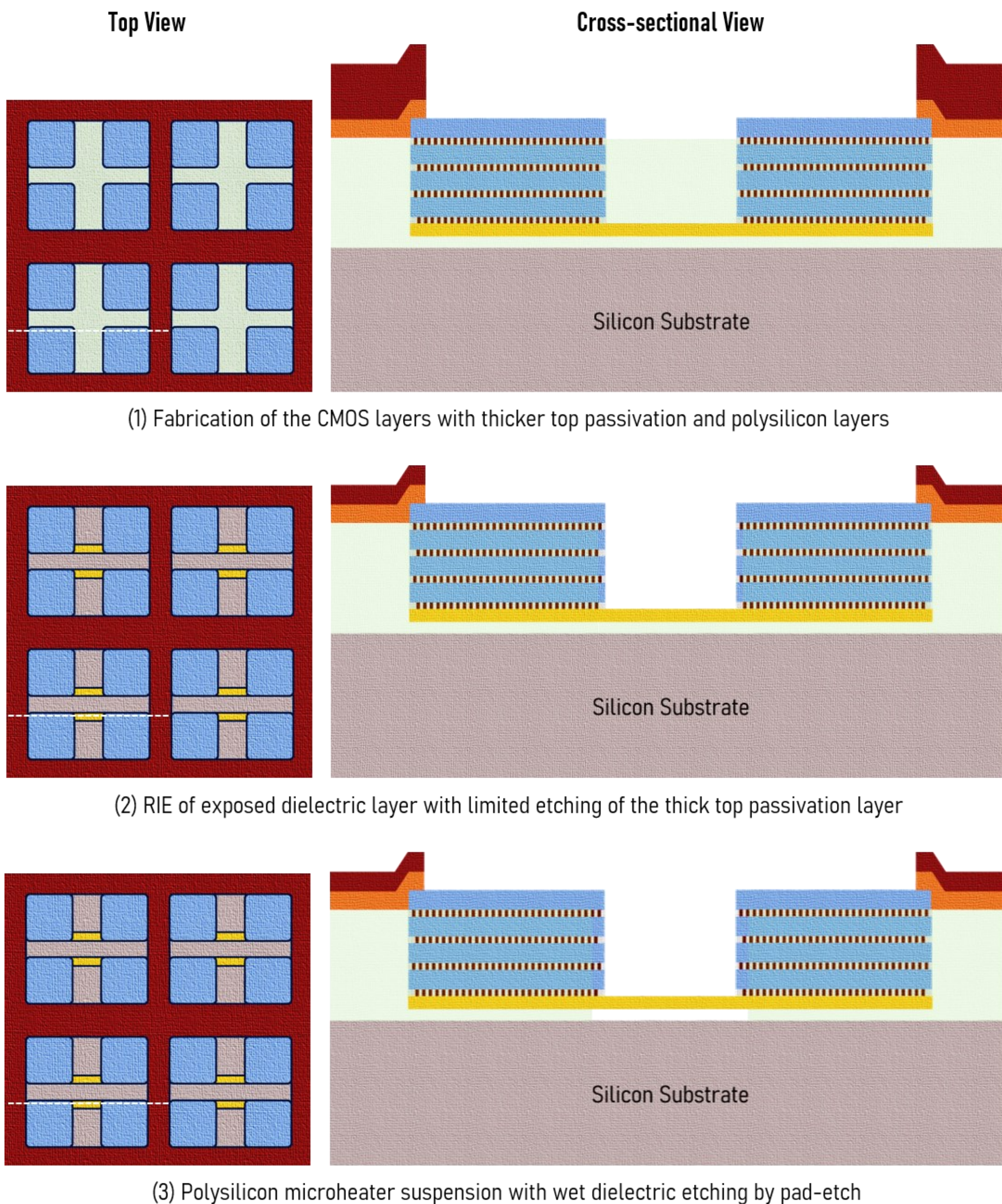
process designed for CNT-to-CMOS integration, which can be carried out in wafer-level fabrication for manufacturing commercially viable CNT-based sensors.

In a CMOS process dedicated for CNT integration, a few modifications can be desirable. In the MEMS-CNT integration process at USN [318], thicker (2 µm) polysilicon MEMS heaters were used compared to the ~200-300 nm thick CMOS-MEMS polysilicon heaters. The MEMS heaters showed better thermo-mechanical stability to obtain higher heater temperature for CNT synthesis. The doping concentration used for the MEMS polysilicon layer resulted in negative temperature coefficient of resistance (TCR) after resistivity reaches peak near the desired CNT growth temperature. It enabled a good electrical control for conveniently operating the heaters at the targeted CNT synthesis temperature [275]. Polysilicon layers with similar characteristics could be adapted for a dedicated CMOS process. In heavily doped polysilicon layers, sheet resistance is affected by temperature cycling [303]. Polysilicon sheet resistance was found to be more stable with increasing layer thickness, tested within 550 – 900 °C for 20 minutes or higher; phosphorous doping was also more effective compared to arsenic and boron doping [303]. Although polysilicon has unstable grain boundary issues, it does not show aggregation at high temperatures unlike most metals [211]. Size of the grains in polysilicon has strong influence on its resistivity; increasing this size can result in stabilized polysilicon resistance [303]. Thermal stability of polysilicon can also be improved through the offered solutions from several articles such as [319–322].

The polysilicon layers are suspended by etching the dielectric layer beneath them. A thicker dielectric layer can reduce the possibility of stiction. Another modification for the dedicated CMOS fabrication process could be increased thickness of the passivation layer so that it does not completely etch away when dielectric RIE is performed. Making the suggested changes in CMOS would degrade the IC performance; a balance should be maintained in this trade-off.

All required CMOS post-processing have been demonstrated at the chip-level; however, these processes are also scalable to wafer-level. With the obtained results, our research takes a big leap in reaching our ambition towards an industrially feasible wafer-level

process [318], and opens the door for a low-cost method of mass manufacturing CMOS-MEMS heaters to locally grow CNTs for commercializing CNT-based sensors. Device to device reproducibility can be a concern for the mass production of these sensors [323], but such issues can be mitigated by smart front-end circuit designs [108]. A wafer-level fabrication process flow for mass producing CNT-based sensors on CMOS is proposed in *Figure 7.12*. It is based on the developed post-processing, which can be incorporated in an already existing CMOS technology with relevant modifications in fabrication process.



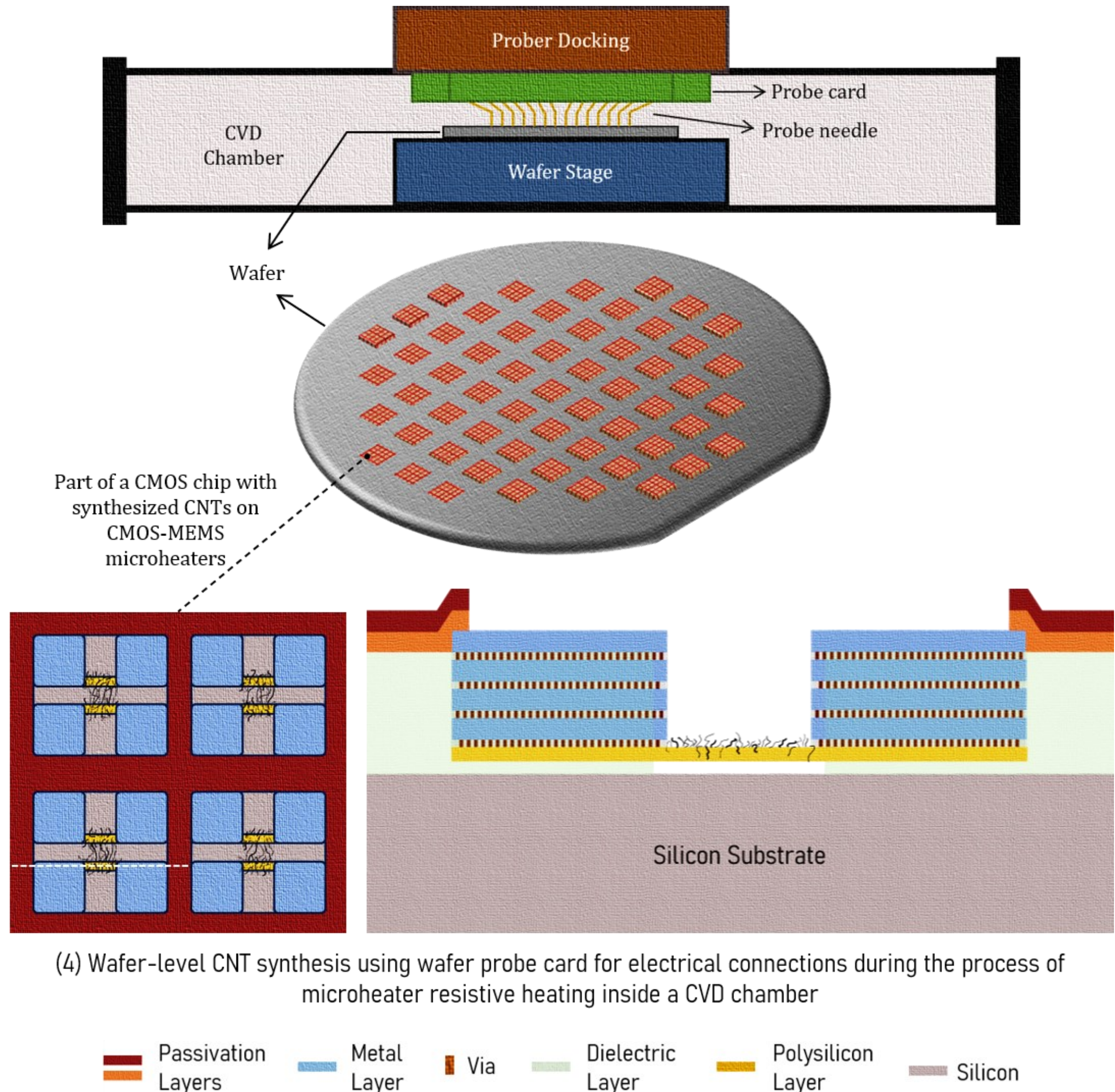


Figure 7.12: Proposed fabrication process flow for wafer-level local CNT synthesis on CMOS.

7.6 Conclusion

The challenges in controlling the temperatures of the polysilicon microheaters were addressed. Incandescence from some microheaters were captured with optical microscope that shows local high hotspots, temperatures of which are estimated below 800 ˚C. The potential strategies to further develop the CNT growth process on the CMOS-MEMS polysilicon heaters were discussed. Based on the developed process of direct CMOS-CNT integration in the chip-level, a wafer-level process was proposed for mass production of the CNT-based sensors.

Chapter 8

On-chip Temperature Sensing and Transistor Characterization

8.1 Introduction

CNTs have been locally synthesized on CMOS-MEMS microheaters at high temperatures (> 650 ˚C). Since the thermal microscopy results were not accurate due to resolution limitations (*section 3.5*), an alternative approach of on-chip temperature sensing was explored to estimate the ambient temperature of the CMOS chip when a microheater is operated at CNT synthesis temperature. Apart from our application, electronics are often exposed to high temperatures in industries such as automotive, avionics & aerospace, oil & gas and many others [324–326]. In all the applications involving high temperatures, a Si-based chip containing CMOS circuitries should be kept within CMOS-compatible temperatures, which can be up to 400 ˚C [186–188] depending on the duration. Long exposure to excessive temperatures can trigger dopant diffusion causing the transistors to lose their original characteristics. An integrated CMOS sensor to estimate the surrounding temperature near the transistor regions can be helpful to avoid damaging the electronic circuits during the high temperature applications.

A temperature sensor can be built on chip through diodes, MOSFETs and resistors; the latter two currently show better power efficiency [327–329]. Based on the calculated resolution figures of merit [330], temperature sensors made of resistors show significantly higher efficiency compared to the other two sensory devices. However, our vision for implementing the in-built CMOS temperature sensors with resistors was based on implementing a simplified approach of approximating local temperature, where signal conditioning circuits are avoided. The four-terminal polysilicon microstructures (*Figure 3.15*) were used to estimate on-chip temperatures based on the temperature-dependant change in resistivity of those resistors.

To claim successful CNT integration in CMOS, it is also important to ensure that the on-chip electronics operate successfully. The fabricated CMOS chips for CNT synthesis have some transistors along with some electronic circuits. These transistors were characterized before and after operating microheaters to CNT synthesis temperatures. Based on changes in the I-V curves of the transistors, CMOS-compatibility can be determined. Results from *section 8.2 & 8.3* of this chapter are published in *Article 7*, while the remaining results will be included in *Article 9 (in preparation)* and in a planned article.

8.2 Characterization of reference polysilicon microstructures

Figure 8.1 shows the experimental setup on a probe station (Micromanipulator) with four probe positioners, optical microscope, and a built-in hotplate. The tungsten probe tips with diameter of 25 µm were placed on the contact pads of the reference polysilicon microstructure in *Figure 3.15*. In the four-point measurements, the current was fixed at 1 mA across two probes using a source meter (Keithley 2602), while voltage was measured with a digital multimeter across the two remaining probes.

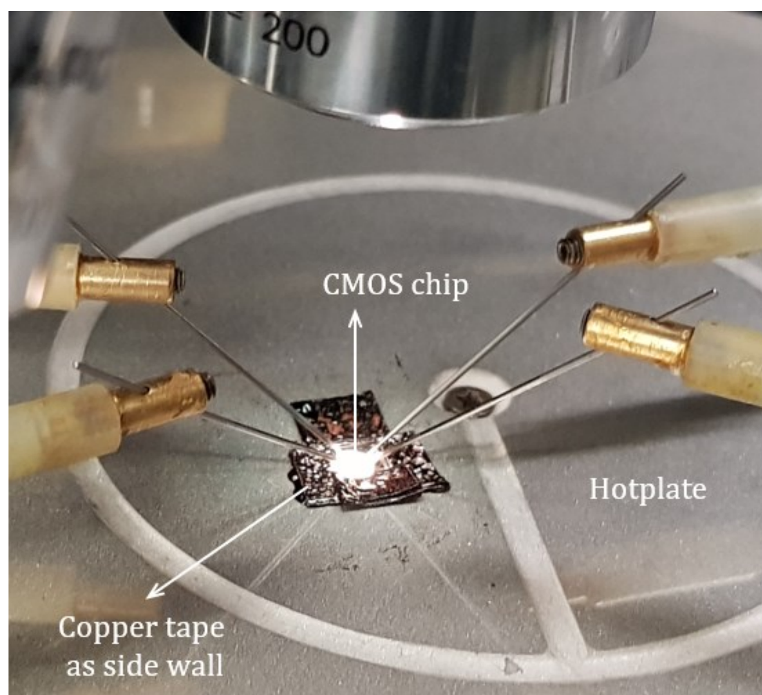


Figure 8.1: Experimental setup for four-point resistance measurements of polysilicon microstructures in a CMOS chip.

The CMOS chip was in direct contact with the hotplate ensuring high heat conduction. Copper tapes were used as walls to fix the position of the chip. The hotplate temperature was increased in steps of 25 ˚C using a remote-control system, which can reach a maximum of 400 ˚C. After changing the hotplate temperature, resistance measurements were taken after a certain duration to ensure stable temperature and proper heat transfer to the polysilicon layer. The resistance for each temperature point was measured when the resistance value becomes steady. The four-point dc resistance measurements were performed for both poly-1 and poly-2 reference microstructures.

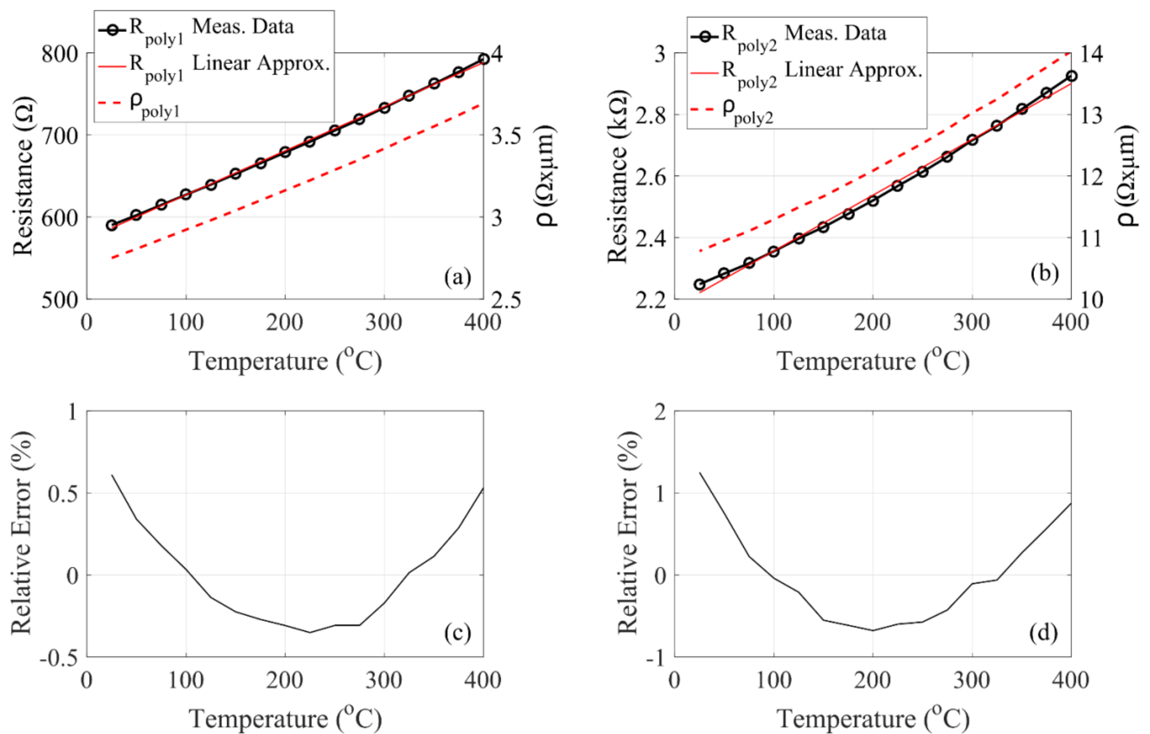


Figure 8.2: Resistance measurements of (a) poly-1 and (b) poly-2 microstructures at elevated temperatures along with calculated resistivity; relative error between the measured data of (c) poly-1 & (d) poly-2 and their linear approximation.

Figure 8.2 shows the static characteristic curves of these two resistors. Measurement results show that the relation between the resistance and the temperature of these two polysilicon resistors is linear within the measured range [25 ˚C, 400 ˚C]. Therefore, corresponding temperature of a resistance value can be easily obtained. Room-temperature resistance of the poly-1 and poly-2 microstructures from the four-point

measurements were ~590 Ω and ~2248 Ω, respectively. With the temperature rise of 375 ˚C, poly-1 resistance had an increase of ~200 Ω (*Figure 8.2a*), while poly-2 resistance was increased by more than 675 Ω (*Figure 8.2b*). Fluctuation in the resistance values were higher at elevated temperatures over 200 ˚C, possibly caused by thermo-emf variations. Also, at such high temperatures, the measuring probe tips sometimes lost connection with the contact pads, possibly due to the thermal expansion of the tungsten probe needles. Minor position adjustments of the probe tips with the probe positioners were sufficient to restore the connection.

Electrical resistivities of the structures are calculated through their dimensions. Poly-2 with around 4-times higher resistivity than poly-1 provides higher temperature sensitivity (~1.81 Ω/˚C) compared to poly-1 (~0.54 Ω/˚C) as calculated from *Figure 8.2*. The linearity of these two resistors was quantified by using a polynomial interpolation, which minimize the error between the data and the polynomial approximation in the least square sense. The relative error obtained from the linear resistance approximation is plotted in *Figure 8.2c* (poly-1) & *Figure 8.2d* (poly-2), which is within 1% for both sensors.

The polysilicon layers in the CMOS chip was covered with the dielectric layer, which provided thermal insulation and minimized heat loss by convection. Also, within the operated temperatures, heat loss due to convection and radiation are negligible for microstructures [238]. Silicon substrate and a thin silicon dioxide (SiO_2) film are the only layers between the reference polysilicon microstructure and the hotplate surface. Therefore, it is considered that the polysilicon resistor has similar temperature to the hotplate, since all measurements are taken after thermal equilibrium is reached. Silicon has high thermal conductivity of ~150 W/m.K at room temperature, which gradually reduces to one-third of this value at the maximum characterization temperature [331].

8.3 Sensor testing with on-chip microheaters

An identical CMOS chip was wire-bonded on a chip carrier, which was then placed inside a vacuum chamber to eliminate the effect of convection, and necessary electrical

connections were established by a feedthrough. The CMOS microheaters are at different distances from the temperature sensing polysilicon microstructures. A CMOS microheater was activated by joule heating, and the temperature on the heater was gradually raised by increasing the voltage stepwise with a source meter. During this operation, resistances of the two polysilicon temperature sensors were simultaneously monitored by four-point measurements.

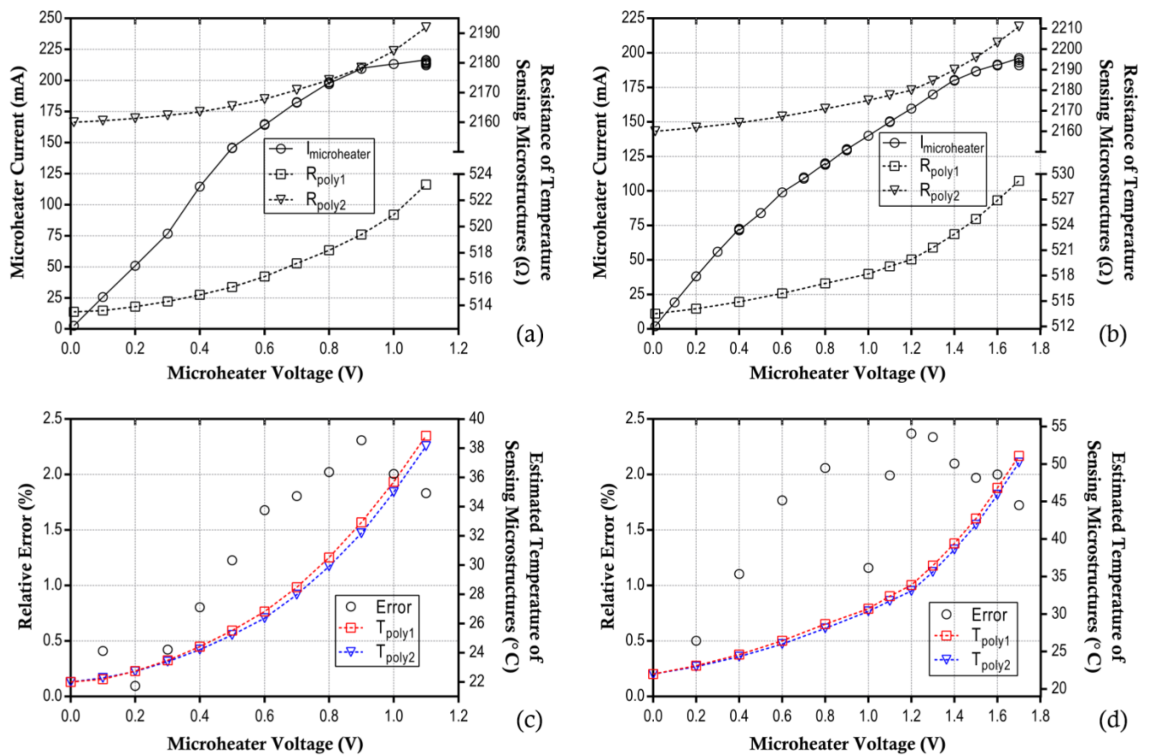


Figure 8.3: I–V curves of (a) M1A and (b) M1B metal microheaters with corresponding resistance measurements of the temperature sensors; estimated temperature by the two polysilicon sensors and the calculated relative error between them with (c) M1A and (d) M1B as heat sources.

Two different metal microheaters (M1A & M1B) located near the temperature sensing polysilicon microstructures were separately activated by joule heating. The microheaters are made of the top metal layer. Since the heaters were operated in a vacuum chamber, heat loss due to convection was avoided. During the high-temperature operation of a microheater, four-point resistance measurements were performed on both poly-1 & poly-2 temperature sensing microstructures. The I–V curve

of the heaters and the measured resistances of the temperature sensors at corresponding heater voltages are plotted in *Figure 8.3a* (for M1A) and *Figure 8.3b* (for M1B). Voltage of the metal microheaters was increased in steps of 0.1 V. At each voltage point, the resistance measurements were acquired after 4-6 minutes to provide sufficient time for transferring heat from the microheater to the temperature sensors and reach thermal equilibrium. M1A and M1B microheaters were broken after an increase in voltage beyond 1.1 V & 1.7 V respectively. Local temperature on the hottest spot of the heaters at the breaking voltages are estimated to be near the Al melting temperature (~660 ˚C).

Room-temperature resistance of the poly-1 and poly-2 sensors were ~514 Ω & ~2160 Ω, respectively. The resistance values increased by ~10 Ω (poly-1) and ~30 Ω (poly-2) when the M1A microheater reached the maximum temperature. For the maximum temperature of M1B microheater, the increase in resistance values were ~16 Ω (poly-1) and ~50 Ω (poly-2). The measured resistance values were used to estimate the corresponding temperature of the sensors based on the reference values plotted in *Figure 8.2*. M1A microheater has a surface area of 10 µm × 20 µm with maximum power consumption of ~240 mW, while M1B microheater has a surface area of 5 µm × 220 µm and maximum power consumption of ~335 mW. Depending on the surface area of these microheaters, the amount of heat conducted to the surrounding chip regions through the dielectric layer will differ.

For CMOS chips identical to the reference chip from *section 8.2*, the room-temperature resistance values of the temperature sensing polysilicon structures can have some variation from one chip to another. However, electrical resistivity values of polysilicon layers are considered to be similar over the manufactured CMOS chips, so the temperature on the sensing microstructures can be approximated from the sensitivity values obtained from reference microstructures in the previous section. These estimated temperature values corresponding to the measured resistance values are plotted in *Figure 8.3c* and *Figure 8.3d*, together with the relative error in temperature estimation through poly-1 and poly-2 sensors. The associated heat sources for the

temperature sensors in *Figure 8.3c* & *Figure 8.3d* are M1A and M1B microheaters, respectively.

At the maximum temperature of the metal heaters, the global temperature of the CMOS chip was raised to around or below 50 ˚C from the 22 ˚C room temperature. This value is consistent to the thermal measurement of a similar CMOS chip using infrared microscopy when a comparable metal microheater was operated at the maximum temperature, as presented in *section 3.5*. Maximum temperature estimated from the sensors due to the heat generation from M1A is ~12 ˚C lower than the M1B heat source. This is due to the 5.5 times lower surface area of M1A heater compared to the M1B heater causing lower heat loss in the surroundings, which is also reflected by the ~100 mW difference in power consumption at the maximum temperature of the heaters.

The calculated relative error reflects the difference in temperature estimation through poly-1 and poly-2 sensors. Temperatures on the regions of poly-1 and poly-2 sensing resistors should be similar since the metal microheaters are equidistant (~0.5 mm) from both of these polysilicon microstructures. However, the maximum temperature of the heaters can shift from the centre of the heaters due to the Thomson effect, which is more prominent when joule heating microstructures [313]. Therefore, the temperature near poly-1 and poly-2 sensors may slightly differ, which can contribute to the relative error between these two resistive temperature sensors.

The temperature sensors were also tested with two different polysilicon microheaters (P1A & P1B) as heat source. These microheaters are made by the poly-1 layer of the CMOS process, and covered with dielectric layer similar to the polysilicon temperature sensors. As a result, heat will conduct through all surfaces of the polysilicon heaters generating higher global temperature than the metal heaters, which only have dielectric contact at the bottom surface. *Figure 8.4a* and *Figure 8.4b* show the I–V curve of the P1A and P1B heaters respectively along with the corresponding four-probe resistance measurements of the temperature sensors. The P1A heater voltage is increased by a step of 1 V, while the voltage increment was 0.5 V for P1B heater due to its 3-times lower resistance than P1A.

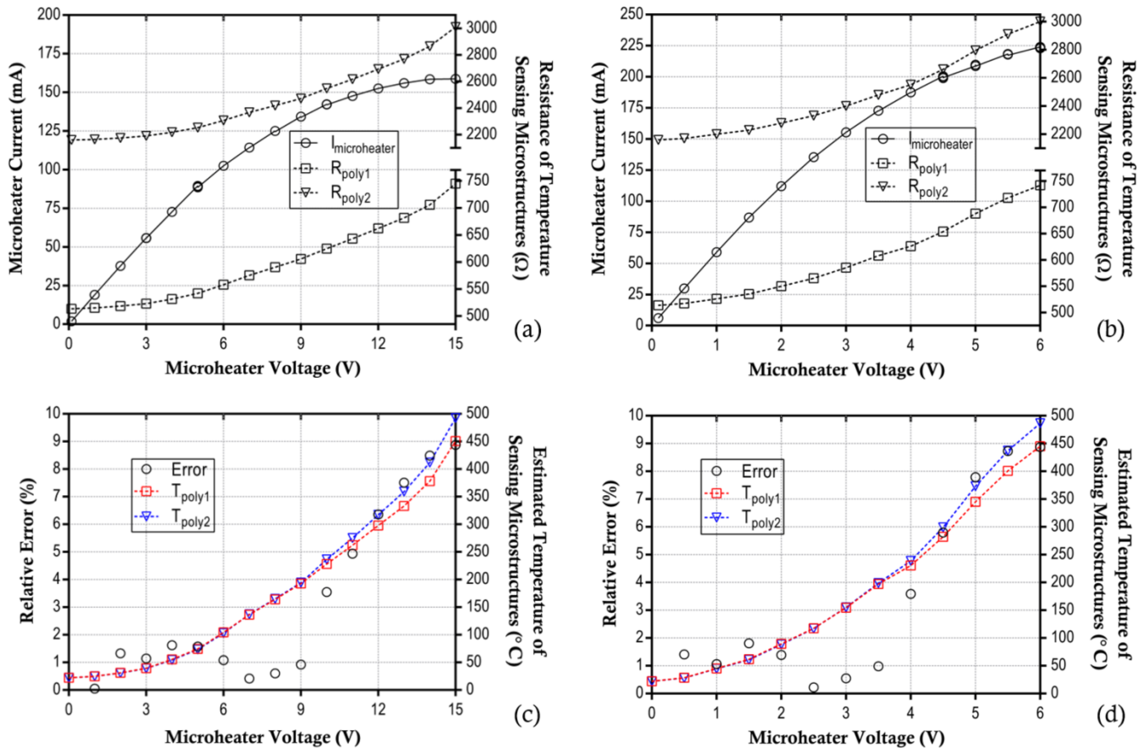


Figure 8.4: I–V curves of (a) P1A and (b) P1B polysilicon microheaters with corresponding resistance measurements of the temperature sensors; estimated temperature by the two polysilicon sensors and the calculated relative error between them with (c) M1A and (d) M1B as heat sources.

P1A heater has a surface area of ~40 µm × 250 µm with maximum consumed power of ~2.38 W. The heater melted when the voltage was increased beyond 15 V (*Figure 8.5*), indicating hotspot(s) of the heater reached Si melting temperature of ~1400 ˚C. Since the polysilicon heaters were buried with dielectric layer, they are mechanically stable at the high temperatures, unlike the exposed polysilicon heaters used for the CNT growth. Surface area of P1B heater is 95 µm × 155 µm, which consumed ~1.35 W power before breaking at a voltage above 6 V. Unlike P1A heater, P1B heater did not melt, as indicated by the heater appearance after the connection is broken. The cause of breaking can be due to thermo-mechanical stress. The maximum estimated surrounding temperature from the sensors are ~450 ˚C (poly-1) and ~490 ˚C (poly-2) for both P1A (*Figure 8.4c*) and P1B (*Figure 8.4d*) as heat sources. Distance of the heaters from the temperature sensors are ~1 mm (P1A) and ~0.4 mm (P1B). Although P1B has higher surface area and is closer to the temperature sensors than P1A, the prior heater did not spread more heat to the surroundings since it did not reach as high temperature as the latter heater.

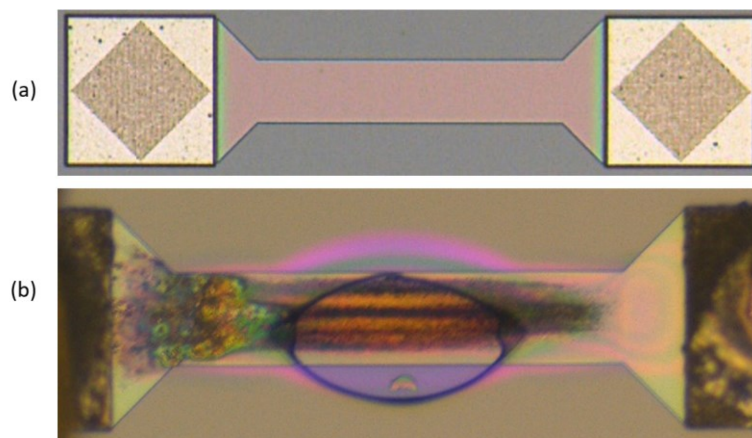


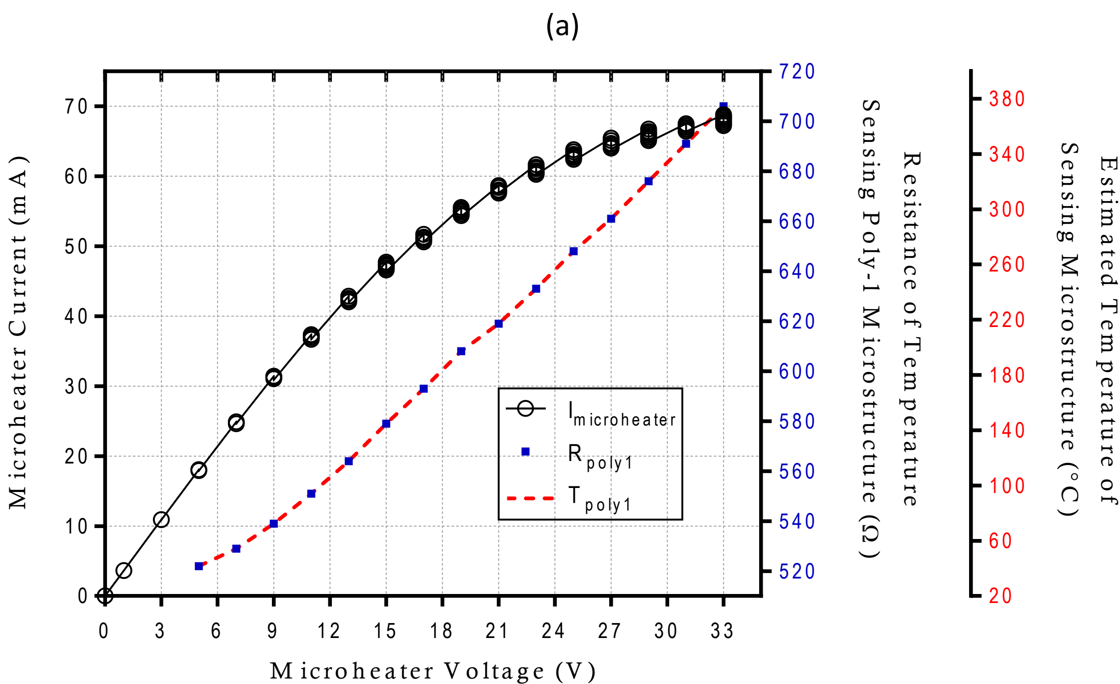
Figure 8.5: Dielectric covered P1A heater (a) before heating and (b) after heating to its breaking point.

CMOS-incompatibility can be determined if 4-point resistance measurement of the temperature sensors exceeds the threshold value (~400 ˚C) during the operation of a microheater. It should be noted that the maximum estimated temperatures in *Figure 8.4c* and *Figure 8.4d* are beyond the maximum reference temperature from *Figure 8.2*. Therefore, it can be decided that the polysilicon microheaters should be operated within 14 V (for P1A) and 5.5 V (for P1B) to maintain CMOS-compatible temperature on the chip.

For the four-point resistance measurements of the reference microstructures (*Figure 8.1*) at high temperatures, there were fluctuations in resistance values due to the lack of proper stable contact between the probe tips and microstructure contact pads. This was not an issue during the sensor testing experiments with microheaters as the sensing microstructures were wire bonded. The relative errors in *Figure 8.4c* and *Figure 8.4d* are higher (> 3%) beyond 200 ˚C, which corresponds to the higher instability in the resistance measurements of the reference polysilicon sensors beyond the same temperature in *section 8.2*. The temperature estimation from poly-1 and poly-2 sensors do not deviate more than 2 ˚C within the 200 ˚C temperature sensing range, while the deviation increases to ~40 ˚C at the highest approximated sensor temperatures. Therefore, these on-chip resistive polysilicon temperature sensors are more precise in estimating temperatures within 200 ˚C. Temperature sensors were also calibrated for four terminal aluminium microstructures; these results will be detailed in *Article 14*, along with further investigation on the resistive temperature sensing.

8.4 Effect of convection

Two identical microheaters (P2A) made of poly-2 layer were used as heat source to estimate the chip temperatures under vacuum and atmospheric condition using the poly-1 temperature sensor (*Figure 8.6*). The P2A heater has identical design to P1A. Under atmospheric condition, the P2A heater was active until 33 V consuming ~1.54 W before breaking; the estimated chip temperature from the poly-1 sensor was ~380 ˚C before the heater collapsed (*Figure 8.6a*). In comparison, the P2A heater in vacuum operated normally until 27 V, before a partial collapse occurred from 29 V (*Figure 8.6b*). Temperature after the partial heater breaking has been discussed in *section 8.5*. Without the heat loss through convection, the P2A heater in vacuum required lower power compared to the P2A heater operated in air pressure for generating similar temperatures; a comparison is made in *Figure 8.7*. For ~380 ˚C measured temperature by the sensor, the heater needed 1.5 times higher power in atmospheric environment than in vacuum. The surrounding temperature estimated by the sensor was similar for both air and vacuum conditions before the heaters were fully or partially broken as seen in *Figure 8.7*. It indicates that even though the power consumption to obtain similar heater temperatures will vary when microheaters are operated under vacuum and gas



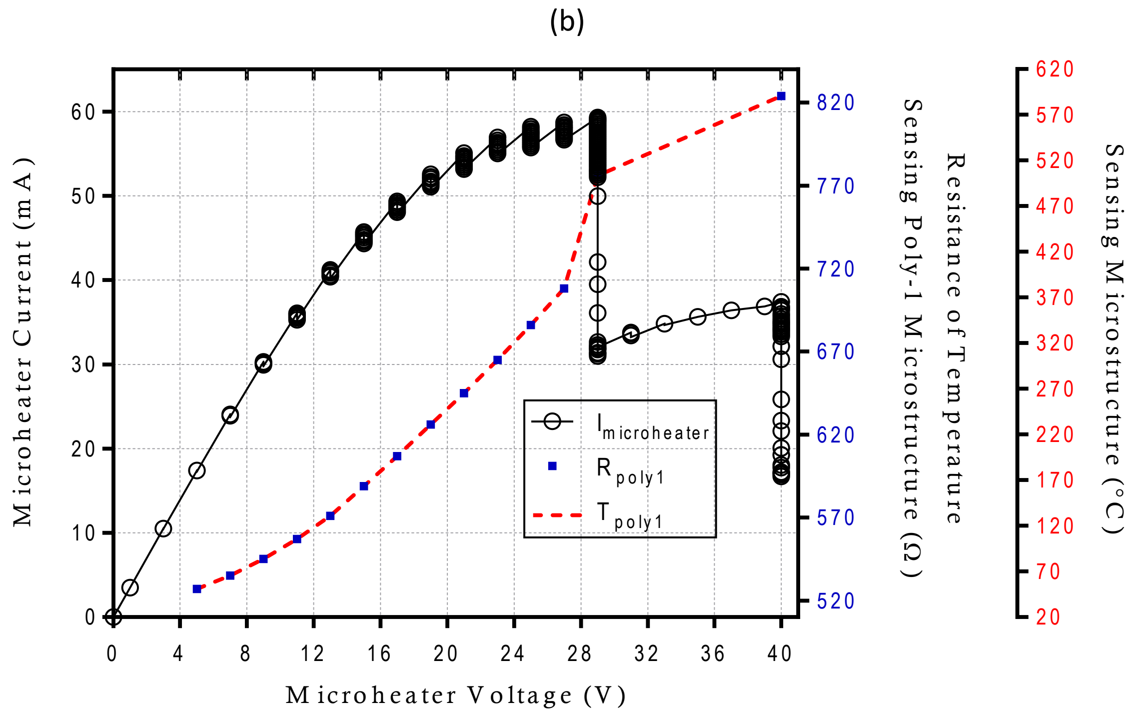


Figure 8.6: Electrical characteristics of identical P2A microheaters with corresponding resistance and estimated temperature from the poly-1 sensor under (a) atmospheric condition and (b) vacuum.

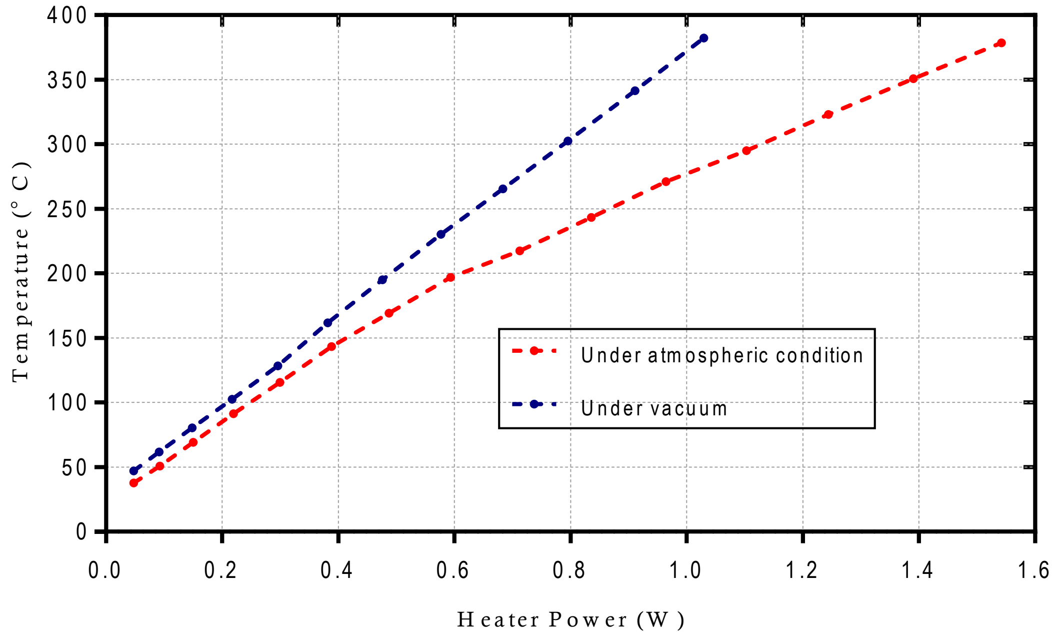


Figure 8.7: Power consumption of P2A microheaters in atmospheric and vacuum condition and corresponding temperature generated in the surroundings as estimated by the poly-1 sensor.

environment due to convection, the final temperatures on an unbroken heater will be similar in both conditions.

8.5 Effect of partially broken microheaters

During the CNT synthesis, several polysilicon microheaters were partially broken, where the heater current dropped rapidly but did not become zero as seen in *Figure 8.6b*. In such a state, it was possible to operate the heaters at a much higher power than in normal condition. Therefore, the generated temperature from these heaters were also higher than normal. Higher success in CNT growth has been found when heaters were partially broken. *Figure 8.8* shows low diameter CNTs grown on the partially broken region of a heater. The partially broken heater in *Figure 8.6b* sustained 40 V to generate ~2 W power that resulted in a temperature of ~ 600 ˚C measured by the sensor. Local melting in polysilicon can cause low-resistance path [309], which can enable the higher power operation of heater.

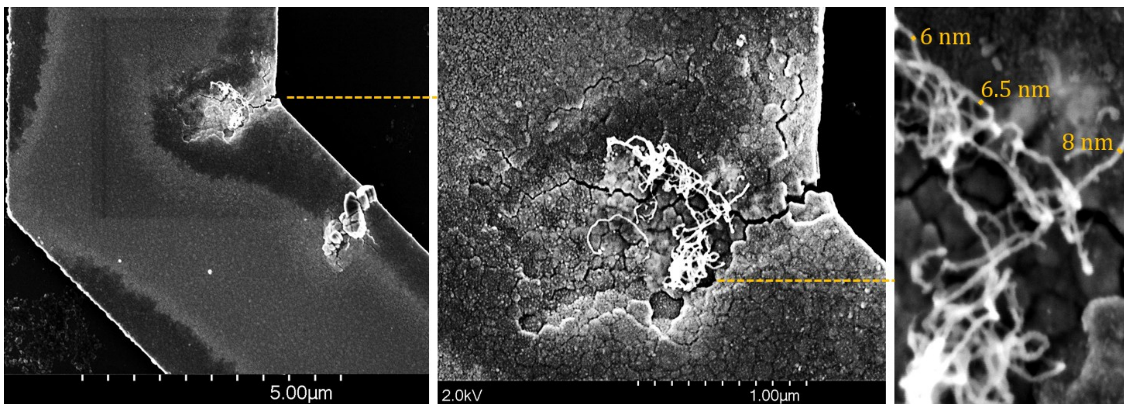


Figure 8.8: CNT growth on the partially broken region of a polysilicon microheater.

8.6 Effect of CMOS microheaters on transistor characteristics

High CNT growth temperatures on the CMOS-MEMS microheaters are only needed during the synthesis process which takes around 5–10 minutes. After CNTs are synthesized, the device can work at room temperature. Unlike typical semiconducting gas sensors [332–334], CNT based gas sensors do not need high temperature during operation. Therefore, once CNTs are grown on the CMOS chips under CMOS-compatible conditions, the ICs will no longer be exposed to high temperatures.

High thermal gradient is crucial to obtain CMOS-compatible temperature when growing CNTs on the CMOS-MEMS heaters. PMOS transistors were found to be more susceptible

to high temperature exposure during a thermal CVD process [233]. Therefore, two identical PMOS transistors (T1 and T2) with 1 µm × 1 µm channel have been characterized after heat exposure from different microheaters. As the non-suspended heaters produce more heat to the surroundings, we only tested them. For more risky case scenarios, heaters covered with dielectric layer were chosen as they obtain higher temperatures and spread more heat in the surroundings as discussed in *section 8.3*.

Four polysilicon microheaters (H1, H2, H3 & H4) with different surface areas were chosen. The transistors were characterized before exposing to the heaters and after operating each heater until its breaking point. The heaters were operated in the order of their surface area. Since higher surface area corresponds to higher global temperature and riskier condition for the transistors, the tests started with H1 due to its low surface area, followed by H2, H3 and H4. The T1 transistor collapsed after heat exposure from H4, while the T2 transistor survived exposure from all heaters. A summary of the performed tests is shown in *Table 8.1*. Position of the heaters and transistors are marked in *Figure 4.9*.

Table 8.1: Summary of transistor condition upon heat exposure from different polysilicon microheaters**.**

	H1	**H2**	**H3**	**H4**
Break Voltage (V)	9.9	34	26	20.5
Break Power (mW)	1100	1765	2030	1825
T1 status*	OK	OK	OK	Collapsed
T2 status*	OK	OK	OK	OK
T1/T2 distance (mm)	~ 1 / 1.5	~ 1.6 / 2	~ 1.6 / 1.9	~ 1.4 / 1.8

* OK refers to similar transistor I/V characteristics to the reference condition (before exposure to heaters)

The T1 transistor characteristics before any heater exposure and after maximum heat exposure from H3 heater is compared in *Figure 8.9a*. No significant change in the transistor current behaviour was found. However, the transistor was broken when

measured after heat exposure from H4 heater as shown in *Figure 8.9b*. This heater is marked as ‘secondary polysilicon microstructure’ in *Figure 3.12c*, and CNT growth results on identical heaters have been shown in *Figure 5.16*. This is also one of the heaters that caused melting in the aluminium contact pads (*Figure 7.7*). CNT growths have been found in the nearby Si substrate region of a heater with comparable surface area as shown in *Figure 8.10*, which indicates the high surrounding temperature generated from such heaters.

Characteristics of the T2 transistor was also compared after it was exposed to the maximum temperature from the H4 heater as shown in *Figure 8.11*. T2 retained its current behaviour. Although the two transistors are identical, they have ~500 µm distance between them. In most cases, the T1 transistor was closer to the heaters (*Figure 4.9*). Hence, T1 was exposed to more heat than T2, which can be the reason why the latter survived all heater tests. High temperatures can induce diffusion of the dopants. Exposure to such high temperatures for longer duration can cause significant dopant diffusion that can result in characteristic changes of the transistor behaviour and consequent failure of the device. This can be a potential reason for the breakdown of the T1 transistor.

Among the four tested heaters, H1 was the nearest to the T1 transistor, which confirms ~1 mm keep-out zone for the electronics from the heater. However, the keep-out is expected to be much shorter, especially for the heaters with lower surface area. The simulation results in *Figure 2.5, 2.6 & 2.10* provide an indication that the keep-out zone can be as short as 10 µm for smaller heaters.

The H4 heater has much higher surface area than majority of the CMOS-MEMS heaters used for CNT synthesis. Moreover, the exposed CMOS-MEMS heaters have higher thermal gradient around them compared the unexposed heaters used in the transistor tests. The thermal isolation is even higher for the partially or fully suspended microheaters. Therefore, it can be concluded that majority of the fabricated CMOS-MEMS heaters can successfully generate local CNT synthesis temperature with high thermal isolation to ensure CMOS-compatible temperature for the ICs.

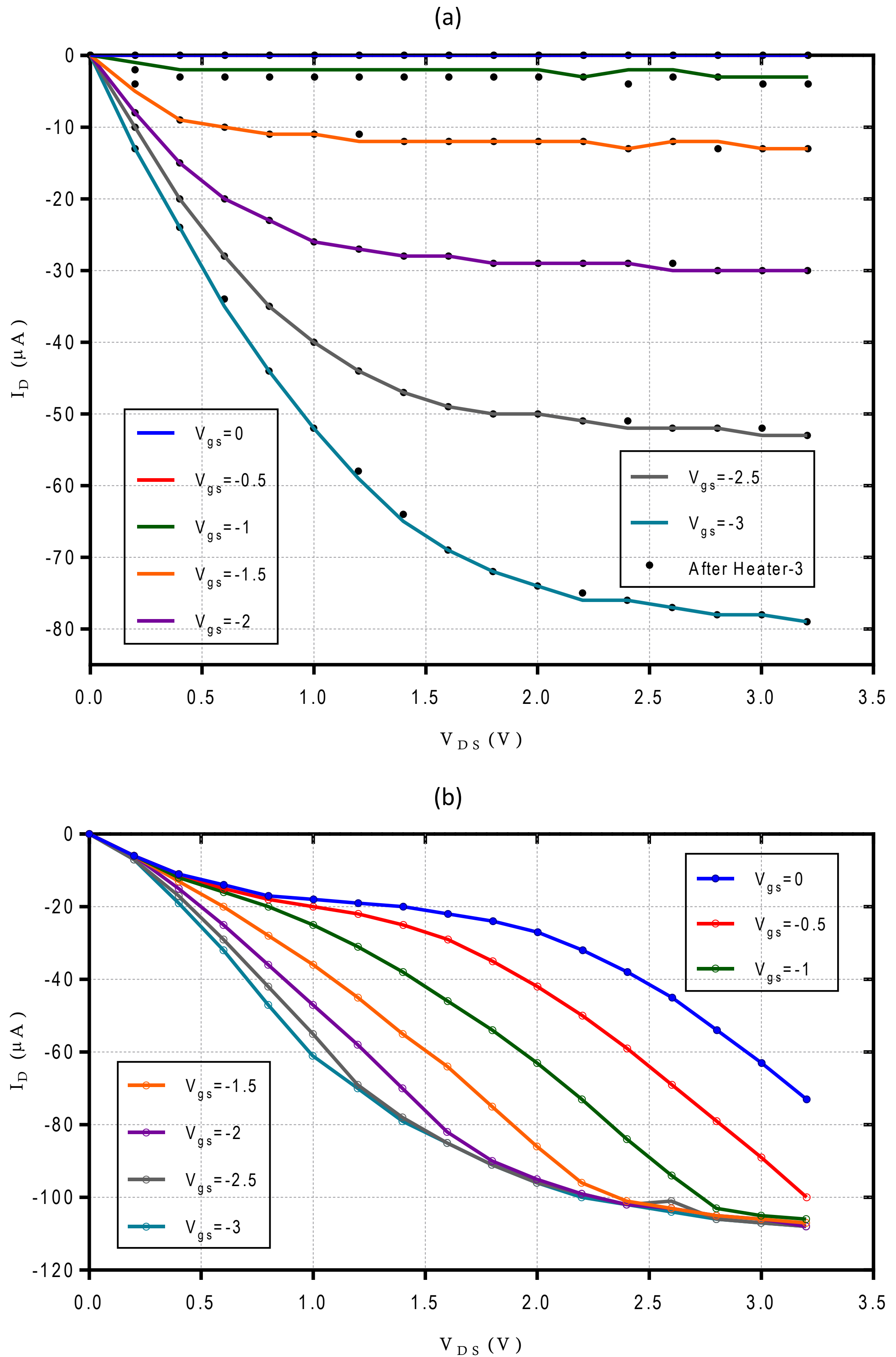


Figure 8.9: I-V characteristics of transistor, T1. (a) Initial characterization before any heat exposure vs after heat exposure from heater, H3; (b) Characterization after heat exposure from heater, H4.

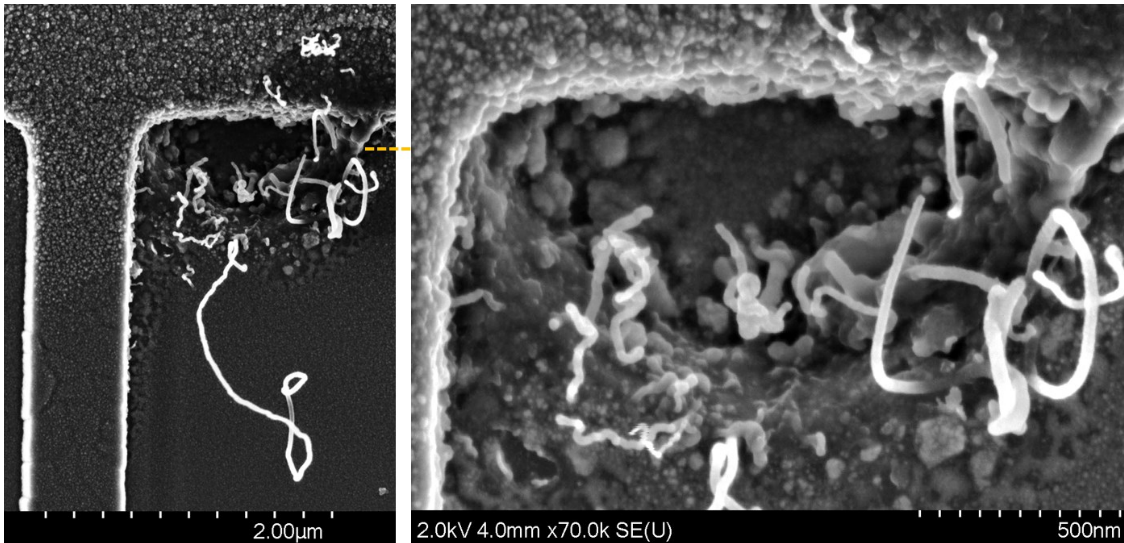


Figure 8.10: CNTs grown on neighbouring silicon substrate of a microheater with high surface area.

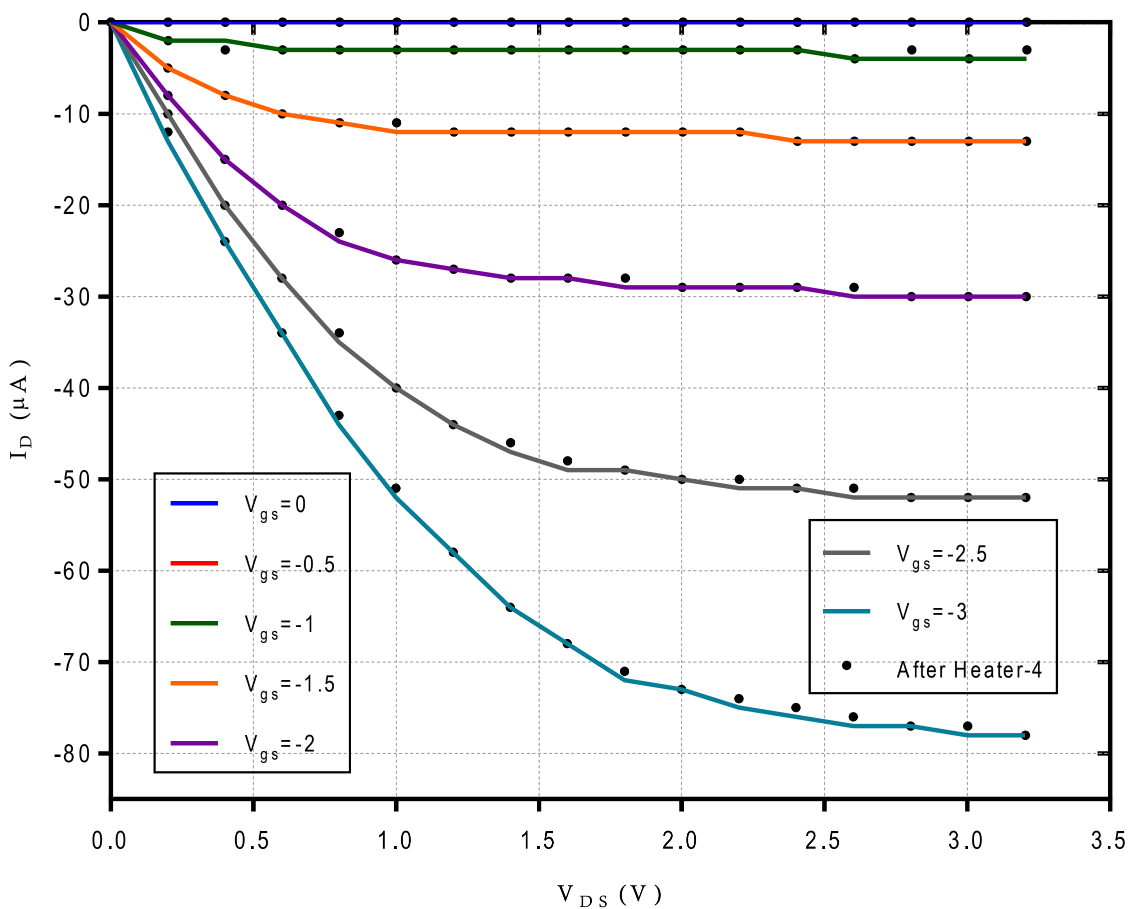


Figure 8.11: I-V characteristics comparison of transistor, T2 between initial characterization before any heat exposure and after heat exposure from heater, H4.

8.7 Conclusion

Polysilicon microstructures with four terminals were used to demonstrate on-chip temperature sensing. Electrical characterization of these microstructures was performed within 25 to 400 ˚C for using four-probe resistance measurement. The sensors were tested with in-built CMOS microheaters as heat source. For measuring temperatures below 200 ˚C, the two sensors using poly-1 and poly-2 have relative errors below 2.5%, while the error increases to 9% when higher temperatures (200 - 500 ˚C) are measured. I/V characterization of transistors were performed after exposing them to the heat generated from non-suspended CMOS-MEMS heaters when they were operated at CNT synthesis temperatures. The results ensured that CMOS-compatible ambient temperature can be achieved during CNT growth for most microheaters.

Chapter 9

Conclusion

9.1 Outcome and outlook

This thesis outlined the development of a process to locally synthesize carbon nanotubes on a low-cost commercial bulk CMOS technology to utilize the potential of this nanomaterial in sensing applications. In the developed process, CMOS-MEMS microheaters were fabricated by post-CMOS processing, where CNTs were grown using local thermal CVD in a low ambient temperature ensuring CMOS-compatibility. CNT-based sensing applications were demonstrated along with temperature estimation using CMOS microstructures. The developed monolithic CMOS-CNT integration process has the potential for transferring to a wafer-level process with minimum modification in standard inexpensive foundry CMOS process.

Microheater designs were simulated using the suitable materials available in standard CMOS process to check the feasibility of reaching CNT synthesis temperature (~900 °C) by local resistive heating, while keeping the CMOS circuits below 300 °C. Polysilicon is the most suitable heater material in CMOS, while the metal options (Al or Cu) needed alloying for the high-temperature application; Ni was identified as the most suitable alloy material. Tri-nickel aluminide and cupronickel (70% Cu–30% Ni) were chosen as the alloys from the investigated materials. Thermal analyses of the simulated microheaters show that they can generate CNT synthesis temperature, while having a high thermal gradient around them. Some non-suspended and most partially suspended heaters provided sufficient thermal isolation for CMOS compatibility. The results show that electronic circuits can be placed only tens of micrometres away from the microheaters as the temperature drops sharply around the heaters. It indicates a very small keep-out zone, which is important to reduce the size of the CMOS chips for producing low-cost CNT-based sensors.

CNT growth structures were designed and fabricated in a standard AMS 350 nm CMOS process, using aluminium and polysilicon layers. Numerous microheaters were designed with various features to facilitate post-processing and CNT-CMOS integration. Passivation layers over the heater regions were avoided by layout design, hence, the top metal microheaters on the fabricated CMOS chips were already exposed, while the polysilicon microheaters were covered by dielectric layer. The subtractive post-CMOS SoC integration technique was used for fabricating the CMOS-MEMS heaters. The challenges with dielectric etching include achieving high aspect ratio for uniform etching with high selectivity and good etch rate. A two-step anisotropic dielectric etching process was developed, where an ICP-RIE process was used first to attain high aspect ratio followed by a RIE process when selectivity becomes most important. Proper CMOS chip design and post-processing approaches held the key of successfully realizing the CMOS-MEMS microheaters. Two generations of CMOS chips were designed and fabricated. The first-generation chip was designed with the maximum heater efficiency in mind, in which several design limitations were revealed during the post-processing. Uniform etching was further facilitated by design improvements in the succeeding generation CMOS chip. The design and dielectric etching process were also improved for minimizing damages on the metal layers and associated issues to the damages. Microheaters were also suspended (fully or partially) on some CMOS chips by wet etching with pad-etch recipe. A single continuous wet etching process is preferred for the polysilicon microheater under-etching due to less damage on the metal contact pads. It was found that both non-suspended and suspended heaters can produce CNT growth temperatures while maintaining CMOS-compatible ambient temperature.

Despite a high demand for cheap gas sensors, there is still no low-cost commercial CNT-based sensors available in the market due to the challenges involved in CMOS-CNT integration. Currently, there is only one reported case of growing CNTs on the polysilicon layers of a bulk CMOS process, which involves extensive post-processing steps that limits the chance of low-cost sensor manufacturing. The post-CMOS processing along with CMOS chip design developed in this PhD work significantly reduces the complexities and steps. This is an important step towards a potential wafer-level compatible approach

that can be incorporated in a commercial CMOS foundry with less process development for the mass production of CNT-based sensors.

CNTs were successfully synthesized on different polysilicon CMOS-MEMS microheaters by local thermal CVD process. However, the heaters did not reach high CNT growth temperature, while temperature control was challenging due to thermal instability in polysilicon grain boundaries. Changing the catalyst to Ni from Fe significantly improved CNT growth yield. On average, Ni-based CNTs had smaller diameter (< 20 nm) than Fe-based growth. Stacked poly-1 – poly-2 heaters provided good growth results on a more consistent basis due to their higher thermo-mechanical stability. CNTs were grown on partially and fully suspended microheaters, where power consumption is less due to lower heat loss, but temperature control is more difficult due to increased thermo-mechanical stress. Including H_2 etching gas in the synthesis process improved growth quality, but further development is needed. Shorter CNTs (< 10 µm) grown on adjacent microheaters could establish connection between the heaters through Si substrate; gas and pressure sensing has been demonstrated using such a connection.

On-chip temperature sensing was demonstrated using four terminal CMOS microstructures. In this temperature sensing approach, complex measurement setup and electronic circuits for signal processing are avoided. Two sensors made of poly-1 and poly-2 were used to estimate the temperature on ASICs with less than 9% relative errors between the range [200 ˚C, 500 ˚C], while a better precision is achieved with relative errors lower than 2.5% in the range [22 ˚C, 200 ˚C]. Two transistors were characterized after exposing to heat from non-suspended heaters with different surface area in stricter scenarios. The results confirmed CMOS-compatibility in almost all cases.

The accomplished results of local CNT synthesis on CMOS-MEMS structures in CMOS chips can be transferred to a wafer-level process, which shows potential for the mass manufacturing of compact low-cost CNT-based smart sensors. The modified processes required for the CNT synthesis can be incorporated with an existing foundry CMOS technology. Therefore, with further development, the utilization of CNTs in commercial sensing applications is promising.

9.2 Recommendations and further work

For direct CNT growth on CMOS structures, some modifications on the CMOS layers are desirable. Due to the thermal instability of polysilicon, thicker polysilicon layer with phosphorous doping is preferred for the microheaters to use in high temperature applications. Doping can be tuned to provide negative TCR near optimum CNT growth temperature for the ease of electrical control. Thicker dielectric can be used beneath the polysilicon layers to minimize stiction possibility if heaters are suspended. It is recommended to increase the passivation layers since the RIE process for dielectric etching can affect its final thickness. The passivation layers can be removed in a smaller region where the heaters are exposed for CNT synthesis.

In-depth analysis of the synthesized CNTs using Raman spectroscopy is beneficial for further development of the CNT growth process and sensor performance. Quality and defects of the deposited CNTs can be analyzed with Raman to study the growth limitations. As CNT defects are influential in gas absorption, detail study on the CNT structures will be effective for performance improvement of the sensors.

Among the current CMOS-MEMS heaters, stacked poly-1 – poly-2 heaters are preferred due to their thickness advantage. Longer and narrower heaters were more challenging to grow CNTs as these heaters break more abruptly. Although most heaters could be operated at low ambient temperatures, heaters with high surface areas should be avoided. For catalyst, Ni is a preferred choice compared to Fe based on the obtained heater temperatures. CNT growth with other catalysts such as Mo-Al-Co can be investigated. CNTs synthesized on the CMOS-MEMS heaters were mostly short; adding etching gas (H_2) in the synthesis process showed promise for longer CNTs with better quality. Ratios between the synthesis gases should be tuned for optimum growth results.

Appendix

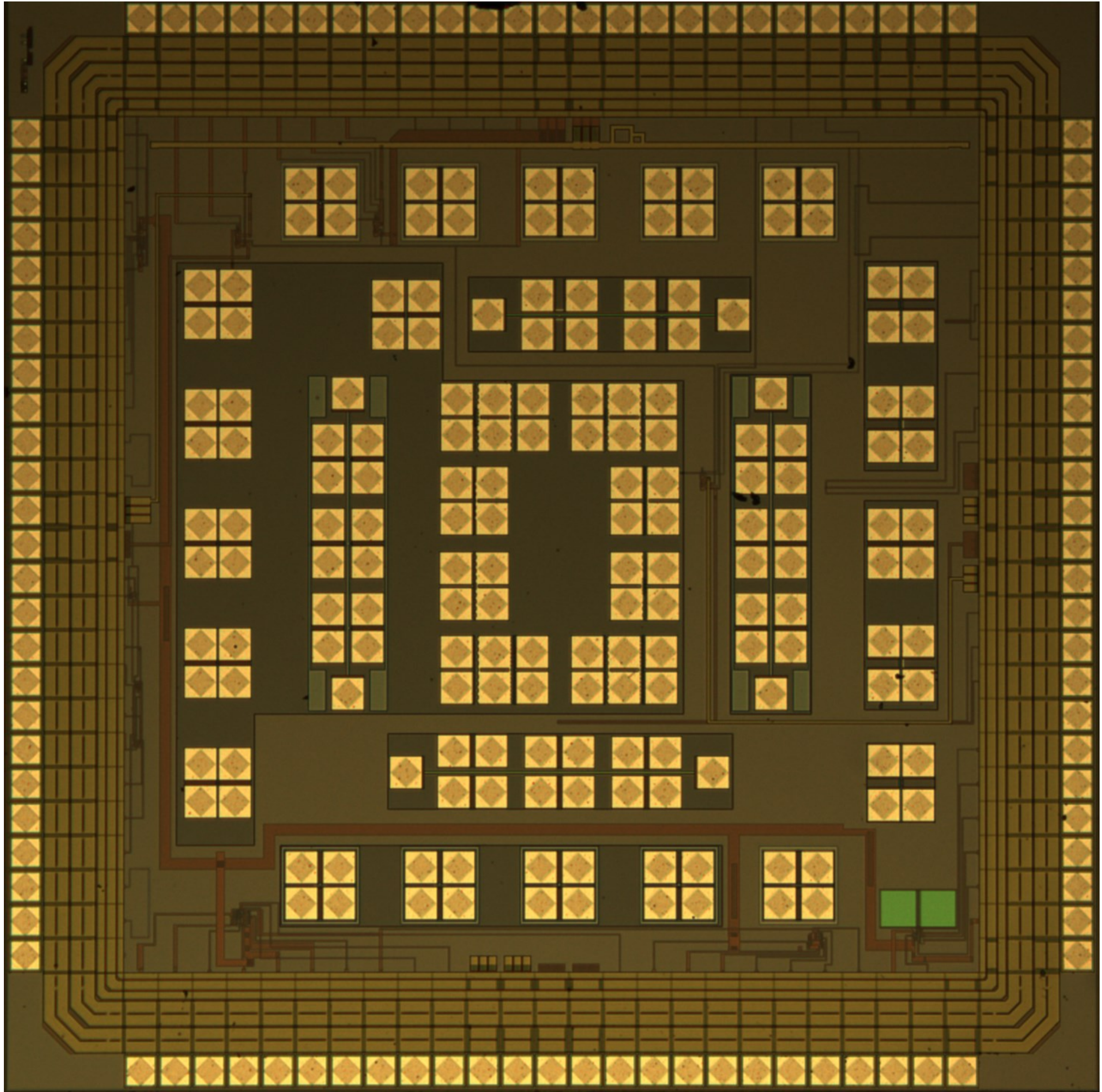


Figure A1: First generation CMOS chip for CNT synthesis.

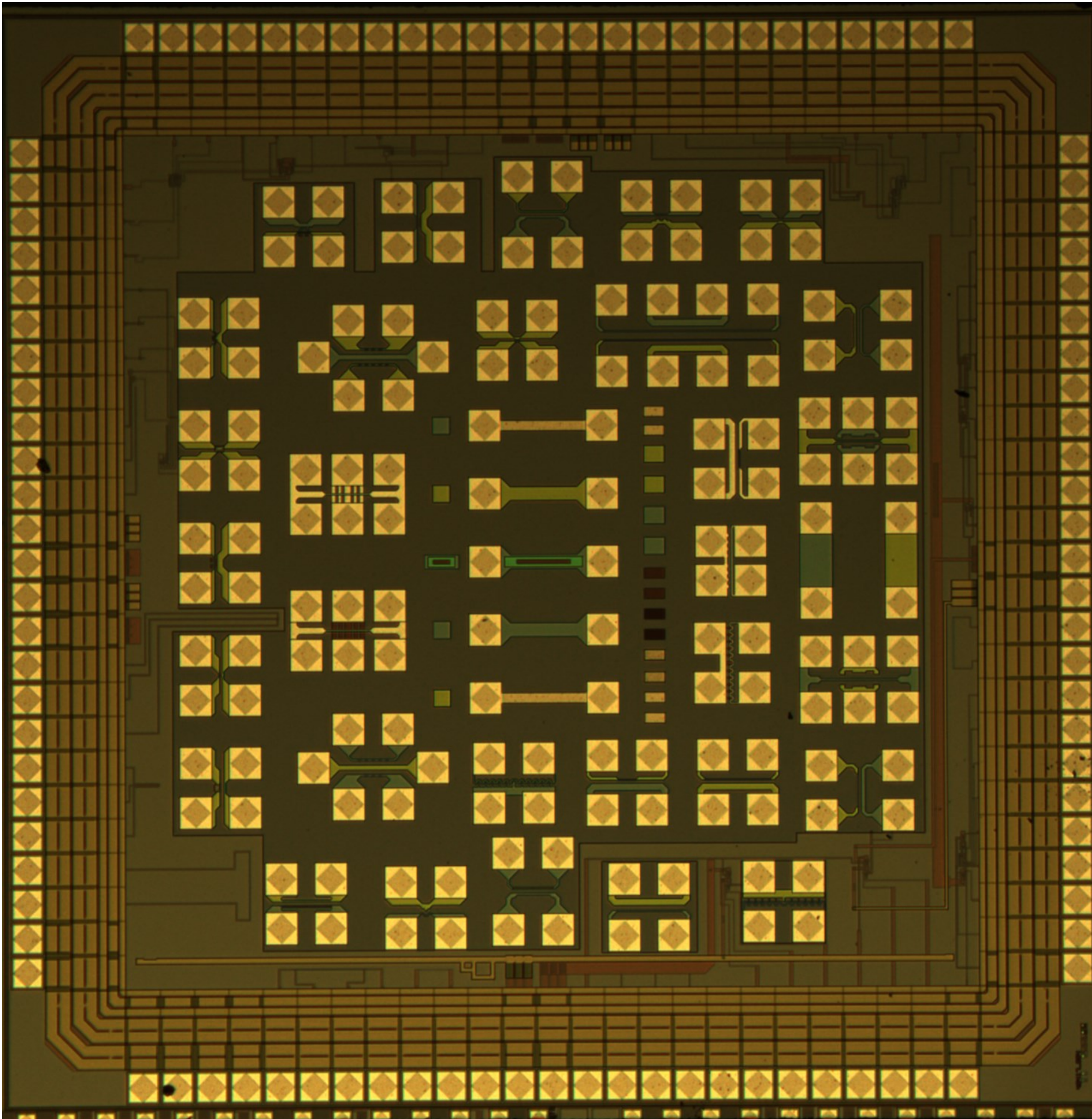
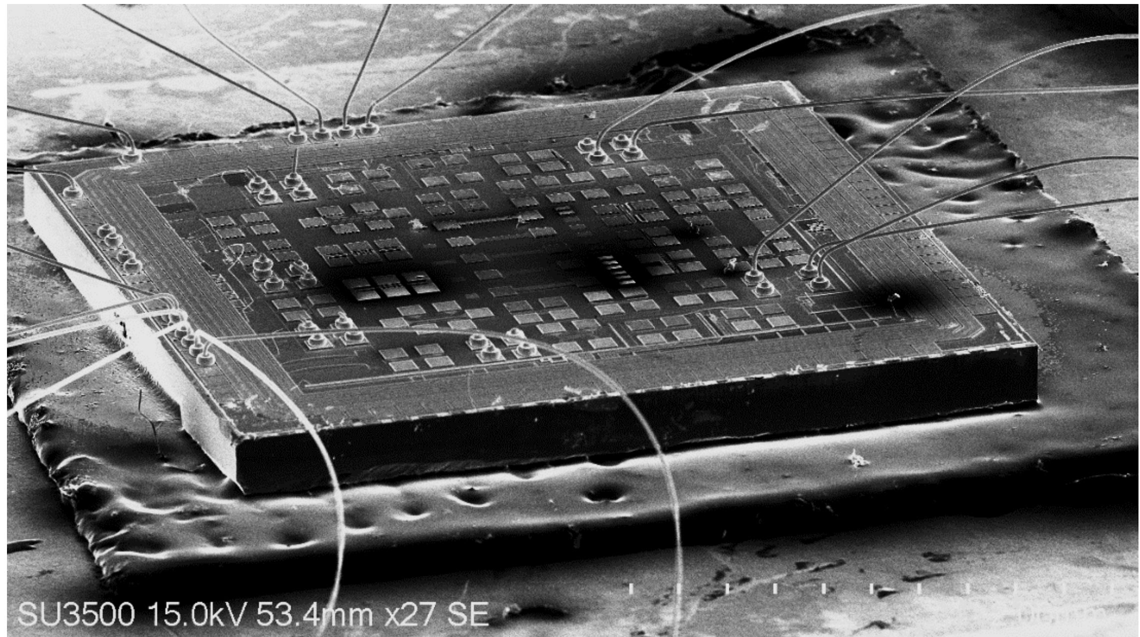


Figure A2: Second generation CMOS chip for CNT synthesis.



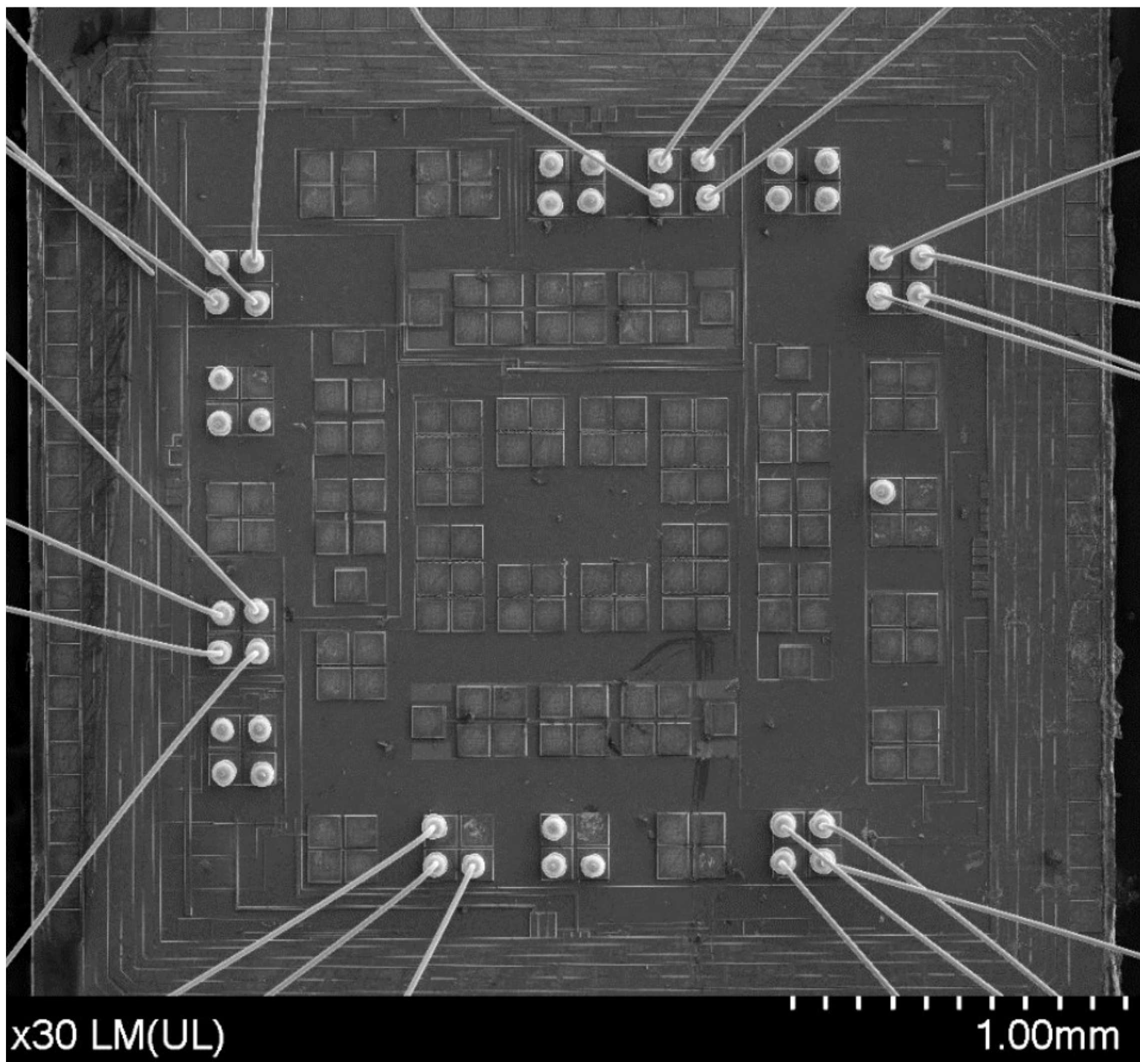


Figure A3: Wire bonded microheaters on CMOS chips.

Table A.1: Summary of results from different SiO_2 dry etching recipes.

Etching recipe	Ar flow rate (sscm)	CHF_3 flow rate (sscm)	O_2 flow rate (sscm)	RF power (W)	ICP power (W)	Pressure (mTorr)	Sample holder temperature (˚C)	Etch Rate (nm/min)	Selectivity* (Qualitative)
R1	15	10	0	20	600	3	0	~70	G
R2	95	15	0	30	1500	20	0	~125	P
R3	95	15	0	300	1000	20	0	~110	G
R4	95	15	0	300	600	20	0	~105	G
R5	95	15	0	300	400	20	0	~85	G
R6	33	17	0	50	1500	10	0	~130	P
R7	38	12	0	80	1500	10	0	~160	P
R8	38	12	0	40	400	10	0	~75	G
R9	38	12	0	80	800	10	0	~105	G
R10	95	15	5	300	0	20	0	~35	P
R11	95	15	2	300	0	20	0	~35	G
R12	95	15	0	300	0	20	0	~30	E
R13	95	15	2	300	0	20	20	~35	G
R14	95	15	0	300	0	20	20	~30	E

* Selectively of Si:SiO_2 is considered poor (P) for a ratio of 1:2 (or lower), good (G) for a ratio higher than 1:2, and excellent (E) when Si etching is very low to quantify

Table A.2: Summary of major equipment used in this thesis.

Application	Equipment	Model	Location
Bonding	Wire-bonder (Ball)	Delvotec 5610, F&K	USN, NO
Characterization	Profilometer	Dektek 150	USN, NO
Characterization	Profilometer	KLA-Tencor P7	UIC, USA
Characterization	Optical Microscope	Leica DM4000M	USN, NO
Characterization	Optical Microscope	Leica DM3 XL	USN, NO
Characterization	Optical Microscope	Zeiss V12	USN, NO
Characterization	IR Microscope	FLIR A6750sc MWIR	UIC, USA
Characterization	SEM	Hitachi SU 3500	USN, NO
Characterization	FE-SEM	Hitachi SU 8230	USN, NO
Characterization	AFM	XE-200, Park Systems	USN, NO
Characterization	Probe Station	450PM, Micromanipulator	USN, NO
Characterization	Probe Station	Micromanipulator	UIC, USA
Characterization	Ellipsometer	Alpha SE, J. A. Woollam	USN, NO
CNT Synthesis	CVD	USN Custom-built	USN, NO
Deposition	Electroplating	USN Custom-built	USN, NO
Deposition	E-beam	ATC 2030-HY, AJA	USN, NO
Deposition	Sputtering	ATC 2030-HY, AJA	USN, NO
Etching	DRIE	Plasmalab System 100	UIC, USA
Etching	ICP-RIE	Mini-lock Phantom III	UIC, USA
Etching	ICP-RIE	PlasmaPro 100 Estrelas	USN, NO
Etching	Plasma Cleaner	AL 18, Alpha Plasma	USN, NO
Sample Preparation	Ion Milling	Hitachi IM4000	USN, NO
Chip Design	Software	Cadence Virtuoso	USN, NO
Control System	Software	LabVIEW	USN, NO
Simulation	Software	ANSYS	USN, NO
Simulation	Software	COMSOL	USN, NO

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Article 1

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Article 2

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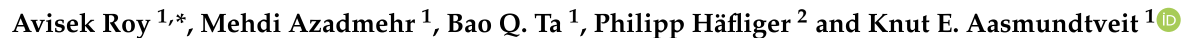
Design and Fabrication of CMOS Microstructures to Locally Synthesize Carbon Nanotubes for Gas Sensing



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Abstract: Carbon nanotubes (CNTs) can be grown locally on custom-designed CMOS microstructures to use them as a sensing material for manufacturing low-cost gas sensors, where CMOS readout circuits are directly integrated. Such a local CNT synthesis process using thermal chemical vapor deposition (CVD) requires temperatures near 900 °C, which is destructive for CMOS circuits. Therefore, it is necessary to ensure a high thermal gradient around the CNT growth structures to maintain CMOS-compatible temperature (below 300 °C) on the bulk part of the chip, where readout circuits are placed. This paper presents several promising designs of CNT growth microstructures and their thermomechanical analyses (by ANSYS Multiphysics software) to check the feasibility of local CNT synthesis in CMOS. Standard CMOS processes have several conductive interconnecting metal and polysilicon layers, both being suitable to serve as microheaters for local resistive heating to achieve the CNT growth temperature. Most of these microheaters need to be partially or fully suspended to produce the required thermal isolation for CMOS compatibility. Necessary CMOS post-processing steps to realize CNT growth structures are discussed. Layout designs of the microstructures, along with some of the microstructures fabricated in a standard AMS 350 nm CMOS process, are also presented in this paper.

Keywords: carbon nanotube; local CNT synthesis; CMOS–CNT integration; microstructures; microheater; CMOS-compatible temperature

1. Introduction

Nanomaterials are a popular research topic as sensing materials for various sensing applications [1–3], including gas detection [4–8], due to their compact size [9], high sensitivity [10], low operating temperatures [11], low power consumption [12], etc. Among different nanomaterials, carbon nanotubes (CNTs) offer a very high surface-to-volume ratio [13], as well as exceptional material properties, including mechanical strength [14], metallic or semiconducting electrical conductivity [15], and high thermal conductivity [16] that facilitates CNTs in diverse applications [17–21]. Electrical properties of CNTs are easily influenced during interaction with different gas molecules [10], making these carbon-based nanomaterials an excellent candidate for ultra-sensitive gas sensing. Moreover, functional materials such as Pd and Pt can be deposited on CNTs [22] to enhance their sensitivity and selectivity to various gases, such as NO_2, NH_3, CO and O_2 [23,24]. A CNT-based gas sensor can have small form factor, while it can sense gases even at low concentration exposure at room temperature. Such a sensor is beneficial to numerous applications, including in the food-packaging industry, where the freshness of the food can be monitored by sensing released gases due to food degradation.

To utilize the functionalities of CNTs in smart gas-sensing applications, high-quality, low-noise CMOS front-end circuits are required for signal conversion and processing. A compact gas sensor containing CNTs as sensing material and CMOS readout circuits needs a standard process for direct CNT–CMOS integration. CNTs were already directly synthesized on MEMS structures, as demonstrated by Englander et al. [25], back in 2003. A similar approach can be used to grow CNTs on CMOS structures [26]. Figure 1 illustrates the process of local CNT synthesis on microstructures. The CNT growth structure (microheater) is locally heated by joule heating to generate temperatures in the region of 900 °C. A pre-deposited thin catalyst layer (iron in our process) on the microheater breaks into nanoparticles at such high temperatures, while a carbon-containing precursor gas enters the chemical vapor deposition (CVD) chamber. CNTs start to grow on the microheater when the precursor gas interacts with the catalyst nanoparticles. An electric field set between the CNT growth structure and another neighboring microstructure guides the growing CNTs toward that nearby secondary microstructure. A circuit containing CNTs as variable resistor is formed once the CNTs land on the secondary microstructure. Such a system can potentially work as a gas sensor, since the change in CNT electrical properties can be monitored upon exposure to certain gases.

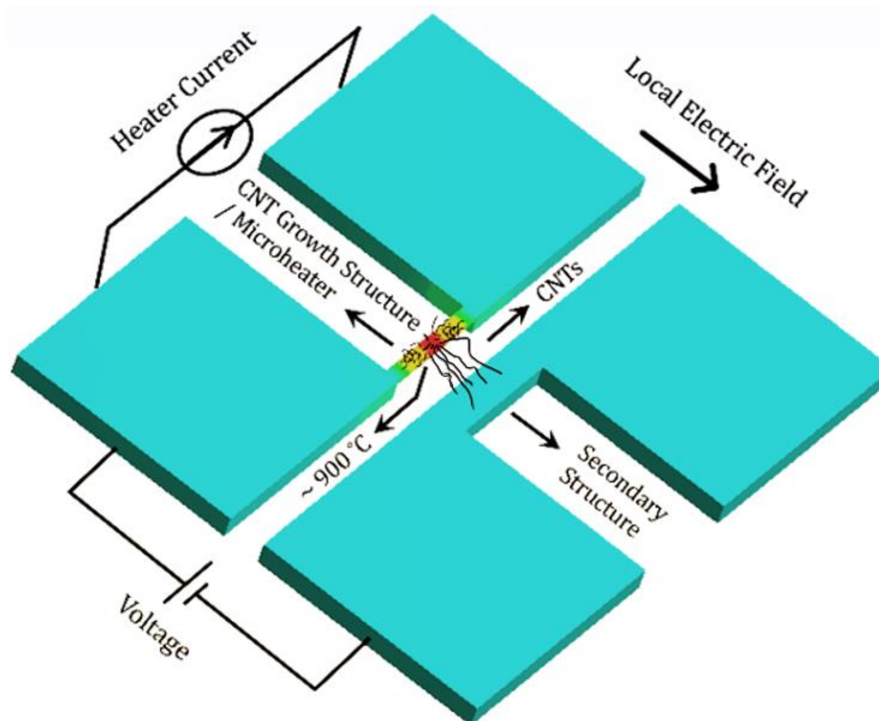


Figure 1. Concept illustration of local carbon nanotubes (CNT) synthesis on microstructures.

CNT–MEMS integration acts as a model system for CNT–CMOS integration. CMOS and MEMS technologies have clear similarities, but demonstration of direct CNT integration in CMOS involves a more complex process than in MEMS. Alternatively, CMOS chips can be assembled with CNT–MEMS to demonstrate the ultimate goal of a single chip with sensing and signal-processing capability. However, MEMS–CMOS assembly adds cost and processing steps, which are not compatible with low-cost mass production.

The main challenge for directly growing CNTs in CMOS chips is the high contrast in temperature, since CNT synthesis using our localized CVD process needs around 900 °C, whereas CMOS circuits are at risk to be degraded at temperatures above 300–400 °C [27–29]. Therefore, it is important to grow the CNTs locally and keep the CNT growth microstructures thermally isolated. In MEMS, CNTs are directly synthesized on a suspended microstructure by local resistive heating during the CVD process [25,30,31]. However, industrial CMOS fabrication platforms do not allow fabricating

suspended structures. For full or partial suspension of any CMOS microstructures, post-processing steps need to be introduced on the CMOS chips.

CNTs can also be synthesized separately at a high temperature and then transferred to the microsystem for integration. Since the CNTs are grown separately, the high temperature requirement for the growth along with other post-growth processes, such as purification or chemical modification, does not have any restrictions in this technique. Among post-growth CNT integration schemes, liquid deposition methods, including dielectrophoresis (DEP) [32] and dip coating [33], are well-known. In general, liquid suspension techniques lack good bonding between the substrate and the nanostructures, and there are possibilities of contamination and sacrificing electrical properties during the protracted process steps [34]. They also often suffer from issues related to non-uniform CNT assembly and misalignment [32,35]. Therefore, it is challenging to realize a reliable and repeatable technique of transferring and assembling CNTs to the microsystem.

In a recent work, Hills et al. [36] proposed a manufacturing methodology for CNTs which combines processing and circuit design techniques to overcome the major challenges related to liquid deposition methods for CNT integration in CMOS. However, the complex nature of this work on CNFET-based digital circuits requires defining a dedicated CMOS fabrication process involving materials such as Pt, Ti for metal layers and SiO_x, HfO_x for PMOS and NMOS passivation layers [36], which are not common is standard CMOS processes. In the case of the DEP process, it provides better alignment and uniformity, but usually has low throughput and requires additional complex metallization steps to achieve better electrical contact between the nanotubes and the electrodes [37]. Seichepine et al. [32] developed CNT integration in CMOS by DEP method with high yield, where 80% of the electrode pairs in the 1024 array of devices only have 1–5 CNT connections per electrode pair; however, these CMOS chips still required extensive metallization post-processing [38]. Local CNT synthesis ensures CNTs with excellent structural quality, but the CMOS-compatible temperature is the main restriction in this integration process [32], and that is what we aim to solve in our approach of CMOS–CNT integration.

The CNT growth structures in CMOS can be fabricated using the polysilicon and metal interconnecting layers. Aluminum (Al) and copper (Cu) are commonly used for metallization in standard CMOS technology [39,40]. These metals, however, are not suitable to serve as microheaters (CNT growth structures) in their original form due to low electrical resistivity and high thermal conductivity. Moreover, aluminum melts at around 660 °C, which is far less than the required 900 °C CNT synthesis temperature. Therefore, we have investigated different binary alloys containing Al or Cu that have material properties suitable for our application. Nickel (Ni) turned out to be the most suitable alloying material for both Al and Cu.

We designed several microstructures suitable for CNT synthesis, using the compatible materials (polysilicon, Al–Ni, and Cu–Ni alloys) in CMOS and performed thermomechanical analyses with the Multiphysics simulation software, ANSYS. Most of these designs involve partially suspended microstructures to balance mechanical stability and high thermal isolation. A few designs involve fully suspended microstructures or no suspension at all. The simulation results presented in this paper show the feasibility of reaching CNT synthesis temperature by local resistive heating, while keeping safe temperatures on the chip for the CMOS circuits. As a result, we also designed a CMOS chip containing different CMOS microstructures with the purpose of local CNT synthesis, and the chips were fabricated using a standard AMS 350 nm CMOS process. Layout designs of some of these CMOS microstructures, as well as optical micrographs of these fabricated structures, are presented in this paper.

2. Design Approach for CNT Growth Structures in CMOS

To grow CNTs in CMOS chips by thermal CVD process, a microheater as CNT growth structure is required that can locally generate a hotspot of ~800–900 °C. Therefore, we have investigated the materials commonly used in standard CMOS processes to design efficient microheaters. It is essential to keep the CMOS circuits at a safe temperature, below 300 °C, when the microheater produces the CNT

synthesis temperature; hence, the design approach to maintain the CMOS-compatible surrounding temperature is also discussed.

2.1. Materials for CMOS Microheaters

The local CNT synthesis temperature was generated by joule heating in the simulations, where an electrical current is passed through a conductor to produce the heat. In our study, we were only considering conduction as a medium of heat transfer, neglecting convection and radiation due their minimal effect in micro scale compared to conduction. The nature of convection can be realized by Rayleigh number (Ra), where higher value of Ra indicates more influence of convective heat transfer, and it was shown that Ra decreases significantly for microscopic structures compared to macroscopic structures; thereby, the effect of convection becomes negligible at the micro level [41]. It was also derived that the heat loss on microstructures due to thermal radiation is less than 1%, even for temperature as high as 1000 °C [41]. Therefore, the dissipated electrical power in resistive heating can be converted to heat by Fourier's law of heat conduction. We have previously derived an equation for a rectangular heater [42], where the maximum temperature (T) at the center can be expressed as Equation (1):

$$T = T_0 + \frac{I^2 l^2 \rho}{8 w^2 t^2 k} \tag{1}$$

where T_0 is ambient temperature, I is the current through the microheater, ρ is electrical resistivity, k is thermal conductivity, and l, w, and t are length, width, and thickness of the microheater, respectively.

Materials for microheaters to grow CNTs should have high electrical resistivity (ρ) for efficient heating and low thermal conductivity (k) to reduce heat loss in the surroundings. In terms of material parameters, the ratio ρ/k is an important factor in achieving high temperature on the microheaters by resistive heating. This ratio is proportional to the maximum temperature on the microheater, as shown in Equation (1); hence, a higher value of this ratio is desirable.

Standard CMOS technologies offer several metal interconnect layers comprising Al or Cu, along with conductive polysilicon layers. The melting point of Al is much lower than CNT synthesis temperature, and ρ/k ratio for both Al and Cu are very low for effective resistive heating. Therefore, we investigated several binary alloy options for both Al and Cu. Alloys provide higher electrical resistivity and lower thermal conductivity than the native form of the involved metals, so higher ρ/k ratio can be obtained. Polysilicon has a very high melting point, as well as high ρ/k ratio, making it the most suitable material in CMOS for our microheater application. AMS 350 nm CMOS process uses two polysilicon layers, one polysilicon layer (poly-1) being thicker than the other (poly-2) [43]. A thinner polysilicon layer (poly-2) results in higher electrical resistivity and can also be mechanically beneficial for suspended microstructures, due to less residual stress compared to thicker structures [44].

In a previous study, we showed Cu–Ni alloy to be the best-suited microheater material among other Cu alloys [42]. It should be noted from Equation (1), microheater thickness square (t^2) is inversely proportion to microheater temperature, and thickness of the microheater depends on the alloy composition. Although a 40% Cu–60% Ni composition (at.%) has higher ρ/k ratio, the lower microheater thickness of 70% Cu–30% Ni alloy makes it a more efficient material in this application. A comparison of the relevant material properties (at CNT growth temperature) of copper and its suitable alloys are presented in Table 1.

Table 1. Comparison between material properties of Cu and relevant Cu–Ni alloys [45,46].

Metal Alloy (Composition, at.%)	Melting Point (°C)	Electrical Resistivity, ρ ($\times 10^{-8}$ Ωm)	Thermal Conductivity, k ($Wm^{-1}K^{-1}$)	Ratio, ρ/k ($\times 10^{-8}$ $\Omega m^2 W^{-1}$ K)
Cu	1080	8.5	340	0.025
Cu–Ni (40%/60%)	1200	54.5	49.3	1.105
Cu–Ni (70%/30%)	1150	39	60.5	0.645

In this study, we investigated suitable aluminum alloys for designing metal microheaters since we have designed and fabricated our CMOS chip in AMS 350 nm CMOS process, which offers aluminum metal layers. It should be noted that Al melts at a far lower temperature (~660 °C) than the required CNT growth temperature (~900 °C). Several compositions of Al–Ni alloys, however, have a melting point higher than 900 °C. Based on the material properties, tri-nickel aluminide (Ni_3Al) is the most suitable aluminum alloy for realizing metal microheaters in the AMS 350 nm CMOS process. A comparison of the relevant material properties (at CNT growth temperature) of aluminum and its suitable alloys are presented in Table 2.

Table 2. Comparison between material properties of Al and relevant Al–Ni alloys [45–48].

Metal Alloy (Composition, at.%)	Melting Point (°C)	Electrical Resistivity, ρ ($\times10^{-8}$ Ωm)	Thermal Conductivity, k ($Wm^{-1}K^{-1}$)	Ratio, ρ/k ($\times10^{-8}$ $\Omega m^2 W^{-1} K$)
Al	650	10.5	200	0.053
Al–Ni (50%/50%)	1680	10	72	0.139
Ni_3Al (75%/25%)	1400	73	36	2.028

Ni_3Al alloy has excellent mechanical strength and wear-resistance at high temperatures [49]. The features of this alloy are well-suited for high-temperature applications, such as promising applications in aircraft engines as structural bulk material [50] and MEMS applications (such as micro-actuators) as thin foils [51,52]. This intermetallic phase also has a potential application in microchemical systems as catalysts (microreactors) [52,53].

In Equation (1), length (l) and width (w) of the microheater are defined by our design; current (I) is a variable during the joule heating process, and the heater thickness (t) and material properties (ρ, k) are CMOS-process-dependent parameters. The ratio ρ/t^2k from the equation is directly proportional to the maximum microheater temperature. Although the value of this ratio depends on the CMOS process, it is modified for the metal microheaters when they are transformed into alloys. Therefore, we plotted this ratio in Figure 2 for five different potential materials from Tables 1 and 2. The values of ρ and k are taken at CNT synthesis temperature. Thickness of the alloys are calculated based on a 0.6 µm thick Al or Cu layer, where atomic weights and mass densities of the associated materials are taken into account. A higher value of the ratio ρ/t^2k corresponds to a more efficient microheater, allowing room for reducing the l/w ratio to achieve mechanically more robust designs for suspended heaters. Based on the plot in Figure 2, Cu (70%)–Ni (30%) and Ni_3Al alloys are the most suitable metallic microheater materials among the available options in CMOS for the CNT synthesis application.

The choice between metal and polysilicon microheaters should be based on suitability in CMOS post-processing, although polysilicon has significantly better material properties in terms of using them as microheaters for local CNT synthesis. The metal options are CMOS-process-dependent. Cu–Ni (70%–30%) is the preferred alloy composition if CMOS metal layers are made of Cu, whereas Ni_3Al alloy is suitable as the microheater material in case Al is used in the metallization layer for the CMOS process. Among the polysilicon options, a thinner polysilicon layer with higher electrical resistivity is more efficient as a microheater.

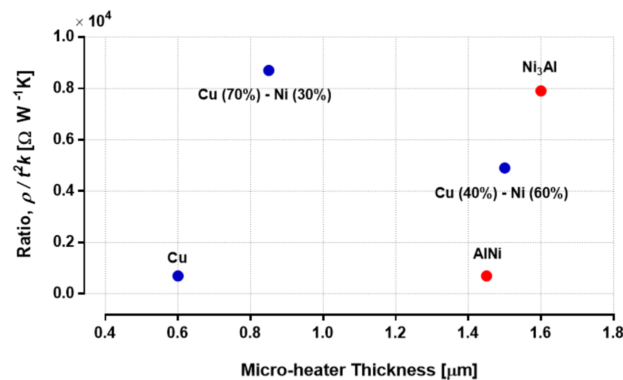


Figure 2. Influential ratio (ρ/t^2k) for maximum microheater temperature plotted against total microheater thickness associated with the material.

2.2. CMOS-Compatible Chip-Surface Temperature

High temperature (~800–900 °C) is necessary to grow CNTs of small diameter (below 10 nm), which ensures aligning of those CNTs by local electric field [54,55] so that they can be suspended between the two microstructures. Therefore, the microstructure/microheater for synthesizing CNTs needs to produce a local hot region of 900 °C. Even if the synthesis temperature is generated by local resistive heating, the entire chip-surface temperature rises higher than the CMOS-compatible temperature due to thermal conduction, since the microstructures in CMOS are surrounded by dielectric layer. Hence, the target is to achieve high enough thermal gradient around the microheater so that CMOS transistors can reside at safe temperatures.

Maximum thermal gradient around the microheaters can be reached by completely etching the dielectric layer underneath those growth structures; however, the microheaters would suffer from undesirable mechanical deformation. Therefore, it is beneficial to keep some dielectric layer underneath the microheaters as a mechanical support. Having dielectric support underneath also means a heat conduction path to the bulk of the chip. It is trade-off between achieving a high thermal gradient and the keeping mechanical integrity of the microheater. So, our goal is to under-etch a sufficient amount of dielectric to get the required thermal isolation for maintaining CMOS-compatible temperatures, while avoiding destructive microheater deformation.

It is important to note that the high microheater temperature is only required for growing CNTs. Therefore, the concern of compatible temperatures for CMOS transistors is limited to the duration of the one-time CNT synthesis process, which takes around 5 min. The CNT-based sensor can operate at room temperature during gas-sensing operation.

3. Thermal Analysis of CMOS Microstructures

We designed several microheaters using the available materials in the standard CMOS process and performed thermoelectric and thermomechanical simulations using Multiphysics simulation software, ANSYS. All microheaters are mechanically stable according to the thermomechanical analysis; however, in practice, the stability of suspended microheaters is significantly affected by the wet etching process. Most of the designed microheaters are partially suspended, meaning a limited amount of the dielectric layer stays underneath the heaters. The simulated models also have a bulk silicon layer and a chip-packaging material layer below the dielectric layer. Room temperature is considered in the bottom surface of the package material as a boundary condition, which is a practical assumption if a heat sink is used during the process. The silicon substrate will be in direct contact with a heat sink if the CNT synthesis process is carried out at the wafer-level during a potential high-volume production, which will further facilitate in maintaining CMOS-compatible temperature.

We have previously worked on thermomechanical simulations of Cu–Ni and polysilicon microheaters [42,56]. However, in the later stage, we chose a standard AMS 350 nm CMOS technology

to design and fabricate the microstructures (detailed in Section 4), which uses aluminum as the interconnecting metal layers. Therefore, in this article, we investigated Al-based alloys suitable for our application, which is reported in Section 2.1, and, consequently, the simulations of the Ni_3Al alloy microheaters are presented in this section. During the CMOS chip design stage, we also found that our previous partially suspended microheater (PSM)-design approaches [42,56] would have some challenges in post-processing and CNT growth, which are discussed in Section 5.3. Hence, we used new PSM-design approaches to overcome those challenges and performed thermal simulations on polysilicon and Cu–Ni microheaters, accordingly. These new simulation results of the mentioned microheaters are also presented in this section.

3.1. Polysilicon Microheaters

The polysilicon microheaters are designed with two different layers: poly-1 and poly-2. In the simulations, the considered sheet resistances of poly-1 and poly-2 are ~6 Ω/sq and ~18 Ω/sq, respectively The fabricated polysilicon microheaters presented in Section 4.2 have ~10 Ω/sq and ~50 Ω/sq sheet resistances for poly-1 and poly-2, respectively. The conservative sheet-resistance values in the simulation mean the fabricated CMOS microstructures should provide better performance as heaters compared to the simulation results. All polysilicon heaters are simulated with 0.85 μm thickness, even though their actual thickness in a CMOS process will be 3–4 times lower. Therefore, the polysilicon heaters will have higher resistance in practice, which is beneficial for resistive heating. In the FEM simulations, higher polysilicon thickness helps to reduce the number of elements for meshing and, consequently, limits the processing time of each simulation.

3.1.1. Polysilicon Microheaters with Limited Under-Etching

The microheaters can be partially suspended along their entire length; Figure 3 reveals the suspended and non-suspended areas. Figure 3a illustrates the microheater surface area, which was divided into three regions. We have presented two PSM designs in this section, where region C is non-suspended and region B is suspended in both designs. A cross-sectional illustration of non-suspended and suspended microheater areas is shown in Figure 3b,c, respectively. The non-suspended regions have a dielectric layer underneath that mechanically supports the microheater.

The designed polysilicon PSMs are 30 μm long and 3 μm wide, giving around 60 and 180 Ω resistance to poly-1 and poly-2 heaters, respectively, when they reach the CNT synthesis temperature. In these models, both region A and B are suspended, keeping dielectric support in region C for design-1, while only region A is suspended for design-2. In design-2, region B can be blocked from under-etching by putting a mask using the top metal layers of the CMOS design on one side of the microheater, as detailed in Section 5.3.

Figure 4 shows the thermal simulation results for both designs, where poly-1 was used as the heater material. The microheaters locally generate the required CNT synthesis temperature in their centers. Design-1 (Figure 4a) achieves a high thermal gradient around the heater due to the 1 μm dielectric etching on both sides (region A and B) of the 3 μm wide heater, leaving 1 μm wide dielectric in the middle (region C). Design-2 (Figure 4b) has a 1 μm wide suspension on one side of the heater (region B), leaving a 2 μm wide dielectric layer (region A and C) underneath the heater. Suspended microheater regions produce a higher thermal gradient around them. Therefore, the microheater in design-2 has lower thermal isolation than the microheater in design-1. Moreover, since a top metal layer blocks heater under-etching on one side (region A), the dielectric layer will remain in the blocked region near that side of the heater, as indicated in Figure 4b, creating more heat-conduction paths. Even with lower thermal isolation of the heater, the average surrounding surface temperature in design-2 is near 100 °C. Therefore, both poly-1 PSM designs maintain the CMOS-compatible temperature in the chip, while producing a local hotspot for CNT synthesis. From a mechanical viewpoint, design-2 is

more preferable over design-1, as it involves less dielectric etching underneath the heater. In terms of power consumption, design-1 (~35 mW) is more efficient than design-2 (~80 mW).

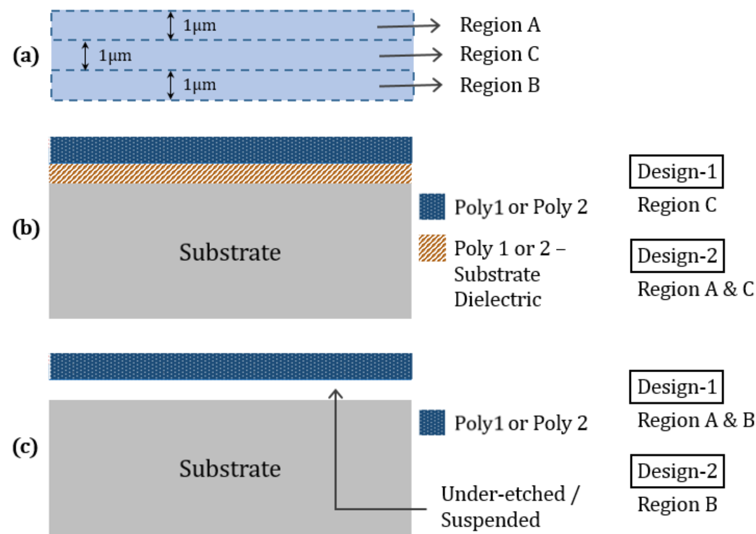


Figure 3. Partially suspended polysilicon microheater design illustrations. (**a**) Microheater surface area; (**b**) cross-sectional view of non-suspended region, and (**c**) cross-sectional view of suspended region.

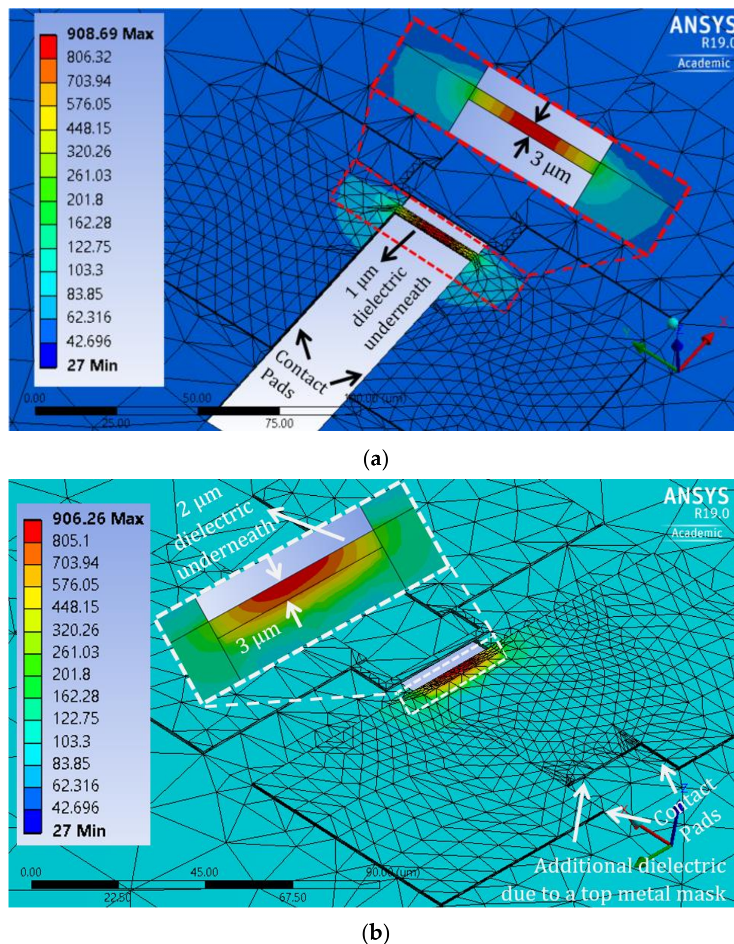
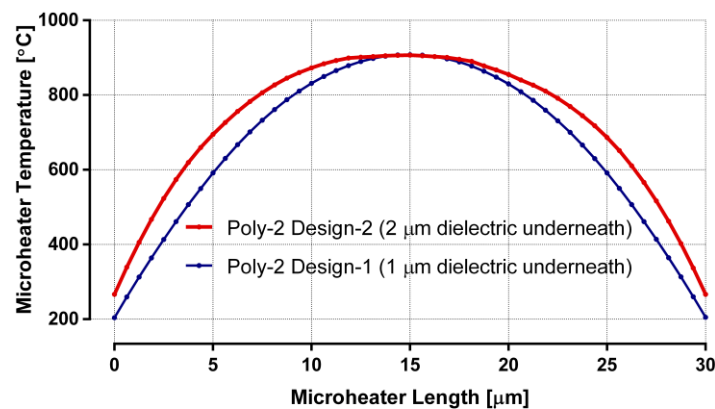
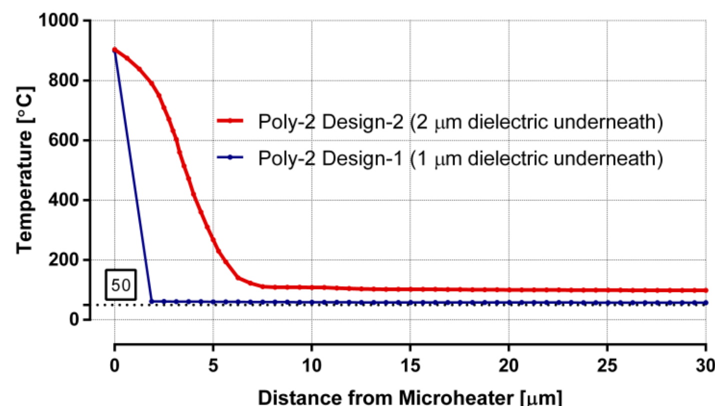


Figure 4. Thermal–electric simulation results of poly-1 partially suspended microheater (PSM) designs: (**a**) design-1 and (**b**) design-2.

The plots in Figure 5 show the thermal-simulation results of poly-2 microheaters for both design-1 and design-2. Temperatures along the length of the heaters are plotted in Figure 5a. The graphs form parabolic shapes (as predicted by Equation (1)) with the maximum temperature (~900 °C) at the center of the heaters, while CMOS-compatible temperatures are reached even at both ends of the heaters. The power requirements for these heaters are similar to the corresponding poly-1 designs. Plots in Figure 5b indicate the temperature drops when moving away from the heaters. High thermal gradient around the heaters is apparent in the plots. Surface temperature in design-1 reaches ~50 °C, within 25 μm away from the heater, achieving an average thermal gradient of 34 °C per micrometer around the heater. In design-2, the surface temperature becomes ~100 °C, within 25 μm away from the heater, indicating an average thermal gradient of 32 °C per micrometer around the heater.



(**a**)



(**b**)

Figure 5. Thermal analysis of partially suspended poly-2 designs: (**a**) microheater temperature along its length; (**b**) temperature distribution from the center of the heater to the surrounding surface.

3.1.2. Non-Suspended and Fully Suspended Polysilicon Microheaters

Two polysilicon microheaters were modelled with a reduced length of 6 μm for simulating non-suspended and fully suspended designs. The widths of the non-suspended and fully suspended designs are 1 and 2 μm, respectively. In the case of the non-suspended design, reduced surface area of the microheater means less of a heat-conduction path through the dielectric layer. The reduced length for a fully suspended microheater offers lower risk of deformation. Although it may still suffer from buckling and stiction, the width of this design was extended to 2 μm for improving mechanical

steadiness. At around 900 °C, resistances of fully suspended and non-suspended designs are ~55 and ~110 Ω, respectively.

These microheaters are only designed with poly-2 layer since it has higher electrical resistivity among the polysilicon options. Thermal responses of both non-suspended and fully suspended designs are plotted in Figure 6. Plots in Figure 6a present the temperatures of the heaters, both having a 2 μm long region in the center, where the heaters reach more than 800 °C, an optimum region to grow low-diameter CNTs. Plots in Figure 6b show that the average surrounding chip temperature reaches far below CMOS-compatible temperature for both designs. Both designs have a very high thermal gradient around the heaters, indicated by the sharp temperature decrease. They also have a similar power requirement of ~20 mW. The non-suspended heater is a clear favorite among these designs, as it avoids mechanical deformation and does not require any dielectric under-etching steps during the CMOS post-processing.

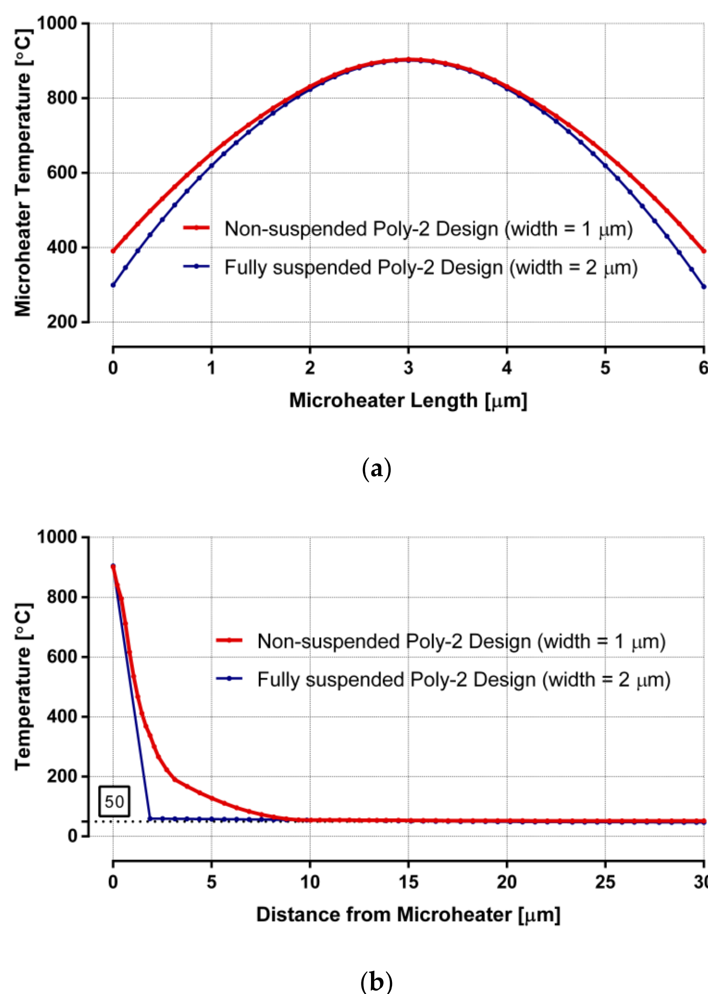


Figure 6. Thermal analysis of non-suspended and fully suspended poly-2 designs: (**a**) microheater temperature along its length; (**b**) temperature distribution from the center of the heater to the surrounding surface.

3.2. Tri-Nickel Aluminide (Ni_3Al) Microheaters

For the standard CMOS process with Al metallization, microheaters were designed and simulated using tri-nickel aluminide (Ni_3Al). Figure 7 shows the thermal simulation results for both non-suspended and partially suspended designs. Around a 1 μm thick layer of Ni needs to be deposited on a 0.6 μm thick Al layer to obtain the Ni_3Al phase, considering the atomic weights and

mass densities of Ni, Al, and Ni_3Al. Therefore, these microheaters are designed with a 1.6 µm thickness. The width of non-suspended design in Figure 7a is 1 µm, whereas PSM (with limited under-etching along the length, similar to design-1 from previous section) in Figure 7b has a 3 µm width. PSMs with a greater width would yield higher mechanical stability in the under-etched design, while lower width of the non-suspended design results in less heat conduction on the substrate.

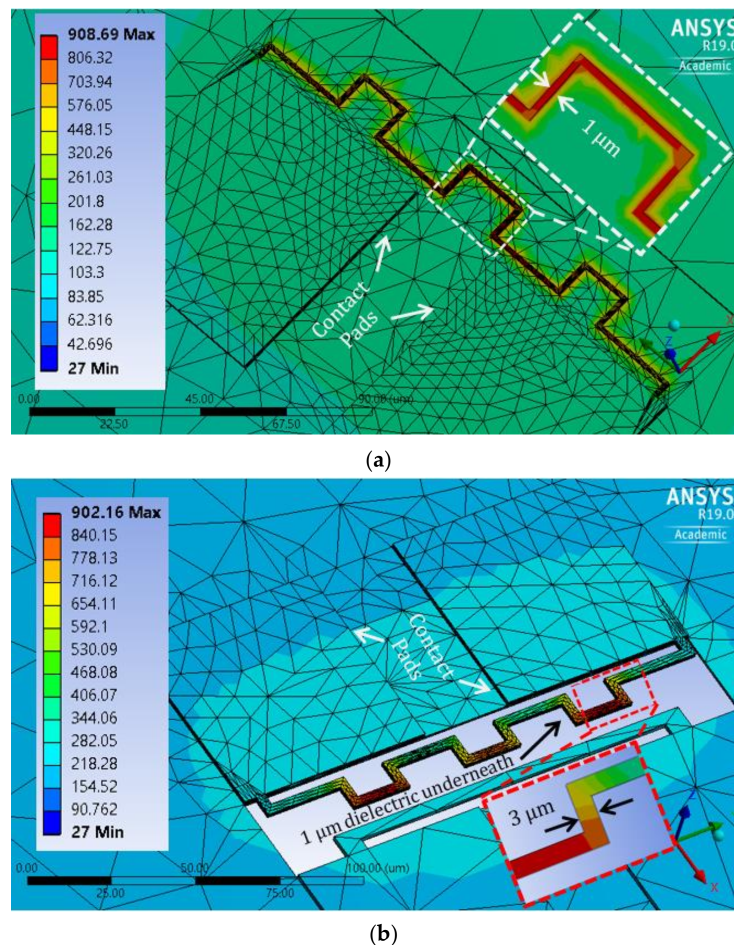


Figure 7. Thermal–electric simulation results of Ni_3Al designs: (**a**) non-suspended and (**b**) partially suspended.

For efficient resistive heating, the microheaters need sufficiently high resistance. Hence, the length of the metal heater designs was extended to ~240 µm for increasing heater resistance. The PSM design had ~15 Ω room temperature resistance, which goes above 35 Ω at the CNT synthesis temperature due to increase in Ni_3Al resistivity at the elevated temperature. The non-suspended design has a 3-times-higher heater resistance due to a 3-times-lower width. The non-suspended design (Figure 7a) produces a chip surface temperature above 300 °C, due to lack of thermal isolation of the heater. This post-processing temperature is not suitable for CMOS circuits. However, the partially suspended design (Figure 7b) has sufficient thermal isolation for the heater, resulting in a CMOS-compatible surrounding temperature of ~200 °C. It requires around 350 and 150 mW power for the non-suspended and partially suspended microheaters, respectively, to generate the CNT synthesis temperature.

3.3. Cupronickel (Cu–Ni) Microheaters

Cu–Ni microheaters were designed and simulated for the CMOS processes that use Cu as interconnecting metal. Material properties of 70% Cu–30% Ni alloy composition is used for the heaters. Considering the atomic weights and mass densities of Cu and Ni, the heaters are modelled with

a 0.85 µm thickness. Depositing 0.25 µm thick Ni on top of a 0.6 µm thick Cu layer is suitable for achieving 70% Cu–30% Ni binary alloy composition upon annealing. The length and width of the heaters in both non-suspended and partially suspended designs are kept same as the Ni_3Al microheater designs. Heater resistances of Cu–Ni designs are also similar to the Ni_3Al heaters, as sheet resistances of both Cu–Ni and Ni_3Al heaters are alike at near CNT synthesis temperature.

Microheater temperatures, along with the surrounding surface temperatures, are plotted for non-suspended, partially suspended, and fully suspended Cu-Ni designs in Figure 8. All these heaters have a local hot region of ~900 °C for growing CNTs, and the temperature starts to drop when moving away from the heaters. The non-suspended design reaches a CMOS-incompatible surface temperature of ~350 °C, while the PSM design manages to achieve a CMOS-compatible chip surface temperature of ~200 °C. Average surrounding temperature of the fully suspended Cu–Ni design drops down to near room temperature. At 25 µm away from the heaters, the average thermal gradients around the non-suspended, partially suspended, and fully suspended Cu–Ni microheaters are 22, 28, and 35 °C per micrometer, respectively. The power requirements of non-suspended and partially suspended designs are similar to the respective Ni_3Al designs, while the fully suspended heater consumes less than 5 mW of power. Even though the fully suspended heater has the maximum thermal isolation and lowest power consumption, the design is not practically feasible, as it is prone to mechanical deformation. Therefore, PSM is the most suitable among the Cu–Ni designs for our application.

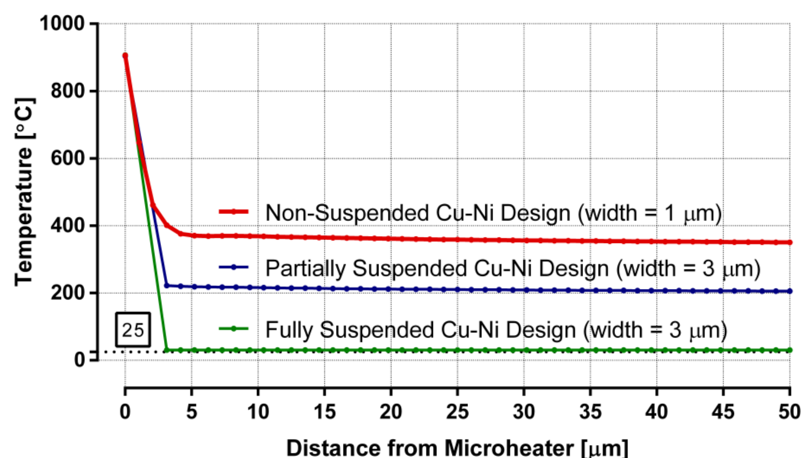


Figure 8. Temperature distribution from the center of different cupronickel microheaters to the surrounding surface.

4. Fabricated CMOS Microstructures for CNT Synthesis

We selected a standard AMS 350 nm CMOS process to fabricate microstructures for locally synthesizing CNTs. In this CMOS technology, aluminum is used for metallization, and copper is not available. Therefore, aluminum and polysilicon layers were used for designing and fabricating the CNT growth structures. The designed 3 mm × 3 mm CMOS chip contains a variety of microstructures, some of which were presented in one of our previous papers [57]. In this article, we present the layout and optical micrograph of the designs relevant to the simulated designs we have presented in Section 3.

4.1. CNT Growth Structures Using Aluminum Layers

Layout design and optical micrograph of the fabricated aluminum microstructures are presented in Figure 9a,b, respectively. The top metal layer was used for the aluminum designs. In this wave-shaped microheater design, the length of the heater is efficiently increased to over 350 µm. The designed width of the heater is 1 µm, resulting in a measured resistance of ~50 Ω. To generate CNT synthesis temperature, Ni needs to be deposited for producing Ni_3Al binary alloy, which will increase both thickness and electrical resistivity of the microheater. Several rectangular beams are used as secondary

microstructures, which go in between the waves of the microheater for producing a high electric field at the beam tips during the CNT growth process, so that some of the synthesized CNTs can be connected to the secondary structures after being guided by the local electric field. The contact pads for the microstructures have a surface area of 95 µm × 95 µm, providing sufficient area for wire bonding. Dimensions measured from the optical micrograph of the fabricated Al microstructures reflect the corresponding dimensions of the layout design.

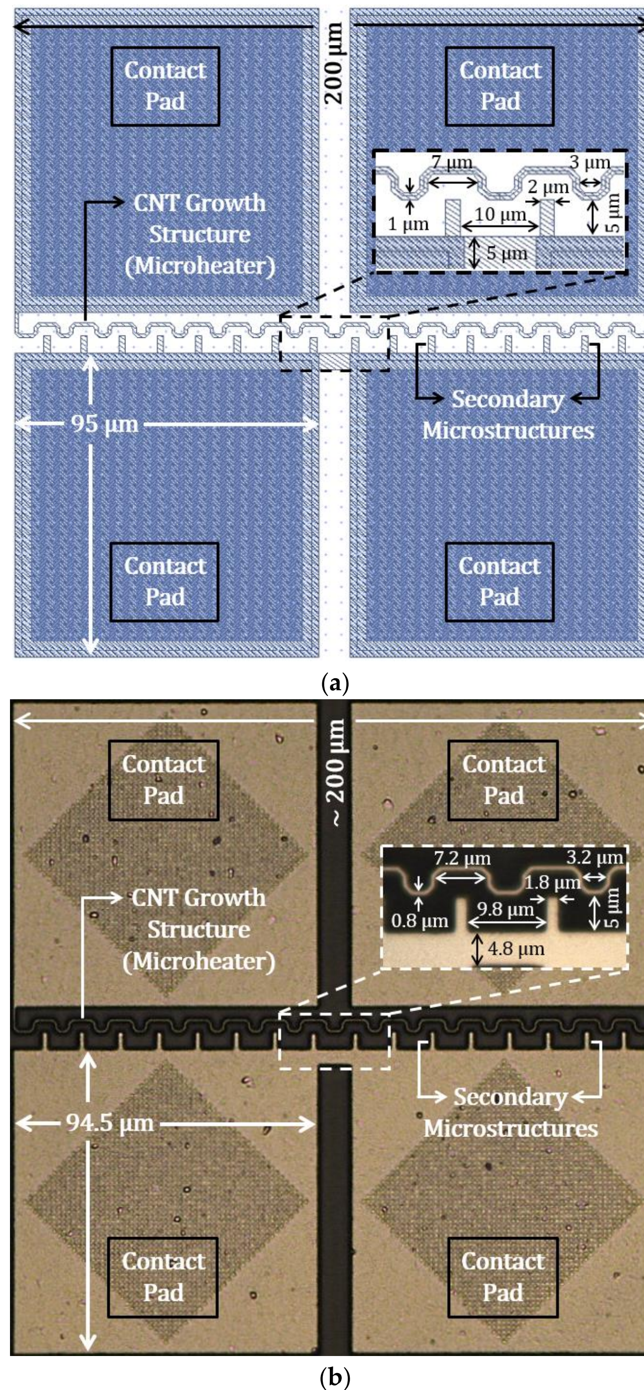


Figure 9. Aluminum CNT growth structures in AMS 350 nm process: (**a**) layout design and (**b**) optical micrograph.

We attempted thermal microscopy of the CMOS microheaters using a high-performance infrared camera, FLIR A6750sc MWIR with a 4X microscopic lens. While the CMOS-chip-surface temperatures

can be measured easily, measuring temperatures on the microheaters was an issue. The camera operates at 3–5 µm wavelengths, with the minimum spot pixel size of 3 µm × 3 µm. The camera also needs an array of 3 × 3 pixels for an adequate thermal measurement. Hence, the narrowest microstructure dimension needs to be at least ~9 µm to obtain acceptable measurements, while most of our microheaters only have ~1 µm widths. Therefore, we did not get accurate temperature data for the microheaters, as the obtained temperature values of the microheaters have an average of the heater temperature and surrounding area temperature of the heater.

Figure 10 shows an infrared image of the Al microheater presented in Figure 9. The heater temperature was controlled by joule heating. Although maximum temperature on the microheater appears to be ~170 °C in Figure 10, the actual heater temperature was much higher. This was confirmed since the Al microheater was melted at the region of maximum temperature when the electrical current through the heater was slightly increased. Therefore, we could estimate that the actual temperature on that hottest spot of the aluminum microheater was ~660 °C (melting temperature of Al). The thermal measurement of the surface surrounding the microheater was accurate, which shows a temperature of ~30 °C. Although the temperature measurement on the microheater was not accurate due to resolution limitation, it is still a positive indication that the surrounding CMOS chip area remains at near room temperature while the Al heater reaches near melting temperature. This shows a convincing sign toward the agreement with the thermal simulation results and maintaining CMOS-compatible temperatures on the chip surface when the microheaters would reach CNT growth temperatures.

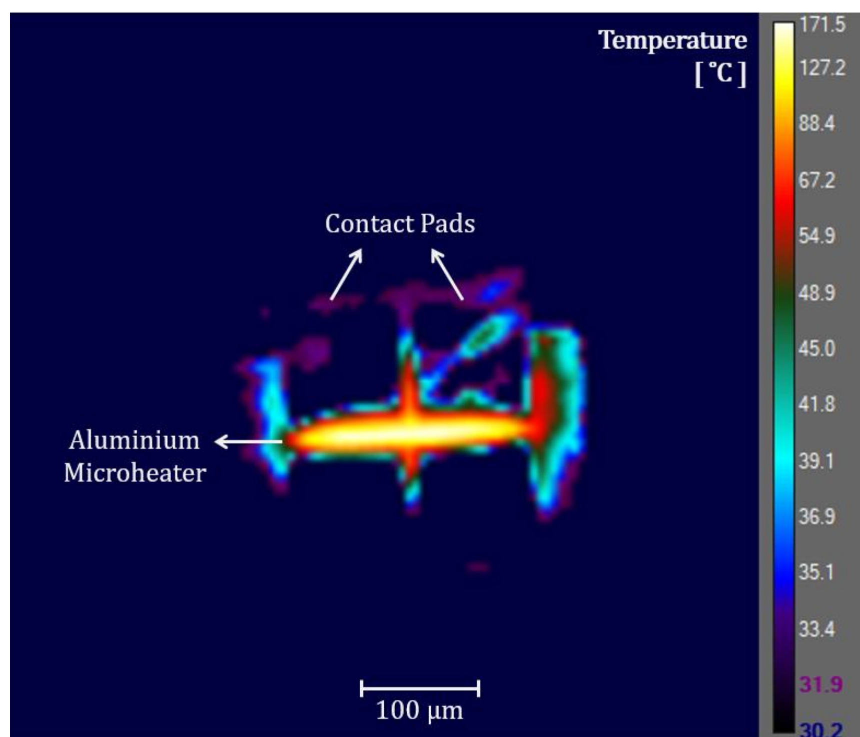


Figure 10. Thermal micrograph of an aluminum microheater on a CMOS chip.

4.2. CNT Growth Structures Using Polysilicon Layers

A poly-1 design for local CNT synthesis application is shown in Figure 11. The CMOS layout design in Figure 11a illustrates all the comprised layers where the vias provide access to metal layers for the polysilicon structures. The extended metal layer aids in designing an 8.3 µm long heater, while keeping a 15 µm distance between the contact pads. The microheater is 0.8 µm wide and has a measured resistance of ~100 Ω. The heater and secondary structures are 4 µm apart. Dimensions of the microstructure layouts are properly translated to the fabricated polysilicon structures, as seen in

the optical micrograph in Figure 11b. This polysilicon microheater has comparable dimensions to one of the simulated heaters in Section 3.1.2.

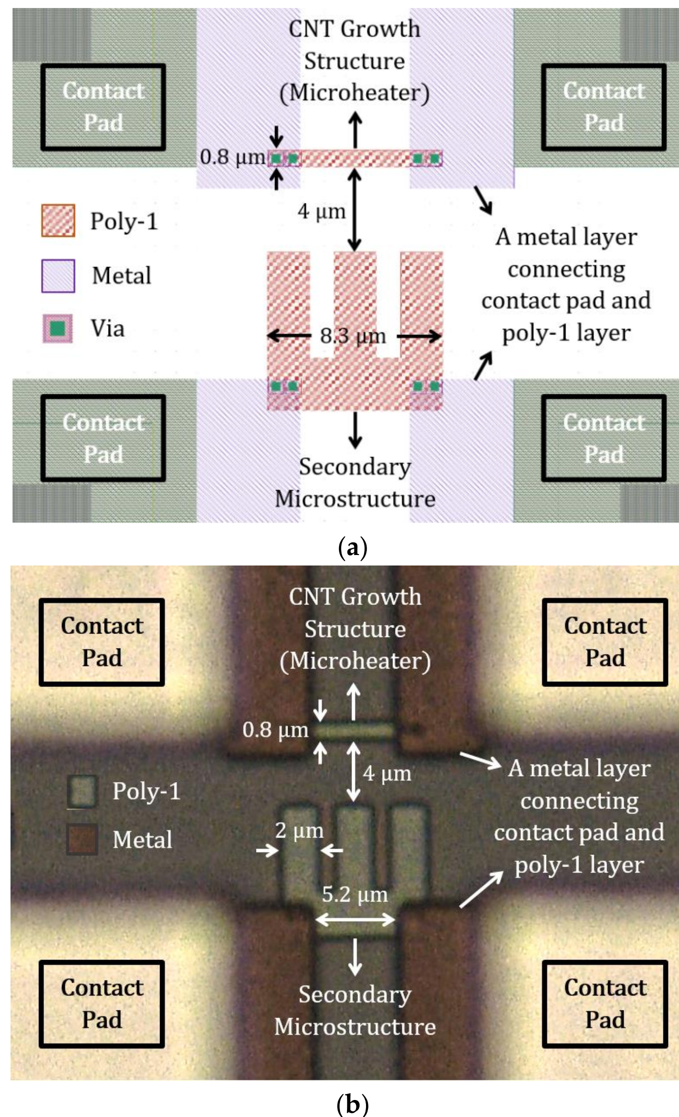


Figure 11. Poly-1 CNT growth structures in AMS 350 nm process: (**a**) layout design and (**b**) optical micrograph.

Figure 12a shows the layout of a poly-2 design, and Figure 12b shows the corresponding optical micrograph of the fabricated CMOS microstructures. The design involves a poly-2 layer, two different metal layers, and vias for electrical connection between layers. Some additional vias are purposely placed in front of the microheater to limit dielectric etching in those regions. In this design, a top metal layer (metal-2) was used as an etch protection mask; hence, the dielectric layer underneath that metal layer is not etched. This poly-2 design resembles a simulated model (design-2) from Section 3.1.1, where the heater is only under-etched from the side facing secondary microstructures. The heater is ~25 µm long and 1.5 µm wide. It has a high measured resistance of ~1 KΩ due to high poly-2 resistivity. The optical micrograph shows the fabricated microstructures, which were rendered well from the designed CMOS layout.

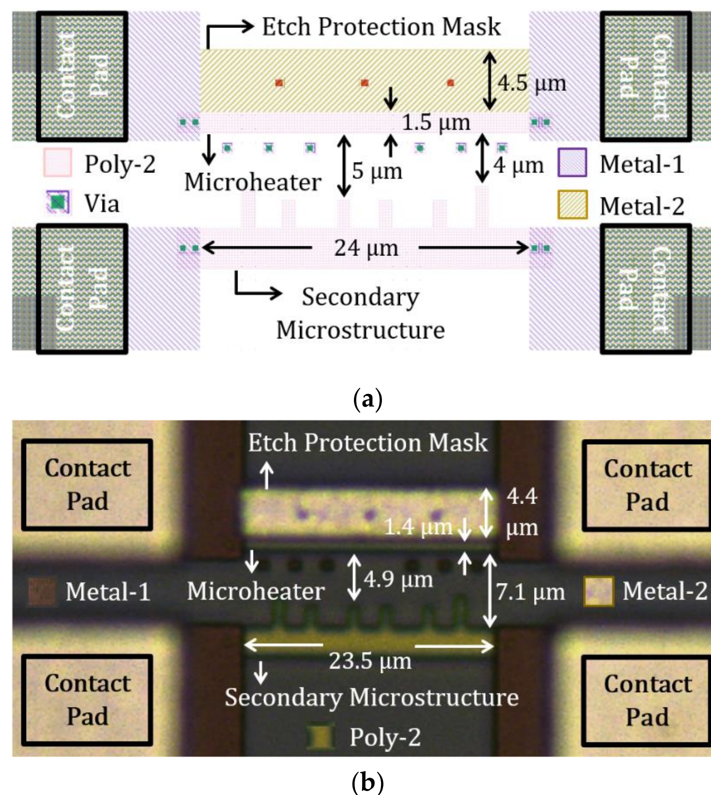


Figure 12. Poly-2 CNT growth structures in AMS 350 nm process: (**a**) layout design and (**b**) optical micrograph.

5. Discussion

Our fabricated CMOS chips need to go through several post-processing steps for growing CNTs. The process complexity will vary depending on the microheater design; non-suspended designs are easier to realize than the suspended ones. For the metal microheaters, alloying is an added step, where the process complexity also differs among the two preferred alloy options. Under-etching approaches of different partially suspended microheaters are included in this part. In prior publications from our group, synthesized CNTs on custom-designed PolyMUMPS [30,58] and SOIMUMPS [31,54] microstructures were presented with relevant SEM and S(T)EM analyses. Polysilicon CNT growth structures used in the PolyMUMPS process have good resemblance with CMOS for CNT synthesis process demonstration.

5.1. CMOS Post-Processing to Realize CNT Growth Structures

Necessary CMOS post-processing to synthesize CNTs on a CMOS chip can be divided into two main stages. The initial stage involves etching the dielectric layers for exposing and under-etching the CNT growth structures in CMOS to achieve high thermal isolation around them. In the case of metal microheaters, this stage also includes making relevant binary alloys. The final stage of the post-processing involves depositing a catalyst layer and growing CNTs on the CMOS microstructures by local thermal CVD process.

The metal and polysilicon layers of a standard CMOS chip are covered with a dielectric layer for electrical isolation, and the entire chip surface is covered with passivation layer(s) for protection from surroundings. In CMOS chip design, we can purposely select regions where the passivation layer(s) can be avoided. It enables an exposed top metal layer surrounded by a dielectric layer. Therefore, the CNT growth structures made from the top metal layer will be readily exposed and available for nickel deposition to produce the alloys.

Nickel can be deposited on the metal tracks (Al or Cu) by evaporation, sputtering, electroplating, or electroless plating. Evaporation and sputtering will need dedicated masks for patterning Ni deposition. Electroless plating can be selective toward deposition on exposed metal tracks, whereas electroplating gives selective deposition on exposed metal tracks that are electrically connected to the electrodes in the electroplating baths. Hence, with an appropriate design, mask-less Ni deposition is possible with plating techniques, where electroplating gives the highest design freedom. Alloying of the Al/Ni bi-layer into homogenous Ni_3Al is performed through local resistive heating, passing a current through the microheater while in inert atmosphere. The method is similar to that used in the formation of a desired composition of cupronickel alloy.

After the alloying process, the metal microheaters are partially suspended for sufficient thermal isolation during resistive heating. Dry etching by RIE (Reactive Ion Etching) can be performed for anisotropic dielectric etching, followed by a wet etching process to partially release the microheaters. The amount of microheater under-etching depends on the wet etching duration for a specific chemical etchant. Therefore, the required amount of heater suspension can be achieved by controlling the etching duration.

In the case of polysilicon heaters, a thick layer of dielectric is removed by RIE to expose the polysilicon layers. Only this step is required in the initial post-processing stage for non-suspended heaters. However, partially or fully suspended microheaters need an additional step of wet dielectric etching. Even though RIE is anisotropic, it can still cause some heater undercuts, which can be a desirable effect for our application. The wet etching step will no longer be required if the microheaters have sufficient undercuts to obtain required thermal isolation.

Once the CNT growth structures are prepared, a thin catalyst layer (~5 nm) is deposited in the beginning of the final post-processing stage. Iron or nickel is commonly used as the catalyst material, which can be deposited by thermal evaporation, e-beam evaporation, or sputtering. The thin metal layer transforms into nanoparticles at ~900 °C, during resistive heating of the CNT growth structure in the CVD chamber. CNTs start to grow when a carbon-containing precursor gas released in the chamber interacts with the catalyst nanoparticles.

The mentioned CMOS post-processing steps are needed at the research level since they will be performed on individual CMOS chips. However, those process steps may be included in a dedicated process designed for CNT-to-CMOS integration, which can be carried out in wafer-level fabrication for manufacturing commercially viable CNT-based sensors. Zhou et al. [26] previously demonstrated CNT growth on polysilicon structures in CMOS involving various post-CMOS microfabrication processes that we avoid in our approach, with the vision to incorporate the CNT synthesis process in a CMOS technology at wafer-level.

5.2. Tri-Nickel Aluminide vs. Cupronickel Microheaters

Forming a tri-nickel aluminide alloy may be more challenging than cupronickel alloy, because of the native oxide layer on aluminum, with Al having a lower electrochemical potential than Cu. Moreover, during the formation of a Ni_3Al alloy, undesirable intermetallic alloys (such as Al_3Ni, Al_3Ni_2) with a melting temperature lower than 900 °C could also form. A detailed process development is needed to ensure a final microheater composition compatible with high-temperature operation. A certain flexibility in the composition is allowed, however, as both the Ni and the AlNi phases have even higher melting temperatures than that of Ni_3Al. For Cu–Ni, the exact composition is not a critical parameter, since Cu and Ni form a solid solution, being completely miscible.

Electrical resistivity to the thermal conductivity ratio (ρ/k) of Ni_3Al is almost twice that of Cu–Ni (70%–30%) at CNT synthesis temperature (~900 °C). A higher ρ/k ratio is desirable for the efficient resistive heating of microheaters. However, the thickness of a Ni_3Al microheater is much higher than that of a Cu–Ni (70%–30%) microheater for a specific Al or Cu thickness, which reduces a Ni_3Al microheater's resistance and, consequently, makes it less efficient for heat generation by resistive

heating. Considering both alloy formation challenges and material efficiency as a microheater, a CMOS process using Cu for metallization is preferred over the one using Al.

5.3. Under-Etching Approaches for PSMs

Two different PSM designs were presented in Section 3.1.1. Design-1 will have limited under-etching along the length from both sides of the heater, whereas design-2 will be under-etched from one side since the other side has a metal mask for avoiding dielectric etching. Our fabricated polysilicon heater in Figure 11 is suitable for design-1 under-etching approach, and the heater in Figure 12 matches the under-etching strategy for design-2. For both designs, under-etching can be obtained by isotropic wet etching, and the amount of suspension depends on the wet etching duration. Different etching times should be attempted to find the optimum duration for the wet etching process to get the required amount of under-etching. The wet etching process may not even be required if the heaters have undercuts within a desired range during the dry etching process, as discussed in Section 5.1.

No mask is needed for the etching process of design-1, but design-2 has a built-in etch protection mask. A top metal block (interconnect layer in CMOS) is placed on one side of the polysilicon microheater, which will act as mask to protect that side of the heater from etching. Therefore, the dielectric layer beneath that metal block will remain. As a result, during the resistive heating process, heat from the microheater will also conduct to the surroundings through the dielectric from that side, which would contribute in making the chip from design-2 hotter than that from design-1.

We have previously designed PSMs using selective patterned under-etching [56]. The surface and cross-sectional view of such a design is shown in Figure 13. Patterned microheater under-etching also needs metal blocks as built-in masks, which will have dielectric material beneath them. Therefore, the top surface of the microheater will be covered with dielectric on the areas where metal blocks are placed above them, as seen in the cross-sectional illustration of Figure 13. This would cause further heat conduction through the top dielectric layer when the microheater is activated, making the chip relatively hotter. Moreover, CNTs cannot grow on the microheater surface, which is covered with dielectric. The improved PSM design approaches presented in this paper solve these issues. Although the microheaters with limited under-etching along their length would be more vulnerable to thermomechanical stress compared to heaters with patterned under-etching, the prior etching approach is still preferred from an overall perspective for PSM designs in our CNT synthesis application.

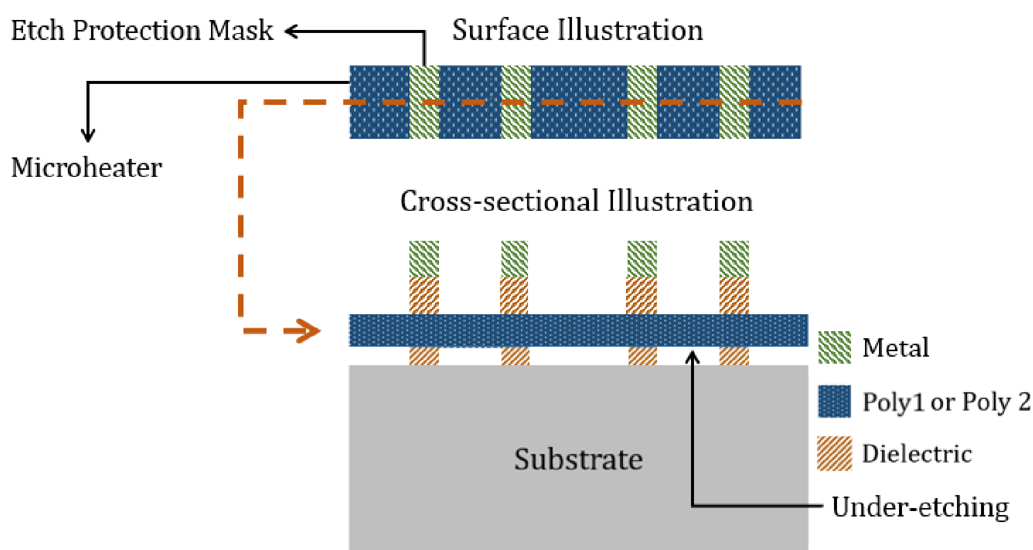


Figure 13. Surface and cross-sectional illustration of a selectively under-etched PSM design.

6. Conclusions and Future Work

We presented several designs of CNT growth microstructures (microheaters) using the materials available in standard CMOS process. Polysilicon is the most suitable material in CMOS to serve as a microheater. The metal options (Al or Cu) need to be alloyed with Ni to produce efficient microheaters for the CNT synthesis application. Tri-nickel aluminide and cupronickel (70% Cu–30% Ni) were chosen as the binary alloys from the investigated materials.

Thermal analyses of the CMOS microheaters show that they can have CNT synthesis temperature (~900 °C) on their surface, while having a high thermal gradient to achieve a CMOS-compatible temperature (below 300 °C) on the remaining chip area. Most of the designed microheaters need partial suspension to obtain necessary thermal isolation for CMOS compatibility. The heaters should have sufficient under-etching to obtain a high thermal gradient around them, while avoiding significant mechanical deformation.

CNT growth structures were fabricated in a standard AMS 350 nm CMOS process, using aluminum and polysilicon layers. The microstructures are properly realized in the CMOS chip, as seen from the presented layout designs and optical micrographs of the fabricated structures. The CMOS chips are required to undergo several post-processing steps to prepare the microstructures for local CNT synthesis.

The metal microheaters (Al or Cu) on the fabricated CMOS chips are already exposed; thus, they need alloying as an initial post-processing step, followed by partial dielectric under-etching, using dry and wet etching methods. The polysilicon microheaters need to be exposed first by dry etching of dielectrics and may require wet etching for partial suspension if there are insufficient undercuts on the heaters during the RIE process. The wet etching process is also avoided if the non-suspended polysilicon microheaters manage to obtain required thermal isolation. Once the microheaters are prepared, a thin catalyst layer needs to be deposited on the CMOS chip before carrying out the CVD process for growing CNTs on the microheaters in the final post-processing step.

We already have an established process for locally synthesizing CNTs on MEMS growth structures. However, the CNT growth structures in CMOS need additional processing steps, as discussed for enabling them to obtain the CNT synthesis temperature in a CMOS-compatible environment. These post-processing steps are currently being developed in our cleanroom, using the fabricated CMOS chips. Our next goal is to locally grow CNTs on the dedicated microstructures in the custom-designed CMOS chips. Direct CNT–CMOS integration will be established once the CNTs are suspended between the CMOS microstructures, and the CNT-based prototype sensor can be tested for gas sensing.

Author Contributions: Conceptualization, K.E.A., A.R., M.A., and B.Q.T.; methodology, A.R.; software (Thermal Simulations), A.R.; software (CMOS Chip Design), A.R., M.A., and P.H.; formal analysis, A.R.; investigation, A.R.; data curation, A.R.; writing—original draft preparation, A.R.; writing—review and editing, K.E.A., A.R., B.Q.T., M.A., and P.H.; validation, K.E.A. and M.A.; visualization, A.R.; supervision, K.E.A., M.A., and P.H.; funding acquisition, K.E.A.

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Conflicts of Interest: The authors declare no conflict of interest.

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Article 3

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Article 4

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Article 5

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Article 6

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