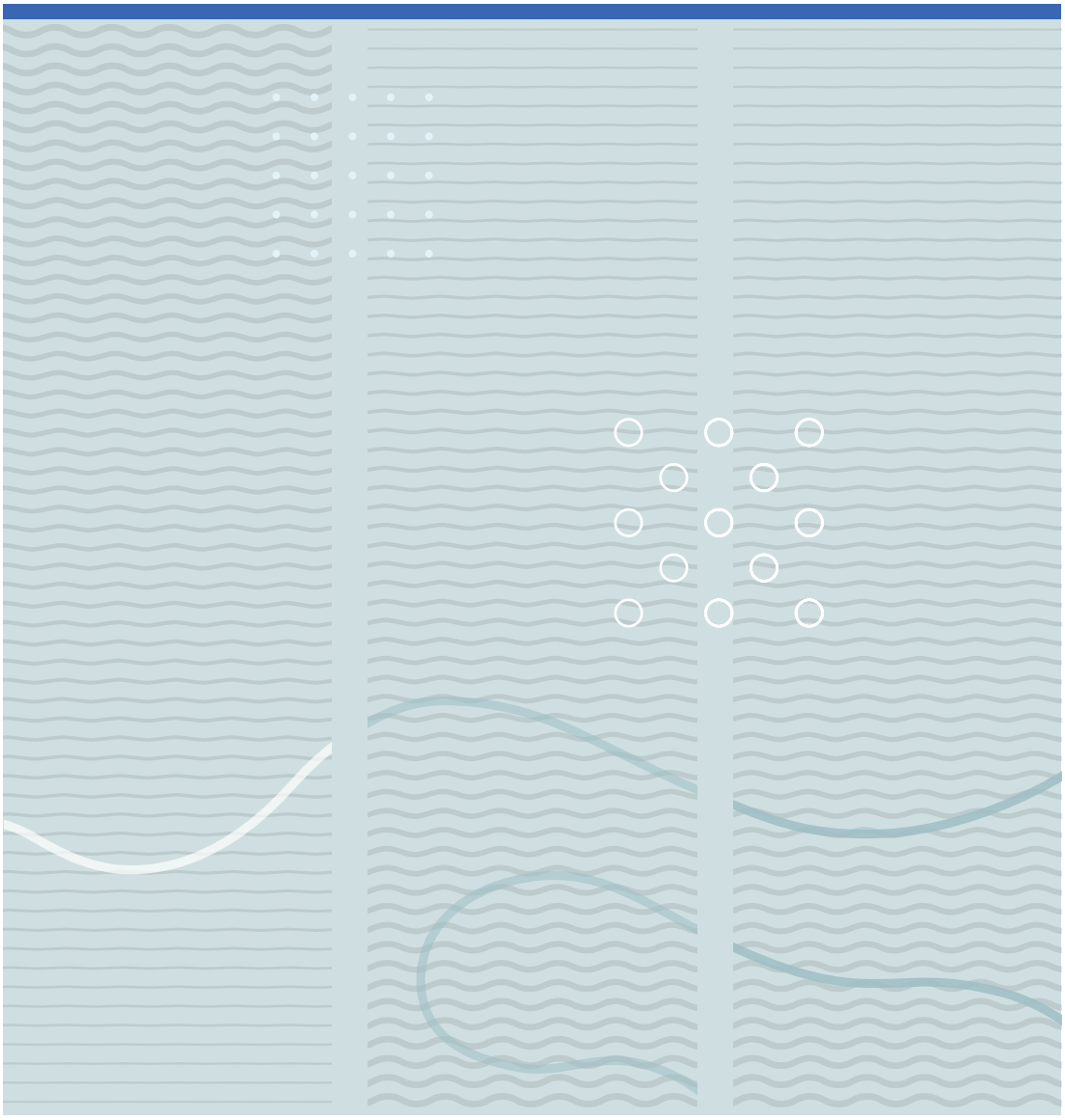
University of South-Eastern Norway
Faculty of Technology, Natural Sciences and Maritime Studies

Doctoral dissertation no. 52
2019

Bjørnar Karlsen

Optically operated pulse-driven Josephson junction arrays and range extension using voltage dividers and buffer amplifiers



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A PhD dissertation in
Applied Micro- and Nanosystems

Faculty of Technology, Natural Sciences and Maritime Studies
University of South-Eastern Norway
Horten, 2019

Doctoral dissertations at the University of South-Eastern Norway no. 52

ISSN: 2535-5244(print)
ISSN: 2535-5252 (online)

ISBN: 978-82-7860-412-0(print)
ISBN: 978-82-7860-413-7 (online)

Print: University of South-Eastern Norway

Preface

This thesis marks the completion of the requirements for the degree of Philosophe Doctor at the University of South-Eastern Norway (USN). This work has been carried out in collaboration between USN and Justervesenet (JV), under the supervision of Per Alfred Øhlckers (USN), Muhammad Nadeem Akram (USN), and Helge Malmbekk (JV).

Work related to the development of voltage dividers and buffer amplifiers draws inspiration from previously conducted research with current shunts and voltage dividers at JV through the EMRP project ”Power & Energy”. The work related to the cryogenically operable pulse-drive for Josephson Arbitrary Waveform Synthesizers draws its inspiration from EMPIR projects Q-Wave and Qu-ADC.

Parts of this research have been performed at the National Physical Laboratory (NPL) in the United Kingdom, at Physikalish-Technische Bundesanstalt (PTB) in Germany, and at the Technical Research Center of Finland (VTT) in Finland. These institutes have made available facilities and equipment to perform tests on our setups and prototype photodiode modules, as well as providing valuable insight into the generation of electrical and optical pulses, as well as the operation of pulse-driven Josephson junction arrays. PTB has also provided important components for the manufacturing of the photodiode modules.

This research has involved many disciplines, such as RF electronics, cryogenics, signal processing, opto-electronics, electronic packaging techniques, and quantum metrology. Further, understanding nonideal behaviors such as stray contributions and electrical reflections in real circuits and components have been essential to obtain and understand the results from this research.

Funding for this research has been provided by the Norwegian Research Council via the program Public Sector PhD, the EMPIR project Qu-ADC, as well as directly from JV.

Acknowledgments

Since I began this research, years have flown by much faster than I could ever have imagined. These years have given me lots of joy, as well as an understanding of what it means to be a scientist. In order to get this far, there are many people that have been important.

Had it not been for my supervisors Per Alfred Øhlckers (USN), Muhammad Nadeem Akram (USN), and Helge Malmbekk (JV) providing guidance throughout this process, I would never have been able to perform this research. They have given tons of knowledge about optics, electronics, cryogenics and metrology, and last, but not least, helping me learn to be accurate in how I understand, present and explain my research and results, for which I am incredibly thankful!

Researchers Kåre Lind (ex JV) and Eivind Bardalen (USN) have also made valuable contributions to this work. Kåre has provided valuable knowledge and experience about electrical circuits. Eivind has been the main brain behind the packaging technique to make cryogenically operable photodiode modules, which has been utilized for many of the articles for this thesis, as well as manufacturing (together with Thai Anh Tuan Nguyen (USN)) most of the sample modules used to conduct this research.

Even though most of the research has been done at JV and USN, at many stages of this research, we have been dependent upon equipment that we have not had available at JV. Therefore, many of our experiments have performed at NPL, PTB, and VTT, who have been more than happy to put their facilities and equipment at our disposal, and providing the liquid helium necessary for the experiments. In particular, I would like to mention Jonathan Williams (NPL), Jane Ireland (NPL), Oliver Kieler (PTB), Ralf Behr (PTB), Luis Palafox (PTB), and Jaani Nissilä (VTT), as well as countless others at these institutes who also have had their inputs into the research.

Knowing that I had family and friends around me to provide moral support whenever I have needed it has made it easier to complete this process. Especially my parents, who have listened to me complaining when thing have been tough, and given me motivation and inspiration to move further in my work.

Abstract

Voltage dividers and buffer amplifier combinations can be used to transfer and extend traceability in voltage and electrical power metrology between a wide range of instruments. For voltages up to 1000 V, resistive voltage dividers are mostly preferred as their operating current vary little in the range 10 Hz to 1 MHz, compared to inductive and capacitive dividers. A buffer amplifier is often used to maintain the divider's division ratio, by fixing the output impedance of the divider, and supplying enough current to drive both low-resistive and high-capacitive loading instruments.

Through several design iterations, a buffer amplifier has been developed (chapter 2), with a near unity gain in an entire decade of applied voltages and frequencies up to 1 MHz. It has been used together with a 10:1 resistive voltage divider, which has also been developed (chapter 2) as a part of this work. This combination has been characterized for applied voltages up to 50 V for frequencies up to 100 kHz, using thermal transfer standards.

Quantum-accurate alternating current voltage waveforms can be synthesized from Josephson junction arrays, by applying a calculated pattern of fast current pulses of up to tens of gigapulses-per-second. By using photodiodes, placed together with the Josephson arrays, in liquid helium, an optical pulse-drive scheme can be used to realize the Josephson effect. The photodiode and Josephson array become an electrically floating unit, which makes it simpler to couple multiple, parallel-driven Josephson arrays in series. By splitting the optical pulse-drive, using fiber splitters, the number of photodiodes that a single optical pulse-source can drive is increased, which constitutes an inexpensive method of increasing the number of parallel-operated Josephson arrays.

In this thesis, a cryogenically operable packaging technique of a photodiode has been developed, and used to generate both uni- and bipolar current pulses in liquid helium. The unipolar module has also been used to drive various Josephson junction arrays consisting of up to 3000 junctions to synthesize both direct current voltage and unipolar alternating current voltage waveforms. This part of the thesis (chapter 3) mainly focuses on the requirements and abilities of the laser-pulsation sources and the photodiode packages to

produce current pulses that can realize the Josephson effect in these arrays. By investigating methods of increasing the pulsation bit rate, and operation of multiple photodiodes from a single source, waveforms with a higher amplitude can be synthesized in these arrays.

Mach-Zehnder modulation of a continuous-wave laser has been performed to generate photo-current pulse widths (full-width-at-half-maximum) as short as 62 ps in the bipolar module, and peak heights up to 16 mA for wider pulses in the unipolar module. A mode-locked laser has been used to generate photo-current pulse widths as short as 37 ps in the bipolar module, and with peak heights up to 6.34 mA. The unipolar photodiode module has been used to operate a single array of 3000 Josephson junctions to synthesize a unipolar waveforms with 18.6 mV peak height at 1.875 kHz, and a 92 dBc suppression of higher harmonics.

List of articles

Article 1:

Characterization of high-precision resistive voltage divider and buffer amplifier for AC voltage metrology

B. Karlsen, K. Lind, H. Malmbekk, and P. Ohlckers

Int. J. Metrol. Qual. Eng., Vol. 10, Aug. 2019, DOI: 10.1051/ijmqe/2019006

Article 2:

Pulsation of InGaAs photodiodes in liquid helium for driving Josephson arrays in AC voltage realization

B. Karlsen, O. Kieler, R. Behr, T. A. T. Nguyen, H. Malmbekk, M. N. Akram, and P. Ohlckers

IEEE Trans. Appl. Supercond. , Vol. 29, No. 7, Oct. 2019,

DOI: 10.1109/TASC.2019.2901573

Article 3: **Excluded from online edition due to publishers' regulations**

A Bipolar Photodiode Module for Pulse-Driven Josephson Arrays in Liquid Helium

B. Karlsen, E. Bardalen, J. Nissilä, O. Kieler, L. Palafox, R. Behr, H. Malmbekk, M. N. Akram, and P. Ohlckers

Submitted to IEEE Trans. Instrum. Meas.

Article 4:**Excluded from online edition due to publishers' regulations**

Packaging and Demonstration of Optical-Fiber-Coupled Photodiode Array for Operation at 4 K

E. Bardalen, B. Karlsen, H. Malmbekk, O. Kieler, M. N. Akram, and P. Ohlckers

IEEE Trans. Compon. Packag. Manuf. Technol., Vol. 7, No. 9, Sept. 2017, pp. 1395-1401

Article 5:

Reliability study of fiber-coupled photodiode module for operation at 4 K

E. Bardalen, B. Karlsen, H. Malmbekk, M. N. Akram, and P. Ohlckers

Microelectronics Reliability, Vol. 81, 2018, pp. 362-367

Article 6:

Evaluation of InGaAs/InP photodiode for high-speed operation at 4 K

E. Bardalen, B. Karlsen, H. Malmbekk, M. N. Akram, and P. Ohlckers

Int. J. Metrol. Qual. Eng., Vol. 9, Nov. 2018, DOI: 10.1051/ijmqe/2018015

Article 7:

Optical pulse-drive for the pulse-driven AC Josephson voltage standard

O. Kieler, B. Karlsen, P. Ohlckers, E. Bardalen, M. Nadeem Akram, R. Behr, J. Ireland, J. Williams, H. Malmbekk, L. Palafox, and R. Wendisch

IEEE Trans. Appl. Supercond. Vol. 29, No. 5, Aug. 2019,

DOI: 10.1109/TASC.2019.2899851

Summary of articles

This section summarizes the articles that makes up the body of work for this PhD thesis. These articles are placed towards the end of this thesis, in the exact order as they are mentioned in this section. My contributions to the articles are stated in the final paragraph in each of the articles.

Article 1:

This article describes the development and characterization of a 10:1 resistive voltage divider and a unity-gain voltage buffer. These objects have been characterized for both AC-DC difference (AC means alternating current, and DC means direct current) using high-precision thermal converters (TCs), and absolute gain using high-precision digital voltmeters (DVMs). These objects have been characterized in the voltage ranges 0.5 V to 50 V at frequencies from 10 Hz to 1 MHz. The measured gain linearity agrees with simulations within 21 μV/V for a nominal gain of 1 V/V.

For this article, I developed and manufactured both the resistive voltage divider and the buffer amplifier. I performed all of the measurements, the data processing, and I wrote the article. The setups used to perform the measurements were already present at JV.

Article 2:

This article describes the high-speed pulsation of the unipolar photodiode module in liquid helium. An optical pulsation setup, consisting of a continuous-wave (CW) laser and Mach-Zehnder modulator (MZM) with modulator driver, has been devised to convert electrical pulses from a pulse pattern generator (PPG) into laser pulses of 1310 nm wavelength. The characterization of return-to-zero single pulses have resulted in a measured maximum pulse peak height of 16 mA for 1 GHz. Pulses with full-width-half-maximum (FWHM) as short as 77 ps have also been produced. The measurements of FWHM have been repeated and reproduced with empirical standard deviations within 6 % for the entire clock frequency span of 1-15 GHz of the PPG. Various bit patterns have been applied to the photodiode module, with bit rates as high as 7.5 Gbit/s.

A characterization of bit pattern stability has been performed on the photodiode module,

using the 10 GHz return-to-zero pulses at 2.5 Gbit/s from the PPG as a basis. This test was performed over a time span of 90 minutes, in 13 data series, where only a small drift in the output waveform was observed, which is attributable to heating of the MZM itself. The data from the first and the final data series were used as a basis to simulate the flux transfer caused by the pulses in a typical Josephson junction (JJ), with I_c=2.9 mA and f_c=10 GHz.

For this article, I put together the optical pulse-drive (CW laser, MZM and modulator driver), and took part in the plans on modifying an already existing cryoprobe to include an optical fiber input interface. All other instruments were present at PTB, and T. A. T. Nguyen (fourth author) at USN manufactured the unipolar photodiode modules. O. Kieler (second author) at PTB and I performed the measurements. I performed all of the data processing, including the simulations, and I wrote the article.

Article 3:

This article describes the development and testing of a first prototype of bipolar photodiode modules, operable in liquid helium. Two setups have been used to test the bipolar modules. The first setup uses a MZM to convert a CW laser into a laser pulse pattern, and the second uses a mode-locked laser (MLL) to produce fast pulses, and a MZM to select a pattern of these pulses. The current manufacturing technique allows for no less than a 4.5 mm wide separation of the two photodiodes. For this reason, samples both with and without 50 Ω on-chip termination were manufactured, to determine whether it is necessary to terminate the photodiodes to reduce the presence of reflections. Although the on-chip termination reduced the output pulse peak height to about half, it is still necessary in this design, due to an abundance of reflections.

Two different setups have been used to test these bipolar photodiode modules. The first setup is based on a CW laser, where a MZM is used to both create and select pulses to be applied to the photodiodes. Consequently, the produced pulse shapes depend upon the electrical signals that is applied to the MZM. The second setup is based on a fast MLL, which produces a continuous pulse train with FWHM less the 15 ps, and where only the pulse selection is performed by the MZM.

In this article, it is also alluded to the possibility of placing the photodiodes with a separation of only 500 μm, given that a new technique to make optical contact is developed. With this configuration, the two photodiodes can be seen as a common point source, hence; on-chip termination might not be necessary. For this reason, simulations model were constructed in COMSOL Multiphysics, where the two photodiodes were separated by both 4.5 mm and 500 μm, and both with and without on-chip termination. The simulation results from the first model resemble the measured results from the prototypes, with an abundance of ringing from reflections in the unterminated version. In the second model, the simulations showed that the ringing was almost completely removed in the unterminated version, and completely gone in the terminated version. The ringing in the latter model, should be so much reduced, that termination should be unnecessary for the operation of a Josephson junction array (JJA), however, this must be verified by actual measurements in a Josephson arbitrary waveform synthesizer (JAWS) setup.

For this article, I partook in the planning of the current bipolar chip-carrier design. E. Bardalen (second author) at USN, who also performed the COMSOL simulations for the current and the proposed new design, manufactured the samples. I performed the measurements together with E. Bardalen (second author) and O. Kieler (fourth author) at PTB, and with J. Nissilä (third author) at VTT. All instruments, but the MZM and modulator driver, were present at the respective institutes where the measurements were performed. I did most of the data processing, and I wrote the article, except for one section about the COMSOL simulation model.

Article 4:

This paper describes the development and DC testing a cryogenically operable, unipolar photodiode module. The module consists of 2 channels of 4 photodiodes, where one of the photodiodes was connected to put out pulses (though not done in this paper), and the 3 other were connected to induce the electrical reverse bias for the first, and for both channels. The photodiodes were flip-chip bonded onto a silicon-based chip-carrier with Nb tracks, and borosilicate sleeves were glued onto the chip-carrier to make optical contact with the photodiodes via a ferrule-ended fiber. The photo current versus laser current relation was shown to be similar for the photodiode at 296 K (at room temper-

ature) and 4 K (in liquid helium), reaching photo currents up to 8 mA. The photodiode module was thermally cycled 5 times, with no clear alteration in its electrical behavior. Therefore, this manufacturing technique has been selected to manufacture photodiode modules for the other papers.

For this article, I made substantial contributions to the conception of the work. I took the photography in Fig. 6 (b), I performed the measurements shown in Fig. 8 and 10, and I took part in the editing process of the article. The article was written by E. Bardalen (first author).

Article 5:

This paper describes the development process of a cryogenically operable, unipolar photodiode module. The photodiodes were flip-chip bonded onto a silicon-based chip-carrier with Nb tracks, and glass sleeves were glued onto the chip-carrier to make optical contact with the photodiodes via a ferrule-ended fiber. Finite-element simulations were performed in COMSOL Multiphysics to investigate the resulting stress from combining the components with different thermal expansion coefficient, to determine which adhesives that would reduce the mechanical stress enough to avoid cracking of the module at liquid helium temperatures. A packaging technique has thus been developed, that could mechanically survive the thermal cycling between room temperature and liquid helium.

For this article, I made substantial contributions to the conception of the work. I took part in some of the measurements, and in the editing process of the article. The article was written by E. Bardalen (first author).

Article 6:

This article describes the AC behavior of the photodiode at various temperatures between 4-296 K, and at frequencies from 100 kHz to 14 GHz.

For this article, I made substantial contributions to the conception of the work. I took part in the measurements, and in the editing process of the article. The article was written by E. Bardalen (first author).

Article 7:

This article describes the use of the unipolar photodiode module, tested in (**Article 2**), to pulse-drive a JJA consisting of 3000 JJs. Both DC voltage plateaus and unipolar AC voltage waveforms (sine waves with a DC offset) were generated. By using a sigma-delta code amplitude of 0.2 at 15 GHz clock frequency, the greatest magnitude of the output waveform was reached at 18.6 mV peak to peak for 1.875 kHz, with a 92 dB suppression of higher harmonics.

For this article, I made substantial contributions in the conceptualizing of the experiments and measurements. In particular, I introduced the Mach-Zehnder Modulator and continuous-wave laser to convert the pulse pattern from the PPG into an optical pulse code. I also, took part in the modification of the cryo probe to include ferrule-ended optical fibers and the use of the cryo-cooled unipolar photodiode module to drive the JJA with fast laser current pulses. I was also heavily involved in the editing process of the article. The article was written by O. Kieler (first author).

List of conference contributions

Conference 1:

Simulation and development of high precision voltage dividers and buffer for AC voltage metrology up to 1 MHz

B. Karlsen, K. Lind, H. Malmbekk, and P. Ohlckers

PRIME 2016, 12^{th} Conference on PhD Research in Microelectronics and Electronics, Lisbon, Portugal, 27-30 June 2016

Conference 2:

Development of high precision voltage dividers and buffer for AC voltage metrology up to 1 MHz

B. Karlsen, K. Lind, H. Malmbekk, and P. Ohlckers

CPEM 2016, 12^{th} Conference on Precision Electromagnetic Measurements, Ottawa, Canada, 10-15 July 2016

Conference 3:

Josephson arbitrary waveform system with optoelectronic drive

J. Ireland, J. Williams, E. Bardalen, H. V. Nguen, P. Ohlckers, O. Kieler, J. Kohlmann, R. Behr, E. Houtzager, R. Hornecker, H. v. d. Brom, H. Malmbekk, and B. Karlsen

ISEC 2017: 16^{th} International Superconductive Electronics Conference, Sorrento, Italy, 12-16 June 2017

Conference 4:

Optical pulse-drive for the Josephson arbitrary waveform synthesizer

O. Kieler, B. Karlsen, P. Ohlckers, E. Bardalen, M. N. Akram, R. Behr, H. Malmbekk, J. Ireland, and J. Williams

KRYO 2018, Kryogenische Bauelemente, Heidelberg, Germany, 7-9 October 2018

Conference 5:

Optical pulse-drive and on-chip power splitter for the pulse-driven AC Josephson voltage standard

O. Kieler, B. Karlsen, P. Ohlckers, E. Bardalen, M. N. Akram, R. Behr, H. Tian, J. Ireland, J. Williams, H. Malmbekk, M. Schubert, K. Peiselt, L. G. Palafox, and R. Wendisch
ASC 2018, Applied Superconductivity Conference, Seattle, Washington, USA, 28 October - 2 November 2018

Conference 6:
Optical pulse-drive and on-chip power splitter for the pulse-driven AC Josephson voltage standard
O. Kieler, R. Behr, H. Tian, L. Palafox, R. Wendisch, R. Gerdau, J. Kohlmann, B. Karlsen, H. Malmbekk, P. Ohlckers, E. Bardalen, M. N. Akram, J. Ireland, and J. Williams
QPM 2019, Quantum and Precision Metrology, Krakow, Poland, 17-19 June 2019

Conference 7:
Optical pulse-drive and on-chip power splitter for the pulse-driven AC Josephson Voltage Standard
O. Kieler, H. Tian, R. Gerdau, R. Wendisch, J. Kohlmann, P. Ohlckers, E. Bardalen, M. Akram, R. Behr, L. Palafox, J. Ireland, J. Williams, B. Karlsen, and H. Malmbekk
ISEC 2019, International Superconductive Electronics Conference, Riverside, California, USA, 28 July - 1 August 2019
(Accepted for presentation.)

Conference 7:
O. Kieler et al.
KRYO 2019, Kryogenische Bauelemente, Braunschweig, Germany, 29 September - 1 October 2019
(Abstract not yet written.)

List of abbreviations

AC	**a**lternating **c**urrent
BIPM	**B**ureau **I**nternational des **P**oids et **M**esures *(French)*
	International Bureau of Weights and Measures *(English)*
CW	**c**ontinous-**w**ave
DC	**d**irect **c**urrent
DVM	**d**igital **v**olt**m**eter
JAWS	**J**osephson **a**rbitrary **w**aveform **s**ynthesizer
JJ	**J**osephson **j**unction
JJA	**J**osephson **j**unction **a**rray
JV	**J**uster**v**esenet
MD	**m**odulator **d**river
MLL	**m**ode-**l**ocked **l**aser
NMI	**N**ational **M**etrology **I**nstitute
MZM	**M**ach-**Z**ehnder **m**odulat
NIST	**N**ational **I**nstitute of **S**tandards and **T**echnology
NPL	**N**ational **P**hysical **L**aboratory
PCB	**p**rinted **c**ircuit **b**oard
PJVS	**p**rogrammable **J**osephson **v**oltage **s**tandard
PPG	**p**ulse **p**attern **g**enerator
PTB	**P**hysikalisch-**T**echnische **B**undesanstalt
RR	**r**ange-**r**esistor
SMD	**s**urface-**m**ount **d**evice
TC	**t**hermal **c**onverter
USN	**U**niversitetet i **S**ørøst-**N**orge *(Norwegian)*
	University of South-Estern Norway *(English)*
VNA	**v**ector **n**etwork **a**nalyzer

Contents

1. Introduction

1.1 Motivation

As technology advances, the need to perform faster, more accurate and more complex measurements is increased. These advancements require better metrological standards, so that the performance of new measurement techniques and instruments can be verified. Because of this push in metrology, work is being done to both improve, and develop new methods of realizing the physical units, and transfer of traceability.

Today, two main forces push forward the need to improve the traceability in AC (alternating current) voltage metrology, namely increased capabilities in signal processing, and an ever-increasing consumption of electrical power. In signal processing, and more specifically the increased accuracy and speed of high-precision analogue-to-digital converters (ADCs) and digital-to-analogue converters (DACs), it has become crucial to synthesize spectrally pure AC voltage waveforms from Josephson junction arrays (JJAs) to be used as standards for calibration of such instruments. The need for production and transport of electrical energy is in stark increase, where the fast development of electrical cars and electronic information are only two causes. Even though work has been done to make electrical devices much more energy efficient, the increased performance of these devices, will also lead to an increased need for electrical power. As a result, the need for better transfer of traceability in voltage metrology at higher voltages via devices such as voltage dividers (and current shunts for current metrology) are needed to ensure better control of electrical-power transport.

With the development of a 10:1 resistive voltage divider, and a unity gain buffer amplifier has been done for this PhD thesis (Chapter 2). The two devices have been characterized using various thermal voltage converters and high precision digital voltmeters. The purpose of these devices is to act as load-independent range-extenders in traceability of AC voltage and electrical power between various types of metrological standards. Divider and buffer combinations can be used to compare voltages with a larger amplitude to synthesized waveforms from Josephson-based setups, or they can be used together with current shunts to extend the range of electrical power that can be sampled. Results from

this work is presented in (**Article 1**).

For the main work going into this PhD thesis (Chapter 3), a technique was developed to manufacture cryogenically-operable photodiode modules based on the high-speed PD20X1 p-i-n InGaAs lensed photodiode from Albis. Tests and simulations were performed to determine the response of these modules, in liquid helium, under irradiation of pulses in the gigabit-per-second range, as well as together with actual JJAs. The main focus of this part of the thesis are the challenges going into generating current pulses from the photodiode modules, that are fast enough to generate the highest possible quantized voltages, but also have pulse peak heights that are tall enough to actually cover the first Shapiro step. The actual goal for this work was to operate a JJA to synthesize AC voltage waveforms using this photodiode module in liquid helium, which has been done successfully for unipolar waveforms. Results from this work are presented in (**Articles 2-7**).

1.2 Electrical metrology

According to the International Bureau of Weights and Measures (BIPM), "Metrology is the science of measurements, embracing both experimental and theoretical determinations at any level of uncertainty in any field of science and technology.". This is done by establishing a commonly accepted reference for these units (primary standard), and then use it to calibrate lower order standards (secondary standards). Having this ability to refer the measured value back to the original reference is what is called a traceability chain. For the most commonly used system of physical units, the SI-units, the BIPM ensures the quality of the traceability internationally, whereas national metrology institutes (NMIs) performs this work nationally.

The fundamental standard for realizing voltage is the Josephson effect [1], which BIPM in 1990 declared to replace the previous standard based on Weston cells [2]. At this time, conventional values were given to the fundamental constants involved in this phenomenon. However, May 20^{th} 2019, this all changed, when the fundamental constants will be given absolute values [3]. The junctions based on this effect is used to realize voltages according to

$$V = Mn\Phi_0 f, \tag{1.1}$$

where M is the number of Josephson junctions (JJs) in series, and n is a quantized number of magnetic flux quanta transferred in each tunneling (also known as Shapiro step). The fundamental flux quantum is $\Phi_0 = \hbar/2e \approx 2.07$ fVs, and f is the RF current frequency (which can be either a sine wave frequency, or a pulse repetition frequency) used to bias the JJs. Thus, the Josephson effect is a quantum-accurate phenomenon, traceable to the highly accurate realization of time. This realization method is best established for direct current (DC) voltage, however, methods based on both programmable binary and pulse-driven JJAs, have been used to synthesize AC voltage waveforms, and the techniques for doing so are developing fast (see section 3.2).

Currently however, then most widespread primary standards in AC voltage metrology are based on thermal converters (TCs) (see section 2.1). These converters alternately convert AC and DC voltages into heat, which is converted into a DC voltage in a thermocouple. By comparing the heat generated by applied AC and DC voltages, and calculating the load impedance of the TC, the traceability of DC voltage has been transferred to AC voltage. In the future, it is prospected that also AC voltage can be fully realized using standards based on the Josephson effect, and use them to calibrate TC to be used as secondary standards.

Because the most accurate TCs are limited to only a few volt, The traceable range of voltage is extended by using range-resistors (RRs) (more about this topic in subsection 2.1.2). These RRs make it possible to indirectly obtain traceability for voltages as high as 1000 V by using these high-precision TCs. Alternatively, high-precision voltage dividers and voltage buffer combinations can be used to extend traceability, however, these are best fitted for transferring traceability between various instruments with greatly varying load impedance, especially in transfer of traceability in electrical power metrology.

1.3 State-of-the-art survey

In metrology, voltage dividers are used to extend the range of voltages and electrical powers that can be sampled, by dividing the voltage down to by a given traceable ratio, so that it can be measured. This voltage division is performed by letting the large voltage drop over a series of impedance elements, and measuring the voltage drop over the last

element in the series. Capacitive [4][5][6] and inductive [7] voltage dividers are typically used for high-voltage applications, where the frequency range is limited. For wideband applications, with a limited amplitude, resistive voltage dividers are more appropriate. This is because the current is much less frequency dependent, however, because current and voltage are in-phase, electrical power is transferred into heat. A few generations of voltage dividers has been developed at RISE (previously known as SP) [8][9][10], as well as by Lei et al. [11] at NMI (China).

When another instrument, and especially when it is a low-impedance load, the effective output impedance of the voltage divider is altered. This changes the input-to-output ratio, which obviously affects the voltage division. In order to protect the division ratio, buffer amplifiers [11][12] or transconductance amplifiers [13] are often used as load for the divider to fix the division ratio, and maintain the ability to drive most loading instruments. To ensure the best possible frequency response, it is important to tweak the phase angle of the total effective output impedance of the voltage divider to match the phase of its input impedance. For a resistive divider, it is also impossible to avoid capacitive impacts in the form of both loading instrument (i.e. the amplifier) and internal stray capacitance [14], especially in the output stage. Consequently, the total effective output impedance of the divider consists of the components in the divider's output stage, stray capacitance, the input load of the amplifier, and any added impedance compensation. Therefore, capacitive elements are also added to the input of the divider [8], to tune the impedance phase enough that the same phase angle is achievable in the output stage. The compensation is typically an added capacitance, which is added in parallel to the output of the divider to ground, between the divider and the amplifier. As an example, RISE has built a capacitive switch-box to easily tweak this capacitance [9][10]. Another measure that has been taken to reduce the effect of stray-capacitance is to add a protective capacitive guard around the divider components [8]. Other uses of buffer and transconductance amplifiers can be to buffer the signal from a Josephson-based system to calibrate low-impedance TCs [13][15].

Pulsed operation of JJAs was first proposed by Monaco [16], and demonstrated experimentally by Benz and Hamilton [17]. This scheme is used to synthesize AC voltage wave-

forms, which require that strictly overdamped JJs be used to realize nonoverlapping Shapiro steps. These junctions typically have barriers consisting of a normal conductor, and multiple barrier materials have been tested, such as PdAu [18] and HfTi [19], but it is the $Nb/Nb_xSi_{1-x}/Nb$ junctions that are most predominantly used today [20][21]. Numerous experiments to synthesize AC voltage waveforms from pulse-driven JJAs have been done, exceeding the 1 V benchmark [22][23][24][25][26], and even reaching 3 V, at a few kilohertz [27]. In all of these experiments, multiple JJAs have been operated in parallel, with their output terminals coupled in series to increase the maximum possible output voltage. AC-coupled pulse pattern generators (PPGs) or arbitrary waveform generators (AWGs) were used to directly provide the pulse patterns for the JJAs, where one pulsation channel either operates a single JJA [24], or run through one or more Wilkinson dividers to operate multiple JJAs [26].

JJAs have in the past also been operated by using photodiodes, both at room temperature [28], and in close proximity to the JJA in liquid helium [29][30]. With this configuration, only two electrical pulsation channels, one for each polarity, are needed to provide the pulse code for bipolar operation of multiple JJAs, as splitting and amplification can be done much simpler in the optical interface, compared to the electrical. Because the JJAs are not coupled directly to the PPG, no DC blocks are needed in the signal path to the JJA. This removes the need to add a low-frequency compensation signal to the JJAs [18], although this can also be accomplished electrically, by replacing conventional pulses with ”pulse-complexes” [31]. Another advantage of this configuration is that the JJAs (and photodiodes) become electrically floating units, which means that they can be coupled without the need to make galvanic isolation between them. Electrically operated JJAs on the other hand, do need additional DC blocks to make galvanic isolation [26].

1.4 Research goals

For the research regarding resistive voltage dividers and buffer amplifiers, the goal was to make a pair that could be used to load signals up to 10 V from DC to 1 MHz from a calibrator such as the Fluke 5700A, where the buffer amplifier could put out signals from 1 mV up to 1 V. The intention was that the buffer should be able to drive measurement equipment with a vast range of impedance, from low-ohmic TCs (down to 90 Ω) to high-

capacitive digital voltmeters (DVMs) like the HP/Agilent/Keisight 3458A (up to 265 pF).

For the research surrounding the optical pulse-drive of the JJAs, the goals were defined through the EMPIR projects Q-Wave and QuADC. The goal was to develop a photodiode module with robust optical and electrical connection, to be used as an optically driven source of current pulses, in close proximity to a JJA in liquid helium. The first stage was to produce a unipolar photodiode module with the ability to produce current pulses in the gigahertz range, with pulse peak heights that are large enough to drive a JJA. This had to be verified by measuring the output waveforms of the photodiode module, under pulsed operation, while immersed into liquid helium. An optical-pulsation setup had to be constructed for the characterization of the photodiode. The second stage was to unite the unipolar photodiode module with an appropriate JJA, i.e. one that the photodiodes can be expected to properly operate (can cover the entire first Shapiro step), and synthesize DC and unipolar AC voltage waveforms. The third stage was to develop and test bipolar photodiode module under the same conditions. For a full-fledged characterization of the bipolar module, two autonomous optical-pulsation channels would be needed to produce independent bipolar pulses from the module. The fourth stage would be to join the bipolar module a JJA to synthesize bipolar AC voltage waveforms.

2. Voltage dividers and buffer amplifiers

This chapter concentrates on the development and characterization of a 10:1 resistive voltage divider and a unity-gain buffer amplifier. The purpose of these devises is to extend the range electrical powers that can be sampled, and to transfer traceability between various AC voltage standards. A variety of thermal transfer standards and digital voltmeters have been used to characterize the divider and buffer in the range from 500 mV to 50 V, and for frequencies from DC to 1 MHz.

The sections in this chapter are organized as follows: An introduction into AC voltage traceability via thermal transfer standards and how the range can be expanded using range-resistors and voltage dividers is presented in ”AC Voltage Traceability”. The concept and work with the development and testing of the voltage buffer amplifier and the resistive voltage dividers are described in ”Voltage Buffer Amplifier” and ”Resistive Voltage Divider”, respectively. The results and further work are discussed in ”Results, Discussions and Further Work”.

2.1 AC Voltage Traceability

This section is meant as an introduction to the current state of high level AC voltage traceability. The main focus will be put on TCs and their use in the traceability chain together with RRs, voltage dividers and buffer amplifiers. The involvement of DC and AC traceability via the Josephson effect will not get more than a few mentions in this chapter as it is more appropriately discussed in chapter 3 of this thesis.

2.1.1 TCs and AC-DC difference

Traceability is best tied to measurements of steady states, as these are easier to know and measure precisely than dynamical states. Consequently, producing good traceability in DC voltage is significantly easier than in AC voltage. During a DC voltage calibration, the aim is to hold the reference voltage constant during the procedure, whereas for AC voltage calibrations, the momentous voltage is intended to change continuously according to a sine wave. Although methods for synthesizing AC voltage waveforms from the JJAs, via either programmable binary or pulse-driven approaches are advancing fast [25][32],

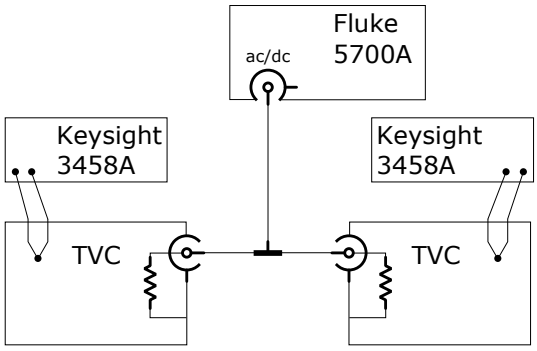

Figure 2.1: Simplified schematic of the AC-DC setup. A calibrator (here Fluke 5700A) is used to apply alternately AC and DC voltage to the two TCs, where the DC changes its polarity for every turn. One of the TCs is selected to be the reference, for which the applied AC voltage is tuned to equal the measured DC voltage, and the other is the test-object. The resistor in the TC transforms the applied electrical power into heat. This heat is converted into a voltage by the thermocouple, which is measured by the DVM (here Keysight 3458A).

the main method for realizing AC voltage traceability has been by using TCs [33]. These devices transfer AC voltage traceability, by converting the applied electrical power into heat, by which the steady state of the rms (root mean suare) value of the AC voltage waveform can be compared to that of DC voltage. This approach is used to measure the so called AC-DC difference [33].

The AC-DC difference is a measure of how closely an object measures AC compared to DC. This value is measured by a so-called AC-DC setup (see Fig. 2.1), where a calibrator (here Fluke 5700A) alternately apply AC and DC voltages to two TCs. One of the TCs is the reference, and the other is the test-object. The voltage applied to the TC is indirectly measured by converting the electrical power into heat. This heat is converted into a voltage by the thermocouple, which is measured by the DVM (here Keysight 3458A). The AC voltage from the calibrator is tuned, so that the reference measures the heat power (E_{AC}) to be the same applied DC voltage (or interpolated to be the same, see Williams [33] or Rydler [34] for reference) heat power (E_{DC}). The true values of the AC (rms value, V_{AC}) and DC (average absolute value of both polarities, V_{DC}) voltages are measured by

the test-object TC, and are put into the following formula for the AC-DC difference, δ:

$$\delta = \frac{V_{AC} - V_{DC}}{V_{DC}}. \tag{2.1}$$

A TC is most accurate, when the applied voltages close to their specified maximum are applied. This is because more heat is produced, hence; the thermocouple senses a stronger signal, and a larger SNR follows. Of course, lower voltages can be applied, but one will have to consider that the SNR is reduced, but also that the TC's load resistance is also sensitive to the temperature drop, caused by less produced heat. This limits the span of voltages that can be applied for a given uncertainty range.

2.1.2 TCs and RRs for extended traceability

A variety of TCs, specified for different voltages do exist, however, they tend to be limited to only a few volt. A proper traceability chain needs to account for voltages up to 1000 V, and in order to obtain this, RRs are placed in front of the TCs. The RR limits the current going through the TC, so that a larger voltage can be applied without overheating the TC [33]. Consequently, the measurement instrument becomes the RR and TC combination. In order to reach 1000 V, RR and TC sets must be characterized, for ever increasing voltage in a stepwise procedure to transfer the traceability to the entire range [33]. At the highest voltages, the level dependency of the resistance in the RRs can be difficult to predict accurately. Especially at higher frequencies, such as 100 kHz, even small inductive and capacitive couplings will greatly affect the AC-DC difference.

2.1.3 TCs and voltage divider with buffer amplifier for extended traceability

RRs can only be used together with specific TCs to extend the voltage range, and the AC-DC difference is only valid for a specific TC and RR pair, and in a limited voltage range. Alternatively, one can use a voltage divider with a buffer amplifier to extend the voltage range. A voltage divider attenuates the input signal with given factor. When a buffer amplifier loads the divider, this combination should be able to drive a vast range of loading instruments. Thus, a voltage divider and buffer combination becomes a self-reliant range extender. In the work for this thesis, it has been attempted to construct a voltage divider and buffer amplifier. These have been tested for a variety of loads, from low resistive TCs in the range 90-1000 Ω as well as DVMs with both high resistance (1-10 MΩ) and

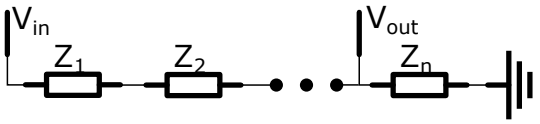

Figure 2.2: Principle sketch of a voltage divider, where V_{in} and V_{out} are the in- and output voltages, respectively, and Z_1, Z_2, and Z_n are the divider's impedance elements.

capacitance (up to 265 pF) such as Fluke 5790A and Keysight 3458A.

A voltage divider take a large input voltage, and reduces it to a smaller output voltage. It does so by letting the input voltage drop over a series of impedance elements, and then take the voltage drop over the final element in the series as output voltage. This principle is schematically shown in Fig. 2.2. The output voltage can be calculated as

$$V_{out} = \frac{Z_n}{\sum_{i=1}^{i=n} Z_i} V_{in}, \tag{2.2}$$

where V_{in} is the input voltage, V_{out} is the output voltage, and Z_i are the impedance elements, of which Z_n is the final element in the series. Since the number of elements that can be placed in a series is quite limited, the value of Z_n tend to be significantly smaller than the preceding elements for dividers with larger division ratios. Between 10 and 20 is a realistic limit of the impedance elements that can be put in series, when it is used for frequencies up to 1 MHz. Voltage dividers can be made out of resistive, capacitive, and inductive impedance elements.

Having a self-reliant range extender has its advantages in traceability transfer from TCs to more complex wide range instruments such as DVMs and calibrators. As an example, a good 1000:1 voltage divider and buffer combination for the lower voltage ranges can be used to calibrate a Fluke 5790A DVS for 1 mV in the 2.2 mV range against a TC measuring 1 V. Another example is to use such a combination together with current shunts [35] to sample an extended range electrical power using for instance multiple Keysight 3458A [36]. Lastly, with the arrival of AC Josephson setups for voltages surpassing the 1 V milestone, for both the programmable binary, and the pulse-driven approaches [25][37], 1000:1 combinations can be used to compare 1000 V from calibrators to the spectrally pure 1 V signals realized by these setups.

2.2 Voltage buffer amplifier

This section describes the development of the voltage buffer amplifier. Simulations of the various buffers designs were performed in LTSPICE using provided models for the transistors and the amplifier unit. A buffer reduces the load effect that the measurement equipment has upon the voltage dividers, especially when it comes to low-impedance TCs. The intended use of the buffer was to sustain the output of voltage dividers, so that they could be calibrated using TCs and high-precision DVMs. The calibration value can then be used to transfer traceability to a variety of standard instruments in both AC voltage and electrical power metrology.

2.2.1 Basic and specific requirements for the voltage buffer amplifier

The basic idea of a voltage buffer (in the non-RF case) is to act as a perfect ”voltage copyer”, with an infinite input impedance to avoid loading the signal source, and an infinitesimal output impedance to avoid dividing down of its output voltage.

Being a perfect ”voltage copyer” entails two features; having a voltage and frequency independent gain of exact 1 V/V, and having absolutely no harmonic distortion and phase displacement. In most cases, the exact 1 V/V gain is not really important as long as it is ”close enough” and repeatable. As a rule of thumb in AC voltage metrology, we can say that a gain within $\pm$1% of unity gain is acceptable, as long as the DC transfer function is linear. The linear transfer function is expressed as

$$V_{out} = aV_{in} + b, \tag{2.3}$$

where V_{in} and V_{out} are the in- and output voltages, respectively, a is the gain, and b is the offset, which should be as close to zero as possible. A voltage dependent gain will lead to a large AC-DC difference already for low frequencies. This is because the instantaneous voltages during the span of an entire cycle will be copied with varying gain, which on average will have the potential to differ from the DC gain. The result is an output sine wave that is deformed, and where the RMS value has been transferred with a different gain than the DC value. Therefore, the DC gain of the buffer should not vary more than 1 μV/V over the entire operating voltage range one intends to use it. The frequency dependance of the gain is less critical, as it is easier characterized and compensated for in

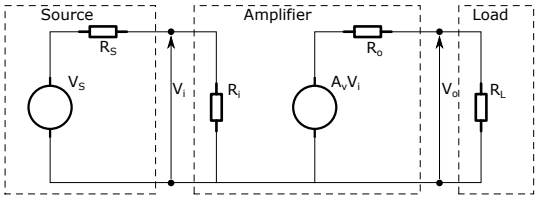

Figure 2.3: Schematic of load dependency of a voltage buffer.

the calculations.

The issue of in- and output impedance of the buffer can be seen from the principle sketch in Fig. 2.3, where the buffer's input loads the source, and its output drives the load. The voltage of interest is the source voltage V_s, however, it is the buffer's output voltage V_o that is measured. At the input of the buffer, V_s is divided down to $V_i = V_s Z_i/(Z_s + Z_i)$. At the output, and assuming A_v=1, The voltage is further divided down to $V_o = V_i Z_L/(Z_o + Z_L)$. Thus, V_o is least altered from V_s when Z_i is large and Z_o is small.

The buffer design has been developed in four generations, where one has even been operated in liquid nitrogen (see subsection 2.2.6). The initial design was inspired by an audio amplifier design based on Darlington-type coupling. The NPN and PNP bipolar transistors were chosen to be as complimentary as possible, and to have the best overlap for the intended operation range. For the latter clause, collector currents of at least 100 mA were to be selected, with frequency range up to a few GHz. Initially, the through-hole transistors NTE2633 (NPN) and NTE2634 (PNP) transistors were used. Later, when the design development was moved to printed circuit boards (PCBs), surface-mount device (SMD) components were more appropriate, so the SMD transistors BFQ19 (NPN) and BFQ149 (PNP) transistors were chosen.

2.2.2 Other buffers in AC voltage metrology

The development of the voltage buffer draws its inspiration from a few previously developed voltage buffers. Perhaps most notably, is the series of buffers developed by Budovsky et al. [12][38]. The basic design principle for these buffers is to have cascading buffer stages, where the successive stage tries to compensate for the error in the amplification of its previous stage.

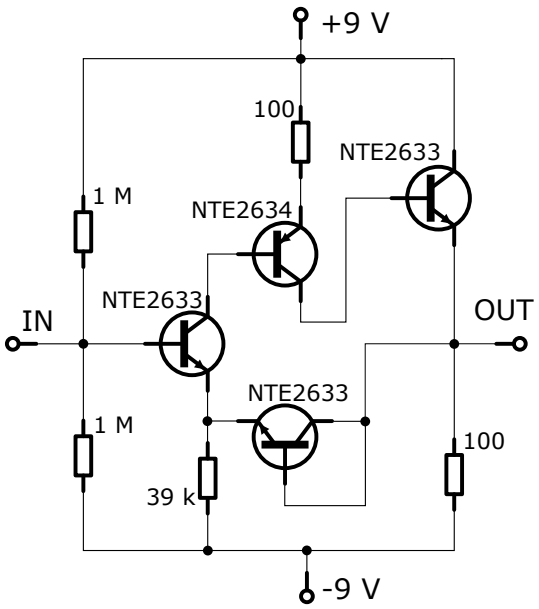

Figure 2.4: Schematic of the 1^{st} generation voltage buffer.

Voltage buffers and transconductance amplifiers have many uses in voltage and electrical power metrology. They can be used to guard the division ratio of a voltage divider [9][11], **Article 1**, so that the divider is loaded by a more or less fixed and high impedance, with negligible impact from the load impedance of the measurement instrument. They can also be used to calibrate TCs, by using an input signal from a Josephson synthesized waveforms as the standard. Séron et al. [15] and Budovsky et al. [13] used a buffer amplifier and transconductance amplifier, respectively, to amplify the signal from a programmable binary JJA, to measure the AC-DC difference of a planar multijunction TC (PMJTC).

2.2.3 The 1^{st} generation buffer

The first design (schematically depicted in Fig. 2.4) was based on a single Sziklai pair (or complementary Darlington pair) [39] with a diode coupled feedback. A Sziklai pair consist of two successive bipolar transistors (each of which has a base-to-collector current-gain factor β), where either the NPN drives the PNP, or the PNP drives the NPN. The signal is applied to the base of the first transistor, whose collector drives the base on the second transistor. The signal is then extracted from the collector on the second transistor, which has been amplified twice with this configuration, and hence, it is a β^2 amplification. The diode-coupled feedback is coupled from the output of the circuit to the emitter of the

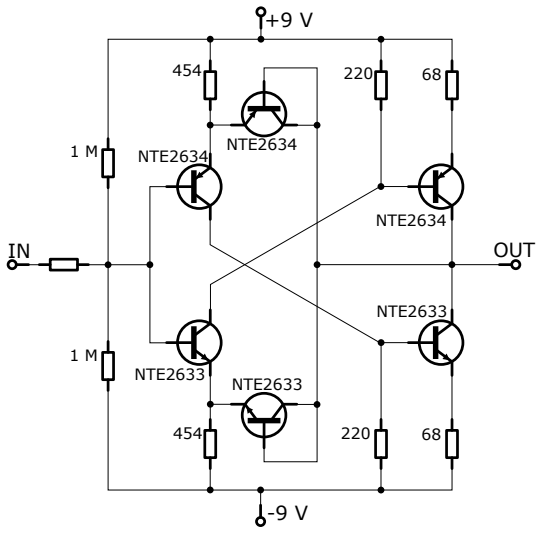

Figure 2.5: Schematic of the 2^{nd} generation voltage buffer.

input transistor. This coupling forces the voltage on the output terminal to follow that of the input terminal via a common-emitter coupling.

The transistors NTE2633 (NPN) and NTE2634 (PNP) were used in this design, where an NPN was driven by the input, and followed by a PNP to drive the output. In order to increase the available output current, the collector of the PNP transistor was fed to the base of an additional NPN transistor, with collector coupled directly to the positive supply voltage, and the emitter directly to the output terminal. Unfortunately, the output waveforms were heavily distorted, where an input sine wave put out a triangular wave. Even though the signals might have been improved by a better selection of component values, this design was discarded for a more promising push-pull design.

2.2.4 The 2^{nd} generation buffer

The second design, schematically depicted in Fig. 2.5, is greatly revised from the previous design. This version of the buffer is also based on typical audio amplifier design, where two complimentary Sziklai pairs are used in the amplification of the signal, both with diode-coupled feedback. The transistors used are still NTE2633 (NPN) and NTE2634 (PNP). This design was considered to be more promising, since the same transistor mechanisms is used to reproduce both the positive and negative halves of the signal, thus forming a push-pull amplification. For the previous design, the output transistor worked

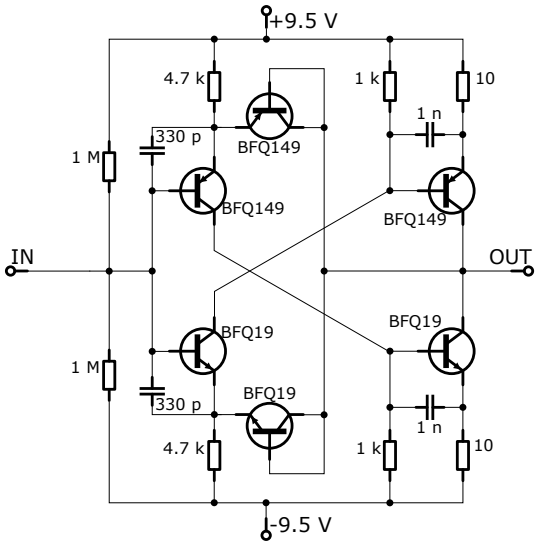

Figure 2.6: Schematic of the 3^{rd} generation voltage buffer.

as a current feeder for positive voltages, and a choke hold for negative. In this design, the output PNP transistor is a current feeder and the NPN is a choke hold for positive input voltages, and vice versa for negative input voltages. This configuration has a wide dynamical range, with output peak voltages approaching that of the power supply. Because of a small 250 MHz stray oscillation in the design, the 50 Ω series resistor was introduced into the design. This modification seemed to remove the oscillation.

Signal frequencies up to 1 MHz were applied, and the output signals were significantly less distorted than in the first generation. However, the signals were still quite noisy. Because of the significant improvement in the output waveforms at 1 MHz, compared to that of the first generation, it was decided to continue using complimentary Sziklai pairs as a basis for the following buffer designs, and improve the circuit layout.

2.2.5 3^{rd} generation buffer

In order to reduce the overall design and to obtain a better control over the coupling noise, the designing process was continued using SMD components on self-etched PCBs made out of flame retardant (FR4) material. This alteration meant that through hole transistors were replaced by SMD transistors, with the new schematic shown in Fig. 2.6. At the time, it was decided to sacrifice some of the collector current margin of the transistors to

the advantage of an increased bandwidth, because it was envisioned that this would improve the response at frequencies close to 1 MHz. Therefore, the transistors BFQ19 (NPN) and BFQ149 (PNP) were chosen. They both have 100 mA maximum collector current and bandwidths of 5.5 GHz and 5.0 GHz, respectively.

An important alteration from the second to the third design, is the inclusion of the 330 pF and 1 nF base-emitter capacitors in the in- and output transistors, respectively. These capacitors serve as low-pass filters for the in- and output signals, by redirecting the current from the base terminals at higher frequencies (>100 MHz). The inclusion of these, completely removed the GHz oscillations in this design.

Even though the buffer seemingly put out smooth waveforms, the measurements of the AC-DC difference had a relatively large offset as shown in Fig. 2.7. This is obviously not good, and this offset is both dependent upon load impedance and applied voltage. In order to investigate these discrepancies, DC simulations were performed for the voltage spans $\pm$1.5 V and $\pm$7.5 V, eclipsing the entire span of voltages for 1 V and 5 V rms, respectively. A linear, DC-coupled buffer amplifier would put out voltages according to equation 2.3, with a gain a=1 V/V, independent upon input voltage, and offset b=0 V. Based on the two DC sweeps, the least-squares methods was used to derive two models of equation 2.3. The models were subtracted from the simulated data, according to

$$\Delta V = V_{out,sim} - V_{out,lsq}(V_{in}), \tag{2.4}$$

where ΔV is the model error, $V_{out,sim}$ is the simulated voltage, and $V_{out,lsq}(V_{in})$ is the linearized model, constructed based on the simulated output, using the least-square method. The model errors are plotted to the top and bottom of Fig. 2.8, for 1 V and 5 V models, respectively. The model errors range from -10 μV to +100 μV in the 1 V sweep, and -13 mV to 15 mV in the 5 V sweep. Therefore, the average gain over one period of the AC voltage will most likely differ from that of DC voltage, even at lower frequencies (around 10 Hz). Consequently, the output voltage of AC and DC voltage is different, which will lead to voltage dependent AC-DC difference, as shown in Fig. 2.7.

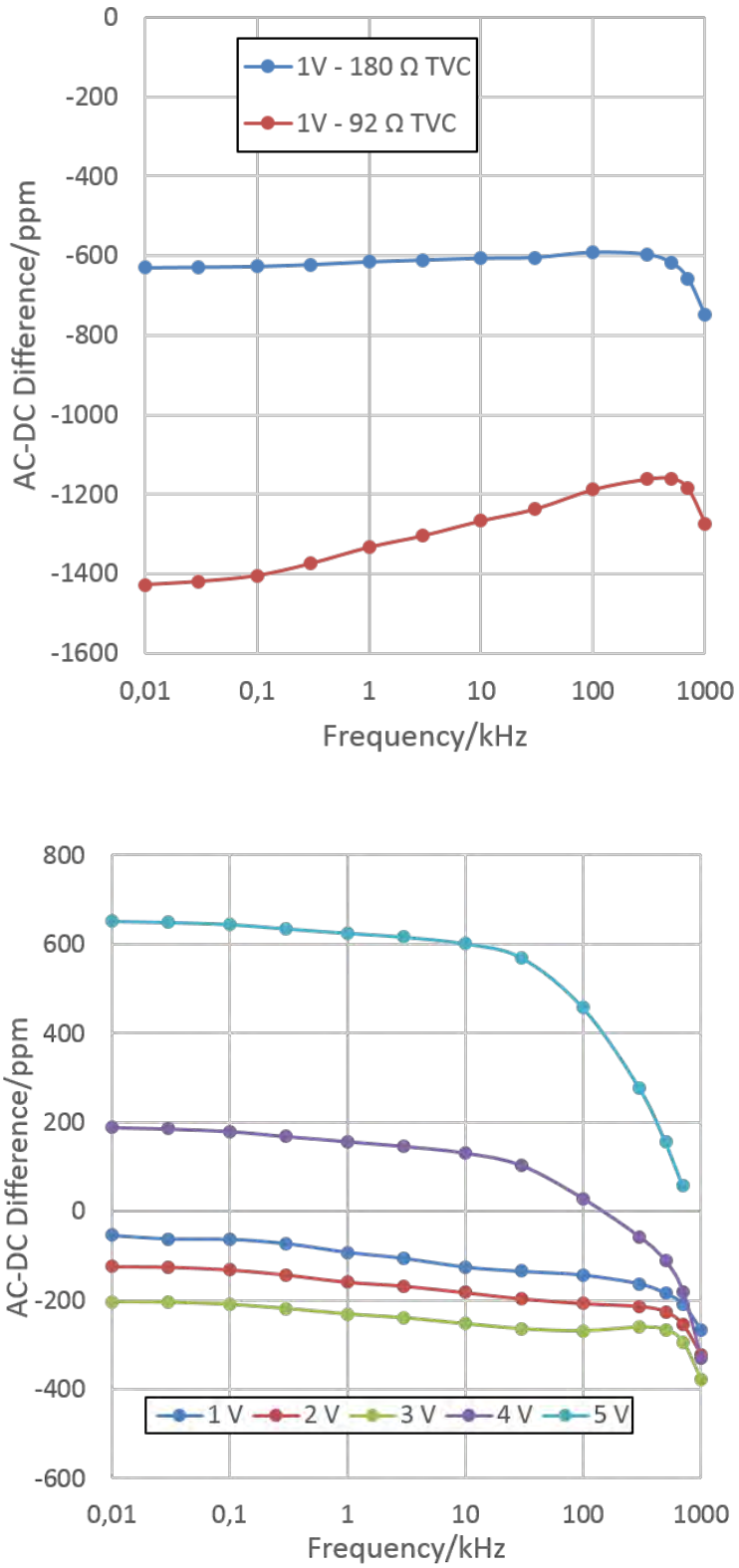

Figure 2.7: The measured AC-DC difference of the 3^{rd} generation buffer. Top: The AC-DC difference for 1 V, using 92 Ω (red) and 180 Ω (blue) TCs as load. Bottom: The AC-DC difference for 1-5 V, using 1 kΩ TCs as load.

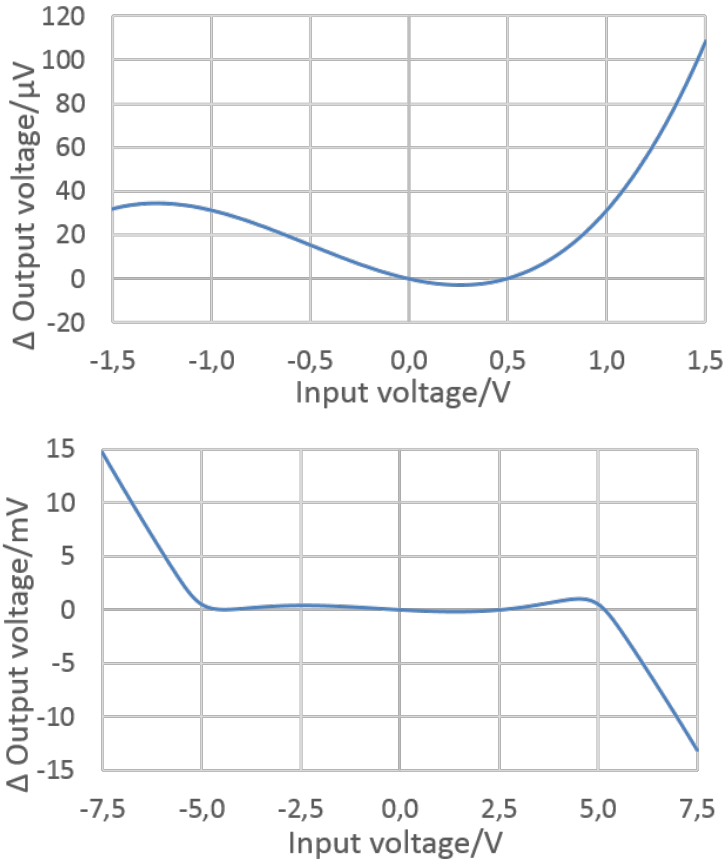

Figure 2.8: Simulated output error from constant amplification. Top: Output error from the gain at 1 V for the ±1.5 V sweep. Bottom: Output error from the gain at 5 V for the ±7.5 V sweep.

2.2.6 Cryogenic buffer

A sidestep to the third generation buffer, was the version modified for operation at cryogenic temperatures. The purpose of this version was to amplify the signal from a JJA array, before loading it by instruments such as a TC, in a similar fashion as has already been done by Séron et al. [15]. For this buffer it was intended to operate the buffer cryogenic temperatures, and using a Josephson arbitrary waveform Sythesizer (JAWS) setup as a basis. The reason for this is to place the buffer amplifier as close as possible to the JJAs to as far as possible avoid damping and distortion of the realized signal before amplifying it. The buffer would have been placed in a warmer outer chamber of the cryostat.

In order to make a cryogenically operable buffer amplifier, two issues needed to be confronted. First issue was the survivability of the circuit for the thermal cycling, where the main focus was directed towards the transistors. For the purpose of testing this, three samples were prepared. One NPN transistor was conventionally soldered to an FR4 circuit board, using standard lead-tin soldering thread, and one of each transistor-type, unsoldered. The test was performed by simply immersing the transistors into a container with liquid nitrogen, and then letting them reheat in lukewarm water. This procedure was repeated roughly 50 times. The survivability was determined by measuring the two diode voltage drops in each of the transistors before each dipping into liquid nitrogen. The soldered transistor started to malfunction after about 10 immersions into the fluid as the base collector voltage changed notably. The two unsoldered transistors on the other hand, no change could be detected in diode voltage drop throughout the 50 immersions. The conclusion form this test was that the transistors themselves survive the thermal cycling, but only if they are not conventionally soldered. The suspected reason for the transistor breakdown was that the transistors could not withstand the mechanical stress that occurs due to differences in thermal expansion when soldered conventionally.

The first attempted solution was to use a softer material in order to solder the transistors with a softer material to let the transistors move more freely. An amplifier unit was made using indium instead of standard lead-tin soldering thread. This unfortunately failed after a few cycles as the waveform started to be heavily distorted.

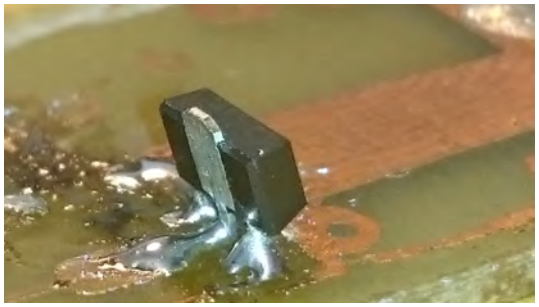

Figure 2.9: Close-up picture of the soldering technique for the cryogenic buffer. The transistor is soldered in a tilt to avoid mechanical breakdown of the transistor at cryogenic temperature.

The second attempted solution was to use an alternative technique for soldering the surface mounted components. Instead of soldering the transistors flat onto the PCB, they were soldered with only the tips of the pads touching the PCB as shown in Fig. 2.9. This way the large collector plate could move freely. The hypothesis was that the thermal cycling would affect the transistors the same way as the two unsoldered transistors. This solution however seemed to survive multiple thermal cycles without any notable distortion in the waveform, for a 1 MΩ load. Further electrical tests could now be performed.

As will be discussed in chapter 3, the general target amplitude for JAWS setups has been the 1 V waveform. For this reason, it was determined to test the minimum load resistance at which the buffer could put out a 1 V signal. This was done by using a standard signal generator as a source to produce a 1 V signal at 1 MHz. This signal was applied to the buffer, which was loaded by a 1 MΩ oscilloscope. The buffer was then immersed into a container with liquid nitrogen. After checking that the output waveform remained a sine-wave, the minimum load resistance was found by shunting the oscilloscope input using hole mounted resistors in the range 100 Ω to 10 kΩ. From this investigation, it turned out that the limit where the waveform begins to notably deform is at about 500 Ω.

With the knowledge that the buffer needs a minimum load of 500 Ω to maintain a 1 V signal at 1 MHz, it was determined to perform an AC-DC characterization of the buffer in liquid nitrogen, using 1 kΩ TCs. However, these TCs are intended for 5 V, so the signal measured by the thermocouple will be only at 1/25 of maximum. Consequently, the

standard deviation in the measurements will be quite large. Still, a measurement series of the AC-DC difference was measured, using the 1 kΩ TCs, with the results for 10 Hz to 30 kHz and 100 kHz to 1 MHz given to the top and bottom of Fig. 2.10, respectively.

Up to 30 kHz, the AC-DC difference of the buffer stays within $\pm$ 85 μV/V, which in itself is better than what it manages at room temperature (see the AC-DC difference in Fig. 2.7 as a reference). However, the fact that the AC-DC difference varies 170 μV/V in this frequency range is not an improvement. Further, already at 100 kHz, the AC-DC difference exceeds 1 mV/V, and even reaches 6.5 mV/V at 1 MHz. Although a cryogenic voltage buffer is interesting as a proof-of-concept, this current design is obviously not suitable for transfer of traceability.

2.2.7 4^{th} generation buffer

As explained towards the end of subsection 2.2.5, the gain of the third generation buffer was nonlinear with respect to the applied voltage, so measures had to be taken to rectify the output. Looking at works done by Budovsky and Hagen [12] and Lei et al. [11], it is a known issue that a single stage amplifier may be insufficient to produce a signal close enough to the input. In both of these cases, one buffer stage is used to produce an output that is used as a signal ground for the successive buffer stage. In the case of Budovsky, four buffer stages have been used, whereas Lei only used two stages. This way, the first buffer produces a rougher signal, which is tuned by the successive stage.

The solution for the fourth generation buffer was to couple the correctional buffer unit in parallel with the main buffer unit. The idea was that the main buffer unit still would produce the same slightly deformed waveform, and then the correctional amplifier would sense the deviation between input and output, and rectify the response. Ideally, the new result of the difference between output and linearized model should be closer to zero. The buffer unit used was the LM6171 from Texas Instruments, coupled as a non-inverting follower, in parallel with the buffer core. This solution proved to be quite successful as can be seen by the simulated DC and AC sweeps of 1 V to the top and bottom of Fig. 2.12, respectively. The input impedance of the design was simulated to be 155 kΩ in parallel with 16 pF.

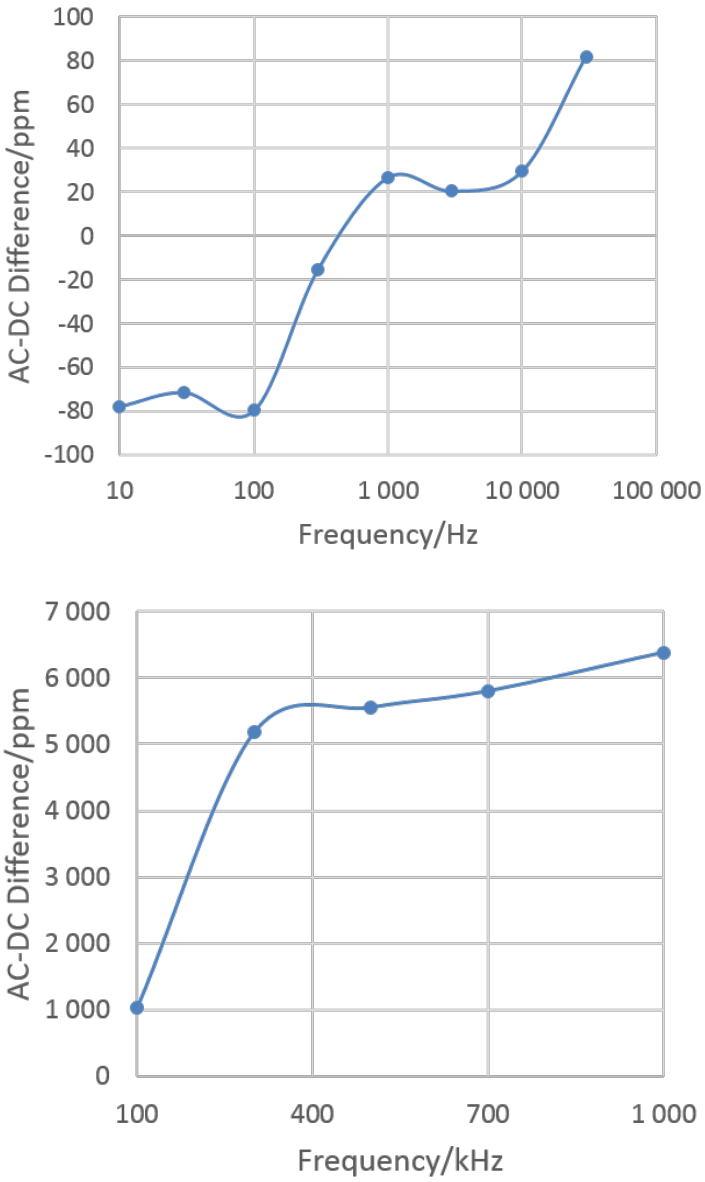

Figure 2.10: The measured AC-DC difference of the buffer in liquid helium. Top: The AC-DC difference from 10 Hz to 30 kHz. Bottom: The AC-DC difference 100 kHz to 1 MHz.

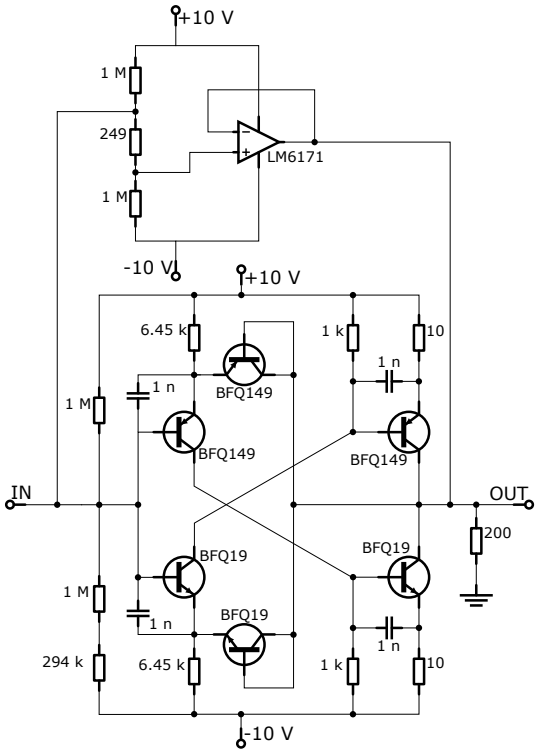

Figure 2.11: Schematic of the 4^{th} generation voltage buffer.

2.2.8 Summary of the development of buffer

The first generation buffer was based on a single Sziklai pair with a diode-coupled feedback. Trough-hole transistors were used. An additional NPN transistor was coupled into the collector of the output PNP transistor to further amplify the current of the output signal. Still, the output was heavily distorted, putting out triangular waves from sine wave inputs. The second-generation buffer was based on two complimentary Sziklai pairs (opposite configurations of NPN and PNP transistors) with diode-coupled feedback to form push-pull amplification of the current. There was a problem with 250 MHz stray oscillations, which were removed by adding a 50 Ω series resistor on the input. The output waveforms, especially at 1 MHz, were still noisy. For the third generation buffer, it was decided to put the buffer circuit onto a PCB in the hope that this would reduce the noise caused by stray interactions between the components. For this design, the trough-hole transistors were replaced by SMD transistors with an even higher bandwidth (about 5 GHz). In order to remove the stray oscillations up to the gigahertz range, basee-emitter capacitors were added to the in- and output transistors in the Sziklai pairs to quench the

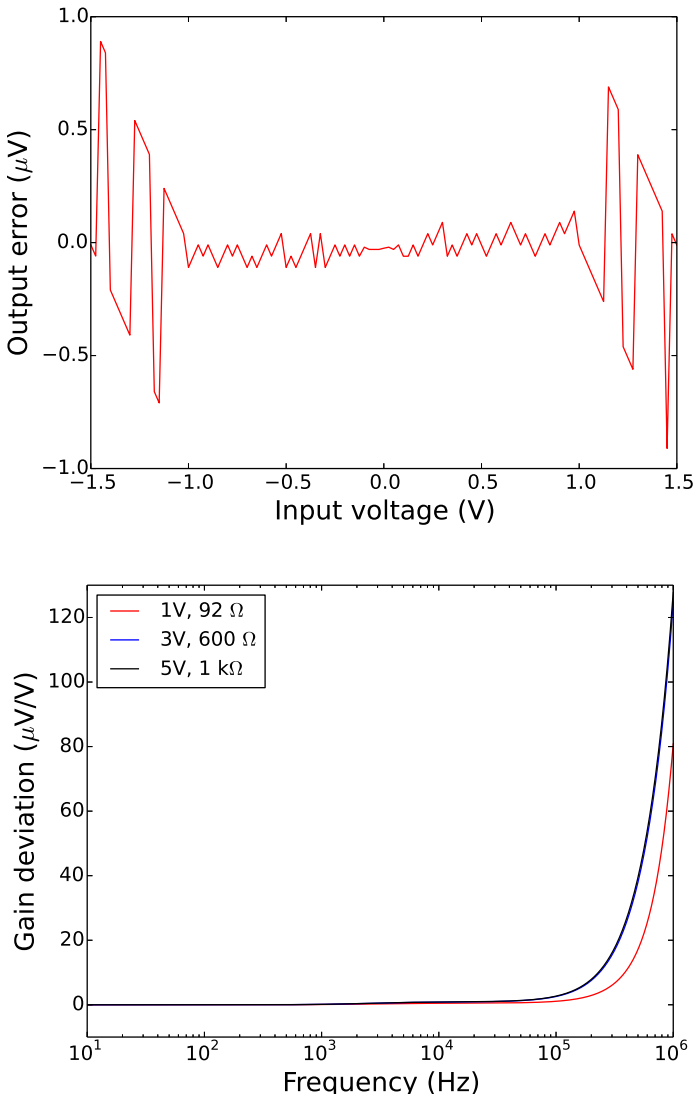

Figure 2.12: Simulated DC and AC sweeps of the 4^{th} generation buffer Top: Output error from the gain at 1 V for the $\pm$1.5 V sweep. Bottom: Deviation in absolute gain for 1 V rms input from that at 10 Hz. Simulated loads of 92 Ω, 600 Ω and 1 kΩ have been used to resemble the TCs typically used at Justervesenet (JV).

amplification for these frequencies. The output signal from this generation of buffers was a lot less noisy, however, off-sets at a typically a few 10^{-4}. Through simulations, it was discovered that the gain of the buffer was not completely linear for DC, rather, the amplification was slightly dependent upon input voltage. In the fourth generation buffer, a low-distortion operational amplifier was added in parallel to the Sziklai-based buffer core to straighten the linearity. Both according to simulations and measurements, the DC gain was linear to within 10^{-6}, except for a small region around zero in the measurements. This design culminated in (**Article 1**), where both absolute AC gain and AC-DC transfer were measured.

2.3 Resistive voltage divider

This section describes the development of the resistive voltage divider as well as plans for further developments. The main focus is put upon this first prototype of a 10:1 voltage divider for operation in the input range 5-50 V in the frequency range from DC to 100 kHz. These voltage dividers are intended to be loaded by the voltage buffer described in the previous section.

2.3.1 Basic and specific requirements for the voltage dividers

As stated previously, voltage dividers can be made out of resistive, capacitive, and inductive impedance elements. The choice between the different elements have their benefits and downsides, which will be discussed further in the next subsection. The most common choice for metrological purposes is perhaps resistive voltage dividers. Voltage dividers of this type has previously been made in multiple generations at RISE (previously known as SP) [8][9][10], and by Lei et al. [11]. Capacitive voltage dividers have been constructed for high-voltage metrology by Shao et al. [4] and Mohns et al. [5]. A three-stage inductive voltage divider has be constructed by Small et al. [7] for frequencies in the 50-1000 Hz range.

The frequency range for the voltage dividers made out of reactive elements are quite limited. This is because the impedance scales with or inverse to the frequency for inductive and capacitive elements, respectively. By going outside a given frequency range, the current becomes either too large for the source to supply, or too small to measure the

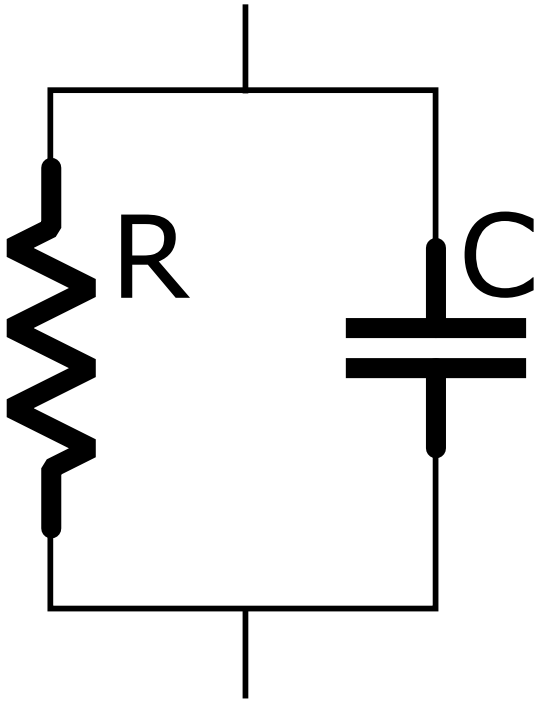

Figure 2.13: Equivalent schematic of a SMD resistor, with the nominal resistance R, and the parallel parasitic capacitance C. For frequencies up to 1 MHz, the inductance is small enough to be neglected.

voltage accurately. Obviously, a resistive voltage divider can take a much wider range of frequencies, since these elements ideally are frequency independent. On the other hand, for reactive elements, the current-voltage phase difference is $\pi/2$, i.e. completely out of phase. This is beneficial when high voltage (beyond 1 kV) is applied, because no transfer of electrical power into heat in this case. Resistive voltage dividers have no current-voltage phase difference, and therefore, a significant amount of heat is produced. Because of these differences, resistive voltage dividers are best used to wideband signals, with a limited voltage range, and inductive and capacitive voltage dividers are best used for high-voltage applications, with a narrow span of frequencies.

2.3.2 Nonideal behavior in real resistors and structures

For resistive voltage dividers, the frequency is limited by both parasitic contributions in the resistive elements, and parasitic elements caused by the geometry of the device itself. In metallic film SMD resistors, the realistic equivalent schematic for this component

is shown in Fig. 2.13. Here, R is the resistance of the metal film, and C is the parallel parasitic capacitance between the two contact points in the component, through its ceramic substrate. The series inductance caused by the metal film (in the nH range) is negligible to the resistance for frequencies up to 1 MHz. The resulting formula for the impedance, Z, for these contributions become

$$Z = R/(1 + j\omega CR), \tag{2.5}$$

where $\omega = 2\pi f$ is the phase frequency and j is the imaginary number. At higher frequencies, the parallel capacitance becomes significant for the balancing of in- and output impedance of the divider. In order to accomplish this, the following must be fulfilled:

$$R_i C_i = R_o C_o, \tag{2.6}$$

where R_i and C_i are the input resistance and capacitance, respectively, and R_o and C_o are the output resistance and capacitance, respectively. For larger division ratios, R_i will become much larger than R_o, and therefore, C_o will have to be increased with respect to C_i.

The structure of the divider itself also make capacitive contributions, which causes leakage currents. The conductive areas in the divider becomes electrodes in a capacitor, and with voltage gradient in the divider, the leakage currents can become large compared to the input current, and must be considered, carefully. For higher division ratios, such as 400:1 and 1000:1, the series of resistors need to be protected, so that the current profile in the divider follow the resistance, and hence the intended voltage profile. Because the input voltage in these dividers are quite high (up towards 1 kV), the resistance must be significantly larger to limit the power consumed by the divider, which reduced the operating current even further. Because the voltages inside the divider is increased, the leakage current is increased. To counteract the effects of this issue, such voltage dividers must be equipped with a capacitive guard [8] to protect the divider elements from leaking current to chassis. For smaller division ratios, such as 10:1 and 40:1, the current leakage becomes relatively small, which makes the guard unnecessary.

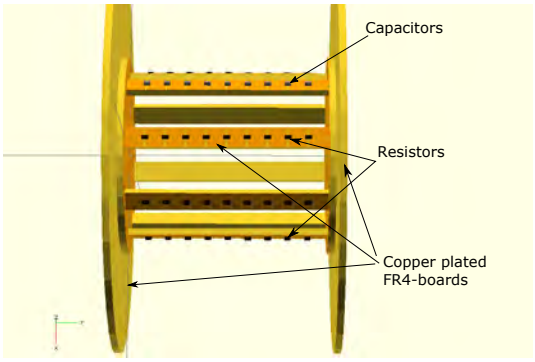

Figure 2.14: Drawing of the opened version of the voltage divider. The FR4 material is in yellow, the copper plating is brown/orange, the resistors are black, and the capacitors are grey.

2.3.3 Voltage divider construction

A 10:1 resistive voltage divider, with capacitive compensation, was constructed, intended for use together with the voltage buffer described in section 2.2. The first intended voltage source for the voltage divider is the Fluke 5700A, and therefore, the total resistance of the divider was chosen to 2 kΩ, so that the DC current at 10 V input was limited to 5 mA. The resulting output resistance was therefore 200 Ω.

Any load put on the voltage divider, comes in parallel to the output impedance, and has the potential to greatly influence its division ratio. The voltage buffer on the other hand, has little dependence upon the loading instrument, and has a more or less fixed input impedance. Therefore, the buffer can be used as a constant load for voltage divider, and all impedance phase considerations can be limited to only the voltage buffer.

The voltage divider (opened version is shown in Fig. 2.14), is constructed as a cylinder, with copper plated FR4 boards on in- and output sides, equipped with female and male N-connectors, respectively. The chassis for the return-current is a folded copper plate. The input resistors are soldered in series of 9, onto 7 strips of FR4 material, and one strip with 9 capacitors in series. These 8 strips are connected to the center conductors of the in- and output N-connectors, via a copper plate FR4 boards. The resistors used for the input were 1.4 kΩ SMD components, forming an input resistance of 1.4 kΩ*9/7=1.8 kΩ. For the capacitive strip, 330 pF SMD components were used, forming a capacitance of

330 pF/9=36.7 pF. The output resistance consists of 5 parallel coupled 1 kΩ SMD components, forming an output resistance of 1 kΩ/5=200 Ω. Thus, the total resistance becomes 1.8 kΩ+200 Ω=2 kΩ, which leads to a division ratio of 2 kΩ/200 Ω=10. There is no need to compensate the output resistance for the buffer's load resistance, since it (according to simulations) is at 155 kΩ (see the end of subsection 2.2.7). The load resistance alters the output resistance by less than 0.2 %, which is comparable to the tolerance of the resistors.

It is of course also important to consider the divider's output capacitance so that equation 2.6 is fulfilled. Here, the buffer's capacitive load becomes relevant, since it (according to simulations) is 16 pF (see the end of subsection 2.2.7). Furthermore, the copper plates, which are separated by the wall on the output of the divider, forms another parallel capacitance for the output of the divider. This capacitance is difficult to predict accurately, however, it can be estimated according to the area and distance of the copper plates to be roughly 55 pF. Because of these relatively large capacities, the strip of input capacitors mentioned in the previous paragraph was introduced, so that the output capacitance could be tweaked by adding more capacitance to the output. Since the exact capacitance needed on the output is difficult to predict accurately enough, the output capacitance was moved to a separate capacitive box, coupled in parallel to the divider's output and the buffer's input. A first "best guess' for the needed capacitive compensation was made, and then optimized through trial-and-error, by measuring the AC-DC difference. Fast measurement series were performed in the AC-DC setup, for various added output capacities. The aim was to find the capacity, at which the AC-DC difference at higher frequencies (100 kHz-1 MHz) was smallest. The result from these series is shown in Fig. 2.15, and a nominal capacitance of 285 pF was found to be the best fit.

Another conclusion from these optimization measurements is that the AC-DC difference is more or less stable for frequencies up to 100 kHz, however, from 100 kHz to 1 MHz, the AC-DC difference is greatly influenced by small changes in the added capacitance. Therefore, the uncertainties will become too large to make use of the divider for frequencies above a few 100 kHz.

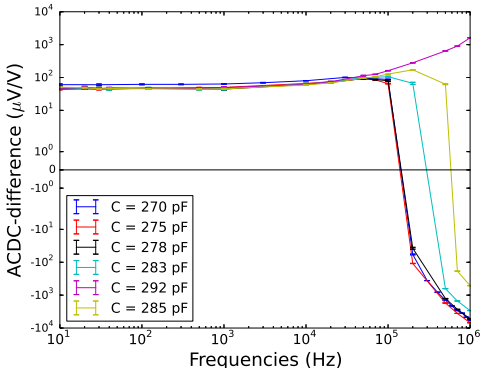

Figure 2.15: Optimization of the output capacitance, where labels refer to the capacitance that was added on the divider's output. The labels are ordered chronologically, according to when the measurements were performed. We selected 285 pF as the best fit, although 292 pF is also a good candidate.

2.4 Results, Discussions and Further Work

This section briefly summarizes the results and conclusions from the attached (**Article 1**). Plans for future developments are also discussed.

2.4.1 Results Summarized

The work described in this chapter, has resulted in the construction of a 10:1 resistive voltage divider and a buffer amplifier, suited for use in electrical power metrology, and possibly also for AC voltage. Characterizations have been performed, both of AC-DC difference using various types of TCs, and of absolute gain using the high-precision DVM Fluke 5790A. These methods have produced overlapping results for the buffer alone in the voltage range 1-5 V, with AC-DC measurements performed up to 1 MHz. Similar results have also been obtained for the voltage divider and buffer combination in the voltage range 10-50 V, with AC-DC measurements performed up to 100 kHz. As mentioned in subsection 2.2.6, measurement of a voltage buffer in liquid nitrogen has also been performed for 1 V, using 1 kΩ TCs.

2.4.2 Further improvements to the buffer amplifier

In (**Article 1**), Fig. 8 shows that there is an offset in the AC-DC difference for the voltage divider and buffer combination. This is most likely due to a DC current sourcing from the buffer input onto the output stage of the divider. This gives rise to an extra DC voltage component to the input of the buffer. The DC shift will not affect the DC measurements due to the averaging of the positive and negative DC values, but it will make a net positive contribution to the AC measurements. Because the buffer is intended to be used to amplify both AC and DC voltages, DC blocks cannot be used to avoid sourcing. However, fine-tuning the bias for the bases on the in- and output transistors using potentiometers can potentially be used to quench the current sourcing, by making a more precise transfer of operation between the input transistors at zero applied voltage.

2.4.3 Further improvements to the voltage divider

With increased applied voltage, more electrical power is dissipated into heat in the divider, and hence increases the temperature in the resistors. This alters the resistor values, and therefore also the division ratio. As Fig. 6 in (**Article 1**) shows, the division ratio increases linearly when the applied voltage is increased. In future voltage dividers, this dependency will be reduced by selecting resistors with a smaller thermal resistive coefficient. The FR4 substrates will be replaced with ceramic materials, such as alumina or aluminum-nitride, to improve the heat conductivity. Dissipation of heat is especially important for dividers of even higher division ratios, as the applied voltage will be much higher. Furthermore, a carefully constructed capacitive guard will be included to avoid capacitive leakage from divider to ground/chassis.

2.4.4 Further improvements to the output capacitance

As stated in subsection 2.3.3, only a single capacitor box, with a fixed capacitance was made. This is because only a first prototype 10:1 voltage divider was made for the one successful buffer amplifier, and therefore, a box with a fixed capacitance is applicable. For a series of voltage dividers, with division ratios up to 1000:1, it is much more practical with an adjustable capacitor box, such as the one used by RISE [9], where the capacitance is selected by on/off switches. This makes it easier to fine-tune the output capacitance,

by selecting between numerous combinations of fixed-value capacitors.

3. Josephson effect

This chapter concentrates on the research to make a cryogenically-operable optical pulse-drive, which has been used to realize the Josephson effect [1]. After almost three decades of research, in 1990, BIPM declared [2] that the Josephson effect had replaced the old Weston cells as the fundamental voltage standard. At the time of this announcement, Lloyd et al. [40] had already constructed a setup, based on the Josephson effect, which had been used to generate DC voltage up to 10 V. Since this accomplishment, work has been done to exceed the 10 V benchmark for AC voltage for the two approaches, namely programmable binary JJAs [41] and pulse-driven JJAs [17]. The first of these methods is better fitted for realization of high voltage at low frequencies (up to 1 kHz). The latter is better fitted for synthesizing arbitrary waveforms and frequencies up to 100 kHz, but it has some challenges related to reaching higher voltages.

High-precision ADCs and DACs have developed fast during the last decade, in terms of speed, accuracy, resolution, and power consumption. This has led to the need to improve the AC voltage realization, so that these converters can be calibrated up to their best performance. Therefore, much work has been done internationally, to push the performance of pulse-driven Josephson setup in terms of output voltage magnitude, frequency, and spectral purity. Currently, the record is at 3 V, and it is desired to reach 10 V, so that the full range of the converters can be directly calibrated using these setups as standard. Obviously, an increased range of frequencies that can be synthesized with good spectral purity will make available wideband calibration of these converters with less uncertainty.

One of the proposed solutions to reach higher voltages in pulse-driven Josephson setups is to use an optical pulse drive to operate photodiodes, in liquid helium, to bias the JJAs. To accomplish this, techniques had to be developed to manufacture photodiode modules, which are operable in liquid helium. These modules must be able to produce current pulses, with peak currents sufficient to realize the Josephson effect, and narrow enough to allow for a high pulsation bit rate. In order to produce these fast current pulses, an accompanying laser-pulsation setup is also needed. It must be based on an appropriate

optical wavelength, and be able to match the photodiodes in both power and pulse width.

The sections in this chapter are organized as follows: The historical and theoretical background of superconductivity, leading to the Josephson effect is presented in ”Historical background”. A description of the Josephson effect, and its applications in electrical metrology is presented in ”The Josephson effect and metrology”. The principle of Josephson arbitrary waveform synthesizer (JAWS) via the pulse-driven JJA approach, and the JAWS setup used in the experiments for this thesis is presented in ”Josephson arbitrary waveform synthesizers”. Various simulation schemes of pulse-driven JJAs based on the Stewart-McCumber model, including the one used in the results section of this thesis, are presented in ”JAWS simulation schemes”. The different photodiode modules, including the COMSOL simulation model, and the challenges in producing photo-electrical pulses in liquid helium are described in ”Photoelectrical pulses at 4 K”. The various test setups used to high-speed testing, of the photodiode modules, as well as the JAWS system are presented in ”Experimental setup”. The results from the tests of both the uni- and bipolar photodiode modules, and the synthesized unipolar waveforms from the optically driven JAWS system are presented in ”Results”. Finally, the prospected future work are presented in ”Further work”.

3.1 Historical background

This section is a short introduction into superconductivity leading up to the phenomena known as the Josephson effect.

3.1.1 Superconductivity

In 1908, Heike Kamerlingh Onnes successfully liquefied helium [42], which made it possible to cool down objects to only a few degrees Kelvin. Already in 1911, by investigating the low-temperature electrical behavior of the materials mercury, lead and tin, Onnes discovered that the resistance vanished at a critical temperature, T_C, which is specific for certain materials. These materials are just some of those that became known as superconductors, of which perfect conductivity is the first and perhaps the more important characteristic. This feature makes it ideal for use in transmission lines for applications of high current or low loss requirements, but also for high-field electromagnets, because no resistance equals no thermal heat development and low electrical attenuation.

The second characteristic of a superconductor is perfect diamagnetism, which means that it fully counteracts any externally applied magnetic fields by inducing a counteracting field. This characteristic was discovered by Walther Meißner and Robert Ochsenfeld in 1933 [43] and became known as the Meißner effect. This discovery lead to the London theory of superconductivity [44] two years later, which described the electromagnetic attributes of superconductors. Related to the superconductive current density $\vec{J}_s$, the equations for the microscopic scale electrical field, $\vec{E}$, and flux density $\vec{B}$ become

$$\vec{E} = \frac{\partial}{\partial t}(\Lambda \vec{J}_s) \tag{3.1}$$

and

$$\vec{B} = -c\nabla \times (\Lambda \vec{J}_s), \tag{3.2}$$

where

$$\Lambda = \frac{4\pi\lambda^2}{c^2} \tag{3.3}$$

and λ is the London penetration depth of the fields, and c is the speed of light in vacuum. For a material-specific critical temperature, T_c, and temperature $T < T_c$, λ can be written

as:

$$\lambda(T) \approx \frac{\lambda(0)}{\sqrt{(1-(T/T_c)^4)}} \tag{3.4}$$

Further explanations of superconductivity was made macroscopically by the GL theory (named after V. L. Ginzburg and L. D. Landau) [45] and microscopically by the BCS theory (named after J Bardeen, L. N. Cooper and J. R. Schrieffer) [46]. Both theories describe the realization of the superconductive phenomena as a preferable state in terms of lower free energy for the superconductive state for temperatures below T_C. The BCS theory describes this more accurately as pairs of electrons condensing in joint superconducting eigenstates, known as Cooper pairs, by releasing a material-specific condensation energy. Both theories are able to describe electrons traveling through a system of inhomogeneous condensation energy. The BCS theory led Brian D. Josephson in 1962 to predict the phenomena later known as the Josephson effect [1], for which he, together with Leo Esaki and Ivar Giaever, won the Nobel Prize in Physics in 1973 [47]. The Josephson effect has since 1990 been the BIPM accepted phenomenon to physically define DC voltage [2].

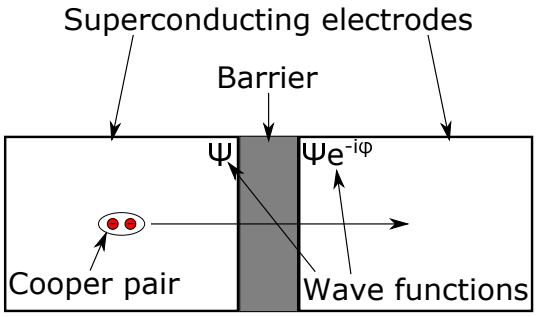

Figure 3.1: A principle schematic of a Josephson junction with a tunneling Cooper pair.

3.2 The Josephson effect and metrology

Today, the research related to the Josephson effect goes on to push the limits of realizable AC voltages with respect to amplitude, frequency and spectral purity. This section will establish the physical and mathematical descriptions of the applications of the Josephson effect in metrology, as well as explaining the different challenges that arise from using different realization methods.

3.2.1 The Josephson effect

In 1962 Brian Josephson [1] predicted out of the BCS theory that a superconducting current should be able to flow between two superconducting electrodes, through a thin barrier (a so-called Josephson junction, depicted in Fig. 3.1), without a voltage drop:

$$I_s = I_c \sin \Delta\phi, \tag{3.5}$$

where I_s is the superconducting current, I_c is the critical current, and $\Delta\phi$ is the phase difference in the Ginzburg-Landau macroscopic wave function between the two sides of the Josephson junction. Further, he also predicted that when a voltage difference is maintained across the junction, then $\Delta\phi$ would evolve according to

$$\frac{d(\Delta\phi)}{dt} = 2\pi \frac{2e}{h} V, \tag{3.6}$$

where t is the time, e is the elementary charge, and h is Planck's constant. A consequence of this equation, is that an oscillating superconducting current is realized of amplitude I_c and frequency $f = 2eV/h$.

Originally met with skepticism in the scientific community, the phenomena was proven experimentally already in 1963 by Shapiro [48]. He showed that not only can a voltage be realized which is proportional to the oscillating frequency of the superconducting current, he also proved that by further increasing the current, additional quantized voltage steps could be reached according to

$$V = n\Phi_0 f, \tag{3.7}$$

where n is the quantized Shapiro step, $\Phi_0 = h/2e$ is the fundamental flux quantum of a Cooper pair and f is the frequency of the oscillating supercurrent, typically in the gigahertz region. An important implication of equation (3.7) is that the realized voltage becomes a product of fundamental constants, quantization number and frequency.

If it is intended to utilize the Josephson effect to realize larger voltages, chips can be manufactured with many Josephson junctions in series, constituting a Josephson junction array (JJA). Given that, the manufacturing of Josephson junctions can be controlled reliably [20], the resulting tunneling of magnetic flux quanta is the same for all junctions, hence the resulting voltage can be expressed as

$$V = Mn\Phi_0 f \tag{3.8}$$

where M is the number of junctions in series in the array, and the rest of the parameters are as in equation 3.7.

Depending upon the stability of the frequency and how well it can be known, the voltage at each Shapiro step may be accurately calculated, and thus they can serve as well-known voltage references. Highly stable oscillators generally are used in the realization of the Josephson effect, the stability of which can be verified by time realization using various atomic clock with accuracy better than 10^{-16}. A vast array of experiments using JJAs, have been performed realizing voltages as high as 10 V with an uncertainty of 3.9 parts in 10^{11} [49].

In other words, the Josephson effect is an ideal candidate for being the metrological standard of voltage realization. Indeed, this is what happened in 1990, when BIPM finally replaced the previous DC voltage standard based on 1.018 V Weston cells with DC voltage realization using via the Josephson effect [2], by using a conventional value for

Planck's constant, h. Consequently, the electrical units have only been linked to the SI units through an uncertainty. This will however change in 2019, when the value of h will be fixed in SI units, after the revision of the SI [50].

An array of international research projects have been and are being carried out to develop equivalent methods for realization for AC voltage from the Josephson effect. These methods are mainly based on two different schemes, namely programmable binary JJA method [41] and pulse-driven JJA method [17], the latter of which is the main topic for this study. Both approaches will be explained further in the following subsections.

3.2.2 Types of Josephson junctions, SNS, SIS and SINIS

As explained in subsection 3.2.1, a Josephson junction consists of two superconducting electrodes separated by a thin barrier, and there are a few ways to constitute these barriers. The original JJAs were constructed using an insulating material as the barrier, forming a so-called SIS (superconductor-insulator-superconductor) junction. It was later discovered that Josephson junctions also could be formed using barriers containing normal conductors, namely SNS (superconductor-normal conductor-superconductor) and SINIS (superconductor-insulator-normal conductor-insulator-superconductor) junctions. The practical implications that follows from the choice of barrier type will be elaborated further upon in the next subsection. It is worth mentioning, that for synthesizing of AC voltage waveforms, both SNS and SINIS junctions have been used, but in recent years, $Nb/Nb_xSi_{1-x}/Nb$ based SNS junctions have lately been the dominant choice in metrology [20][21].

3.2.3 The Stewart-McCumber model

Already in 1968, Stewart [51] and McCumber [52] made their descriptions on the AC behavior of a real Josephson junctions as an ideal Josephson junction with critical current I_c shunted by a resistance R and a capacitance C (see Fig. 3.2). This description can be formed into the equation

$$\beta \frac{d^2\phi}{d\tau^2} + \frac{d\phi}{d\tau} + sin\phi = i\left(\frac{\tau}{2\pi f_c}\right), \tag{3.9}$$

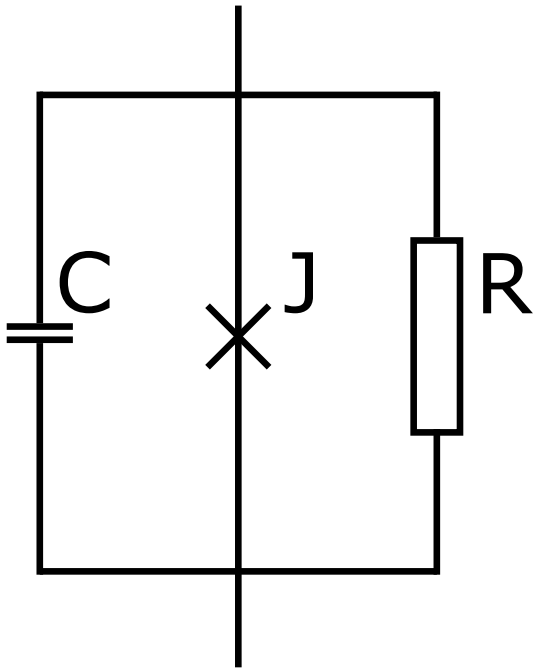

Figure 3.2: Equivalent circuit of a real Josephson junction, where C, J, and R refer to capacitive element, ideal Josephson junction, and resistive element, respectively.

where

$$i(t) = \frac{I(t)}{I_c}, f_c = \frac{2e}{h} I_c R, \beta = 2\pi f_c RC, \tau = 2\pi f_c t, \tag{3.10}$$

and ϕ is the phase difference in the macroscopic wave-function between the two electrodes in the junction, t is the time, and $I(t)$ is the current that is applied to the junction. Planck's constant and the elementary charge are h and e, respectively. This model has become known as the Stewart-McCumber model or the RCSJ (resistive and capacitive shunted junction)-model, and describes how the applied current is distributed over the realistic junction elements (the R, C and J), and how it relates to the evolution of ϕ. This current could in theory take any form, however, as will be explained more extensively in later subsections, either an RF current (with or without a DC current bias) or a train of current pulses according to certain patterns are mainly used.

When it comes to the choice of Josephson junction type, it is important to note that the value of the parameter $\beta \propto R^2C$ has a great impact on the behavior of the junction. For $\beta < 1$ the junction is a so called overdamped system, which is the case for SNS and SINIS junctions, as C tends towards zero. These junctions exhibit the more expected

characteristic of clear nonoverlapping Shapiro steps. In these cases, equation (3.9) can be simplified to

$$\frac{d\phi}{d\tau} + sin\phi = i\left(\frac{\tau}{2\pi f_c}\right). \tag{3.11}$$

For $\beta >> 1$ however, the junctions are underdamped, which is the case for SIS junctions. These junctions have overlapping Shapiro steps; however, this is not a big issue for DC voltage realization, since there is no on/off switching of the junctions during this process. For realization of AC voltage, the Shapiro step number must be absolutely known; hence, nonoverlapping steps is a requirement to realize calculable voltages. As explained above, this is the case for SNS and SINIS JJAs, and therefore, only these are acceptable in AC voltage metrology.

3.2.4 DC Josephson

When operating JJAs for DC voltage realization, the voltage can be simply realized according to equation (3.7). That is, a highly stable RF current needs to be applied to the array yielding a stable frequency, f. The value of f must be closely monitored, and traced to realization of time using atomic clocks, and in turn, the exact value of the realized DC voltage level can be calculated. Furthermore, a DC current bias might be applied to the RF current in order to select and maintain a stable Shapiro step, n.

Obviously, it is best to be able to realize the highest possible voltage. For DC voltage realization, this means to use the highest values of array-length, RF frequency and Shapiro step. By using SIS junctions, R and C are obviously large, and therefore, $\beta >> 1$ and f_c is also quite large. Such underdamped junctions have overlapping Shapiro steps, which makes higher steps available, and a higher value of f_c, allows for an increased operating frequency of the JJA [53][54].

The RF source for these JJAs has generally been either a Gunn diode in older setups or a microwave synthesizer in more recent setups. These sources are operated at room temperature, and aimed to send the RF electromagnetic signal down to a finline taper antenna on the JJA-chip. This antenna recreates the RF current signal and applies it to the JJA. The RF source is typically adjusted to bias the JJAs with microwave currents of about 20 GHz or 70 GHz, depending upon both characteristic parameters of the JJA, and the

desired ratio between the characteristic and microwave frequencies. This approach was used to exceed 1 V in 1984 by Niemeyer et al. [55], and later, in 1987 and 1990, 10 V was reached by Lloyd et al. [40] at National Institute of Standards and Technology (NIST) and Pöpel et al. [56] at Physikalisch-Technische Bundesanstalt (PTB), respectively. However, because programmable binary JJAs are easier to operate, and produce better uncertainties [57][58][59], these have become preferable in DC voltage realization. These are also more robust and reliable in long-term automated measurements with reversals [60]. On the other hand, leakage resistance to ground (LRG) is larger for binary JJAs than for conventional JJAs [61]. This is because the former is overdamped, and thus require a DC bias to realize Shapiro steps, whereas the latter is underdamped, and can be manufactured to be operated without DC bias. The LRG will therefore lead to a systematic error.

3.2.5 Programmable binary JJAs

Hamilton et al. [41] initiated the first approach to generate quantum-based AC voltage waveforms, by using the method that is now known as programmable binary JJAs. This method still uses equation 3.8, but where the number of active junctions, M, is time dependent. Thus, the equation is in this case written as

$$V = M(t)n\Phi_0 f. \tag{3.12}$$

The value of M is varied by dividing the JJA into segments of different lengths, which are activated and deactivated in a certain order, by switching their DC current bias on and off, respectively. This bias switching is performed by a multi-channel programmable source [62] with both positive and negative operation, such that both positive and negative voltages can be generated. The source is pre-programmed to apply currents from the channels in the previously mentioned order, so that a stepwise sine wave is approximated. Therefore, these setups are also known as programmable Josephson voltage standards (PJVSs).

It is however important to use overdamped arrays for AC voltage realization in order to make sure that always the same Shapiro step is used throughout the operation. This means that $\beta \propto R^2C \approx 0$ is required, which means that normal SIS junctions are out of the question since both R and C of the insulator-barrier are both quite large. Externally

shunted SIS junctions were tested by Hamilton et al. [41] to obtain overdamping, but this approach was discarded due to poor microwave behavior caused by large parasitic inductance.

As was done for single-segmented SIS JJAs for DC voltage realization, a Gunn diode or a microwave synthesizer [63] is used to generate the microwave current in the finline taper on the JJA-chip. The microwave current is then distributed to the different segments via a microwave distribution network. The first 1 V PJVS was demonstrated at NIST in 1997, by Benz et al. [64], using SNS JJAs, whereas SINIS JJAs were used at PTB to produce 1 V in 1999, by Behr et al. [65], and 10 V in 2000, by Schulze et al. [37]. The PJVS approach has since been improved, by increasing the number of segments and their resolution, which makes it possible to fine-tune the generated voltage (see example Müller et al. [66]), and by reaching voltages as high as 20 V by Yamamori et al. [67]. Further information regarding the instrumentation involved in PJVS can be found in the ”Good Practice Guide on the operation of AC quantum voltage standards” [68].

3.2.6 Pulse-driven JJAs

Going from DC voltage realization via the Josephson effect to generating stepwise approximations of sine waves is in principle a straight forward task. Using this approach, waveform points of quantum-accurate voltage can be produced with peak values similar to that which can be reached in DC voltage realization, i.e. 10 V. However, for frequencies beyond a few kilohertz, transients caused by the on/off switching of array segments dominate the synthesized waveform, and the quantization is lost. Therefore, research had to be done in order to discover an approach whereby an actually quantum-accurate waveform could be realized.

The alternative to microwave-based PJVSs is to operate the JJAs using fast current pulses to synthesize smooth voltage waveforms. This method still obeys equation 3.8, however, the junction number M is kept constant, and the frequency f becomes time dependent. A pulse code with varying pulse density is applied, hence; the equation becomes

$$V = Mn\Phi_0 f_p(t), \tag{3.13}$$

where $f_p(t)$ is the time dependent pulsation frequency. This operation of JJAs was first

proposed in 1990 by Monaco [16] and later demonstrated by Benz and Hamilton [17]. Driving the arrays using current pulses improves the quality of the realized waveforms by producing an actually quantized waveform that is spectrally pure. Also, where microwaved operation require specific frequencies and bias to realize first Shapiro step, pulse driving can be used to make quantization for a wide variety of pulse width, pulsation rate, pulse height and both positive and negative biases, and even no bias [28].

Setups based on pulse-driven JJAs can be used to realize a variety of waveform, and hence; these setups have become known as Josephson arbitrary waveform synthesizers (JAWSs). The JJAs are typically operated directly or indirectly (see later in subsections 3.3.2 and 3.3.4) by a PPG, which provides a programmed electrical pulse code, calculated by a sigma-delta encoding algorithm, to generate a certain waveform [69][70]. The direct pulsation works by coupling the ternary PPG (capable of delivering both pulse polarities), directly or through an amplifier, via a DC block, and into the JJA to generate the waveform. This has been the main approach for operation of JJAs, whereby waveforms up to 1-3 V have been realized for a few kilohertz [22][23][24][25][26][27][71]. These setups work by using PPGs with up to 8 channels to operate several arrays in parallel, and coupling the output terminals of the arrays in series. On-chip Wilkinson dividers have also been used to realize the Josephson effect in multiple parallel arrays in order to increase the total output voltage.

JJAs can also be operated indirectly by using photodiodes to drive it. The sigma-delta-code is still provided by a PPG, but it has to be converted into an equivalent optical signal, and used to irradiate photodiodes to reproduce the electrical driving signals. This can be done directly using an electroabsorption modulated laser, or indirectly using an intensity modulator to convert either a continuous-wave laser or a mode-locked laser into the desired optical pulse code.

3.3 Josephson arbitrary waveform synthesizers

As stated in subsections 3.2.5 and 3.2.6, quantum-based AC voltage waveforms are mainly synthesized by either the programmable binary or the pulse-driven approach. In the first method, the JJA is divided into segments of varying lengths, which are alternately activated by the programmable DC biasing source to stepwise approximate a sine wave [64]. In the second method, which is the topic for this thesis, the JJAs are driven with fast current pulses of varying repetition frequency [17][72][73]. This section presents a closer description of the schemes used to synthesize actual AC voltage waveforms from pulse-driven JJAs.

3.3.1 Output filtering of pulse-driven JJAs

Pulse-driven JJAs are typically equipped with a built-in low-pass filter [74], [75], where the cut-off frequency is set to be logarithmically somewhere in the middle between the pulsation clock frequency and the span of realizable waveform frequencies. This removes the supra-high frequency (higher harmonics of the pulsation clock frequency) voltage components that arise in the junctions during the span of a pulse. The result is a smooth curve corresponding to the target waveform.

3.3.2 Electrical pulses

The traditional way of operating a pulse-driven JJA, is to upload a fixed, calculated, 3-level sigma-delta code (see subsection 3.3.3) into a ternary PPG. The PPG generates the electrical sigma-delta pulse code, which is applied to the chip with one or more JJAs. The pulse-signal is AC-coupled, and often amplified, and led via coaxial cables down a cryoprobe to the JJAs in liquid helium. The output terminals of these JJAs are coupled in series, and the realized voltage waveform is extracted via thin leads to a high-speed, low-noise digitizer. A schematic representation of such a setup, which is the one that is used at PTB, is schematically presented in Fig. 3.3. This setup also forms the basis for the Josephson related measurements for this thesis, albeit with some modifications.

The exact system in Fig. 3.3 has previously been used realize waveforms beyond 1 V for frequencies up to 1.85 kHz at PTB [24][71]. In that experiment, 8 arrays were operated in parallel, and the output ports of the arrays were coupled in series. In this case, a PPG

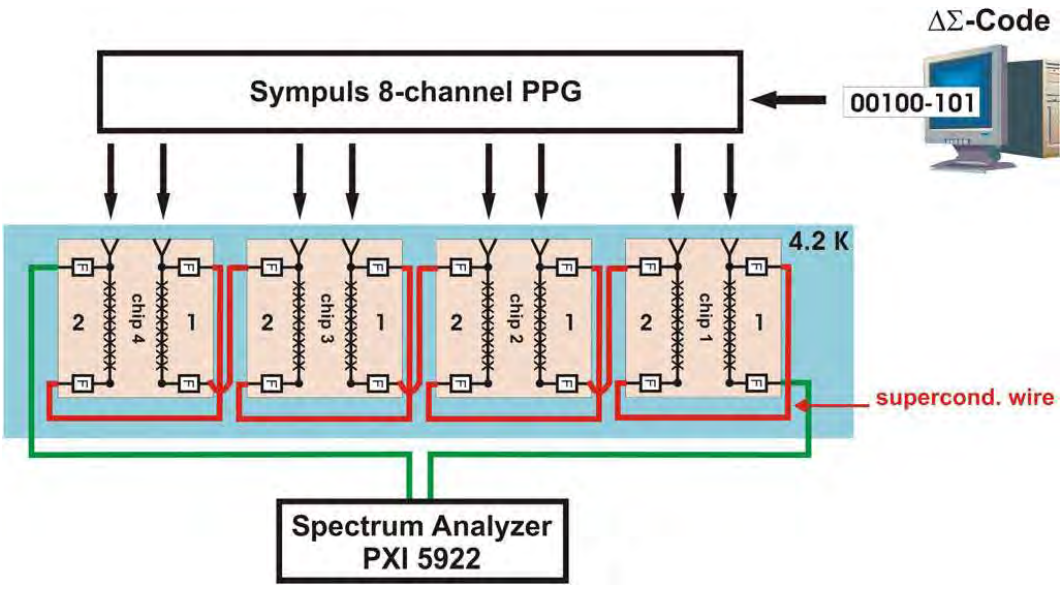

Figure 3.3: The basic JAWS setup used at PTB to synthesize 1 V in [24] from 8 JJAs, operated in parallel. Figure lifted from [24].

with 8 individual channels capable of delivering '-1', '0' and '+1' had to be used where great care had to be taken that all channels were satisfactory synchronized. Failing to do so, would cause the macro output waveform to consist of 8 micro waveforms with phases displaced from one another, hence a distorted macro waveform would occur.

Similar systems have also been constructed at NIST where 3-4 V has even been reached [27]. Their approach to enhance the realized voltage, has been to reduce the amount of PPG channels needed to drive multiple arrays, by introducing on-chip Wilkinson dividers in up to two stages [26]. Operational margins have been demonstrated in [25][26] for this approach to operate multiple JJAs, which makes this one promising option to realize stable quantum-based waveforms of ever higher voltage amplitude. NIST has also worked on replacing conventional pulses with zero-compensated "pulse-complexes", with 3-level pulse codes by Benz et al. [76], and the 5-level pulse codes by Zhou et al. [31]

3.3.3 JAWS setup at PTB

As suggested in subsection 3.2.6, and clearly expressed by equation (3.13), the voltage realized in a JJA, by pulsed operation, is proportional to the pulsation frequency, f_p, in the same manner as the microwave frequency, f, in the standard microwave operation

(equation (3.7)). However, for a JAWS setup, where an actual waveform is to be realized, the operation, and voltage magnitude become more complicated to calculate.

The most common signals to synthesize are sine waves. These signals have smooth slopes, and vary continuously. In order to synthesize these waveforms, the pulse repetition frequency needs to be varied in line with their theoretical evolution. Therefore, a pulse density modulation with sigma-delta encoding algorithm needs to be applied, which in theory can be used to synthesize any desired voltage waveform. The second-order sigma-delta modulator used to generate the pulsation code for this setup is described by Kieler et al. [70], which is schematically represented in Fig. 3.4.

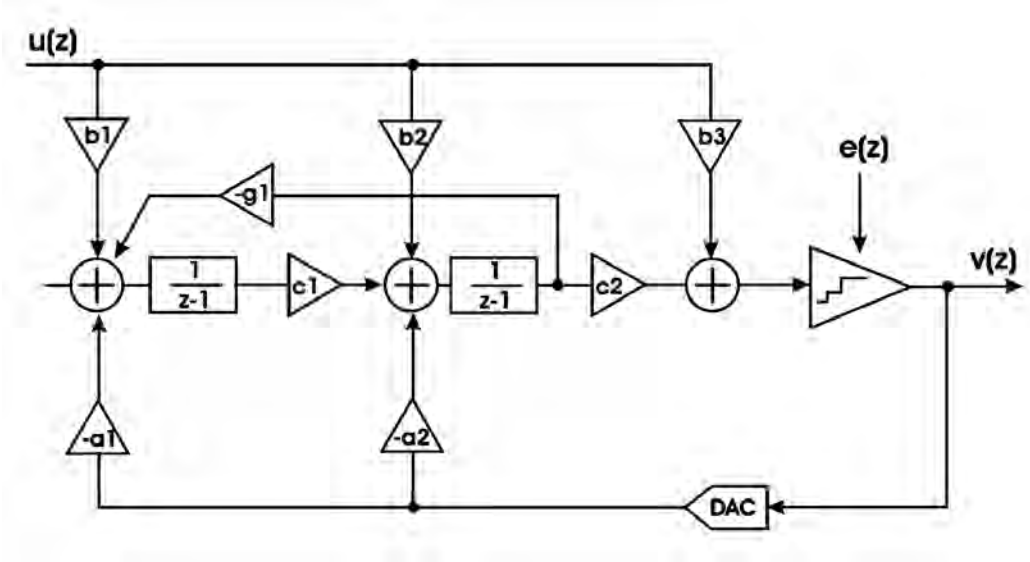

Figure 3.4: A schematic representation of the second-order sigma-delta modulator used at PTB, which is described in and lifted from [70].

The pulsation bit pattern is calculated with a waveform-bit-pattern length, $L_{\Sigma\Delta}$, which determines the synthesized signal frequency, f_s, according to

$$f_s = T_{\Sigma\Delta}\frac{f_{clk}}{L_{\Sigma\Delta}}, \tag{3.14}$$

where $T_{\Sigma\Delta}$ is the given integer number of periods in the output signal that the bit pattern shall produce, and f_{clk} is the given clock frequency of the PPG. Consequently, the PPG sets the minimum frequency for the signals that can be synthesized at where $T_{\Sigma\Delta}$=1, length of $L_{\Sigma\Delta}$ fully occupies the available memory in the PPG, and f_{clk} is set to the absolute minimum. In principle, the maximum f_s that can be synthesized, is the same as

f_{clk}, by setting $T_{\Sigma\Delta}/L_{\Sigma\Delta}$=1, however, the output waveform will become highly distorted. The smoothest waveforms are obtained when a long bit sequence is used to constitute one period in the synthesized waveform. Therefore, in order to increase the synthesized frequency, the largest available f_{clk} should be chosen. $T_{\Sigma\Delta}$ can be increased, but not with many orders of magnitude.

When using the sigma-delta modulation described in this section, as well as in [70], the formula for the voltage magnitude of the synthesized waveform must also include the so-called code amplitude, $A_{\Sigma\Delta}$. The code amplitude is the feedback parameter in the sigma-delta loop, and an input parameter to calculate the pulse code. It is a well-defined real number, and it has to be between 0 and 1, to maintain stable operation of the loop. It also constitutes the maximum pulse density in the code. Therefore, it limits the peak output voltage in the JAWS system to

$$V_s = A_{\Sigma\Delta} * n * M * \Phi_0 f_p, \tag{3.15}$$

where f_p is the maximum pulse repetition frequency, and the rest of the parameters are as defined in equations 3.7 and 3.8. The realized voltage waveform is sampled by the high-speed, low-noise digitizer.

3.3.4 Photoelectrical pulses

Direct pulsation of JJAs seem like a straightforward approach, but there are two reasons that makes it advantageous to use an indirect approach. The direct pulsation requires that the signal path between the PPG to the JJAs must include DC blocks, to avoid introduction of coupling noise into the JJAs. A DC block obviously removes the DC components, which are non-zero for regular pulses. The DC component in a pulse train also vary with pulse density. Therefore, when a complex pulse code is run through a DC block, a low-frequency compensation signal must be added to ”repair” the pulses. Further, when the Wilkinson dividers are used to operate multiple JJAs, in order to couple their outputs in series, the JJAs must be galvanically decoupled. This is done by using on-chip DC blocks for both the signal and the signal ground for each individual JJA. This is because the JJAs must remain floating, so that they can be coupled together.

Alternatively, one can apply zero-net-area ”pulse-complexes”, such as the ones used by

Zhou et al. [31], which already have zero DC components. However, the downside with the pulse-complexes used in Zhou et al. [31], is that it require a 5-level AWG (arbitrary waveform generator), which was not available for the experiments, and that the pulse-complexes need 4 bits per pulse, compared to only 2 bits for regular pulses.

Perhaps the strongest alternative to directly applied electrical pulses from the PPG onto the JJAs is to operate the arrays using photodiodes. This approach separates the JJAs electrically from the PPG, making the compensation signal obsolete. This reduces the complexity, and thus has the potential to improve the margins of the Shapiro steps. Since an isolated photodiode module can be used to operate an array, many arrays can have their output terminals coupled in series without DC blocks to galvaniclly isolate the JJAs. The splitting process of the optical signal can also be performed quite easily using commercially available fiber splitters. This has the same mission as the Wilkinson dividers had as described in the previous section, that is, to increase the number of JJAs that can be operated per PPG channel. An added benefit of the splitter is that fewer lasers, Mach-Zehnder modulators (MZMs) and RF amplifiers are necessary to purchase and operate in this system. Furthermore, because the optical splitters are not very frequency dependent and are readily available, they are quite advantageous compared to Wilkinson dividers. The optical splitters can be used in many stages, and at vastly varying clock frequencies, whereas Wilkinson dividers are tailored for a specific frequency range, and they must be carefully designed for a single chip.

A few experiments has already been performed using photodiodes to realize the Josephson effect, both at room temperature by Williams et al. [28], and at liquid helium by Wang et al. [30] and Urano et al. [29]. Wang et al. [30] demonstrated single-flux-quantum pulses from a Josephson junction driven by a metal-semiconductor-metal photodiode in liquid helium, whereas Urano et al. [29] realized unipolar 1 mV peak-to-peak voltage waveforms in a cryocooler at 4 K. Williams et al. [28] used a photodiode-module at room temperature to drive a JJA in liquid helium, and showed that the results agreed with theoretical simulations based on the Stewart-McCumber model.

3.4 Simulation model of JAWS

This section describes a numerical simulation model for pulse operation of the JJAs. The purpose of this model is to help determining the voltage realized in different JJAs based on the pulses produced in the photodiodes. For a JJA, with given parameters I_c and f_c (see equation 3.9 and 3.10), this model will be able to predict which pulse peak heights and widths are needed to realize Shapiro steps. This model will also be able to give an indication of how stable the Shapiro steps are for various JJAs and pulsations.

3.4.1 Previous simulations

Last few decades, quite a few simulation models have been made to investigate the behaviors of different realistic JJs. These models typically apply the Stewart-McCumber model of JJs, where the capacitance is assumed to be negligible, and hence the second derivative of the superconductive phase vanishes because β=0, and therefore, the model can be simplified into equation (3.11). As mentioned in subsection 3.2.3, this describes an overdamped JJ, hence only nonoverlapping Shapiro steps are present.

Simulations, as well as the very first demonstration of pulse driven JJAs was already described 1996 by Benz and Hamilton [17]. Their simulations were based on square pulses with cosine-shaped transients, and showed that Shapiro steps are present for repetition frequencies up to f_c with step widths more than 0.8I_c. The continuous wave simulations on the other hand only produces Shapiro steps for certain combinations of microwave frequency, amplitude and DC bias. Shapiro steps were demonstrated on a 512 junction array made out of Nb-PdAu-Nb (SNS) with I_c=1.9 mA and $f_c \approx$4.0 GHz.

Another simulation model of a theoretical JJ was made by Williams et al. [28] in 2004. The model was verified by measurements on a SINIS JJA, consisting of 100 JJs. The simulations were performed on an arbitrary JJA, with critical current I_c and characteristic frequency f_c. In order to mimic the behavior of photodiodes, Gaussian shaped current pulses were applied in the simulations. By plotting the simulated voltage plateaus as in Fig. 3.5, for W (which is the full-width-half-maximum (FWHM)) at $1/2\pi$, $2/2\pi$, $4/2\pi$, and $8/2\pi$ units of f_c^{-1}, and as a function of pulse area, relations were found between pulse area and realized Shapiro steps. The pulse area contribution, A_1, needed to traverse one Shapiro

step was found to be close to constant, and can approximated to

$$A_1 \approx \frac{I_c}{f_c} = \frac{h}{2eR}, \tag{3.16}$$

where h is Planck's constant, e is the elementary charge and R is the normal state resistance of the barrier in the junction. In other words, this equation suggests that the width of any Shapiro step is only dependent upon the parameters of the junctions themselves. Furthermore, the pulse area needed to traverse to the first Shapiro step is also dependent upon the actual pulse width:

$$A_2 \approx \left(W f_c + \frac{1}{2}\right) \frac{I_c}{f_c}. \tag{3.17}$$

The equations (3.16) and (3.17) were derived by plotting the realized Shapiro steps per pulse area for W=1, 2, 4, and 8 in units of $1/2\pi f_c$, as in Fig. 3.5 (lifted from [28]).

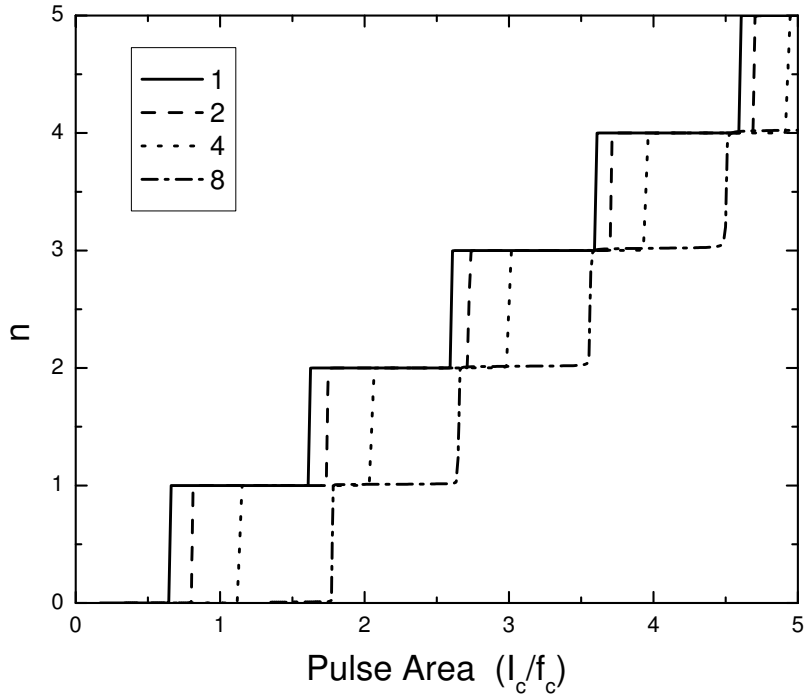

Figure 3.5: Simulation results (obtained from Williams et al. [28]), for W=1, 2, 4, and 8 in units of $1/2\pi f_c$.

The simulation model [28] was verified by using a 100 junction SINIS array operated by a photodiode at room temperature, and plotting corresponding simulations and measurements together in Fig. 3.6. The array was biased with $W = 5.1/2\pi f_c$ pulses of heights

up to 80 mV. The sloped transients between the steps in the measurements are due to a mismatch of Shapiro steps in these regions. In other words, the sloped transients between the quantized voltage steps result from the spread of realized Shapiro steps when the pulse area is close to limit between them.

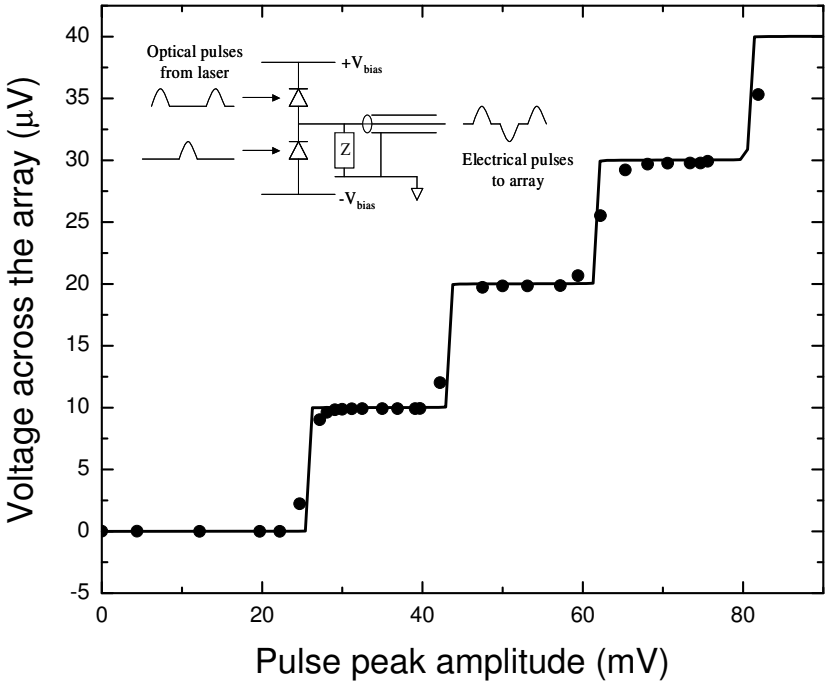

Figure 3.6: Simulation (solid line) and measurement (dotted points) results shown together (figure obtained from Williams et al. [28]), for W=5.1 units of $1/2\pi f_c$.

3.4.2 Evaluation tool for appropriate JJAs

In a JAWS system, the choice of JJA (in terms of I_c and f_c, see equation (3.10)) and pulsation regime (pulse peak height and width) must be such that the entire first Shapiro step can be covered. This is to ensure that the system can reliably produce quantum-accurate voltage signals with a margin. Consequently, if the maximum optical power is sufficiently large to reach the second Shapiro step, then this requirement has been met. The pulse area, A_p, can be approximately expressed as $A_p = I_p W$, where I_p is the current pulse peak height and W is the FWHM. The minimum pulse area needed to cover the entire first Shapiro level is calculated by adding equations 3.16 and 3.17 together as $A_p \geq A_1 + A_2$.

By rearranging this expression, we obtain the following minimum requirement for I_p/I_c

$$\frac{I_p}{I_c} \geq \frac{3}{2}\frac{f}{f_c} + 1, \tag{3.18}$$

where f is the inverse of W. Alternatively, an appropriate JJA can be selected from the known pulsation ability. By rearranging equation 3.18, the maximum value of I_c/I_p, where the entire first Shapiro step can be covered, becomes

$$\frac{I_c}{I_p} \leq \frac{2(f_c/f)}{3 + 2(f_c/f)}. \tag{3.19}$$

The equations 3.18 and 3.19 are shown graphically to the top and bottom in Fig. 3.7, respectively. The maximum available I_p must be above the red line for a given JJA and f in the top graph, and the selected JJA must have I_c and f_c below the red line for a given pulsation mode.

3.4.3 Simulation scheme

The simulation model used in (**Article 2**) to describe the behavior of a pulse-driven JJA was written in Python (see Appendix A), and was based on the Stewart-McCumber model (see subsection 3.2.3) [51], [52] of a single JJ. This simulation model assumes a strictly overdamped JJ, so the second derivative of the phase ϕ is removed, as $\beta \approx 0$ in this case. The equation (3.11) is therefore solved in discrete time of identical steps.

The model operates with reduced time, τ, as described in equation (3.10), which is discretized into N equal steps, $\Delta\tau$. The model calculates the corresponding current values of the pulse (will be discussed later in this section) applied to the JJ, and then evaluates the reduced time derivative of the phase according to the following discretization of equation (3.11):

$$\frac{d\phi^n}{d\tau} = i\left(\frac{\tau^n}{2\pi f_c}\right) - sin\phi^n, \tag{3.20}$$

where n corresponds to the current time step. From this, under the assumption that $\phi(0) = 0$, the model extrapolates the next phase value, ϕ^{n+1} according to:

$$\phi^{n+1} = \phi^n + \frac{d\phi^n}{d\tau}\Delta\tau \tag{3.21}$$

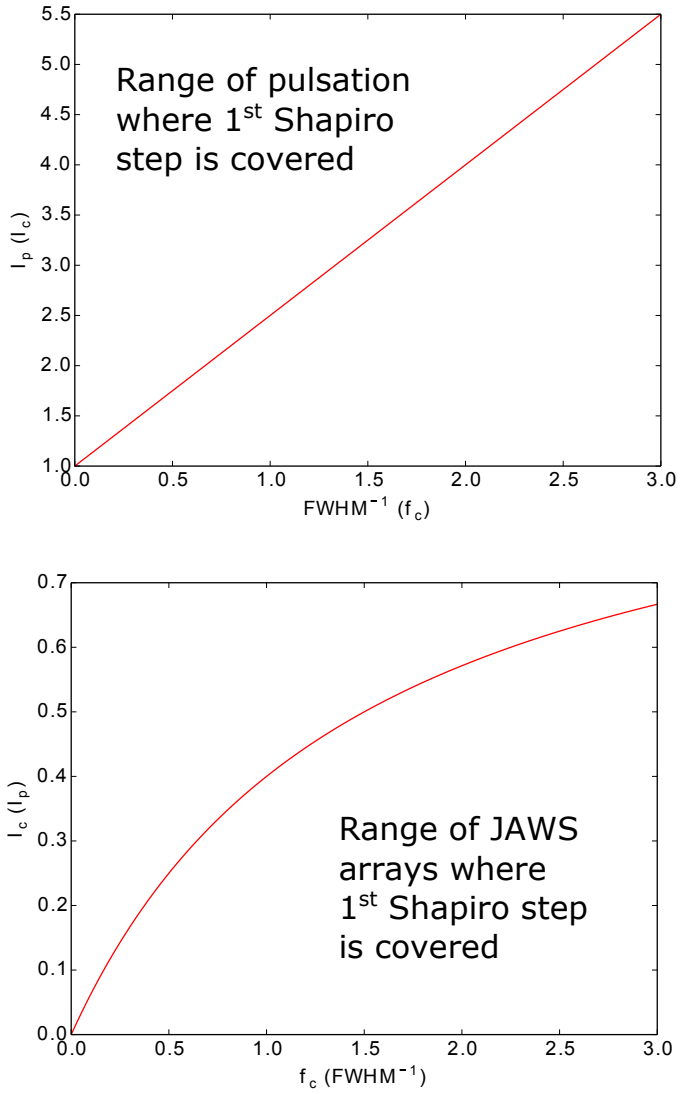

Figure 3.7: Graphical representation of equations 3.18 and 3.19. In the top graph is the minimum required I_p for a given JJA and f. The value of I_p/I_c must be above the red line. In the bottom graph is the maximum value of I_c that the pulsation source can satisfactory realize first Shapiro step for a given pulsation mode and f_c. The value of I_c/I_p must be below the red line.

The resulting Shapiro step realized for the given pulse is calculated as the total phase evolution of a single pulse divided by 2π:

$$Shapirostep = \frac{\phi^N}{2\pi} \tag{3.22}$$

The current pulse values can be calculated according to a hard-coded function. In principle, the pulse shape could take any form. The most common pulses to model for the simulation is either a Gaussian or a square pulse with cosine-shaped transients. The most realistic simulation results are obtained by using real pulse-waveform data, measured by a 50 Ω oscilloscope, which was done for a simple pulse train in (**Article 2**).

3.5 Photoelectrical pulses at 4 K

In this section, the issues surrounding the transduction of optical pulses into electrical ones in liquid helium are described.

The main issue is the development of a photodiode packaging technique to produce photodiode modules that can mechanically survive the extreme temperature shift, and at the same time maintain optical and electrical contact.

As the technology for 1550 nm lasers is more mature than for 1310 nm, InGaAs p-i-n photodiodes are mostly operated at this wavelength at room temperature. However, since the photodiodes are to be operated at 4 K, the bandgap in InGaAs is increased, hence; shorter wavelengths are needed in order to excite charge carriers.

In order to make a mechanically protected interface between the in- and outputs and the test-objects in liquid helium, a cryoprobe has been devised. The cryoprobe is described toward the end of this section.

3.5.1 Bandgap issues at 4 K

When operating photodiodes at temperatures far from room temperature, it has to be made sure that laser to be used can excite charge carriers. This means that the wavelength of the laser has to be chosen so that the photon energy is at least slightly larger than the bandgap energy of the base material of the photodiode.

In this experiment, the PDCS24L InGaAs photodiode from Albis is used. The data sheet [77] states that the operating wavelength ranges from 1260 nm to 1620 nm. However, these values assume that the temperature is above the minimum specified operating temperature of -40 C. Here it is intended to operate the photodiodes at 4 K, that is 230 K lower than what the data sheet guarantees. Therefore, bandgap calculations needs to be performed and compared to the photon energy of the laser in order to determine the usable wavelength. Here the bandgap model is provided by Paul et al. [79], where T is the temperature in kelvin and x is the gallium-to-arsenide-ratio as given in $In_{1-x}Ga_xAs$:

$$E_g(x,T) = 0.42 + 0.625x - \left(\frac{5.8x}{T+300} + \frac{4.19(1-x)}{T+271}\right) 10^{-4}T^2 + 0.475x^2[eV] \quad (3.23)$$

For the most commonly used gallium-to-arsenide-ration x=0.47, the resulting temperature dependence of this alloy becomes:

$$E_g(T) = 0.819 - \left(\frac{2.726}{T+300} + \frac{2.221}{T+271}\right) 10^{-4} T^2 [eV] \tag{3.24}$$

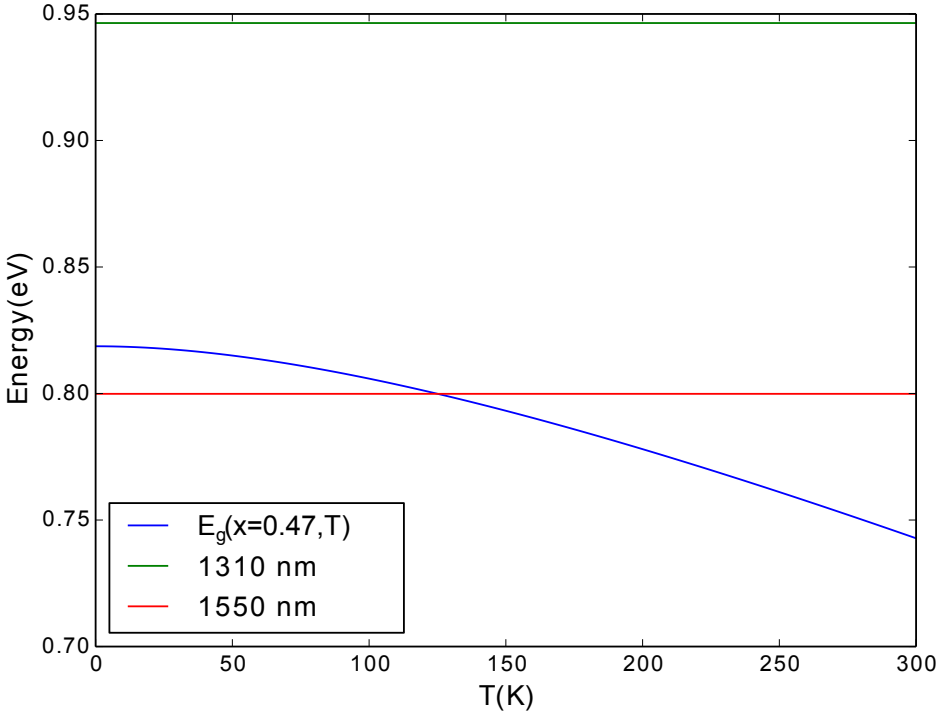

Figure 3.8: Energy vs Temperature of the standard In-to-As ratio, x=0.47 (blue), compared to the photon energy of 1310 nm (green) and 1550 nm (red) wavelengths. The intersection between the blue line and the two other lines represent the lower marginal temperature, where the lasers can excite charge carriers for the standard value of x.

In the IR-based telecoms industry, the two most commonly available laser wavelengths are 1550 nm and 1310 nm. The better developed technology exists for 1550 nm, however, for operation at 4 K, the photon energy is insufficient to excite the charge carriers. The bandgap calculation presented in Fig. 3.8, shows that the bandgap energy becomes larger than the 1550 nm photon energy already at 130 K. On the other hand, the 1310 nm photon energy is larger than the bandgap all the way down to 0 K, and is larger than the bandgap at 4 K by about 0.13 eV.

The Ga-In ratio currently is fixed to 0.47-0.53 in large-scale manufacturing due to it being

lattice matched to be grown on a InP surface. However, in the future, it can be envisioned that a method might be developed, where the value of x can be selected more or less freely. With this ability, it would be beneficial to select the mixture such that the bandgap is 0.01-0.02 eV smaller than the photon energy of either 1310 nm or 1550 nm for the target temperature, most of the optical energy is used to excite charge carriers, rather than heating the photodiodes. At 4 K, the formula in equation 3.23 for the bandgap energy, for a given x, becomes:

$$E_g(x) = 0.42 + 0.625x + 0.475x^2[eV] \tag{3.25}$$

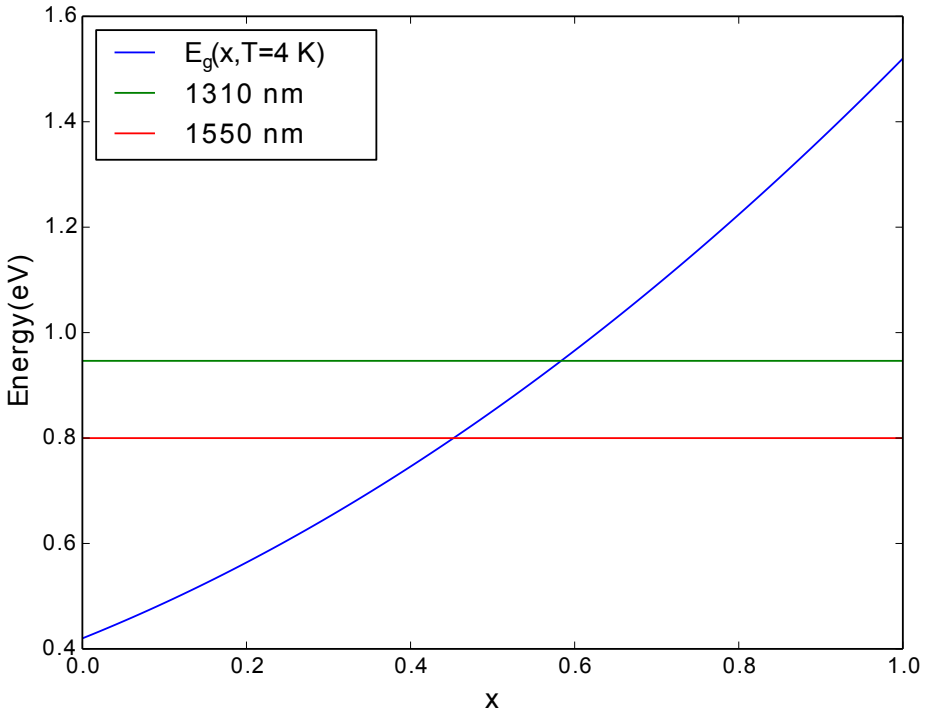

Figure 3.9: Bandgap energy vs In-to-As ratio, x at 4 K for InGaAs (blue), compared to the photon energy of 1310 nm (green) and 1550 nm (red) wavelengths. The intersection between the blue line and the two other lines represent the upper marginal values of x, where the lasers can excite charge carriers at 4 K.

This equation is graphically represented in Fig. 3.9 together with the photon energy of 1310 nm and 1550 nm photons. The band gap energy intersects with the optical energies where x equals 0.58 and 0.45 for the two wavelengths respectively. This means that

reducing the amount of gallium by only 2 % with respect to arsenide would have made 1550 nm technology available for 4 K operation.

3.5.2 Unipolar photodiode module

The unipolar photodiode module shown in Fig. 3.10 contains bare photodiode chips on a silicon based chip carrier, which again is glued onto a PCB made out of RO3006 (laminate material from Rogers Corp.) with SMA connectors. The photodiode chips are the PDCS24L form Albis (see close-up image and schematic of the coupling in Fig. 3.11 to the left and right, respectively), a lensed, bottom-illuminated, InGaAs diode, with a 28 GHz bandwidth. This diode has been flip-chip bonded onto the chip carrier, and bonded with AuSn solder paste. The diodes are under filed with Stycast 1266 glue in order to increase the mechanical strength of the flip-chip bonds. It is necessary to reinforce the bonds in such a way because of the mismatches in thermal expansion coefficients of the materials involved.

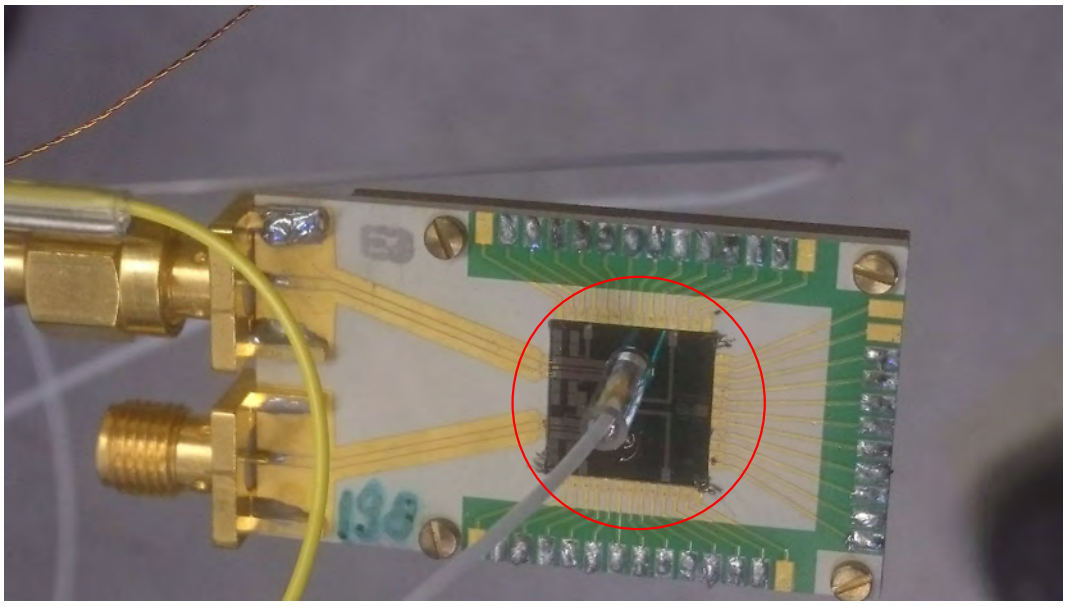

Figure 3.10: Picture of a finished cryogenically operable, unipolar, photodiode module. The photodiodes are flip-chip bonded onto the silicon-based chip-carrier (in the red circle), which in turn is glued to a PCB made out of RO3006b (versions made out of RO3450b have also been made) from Rogers Corp.

The chip-carrier, which is encircled in red in Fig. 3.10, is a silicon-based chip with 50 Ω

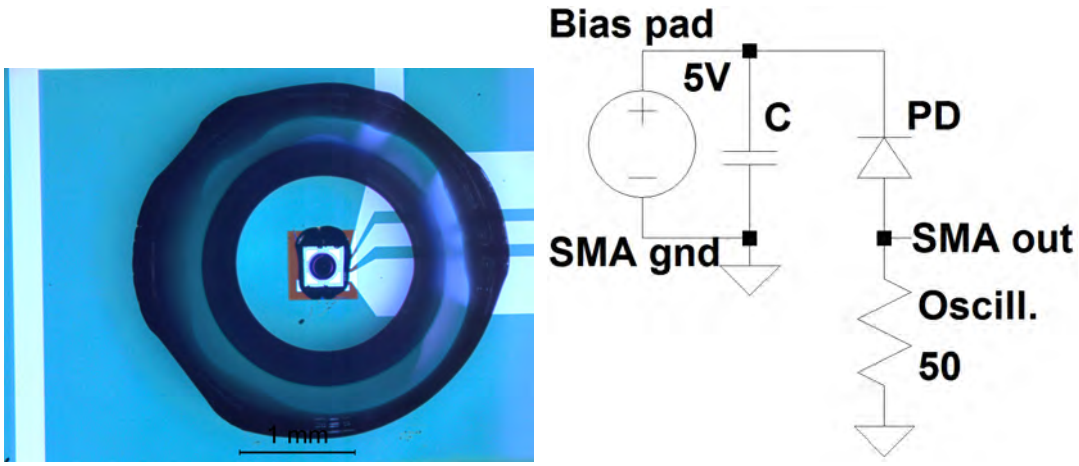

Figure 3.11: Left: Close up picture of the photodiode through the glass sleeve. The photodiode is the lensed bottom illuminated version of PD20X1 from Albis. Right: Schematic representation of the chip carrier with photodiode. The diode is loaded by a 50 Ω oscilloscope.

transmission lines made out of niobium. All of the bonding pads are plated with AuPd to ensure good Au-based bonding contacts. These chips were originally designed by a collaboration between JV, National Physical Laboratory (NPL) and PTB [80] for the purpose of pulse driving these exact photodiodes in liquid helium. These chip carriers are being produced at PTB. The reason for choosing niobium for the transmission lines is that it becomes superconductive in liquid helium. The limiting factor for the frequency response in such an assembly is the RC-term, and with the R reduced to almost zero in the chip carrier. Therefore, the available frequency range should only be limited by the photodiode.

The laser signal is led down to the photodiodes through 1.8 mm ferrule ended optical fibers. This ferrule is kept in place with a 1.818 mm borosilicate glass. These sleeves have been glued to the chip-carriers using Stycast 1266 glue, and the positions have been fine-tuned using a microscope.

3.5.3 Bipolar photodiode module

A complete JAWS setup needs to have both positive and negative pulses applied to the JJA. This is so that waveforms with both positive and negative voltages may be realized, by effectively realizing the quantum levels n=+1 and n=-1. Certain PPGs are so-called ternary PPG, which means that altogether three Boolean voltage levels can be applied to the JJA,

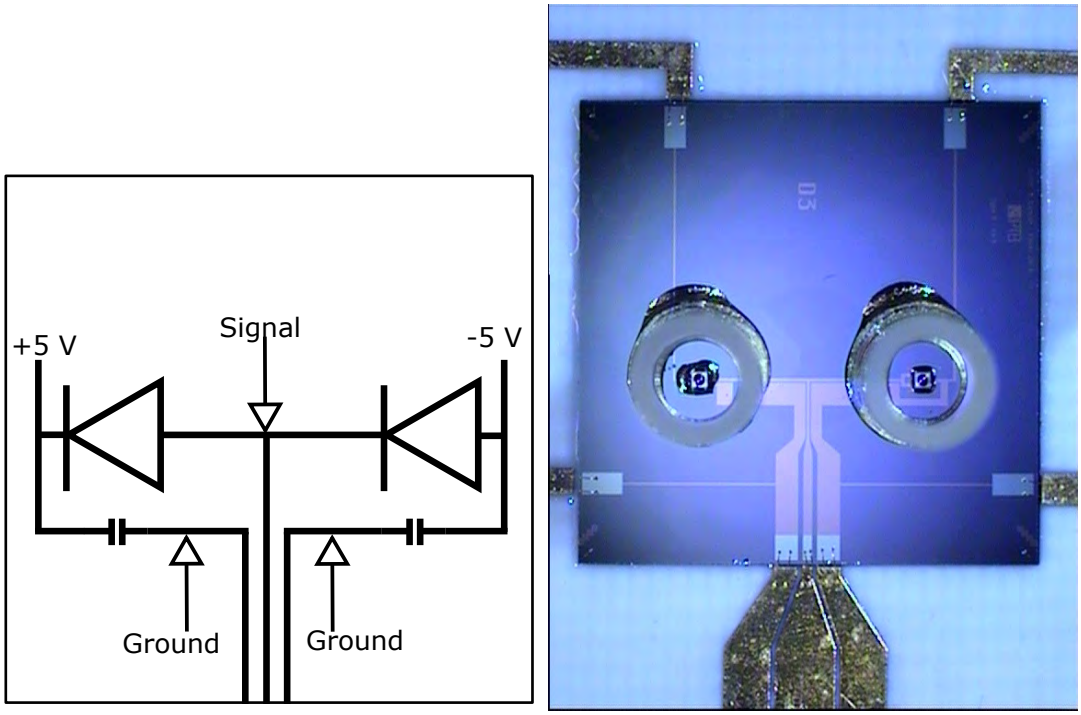

Figure 3.12: Left: A schematic representation of the chip-carrier with two photodiodes. This chip-carrier was glued and aluminum-wire bonded onto a sample holder made out of either RO3006b or RO4350b material from Rogers Corp. The photodiodes are illuminated via a ferrule-ended optical fiber, and the electrical signal is measured via a female SMA (SubMiniature version A) connector. Right: Photography of the bipolar chip-carrier, fully equipped with photodiodes and sleeves, and glued and wire bonded onto a sample holder made out of RO4350b laminate material from Rogers Corp.

namely '+1', '0' and '-1'. When photodiodes are driven optically, a reverse voltage bias is applied, which makes it unidirectional. Therefore, in order have a photodiode module that can produce bipolar opto-electrical pulses, two photodiodes must be coupled in opposite direction to the module's output. A bipolar chip-carrier was designed, which is schematically depicted in Fig. 3.12. In this design, two photodiodes were coupled in series, and the bipolar driving signal for the JJA was taken out between them.

The chip-carrier has its signal path laid out as a "T-junction", where the two photodiodes are placed on the end of the arms on the top, and the output signal goes out through the bottom. Here, we refer to the photodiodes as positively and negatively coupled. The positively coupled photodiode has its anode connected to the signal path, and its cathode coupled to a +5 V bias, thus producing a positive current pulse. The negatively coupled photodiode has its cathode connected to the signal path, and its anode coupled to a -5 V bias, thus producing a negative current pulse. The positively and negatively coupled photodiodes are placed on the left and right arm of the "T", respectively.

In (**Article 4, 5**), a manufacturing technique had been developed for making unipolar photodiode modules (see section 3.5.2). This same technique was used to assemble the new bipolar module, where only the number of photodiodes and optical connections were increased. The PCB sample holder was also changed into a centered single output design.

Because the current manufacturing technique makes use of an optical connection, where a ferrule with a 1.8 mm diameter is placed inside a glass sleeve with an even larger diameter, the distance between the two photodiodes was set to be 4.5 mm. In silicon, for a typical signal frequency of 10 GHz, this distance is roughly half a signal propagation wavelength, thus; a 50 Ω termination in the merger point of the signals from the two photodiodes might be necessary to avoid significant reflections. Therefore, two versions of the bipolar module was made, one without and with termination. The termination consisted of two parallel coupled 100 Ω on-chip resistors, in parallel, going from the merger point to each of the ground lines in the output CPW.

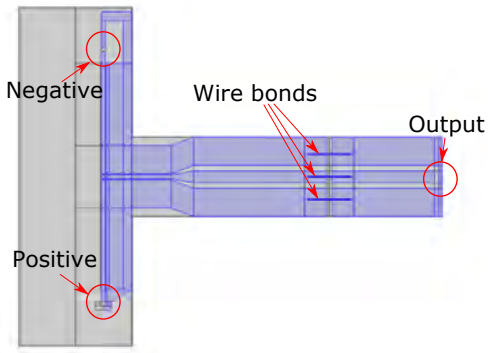

Figure 3.13: The COMSOL model of the current design, where the photodiodes are separated by 4.5 mm.

3.5.4 Simulation model of the bipolar chip-carrier in COMSOL Multiphysics

In order to verify and investigate flaws in the bipolar chip-carrier design, the simulation model shown in Fig. 3.13 was constructed in COMSOL Multiphysics. This model was laid out with dimensions resembling the real chip-carrier, where the photodiodes themselves were replaced with capacitors of the same value as their internal parasitic capacitance. The wire bonds from the chip-carrier to the PCB were also included, since these are highly inductive, and therefore have a great impact at RF frequencies. The RF module was used to perform simulations of the time-domain response from a Gaussian shaped pulse with a FWHM of 50 ps, with origin at the positively coupled photodiode.

An alternative chip-carrier design, shown in Fig. 3.14 was also simulated, where the two photodiodes are placed with their centers only 500 μm apart from each other. The positively and negatively coupled photodiodes have been rotated clockwise and counter-clockwise, respectively, where the two signal paths merge in a 120 degree angle. In this design, the merging distance is reduced to only about 1/20 of a wavelength, thus; a better signal transmittance can be expected, and perhaps remove the need for an on-chip termination. The same simulations were performed for this design, as for the current design. It should also be mentioned, that the reason for not manufacturing chip-carriers from this design, is that a new optical connection must be developed, which allows for such tight placement of the photodiodes.

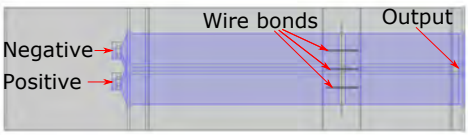

Figure 3.14: The COMSOL model of the proposed new design, where the photodiodes are separated by 500 μm.

3.5.5 Optical pulse generation

The pulse patterns to be applied to the photodiode first have to be generated electrically by a PPG. For realization of AC voltage waveform, more complicated pulse patterns like a delta-sigma code must be applied. This code must be externally applied, either by a hard coded pattern [70], or as a part of a feed-back loop [81]. For the case of the photodiode testing however, the pulse pattern can be set manually on the PPG's display. This is because the only characterizations that are searched for is the available pulse output of the photodiodes as well as their ability to replicate pulse patterns.

Quite a few methods can be used to convert the electrical signal into optical pulses. One of the simpler ways to accomplish this is to use a directly modulated electron-absorption laser. Such a laser was used to perform the initial tests where a vector network analyzer (VNA) was used as signal source for a small-signal AC analysis. In order to increase the amplitude of the optical signal, the directly modulated laser was replaced by continuous-wave (CW) laser, which is modulated by a Mach-Zehnder modulator into an optical pulse pattern. Whereas typical directly modulated lasers at 1310 nm generally have a maximum optical output of about 20 mW, and much lower maximum pulse peak height, the modulator chosen for this setup has a maximum input of 80 mW, with an output pulse peak height of about 30 mW. The resulting optical pulse pattern will thus be analogous to the electrical pulse pattern produced by the PPG. With this setup, the peak of the electrical pulses from the photodiode could be increased.

Mach-Zehnder modulators like the one used in this experiment need a quite high RF power in order to modulate the laser. The requirement also increases with frequency,

starting from about 4 V peak-to-peak at low frequencies and up to 7 V peak-to-peak at 20 Gbit/s. Most PPGs tend to be limited to signal amplitudes in the range 0.25-2.00 V peak-to-peak, which means that the signal has to be amplified using a modulator driver for the Mach-Zehnder to make large laser pulse peaks.

Operating multiple photodiodes using only one PPG channel and MZM with modulator driver (MD), is easily achieved using an optical fiber splitter. In (**Article 3**), a 1:4 optical splitter was used to split the laser signal to operate two photodiodes in a bipolar module. Here, a 2 m fiber extension was used to make a small time delay was applied to the negatively coupled photodiode to demonstrate bipolar pulsation.

In the future, when the splitter is used to optically operate four pulse-driven JJAs, it must be made sure that the pulses from the photodiode onto the JJAs are sufficiently synchronized. It is a great concern that the pulses from the four photodiodes are de-synchronized due to the production variance of the fiber lengths. For an effective light-speed of half that in vacuum, the time offset between two photodiodes becomes roughly 5 ps/mm fiber length disparity. Possible de-synchronizations caused by disparity of fiber lengths can potentially be tuned away using tunable optical delay elements.

3.5.6 Setup for cryogenic measurements

The sample is immersed into a dewar containing liquid helium using the cryoprobe depicted in Fig. 3.15. The sample is attached to the cryoprobe via the semi-rigid coaxial cable running through it, which also is used to extract the output signal from the sample. A metallic shield is screwed onto the bottom of the cryoprobe to protect the sample for hitting anything.

The laser pulse signal enters the cryoprobe via an FC-to-FC mating sleeve running through the wall of its head. The signal is led down to the sample via a single mode fiber with a standard FC/PC connector in one end, and a ferrule in the other end. As mentioned in section 3.5.2, the ferrule is flat ended with a diameter of 1.8 mm, and it fits perfectly inside the borosilicate glass sleeve with a margin of only 18 μm. The FC/PC connector is screwed to the mating sleeve end on the inside of the probe head, and the ferrule end is led down through the tube and into the glass sleeve surrounding the photodiode.

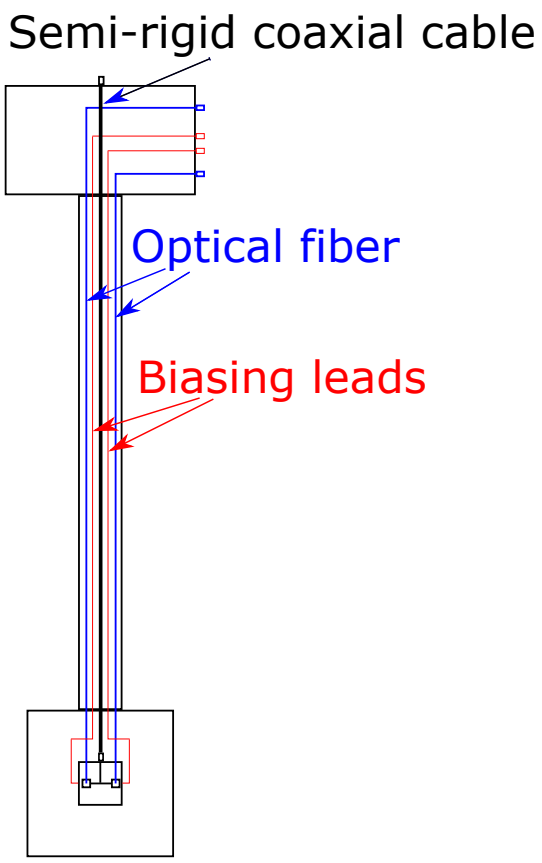

Figure 3.15: Schematic depiction of the cryoprobe used for these experiments. The thick black coaxial cable has female K-connectors, the blue optical fibers have FC/PC-connectors, and the thin red biasing leads for the photodiodes have an erni connector

Reverse bias is applied to the photodiode via two thin copper leads that are led down through the cryoprobe tube. These leads are soldered to a connector through the probe head in one end, and soldered to the signal ground and the anode of the photodiode in the other end. A positive voltage of 5 V is then applied to the anode with respect to signal ground.

The signal from the photodiode is then extracted through the coaxial cable to a 50 GHz oscilloscope, which will be described later in section 3.6.2.

3.6 Experimental setups

This section describes the experimental setups that are used for the experimental work for this thesis. Because the high-speed behavior of the photodiodes alone and together with JJAs are of interest in this thesis, only these setups are described in this section. The main focus have been put upon the optical pulsation setups, because these are used to demonstrate the ability of the photodiodes to generate electrical pulses in liquid helium, which are capable of driving a JJA.

3.6.1 Small-signal AC analysis

Because the photodiode is not specified for 4 K, it had to be verified that it could handle high-speed operation at this temperature. Therefore, AC analyzes were performed on the photodiode in (**Article 6**). It should be mentioned that the photodiode samples used in this experiment were not the unipolar photodiode modules described in section 3.5.2, rather, the photodiodes were manufactured with small ceramic submounts, which in turn were glued and wire bonded onto RO4350b-based PCBs.

The test setup is schematically depicted in Fig. 3.16. The basis for the AC analysis was the Rode & Schwartz ZVL vector network analyzer (VNA), with a maximum 0 dBm RF power output, and a frequency range from 100 kHz to 14 GHz. The output electrical signal from the VNA was converted into a 1310 nm laser signal using the Eudyna FLD3F10NP-A DFB laser, which had an integrated electro-absorption modulator. The laser signal was then led to the photodiode via optical fibers. The output electrical signal from the photodiode was led back to the VNA's input via a coaxial cable, which was attached to the SMP-connector on the photodiode sample.

3.6.2 Unipolar pulsation

In order to operate a pulse-driven Josephson setup, large pulses must be applied on the JJA in order to transfer flux quanta. The large-pulse characterization of the photodiode module is the topic in (**Article 2**), and the subsequent use of this photodiode module to generate a unipolar waveform by using a JJA with 3000 JJs is the topic of (**Article 7**).

The setup used to perform the large-pulse characterization is schematically depicted in

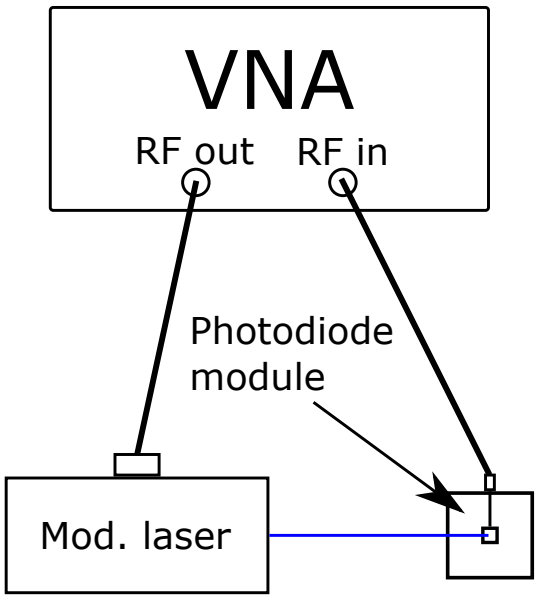

Figure 3.16: The setup used to perform small-signal AC characterization of various prototypes of the unipolar photodiode module. The prototypes have been put at various temperature in the range 4-300 K.

Fig. 3.17. As mentioned in subsection 3.3.2, pulse-driven JJAs are typically operated by a PPG according to a calculated bit pattern. This is also the case for this setup, where the Sympuls Aachen BPG 30G - TERx8 PPG was used to produce the electrical bit pattern, which is to be converted into optical pulses. In order to increase the peak height, a MZM (iXblue MX1300-LN-20) was used convert a high-powered CW laser into the optical pulse pattern. The RF input of the MZM needed a peak-to-peak voltage of 6-7 V, so a modulator driver (iXblue DR-DG20-MO) was used to amplify the signal from the PPG.

Unfortunately, we had to use a Fabry-Perot (FP) laser to drive the MZM, since we were unable to find a 1310 nm distributed feedback (DFB) laser that could produce more than 20 mW optical power. The disadvantage of a FP laser is that it produces light with a much larger range of wavelengths compare with a DFB laser. Our laser, the Thorlabs FPL1053, had a typical wavelength spectrum of 1310 nm $\pm$10 nm, whereas a typical DFB laser would have a typical wavelength spectrum of 1310 nm $\pm$0.1 nm. A wide wavelength spectrum will cause problems with the laser extinction in the MZM.

The characterization of the output signal from the photodiode in liquid helium was per-

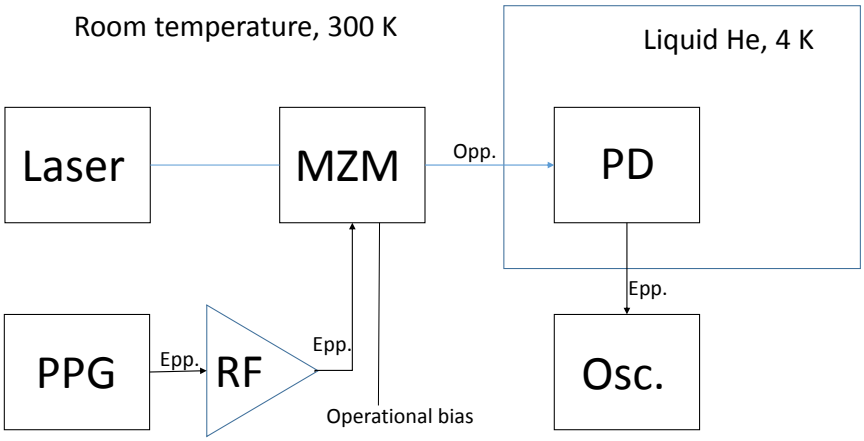

Figure 3.17: Schematic of the setup used to generate the optical pulses and measuring the response form the unipolar photodiode module.

formed using an oscilloscope consisting of a TDR/Sampling module (Tektronix 80E10) and a digital serial analyzer (Tektronix DSA8200). This oscilloscope had a 50 GHz bandwidth, which is well beyond both the typical 28 Gbit/s specification of the photodiode and the 25 GHz bandwidth of the MZM. A -8 dB attenuator was attached to the TDR/Sampling module in order to protect it from the reverse bias applied to the photodiode, in the event that the photodiode should short-circuit.

3.6.3 Unipolar optical operation of a JJA

The setup used to perform the unipolar optical operation of a JJA is schematically depicted in Fig. 3.18. The basis for this setup, is the JAWS setup at PTB, which has been described in subsection 3.3.3 as well as in [70] and [24]. This setup has been modified to include an optical PPG channel. As mentioned in subsection 3.5.3, because photodiodes are unidirectional, and since this photodiode module consists of only one photodiode, only unipolar pulses can be produced. Hence, only unipolar voltage waveforms can be synthesized in this setup, which means, that a sine wave can only be synthesized, if it includes a larger DC offset.

Based on the pulsed characterization of the unipolar photodiode module (see (**Article 2**)),

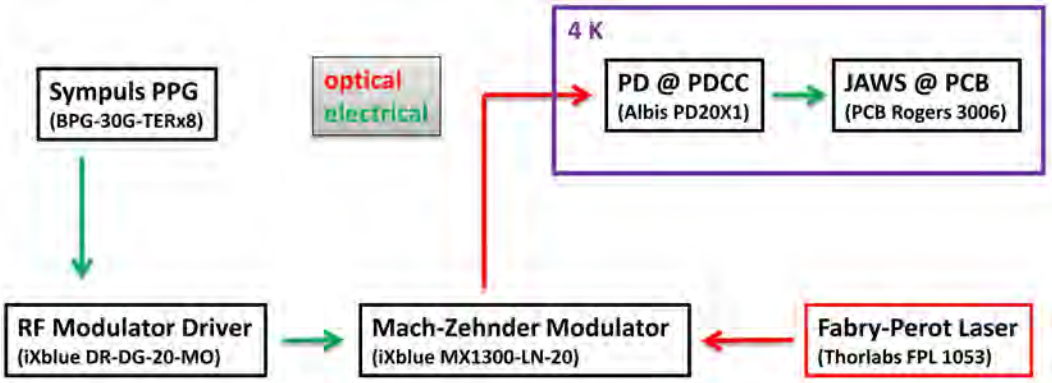

Figure 3.18: Schematic of the setup used for operating the unipolar photodiode module to synthesize voltage waveforms from a JJA. The figure is lifted from (**Article 7**).

a JJA with 3000 JJs with I_c= 2.8 mA and f_c= 4.2 GHz was chosen for this experiment. The photodiode module was attached to the JJA, and the output was measured for both DC and AC output voltages, by using two different schemes. First, a constant pulse pattern was applied on the JJA in order to realize DC-voltage Shapiro steps. This was done by coupling the JJA to a current-voltage curve tracer, which sweeps a DC-current bias on the constant pulses in order to measure the various stable constant-voltage Shapiro steps. These results are presented in (**Article 7**).

A sigma-delta pulse code was applied on the photodiode-driven JJA, and curve tracer was replace by the high-speed, low-noise digitizer NI-PIX5922. The digitizer was used to sample the synthesized voltage waveform, and the data was used to analyze the spectrum of the synthesized waveform. The setup used for measuring and analyzing the waveform was already presented for the case of electrical pulsation in Fig. 3.3.

3.6.4 Bipolar pulsation

A complete JAWS system require the ability to generate voltage waveforms with both positive and negative polarities. Therefore, the setup described in the two previous subsections would have to be developed further to accommodate the newly developed bipolar photodiode package described in subsection 3.5.3. In such a setup, two optical PPG channels would have been needed, that is, two 1310 nm lasers, two MZMs, and two modulator drivers put together, and an electrical bit patterns from two PPG channels. One optical channel is led to the positively coupled photodiode, and the other is led to the negatively

coupled photodiode. A ternary bit pattern (consisting of '+1', '0' and '-1' bits) can be used to generate a bipolar waveform from a JJA with photodiodes as source. For this case, only the amplitude of the positive bits are non-zero for the PPG channel that leads to the positively coupled photodiode, and likewise, only the amplitude for the negative bits are non-zero for the PPG channel that leads to the negatively coupled photodiode. As a result, the pulse pattern from the bipolar photodiode module corresponds to the bit pattern from the PPG.

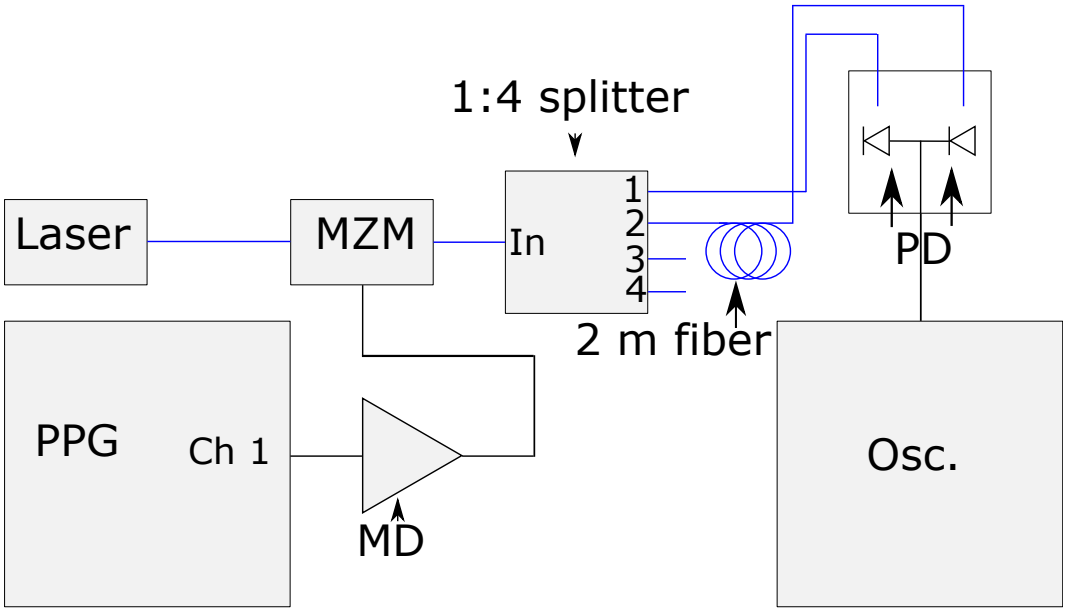

Figure 3.19: Schematic of the setup used to mimic bipolar optical pulses, and then measure the response form the bipolar photodiode module.

Unfortunately, we were not able to put together this bipolar optical setup, so we had to make due with the second best option to demonstrate bipolar operation. The unipolar optical setup described in subsection 3.6.2 was used as a basis to form the setup shown schematically in Fig. 3.19, where the 1:4 optical splitter Thorlabs FCQ1315-FC was used to split the output signal of the MZM. Output channel 1 from the splitter was led directly to the positively coupled photodiode, and channel 2 was led to the negatively coupled photodiode via a 2 m fiber extension, effectively delaying these pulses by about 10 ns. Thus, the pulses have been separated, and bipolar operation of the bipolar photodiode module can be demonstrated.

3.6.5 Pulsation using a mode-locked laser

The setup described in subsections 3.6.2 to 3.6.4 uses a modulator driver and a MZM to create laser pulses out of a CW laser. In (**Article 3**), it was discovered that the modulator driver limited the pulse speed obtained from the photodiodes. Therefore, the CW laser was replaced by a mode-locked laser (MLL) (described in [82]) as schematically depicted in Fig. 3.20, based on a 1340 nm wavelength. This setup was also used in (**Article 3**). The MLL produces laser pulses with a fixed FWHM at 15 ps, where the constant pulse repetition frequency is set by a microwave source (Agilent E4436B, labeled ”MW1” in Fig. 3.20), at a maximum of 2.5 Gpulse/s. The output of the MLL is split with a 94-6 optical splitter, where the 6 % output was fed directly to the ”New Focus 1014” 45 GHz IR photodetector, which is connected to channel 1 on the oscilloscope (Agilent Infiniium DCA 86100A oscilloscope with a 86112A channel module, 20 GHz bandwidth). The 94 % output was used to fed continuous pulses at point ”A”. Point ”A” was used to either feed continuous pulses to the commercially packaged photodiode or the bipolar module prototypes, or to a MZM (iXblue MX1300-LN-20) to select a pattern of pulses at point ”B”. The pulse pattern at point ”B” was also fed to the bipolar module prototypes. At both points, the photodiodes were measured at channel 2 on the oscilloscope.

When the MZM was used to modulate the pulse pattern from the MLL, another microwave source (Agilent E4436B, labeled ”MW2” in Fig. 3.20) was used to provide the modulation signal. In order to drive the MZM properly, the microwave had to be shaped into a square wave using a limiting amplifier (ONET1191P), and amplified by a modulator driver (iXblue DR-DG20-MO). Instead of using a microwave source and a limiting amplifier, sources providing square-shaped bit patterns, such as a PPG, FPGA or AWG could have been used; however, these were not available during these measurements.

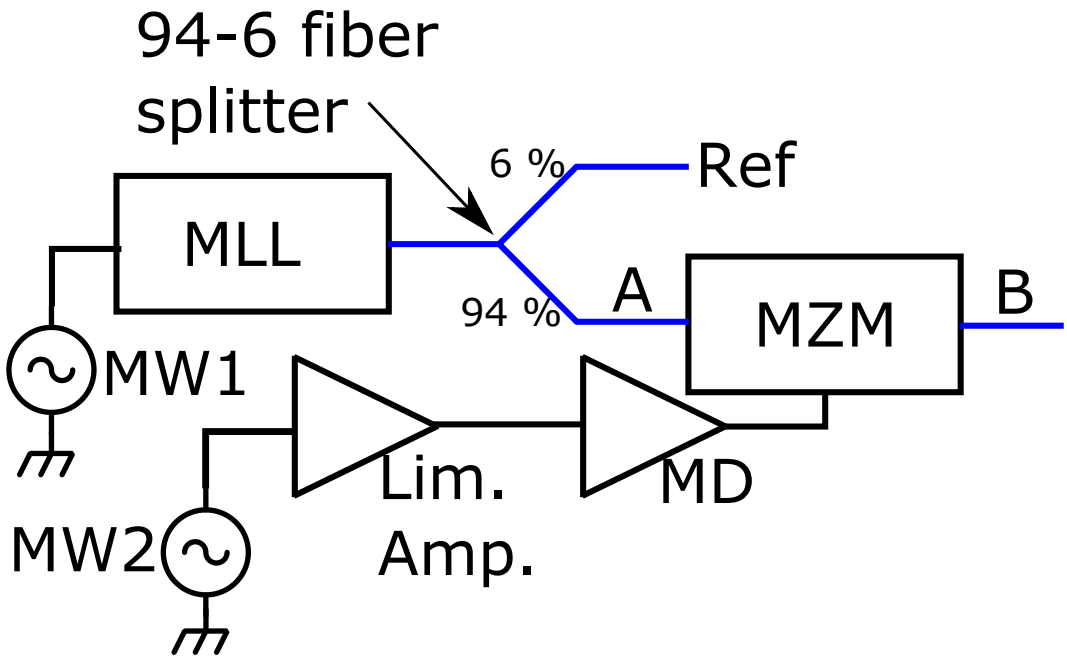

Figure 3.20: Schematic of the setup used to characterize the bipolar photodiode modules using a fast MML for fast laser pulses at 1340 nm. The microwave source MW1 was set to roughly 2.3 GHz to produce a continuous pulse train, of the same repetition frequency from the MLL. The pulses from the MLL have a FWHM less than 15 ps, independent of the frequency of MW1. The output signal of the MLL is split by a 94-6 optical splitter, where the 6 % output is used as a reference signal for the continuous pulse pattern, and the 94 % (the point denoted ”A”) is used either directly to the bipolar photodiodes, or indirectly via the MZM at point ”B”. When the modulated output is used, the microwave source MW2 provides the modulation signal, which is shaped into a square wave by the limiting amplifier (labeled ”Lim. Amp.”), and amplified by the modulator driver (labeled ”MD”).

3.7 Results, Discussions and Further Work

This section contains a brief summary of the obtained results from this research through the attached (**Articles 2-7**). The shortcomings of the current method for synthesizing AC voltage waveforms are also discussed, and with proposals to improving the setup. At the end of this section, a description of suggested further work is presented.

3.7.1 Results Summarized

The main benchmark from this research has been the development of a unipolar photodiode module, which is operable in liquid helium. It has been used to produce fast current pulses, with FWHM as low as 77 ps, and pulse peak heights as tall as 16 mA in (**Article 2**). This module has also been used to realize both DC and AC voltages from various JJAs, and most notably, an array consisting of 3000 JJs was used to synthesize a unipolar waveform (sine wave with a larger DC offset) of 18.6 mV_{pp} at 1.875 kHz with a distortion suppression of -92 dBc (**Article 7**). This successes led to the construction of our first prototype bipolar modules, one with and one without 50 Ω on-chip termination, which were tested in (**Article 3**). The unterminated version was used to demonstrate bipolar pulsation.

3.7.2 Challenges in pulsation

Towards the end of section V in (**Article 2**), the concern is raised about the reduction in maximum pulsation bit rate that can be expected from the setup. According to the PPG's data sheet, assuming linearly rising and falling flanks, the full rise-and-fall time limits the maximum pulsation bit rate to 15 Gbit/s, which corresponds to the maximum return-to-zero bit rate that the PPG can be set to produce. It was further discussed, that since the rise/fall times of the modulator driver was significantly slower than that of the PPG used in the factory-calibration, then it would further reduce the maximum pulsation bit rate to about 12 Gbit/s, and that the MZM probably would reduce it even further.

From the characterization of the single pulse response of the unipolar photodiode module in (**Article 2**), the shortest measured FWHM was at 77 ps, which is about 40 ps wider than the corresponding pulses from the PPG. This of course, is a significant widening of the pulses, which at first was assumed to be caused by either the cooling of the photodiode, or the packaging. However, in (**Article 3**), the FWHM of both photodiodes in the terminated bipolar module, the unipolar module, the PPG, and the modulator driver were plotted together (plot repeated in Fig. 3.21). By doing this, the main cause for the widening of the pulses became quite apparent, that the modulator driver is the bottleneck for the pulsation bit rate, as all of the other curves overlap. Obviously, the photodiodes cannot put out pulses faster than the incoming optical pulses, and therefore, a setup similar

to that which is described in subsection 3.6.5 is needed to increase the maximum pulse rate from the photodiodes.

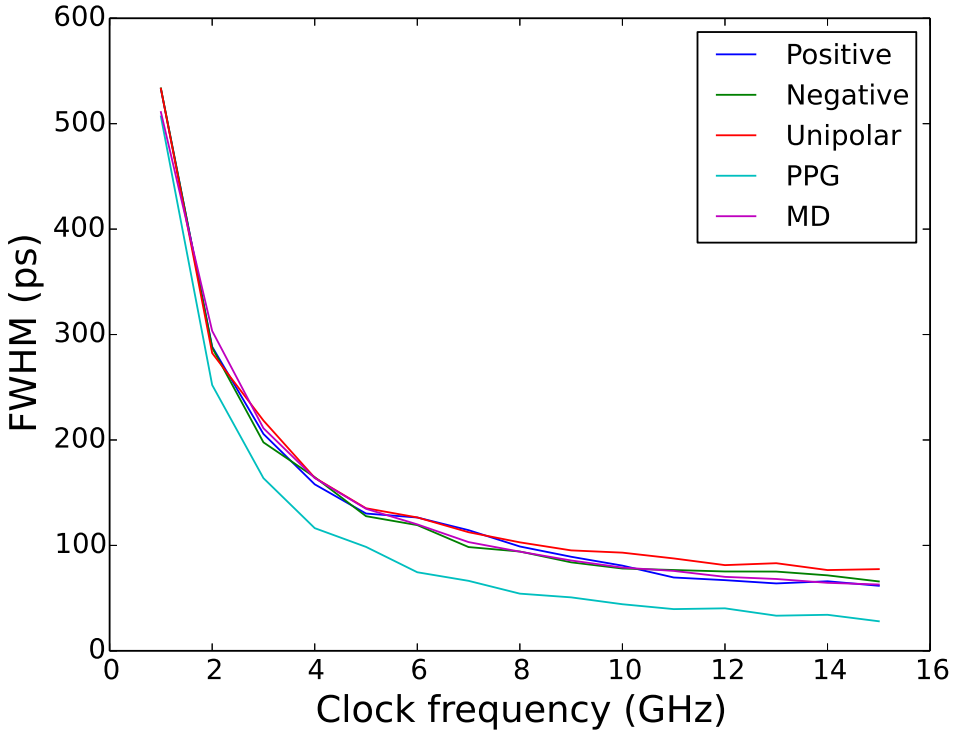

Figure 3.21: Measurement results of the FWHM of the bipolar module, the unipolar module, the PPG, and the modulator driver. The positive and negative photodiodes on the bipolar module, labeled ”Positive” and ”Negative”, respectively. The unipolar photodiode is labeled ”Unipolar”. The PPG and the modulator driver are labeled ”PPG” and ”MD”, respectively.

Because a strict DC voltage was used for the biasing of the MZM, the sigma-delta code amplitude, for which quantized waveforms could be synthesized, was limited to 0.2. Since the RF-path between the PPG and the MZM contains multiple DC blocks, the voltage level for ’0’ that is delivered to the MZM becomes dependent upon the momentary pulsation bit rate, which obviously affects the extinction of the optical ’0’ when a CW laser is used as the optical source. Likewise, ’1’ might also be impacted by a small extinction, when it ideally should be none. Therefore, an AC perturbation should be added to the MZM bias in order to make optical pulses that are less dependent upon the momentary pulse density.

3.7.3 Revision of the bipolar photodiode module

(**Article 3**) demonstrated that the current bipolar photodiode module could produce pulses as narrow as those from the unipolar module could, when the CW laser is used as optical source. Further, it demonstrated that even faster pulses could be produced when a fast MLL is used as optical source. However, it was also shown that the 50 Ω on-chip termination resistor was necessary to reduce the ringing after the pulses, in the current layout, when the photodiodes are separated by 4.5 mm. This ringing was also reproduced by the COMSOL simulation model of this design (see subsection 3.5.4). By modifying this model to place the two photodiodes only 500 μm apart, center-to-center, the simulation model (simulation results in Fig. 3.22) predicts a significant reduction in the ringing after the pulse, compared to the current design, which probably makes the on-chip termination redundant. The simulations both with and without including the inductive behavior of the wire bonds were performed on the proposed new design, and is also shown in Fig. 3.22. For the first tests with this new design, versions both with and without on-chip termination will be tested, to see whether or not it can be removed to the advantage of higher output pulse peak height.

In order to make contact with a photodiode pitch of 500 μm, the ferrule ended fibers cannot be used, as these have a diameter of 1.8 mm. Therefore, a new technique must be developed to make optical contact, which is both robust, and easy to connect. For future research, we will attempt to develop a custom fiber coupling, with two pairs of de-coated fibers. These fibers can be placed in a v-grooved silicon chip, and the lasers will be beamed from the fibers to the photodiodes, via mirrors embedded in this chip. With this optical connection, we will be able to make a dual-channeled, bipolar photodiode module, to operate two JJAs simultaneously, all on a single chip.

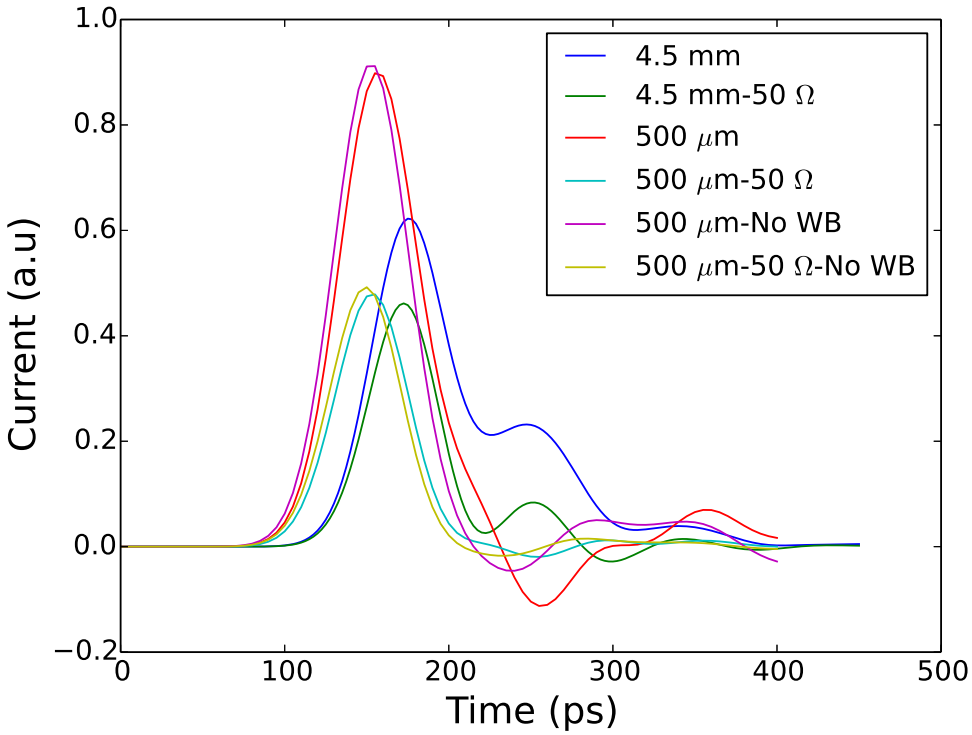

Figure 3.22: COMSOL simulation results from the bipolar photodiode modules. The label ”4.5 mm”, refers to the current model (shown in Fig. 3.13), where the photodiodes are separated by 4.5 mm. The label ”500 μm”, refers to the suggested new module (shown in Fig. 3.14), where the photodiodes are separated by only 500 μm. The label ”No WB” refer to the module where the inductive, wire-bond effect has been removed. The label ”50 Ω” refer to the inclusion of a 50 Ω on-chip termination onto the chip-carrier.

4. Summary, Conclusion and Further work

This PhD work has consisted of a minor topic about transfer of traceability of AC voltage and electrical power via a resistive voltage divider and buffer amplifier and a major topic about the use of cryo-cooled photodiode modules synthesize quantum-based AC voltage waveforms from pulse-driven Josephson junction arrays.

4.1 Voltage Divider and Buffer Amplifier

A unity gain buffer amplifier and a 10:1 resistive voltage divider has been constructed from this work. Although the buffer and the divider and buffer union were intended to be used for up to 1 V outputs, the devices were demonstrated to handle 5 V. Unfortunately, due to current sourcing from the buffer, the lower cut-off for the output voltages were set to 0.5 V. This is also seen in the measurements of the AC-DC difference of the divider and buffer union, where the DC offset caused by the current sourcing gives rise to an offset in the AC-DC difference already at 10 Hz. Another issue is that the AC-DC response of the divider and buffer union is not low enough to use it beyond a few hundred kHz. The current divider and buffer union is only applicable in electrical power metrology.

In order to make the divider and buffer useful in AC voltage metrology, the AC-DC difference needs to be reduced to less than 10 μV/V for frequencies up to 1 kHz, and a few hundred μV/V up to 1 MHz. The first and perhaps most important measure would be to remove the current sourcing from the buffer. The second measure would be to introduce a guard for the divider, so that the capacitive leakage is reduced for higher frequencies (up to 1 MHz). The third measure would be to introduce a capacitive switch-box (similar to the one used at RISE), with a greater flexibility to fine-tune the activated capacitance. In AC voltage and electrical power metrology up to 1000 V, full set of voltage dividers would go all the way up to 1000:1, with two dividers per decade.

4.2 Optically-Driven Josephson Arbitrary Waveform Synthesizer

Optical pulse-drive of a Josephson junction array with 3000 junctions has been demonstrated by using a cryogenically operable unipolar InGaAs photodiode module to convert fast laser pulses into current pulses. Because only unipolar current pulses could be pro-

duced, only unipolar AC voltage waveforms could be synthesized from the Josephson junction array. The photodiode alone could produce pulse peak heights as high as 16 mA, and full-width-half-maximum of 77 ps, although even faster pulses at 37 ps have been observed from the bipolar module using a fast mode-locked laser as source of optical pulses. Waveforms up to 18.6 mV peak-to-peak at 1.875 kHz with suppression of distortion of -92 dBc were synthesized. This came as a result of using a sigma-delta-code amplitude (a well-defined real number related to the relative maximum pulse rate in the code) of 0.2, compared to an amplitude of 0.9 typically used in direct coupling between the pulse pattern generator and the Josephson junction array, with low-frequency compensation. The maximum code amplitude for the optical pulse-drive could have been increased, by applying a low-frequency perturbation to the bias of the Mach-Zehnder modulator, to maintain the pulse quality invariant with the pulse density.

A cryogenically operable bipolar module has been developed as a result of the success of the unipolar module. Versions both with and without on-chip terminations of the high-frequency transmission lines have been tested with fast laser pulses, while immersed in liquid helium. The produced current pulses from these prototypes included a low of ringing. Due to the 4.5 mm separation of the two photodiodes, which is comparable to the propagation wavelengths of the signals above 10 GHz, ringing was an expected outcome. This was also replicated by simulations in COMSOL Multiphysics, which also indicate that the ringing will be almost completely removed by placing the photodiodes closer together, to a separation of only 500 μm, center-to-center. According to these simulations, only a 10 % attenuation of the pulse produced in the photodiode can be expected, which means that pulse peak heights of at least 14 mA is achievable with this configuration. In order to accomplish this, a new method to make optical contact to the photodiodes has to be developed, which is already in progress.

When the above-mentioned technique has been matured, chips with Josephson junction arrays will start to include photodiode chip-carriers. This is to reduce the distance from source (i.e. the photodiodes) and load (i.e. the Josephson junction array), and to remove the need for inductive wire bonds to transfer the pulses. This will increase the quality of the pulses that are applied to the Josephson junction arrays, and thus increase the

effective pulse rate and number of junctions that can be quantized at the same Shapiro step.

A. Python script for simulating the transport of magnetic flux quanta

The following is the python code that was used to perform the simulation of magnetic flux quanta over a single overdamped Josephson junction with realistic junction parameters. This code was used to obtain the results presented in Fig. 11 in (**Article 1**).

```
import scipy
import numpy as np
import matplotlib.pyplot as plt

# Realistic JAWS array parameters
Ic=2.9  # [mA]  Critical current
fc=10.  # [GHz] Characteristic frequency
scale=[0.60,0.85,1.00]  # Scaling factor of the current to




# PD pulsation
nData=4000      # Number of data points in the file
TimeStamps=[1700,1830]
Lab=["0 min","90 min"]
f=[10]  # [GHz]
# Setting resolution of the oscilloscope
dt=np.zeros(len(TimeStamps))
for i in range(len(TimeStamps)):
  dt[i]=0.5/1000.       # ns

ti=[ [0] * n for _ in range(len(TimeStamps))]   # Time array
# Setting simulation timescale for the Stewart-McCumber,
# i.e. time/2*pi*fc
```

```
for i in range(len(TimeStamps)):
  for j in range(n):
    ti[i][j]=j*dt[i]*2.*np.pi*fc

# Waveform data [mA]
Idata=[ [0] * nData for _ in range(len(TimeStamps))]
# Simulated phase of the superconducting waveform between
# the superconductive electrodes, according to
# the Sewart–McCumber model
phiData=[ [0] * nData for _ in range(len(TimeStamps)*len(scale))]
# Simulated phase derivative of the superconducting waveform
# between the superconductive electrodes, according to
# the Sewart–McCumber model
dphiData=[ [0] * nData for _ in range(len(TimeStamps)*len(scale))]

for i in range(len(TimeStamps)):
# Opening and reading input data file:
  ReadFile=open(str(TimeStamps[i])+".txt","r")
  indata=ReadFile.readline()
  a=indata.split(",")   # Splitting input data into a string array
  for k in range(len(scale)):   # For each margin extrema
    for j in range(nData):      # Treating all data points
# Converting data from V over a 50 ohm load into mA,
# and normalizing to the critical current, Ic:
      Idata[i][j]=float(a[j])*20./Ic
# Correction for the 8 dB attenuator on the oscilloscope:
      Idata[i][j]=Idata[i][j]*(10.**(8./20.))
# Scaling down from maximum current:
      Idata[i][j]=Idata[i][j]*scale[k]
      if j==0:
        phiData[i+k*len(TimeStamps)][j]=0.  # Initial phase
```

```
      else:
# Updating phase from the phase deriative from
# the Setwart-McCumber model:
        phiData[i+k*len(TimeStamps)][j]=
          phiData[i+k*len(TimeStamps)][j-1]
          +dphiData[i+k*len(TimeStamps)][j-1]
          *(ti[i][j]-ti[i][j-1])
# Calculation of phase derivative from the Stewart-McCumber model
      dphiData[i+k*len(TimeStamps)][j]=
        Idata[i][j]-np.sin(phiData[i+k*len(TimeStamps)][j])
# Scaling back to maximum current:
      Idata[i][j]=Idata[i][j]/scale[k]
    for j in range(nData):
# Converting the phase from rad to rad*2*pi:
      phiData[i+k*len(TimeStamps)][j]=
        phiData[i+k*len(TimeStamps)][j]
        /(2.*np.pi)

# Curve colors blue (initial data serie)
# and red (final data series):
color=['b','r']

# Setting the real time axis for the simulation:
for i in range(len(TimeStamps)):
  for j in range(nData):
    ti[i][j]=1000*j*dt[i]

# Plotting of the simulated data:
for i in range(len(TimeStamps)):
  plt.plot(ti[i][:],phiData[i][:], label=Lab[i],color=color[i])
  plt.plot(ti[i][:],phiData[i+2][:],color=color[i])
```

```
    plt.plot(ti[i][:],phiData[i+4][:],color=color[i])
plt.legend(loc=2,fontsize=15)
plt.xlabel("Time (ps)",fontsize=15)
plt.ylabel("Phase transition (2$\pi$ rad)",fontsize=15)
plt.show()
```

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Article 1:
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Int. J. Metrol. Qual. Eng., Vol. 10, Aug. 2019, DOI: 10.1051/ijmqe/2019006

Int. J. Metrol. Qual. Eng. **10**, 8 (2019)

https://doi.org/10.1051/ijmqe/2019006

International Journal of Metrology and Quality Engineering

Available online at:
www.metrology-journal.org

RESEARCH ARTICLE OPEN ACCESS

Characterization of high-precision resistive voltage divider and buffer amplifier for ac voltage metrology

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Received: 11 April 2019 / Accepted: 4 July 2019

Abstract. A high-precision voltage buffer and a 10:1 resistive voltage divider have been constructed for use in ac voltage and electrical power metrology. Long-term stability of the buffer's dc response has been demonstrated by two dc sweeps performed 20 days apart, with best-fit linearized gain varying less than 1 μV/V. The absolute ac gain has been measured using a high-precision digital multimeter for 10 Hz and 1 kHz with results consistent with dc within 5 μV/V. This value agrees with the characterization of ac–dc difference using thermal converters from different producers with a variety of resistance for various voltages from 1 V to 5 V. The ac–dc difference was further characterized better than 40 μV/V for the same voltages up to 100 kHz and better than 100 μV/V for 3 V at 1 MHz. Absolute ac gain and ac–dc difference has also been measured for the voltage divider and buffer combination from 10 V to 50 V, with similar agreement up to 1 kHz. The ac–dc difference from 10 Hz to 100 kHz of this combination shows an agreement well within 30 μV/V in this entire voltage span with a total response not exceeding 125 μV/V. This make the voltage divider and buffer combination suitable for sampling electrical powers for a wide range of voltages.

Keywords: ac voltage metrology / traceability / voltage buffer / resistive voltage divider

1 Introduction

Today's developments within the electronics industry have greatly advanced the performance of analogue-to-digital and digital-to-analogue converters in terms of speed, resolution, accuracy and power consumption. Consequently, the accuracy requirements for the calibration of these instruments have become even greater. This has driven the need to improve both measurement standards and methods of traceability transfer, so that more accurate calibrations can be delivered.

Although extensive efforts have been made to push pulse-driven Josephson setups to synthesize ac voltages beyond 1 V [1–3], standards and techniques to transfer the traceability are also needed to perform more accurate calibrations. In practice, more convenient instruments, such as thermal converters (TCs), and digital multimeters (DMMs), such as Fluke 5790A and Keysight 3458A, are used to perform every-day calibrations. The most precise of these are the TCs, which transfer traceability from dc to ac, by making a thermal comparison between applied ac and dc voltage (or current). These have long been the preferred standards for ac voltage, where voltages up to 1000 V can be traced by coupling the TC in series with range resistors (RRs).

In a similar manner, a voltage divider and voltage buffer combination can be used to extend the traceability range. Whereas a RR serves as current limiter for the TC, a voltage divider has a given division ratio, which it applies to the input voltage. Consequently, a divider and buffer combination can be used to extend the traceability range for a much wider range of instruments.

Good examples of previously constructed voltage buffers are those made by Budovsky et al. [4,5]. These voltage buffers have been made in different varieties intended for different loads. Budovsky et al. have also constructed a few resistive as well as inductive voltage dividers for ac–dc transfer and power metrology [6,7]. Another buffer has been constructed together with a 120:4 resistive voltage divider by Lei et al. [8], where they have characterized it using a Fluke 5790A. An array of resistive voltage dividers have also been made at the Swedish metrology institute (RISE, earlier SP) [9,10].

Through the previous EMRP project "Power & Energy", current shunts and a few resistive voltage dividers were constructed at Justervesenet (JV). The current shunts proved quite successful [11], whereas only one 100:1 divider turned out satisfactory. A further development of the previous work has been initiated,

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[a] Retired.

with dividers ranging from 10:1 up to 1000:1, all specified to give out nominal voltages in the range 0.5 V to 5 V. A first prototype of the 10:1 divider and a voltage buffer amplifier have been constructed. In this paper, these have been characterized on both absolute gain and ac–dc difference.

In the future, we intend to use the voltage divider and buffer together with current shunts [11] to sample a wider rang of applied electrical powers [12]. For this application, it is important that a given range of applied powers only has a small impact on the divider's division ratio, so that the response can be accurately compensated. Therefore, it is important to characterize the voltage divider and buffer on absolute gain, as well as ac–dc difference. We also intend to use the voltage divider and buffer to divide a wider range of applied voltages from a calibrator, to compare the signal generated from Josephson-based setups.

2 The ac–dc difference

For traceability in ac voltage metrology, thermal transfer via ac–dc difference measurements are still the industry standard, even though Josephson-based ac voltage waveform synthesizers are beginning to become a part of traceability chain. The ac–dc difference (for voltage) is measured by setting two objects (a reference and a test object) in parallel to each other, and simultaneously measure the heat deposition from the load resistance from alternately applied ac and dc voltage. The heat is indirectly measured by a thermocouple. The ac–dc difference is measured either directly using a TC-based DMM, or indirectly using a TC with an external DMM. The TC can be used alone or together with RR, buffer or voltage divider. In any case, the amplitude of the applied ac voltage is adjusted, so that the dissipated power (E_{ac}) matches the dissipated power (E_{dc}) of the dc voltage, in the reference. The measured ac and dc voltage in the test object, denoted V_{ac} and V_{dc}, respectively, are inserted into equation (1) to calculate the ac–dc difference, δ. A more thorough explanation of measurements of ac–dc difference can be read in [13].

$$\delta = \frac{V_{\mathrm{ac}} - V_{\mathrm{dc}}}{V_{\mathrm{dc}}}, E_{\mathrm{ac}} = E_{\mathrm{dc}}. \quad (1)$$

3 Voltage buffer design

The buffer design described in this paper is depicted in Figure 1, and it is a further development of the versions described in [14,15]. Its core module is based on two complimentary Sziklai pairs with diode-coupled (base-collector is shorted) feedback. This is a similar design to those often found in audio amplifiers. Whereas a Darlington pair consists of either an NPN transistor driving another NPN, or a PNP driving another PNP, a Sziklai pair [16] consists of an NPN driving a PNP, or vice versa. Both Sziklai and Darlington pairs are used to amplify the signal applied to the input twice on its way to the output. Furthermore, using two complementary pairs, as have been done in this design, a push-pull configuration is made,

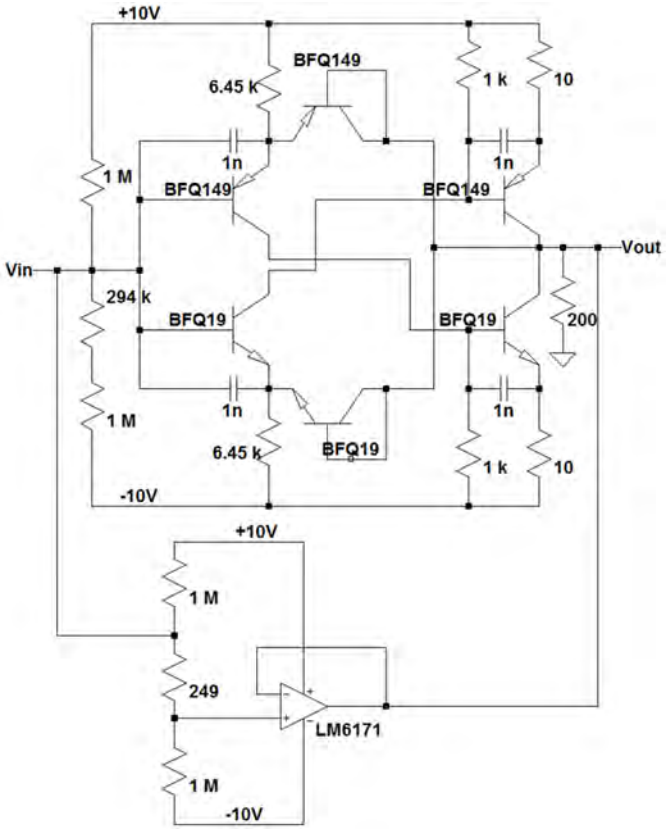

Fig. 1. Schematic of the voltage buffer where Vin is the input female N-connector and Vout is the output male N-connector. The ground on the power supply is coupled to the chassis and outer conductor of the N-connectors. The main buffer core is the push-pull coupled Sziklai pairs (NPN: BFQ19, PNP: BFQ149) with diode-coupled (base-collector is shorted) feedback. The module based on the LM6171 operational amplifier serves as a voltage follower which senses and corrects for the errors in the output waveform produced by the previously mentioned buffer core. The non-inverting input has been shifted downwards in voltage to compensate for the internal offset in the LM6171.

which amplifies the signal more equally for both positive, and negative voltages. This is a good wideband design, because fewer stages generally cause only a short time delay. The transistors selected have a relatively similar operation specs with specifications up to 100 mA collector current, and with maximum operational frequencies of 5 GHz and 5.5 GHz for PNP (BFQ149) and NPN (BFQ19), respectively. This should have a relatively flat frequency response up into the MHz range.

However, contrary to what is normal for audio amplifier circuits, this buffer must be able to amplify both ac and dc voltages rather than just ac signals. For strictly ac usage, large capacitors are generally placed on both input and output in order to avoid dc current sourcing. This cannot be done in a design like this as dc voltages also must be applicable. Because of this, the sourcing is minimized by tweaking the input resistance to compensate for the leakage.

Transistors in general have an exponential current–voltage (IV) characteristic, whereas an amplifier have to be

linear in order to put out a pure voltage waveform. For metrology in particular, avoiding distortion is of utmost importance, so the transistor characteristics is dragged into more linear operation points, to the cost of higher supply power consumption. Also, for a push-pull configuration, the risk is that the operation points of the transistors are not set appropriately, so that either a horizontal or vertical plateau in the IV-characteristic may occur in the cross-over point. Individual mismatch between the threshold voltages of the transistors, may cause an uneven transition of operation between them. In other words; the individual mismatch of the transistors could cause one of the in- or output transistors to either shut or leak when it is not supposed to do so, and thus lead to a spike around 0 V input. This is an issue that might be present in a physical circuit, but not the simulated one.

Most of the current needed to drive the load is provided by the main buffer-core. However, its gain is slightly dependent upon the applied voltage, which distorts the output waveform. To rectify this error, a high-speed, low-distortion, unity-gain amplifier has been added as a correctional stage. This amplifier has been coupled as a non-inverting voltage follower where the working point for the non-inverting input has been shifted in order to compensate for its internal offset. The purpose of this stage is to correct the non-linearity of the buffer core stage by sensing, and then equalizing the difference in voltage level between the buffer's input and output.

The buffer has been designed to optimize two features, namely good dc and ac gain linearity. For this purpose, a simulation model was made in LTspice version 4.23l based on transistor models created by the original producer, Philips Semiconductors, and the model of the operational amplifier created by National Semiconductor, Inc. This simulation model takes into consideration the parasitic contributions of the transistorsa and connectors. Generally, parasitic contributions do not make too much of an impact however; in a feedback circuit, such as this buffer, these contributions may lead to undesired oscillations. In fact, before these parasitic contributions were included into the model, constructed prototypes had a tendency to oscillate at frequencies above 100 MHz, where as this behavior was not mirrored in the model. After introducing these parasitics into the model, the oscillations started to show up in the simulation results as well. These oscillations were quenched in both the model and the prototypes by including 1 nF base-emitter capacitors.

As stated previously, good dc-gain linearity is important for ac–dc comparisons, even for low frequencies. The dc-gain of an amplifier is expected to be constant, hence the output voltage follows:

$$V_{\text{out}} = a * V_{\text{in}} + b, \tag{2}$$

where V_{out} is the output voltage, V_{in} is the input voltage, a is the gain and b is the offset. Simulation of the dc gain linearity in the range from −1.5 V to 1.5 V is presented to the top of Figure 2 as the output voltage subtracted by the linearized gain of the buffer (Eq. (2)). The sweep is presented this way in order to magnify any non-linear tendencies in the dc gain. For a load equivalent to an HP 3458A DMM, the linearization gave $a = 0.999\,722$ V/V and $b = 249\,\mu$V and variation within $\pm 1\,\mu$V.

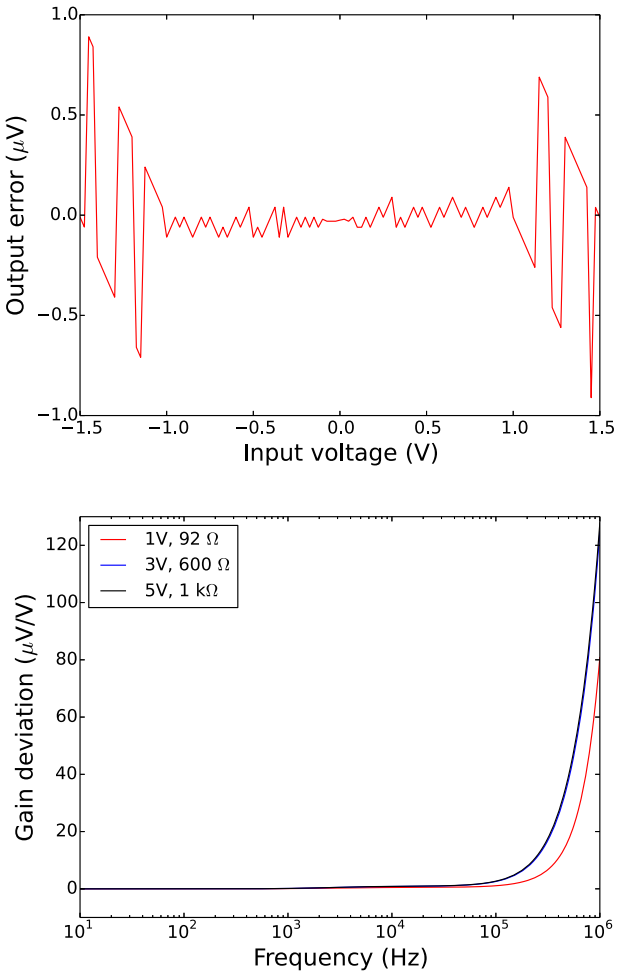

Fig. 2. Simulation results from the optimized buffer model. The top graph is the simulation of error in dc gain linearization according to equation (2). The bottom graph is the simulation of ac gain deviation from 10 Hz for 1 V, 3 V and 5 V input voltage with loads equal to the TCs used in equivalent measurements of ac–dc difference.

Table 1. Simulated ac gain at 10 Hz of the voltage buffer for the three cases of 1 V, 3 V and 5 V input voltage.

Input voltage (V)	Load resistance (Ω)	Gain (V/V)
1	92	0.999 706
3	600	0.999 719
5	1k	0.999 720

To ensuring a good ac gain linearity is to make the output of ac at higher frequencies (in metrology above 100 kHz) comparable to that of lower frequencies, as well as dc. Simulation of the ac gain is shown to the bottom of Figure 2, for 1 V (92 Ω load), 3 V (600 Ω load), and 5 V (1 kΩ load) input as deviation from the gain at 10 Hz. The gain at 10 Hz is shown in Table 1 for each of the three cases. The loads are chosen to mimic the TCs used for equivalent measurements of ac–dc difference.

4 Voltage divider design

The voltage divider is designed to attenuate signals up to 50 V and 1 MHz by a factor 10 V/V with a minimal dependance upon frequency and magnitude. In general, the signal will be supplied by calibrators such as Fluke 5730 or 5700. These calibrators can provide currents up to 35 mA, which means that the resistance of the divider must be selected large enough that this limit is not exceeded at 50 V.

The in- and output stages of the divider were set to be 1.8 kΩ and 200 Ω, respectively, so that the current drawn at 50 V dc would be no greater than 25 mA. However, the divider is to be directly loaded by the voltage buffer, which was described in the previous section. According to simulations, the input impedance of the buffer is 155 kΩ||16 pF. This load comes in parallel with the output stage of the divider, and it must be compensated to avoid a situation where the division ratio greatly depends upon frequency. Also, the geometry of the output stage of the divider contributes with parallel parasitic capacitance, which adds to the total output capacitance. To avoid a phase shift between the in- and output stages, relatively large capacitive components are added to the input stage as well. The aim is to have the product of resistance and capacitance of the input (R_i and C_i, respectively) equal that of the output (R_o and C_o, respectively):

$$R_i C_i = R_o C_o. \tag{3}$$

A simple calculation of the stray capacitance of the output geometry can be performed according to

$$C = \epsilon_0 \epsilon_r \frac{(r_o^2 - r_i^2)\pi}{d}, \tag{4}$$

where ϵ_0 and ϵ_r(=4.4) are the permittivity of vacuum and relative of FR4 (Flame retardant 4, circuit board material), respectively, r_o (=4 cm) and r_i (=1 cm) are the outer and inner radii, respectively, of the disc-shaped output plate, inside the divider, and d (=3.2 mm) is the thickness of two one-layered 1.6 mm thick FR4 boards (inside and outside the divider). Although the output of the divider has a lager disc on the outside than on the inside, the stray output capacitance is calculated according to the lesser disc. By putting these numbers into equation (4), the output stage stray capacitance becomes 57 pF. Added with the input capacitance of the buffer, the total added parasitic capacitance ends up at 73 pF. However, the exact total parasitic capacitance is difficult to accurately predict, and the commercially available capacitors generally have quite a wide tolerance (often up to ±5% of the nominal value). Therefore, the best capacitive compensation must be fine-tuned by a trial-and-error approach.

The voltage divider described in this paper has a cylindrical design with an outer shielding of copper. Both the input resistors and capacitors are mounted to a total of 8 narrow copper-plated FR4 strips, in parallel, 7 strips with resistors, and 1 with capacitors, as depicted in Figure 3. The reason for using only narrow strips is to reduce metal surface in the divider, and hence reduce capacitive leakage,

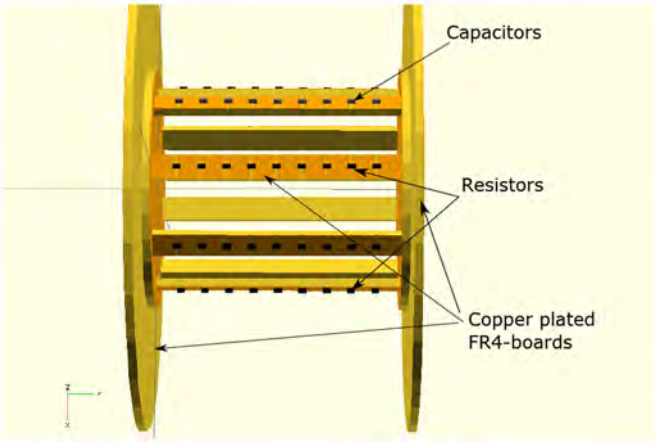

Fig. 3. Simplified model of the Voltage Divider's inner body. The black and grey prisms respectively represent 1.4 kΩ resistors and 330 pF capacitors.

which tends to have a great impact on the division ratio when approaching 1 MHz. The strips are mounted to the input and output planes of the divider, both going directly to their respective female and male N-connectors. The output resistors are mounted on the output connector, directly between the center conductor to a copper film on the flange.

In regards to the set resistance value of the input stage, surface mounted device (SMD) resistors of value 1.4 kΩ were selected, so that the equivalent circuit resistance became 1.4 kΩ*9(series)/7(parallels) = 1.8 kΩ. SMD capacitors of value 330 pF were used for the capacitive strip with an equivalent circuit capacitance of 300 pF/7(series) = 36.7 pF. For the output stage, the resistors were mounted in star formation across the N-connector from the central pin to the copper film on its flange. To form a 200 Ω output resistance, 5 resistors of 1 kΩ were put in parallel. As mentioned previously in this section, the best fit output stage capacitance must be arrived at by trial-and-error. For this reason, the easiest approach to insert this compensation is to couple it in parallel with the divider's output, in a separate box, in a similar fashion to that has been done by RISE [10]. This way, capacitors can be freely added or removed with no fear of altering any other parameters.

For these selected component values, and following equation (3), the theoretically correct total output stage capacitance (parasitic+buffer+compensation) should be 330 pF, and missing this with only a small amount will cause a substantial shift in the division ratio when approaching 1 MHz. The absolute value of the impedance of a parallel RC-junction can be written as

$$|Z| = \frac{R}{\sqrt{1 + (2\pi f)^2 C^2 R^2}}, \tag{5}$$

where R is the resistance, C is the capacitance, f is the frequency, and $|Z|$ is the resulting absolute value of the junction impedance Z. From this, and because the phase in the impedance will be chosen to be more or less the same for

Table 2. Results form the linear regression of the two dc sweeps. The parameters a and b represent gain and offset respectively.

Sweep no.	a (V/V)	b (μV)
1	0.999 701	–770
2	0.999 701	–778
Sim.	0.999 722	249

in- and output, the division ratio can be approximately expressed as

$$\frac{|Z_{\text{out}}| + |Z_{\text{in}}|}{|Z_{\text{out}}|} \tag{6}$$

where Z_{in} and Z_{out} refer to the in- and output stage impedance respectively. For the ideal case where all component values are perfectly nominal, missing the output capacitance by only 1 pF, will lead to a division ratio deviation of about 4000 μV/V at 1 MHz according to the equations (5) and (6).

The approach used to fine-tune the capacitive compensation is to aim for the lowest possible ac–dc difference, by using high-precision TCs. Quick series were measured, where the output capacitance of the voltage divider was tweaked to obtain the response of the ac–dc difference closest to 0 μV/V for the highest frequencies. The best fit was a nominal capacitance of 285 pF.

5 Results

In order to ensure that the gain linearity is good, two dc sweeps were performed 20 days apart, from −1.5 V up to +1.5 V, in steps of 25 mV. Both in- and output voltages were measured using a Keysight 3458A DMM as load. In an optimal buffer, the gain should be perfectly constant. A real buffer however, may have some variation in the gain, which gives rise to distortion of the output waveform. The input voltage versus output voltage for these two sweeps can again be expressed as the linear function in equation (2). The parameters found for each sweep is found in Table 2 together with the simulated values.

The results of the two sweeps are shown in Figure 4 as the output voltage, subtracted by the linear expression, using the corresponding parameter values of a and b. As alluded to in Section 3, such a plot should expose any non-linear tendencies in the buffer.

Two sweeps were performed to check whether or not the buffer had a tendency to over or under amplify any voltage regions, as well as to detect possible drift. Other than a narrow region around 0 V input, all deviations seem to be random. The gain remained within 1 μV/V the same however, as can be seen in Table 2, the offset had shifted downwards about 8 μV. This change is attributable to re-adjustments of the power supply between the two sweeps. The spike in the response in the cross-over point has already been alluded to in Section 3, and is most likely due to the variation of the production of the transistors. Still,

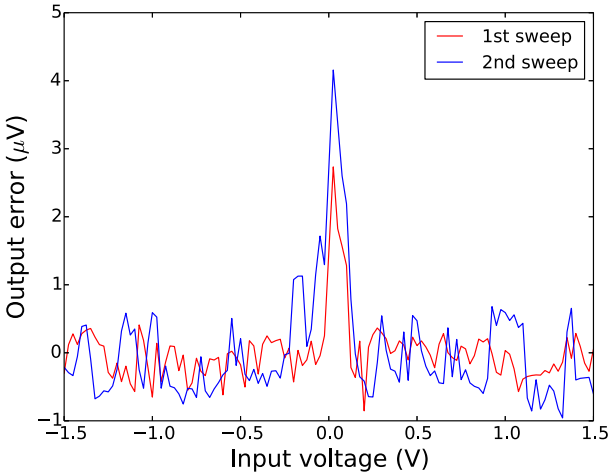

Fig. 4. Resulting error in the linear regressions (parameters found given in Tab. 1) of the two dc sweeps performed on the buffer. The first sweep is in red and the second sweep is in blue. The deviation is well within the ±1 μV band over the entire sweep between ±1.5 V with the exception of small section around 0 V. Here the output deviation peaks, but it is still less than 5 μV, and is due to the slight mismatch in the manufacturing of the transistors themselves since this feature is not found in the simulation presented on the top of Figure 2.

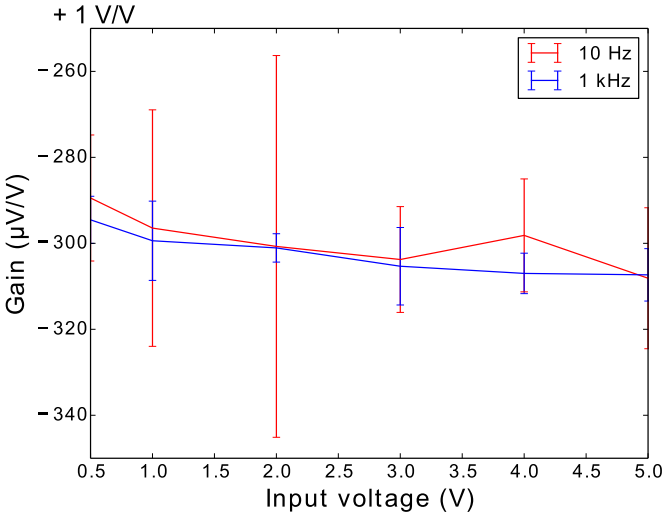

Fig. 5. Resulting absolute ac voltage gain of the buffer. The 10 Hz sweep is in red and the 1 kHz sweep is in blue.

the peak is less than 5 μV in the span of only a few hundred millivolt input voltage, which makes it insignificant compared to the total rms-integral for a nominal 1 V ac.

The absolute gain of the buffer was measured for voltages ranging from 500 mV up to 5 V at 10 Hz and 1 kHz using a Fluke 5790A as load. The signal was applied using a calibrated Fluke 5700A calibrator. The gain linearity of both series are presented in Figure 5 as absolute gain deviation from 1 V/V. The gain consistency was within 19 μV/V and 13 μV/V for 10 Hz and 1 kHz, respectively. For a nominal 1 V input, the gains were 0.999 704 V/V and 0.999 701 V/V for 10 Hz and 1 kHz, respectively.

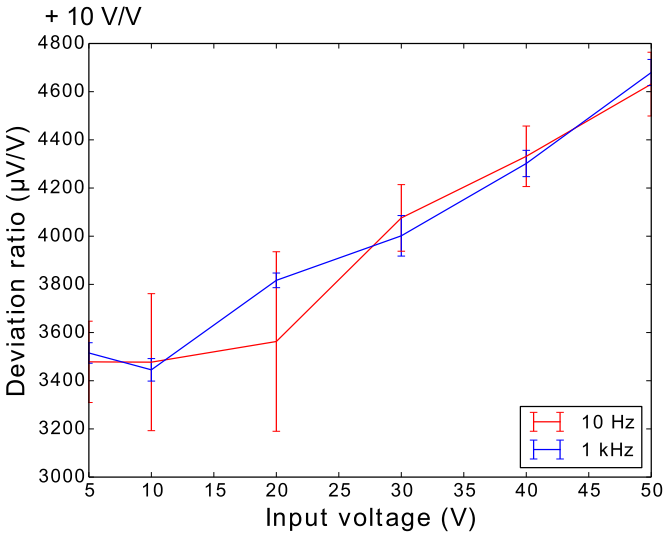

Fig. 6. Resulting absolute ac voltage division ratio of the divider and buffer combination. The 10 Hz sweep is in red and the 1 kHz sweep is in blue.

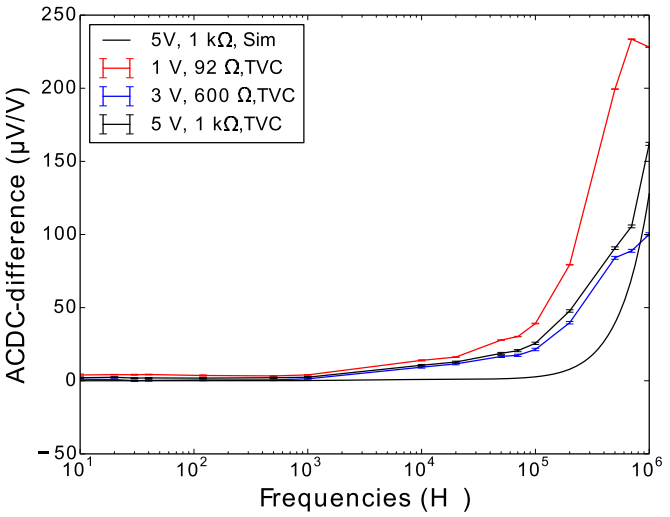

Fig. 7. Resulting ac–dc difference for the buffer from 10 Hz up to 1 MHz. The red curve contains the measurements for 1 V, the blue curve contains the measurements for 3 V, and the black curve contains the measurements for 5 V. The equivalent simulation of applied 5 V has been included in black, without error-bars.

The absolute gain was also measured for the combination of voltage divider and buffer from 5 V up to 50 V for 10 Hz and 1 kHz, in the same fashion as the buffer alone. Here however, it is more appropriate to present the data in terms of division ratio. The results are shown in Figure 6 as the absolute division ratio deviation from 10 V/V. The division ratio consistency was within 1150 µV/V around 10.003 48 V/V for 10 Hz and 1230 µV/V around 10.003 45 V/V for 1 kHz, both for nominally 10 V input.

In order to demonstrate the buffers all-round capability, it was characterized using three sets of TCs. The first set consisted of two 92 Ω TVs from Leibniz-Institut für Photonische Technologien (IPHT Jena), used at 1 V. Next were two sets from National Institute of Standards and Technology (NIST), a set of two 600 Ω TCs and a set of two 1 kΩ TCs, used for 3 V and 5 V, respectively. The characterizations were performed for the traceable frequencies from 10 Hz up to 1 MHz, with 4 measurements per frequency. The results of these characterizations are presented combined in Figure 7. The most noteworthy result is the measurement of 3 V with an ac–dc difference within 100 µV/V at 1 MHz.

For the ac–dc characterization of the voltage divider and buffer combination, the characterisation was performed for 10 V, 30 V and 50 V, using the same TCs as for 1 V, 3 V and 5 V, respectively, as loads for the buffer. As the reference, a combination of RRs (4 kΩ for 10 V and 12 kΩ for 30 V and 50 V) from Balentine and 600 Ω TCs from NIST were used. The results of these measurements are shown together in Figure 8 for frequencies up to 100 kHz. The variation of the ac–dc difference for these various loads and applied voltages is well within 30 µV/V from one another up to 100 kHz with frequency response not exceeding 125 µV/V.

The ac–dc difference for the divider and buffer combination, has a relatively large offset for lower frequencies compared to the buffer alone. The introduction

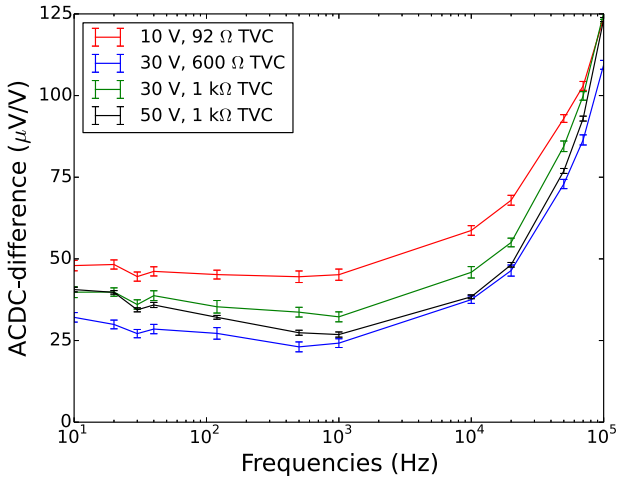

Fig. 8. Resulting ac–dc difference for the divider and buffer combination from 10 Hz up to the maximum capability of the calibrator. Red curve contains the measurements for 10 V, blue curve contains the measurements for 30 V, and black curve contains the measurements for 50 V. The green curve contains the measurements for 30 V, by using the references used for 50 V.

of a fully passive voltage divider should in principal not add to the low frequency response. One reason for this offset could be that the buffer sources current in both in- and output. When using the buffer alone, this sourcing could make an even impact on the reference and object TCs, whereas when the voltage divider is attached to the input of the buffer, the sourcing from the buffer's input is absorbed by the output stage of the divider. Other reason could be either leakage current to ground in the divider or some large induction in the divider itself.

6 Discussion

The real strength of the buffer, is its relatively low variance in both absolute gain and ac–dc response in a wide spectrum of voltages and load impedance. The ac gain varied less than 20 μV/V over an entire decade of voltages from 500 mV to 5 V for both 10 Hz and 1 kHz. For both ac and dc, the gain at 1 V differ less than 4 μV/V, which is especially good as they are loaded by two vastly different DMMs. This robustness is also shown in the ac–dc response, where the applied voltage spans half a decade and the load resistance of the TCs span more than a decade. From 10 Hz up to 1 kHz the ac–dc response for all three measurement series are within 5 μV/V. Comparing this to the just mentioned variation in absolute gain at the same frequencies, it agrees within 5 μV/V in the same direction (meaning slightly higher gain for 10 Hz), and hence good consistency and robustness in the buffer for various voltages and loads.

Combining the voltage divider and buffer, the absolute division ratio for 10 Hz and 1 kHz differed less than 40 μV/ V from each other at 10 V, and less than 3500 μV/V from the nominal 10 V/V division division ratio. Compared to the ac–dc difference at 10 V using the 92 Ω TC as load, the response varies within 5 μV/V (corresponding to a deviation of 50 μV/V in absolute division ratio) in the entire span from 10 Hz to 1 kHz. From 10 V to 50 V the division ratio increases almost linearly but equally for both series, and differing only about 50–100 μV/V at 30 V and 50 V. Again, comparing this to the equivalent measurements of ac–dc difference, from 10 Hz to 1 kHz these measurements only vary within 10 μV/V (corresponding to a deviation of 100 μV/V in absolute division ratio) as well. From this, it can be concluded that in the frequency range 10 Hz to 1 kHz both the measurements of absolute division ratio and ac–dc difference are in good agreement for both the buffer alone and the divider and buffer combination.

Up to 10 kHz, the ac–dc response of the voltage divider and buffer is flat and consistent, although with an offset. In electrical power metrology, the uncertainty requirement is less strict than for ac voltage. This makes it suitable for sampling of electrical power up 100 kHz.

Although the voltage buffer has a relatively good response, improvements can still be made, especially with regards to sourcing and fine-tuning the bias for each of the individual transistor. This could be performed by replacing the 1 kΩ resistors from the supply voltages to the bases on the output transistors with potentiometers with for example a 4.7 kΩ maximum resistance. Also, the input resistors on the buffer core could be replaced by a series of a fixed 1 MΩ resistor and a 1 MΩ potentiometer from signal to each supply voltage. It would also be worthwhile to handpick individual transistor units with the least production variance, especially when it comes to gain and base-emitter threshold voltage. Obviously, consistency in the gain of the transistors equalizes the gain for the two voltage polarities, and equal threshold voltage ensures correct voltage level of the feedback.

The voltage dependence on the measured ac division ratio of the voltage divider can be explained in terms of the increased power and hence thermal heating of the resistors. Future voltage dividers can be improved in the range above 10 V by replacing FR4 with a ceramic material such as Al_2O_3 or AlN. This will insure better heat dissipation and less electrical leakage. In addition, components with lower thermal coefficients should be chosen to reduce the resistance alteration caused by the internal heat development.

For a future 100:1 divider, or a second generation 10:1 divider, these two above-mentioned should be introduced, as well as the inclusion of a capacitive, protective guard for the resistive divider elements. The guard has to be carefully constructed, to form the same voltage profile, as that which is intended for the divider, to exclude capacitive leakage from the divider element. This becomes even more crucial for higher division ratios, since the leakage current becomes proportional to the applied voltage, whereas the applied current has to be limited to what the source can produce. The ratio between leakage and applied current must be reduced to avoid uncertainty in the division ratio.

7 Conclusion

A high-precision voltage buffer and a 10:1 resistive voltage divider have been constructed for use in ac voltage and electrical power metrology. The dc gain of the buffer was measured to be 0.999 701 V/V in the range ±1.5 V, varying less than 1 μV/V over the span of 20 days, including reattachment of the buffer into the setup. Absolute gain and ac–dc difference have been measured for the buffer alone, and for the divider and buffer combination, where both agree within 10 μV/V in the overlapping areas, despite both loads and measurement schemes being vastly different. For the ac–dc difference, voltages from 1 V up to 50 V have been characterized using a variety of thermal converters from different producers, with load impedance ranging from 92 Ω to 1 kΩ. The buffer alone was characterized for 1 V, 3 V and 5 V with responses within 40 μV/V for frequencies up to 100 kHz, and less than 100 μV/V for 3 V at 1 MHz. Improvements can be made by manually fine-tuning the biasing points of the individual transistors, manually, using potentiometers. The divider and buffer combination was characterized for 10 V, 30 V and 50 V, all agreeing well within 30 μV/V of each other from 10 Hz to 100 kHz, with a maximum response less than 125 μV/V. This make the voltage divider and buffer combination suitable for sampling of electrical powers up to 50 V and 10 kHz, and even 100 kHz, albeit with a larger uncertainty.

This work has been supported by The Norwegian Research Council through the Public Sector Ph.D. program. We would like to thank Muhammad Nadeem Akram and Kristian Ellingsberg for contributing to this work with valuable discussions on theory.

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Cite this article as: Bjørnar Karlsen, Kåre Lind, Helge Malmbekk, Per Ohlckers, Characterization of high-precision resistive voltage divider and buffer amplifier for ac voltage metrology, Int. J. Metrol. Qual. Eng. **10**, 8 (2019)

Article 2:

Pulsation of InGaAs photodiodes in liquid helium for driving Josephson arrays in AC voltage realization

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IEEE Trans. Appl. Supercond. , Vol. 29, No. 7, Oct. 2019,
DOI: 10.1109/TASC.2019.2901573

Pulsation of InGaAs Photodiodes in Liquid Helium for Driving Josephson Arrays in AC Voltage Realization

Bjørnar Karlsen, Oliver Kieler, Ralf Behr, Thai Anh Tuan Nguyen, Helge Malmbekk, Muhammad Nadeem Akram, and Per Ohlckers

***Abstract*—A commercially available InGaAs p–i–n photodiode chip has been custom packaged and high-speed operated in liquid helium. The photodiode was driven by light pulses using a dc-biased 1310-nm laser, a Mach–Zehnder modulator, and a return-to-zero pulse pattern generator up to 15 GHz clock frequencies, which produced pulse widths down to 77 ps and maximum peak current heights above 10 mA. With the prospect of using this photodiode assembly to operate pulse-driven Josephson junction arrays for ac voltage realization, pulsation modes with constant pulse width and varying pulse density were applied to the diode, which resulted in consistent pulse shapes for bit rates as high as 7.5 Gb/s. This could yield realizable peak voltages as high as 15.525 μV per Josephson junction. Time-lapse pulse measurements were performed over the span of 90 min, which demonstrated good waveform stability. Using the measured current waveforms, the behavior of a typical Josephson junction was simulated according to the Stewart–McCumber model, which resulted in an operational margin of 2 mA for the first Shapiro step.**

***Index Terms*—Cryogenic electronics, high-speed electronics, Josephson arbitrary waveform synthesizer, Josephson voltage standard, optical pulse-drive.**

I. Introduction

TRADITIONALLY, the Josephson effect [1] has been realized by applying a microwave current with dc offset to an array of Josephson junctions. However, since it was demonstrated by Benz and Hamilton [2] that the Josephson effect could be realized by current pulses, this method has become the dominant approach to generate quantum-accurate ac voltage waveforms. This technique uses pulse density modulation with a delta–sigma encoding algorithm to produce any arbitrary voltage waveforms; hence, it is known as the Josephson arbitrary waveform synthesizer (JAWS). A variety of such setups have been constructed, where some have even exceeded the 1 V milestone for frequencies at a few kilohertz [3]–[6]. These systems typically involve driving multiple Josephson arrays simultaneously by directly applying current pulses from a pulse pattern generator (PPG), and coupling the outputs of the arrays in series.

Operating Josephson junction arrays (JJAs) using photodiodes, as current sources, in close proximity can be quite beneficial for a few reasons. First, to remove the coupling noise from the PPG to the arrays by transferring the pulse code from the PPG to an optical code. The optical signal is then applied to a photodiode to generate electrical current pulses for operating the JJA. This approach isolates the PPG electrically from the JJA. Second, the current signals can be generated close to the arrays inside the cryostat, which means that the current pulses face little distortion and damping before reaching the array. Third, this method provides a potentially better way of reducing the required number of PPG channels, in order to realize the Josephson effect in multiple parallel arrays.

For most setups, where the direct electrical pulsation approach has been used, only one JJA was operated per PPG channel. Recent tests at the National Institute of Standards and Technology (NIST) have demonstrated that the signal from one PPG channel can be split to simultaneously drive up to four arrays with margins by using on-chip Wilkinson dividers [6]. However, pulses from a PPG are ac coupled, which makes it necessary to add a low-frequency compensation signal, when synthesizing waveforms of sufficiently large amplitude [7]. Also, when using Wilkinson dividers, a galvanic decoupling is needed by including dc blocks. An alternative future method to reduce the number of channels needed to operate multiple JJAs, and at the same time decrease the complexity in the circuit design, is to use photodiodes and fiber splitters. With this approach, one PPG channel is used to operate a Mach–Zehnder modulator (MZM), and the optical signal can be split to run multiple photodiodes, each of which can drive its own JJA. This operation can be performed without the need to add a compensation signal, hence lower uncertainties can potentially be obtained for ac voltage realization at higher frequencies. It should, however, be mentioned that as described by Zhou *et al.* [8], the net current area of the pulses

Manuscript received July 6, 2018; revised December 19, 2018; accepted February 5, 2019. Date of publication March 27, 2019; date of current version April 22, 2019. This work was supported in part by JRP QuADC and in part by the Norwegian Research Council via the Program Public Sector Ph.D. The QuADC project has received funding from the EMPIR program co-financed by Participating States and from European Union's Horizon 2020 research and innovation program. This paper was recommended by Associate Editor M. Noe. *(Corresponding author: Bjørnar Karlsen.)*

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Digital Object Identifier 10.1109/TASC.2019.2901573

still make an inductive contribution in the JJA, which must be considered in an ac voltage realization. An added benefit is that the optical pulses can be transferred back to electrical pulses close to the JJA, and thus face less distortion between source and array.

With the prospect of having an optically operated JAWS system, a prototype photodiode package has previously been developed and tested for viability and dc operation at 4 K by Bardalen *et al.* [9], [10]. This assembly must be able to generate current pulses that have a large enough peak to cover the entire first Shapiro step, and short enough duration to allow for a high pulsation bit rate.

This article is organized as follows: basic theory and operating regime are discussed in Section II, the photodiode assembly procedure is described in Section III, the experimental setup is described in Sections IV and V, the measured results are presented and discussed in Section VI, and simulation results of a typical Josephson junction are discussed in Section VII.

II. Pulse-Driven Josephson Arrays

When biasing a Josephson junction with current pulses, an instantaneous voltage develops across the junction that comes from the magnetic flux quanta tunneling through it. Consequently, the average voltage becomes proportional to the pulsation bit rate

$$V = n\frac{h}{2e}f_b \tag{1}$$

where n is the quantized Shapiro step, h is Plank's constant, e is the elementary charge, and f_b is pulse bit rate at which the junction is biased. The two values in this equation that are tunable are n and f_b. However, JAWS systems are typically run at the first Shapiro step ($n = 1$), so the only parameter that is tunable in practice is the pulsation bit rate. According to Benz and Hamilton [2], the maximum allowable pulse rate is half of the inverse full width at half maximum (FWHM) of the pulse.

It must be made sure that the pulse peak height is large enough to operate the JJA over the entire first Shapiro step. This is to make sure that a wide plateau of constant voltage can be maintained over time. An indication of this can be simulated using the resistive-capacitive-Josephson model, also known as the Stewart–McCumber model [11], [12]

$$\beta\frac{d^2\phi}{d\tau^2} + \frac{d\phi}{d\tau} + sin\phi = i\left(\frac{\tau}{2\pi f_c}\right) \tag{2}$$

where $i(t) = \frac{I(t)}{I_c}$, $f_c = \frac{2e}{h}I_cR$, $\beta = 2\pi f_cRC$, and $\tau = 2\pi f_ct$. R and C are the parasitic parallel resistance and capacitance, respectively, of the Josephson junction, I_c is the critical current of the junction, f_c is the characteristic frequency, and ϕ is the phase evolution of the superconducting waveforms traveling through the junction. For overdamped junctions, it is appropriate to simplify the expression by setting $\beta = 0$. Using this model for Gaussian-shaped current pulses, Williams *et al.* [13] arrived at two approximate theoretical limits for traversing Shapiro steps

$$A_1 \approx \frac{I_c}{f_c} \tag{3}$$

is the pulse area covering the width of any one entire Shapiro step, and

$$A_2 \approx \left(\frac{f_c}{f} + \frac{1}{2}\right)\frac{I_c}{f_c} \tag{4}$$

is the pulse area required to reach the first step, where f is the inverse FWHM time of the pulse. These theoretical approximations would suggest that the transition from one step to the next is without transients. However, in real arrays with many hundreds and even thousands of junctions in series, the transients between the quantized levels are more gradual. For this reason, it must be guaranteed that the applied pulses can cover the entire first Shapiro step in order to ensure proper operation of the JJA. Therefore, the minimum pulse area A_p needed is the sum of A_1 and A_2

$$A_p \approx \frac{I_p}{f} \geq A_1 + A_2 \approx \left(\frac{f_c}{f} + \frac{3}{2}\right)\frac{I_c}{f_c} \tag{5}$$

where I_p is the pulse peak height. By rearranging this expression, the minimum current peak pulse requirement per pulse width for operating a JJA at a given pulsewidth is given by

$$\frac{I_p}{I_c} \geq \frac{3}{2}\frac{f}{f_c} + 1. \tag{6}$$

This expression can also be rearranged to select which JJAs that the photodiode can properly operate at a given pulsewidth

$$\frac{I_c}{I_p} \leq \frac{2(f_c/f)}{3 + 2(f_c/f)}. \tag{7}$$

As stated by Williams *et al.* [13], (3) and (4) are only validated for Gaussian-shaped pulses, although most pulse shapes should be applicable. It must also be stressed that the first approximation made in (5) assumes that the pulse area can be written as the product of peak height and FWHM. Fig. 1 depicts these two limits of (6) and (7) as the relative relation between pulse shape and the characteristic parameters of the JJA. The graph on the top of Fig. 1 implies that the pulses applied to the array must be such that, relative to I_c and f_c, the pulsation must be above the red line. For example, if a JJA with $I_c = 1$ mA and $f_c = 10$ GHz is used for pulses of FWHM $= 100$ ps, the minimum required peak pulse height to cover the first Shapiro step is 2.5 mA. On the other hand, the graph on the bottom of Fig. 1 can be used to select a suitable JJA for a given pulse operation. Given a peak pulse height and width, only a certain set of JJAs exist, for which the entire first Shapiro step can be covered. For proper pulsation, an array below the graph must be chosen. For example, if pulses at 10-mA peak pulse height and 100 ps FWHM are used, then only arrays with $f_c = 20$ GHz can be used to cover the entire first Shapiro step if $I_c \leq 2.5$ mA.

III. Photodiode Assembly

The chip InGaAs p–i–n photodiode (Albis PD20X1) [14] used in this experiment has been flip-chip-bonded onto a silicon-based chip-carrier with superconductive niobium tracks. This carrier has been developed by a collaboration between the National Physical Laboratory (NPL), Physikalisch-Technische Bundesanstalt (PTB), and Justervesenet (JV) [15]. The carrier

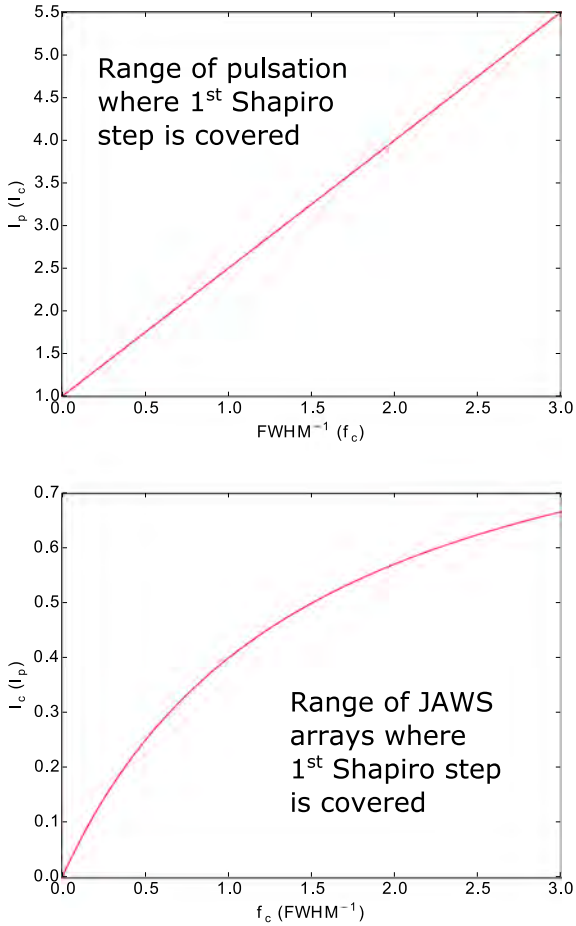

Fig. 1. Top: Minimum current pulse peak to cover the entire first Shapiro step according to (6). For a given JJA, the maximum available current peak height must be above the red line for the applied pulse width. Bottom: Maximum relation between I_c and f_c in (7) that a JJA can have where the first Shapiro step is covered for a given pulse shape in terms of peak height and FWHM.

has been glued and wire bonded to a circuit board made out of RO3006 material from Rogers Corp. with SubMiniature version A (SMA) connectors at the end of the board. A borosilicate glass sleeve with an inner diameter of 1.818 mm was glued to the carrier according to alignment markings on the carrier itself. A ferrule-ended fiber, with a diameter of 1.8 mm, was placed inside this sleeve for illumination of the photodiode. A close-up image of the photodiode inside the sleeve is shown to the left in Fig. 2. A schematic representation of the chip carrier with photodiode is depicted to the right in Fig. 2.

The crucial issues surrounding these samples are the mechanical stress between the chip-carrier and the sleeve surrounding the photodiode, and the focus of the laser beam onto the photodiode. Therefore, we have worked on these issues, and the results were published in [9] and [10]. In [9], simulations were performed in COMSOL, which suggested that air gaps as large as 100 μm will only cause a loss of less than 1 dB for a misalignment of up to 45 μm. For an air gap of 400 μm, a misalignment of up to 30 μm will cause a loss of less than 1 dB. Attaching the fiber in such a way that the ferrule-end gently pushes against the photodiode, will leave a smaller gap, and therefore, a larger misalignment is permissible. Stress and thermal cycling are discussed in [10], where the justification is given for the materials

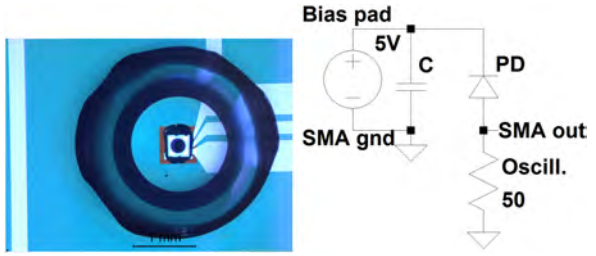

Fig. 2. Left: Close-up picture of the photodiode through the glass sleeve. The photodiode is the lensed bottom-illuminated version of the PD20X1 from Albis. Right: Schematic representation of the chip carrier with photodiode. The diode is loaded by a 50-Ω oscilloscope.

used in the mounting process. The same publication reports that after ten immersions into liquid nitrogen no sign of failure was seen in the samples; however, a few photodiodes have broken in liquid helium. Therefore, the measurement equipment must be protected so that it will not be destroyed by a reverse bias if the photodiode short circuits.

For this experiment, two samples were tested with a reverse bias of 5 V. The sample that has been used for most of the measurements is named #197L (this was the sample that was used unless noted otherwise), and the other one is named #204L.

IV. Cryoprobe Setup

A cryoprobe has been modified to take a single-mode optical fiber with an FC/PC connector as input, and a coaxial cable with SMA connectors as output. The optical input was connected to a single-mode FC/PC to ferrule (1.8-mm diameter) fiber on the inside of the cryoprobe tube. The photodiode was illuminated through the glass sleeve from the ferrule end of the fiber, and the FC/PC end was inserted into a mating sleeve that was fixed through the wall of the head of the cryoprobe. The sample itself was attached to the bottom of the cryoprobe using a semirigid coaxial cable with SMA connectors that runs through the tube and up to the head of the probe. A shield was fixed to the bottom of the probe to protect the sample from mechanical damage while being inserted into and removed from the liquid helium dewar. Thin copper leads were used for the electrical biasing of the photodiode. The negative bias lead was soldered to the outer conductor of the SMA connector, and the positive lead was soldered to a pad that is connected directly to the cathode of the diode. The output signal was measured via the coaxial cable. The attachment of the photodiode sample to the cryoprobe bottom is shown in Fig. 3.

V. Instrumental Setup

The photodiode sample was tested using optical signals with varying pulse width, pulse height, and pulse repetition frequency. The pulse codes were first generated electrically by a PPG (Sympuls Aachen BPG 30G - TER $\times$ 8). These signals were amplified by a modulator driver (iXblue DR-DG20-MO), and then applied to a MZM (iXblue MX1300-LN-20). The modulator was used to convert a high-power continuous-wave Fabry–Perot laser (Thorlabs FPL1053, 1310-nm wavelength)

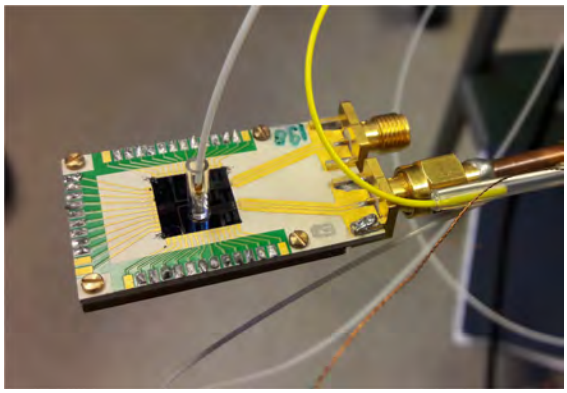

Fig. 3. Picture of the photodiode sample attached to the bottom of the cryoprobe. The ferrule end of the optical fiber is inserted into the glass sleeve to make contact with the photodiode on the inside (see left-hand side of Fig. 2). The sample is fixed to the cryoprobe via the SMA connector on the semirigid coaxial cable. Thin copper leads were soldered to pads to apply a reverse electrical bias to the photodiode.

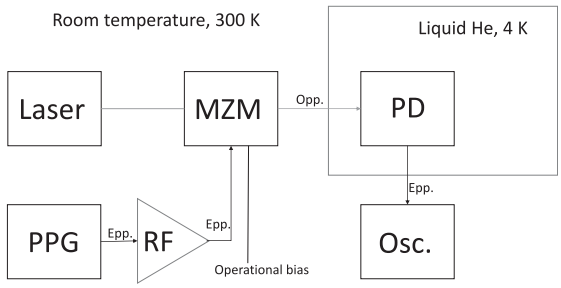

Fig. 4. Schematic representation of the photodiode pulsation setup. In the schematic, Epp. and Opp. represent the electrical pulse pattern and optical pulse pattern, respectively. PPG is the pulse pattern generator, MZM is the Mach–Zehnder modulator, RF is an RF amplifier (or modulator driver), PD is the photodiode sample, and Osc. is the high-speed oscilloscope.

beam into laser pulse codes equivalent those generated by the PPG. These optical signals were then applied to the photodiode, and the resulting photocurrent pulses were measured via the SMA cable using a 50-Ω sampling system. The sampling system had 50 GHz bandwidth and consisted of a digital serial analyzer (Tektronix DSA8200) and a time domain reflectometry (TDR) sampling module (Tektronix 80E10). A schematic of the entire setup is shown in Fig. 4.

Although 1550-nm laser technology is more developed and commercially available, a wavelength of 1310 nm was chosen for this setup. This was due to the increase of the energy bandgap in InGaAs as its temperature approaches 4.2 K. According to the formulas in Paul *et al.* [16], the bandgap of standard InGaAs becomes 0.82 eV at 4.2 K. The photon energy of a 1550 nm laser is 0.80 eV, so it will be unable to excite charge carriers in InGaAs at this temperature. Therefore, a 1310-nm laser was used, which has a photon energy of 0.95 eV that is more than sufficient to excite charge carriers.

A binary operated (the PPG is ternary, but "−1" is never used) return-to-zero PPG was used in this experiment, where a pulse is emitted for every bit that has been set to "1." This also means that the FWHM of the pulses are half the period of the clock frequency. The PPG was a limiting factor in extracting the

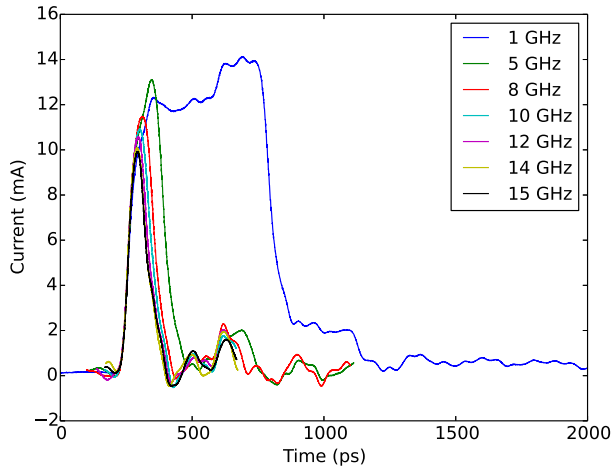

Fig. 5. Plot of single bit pattern waveforms for a few selected clock frequencies.

highest performance from the photodiodes themselves in terms of pulse density. The rise/fall times (20%–80%) of the PPG is specified to be as high as 20 ps. Assuming this number with linearly shaped bit transients, the full rise/fall times (0%–100%) becomes 20 ps/(0.8–0.2) = 33.3 ps. Adding the rise and fall times together the total time that goes to transients in one pulse (i.e. 0%–100%– 0%) becomes 66.6 ps. This yields a theoretical maximum bit rate of 15.0 Gb/s, which corresponds to the PPG's maximum clock frequency with a full bit-register set to "1."

One can expect that the modulator driver also causes some limitation in the optical pulse generation. In its test report for this modulator driver, the characterization of it was performed using a reference signal from a PPG operated at 20 Gb/s and 0.45 V_{pp}, with rise/fall times of 8.53/8.27 ps (10%–90%). The resulting output signal from the driver was 6.07 V_{pp} with rise/fall times of 13.20/13.60 ps (10%–90%). Since these values were calibrated using a considerably faster PPG, one cannot expect that the rise/fall times will be less than 25 ps (20%–80%) for the PPG used in this experiment. Following the exercise in the previous paragraph, the total transient time for one pulse becomes 2*25 ps/(0.8 − 0.2) = 83 ps, which corresponds to a theoretical maximum bit rate of 12.0 Gb/s in this setup.

Unfortunately, no information about the rise/fall times of the MZM is given in the calibration sheet. However, it can be expected that it will further decrease the maximum operational frequency of this system. Thus, it is reasonable to assume that an absolute maximum bit rate of the system cannot be greater than 12 Gb/s due to the rise/fall times.

VI. Results and Discussion

The pulse response has been tested using the PPG's entire clock frequency span of 1–15 GHz. The modulator driver and modulator were tuned to provide the maximum signal for one bit set to "1" in the 16-bit register at each frequency. The output pulse waveforms for a few selected frequencies are presented in Fig. 5, and the amplitude and FWHM for all frequencies are presented in Fig. 6, together with the electrical signal measured directly from the PPG as a comparison. For all frequencies, the

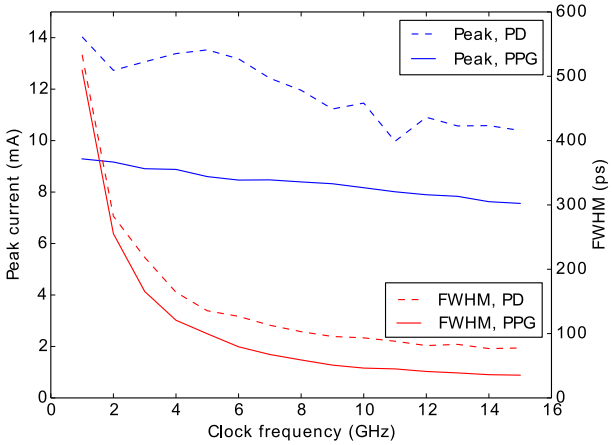

Fig. 6. Current pulse peak (blue) and FWHM (red) of single-bit patterns for all frequencies, both for the photodiode (labeled PD, dashed lines) and the signal taken directly from the PPG (solid lines).

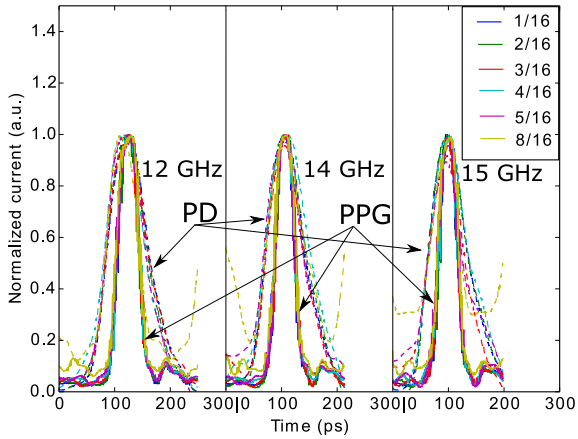

Fig. 7. Plot of overlapping waveforms for different pulse densities, which have been grouped together according to clock frequency, as depicted on the graph. The label PPG denotes the signal directly from the PPG, and PD denotes the signal from the photodiode. The *y*-axis has been normalized by the maximum current peak height. The legend refers to how many bits that are set to "1" in the 16-bit register. For example. "4/16" means that 4 out of the 16 bits are set to "1," and the rest are set to "0." The solid and the dashed lines represent the measurements of the PPG and the photodiode, respectively.

peak current height from the photodiode was more than 10 mA, and a FWHM down to 77 ps was reached. Thus, pulses larger than 770 fAs can always be generated.

In Figs. 5 and 6, it can be seen that the peak from the photodiode varied within 1 mA in the clock frequency range of 1–5 GHz with the FWHM being half of the inverse clock period. Above 5 GHz, however, the peak height began to decline. This was because the full rise time was longer than the bit's allocated time slot. Relative to 1 GHz, the amplitude at 15 GHz is at -3 dB. This was a lowering of the bandwidth of the photodiode sample, which the data sheet states is typically 20 GHz [14]. This discrepancy can be attributed to additional parasitic components in the surrounding sample circuitry, such as the solder joints and wire bonds.

When operating a JJA for ac voltage realization, the pulse density varies greatly throughout the code. In order to generate high-quality waveforms, the pulses from the photodiode must be independent of pulse density. In other words, the produced pulses must be the same regardless of the distance between two successive pulses. To investigate this, the photodiode was pulsed with codes where the 1, 2, 3, 4, 5, and 8 bits were set to "1," and spread as uniformly as possible in the register. This was done for a select number of clock frequencies, 1, 5, 8, 10, 12, 14, and 15 GHz, and the data (dashed lines) from the three highest frequencies are shown in Fig. 7 together with the signal directly from the PPG (solid lines).

It can be seen in Fig. 7 that the photodiode produced much less electrical noise than the signal directly from the PPG. The obvious benefit of this is a better control over the frequency spectrum that is applied to the Josephson array. This excludes higher-order distortions of the realized output waveform, and hence larger operational margins can be obtained. Furthermore, since the pulses from the photodiode will be used to operate the JJA in closer proximity compared to the oscilloscope used in this experiment, even less noise will interfere with the array. A second advantage to using the photodiode is that the input cable used in the direct electrical operation of the Josephson arrays is replaced with an optical fiber. This removes the crosstalk that else would have occurred between the input electrical pulses through the cable and the output leads for the quantized waveforms.

The pulses in Fig. 7 have more or less the same shape considering the photodiode and the PPG signals separately. The photodiode can be irradiated with laser pulse codes with pulse density up to 8/16, and the PPG can be used to produce pulse densities even higher than this. When coupling these photodiodes to a JJA for realizing ac waveforms, codes can be used to generate a peak voltage of 15.525 μV per junction according to $f_b = 7.5$ Gb/s in (1). Pulses directly from the PPG can be used to realize even higher voltages, potentially up to 31.05 μV per junction for $f_b = 15$ Gb/s.

When considering the ability of the pulses to produce clearly quantized flux transfers in the Josephson junctions, they should fall relatively quickly to a stable "0." Looking at (2) for $\beta = 0$ and $i = 0$, ϕ will take some time to settle at a quantized $2\pi n$. Following Fig. 7, this is something that the pulses from the PPG manage better than the photodiode in this setup.

Measurements of the full 16/16 bit pattern have also been performed; however, above a few gigahertz clock frequency, the pulses started having problems settling to 0 mA after each pulse. This issue has already been alluded to previously in this paper, and it is due to the increase in rise/fall times of the laser-pulse-delivery system is too long to properly realize an optical bit rate approaching 15 Gb/s. Fig. 8 shows the output waveform for a 15 Gb/s signal from the photodiode. It is pointless to compare the waveforms for the 16/16 bit pattern to those of the lower densities since this signal is more similar to a sine wave than a pulse train. This signal can still be used to realize dc quantum voltages, but the critical current of the Josephson array that is used must be greater than the current waveform trough, so that the phase settles after each pulse. For 15 Gb/s, 31.05 μV can be realized per junction.

To verify the repeatability and reproducibility of the signals, the following measurements were also performed. A measurement of the 1/16 bit-patterns for the clock frequencies 1, 5, 8,

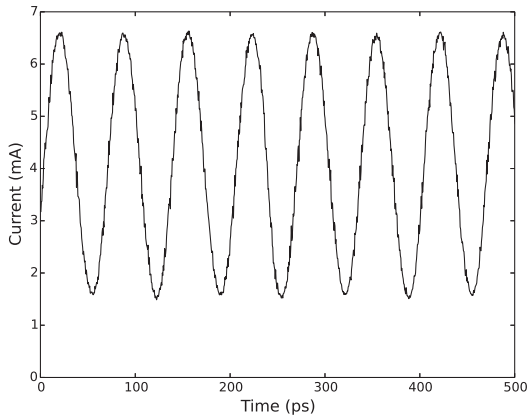

Fig. 8. Plot the output waveform from the photodiode when being irradiated with 15 Gb/s laser pulses.

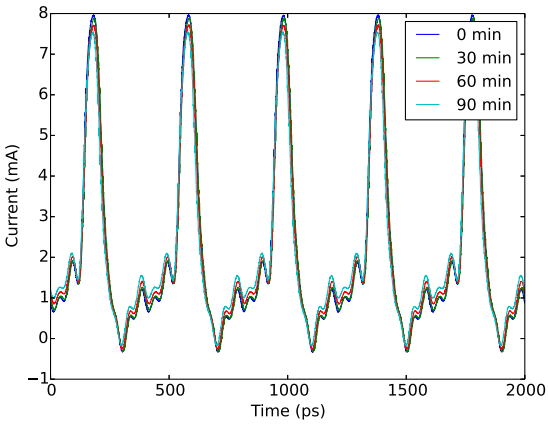

Fig. 10. Time-lapse of the 4/16 bit pattern at 10 GHz clock frequency. Each successive series is taken 30 min apart. The labels indicate the time that has passed since the first measurement.

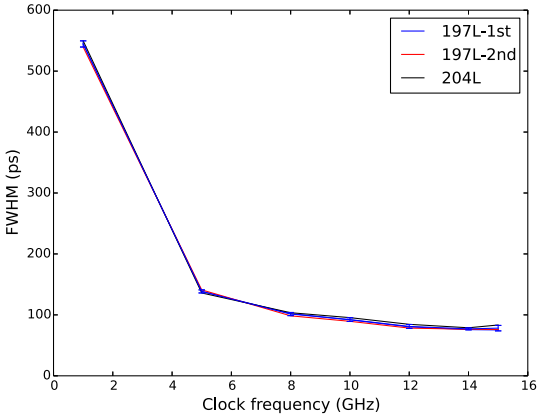

Fig. 9. FWHM plot for 1/16 pulse pattern for samples #197L (the first measurement is labeled "197L-1st" and the second is labeled "197L-2nd") and #204L at the selected clock frequencies 1, 5, 8, 10, 12, 14, and 15 GHz. The relative standard deviation is less than 6% for all clock frequencies in this ensemble of measurements.

10, 12, 14, and 15 GHz was repeated for sample #197L, and then reproduced using sample #204L. The FWHM of the first and second measurements for #197L and #204L are presented in Fig. 9 along with the empirical standard deviation, which was calculated for each frequency in the three series. Between the first and second #197L series, the sample was immersed into liquid helium tens of times, and the bias leads reattached and resoldered. Obviously, #204L is a different sample and has, prior to these measurements, only been mechanically tested in liquid nitrogen. Despite all of these differences, the relative deviation for all of these series combined is below 6% for all frequencies.

Finally, the long-term operational stability was tested for sample #197L. The 4/16 bit code at 10 GHz clock frequency, effectively 2.5 Gb/s, was applied to the sample during the span of 90 min. Throughout this time span, no parameters were adjusted, and 13 data series were extracted. The measurements presented in Fig. 10 show the waveforms separated by 30 min. A small drift can clearly be seen. The drift goes downward for the pulse peak and upward for the signal floor. Such a drift may indicate that the modulation is out of phase, that is, the delay in the modulated path inside the MZM does not remain at exactly π radians between the pulses during the time it is used. The phase delay probably decreases a little from π radians, since the destructive interference is not complete between the pulses, and the peak is decreased. In other words, the drift is caused by the modulator and not by the photodiode, and it can be counteracted by continuously adjusting the bias voltage of the modulator. Using the pulsation rate of 2.5 Gb/s, voltages of 5.175 μV can be realized over each junction in the array at first Shapiro step.

VII. Selection and Simulation of a Josephson Array

Numerical simulations have been performed according to (2). The actual time-lapse measurements of the current signal from the photodiode, presented in Fig. 10, were used as the basis for these simulations. Here $\beta = 0$, which is appropriate for overdamped junctions, and the time steps were limited by the time resolution of the data series. The time evolution of ϕ was solved by the forward Euler method using $\phi(\tau = 0) = 0$ as initial condition, where $d\phi/d\tau$ was calculated by rearranging (2). From this, the obtained Shapiro step was evaluated by the final phase after the pulse as $n = \phi_{\text{final}}/2\pi$.

Equations (6) and (7) can be used to choose an appropriate JJA for the pulses that are produced by the photodiode, given that they are more or less Gaussian-shaped. Using metal-like NbSi barriers for the Josephson junctions [17], [18], a wide selection of JJAs can be manufactured, ranging in $I_c \in [0.25, 5]$ mA and $f_c \in [5, 15]$ GHz, so that any conceivable array within these limits can be expected to represent realistic arrays. As stated previously, an array that is appropriate for a JAWS system is one where the entire first Shapiro step can be covered by the maximum extractable pulse height from the photodiodes. This means that the array chosen must be one where the full current pulse height is able to reach the second step. Then, in an actual ac voltage realization, the optical power applied to the photodiodes can be reduced to remain on the first step.

For a stable pulsation signal, with maximum peak pulse height of 7.5–8 mA and FWHM of 75–81 ps, a selection of JJAs can be used. According to (6) and (7), an array with $f_c = 10$ GHz and with a corresponding theoretical maximum $I_c = 2.5$ mA is just inside the limit that can be used where the entire first Shapiro step is covered. Again, this is for shapes such as Gaussian pulses,

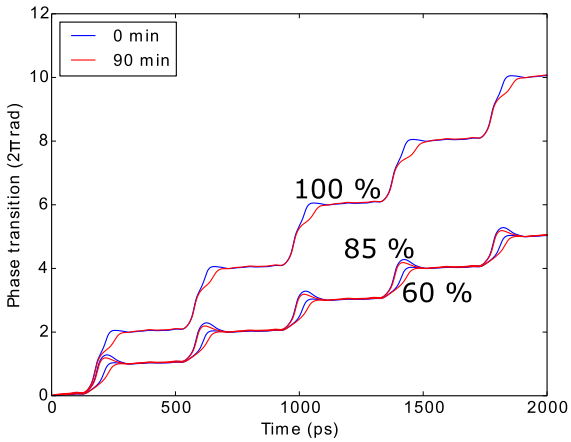

Fig. 11. Simulation of phase transients based on the first and last data series of the time span of the 4/16 bit pattern at 10 GHz clock frequency presented in Fig 10. The label "100%" represents the unscaled pulsation current, and labels "85%" and "60%" represent the waveforms scaled down to 85% and 60%, respectively.

where the rise and fall is sharp, and the pulse area can be approximated by the product of peak height and FWHM. In this case, the signal floor rises prior to the pulse, so the pulse area is slightly larger, and therefore, a larger I_c can theoretically be used. To verify these claims, simulations of the phase evolution has been performed according to the Stewart–McCumber model based on the current data from the photodiode in the time-lapse. A JJA with $f_c = 10$ GHz and $I_c = 2.9$ mA turned out to produce two flux quanta. The results are shown in Fig. 11 for the full height of the waveform, and for the data scaled down to 85% and 60% for the first and the last data series. The 100% series shows that the pulsation measured in the entire time span is sufficient to transfer two flux quanta for each pulse. In other words, reaching the second Shapiro step is possible, which means that the entire first Shapiro step is completely covered. For the 85% and 60% series, one flux quantum is transferred for each pulse, and they represent the outer points of the current peaks that will reach first Shapiro step in each pulse for the entire duration of the time span. This means that the theoretical operating margin for this JJA using this pulsation regime is at 85–60% = 25% of the maximum current, or an operating margin in the peak height of about 2 mA.

VIII. Conclusion

A commercially available InGaAs p–i–n photodiode has been custom packaged to operate Josephson arrays in liquid helium. The 1/16 laser bit pattern has been applied to the photodiode for clock frequencies up 15 GHz, where the amplitude has been measured to be more than 10 mA for the entire frequency range with FWHM down to 77 ps. Thus, even for the highest frequencies, pulse areas greater than 770 fAs can be produced.

Patterns of varying pulse density have been tested to transduce codes up to 8/16 bit for up to 15 GHz clock frequency. This means that codes with instantaneous bit rates as high as 7.5 Gb/s can be applied in a JAWS system using this photodiode as pulsation source for the JJA, yielding realizable voltage peaks as high as 15.525 μV per junction. The full 16/16 bit pattern has also been tested, yielding bit rates as high as 15 Gb/s. However, the pulses do not fall quickly enough to 0 mA between each new bit for the highest frequencies. This pattern can still be used to realize quantized dc voltages as high as 31.05 μV per junction.

The 1/16 bit pattern has been repeated for sample #197L and reproduced for sample #204L for a selection of clock frequencies from 1 to 15 GHz, resulting in relative standard deviations of less than 6% for every frequency in the combination of these three series.

The long-term stability was investigated over a 90 min interval for the 4/16 bit pattern at 10 GHz clock frequency, with no visible change in the waveform other than the drift in the required modulator bias. The measured data from the initial and final data series of this time span were used to perform simulations of the phase evolution of a selected typical JJA, where the operational margin for the first Shapiro step was found to be 2 mA.

Acknowledgment

The authors would like to thank Eivind Bardalen for helpful guidance in the construction of the samples and Luis Palafox for helpful discussions.

The authors also thank the Department of Electrical Quantum Metrology at PTB for providing both facilities and guidance for the measurements. The authors especially thank Luis Palafox for helpful discussions.

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Article 3:
A Bipolar Photodiode Module for Pulse-Driven Josephson Arrays in Liquid Helium
B. Karlsen, E. Bardalen, J. Nissilä, O. Kieler, L. Palafox, R. Behr, H. Malmbekk, M. N. Akram, and P. Ohlckers
Submitted to IEEE Trans. Instrum. Meas.

Excluded from online edition due to publisher's regulations

Article 4:
Packaging and Demonstration of Optical-Fiber-Coupled Photodiode Array for Operation at 4 K
E. Bardalen, B. Karlsen, H. Malmbekk, O. Kieler, M. N. Akram, and P. Ohlckers
IEEE Trans. Compon. Packag. Manuf. Technol., Vol. 7, No. 9, Sept. 2017, pp. 1395-1401

Excluded from online edition due to publisher's regulations

Article 5:

Reliability study of fiber-coupled photodiode module for operation at 4 K

E. Bardalen, B. Karlsen, H. Malmbekk, M. N. Akram, and P. Ohlckers

Microelectronics Reliability, Vol. 81, 2018, pp. 362-367

Microelectronics Reliability xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Reliability study of fiber-coupled photodiode module for operation at 4 K

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ARTICLE INFO

Keywords:
Optoelectronic packaging
Cryogenics
Voltage standards

ABSTRACT

The reliability of a photodiode module intended for operation at 4 K was investigated. Flip-chip bonded photodiodes and an adhesively bonded optical fiber attachment structure were considered. Finite element simulations of the thermomechanical stress were used to evaluate the stresses in different design configurations. Results showed that issues with chip cracking in silicon were eliminated by proper selection of component materials. Photodiode modules survived thermal cycling to 77 K and extended operation in 4 K.

1. Introduction

Since 1990, the SI volt has been defined by the Josephson effect, a superconducting phenomenon which enables the generation of precise voltages steps by exciting Josephson junction arrays (JJA) with a microwave frequency f [3]. The output voltage is traceable to elementary physical constants:

$$V = Nn\frac{h}{2e}f, \quad (1)$$

where n is the Shapiro step number, N is the number of Josephson's junctions in series, h is Planck's constant and e is the electron charge. The JJA is typically operated at 4 K, using niobium (Nb) as the superconducting material.

Today, a significant effort is put into developing techniques for synthesizing alternating and arbitrary voltage waveforms based on the Josephson effect. The Josephson Arbitrary Waveform Synthesizer (JAWS) [6] is based on utilizing a digital pulse train generated by a pulse pattern generator (PPG) with a variable repetition frequency f, rather than a constant microwave signal. Recently, voltages up to 1–2 V at frequencies up to several kHz has been demonstrated [7] [8]. This is achieved by arranging two or more JJAs on a single chip, and operating multiple chip in parallel.

Replacing the direct electrical link to the JJA with optically controlled high-speed photodiodes may have several advantages, such as reduced electrical loss and insensitivity to electromagnetic interference. Instead, the PPG is used to modulate a laser source which is connected with an optical fiber to a photodiode, and is therefore electrically isolated from the JJA. This approach has previously been demonstrated [9,10].

By designing a photodiode module from scratch, utilizing commercial components, it is possible to make the module compatible with the JJA integrated chip. In particular, by locating a photodiode module in the cryogenic chamber, multiple photodiodes channels may be connected directly to the JJA chip through wire bonds, eliminating the need for high-speed coaxial cables inside the Helium Dewar.

Such a module must have compact size and tolerate thermal stress due to cooling down to 4 K, as well as handling stresses. Careful consideration of materials and component selection is needed in order to keep thermal stresses below critical values. In its lifetime, the device is expected to have stable performance at 4 K in intervals of up to several hours, as well as being able to survive 10s of thermal cycles between room temperature and 4 K.

In microelectronic packaging cycled to cryogenic temperatures, issues such as wire bond failure, chip cracking [2,11] and have been reported.

In general, design parameters such as layer thicknesses and mechanical properties of adhesives and components should be optimized to reduce the thermal stresses. For flip-chip bonded dies on organic substrates, it has been shown that the die-substrate thickness ratio should be reduced in order to reduce the maximum tensile stress on the die [12] [13].

In the following, we investigate the long-term reliability of a proposed photodiode module structure. Finite element modelling (FEM) is used to assess the mechanical stress caused by an adhesive fiber attachment technique. The long-term reliability of the assembly was assessed using thermal cycling tests between room temperature and 4 K.

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https://doi.org/10.1016/j.microrel.2017.10.034
Received 7 September 2017; Accepted 28 October 2017

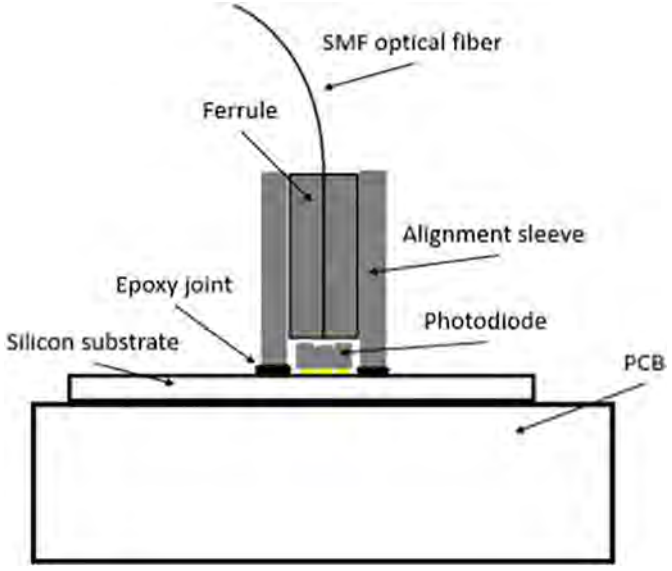

Fig. 1. Cross section view of assembly structure concept. The module consists of several layers, including PCB, silicon substrate, optical fiber alignment sleeves and flip-chip bonded photodiodes.

2. Device description and modelling

2.1. Device structure

The basic assembly structure is shown in Fig. 1. Silicon substrates with Niobium coplanar waveguides (CPW) and conducting lines were fabricated, providing electrical connection between photodiodes and the JJA, as well as for external biasing. A pair of commercial lensed photodiodes, Albis PDCS24, is flip-chip bonded onto AuPd pads. The photodiodes is illuminated from above by an optical fiber terminated by a ferrule. Alignment sleeves are adhesively bonded directly to the silicon substrate, into which the ferrule is inserted. The silicon substrate is then adhesively bonded to a Printed Circuit Board (PCB).

2.2. Photodiode bonding

We have previously demonstrated photodiode bonding using Au stud bumps [14]. However, the use of stud bumps require high ball uniformity and small size in order to reduce the risk of short circuiting due to ball deformation in the bonding process.

In order to resolve this issue, an alternative bonding technique is tested here by using a 4 µm thick AuSn solder bump deposited on the photodiode pads by the manufacturer. The bonding process was done by heating at 250 °C with 1 N force for 30 s, followed by heating to 300 °C for 15 s without applying force. The photodiodes were then underfilled by epoxy, as shown in Fig. 2 (a). Such underfill may improve lifetime by reducing stress concentrations [15], which is a particular concern for solders that become brittle at cryogenic temperatures.

2.3. Optical fiber assembly

Two types of optical fiber ferrules/alignment sleeves were tested: Ceramic (zirconia) ferrules (Thorlabs part no: ADAF1) with 3.2 mm outer diameter and borosilicate glass sleeves (Thorlabs part no: 51-2800-1800) with 2.8 mm outer diameter. Both sleeves have sufficiently small size to allow bonding of multiple components on a small space.

The positioning of the alignment sleeves is done manually using a microscope to measure the offset between the photodiode and center of the sleeve. Epoxy is then applied around the edges and under the alignment sleeves for permanent bonding, as shown in Fig. 1 (b).

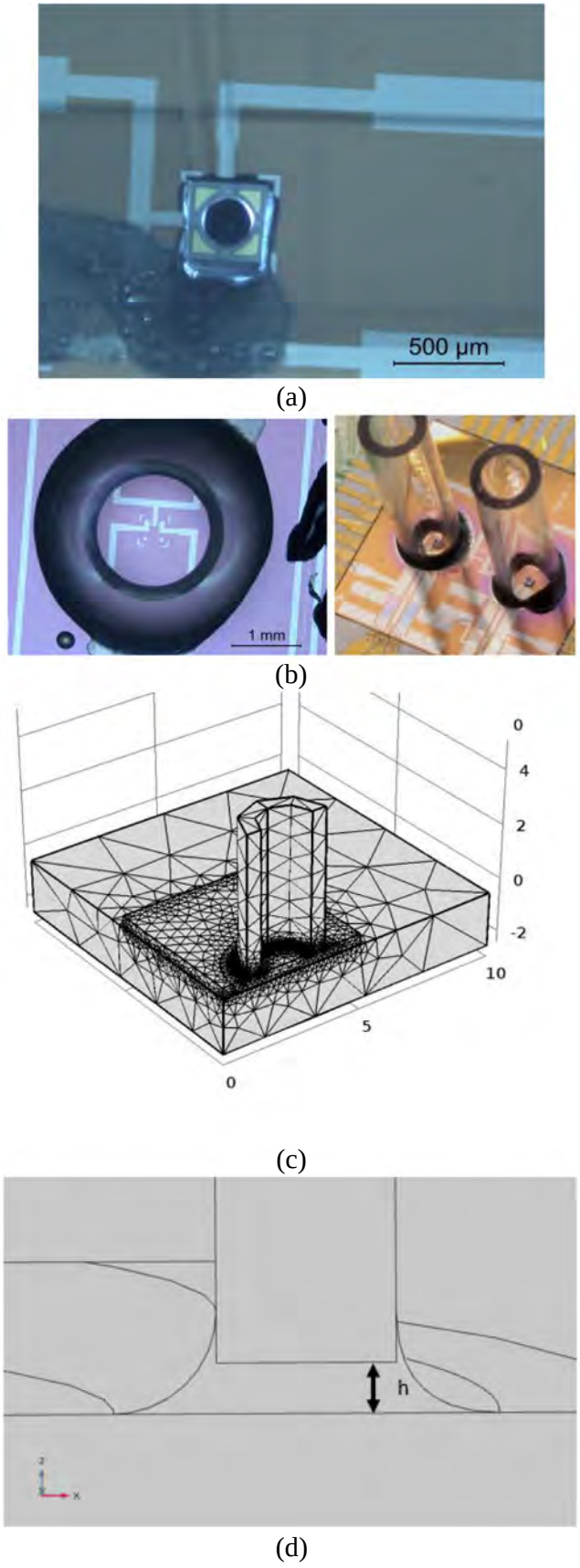

Fig. 2. (a) Underfilled and bonded photodiode. (b) Left: Top view of glass alignment sleeve after adhesive bonding. Right: Pair of bonded glass sleeves on silicon substrate, with bonded photodiodes. (c) Finite element model with dimensions are in mm. (d) Close-up of the epoxy joint model, showing parameter h, the sleeve-substrate-gap.

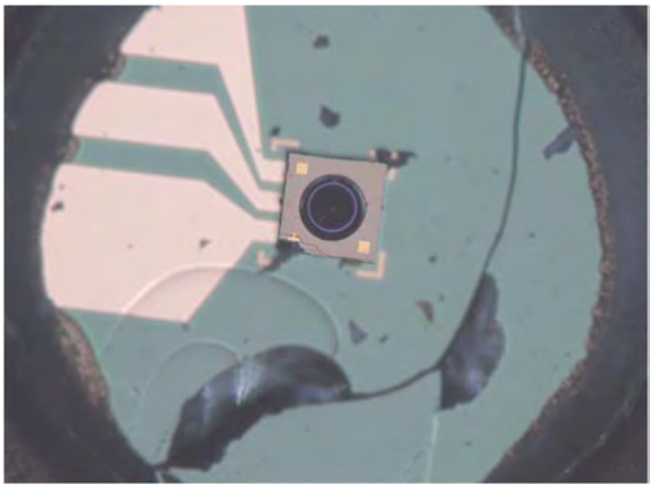

Fig. 3. Microscope image showing cracking in silicon substrate after cooling down to 4 K.

The substrate was then glued and wirebonded to a sample holder/PCB. The curing schedule for the epoxy consisted of 24 h gelling at room temperature, then 3 h of curing at 80 °C. The role of the PCB is to provide the electrical connections between the photodiode module and external equipment, and in the future, between the optical module and the JAWS array.

3. Finite element modelling

In initial tests, using zirconia alignment sleeves and FR2 PCBs, cracking in the silicon substrate was observed after cooling with liquid Helium. Fig. 3 shows one example of such cracking. No adhesive failure, such as delamination or cohesive failure was found. In order to investigate this issue, a thermomechanical FEM study was performed.

3.1. Model details

A 3D model of the circuit board, adhesive layers, silicon die and the optical fiber attachment structure is built in COMSOL. In order to avoid unrealistic stress singularities, the epoxy joint is modelled with fillets near the edges, as seen in Fig. 2 (d). Taking advantage of the symmetry of the structure, only a quarter of the structure is simulated, with symmetry conditions on the cut planes.

In the simulations, several design parameters were varied to determine the effect the following design configurations and parameters:

1) Thickness of the PCB board, d.
2) Elastic modulus, E, and coefficient of thermal expansion at 300 K, $\alpha = \frac{1}{L}dL/dT$, of the PCB.
3) The substrate-sleeve standoff h.
4) Alignment sleeve type
   - o 3.2 mm Zirconia sleeve
   - o 2.8 mm Borosilicate sleeve
5) Epoxy type
   - o Stycast 1266
   - o Masterbond EP29LPSPAO-1 BLACK

3.2. Material properties

As the assembly is subjected to a large temperature span, from room temperature to 4 K, the material properties may change significantly. In general, the CTE decreases to 0 at 0 K, while the stiffness, as given by Young's modulus, increases.

In particular, epoxies are noted for their high increase in stiffness at low temperatures, which may vary significantly depending on factors such as filler content and type (see e.g. [16]).

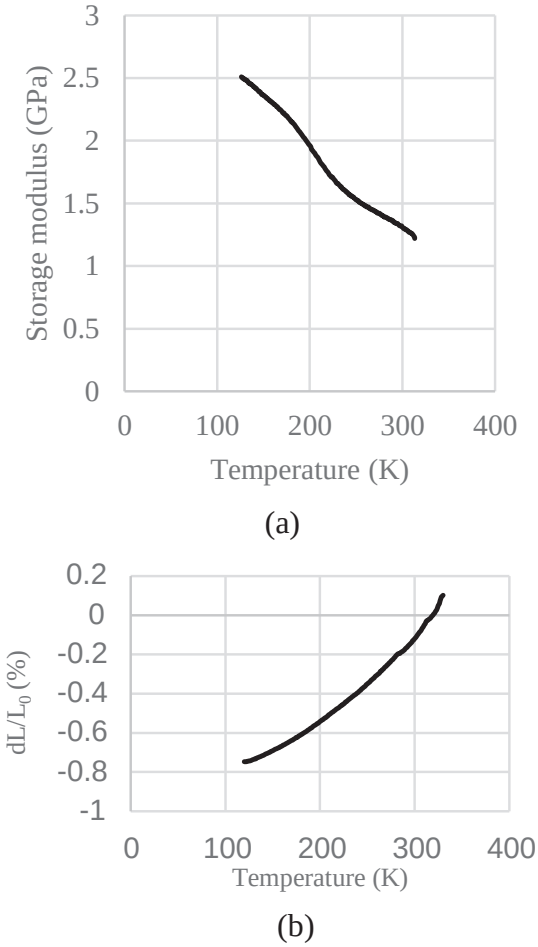

Fig. 4. Measured storage modulus (a) and thermal expansion of Masterbond EP29LPSPAO-1 BLACK from RT to − 150 °C.

There exists several commercial epoxies designed for cryogenic applications. As a general rule, to avoid cracking in brittle materials, the epoxy should remain sufficiently compliant, meaning low elastic modulus, at low temperatures. Two similar epoxies with similar properties were tested: Masterbond EP29LPSPAO-1 BLACK and Stycast 1266. As temperature-dependence of the CTE and elastic modulus of the Masterbond epoxy was lacking, dynamical mechanical thermal analysis (DMTA) and dilatometry measurements were performed. The measured shear modulus was converted to elastic modulus using the formula $E = 2G(1 + \nu)$, assuming $\nu = 0.3$ as the value for Poisson's ratio. The measurement results are shown in Fig. 4 (a,b). The curves were then extrapolated to 4 K.

Stycast 1266 has similar mechanical properties [2]. However, it is transparent and has a much lower viscosity than Masterbond EP29LP-SPAO-1 BLACK.

Only a limited number of studies report on the elastic modulus of organic (PCB) substrates at low temperatures. The elastic modulus at room temperature typically varies between 15 and 30 GPa. An increase of around 1–2 GPa for every 100 K decrease is a reasonable assumption [17] for organic PCB. Typical values of CTE at room temperature are 10–25 ppm/K. In the simulations, α was assumed to decrease linearly from α at 300 K to 0 ppm/K at 0 K. For the remaining materials, the temperature-dependent values of the CTE and elastic modulus from room temperature to 4 K were taken from literature. In some cases, extrapolations were made when data was missing for the lowest temperatures.

The total relative thermal expansion, ΔL/L, from RT to 4 K was found by taking the integral of α. The used properties are listed in

Table 1
Material properties used in finite element simulations.

Material	α (293 K) ($10^{-6}\frac{m}{mK}$)	$\frac{L_{4K}-L_{293K}}{L_{293K}}$, %	Young's modulus, E (GPa)	
			293 K	4 K
Si [1]	2.6 ppm	− 0.0024	130	130
Masterbond EP29LPSPAO-1 BLACK	–	− 0.67[a]	3.3	9[a]
Stycast 1266 [2]		− 0.15	3.2	11.0 (77 K)
Zirconia [4]	8.7 ppm/K	− 0.18	250	250[a]
Borosilicate [5]	3.25 ppm/K	− 0.06[a]	64	64[a]

[a] Estimated values based on extrapolation.

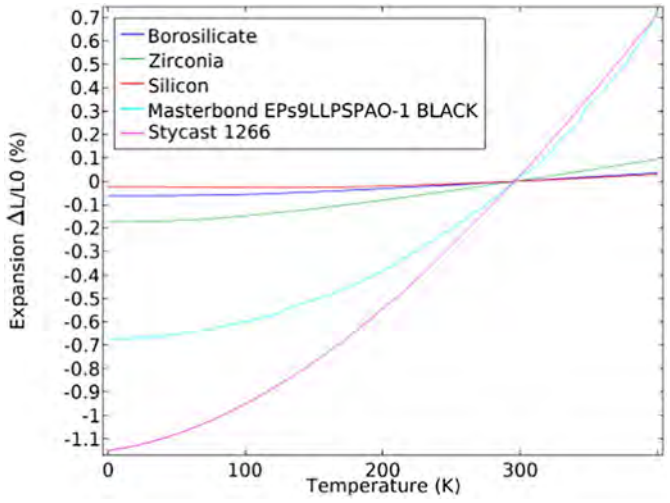

Fig. 5. Values of total thermal expansion relative to room-temperature (300 K) used in thermomechanical simulations. All values except from those of the adhesive are based on data taken from literatures. Extrapolation to the lowest temperatures was used in case of missing data.

Table 1. In Fig. 5, the total relative expansion is shown for all materials, except PCB material, in the full temperature range.

3.3. Discussions of simulation results

Silicon is a brittle material in which cracking occurs above a given stress level. Most likely, cracking is initialized at a preexisting flaw from the sawing/dicing process. Thus, the strength of the silicon die may vary significantly. However, it is far below the ultimate yield strength of silicon. Typical values of silicon die strengths are in the range 300–700 MPa (e.g. [18,19]).

In brittle materials, the maximum principal stress is often used to predict failure. However, following the reasoning in [12], the axial stress (σ_{xx}) is used to assess the stresses in the following results.

First, the stress due the adhesive bonding between the substrate/sample holder was simulated for varying PCB properties. Fig. 6 shows the distribution of the tensile stress σ_{xx} on the top surface of the die at 4 K. Fig. 7 (a) show σ_{xx} along the center line for different values of E, α and d, while Fig. 7 (b) shows the displacement in the z-direction. In all cases, a tensile stress is present near the edge. For 2 mm PCB thickness, the stresses are compressive near the center, while for 1 mm thickness, the stress is tensile. The bending increases for higher values of E and α, while higher thickness, d, of the PCB, reduces the bending. Likely, the compressive stress is due to the larger contraction of the PCB relative to the die, while the tensile stress is caused by the bending of the die.

Next, the adhesive fiber attachment was included in the model.

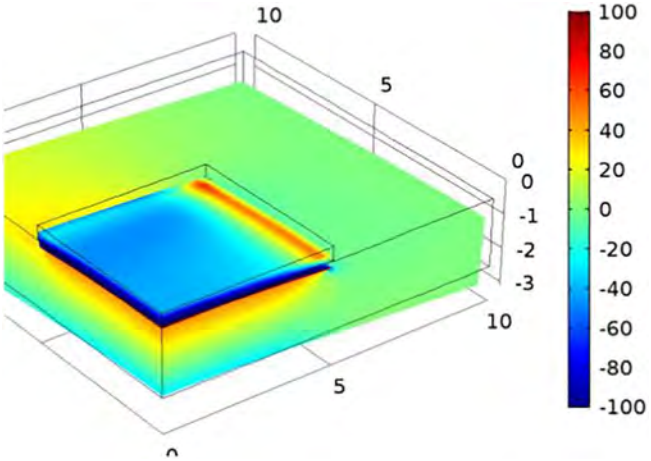

Fig. 6. Simulated axial stresses (σ_{xx}) at 4 K for a bare 10 mm × 10 mm silicon die on PCB with properties d = 2 mm, E = 20 GPa, α = 15e − 6/K.

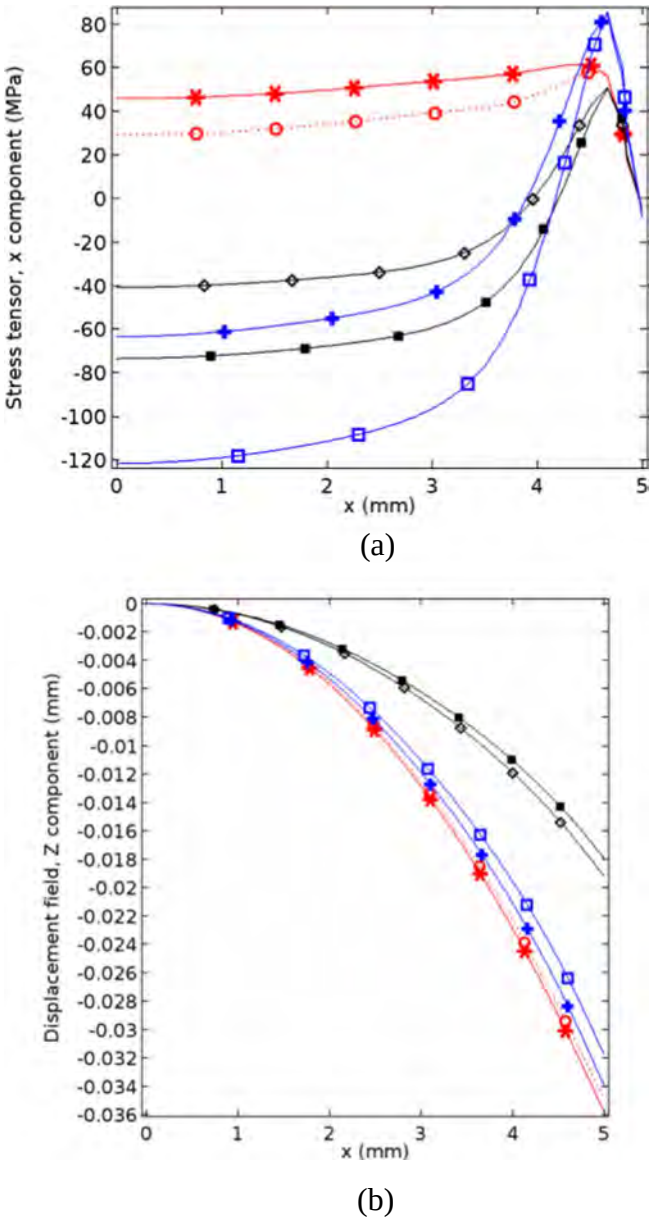

Fig. 7. (a) Magnitude of σ_{xx} along the top center line on die. (b) Displacement in z-direction along top center line. Legend for graphs (a) and (b) is given below.

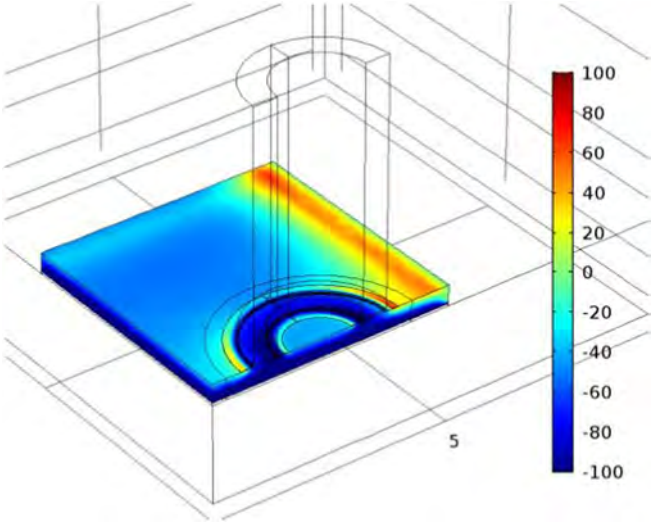

Fig. 8. Axial stresses (σ_{xx}) in silicon die on PCB substrate with zirconia alignment sleeve with 5 µm standoff, at 4 K.

Material properties for the PCB were chosen to be: E = 20 GPa, α = 15e − 6/K, d = 2 mm in the following results. These values were selected as they are similar to mechanical properties of the PCB material used for later experimental testing.

σ_{xx} on the surface of the silicon carrier with a borosilicate sleeve is shown in Fig. 8. It can be seen that the bonding of the sleeve has a significant impact on stresses compared to the bare substrate. In particular, the stresses increase in the vicinity of the alignment sleeve compared to the bare die. The maximum values of σ_{xx} in the die is shown in Fig. 9, for different values of standoff height *h*. The zirconia sleeves causes higher stresses than the borosilicate sleeve. For increasing *h*, the stress decreases for the zirconia sleeve, although levelling off at higher values than for the bare die. On the other hand, the borosilicate sleeves lead to overall lower σ_{xx}, while being relatively insensitive to both *h*.

The results also show that the epoxy with higher thermal expansion and elastic modulus at 4 K leads to increased stress.

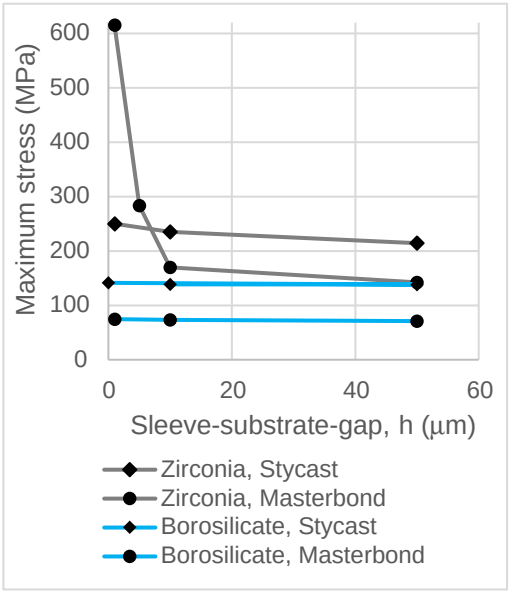

Fig. 9. Maximum axial stress (σ_{xx}) in silicon at 4 K versus sleeve-substrate distance *h*. For $d < 10$ µm, the result from one configuration (Zirconia, Master) diverged from other results, possible due to the presence of unphysical stress singularities. (a) Zirconia sleeve. (b) Borosilicate sleeve.

The increase in stress caused by the alignment sleeve bonding may be explained by the competing bending forces caused by the sample holder and the alignment sleeve. As both the alignment sleeve and the sample holder have higher CTE than the silicon substrate, they will impose opposite bending moments on the substrate, leading to higher local stresses. However, as borosilicate is more closely matched to silicon, the stresses in this case are lower as compared to zirconia.

4. Experimental tests and results

Test samples with different configurations were prepared as described in Sections 2.2 and 2.3. Owing to the results of the finite element simulations, zirconia sleeves were not tested further. The two different types of epoxy described in Section 3.2 were used for alignment sleeve bonding, while a 2 mm thick Ro4350b was used as the PCB. The CTE of this material is given as $11 \cdot 10^{-6}$/K, and the elastic modulus is given as 16.7 GPa at room temperature. Thus, the values are similar to those used in the simulations.

The borosilicate sleeves were aligned to the silicon substrate with a small air gap before epoxy was applied around the edges. Due to the lower viscosity of the Stycast epoxy, it was found that the epoxy could fill the sleeve-substrate gap, as shown in Fig. 2 (b), even when placed directly on substrate.

After preparation, the electrical response of the photodiodes was tested to find the initial characteristics.

The test regime consisted of rapid thermal cycling between room temperature and 77 K by immersion in a liquid Nitrogen bath. Thereafter, the assemblies were operated for up to 1 h in liquid Helium.

A criterion for assessing the reliability of photodiodes is if the dark current exceeds a given treshold. In [20], it was shown that planar InGaAs photodiodes exposed to 200 °C have a lifetime above 8000 h. A further performance measure of the photodiodes was adapted by taking the ratio of voltage, U, to current, I, for a given voltage. Thus, an increase in this measure indicates increased resistance of the conducting and the photodiode connection. As the photodiode characteristics vary significantly with temperature, voltage bias of 0.6 V was used at room temperature, while voltage bias of 0.8 V was used at 77 K. Fig. 10 shows the evolution of U/I during the first 10 thermal cycles, which shows that the photodiode response was stable during thermal cycling between room temperature and 77 K.

In a following extended test at 4 K, the photodiodes showed no signs of degradation. The dark current at − 2 V reverse bias was stable, below 1 nA in all test, both a room temperature and 4 K.

No adhesive failure, cracking in silicon or photodiode detachment was observed for several devices tested. Fig. 11 shows an assemble

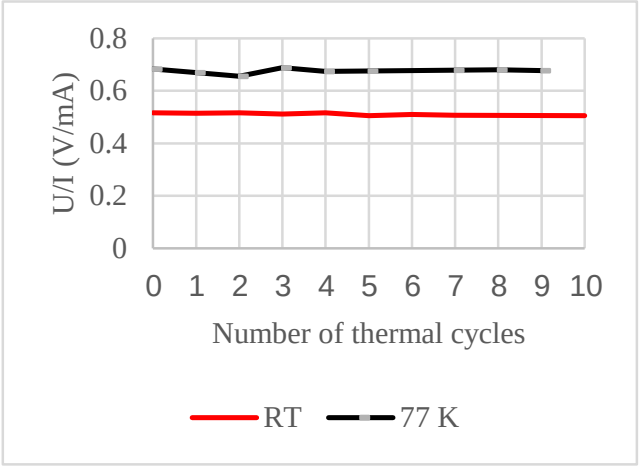

Fig. 10. Photodiode resistance U/I for voltages 0.6 V and 0.8 V at room temperature and at 77 K respectively.

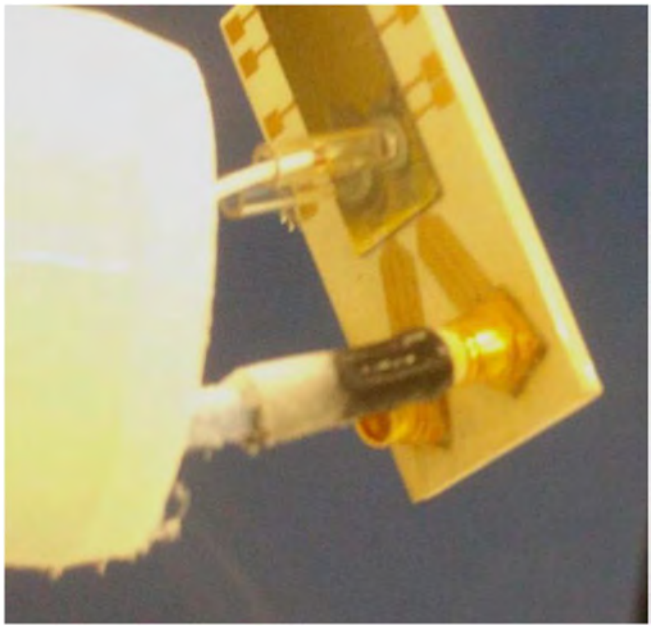

Fig. 11. Example of photodiode module sample with after cooling with liquid Helium.

module after immersion in liquid Helium.

However, in some cases, we have observed degradation of the photodiode response after storage. In a single case, a sudden photodiode failure was observed during immersion in liquid Helium. The cause of these failures, however, is unclear, as effects such as ESD cannot be excluded.

5. Conclusion

Finite element modelling and thermal cycling test were used to assess the reliability of a photodiode module structure intended for cryogenic applications. The finite element model showed that the mechanical properties of the PCB, as well as the properties of the optical fiber alignment sleeve significantly influence the stresses. Using epoxy with lower CTE/elastic modulus, using thicker/stiffer PCB material, as well as borosilicate sleeve may significantly reduce chance of cracking.

Thermal cycling tests showed the capability of the module to tolerate both thermal shocks and thermal cycling and operation between room temperature and 77 K, as well as long-term immersion in liquid Helium.

Acknowledgements

Oliver Kieler at Physikalisch-Technische Bundesanstalt, Germany is acknowledged for fabrication of the silicon substrates used in these tests.

This work was partly carried out with funding by the European Union within the EMRP JRP SIB59 Q-WAVE and EMPIR JRP 15SIB04 QuADC. The EMRP and EMPIR are jointly funded by the EMRP participating countries within EURAMET and the European Union.

In addition, the work was also partly funded by a PhD scholarship from University College of Southeast Norway funded by the Norwegian Ministry of Education and Research.

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Article 6:
Evaluation of InGaAs/InP photodiode for high-speed operation at 4 K
E. Bardalen, B. Karlsen, H. Malmbekk, M. N. Akram, and P. Ohlckers
Int. J. Metrol. Qual. Eng., Vol. 9, Nov. 2018, DOI: 10.1051/ijmqe/2018015

Int. J. Metrol. Qual. Eng. **9**, 13 (2018)

https://doi.org/10.1051/ijmqe/2018015

International Journal of Metrology and Quality Engineering

Available online at:
www.metrology-journal.org

RESEARCH ARTICLE OPEN ACCESS

Evaluation of InGaAs/InP photodiode for high-speed operation at 4 K

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Received: 11 December 2017 / Accepted: 14 October 2018

Abstract. An optically controlled high-speed current source located at 4 K is likely to improve the performance of pulse-driven Josephson junction arrays. A custom photodiode module with an Albis PDCS24L InGaAs/InP PIN photodiode is investigated in order to determine the suitability at 4 K. The DC and frequency response were tested at room temperature and at temperatures down to 4 K. For continuous wave optical input, photocurrents above 15 mA were produced at both room temperature and 4 K. *I*–*V* measurements show that the threshold voltage increased from 0.5 V at room temperature to 0.8 V at 4 K. The transmission coefficient S_{21} of the optoelectronic system, including cables and modulated laser source, was measured using a vector network analyzer. Up to 14 GHz, the results showed that the frequency response at 4 K was not degraded compared to room temperature. At room temperature, reverse bias voltages of up to 3 V was required for the highest bandwidth, while at 4 K, the photodiode was operated at nearly full speed even at 0 V reverse bias.

Keywords: optoelectronics / cryogenics / voltage standards

1 Introduction

The pulse-driven Josephson Voltage Standard [1] is a technique for generating quantum-accurate voltages, by transferring short current pulses through Josephson junction arrays (JJA), which are often operated by cooling with liquid helium, at a temperature near 4 K. Any voltage waveform may be generated by modulating the repetition frequency $f(t)$:

$$V(t) = Nn\frac{h}{2e}f(t), \tag{1}$$

where N is the number of Josephson junctions in series, h is Planck's constant and e is the electron charge. The Shapiro step number n depends on pulse parameters such as width and height [2].

Recently, very pure sine waves with voltages up to 1–2 V with frequencies up to a few kilohertz have been demonstrated using this technique [3,4]. Here, several Josephson junction arrays are operated in parallel, with the output voltage coupled in series, in order to increase the output voltage.

Utilizing optoelectronics to generate the high-speed pulses is believed to have several benefits compared to a direct electrical link between room-temperature pulse pattern generator (PPG) and the cryogenic chamber [5]. As the optical link is electrically isolated from the signal generator, reduced cable crosstalk and electromagnetic interference may be expected. By locating the photodiode close to the JJA, at 4 K in the cryogenic chamber, the cable length can be minimized and even eliminated.

The optoelectronic system consists of a laser source where the optical output is modulated by the PPG. The high-speed optical pulses are connected with an optical fiber to a photodiode, which converts the optical pulses into current pulses, which are transmitted to the JJA. The system may also contain other elements such as optical attenuators to fine-tune the pulse height.

In the following, an optoelectronic system has been set up for testing the small signal frequency response of a high-speed photodiode. However, the test setup does not include the JJA chip. The photodiode, a commercial InGaAs/InP PIN photodiode, is tested with the purpose of comparing the performance at 4 K compared to room temperature. Similar photodiodes have been shown to have no decrease in bandwidth at temperatures below 10 K, even operating with improved performance [6,7].

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Fig. 1. Sample 1. Assembly with adhesively bonded fiber components and SMP connector. Inset shows microscope image of photodiode on submount with wire bonds, with a manually aligned optical fiber.

2 Test setup and sample preparation

A Rohde & Schwarz ZVL vector network analyzer (VNA) was used to measure the frequency response of the laser-photodiode setup. The output port of the VNA was connected to the modulation port of a modulator-integrated 1310 nm Eudyna FLD3F10NP-A DFB laser, which is specified to have a minimum bandwidth of 10 GHz and maximum optical output power of around 1 mW. The laser was also biased with a constant DC current. The optical output consisted of a continuous wave (CW) combined with a smaller modulated signal as the output power from the VNA is not sufficient to completely extinguish the CW.

In addition, a higher powered 1310 nm laser source, with optical output power up to 30 mW, was used to measure the photocurrent for different CW powers.

The optical output from the laser was coupled via a single mode optical fiber (SMF) to the photodiode. The electrical output from the photodiode was connected to a coaxial cable. A bias tee separated the RF output to the input port of the VNA and the DC component to a Keithley 6430 source meter, which was also used to apply bias voltage to the photodiode.

The photodiode used in these tests were Albis PDCS24L photodiodes mounted on small ceramic submounts. These photodiodes were selected as they have a bandwidth of up to 28 Gbps and are available as bare chips, thus enabling custom packaging for later integration with the Josephson system. Different configurations of illumination and sample mounting were tested to uncover potential limitations in photodiode packaging. The photodiode is illuminated via an integrated lens, which makes optical alignment rather easy. The sample configurations were as follows.

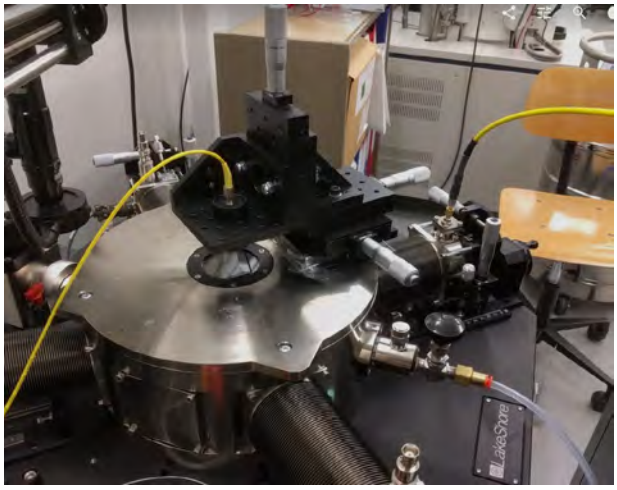

Fig. 2. Sample 2. The photodiode is located in vacuum and is illuminated using a focused beam through cryoprobe window.

2.1 Sample 1: Photodiode with direct optical fiber coupling

In the first configuration, optical fiber-connected samples were made for directly immersing in liquid helium. The photodiodes were adhesively bonded to a 2 mm thick Rogers RO4350b sample holder with copper coplanar waveguide (CPW) transmission lines designed for 50 Ω characteristic impedance. The ceramic submount was glued directly to the sample holder and wire-bonded to the CPW. Surface-mounted SMP connectors were soldered to the CPW, where a high-speed coaxial cable was connected, as shown in Figure 1.

A single mode fiber terminated by glass ferrule (Thorlabs part no: SMPF021) was inserted into a matching borosilicate sleeve (Thorlabs part no: 51-2800-1800) that was aligned to the photodiode and glued directly to the sample holder with epoxy (Master Bond EP29LPSPAO-1 BLACK).

2.2 Sample 2: Photodiode mounted in cryoprobe

The second sample was mounted inside a cryogenic probe station, Lakeshore CPX, for operation at temperature between 4 K and room temperature in vacuum. The ceramic submount was glued to a small alumina plate that was thermally anchored to the cold plate of the cryoprobe.

A biconvex lens mounted to a micrometer stage was used to focus the beam from the SMF fiber through the outer cryoprobe window, as seen in Figure 2. The inner cryoprobe window was removed as it blocks infrared radiation. An RF probe was used to measure the signal output from the photodiode.

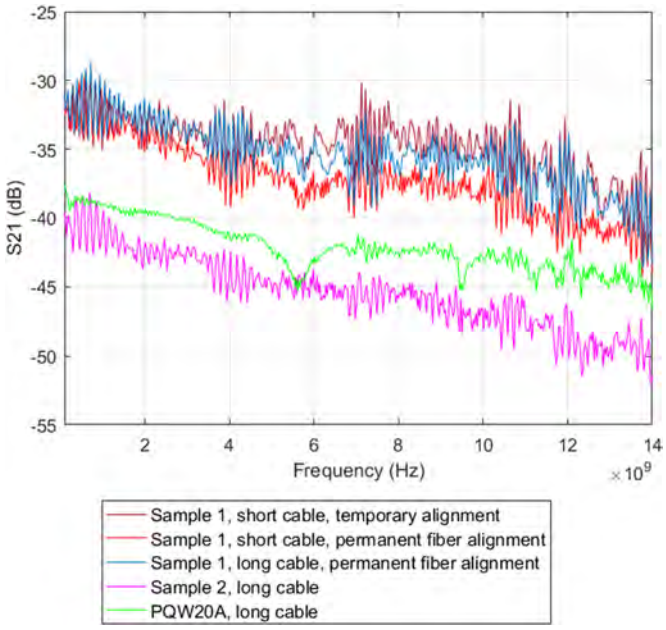

Fig. 3. Transmission for sample 1, sample 2 and the Albis PQW20A module in different configurations at room temperature. Reverse bias voltage of 3 V is used in all measurements.

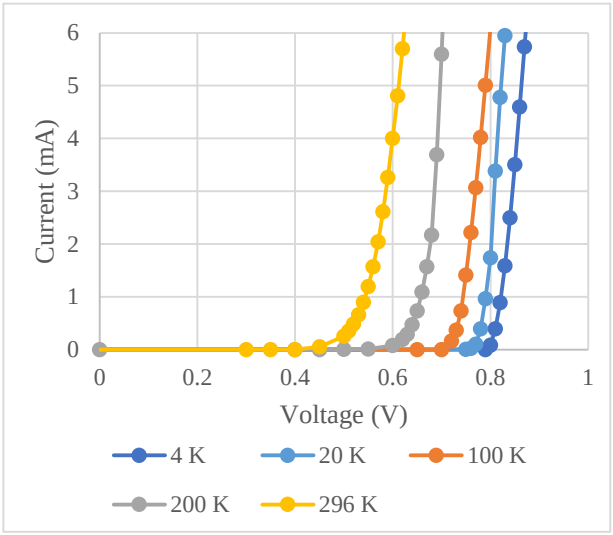

Fig. 4. *I*–*V* measurements of sample 1 (4 K) and sample 2 (20, 100, 200 and 296 K).

Additionally, for comparison with sample 1 and 2, a commercial photodiode module, Albis PQW20A, was tested in the same setup. This module also contains an Albis InGaAs PIN photodiode but has an integrated biasing circuit that includes a 50 Ω resistor to ground. This resistor is likely intended to minimize standing waves in the electrical output cable. In this case, the bias voltage is applied directly to the PQW20A module.

3 Results

Sample 1 was measured at room temperature and in liquid helium, while for sample 2, S_{21} was measured at temperatures 20, 100, and 200 K as well as at room temperature.

The transmission coefficient S_{21} was measured from frequencies between 100 kHz and 14 GHz for various bias voltages of the photodiode.

3.1 Effects of optical fiber alignment and cable length

The measured transmission coefficients include attenuation and reflections inside the complete system, including the laser, photodiode and in cables/connectors. To evaluate the effect of these different factors, the photodiode was first measured at room temperature with the optical fiber aligned by a micrometer stage. Next, the optical fiber was permanently mounted and the assembly was tested with different cable lengths in order to establish a baseline for the cryogenic measurements. Figure 3 shows S_{21} from frequencies 100 kHz to 14 GHz. At frequencies higher than 5 GHz, the permanent fiber alignment slightly reduced the transmission by about 2 dB, compared to the manual alignment. Inserting a 2 m coaxial patch cable between the bias tee and the SMP connector further reduced S_{21}, in particular at frequencies above 1 GHz.

Sample 2 has a similar response to sample 1. However, due to the less efficient optical coupling, the frequency response was reduced by 6–8 dB.

Both sample 1 and sample 2 contained large oscillations in the frequency response, of around 1–4 dB with a period of around 125 MHz.

The overall transmission for the PQW20A module was reduced by more than 3 dB for all frequencies compared to sample 1. This is consistent with the use of the 50 Ω resistor, which theoretically reduces the power output to the output connector by half. The large oscillations seen in sample 1 and 2 were reduced significantly, although they are still present.

The overall system response was less than −30 dB for all frequencies, which can mostly be attributed to a high loss in the laser modulation input. In the best case, a −3 dB bandwidth of the system can be found at approximately 10 GHz. However, packaging and coaxial cables reduced the bandwidth significantly.

3.2 Temperature effects

The 2 m patch cable is used following the results in order to facilitate immersion in the liquid helium Dewar. A numerical smoothing function was applied to all results in order to improve the readability of the curves.

The DC response of the photodiode in dark condition is shown in Figure 4. It can be seen that the threshold voltage increases, as expected, at lower temperatures.

The photocurrent response to CW input for different laser currents was measured at room temperature and at 4 K for sample 1, as shown in Figure 5. The photodiode was able to produce currents well above 15 mA at both temperatures. At 4 K, the current response was reduced to by approximately 10% compared to the room temperature result.

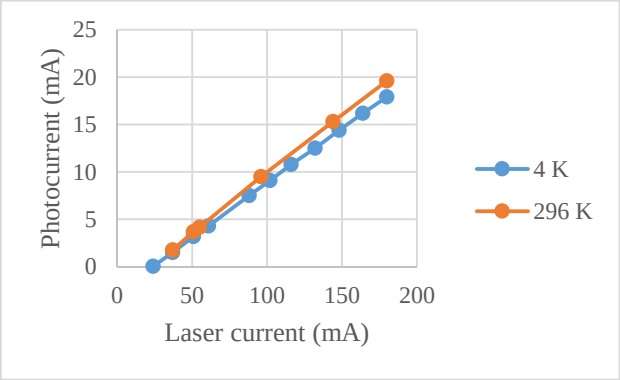

Fig. 5. Photocurrent generated by sample 1 for varying laser current, with 0 V bias applied to photodiode.

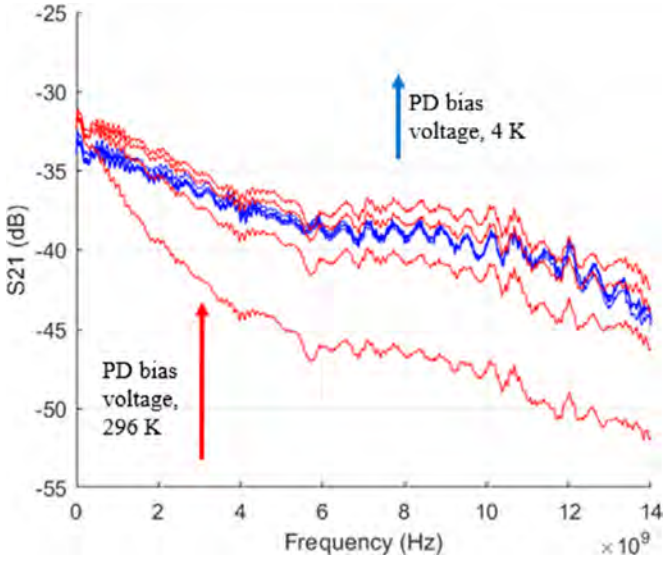

Fig. 6. Transmission measurements of sample 1 at room temperature (red lines) and at 4 K in liquid helium (blue lines) for different bias voltages (0, 1, 2, 3 V). A numerical smoothing function was used to remove oscillations seen in Figure 3. At room temperature, full speed is reached for bias voltages close to 3 V. At 4 K, the photodiode reaches full speed at a bias voltage close to 1 V.

Figure 6 shows the frequency response at room temperature and at 4 K for sample 1 for reverse voltages between 0 and 3 V. At room temperature, the frequency response was maximized at bias voltages of approximately 3 V. At 4 K, full speed was achieved at very low bias voltage. Changing the bias voltage from 0 to 3 V resulted in less than 1 dB difference in S_{21}. The responsivity was reduced by around 1.5 dB at 4 K compared to room temperature.

For comparison, the measurements were repeated in the cryoprobe for sample 2, using a focused beam as described in Section 2. The sample stage reached a temperature of 4 K, while the temperature of the cryogenic probe arm was 20 K. Therefore, the temperature is assumed to be 20 K. Figure 7 shows that at 20 K, the transmission

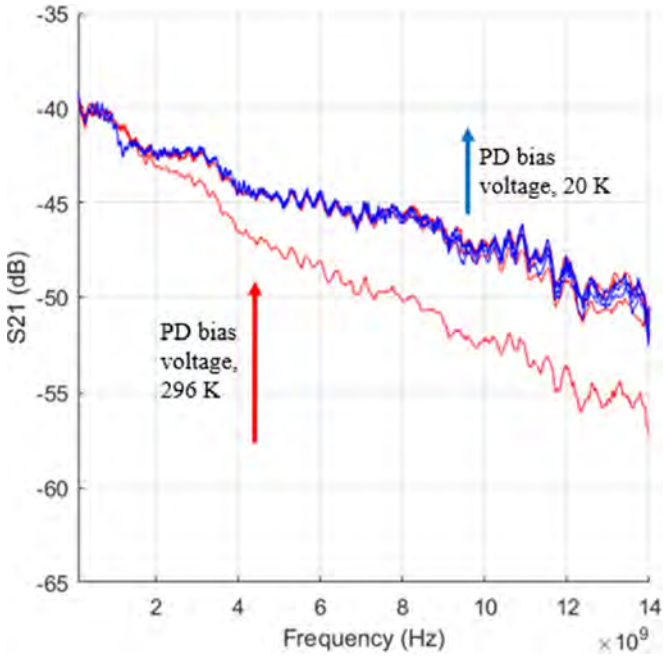

Fig. 7. Transmission measurements of sample 2. Transmission S21 at room temperature (red lines) and 20 K in cryoprobe (blue lines) for different bias voltages (0, 1, 2, 3 V). A numerical smoothing function was used to remove oscillations seen in Figure 3. At room temperature, increasing the reverse voltage above 2 V has almost no influence on bandwidth, while at 20 K, 0.5 V is sufficient.

curves overlap the curves for room temperature. Furthermore, the measurements show a lower dependence on bias voltage at both temperatures. At 20 K, the gain effect of increasing bias voltage from 0 to 3V is less than 1 dB.

4 Discussion

The photodiode frequency performance at low temperatures is affected by several temperature-dependent effects. These include incomplete ionization and changes in physical properties such as bandgap and electrical mobility. The reduced need for bias voltage at 4 K may be explained by a higher electric field in the absorption layer of the photodiode due to the increase in bandgap and changes in the Fermi level, as well as changes in electrical mobility in InGaAs and InP. The reduced DC responsivity, as shown in Figure 5, observed at 4 K for sample 1, may be partly explained by increased bandgap in InGaAs. However, thermal deformations may also have influenced the optical coupling efficiency between the photodiode and the optical fiber. This may also explain the lower overall frequency response at 4 K for sample 1.

Operation of JJA would require current pulse amplitudes comparable to the critical current density I_c in the JJA [2], which may be up to several mA. At higher optical power input, the frequency response may be reduced due to space-charge effects [8] and changes in bias voltage caused by the load resistance [9]. For JJAs, it is common to

terminate the array with a 50 Ω resistor. Thus, higher reverse bias may be needed at 4 K than the results shown here indicate.

5 Conclusions and further work

A setup consisting of a modulated laser and a commercial InGaAs/InP photodiode was characterized at room temperature and 4 K using a network analyzer. The results show that the cryogenic environment does not negatively impact the photodiode response, and may even improve performance as lower bias voltage is required.

This may enable the operation of Josephson arrays using optical fiber-coupled photodiodes cooled to 4 K. However, further consideration of impedance matching and transmission line design may be necessary to reduce unwanted reflections.

The photodiode response to optical pulses with amplitudes of several mW must be tested using a high-speed PPG, suitable laser source/modulator and oscilloscope.

The prospect of closely integrating the photodiode with the Josephson array is to be investigated. For example, photodiodes may be flip-chip bonded to a silicon substrate with superconducting transmission lines, or directly onto the JJA-integrated circuit silicon chip.

Another interesting prospect is to perform numerical simulations of both photodiode behavior and the complete system behavior. Such simulations may enable better predictions of performance, also enabling improvement in system design.

This work was partly carried out with funding by the European Union within the EMRP JRP SIB59 Q-WAVE and EMPIR JRP 15SIB04 QuADC. The EMRP and EMPIR are jointly funded by the EMRP participating countries within EURAMET and the European Union.

In addition, the work was also partly funded by a PhD scholarship from University College of Southeast Norway, funded by the Norwegian Ministry of Education and Research.

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Cite this article as: Eivind Bardalen, Bjørnar Karlsen, Helge Malmbekk, Muhammed Nadeem Akram, Per Ohlckers, Evaluation of InGaAs/InP photodiode for high-speed operation at 4 K, Int. J. Metrol. Qual. Eng. **9**, 13 (2018)

Article 7:

Optical pulse-drive for the pulse-driven AC Josephson voltage standard

O. Kieler, B. Karlsen, P. Ohlckers, E. Bardalen, M. Nadeem Akram, R. Behr, J. Ireland, J. Williams, H. Malmbekk, L. Palafox, and R. Wendisch

IEEE Trans. Appl. Supercond. Vol. 29, No. 5, Aug. 2019, DOI: 10.1109/TASC.2019.289985

Optical Pulse-Drive for the Pulse-Driven AC Josephson Voltage Standard

Oliver Kieler, Bjørnar Karlsen, Per Alfred Ohlckers, Eivind Bardalen, Muhammad Nadeem Akram, Ralf Behr, Jane Ireland, Jonathan Williams, Helge Malmbekk, Luis Palafox, and Ruediger Wendisch

***Abstract*—We developed an optical pulse-drive for the operation of the Josephson Arbitrary Waveform Synthesizer (JAWS) using a fast photodiode (PD) operated at 4 K, close to the JAWS chip. The optical pulses are transmitted to the PD by an easily removable optical fiber attached to it. A bare-lensed PD is mounted by flip-chip technique to a custom-made silicon-carrier chip. This carrier chip is equipped with coplanar waveguides to transmit the electrical pulses from the PD to the JAWS chip mounted on a separate printed circtuit board (PCB). The main components of this optical setup are a laser source, a high-speed Mach–Zehnder modulator, and the modulator driver. The waveform pattern is supplied by a commercial pulse pattern generator providing up to 15 GHz electrical return-to-zero (RTZ)-pulses. Unipolar sinusoidal waveforms were synthesized. Using a JAWS array with 3000 junctions, an effective output voltage of 6.6 mV root mean square (RMS) at the maximum available clock-frequency of 15 GHz was achieved. Higher harmonics were suppressed by more than 90 dBc at laser-bias operation margins of more than 1 mA.**

***Index Terms*—AC Josephson voltage standard, Josephson arbitrary waveform synthesizer, SNS Josephson junction, sigma-delta modulation, optical pulse-drive, flip-chip technology.**

I. Introduction

AFTER many years since the first realization of a pulse-driven AC Josephson voltage standard [1], recent developments in increasing the effective output voltage to 1 V root mean square (RMS) or even more [2]–[5] show that the use of a pulse-driven Josephson voltage standard is an important approach for voltage metrology. This AC Josephson voltage standard is often called "Josephson Arbitrary Waveform Synthesizer" (JAWS) and it is already used in several NMIs for metrology applications [6]–[15]. For the application in JAWS, the Josephson junctions are operated by short current pulses to directly transfer flux quanta. According to the Josephson equation, a time-dependent voltage, which is quantized at all times, is generated. The signal-voltage and frequency are well defined by these two basic equations:

$$V_{signal} = A_{\Sigma\Delta} \cdot n \cdot m \cdot \Phi_0 \cdot f_{clock} \tag{1}$$

$$f_{signal} = T_{\Sigma\Delta} \cdot f_{clock} / L_{\Sigma\Delta} \tag{2}$$

The output voltage V_{signal} is the product of the Shapiro-step number n (typical: $n = 1$), the number of junctions in the series array m, the flux quanta $\Phi_0 = h/2e$ (h is the Planck constant and e the elementary charge), the sigma-delta code amplitude $A_{\Sigma\Delta}$ ($0 < A_{\Sigma\Delta} < 1$) and the clock-frequency f_{clock}. The maximum pulse-repetition frequency $f_p(t)$ used for our JAWS is 15 GHz, limited by the maximum clock frequency f_{clock} of commercially available pulse pattern generator (PPG). $A_{\Sigma\Delta}$ is a real number ($0 < A_{\Sigma\Delta} < 1$), but well defined. Since the numbers ($A_{\Sigma\Delta}$, n, m) are known, Φ_0 is determined by natural constants and f is very well defined, the JAWS delivers quantized arbitrary waveforms. The signal frequency f_{signal} is determined by the simple equation (2): the number of periods in the code $T_{\Sigma\Delta}$, the clock frequency f_{clock} of the PPG and the length of the waveform bit pattern $L_{\Sigma\Delta}$.

This fundamental approach enables the generation of quantized arbitrary waveforms with excellent spectral purity with low noise and no drift.

The use of an optical drive with photodiodes (PDs) operated at 4 K close to the JAWS chip could improve the JAWS in several ways:

1) Some years ago, Urano et al. [16] presented a JAWS system with optical drive. Our approach, using small bare PDs on a custom-made carrier, could provide an alternative way for parallel operation of several arrays that is easier and more cost efficient, because one optical channel can be split into several channels and each can operate one JAWS array. Therefore, output voltages could be increased to the range of 10 V RMS, which is desired for covering the whole voltage range for applications in DC/AC voltage metrology.
2) The use of optical fibers instead of high-frequency coaxial cables will reduce the thermal load to the system, which is an important aspect for operating JAWS systems in closed-cycle pulse-tube cryocoolers.
3) The optical drive also removes the coupling noise introduced by the PPG, which is important when extending the

Manuscript received October 25, 2018; accepted February 11, 2019. Date of publication February 18, 2019; date of current version March 27, 2019. This work was supported by the EU within the EMPIR JRPs QuADC. The EMPIR is jointly funded in part by the EMPIR participating countries within EURAMET and in part by the European Union. *(Corresponding author: Oliver Kieler.)*

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Digital Object Identifier 10.1109/TASC.2019.2899851

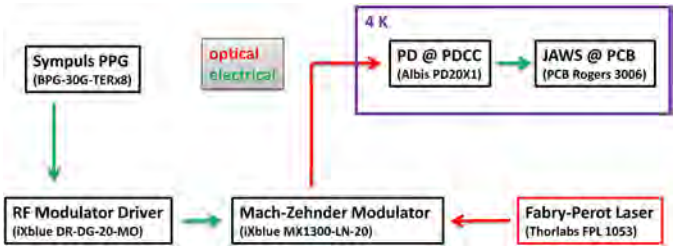

Fig. 1. Block diagram of a JAWS system with optical pulse-drive.

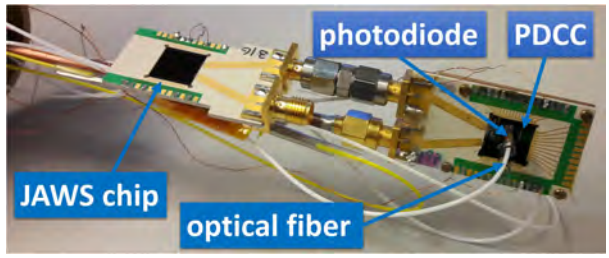

Fig. 2. Photograph showing the JAWS chip (left) and PDCC chip (right) connected. The optical fiber (white) is attached by glass tube guide to the PD mounted by flip-chip to the PDCC chip.

JAWS to higher signal frequencies above 1 MHz. Moreover, crosstalk between several high-frequency coaxial cables for transferring the pulses, is avoided by an optical drive.

4) Establishing a setup, where the PDs are very close to the JAWS chip significantly reduces the distortion and attenuation of the pulses, thus increasing the operating margins.

Pioneering work was done realizing an optical setup for JAWS [16], [17]. Here, only a small number of junctions (fewer than 500) and lower clock frequencies (up to 10 GHz) were used. As a consequence, the maximum effective output voltage was limited to well below 1 mV RMS.

As part of a collaboration between Justervesenet, University of South-Eastern Norway (USN), NPL and PTB, the development of an optical drive for a JAWS system was also begun [18]–[23].

This paper describes the combination of the newly developed optical pulse-drive system, including the optimized assembly for PD operation at 4 K. For this proof-of-principle experiment just a single JAWS array was used and first results will be presented.

II. Setup

SNS-type Josephson junctions (S . . . superconductor, N . . . normal conductor) with Nb_xSi_{1-x} [24], [25] as the normal-metal barrier material are used for the realization of several JAWS systems at PTB. The JAWS circuit design is based on a coplanar waveguide (CPW) high-frequency transmission line with series arrays of Josephson junctions embedded in the central conductor, similar to the designs used at NIST [1] and AIST [16]. For the PTB 1.5 V RMS JAWS setup [26], the electrical pulses are delivered by a Sympuls BPG30G-TERx8[1] ternary PPG with a data rate of up to 30 Gbit/s. The electrical pulses are transmitted by a length of about 1.5 m HF coaxial cable from the PPG output to the cryoprobe head. Inside the cryoprobe a 1.2 m semi-rigid HF coaxial cable transfers the pulses to the printed circtuit board (PCB)-carrier at the LHe temperature of 4 K, where the JAWS chip is mounted. One channel of this setup was used for the experiment described here.

This electrical pulse transmission is replaced now by an optical pulse-drive, shown schematically in Fig. 1. The pulse pattern is provided by the PPG (Sympuls, BPG-30G-TERx8) and electrically transferred to the RF Modulator Driver iXblue DR-DG-20-MO (RF-MD), which works as an amplifier for the electrical pulses. This RF-MD is biased at $V_{bias-RF} = 12$ V, $V_{amp-RF} =$ 0.3–0.8 V, $V_{xp-RF} =$ 0.7–0.8 V and provides a flat gain up to 10 GHz with a maximum output voltage of 8 V PP. The amplified pulses are transferred electrically to the Mach-Zehnder Modulator iXblue MX1300-LN-20 (MZM). The MZM was an $LiNbO_3$ based intensity modulator designed for 1310 nm lasers operated with a bias voltage of $V_{bias-MZM} =$ 9.2–10.2 V. The electro-optical bandwidth is 20 GHz and the electrical and optical properties are well suited for our application. The 1310 nm Fabry-Perot Laser Thorlabs FPL-1053 (FPL) output is coupled to the MZM. The O-band FPL delivers an adjustable maximum optical power of 130 mW, which should be sufficient to operate the PD. From the MZM the optical pulse pattern is guided to the cryoprobe by a 1 m FC/APC to FC/PC optical fiber (angled to flat patch cable) and a 2 m FC/PC to FC/PC fiber extension. A high performance InGaAs PD with an integrated lens (Albis PD20X1) [27] is selected to ensure an output current of up to 7 mA [22] at the operation temperature of 4 K ($V_{bias-PD} =$ 5 V). This bottom illuminated PD was optimized for high data rate of at least 28 Gbit/s and offers excellent dynamic response in the wavelength range between 1260 nm and 1620 nm at 300 K. The upper limit at 4 K is about 1510 nm due to the band gap increase at cryogenic temperatures as described in [21]. Providing a relatively large lens diameter of 100 μm, it is easy to implement it to the setup for a robust and reliable operation. Detailed optimizations and investigations of the high-speed performance at room-temperature and 4 K were performed [21], [22] and the optical pulse setup is described [23]. Finally, the PD produces the electrical pulses, which are transferred over a comparable short distance of about 4 cm from the custom-made silicon-based PD-chip-carrier (PDCC) to the JAWS chip (see Fig. 2), both mounted on separate PCB carriers. The PD and the JAWS array are directly coupled. The JAWS chip contains two separate identical JAWS arrays, but only one is used in this paper. Therefore, the lower uncovered SMA connector at the JAWS PCB shown in Fig. 2, is not used. For operation of the different components of the optical setup, the above mentioned six adjustable DC bias supply-voltages are used. A PPG pulse amplitude of 500 mV PP was used to drive the RF-MD. All components of the setup are matched to a 50 Ω impedance.

For electrical and/or optical operation a cryoprobe was constructed, equipped with a semi-rigid HF-cable and a pair of optical fibers (1.5 m FC/PC to 1.8 mm ferrule) to directly transmit the laser pulses to the PD. The fiber input uses an FC/PC connector and is connected to a single mode FC/PC to ferrule fiber inside of the cryoprobe.

The tiny PDs (350 μm $\times$ 350 μm) are illuminated through the lens on the back of the diode and are mounted by a sophis-

ticated flip-chip technology to the PDCC chip [21], [22]. A big advantage for practical use is that the optical fiber, connected via a glass tube glued to the PDCC chip, is removable. This tube is precisely aligned to the PD on-chip to ensure high-efficiency of the illumination. The flip-chip technique was established and performed at USN/JV in cooperation with NPL and PTB. The PDCC chip layout includes the contact pads for the PD, an alignment marker system for the flip-chip procedure of the PD and the alignment of the glass tube. DC-bias lines provide the bias voltage for the PD. The electrical pulses generated by the PD are transmitted by CPW high-frequency transmission lines with an impedance of 50 Ω. The width tapered CPW on the PDCC chip is wire bonded to a PCB-chip carrier, which carries the signals to edge launchers for 2.92 mm connectors.

The PDCC is fabricated at the clean-room facility at PTB using Nb for the DC/HF-lines and AuPd for the alignment markers and contact pads (PD and wire bond pads). An additional SiO_2 layer is deposited by PECVD to effectively protect the sensitive on-chip dc-block capacitors against electrical damage during operation. In particular, the post-clean room attachment of the PD and the gluing of the glass-tube introduces some particle contamination. This PDCC chip is then glued to a specially designed PCB-chip carrier (RO3006 material from Roger Corp.) containing Au-plated 1 oz. Cu-lines with tapered 50 Ω CPW lines to attach K-type PCB-edge connector directly to it. The JAWS PCB chip-carrier (Roger 3006) is connected at this point via an adapter. Both chips, JAWS and PDCC are connected by Al or Au wire bonds to the PCB carriers.

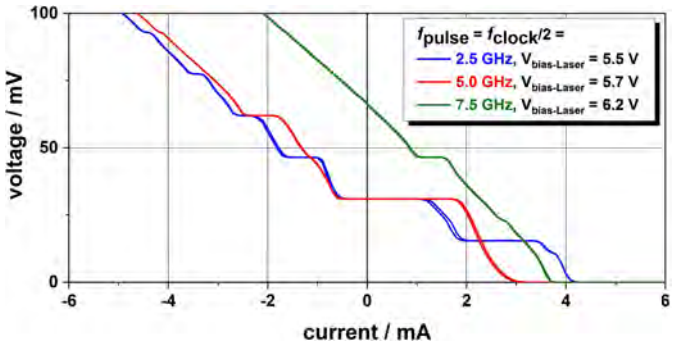

Fig. 3. Current-voltage characteristic under irradiation of optical pulses for 3 different pulse repetition frequencies. The pulse amplitude was adjusted for each frequency to maximize the Shapiro step width.

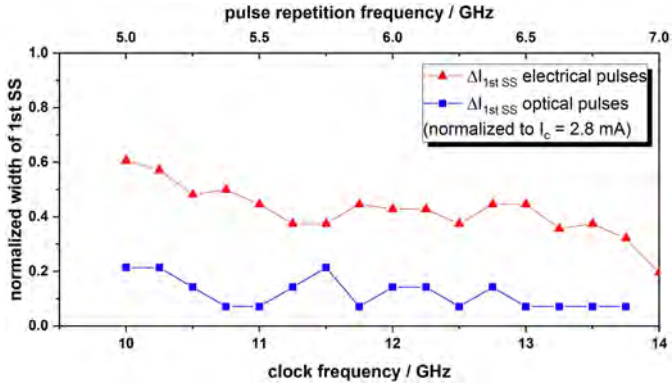

Fig. 4. Normalized Shapiro step width for electrical and optical pulses vs. clock frequency.

III. Measurements

For the measurements presented in this paper, a single JAWS array with 3000 Josephson junctions was selected. The array was characterized by electrical pulses first. The basic parameters are the critical current of 2.8 mA and the characteristic frequency of $f_c = 4.2$ GHz. At a constant pulse repetition frequency of $f_p = 4.2$ GHz the 1st Shapiro step (SS) with a maximum width of 1.8 mA can be generated with optimized pulse amplitude. At 10 GHz this step is still 1.4 mA wide. Synthesizing a sinusoidal waveform with electrical pulses only, pure spectra can be observed up to a sigma-delta code amplitude of $A_{\Sigma\Delta} = 0.9$ at a clock-frequency of $f_{clock} = 14$ GHz. This corresponds to a bipolar output voltage of $V = 55$ mV RMS with current operation margins of about 0.7 mA and a spectral purity of about 112 dBc spurious-free-dynamic-range (SFDR).

Fig. 3 shows three current-voltage characteristics (IVC) for optical pulses applied with constant f_p using a simple 2-bit alternating pulse pattern "10". The IVCs are shifted in the x-axis depending on the laser bias-voltage. Three different pulse repetition frequencies $f_p = f_{clock}/2 = 2.5/5.0/7.5$ GHz were realized ($f_{clock-max} = 15$ GHz). For each frequency the laser bias-voltage (i.e., the pulse amplitude) was adjusted for the maximum width of the Shapiro step. We measured a step width of about 1.9 mA at $f_p = 5$ GHz (with optimized pulse amplitude), which is slightly larger than with electrical pulses. The maximum pulse amplitude available from our optical pulse drive at $f_p = 7.5$ GHz is not sufficient for evolution of the maximum possible Shapiro step width. This will lead to low operating margins or restrict the operation to smaller clock frequencies or sigma-delta code amplitudes. Further work is ongoing to overcome this limitation.

Fig. 4 shows the Shapiro step, normalized to the critical current, for electrical and optical pulses in the clock frequency range from 10 GHz to 14 GHz. The same simple bit pattern used in Fig. 3 was applied. The optical pulse amplitude was adjusted in advance to achieve pure spectra at $f_{clock} > 10$ GHz and then was kept constant for all measurements. Although the $+1$st SS are narrower compared to Fig. 3, they are present at all frequencies, as required for synthesizing pure spectra in pulse-mode operation in JAWS. The width of the optically generated $+1$st SS is about three times smaller than for the electrical pulses. We note that the power for electrical pulses is reasonably larger, because there is a 16 dB amplifier installed at the PPG output. The Shapiro steps are more or less overlapping in the current axis (not shown). At the highest clock frequencies, the step widths are small (less than 0.3 mA) and the step position is shifted due to the limited pulse power. Again, this is an indicator of possible reduced operation margins at high pulse densities.

Due to the optical setup with just one PD implemented, unipolar waveforms can be synthesized using the 0th SS and $+1$st SS only. Therefore, the corresponding sigma-delta code, containing the bit-pattern for the desired waveform, was calculated accordingly. A DC-shift was included to ensure, that the minimum AC-voltage is zero. Additionally, only a first-order sigma-delta modulation was applied. Both modifications guarantee that there is no "-1" in the sigma-delta code, avoiding the -1st SS.

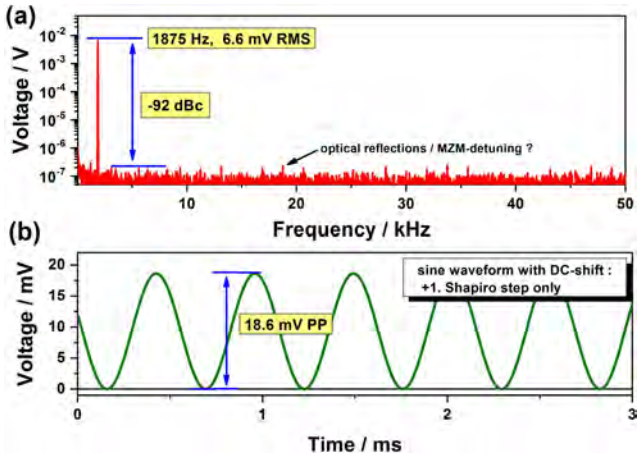

Fig. 5. (a) Frequency-spectra and (b) time-domain of a unipolar sinusoidal waveform at a signal frequency of 1875 Hz and amplitude of 6.6 mV RMS. A PD operated at 4 K and 15 GHz was used to provide the pulses to the JAWS array with 3000 junctions.

However, due to this unipolar operation the possible maximum output voltage of the JAWS array is reduced by a factor of two.

Fig. 5 shows the frequency spectrum (a) and time-domain signal (b) of a sinusoidal waveform synthesized at the maximal available clock-frequency of $f_{clock} = 15$ GHz. An output voltage of $V = 6.6$ mV RMS at a signal frequency of 1.875 kHz was generated using a sigma-delta code amplitude of $A_{\Sigma\Delta} = 0.2$, where no AC-coupling compensation [28] signal was applied. The time-domain shows the described DC shift of the sine wave – the minimum signal amplitude is at zero voltage. The laser-bias current, determining the pulse amplitude, was the only input parameter for the JAWS array. The Laser-bias operating margins are 1 mA (corresponding to about 300 μW power). The margins are small compared to the total laser power, but sufficient. In this range the signal amplitude and the spectrum were unchanged, which is a clear indication of operation margins. However, no metrological precision measurements were performed to confirm this. No extra dither current was applied to evaluate the overall current operation margins, and only one input parameter was used to operate the JAWS array. The purpose of this paper was to operate the PD as fast as possible for demonstrating the potential of this setup at high speed – regardless of the total range of operation margins. Laser-bias margins of about 1 mA are more than sufficient for many applications already. For lower clock-frequencies the laser-bias operation margins are larger (e.g., at $f_{clock} = 10$ GHz and $A_{\Sigma\Delta} = 0.2$ we determined margins of about 20 mA). The SFDR in Fig. 5(a) is about 92 dBc. Minor distortion tones are visible above the noise floor, which need further investigation. A possible reason is most likely related to MZM detuning and/or optical reflections. Another source of these harmonics could be the wide-range of wave-lengths emitted by the FP-laser. Due to this, the "0" parts of the optical signal cannot be completely extinguished, and noise may arise from this. Distributed Feedback (DFB) and Distributed Bragg Reflector (DBR) lasers provide a narrower range of wave-lengths, but they produce less power at 1310 nm. The connection of the JAWS chip to the PDDC is far from optimum and might also be the reason for these small distortions.

We also note that for $A_{\Sigma\Delta} > 0.3$ the JAWS is not on quantized operation margins anymore and higher harmonics appear in the frequency spectrum. A detailed analysis of the optical generated pulses and comparison with the electrical pulses from the PPG in [23] was performed. It was discovered that the optical pulses show about 1.5 times larger rise/fall time compared to the electrical pulses at highest clock rates.

Furthermore, the optical pulses do not perfectly return to zero current, when the pulse density is increased. This could directly explain the limitations for higher sigma-delta code amplitudes. However, when investigated with a sampling oscilloscope, the full width at half maximum of the optical pulses was about 80 ps at 4 K [23], which matches electrical pulses that have been successfully used with this JAWS array.

IV. Conclusion

We have tested the performance of an optical pulse-drive setup for JAWS. We used a single JAWS array containing 3000 Josephson junctions with a PD operating at 4 K close to the JAWS chip. The PD was connected by flip-chip technology to a specially manufactured carrier chip. A sophisticated easy-removable connection was developed to attach an optical fiber to the cold PD. This robust solution together with its small footprint offers a cost-efficient operation of several PDs in parallel, together with several JAWS arrays to increase the overall output voltage.

The IVC for constant pulse repetition frequencies at different clock frequencies and pulse amplitudes shows wide $+1$. Shapiro steps, as a precondition for the generation of arbitrary waveforms by the JAWS in the future. At the highest clock-frequency, the available laser power limited the width of the first Shapiro step that could be measured, which led to reduced operating margins at higher pulse-densities or/and pulse-rates.

We demonstrated a unipolar sinusoidal waveform at 1.875 kHz and 6.6 mV RMS with high spectral purity and wide operation margins, but no metrological precise measurement was performed to confirm the quantum accuracy of the synthesized signal. The PD was operated at the maximum available clock frequency of 15 GHz return-to-zero (RTZ)-pulses.

Further investigations of the pulse quality will be performed in the future. A more powerful laser will be used to overcome the limitations at high pulse repetition frequencies. The connection of the JAWS and the PD carrier chips must be optimized as well. In a next step we will combine two PDs for bipolar operation of a single JAWS array.

Acknowledgment

The authors would like to thank Th. Weimann, S. Bauer, and J. Kohlmann for valuable discussions and K. Stoerr, P. Hinze, B. Egeling, M. Schroeder, S. Gruber, and G. Muchow for technical assistance. This work has been funded by JRP QuADC. The QuADC project has received funding from the EMPIR program co-financed by the Participating States and from the European Union's Horizon 2020 research and innovation program.

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Doctoral dissertation no. 52
2019

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Optically operated pulse-driven Josephson junction arrays and range extension using voltage dividers and buffer amplifiers

Dissertation for the degree of PhD

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Bjørnar Karlsen

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ISBN: 978-82-7860-412-0 (print)
ISBN: 978-82-7860-413-7 (online)

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