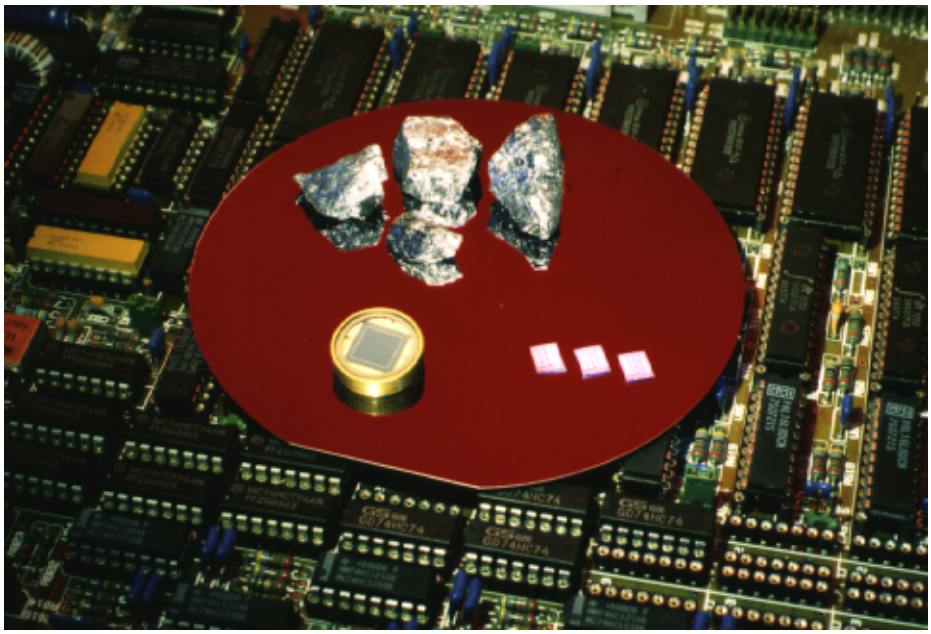
ELECTRONIC COMPONENTS, PACKAGING AND PRODUCTION



Leif Halbo and Per Ohlckers

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ELECTRONIC COMPONENTS, PACKAGING AND PRODUCTION

by

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University of Oslo

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PREFACE

The present book is primarily meant for university education in introductory electronic packaging technology. We attempt to give an overview that encompasses aspects of material technology, metallurgy, chemistry, physical properties, and mechanical properties. An understanding of the interplay of all these basic fields is necessary for choosing and using the available technologies in a best possible way in combination with a good design to get a product with the right quality. We describe component technologies, basic processing methods, design guidelines, the production of printed circuit boards and the common hybrid technologies, including multichip modules.

The book is primarily based on a course developed at the University of Oslo during the last 6 years. Parts of it have also been used at Norwegian Institute of Technology, Trondheim, Møre og Romsdal ingeniørhøgskole, Ålesund, Narvik ingeniørhøgskole, Narvik and the Defence Research Establishment, Kjeller, and a number of seminars.

When we started the course, there were practically no textbooks on the topic of packaging technology. Now there is an abundance of very good books, review articles, conference proceedings. Still we hope this presentation is found worthwhile, attempting to give a view of a broader area than what is common.

The course at University of Oslo has included some 40 lectures, starting with a video, made especially for the course, introducing the topic. Demonstrations of "hardware", i.e. numerous examples of products that illustrate the different technologies discussed, have been important as part of the lectures, bringing the principles "down to earth".

Three "projects" or lab experiments were part of the course:
- Design and manufacturing of a surface mounted printed circuit board
- Thermal simulation of a circuit (PCB) by a thermal CAD system
- High frequency calculations of characteristic impedance and losses.

Finally, 3 - 5 visits were made, to electronic companies producing advanced electronics with various types of modern technology (highly automated surface mounting, printed wiring board manufacturing, thick film and thin film hybrid circuits, monolithic silicon circuits), with generous attention from the key technical and managerial people in the companies.

We believe this combination of classroom teaching, lab work and a look inside the practical reality in industry is a key for the students to understand the important issues in packaging technology. They will not be skilled designers after this introduction, but hopefully it will be easier for their later employer to make them good designers or production specialists.

Thanks are due to the following people, among many others:

Markus Bayegan, Are Bjørneklett, Jan Brun Johansen, David Wormald, Henrik Jakobsen, Thor-Erik Hansen, Benjamin Baraas, Helge Osvold, Ernest Skontorp, Per Ohlckers, Helge Kristiansen, Agnar Grødal, Kjell Kristiansen, Torstein Gleditsch, Jørgen Andersen, Øystein Ra, Ole Flesaker.

Their help is gratefully acknowledged, for good discussions, reading parts of the manuscript, providing suggestions for contents, running labs, donations of illustrative products even before they were on the market, etc.

Financial support from COMETT, Project INSIGHT, and the Norwegian Research Council (NFR, previously NTNF), is gratefully acknowledged.

Oslo, September 1993

Leif Halbo

The most important change in this revised edition from 1995 is an additional chapter on micromachined devices. (Chapter 9) The other chapters have only minor changes. Figures and tables are integrated in the text, and page references are included in the table of contents. These and other modifications should improve readability. To keep in pace with new developments in electronic packaging technology, we recommend that the book is supplemented with an appropriate choice of recent published literature in emerging fields. For example, multichip technology and ball grid array technology are emerging fields with new developments frequently published these days.

This textbook is now in regular use at several places. Examples are: University of Oslo, Norwegian Institute of Technology in Trondheim, Oslo College, Faculty of Engineering, Royal Institute of Technology in Stockholm and Ericsson Components in Sweden.

The course at the University of Oslo has a web site:

http://www.fys.uio.no/kurs/fys317

Please refer to this page for updates, downloads and other information.

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Oslo, December 1995

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CHAPTER 1

INTRODUCTION

1.1 ELECTRONIC PRODUCTS, TECHNOLOGIES AND PACKAGING

The demands on electronic products vary enormously, depending on their use and their market. Some examples can be given:

- Satellite electronics: One unit, required mean time to failure 10 - 20 years, extreme demands on performance, reliability, low weight, small volume and low power consumption. Repair impossible, very high development- and production cost is acceptable.
- Military electronics: Must tolerate very harsh environments and rough handling. High reliability.
- Computer and telecommunication electronics: Wide range of demands, depending on the products. Maximum performance, short market window, i.e. the marketing and production must start at the right time, delays are very costly.
- Low end consumer electronics, like pocket calculators and watches: Very large market volume, extreme price pressure, low weight and power consumption. Lifetime: A few years. Replace, not repair.

These differences will be reflected in the technology used for the products, how they are designed and produced.

The main technologies used for electronic systems will be described in this course. Each has preferred types of applications, where it is the optimal choice.

Previously the properties of an electronic product were determined by its components, and the interconnection of the components was simple. Today the technology and materials chosen for interconnecting the integrated circuits and passive components may be the critical factor for the performance in a system, as well as for the price, reliability, etc.

"Electronic packaging" is a term describing the physical realisation of the electronic system. It implies the choice of technology and production method. The "packaging technology" starts where circuit design ends, with the circuit diagram. The designers responsible for the packaging will convert the circuit diagram into a physical product that works, can be produced at an acceptable cost, is testable - and repairable if desired - satisfies reliability requirements, etc.

Packaging requires knowledge of many disciplines: electronics, mechanical properties such as strength and thermal behaviour, material properties and -compatibility, chemistry, metallurgy (soldering, corrosion, etc.) production technology, reliability, etc. An understanding of the interplay between the disciplines and properties is most important.

1.2 PHASES IN THE DEVELOPMENT OF A PRODUCT

When a product is being developed the work is divided into different phases. This is to get a systematic process where results can be described and decisions can be made at defined points in time. An example, for large systems, is given in Figure 1.1.

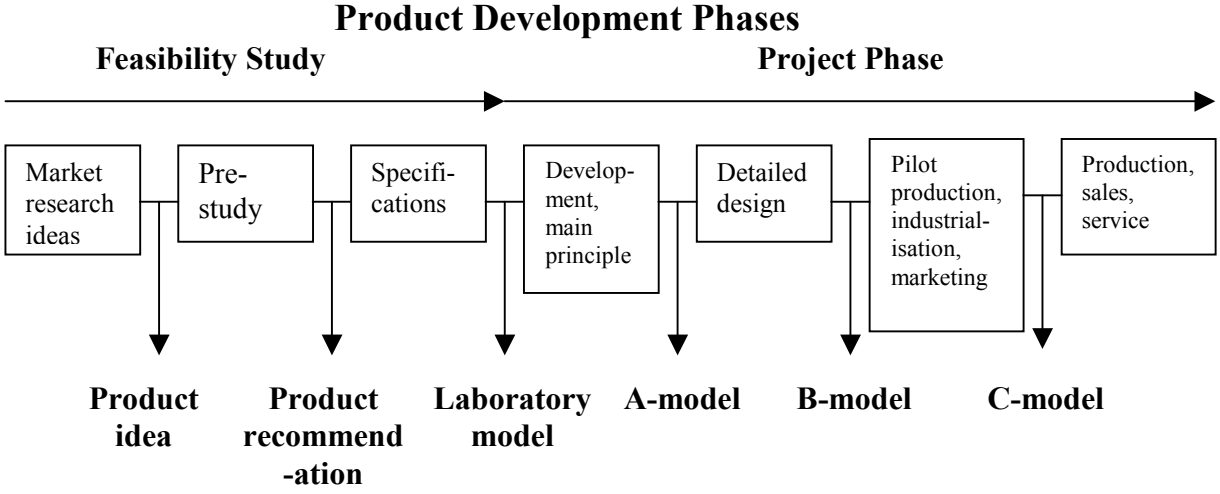


Fig. 1.1: Phases in the development of electronic systems.

The development starts with market investigations, and a description of what properties and specifications the market needs. This is coupled to our own ideas for the new product. The ideas are refined and made concrete during several rounds of studies and evaluation. Then the implementation starts. The main specifications and the main functional blocks are defined, and simulations are performed. Critical parts and details are made in hardware. Several generations of lab models and prototypes are made, evaluated and modified. At each stage the model is made more like the production version. At each stage a new decision is made: Do we still believe there is a market for the product, with the performance and cost we can obtain? It is easy to discontinue development at an early stage, and little money is lost, but it is very costly to discover that the market is not there after full production has started. It may also be concluded that the development is too slow and more resources should be allocated to speed things up.

In the first period expenses for development and industrialisation accumulate. The profit comes later, during the full scale production and sale. After some time the product is outdated in the market, either because new products have better properties, or because new technology makes it possible to produce a similar product significantly cheaper, smaller, etc. The time span that the product can be sold at a profit depends on when we get it on the market. This also determines the total profit we can obtain. In order to make the accumulated profit as large as possible, it is essential to get the product on the market as early as possible. If we can shorten the development time it may justify a much higher development cost. The market life time, "market window" for profitable production of many electronic products is only a few years.

The pressure to reduce the development time has led to the method of "concurrent engineering", in which the various phases of development are partly done simultaneously in an intimate co-operation between various groups of personnel. The main advantage is that this will give an earlier market introduction, giving extended lifetime of the product in the market with larger sales volumes and better prices. The main disadvantage is that this generally needs more resources to coordinate the different concurrent activities and the need for more adjustments of the work pursued.

In practice, most product development projects are partly serial, partly concurrent, based upon an assesment of where concurrent engineering is predicted to be more profitable than serial development.

1.3 LEVELS OF INTERCONNECTION

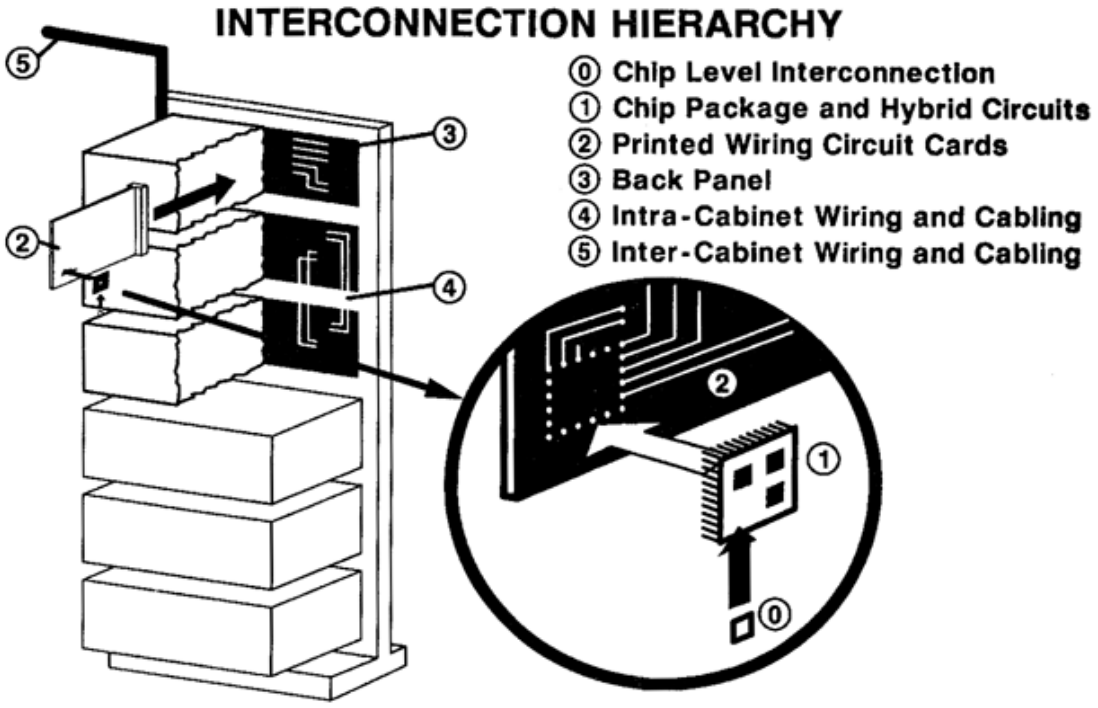


Fig. 1.2: Levels of interconnection in large electronic systems.

In electronic systems we talk about different "levels of interconnection", please refer to Figure 1.2. The lowest, level 0 is the interconnection of integrated, single transistors on a silicon (or gallium arsenide) integrated circuit (IC) chip. The chips communicate by interconnection on level 1, which is a hybrid circuit or a module. Alternatively it can be the wiring inside an IC package, between the chip and the external solder joints of the package. Level 2 is the wiring on a printed circuit board (PCB) where ICs and discrete components are mounted.

The circuit boards in a larger system are mounted on to a back plane, interconnection level 3. Several back planes may make up a cabinet, with internal cabling, level 4. Very large systems have several cabinets with cabling between them, interconnection level 5.

This is the traditional hierarchy of interconnection levels. In some of the multitude of technologies available today, there may be extra levels, or some levels may be missing.

In this course we shall emphasise levels 1 and 2. Level 0 is thoroughly described in many books [1.1] and courses and is outside our scope. The higher levels of interconnection are very product dependent and often represent a minor part of the product value. However, most companies attempt to standardise even here [1.2, 1.3].

REFERENCES

[1.1] See e.g.: S. M. Sze: "VLSI Technology". (McGraw Hill, 2nd. Ed. 1988.)

[1.2] See e.g.: W. L. Harrod and W. E. Hamilton: "The Fastech Integrated Packaging System" (AT&T). Solid State Technology, June 1986, p. 107, and AT&T Technical Journal July/Aug. 1987.

[1.3] Numerous examples of the technology and interconnection hierarchy of electronic products are described in: R. Tummala and E. J. Rymaszewski: "Microelectronics Packaging Handbook". (Van Nostrand, 1989.)

CHAPTER 2

TECHNOLOGIES FOR ELECTRONICS - OVERVIEW

2.1 INTRODUCTION

In this chapter we shall give a survey of the mainstream technologies for hardware realisation of electronic systems. Most of the technologies will be presented in more detail in later chapters. Some, such as application specific ICs, are mentioned here for completeness, and will not be treated in detail.

Electronic systems can be implemented in a number of technologies. The optimal choice of technology or combination of technologies in a system is dependent upon a multitude of factors such as:

- Performance specifications: Speed of operation, accuracy, power consumption, weight, size, etc.
- Operating environment - corrosive media, high temperature, etc.
- Required reliability and lifetime of the product
- Production volume
- Need of reparability
- Cost

In each application the factors governing the choice of technologies for the product will have different importance. We illustrated this with some examples in Chapter 1.

2.2 HOLE MOUNTING TECHNOLOGY ON PRINTED WIRING BOARDS

In printed circuit boards (PCBs) with hole mounting, or insertion technology, the components are mounted by insertion through holes in a laminated substrate, the printed wiring board (PWB), and the pins are soldered to the substrate wiring on the backside. This is the traditional way to build electronic circuits, please refer to Figure 2.1.

The components are interconnected on the laminated substrate by conductor lines that are defined in a single layer or multiple layers of copper foil by etching techniques. The components are discrete devices (resistors, capacitors, transistors, switches, connectors, etc.) or integrated circuits. The dual-in-line package (DIP) having a center-to-center pin pitch of 0.1" (2.54 mm) is the most used package for integrated circuits.

Laminated glass/epoxy is the most used substrate material. This is made of several layers of woven fibreglass sheets in a matrix of epoxy. The substrate conductor pattern is single sided on the simplest printed wiring boards. Most used are double layer boards with conductor pattern on each side of the board and interconnections between the sides by metallised holes, through hole plating. Multilayer boards can also be made, by laminating several layers of glass epoxy substrates with copper conductor patterns on each one.

Fig. 2.1: Hole mounting (insertion-) technology printed circuit board.

Most often the components are mounted on the same side of the board - the primary -, or component side - and are soldered on the secondary - or soldering side of the board. The component insertion is most often done by automatic insertion machines.

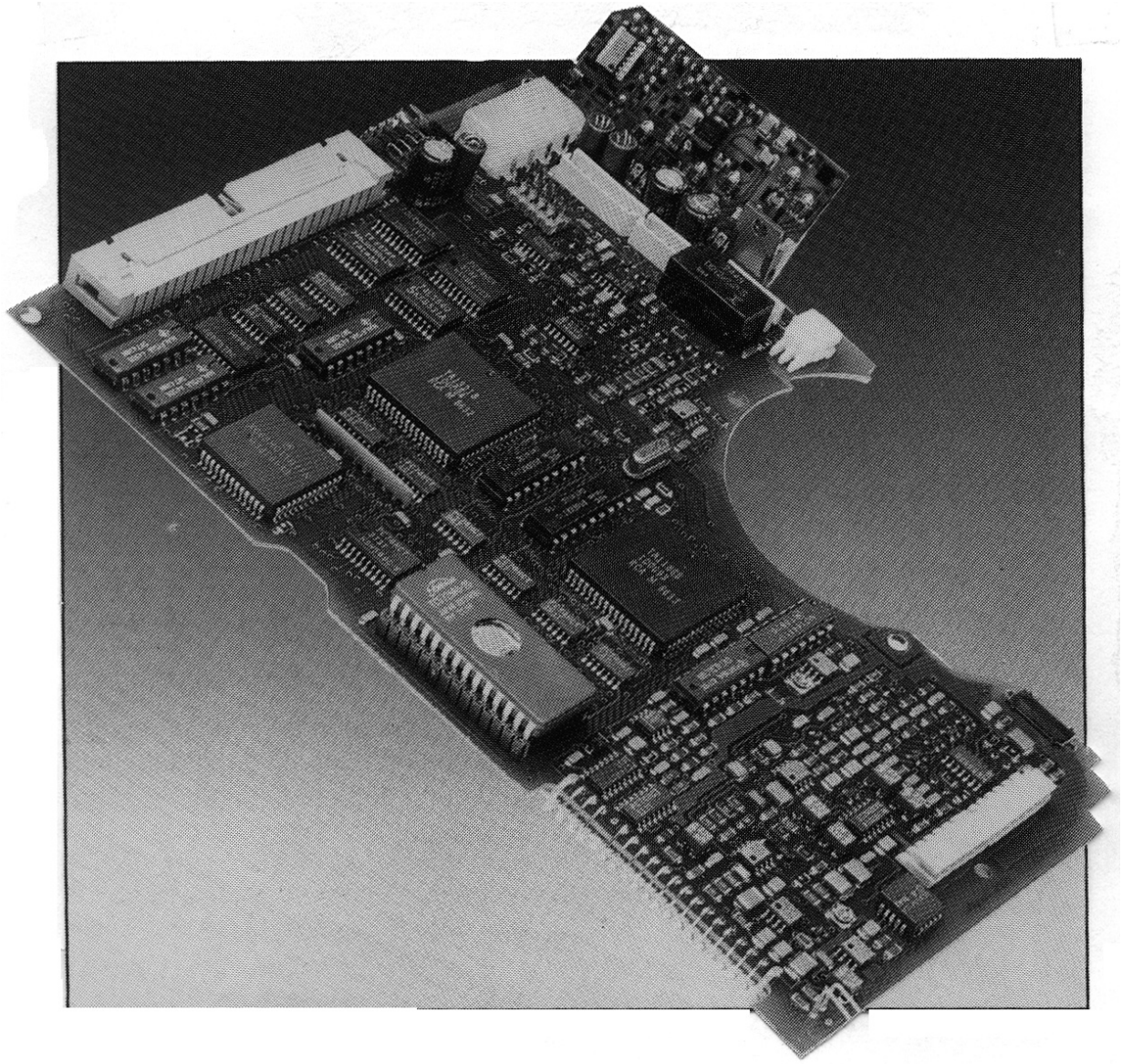


Fig. 2.2: Surface mount technology printed circuit board.

Wave soldering is the dominant soldering method. The printed circuit board with inserted components are passed through a wave of molten solder material. The wave wets the copper soldering pads and the component leads, and solder joints are established as the board leaves the wave. These solder joints make up both electrical contact and mechanical support.

2.3 SURFACE MOUNT TECHNOLOGY (SMT)

In this technology surface mounted devices (SMDs) are soldered to bonding pads on the surface of the substrate, Figure 2.2, in contrast to the hole mounted devices. This technology has been growing very fast since approximately 1980, and is expected to take over the lead from insertion technology as the dominating PCB mount technology, as shown in Figure 2.3. The most striking advantage of surface mount technology compared to insertion technology is the increased packaging density - the devices are smaller and the conductor pattern of the substrate is routed with a finer pitch.

The following are important advantages of surface mount technology:

- Increased packaging density: A surface mount printed circuit boards typically needs only 30 - 70% of the area required for insertion technology. The main reasons for the increased packaging density are more compact devices (Figure 2.4), mounting of devices on both sides of the printed circuit board and the avoidance of area-consuming holes for component insertion.

- Highly automated and cost-effective production: Surface mounted components are well suited for automation, and some of the manufacturing processes of insertion technology are avoided, e.g., sequencing, cutting and bending of component leads - see Chapter 7.

- Improved electrical characteristics: As a consequence of more compact devices and closer placement on the substrate, the parasitic resistances, capacitances and inductances of the interconnection lines are reduced, giving reduced time delays, see Figure 2.5, and noise. Electromagnetic compatibility is also improved, since both electromagnetic radiation and pickup are reduced.

- A potential for higher reliability: For some types of components, we have eliminated one of the material interfaces of the interconnections. Such interconnection interfaces of dissimilar materials are prone to failure. Plated through holes are also susceptible to failure - a reduction of their use also improves reliability.

- Expected lower component costs: Surface mount devices have the potential for being manufactured at lower cost, and this is expected to result in lower prices. (This has not yet fully come into effect - the market mechanisms have so far even resulted in higher prices for some surface mount devices.)

- The most complex circuits of the future will have to be assembled by surface mount technology. This is both because their lead pitch is too low for insertion technology - leaving insufficient room for through holes in the substrate - and because the number of leads is so high that an unacceptable large area would have to be used.

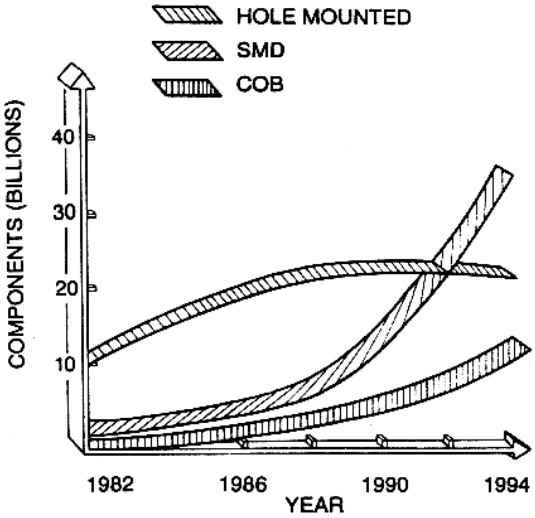
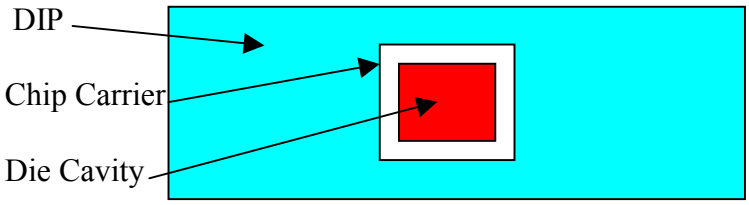


Fig. 2.3: Volumes of different kinds of components used 1980 - 94.



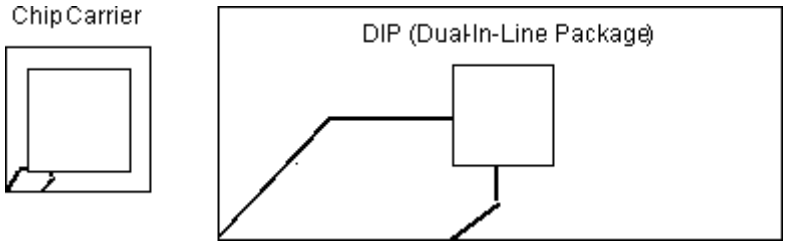
Lead Count	DIP Area : Chip Carrier Area
18	2.7 : 1
24	4.5 : 1
40	5.2 : 1
64	5.6 : 1

Fig. 2.4 a): Size comparison of different package types with approximately the same lead count which can be used for the same size of integrated circuit chip.

There are also some drawbacks with surface mount technology:

- In some cases reduced reliability due to thermal mismatch between substrate and components, because of the shorter component leads, or no leads at all, for surface mount devices.
- Reduced reliability due to higher power dissipation per unit area or volume as a consequence of higher packaging density.
- The components are exposed to high thermal strain during the soldering process in SMT, leading in some cases to reduced reliability.

- More complex test methods need to be implemented, due to smaller components, inaccessible terminals and components on both sides of the board.



Lead Count	Longest Conductor DIP : Longest Conductor Chip Carrier
18	2 : 1
24	4 : 1
40	5 : 1
64	6 : 1

Fig. 2.4 b): The smaller dimensions of surface mount technology packages result in smaller parasitic capacitance and inductance, and therefore improved high frequency performance. Both electromagnetic radiation and electromagnetic susceptibility are also reduced.

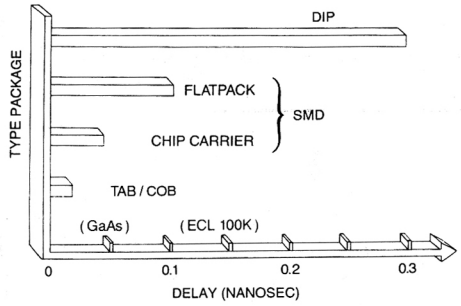


Fig. 2.5: Typical time delay for different component package types, and for Tape Automated Bonding (TAB)/wirebonding of naked chips. Shown on the abscissa: typical time delay on the semiconductor chip with Si ECL (Emitter Coupled Logic) with 100 kgates and GaAs technologies.

Usually, components are placed on both sides of the board when using surface mount technology. This approximately doubles the component density for the whole printed circuit board, when compared to single-sided component placement. However, this calls for a substantially more complex production process. The components on the secondary side can be wave soldered, just like insertion technology processing, but the SMDs must be attached to the board with adhesive beforehand, to stay on the board during soldering, at which time they are hanging underneath the board.

Soldering of the SMDs on the primary side is usually done with reflow soldering. This process is based upon screen printing of solder paste on the solder pads of the board before component placement. This is an adaptation of the general screen printing process used for graphical work of art, etc. The solder paste is squeezed through openings of the printing screen with a "squeegee", see Chapter 8. Next, the components are placed with the leads on the corresponding

solder pads. Thereafter, the assembly is heated until the solder paste melts and forms soldered joints between the component leads and the bonding pads on the substrate.

The supply of SMDs is still incomplete, making it necessary to use of both SMDs and insertion mounted devices - "mixed technology". Using this process, the hole mounted components are wave soldered in the same process step that is used to solder the SMDs on the secondary side of the board.

Both leaded and unleaded SMDs are available. Standard, small-size resistors and capacitors usually have leadless ceramic bodies with solder terminals on both ends. Plastic packaged active devices are normally leaded. Hermetically sealed integrated circuits are specified in some high-end applications, and in these cases ceramic packages are used. The ordinary ceramic packages are leadless, giving rise to mechanical stresses, because the normal glass/epoxy wiring board has a much higher thermal coefficient of expansion (TCE) than the ceramic. This can result in catastrophic failure, after the soldering process, or fatigue stressing of the solder joints after long time in operation.

One way to avoid susceptibility to such strains when using large ceramic packages is to use other types of substrate materials than the normal glass/epoxy laminate.

Surface mount technology is now in widespread use as an established technology in the electronics industry.

2.4 CHIP ON BOARD

Naked silicon chips can be mounted directly on the PWBs or other types of substrates, without encapsulation. This technology is called "Chip on board" (COB) The three most used electrical connection methods between the chip and substrate are visualised in Figure 2.6.

Wire bonding is done in the same way as for chip connection in packages: A gold or aluminium wire is bonded between each bonding pad of the chip and the corresponding pad on the substrate. After mounting and bonding, process steps to establish corrosion protection and mechanical protection of the chip are needed, either by hermetic sealing of the assembled board, or locally by "glob top" sealing with a droplet of sealing material, e.g., epoxy. Wire bonding of bare chips is used in hybrids, most often with a ceramic substrate. Chip on board is also used with glass/epoxy laminates in some consumer applications (pocket calculators, watches, smart cards, etc.), and occasionally in professional applications.

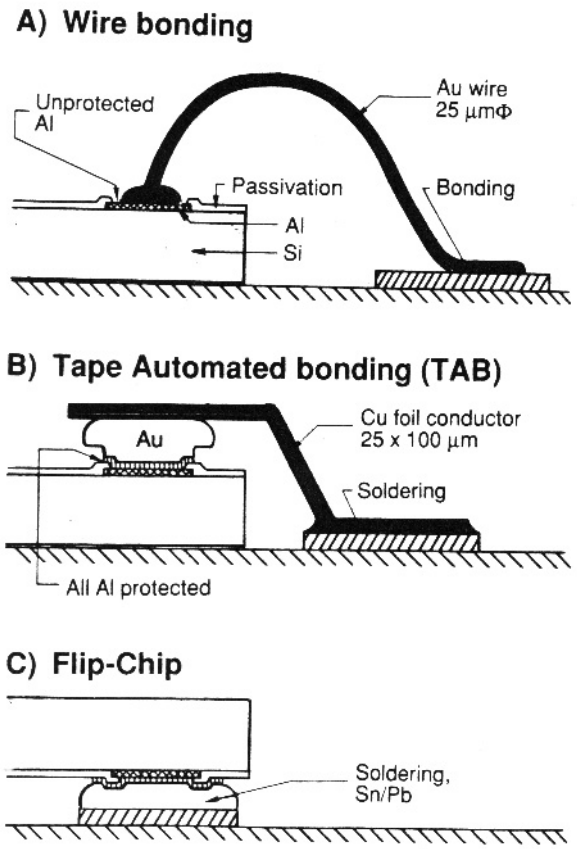


Fig. 2.6: Chip connection by wire bonding, tape automated bonding (TAB) and flip chip, schematically.
- Wire bonding (Chip and wire)
- Tape Automated Bonding (TAB)
- Flip chip.

Tape Automated Bonding (TAB) has a conductor pattern of copper as interconnections between chip and substrate. The conductor pattern is pre-processed from a continuous copper tape on a dielectric carrier film. It is first bonded to gold "bumps" on the silicon chip (inner lead bonding). Mounting of the chip on the substrate is done after cutting off the copper fingers from the tape just outside the chip area. The leads are soldered to the substrate with a specialised tool called thermode ("Impulse soldering") TAB is in widespread use in liquid crystal displays, electronic watches and other high volume consumer products. Other TAB applications are VLSI circuits with a high lead count and other high-end needs.

Flip chip is done by mounting the chip upside down on the substrate, after having deposited solder bumps on all interconnection pads of the chip. The chip is soldered directly onto the substrate, calling for close thermal matching of the chip and substrate. Flip chip technology gives the highest packaging density of the different interconnection methods, It gives excellent electrical characteristics and high reliability when properly used, but it is a very demanding technology both to establish and operate. Initial costs are high, favouring high-volume or high-end applications.

2.5 THICK FILM HYBRID TECHNOLOGY

2.5.1 High temperature thick film hybrid technology

In hybrid technology, chips are interconnected on a substrate with the capability of including passive components such as resistors, capacitors and insulators as an integrated part of the substrate. The hybrid technologies have packaging density between integrated circuit technology and printed circuit board technology.

High temperature thick film hybrid technology generally uses sintered Al_2O_3 (alumina, ceramic aluminium oxide) as the substrate material. Conductors, resistors and insulators are made as thin layers, deposited by screen printing. Use of thick film pastes with low resistivity gives conductors, while pastes with a higher resistivity give resistors. Insulators are made with dielectric pastes. An example is shown in Figure 2.7

Capacitors are screen printed in a three-stage process. First, a conductive layer is printed as the bottom electrode. Thereafter a thin layer of dielectric material is printed, and finally a second conductive layer as the top electrode.

The thick film pastes for conductors and resistors are made up of conductive particles (metals or metal oxides) in a matrix of glass particles, organic filler materials and solvents. After each printing step, the hybrid substrate is dried and heat treated at a high temperature (700 - 900°C) to remove the solvent and the organic vehicles by evaporation. Mean while the glass melts to make up a homogenous mixture of conductive filler in a glass matrix.

Surface mount technology devices are solder to the thick film substrate by reflow soldering. Bare silicon chips can also be used. They are most often mounted with adhesive and electric contact to the substrate is provided by wire bonding.

Features of the high temperature thick film hybrid technology are high reliability and stability of both components and interconnections. The packaging density is also high, with the capability of multilayer conductor patterns and printed components integrated in the substrate area underneath the mounted components.

One of the drawbacks is a relatively high cost. The ceramic substrates are much more expensive than the typical glass/epoxy laminates used for printed circuit boards. Alumina is a brittle material prone to breakage. There may also be a slight warpage due to mechanical stress. Therefore the maximum substrate area is normally limited to 100 x 150 mm or less. Some of the thick film pastes contain precious metals, making them expensive.

Electronics circuits made by high temperature thick film hybrid technology constitute approximately 5% of all electronics when measured in value. Thick

film hybrid manufacturers are typically small and medium size enterprises, serving first the local markets where closeness to the customer is a competitive edge.

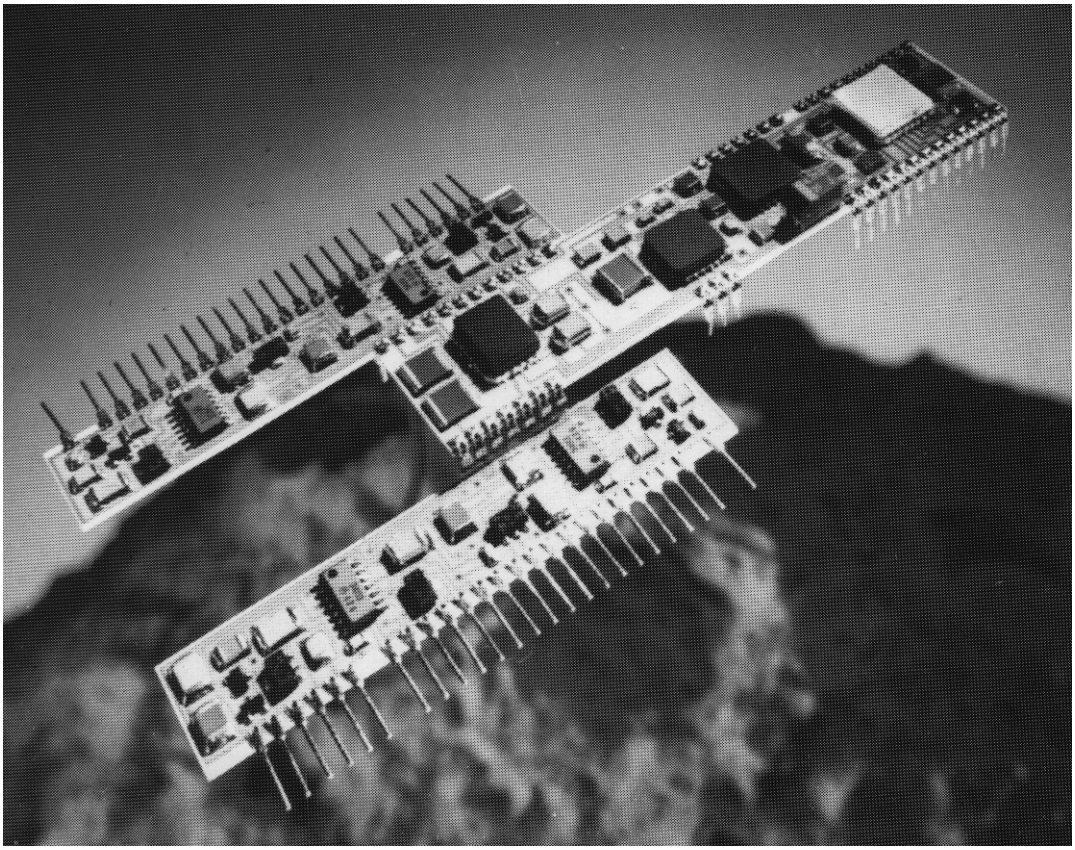


Fig. 2.7: Thick film hybrid circuits.

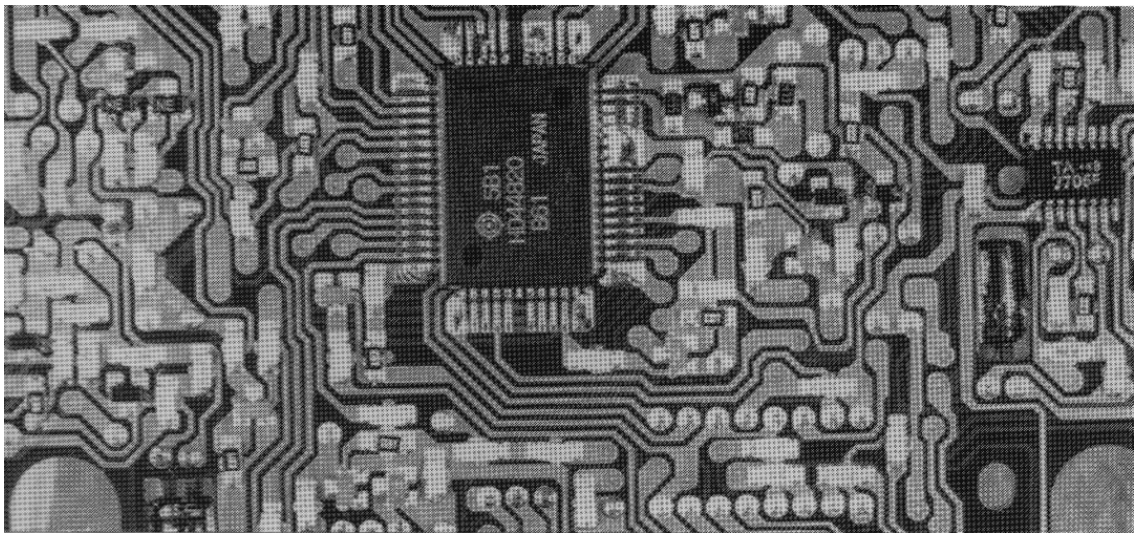


Fig. 2.8: Polymer thick film hybrid circuit.

2.5.2 Polymer thick film hybrid technology

The relatively high cost of the thick film hybrid technology is related to the high temperature processing temperature. The high temperature makes it necessary to use costly ceramic substrates and pastes with precious metals. The high processing temperatures are needed to melt the glass particles in the paste into the matrix of the thick film.

As a way to cut costs, alternative thick film pastes are developed making use of organic, polymer materials instead of glass as matrix material. Such "polymer thick film" pastes can be printed on ordinary glass/epoxy laminates and cured at 150-200 °C. The polymer thick film technology (PTF) can therefore be combined with traditional printed circuit board technology, Figure 2.8. The conducting particles in the pastes are silver, copper or carbon.

PTF has inferior long term reliability compared to traditional hybrid technology and printed circuit board technology, and relatively poor long term stability of the printed resistors. The PTF technology is in widespread use in Japan, especially in consumer applications. So far the PTF technology has not gained widespread use in the western industrialised world.

2.6 THIN FILM HYBRID TECHNOLOGY

In thin film hybrid technology, the conductors, resistors and capacitors are also processed on the substrate, like in thick film technology, but the materials used and deposition techniques are different. The layers are generally well below 1 μm in thickness - this explains the term "thin film". Examples of thin film hybrids are shown in Figure 2.9.

Glass and alumina are the most common substrate materials. Conductors are made by deposition of a thin film of metal, with a typical thickness of 1 μm, most often gold or aluminium. This is done by evaporation or sputtering deposition. These methods are presented in Chapter 3.

The conductor pattern is defined by photolithography, see Chapter 3, and the metal is etched off, using photoresist as etch mask.

The resistors are made in a similar way, using mostly thin film layers of NiCr alloys or Ta_2N.

Insulating layers and dielectric layers for capacitors can be Si_3N_4, SiO_2, etc. They are made by different processes described in Chapter 3.

Traditional thin film circuits are made with one layer of conductor lines and one resistor layer. Recently, the more complicated multilayer thin film hybrid technology has increased in use. With multilayer technology, higher packaging density and higher complexity can be achieved. Electrical characteristics can also be improved by adding separate ground and power supply conductor layers, giving better shielding and possibility to obtain controlled characteristic impedance in high frequency applications, etc.

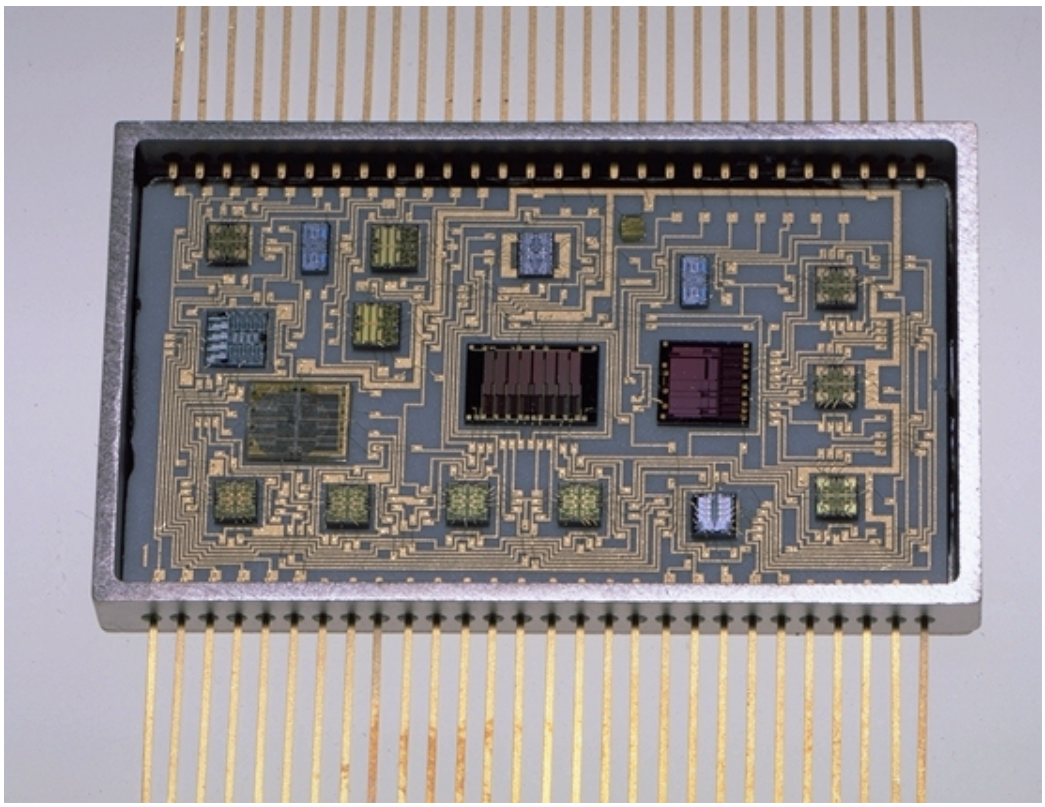


Fig. 2.9: A thin film hybrid circuit.

Most thin film hybrid circuits are using transistors and integrated circuits in the form of bare silicon chips, which are mounted with adhesive and connected by wire bonding. Usually, the complete circuit is packaged in a hermetic metal- or ceramic package.

Thin film technology offers a substantial increase in packaging density compared to thick film hybrid technology. It has excellent electrical characteristics and high reliability. Thin film technology is a specialised technology with relatively few suppliers.

2.7 MULTICHIP MODULES

The continuing increase in maximum operating speed, number of in- and outputs and power dissipation of the semiconductor IC chips requires higher performance in the next level of interconnection. The following needs are of particular importance:

- Fine-line conductor dimensions with short conductor lengths
- Controlled characteristic impedance

- Low thermal resistance to heat sink
- Matched thermal expansion coefficients,
- Etc.

Some of these features can be met by using advanced multilayer printed circuit boards made of advanced materials with special processing. Nevertheless, printed circuit board technology has inherently limited performance. As an example, narrow conductors are difficult to make, and 100 μm a typical minimum line width for printed circuit boards, compared to less than 1 μm for silicon integrated circuits. Conventional thin film, and the most advanced thick film technologies have minimum line widths smaller than that of printed circuit boards, but are still far from the line widths of integrated circuits.

The maximum achievable interconnection density may be defined as the maximum total line length per unit area when using minimum line width and line spacing times the no. of conductor layers, - e.g., cm line length per cm^2 area. There is a "technology gap" in interconnection density between the conventional substrate technologies and semiconductor technology. This is shown in Figure 2.10.

New technologies are emerging to give substrates with increased interconnection density as well as higher speed and improved thermal characteristics for high performance system modules: Multichip module (MCM) technology [2.9]. A multichip module is a structure consisting of two ore more integrated circuit chips electrically connected to a common circuit base and interconnected by conductors in that base.

The main driving forces behind MCMs are the rapid developments in semiconductor technology that make ever more advanced electronic systems possible. Some important trends for the systems development are:

- Smaller critical dimensions, i.e. line widths and distances on the IC and module/PCB.
- Increasing packaging density, i.e. more and more electric functions are possible to implement in a given area or volume.
- Increasing maximum operating speed. (frequency/bit rate)
- Increasing power dissipated per unit area and -volume.
- Increased possibility to realise complex circuit functions with standard hardware in combination with programming software.
- Ever lower price per electrical function.

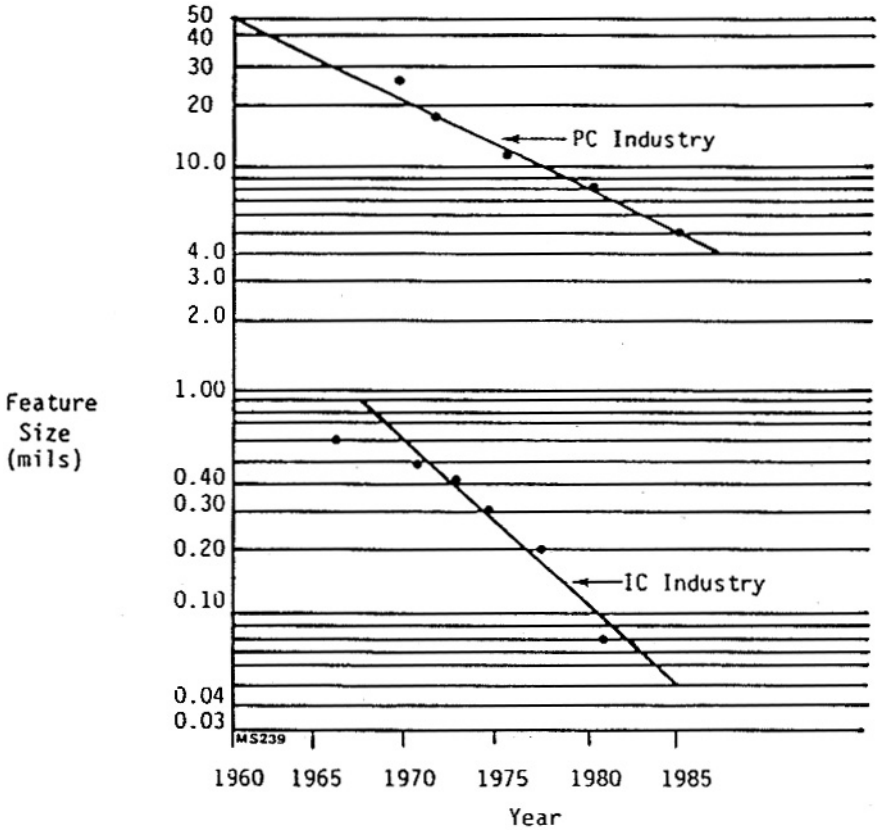


Fig. 2.10: Trends in leading edge fine line pitches for printed circuit boards and integrated circuits from 1965 to 1985 show a widening gap. [2.5].

The MCM technologies make up a family of substrate technologies, which can be divided into the following 4 main groups with the following definitions:

1) MCM-Z (Z for Zero): Modules using no substrates with direct chip-to-chip interconnection and direct chip-to-package connection.
2) MCM-L (L for Laminate): Modules using fine-lined printed wiring board technologies to form the copper conductors on plastic laminate-based dielectrics.
3) MCM -C (C for Ceramic): Modules constructed on cofired ceramic substrates using thick film (screen printing) technologies to form the conductor patterns. ("Cofired" means that the conductors and the ceramic are all heated in an oven at one time) In addition, we include here modules made by thick film printing of conductor pattern on prefired bulk ceramic substrates with no previous conductor pattern.
4) MCM-D (D for Deposited) are modules whose interconnections are formed by the thin film deposition of metals on deposited dielectrics, which may be polymers or inorganic dielectrics. Ceramic, glass, silicon or metal are used as base substrate. The denotion MCM-S is sometimes used for MCM-D on silicon substrate.

Typical achievable interconnection densities for these as well as some other technologies are shown in Figure 2.11. Typical cost per unit substrate area is also included.

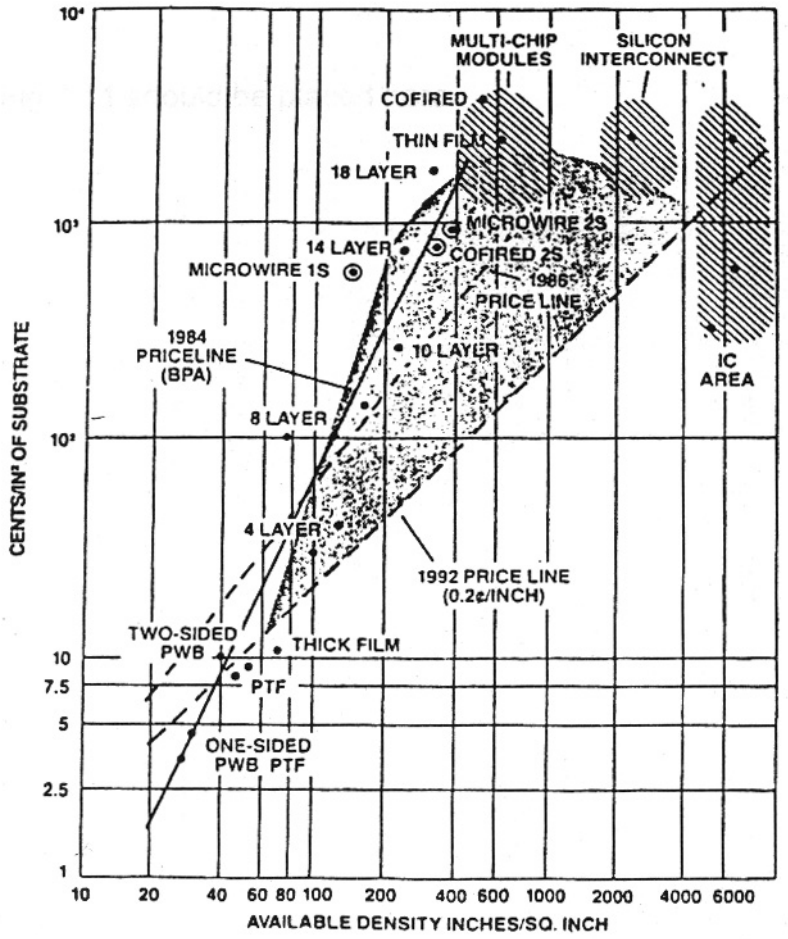


Fig. 2.11: Interconnection density (inches of conductive path length per square inch area) for different kinds of technology. The Y-axis gives the typical price in cents per square inches area for each technology. [2.6]. (The price in the figure can be misinterpreted because the number of circuit functions per area is also strongly dependent of the interconnection density. Therefore, for a given, complex circuit function, the technologies towards the right side usually are the most competitive.)

2.7.1 Multilayer ceramic modules

Multilayer ceramic modules are made by stacking up many layers of unsintered ceramic sheets - "green tape" - with screen printed conductor pattern on one side and metallised via holes as interconnections to the next layer. All the layers are sintered together at high temperature, making up a compact multichip substrate with very good electrical and thermal characteristics.

Packaged surface mount devices or bare IC chips are mounted on top of the substrate, or in recesses - "cavities" - which are made during the ceramic processing, Figure 2.12. This technology is developed from the technology that is used to make ceramic chip carrier packages or multilayer ceramic capacitors.

At present, there is a limited availability of custom designed multilayer ceramic modules. World-wide there are only a few vendors. The technology is expected to get more widespread use when lower temperature materials have been developed, which are compatible with some of the materials and processes used

in thick film hybrid technology. The technology is described in more detail in Chapter 8.

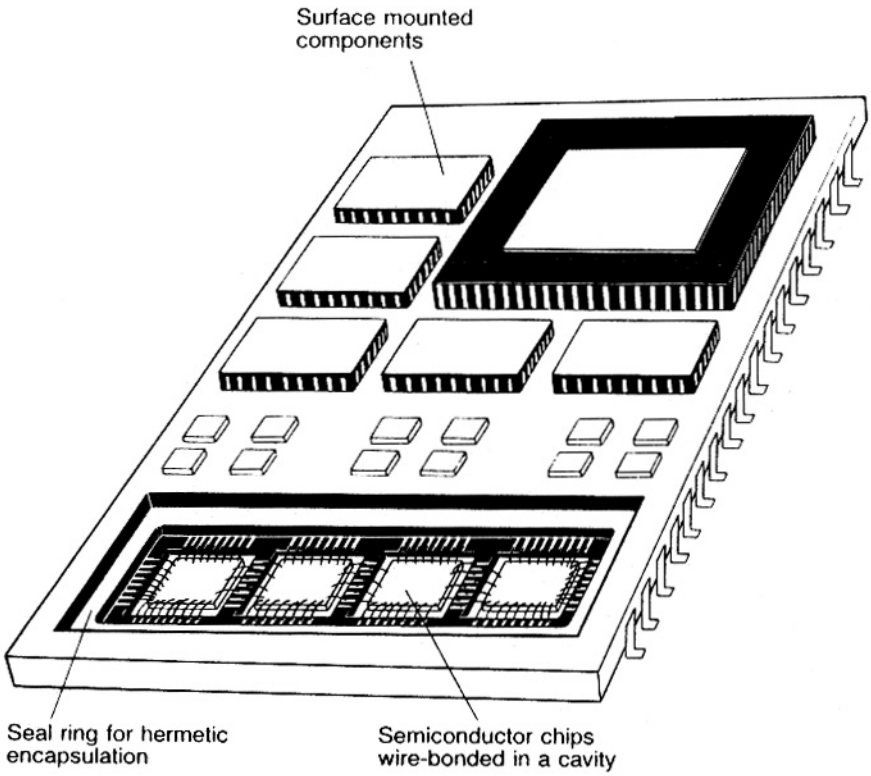


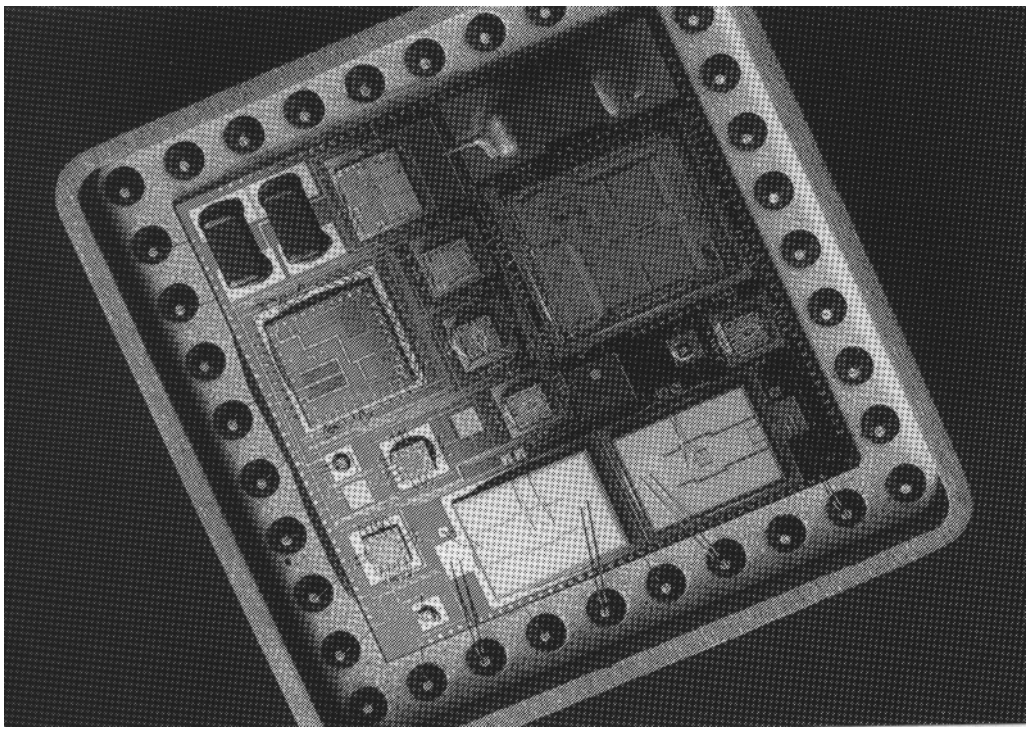
Fig. 2.12: With the multilayer ceramic module it is possible to combine hermetically sealed, wirebonded Si chips in a cavity with lid, soldered, surface mounted packaged chips, and soldered passive components.

2.7.2 Multilayer thin film modules, silicon as a substrate

Silicon multichip modules are using silicon as the substrate material for multilayer thin film modules, see Figure 2.13. Dielectric and conductive layers are deposited on top of the silicon wafer using straightforward or modified thin film technology. Polyimide, that is spin coated, is the most used dielectric. For more details, please refer to Chapter 8. The IC chips are interconnected by wire bonding, tape automated bonding (TAB) or flip chip soldering.

Distinct features of this technology are perfect matching of thermal expansion coefficients of the substrate and the silicon chips, high thermal conductivity, and an industrial infrastructure already established to serve the silicon integrated circuit market. Minimum feature sizes are typically 10 - 20 μm.

The silicon multichip module technology is still immature, with a low market penetration. However, there is a growing R&D activity world-wide giving a technology push. Many successful products are already using the technology, e.g., the VAX 9000 computer from Digital.



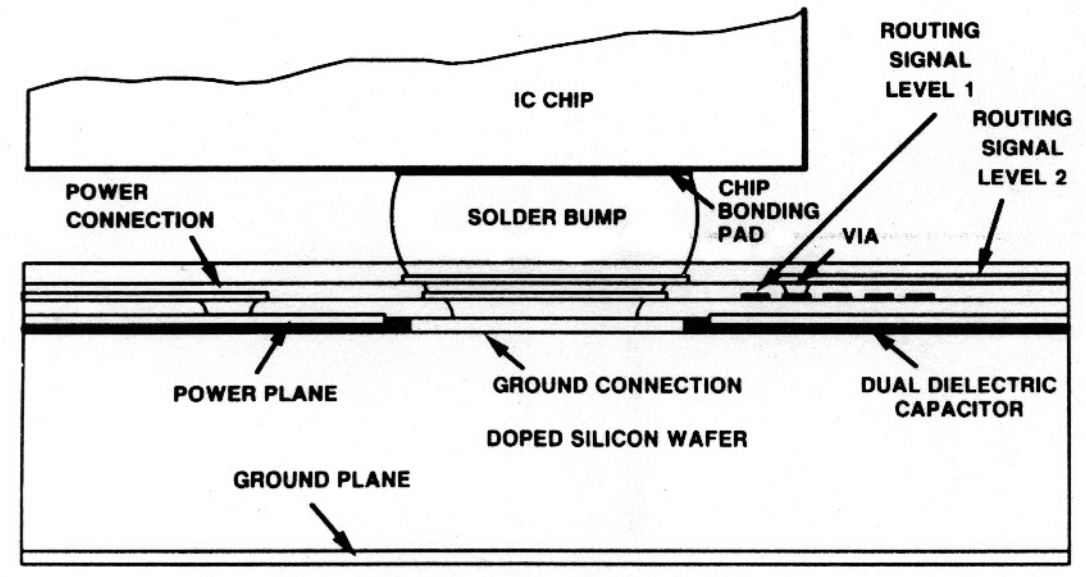


Fig. 2.13: A silicon multichip module. The top figure shows a complete module with wirebonded Si chips and glued passive components, in a hermetic metal package. The bottom figure shows schematically a Si substrate with multilayer thin film and a Si chip mounted with flip chip technology.

Ceramic can be used as an alternative substrate material for multilayer thin film technology, giving approximately the same features.

Multilayer thin film and multilayer ceramic technologies can be combined, implementing each part of the system in the most suitable technology, e.g., silicon multichip technology for the most critical parts calling for high

interconnection density and high speed operation, while the less critical parts are implemented in multilayer ceramic technology.

2.7.3 Wafer scale integration (WSI)

In wafer scale integration [2.8, 2.9] all the integrated circuits constituting the module are interconnected on the same wafer - in practice integrated into one very large integrated circuit using the whole wafer area. Due to defects originating both from the substrate and the processing, redundancy must be built into the circuitry, allowing for elimination of defect circuit parts by choosing only operating parts. This can be achieved by some kind of decoupling scheme, e.g. laser cutting.

So far, WSI technology is not been used commercially to any extent, in spite of large R&D efforts. The production yield problems have not been solved.

2.7.4 Silicon sensor technology

Another specialised application of silicon substrate technology is in silicon sensor technology.

Silicon sensor technology takes advantage of the following features of silicon:

- Si is an excellent mechanical material with high strength and almost perfect elasticity until it breaks.
- The physical properties of Si permit many sensor principles.
- Si is an excellent electronic material, and the sensor elements can be combined with integrated electronics, giving "smart sensors".
- Three-dimensional structuring can be done by anisotropic etching, etc. This is a new field called micromechanics in silicon.
- The Si microelectronics manufacturing technology infrastructure can be adapted.

2.8 APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASICs)

Usually, an electronic designer will build up his design using standard devices, with specifications listed in the data sheets of the supplier.

However, integrated circuits can be tailored for each specific application, either by designed modification of pre-processed chips or by full custom design.

2.8.1 PROM, PAL, GAL, field programmable gate arrays

Programmable integrated circuits are a class of chips that the designer can modify by programming standard chips. Programmable memories are the most used type of such circuits: Programmable Read Only Memory (PROM), Erasable PROM (EPROM), etc., are supplied as standard chips and programmed

more or less permanently. One way of programming is cutting, or "defusing", of interconnections by electrical voltage pulses.

This principle has been adapted for logical circuits in Programmable Array Logic (PAL). The initial standard chip is made out of an array of logical AND and OR elements, all interconnected. By defusing, the specified logical function can be made, see Figure 2.14. Both the PROM and the PAL concepts have been developed by Monolithic Memories, and are implemented in bipolar technology.

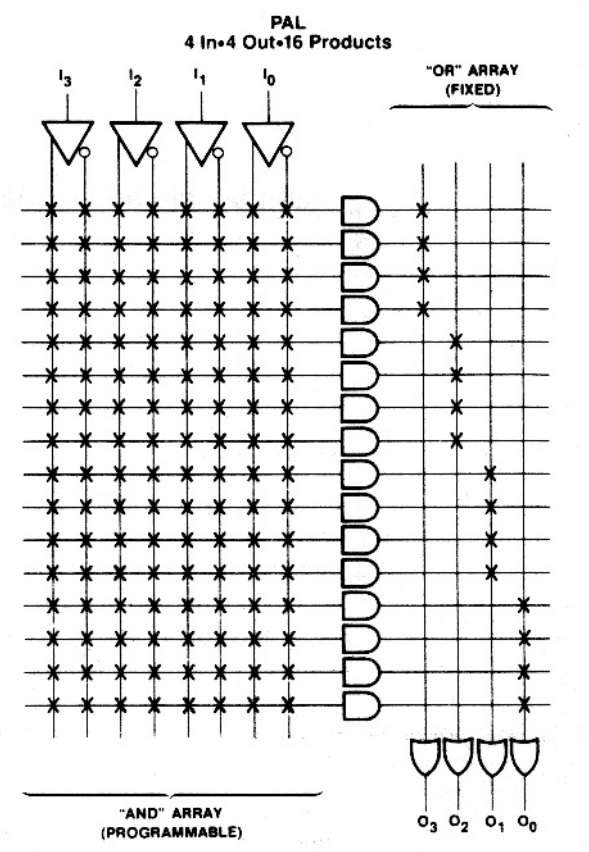


Fig. 2.14: The logical structure of a PAL (Programmable Array Logic). Programming is done by disconnecting elements in the "AND" array [2.12].

Generic Array Logic (GAL) uses CMOS technology. Here the interconnection network from the standard logical array is established by electrical programming of floating MOS switches. This way of non-destructive programming gives the technology high flexibility, since reprogramming is straightforward. GAL was introduced by Lattice Semiconductor Corporation.

The "field programmable gate array" consists of two chips. The main chip has configurable logic blocks as well as an on-chip random access memory. The other chip is a PROM. The user programs the PROM according to the desired circuit function. At start-up the PROM program is loaded into the RAM that configures the logic array for the specific application. Program errors or modifications in the application can be handled by programming a new cheap PROM, whereas the valuable main chip may be used for any number of applications. This powerful concept is used in the devices from XILINX [2.13], and similar principles are used by several other companies.

2.8.2 Custom design ICs

During the last 10 years, custom design of integrated circuits (silicon or GaAs monolithic integrated circuits) has become increasingly common for the most critical part of electronic systems. After the design by the user or special design houses, the chips are fabricated by semiconductor processing companies ("silicon foundries").

Custom designed ICs are classified in three main types:

- Gate array custom design
- Standard cell custom design
- Full custom design

A gate arrays is made up of a prefabricated layout of transistors and basic logical elements. The customer needs only to design the conductor pattern in the way that meets the specified electrical functions. Since most of the wafer processing steps are common to all users and are manufactured as a high volume process, this method is inexpensive, and the "personalisation" is fast. However, it gives limited electrical performance and limited design flexibility.

For standard cell custom design the silicon foundry has available a set of predesigned and characterised electrical building block - the standard cells - that can be combined to give the desired function of the chip. The standard cell library is available to the customer as computer aided design (CAD) layouts and/or net lists with documentation of function and performance. In this way the customer has fast access to complex and debugged circuit blocks, saving time and costs.

Full custom design is performed by designing the circuits in full detail down to the transistor level. This makes it possible to optimise electrical performance and minimise the silicon chip area for the particular application. Properly used, full custom designs give the best electrical characteristics and highest packaging density, but it requires a strong design know how, advanced equipment, and it is time consuming. Therefore, this design method is best suited for high volume or high-end applications.

In practice, many designs can be classified somewhere between standard cell custom design and full custom design; whenever appropriate, standard cells are used, but in combination with full custom design of critical parts where availability or performance of the standard cells is insufficient.

A rough outline of the design methodology for a custom designed integrated circuit is as follows [2.11]:

The semiconductor chip processing company (the foundry) supplies design rules for each of their processes available for custom designed ICs. The rules are supplied in hard copy or implemented in CAD tools. The customer generates in his CAD system a schematic capture, he simulates the functionality and makes a net list describing the circuit elements and interconnections. Alternatively he designs a graphical layout describing each of the photolithographic masks used during wafer processing.

The foundry makes the masks and fabricates chip prototypes that are packaged and sent to the customer for evaluation. For gate arrays, most of the processing is already done, and only the masks describing the custom designed interconnection patterns are made specifically for each customer. At receipt of prototypes, the customer tests functionality and other specifications. If needed, design errors are corrected, modifications are made and new prototypes fabricated. When specified performance is achieved, full scale production is done. Modern ASIC design is impossible without powerful computer aided design tools. One class of tools focuses on maximising the automation of the design cycle - this class of tools is named silicon compilators.

At the present time there are only a few major semiconductor chip processing companies that offer ASIC processing services world wide, while system companies and local or small design companies focus on having the design knowledge in-house. This is because of the extremely high cost of building, updating and operating a modern silicon processing line. On the other hand, IC design requires much smaller resources and is considered by most system companies as strategically important.

The industry structure in Norway illustrates this. Norway has no semiconductor integrated circuit processing company, but some 20 or 30 % of the Norwegian electronics producing companies have designed ASICs during the last years.

2.9 OPTOELECTRONICS PACKAGING TECHNOLOGY

Optoelectronics is a promising, fast-growing technology, partly replacing purely optical systems or electrical systems, and partly opening up new applications. The solid state laser and the low loss optical fibre are its key elements. Achievable frequency bandwidths in optoelectronics systems are several orders of magnitude higher than in purely electrical systems. We find typical applications in telecommunications systems, e.g. optical fibre networks, high speed computer networks, video cameras, etc.

Optical interconnect inside electronics systems, i.e. replacement of conductive paths with optical paths can give enhanced performance, such as higher speed, galvanic isolation, etc. [2.16]. This requires new methods and materials for the packaging, in order to maintain both electrical and optical performances. For example, packages must have optical input/output paths, such as optical windows in lasers and detectors or fibre interconnections for optical interconnects, without interfering with electrical characteristics. Examples of optoelectronic components and interconnection technology are shown in Figure 2.15

2.10 TECHNOLOGY TRENDS

The development in semiconductor technology makes ever more advanced electronic systems possible. Some important trends for the systems development are:

- Smaller critical dimensions, i.e. line widths and distances on the IC and module/PCB

- Increasing packaging density, i.e. more and more electric functions are possible to implement in a given area or volume
- Increasing maximum operating frequency/bit rate
- Increasing power dissipated per unit area and -volume
- Increased possibility to realise complex circuit functions with standard hardware by programming software
- Ever lower price per electrical function

The established technology cannot satisfy the needs and requirements, and new technology always appears. It seems as if we hit physical limits on many fronts [2.14, 2.15]. However, earlier, when such limits have appeared, new ideas and new principles have been found. This will probably also happen in the future and will make the field of microelectronics dynamic and exciting in the future, for scientists as well as for users.

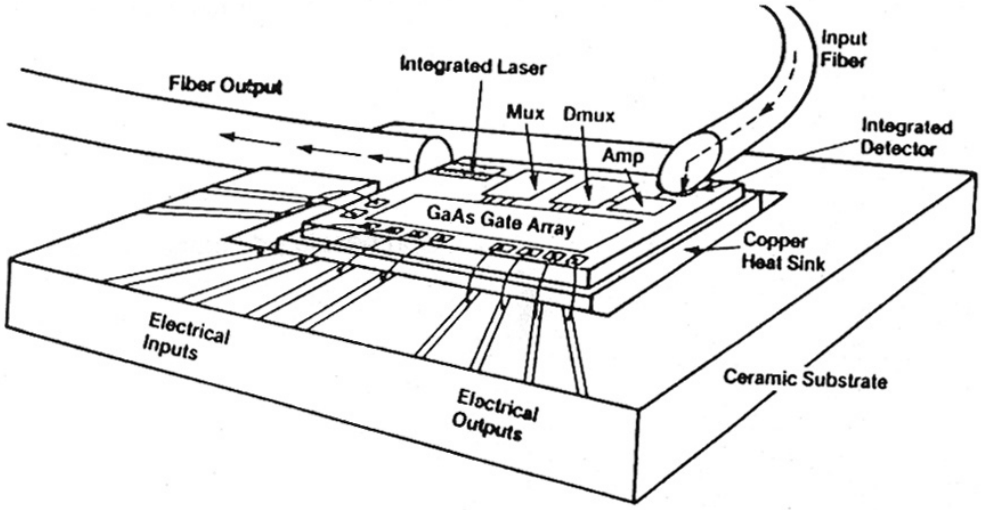
2.11 SELECTING THE OPTIMAL TECHNOLOGY

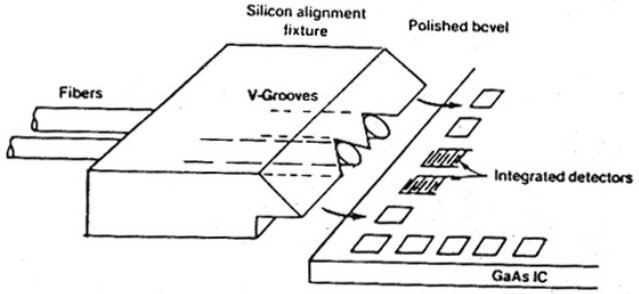
All the technologies described in this chapter have their specific advantages and drawbacks, most of which will be dealt with in more detail later. Each technology has applications where they are well suited. Starting up a product development, it is important to make technology assessments early, to pick the most suitable technology and make the design optimised for production with the chosen technology or technologies. Then the development costs can be minimised, production can be done cost-effectively, and a product with high performance/price ratio is put on the market as fast as possible.

The technology assessment should be done based upon detailed system specifications and other requirements for the product:

- Electrical specifications
- Reliability and lifetime
- Operating and environment conditions for the product. Temperature, vibrations, electromagnetic radiation, etc.
- Production volume
- Available area/volume
- Maintenance and reparability considerations
- Acceptable price/cost level
- Time-to-market
- Etc.

System level computer modelling [2.16] may be of help in the analysis and comparisons of technology choices.





Electrooptic coupler

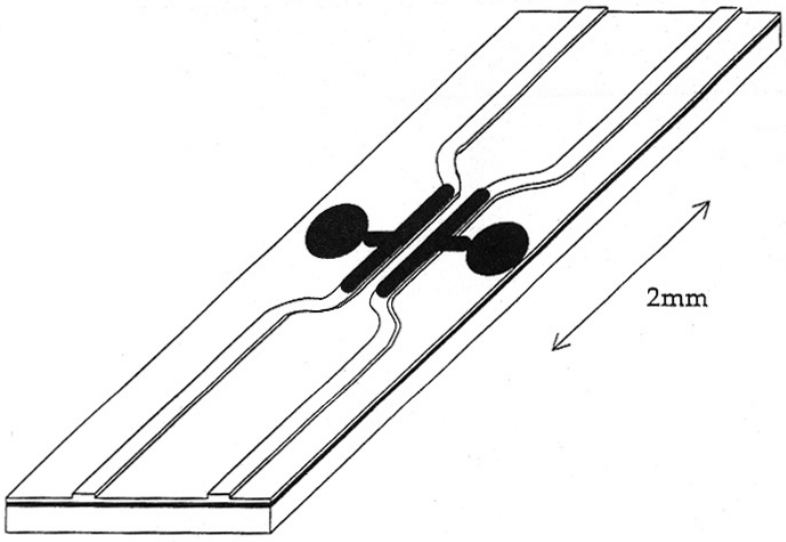


Fig. 2.15: Optoelectronics: The top figure shows different electronic and optical electronic functions in the same circuit. The middle figure shows one way to couple incoming light by reflection in 45 degree angle fixture ends, and use of a Si fixture with anisotropically etched alignment grooves. The bottom figure illustrates manipulation of light in a coupler with "light guides". By electric signals a variable interference and coupling between the two light guides can be achieved.

Traditional design philosophy took it for granted that a product should be designed based upon an established assortment of standard components interconnected with traditional printed circuit board technology. Today, a system design approach has to be taken, considering from the start the combination of electronics, mechanics, production, test, repairs, and maintenance. Selecting the technologies that give an optimal solution. This process is multidisciplinary and should involve personnel from all these fields, as well as people with intimate knowledge of the application and market- and user preferences. This interdisciplinary group should also be involved in the whole development cycle, to make optimised use of the chosen technologies.

2.12 FUTURE TRENDS FOR USERS AND DESIGNERS OF ELECTRONIC SYSTEMS

Some main trends in the evolution of technology for electronic products can be observed:

- The assortment of standard components is ever increasing, with availability of more and more complex integrated circuits and modules as standard components, with improved performance. Programmable standard components can be customised to specific applications.

- Emerging of industrial standards for specifications and documentation of standard technologies for easier communication between users, designers, producers, and subcontractors, with effective communication network based upon information technology. This infrastructure simplifies both bidding procedure and production by subcontractors, with decreasing importance of geographical closeness.

- Advanced technologies are emerging offering a broader range of features from high-end specifications to low cost than available in traditional technologies.

- Such advanced niche technologies are more specialised, making it inconvenient for most companies to have it as an in-house capability. This opens up a market with specialised subcontractor services.

- New product development should take technology assessment as an important task to be dealt with in detail with system optimisation in focus, all the way the initiation of the development.

- The market lifetime of the product is getting shorter and shorter, and therefore time-to-market must be minimised to obtain sufficient market penetration.

These factors have had a large impact of the industry structure of the electronics business the last years - a restructuring that will probably continue for at least the next 5 - 10 years.

REFERENCES

[2.1] S. M. Sze: "Physics of Semiconductor Devices". (John Wiley, 2nd Ed. 1981.)

[2.2] S. M. Sze: "VLSI Technology". (McGraw Hill, 2nd. Ed. 1988.)

[2.3] As an example: W. L. Harrod and W. E. Hamilton: "The Fastech Integrated Packaging System" (AT&T). Solid State Technology, June 1986, p. 107, and AT&T Technical Journal. July/August 1987.

[2.4] A multitude of examples of interconnection and packaging in established electronic products are given in: R. Tummala and E. J. Rymaszewski: "Microelectronics Packaging Handbook". (Van Nostrand, 1989.)

[2.5] BPA (Technology and Management) Ltd: "Compass Programme", 1986, Vol. 3.

[2.6] G. Messner: "Derivation of Uniform Interconnection Density Analysis". Proc. 7th Int. Electronics Packaging Conf., Boston, Nov. 1987, p. 833.

[2.7] IBM J. of Res & Dev. 1983; Scientific American 1983.

[2.8] As an example: S. K. Tewksbury and L. A. Hornak: "Wafer Level System Integration: A Review". IEEE Circuits and Devices Magazine, 1989.

[2.9] R. Wayne Johnson et al., eds.: "Multichip Modules - Systems Advantages, Major Constructions, and Materials Technologies". Selected reprints, IEEE Press 1991.

[2.10] A. Hanneborg og P. Ohlckers: "SIs smarte silisiumsensor". Elektro, nr. 15 - 1985. (In Norwegian)

[2.11] Y. Lundh, O. Søråsen, M. Bayegan og J.E. Pedersen: "Konstruksjon av integrerte kretser" (Universitetsforlaget, 1983).(In Norwegian)

[2.12] Monolithic Memories: "PAL Handbook".

[2.13] Xilinx handbook: "The Programmable Gate Array Databook."

[2.14] R. C. Landis: "Electronic Packaging for the Year 2000". Proc. IEPS 1988, p. 535.

[2.15] J. D. Meindl: "Opportunities for Gigascale Integration". Solid State Technology, Dec. 1987, p. 85.

[2.16] H. B. Bakoglu: "Circuits, Interconnections and Packaging for VLSI" (Addison-Wesley, 1990).

CHAPTER 3

MATERIALS AND BASIC PROCESSES

3.1 INTRODUCTION

In this chapter we have included several general topics as a background for the later chapters. We will discuss material properties for important materials, processes that are used in several types of technology and methods for assembly or interconnection of components to achieve mechanical and electrical contact.

MATERIALS

Metals, semiconductors, inorganic insulators, such as ceramics and glasses and organic materials and plastics are important for various areas of usage in electronic systems. There are tough demands on the electrical, mechanical, chemical, and metallurgical properties, as well as low flammability, corrosion resistance, stability and compatibility with other materials used. Weight, price and ease of processing are important. Low absorption of moisture may be of great importance for specific areas of applications where the materials must tolerate harsh environments and tough use.

We shall look at selected properties and applications for certain important materials. Among these materials are plastics, which are steadily increasing in importance. Most electronic engineers know little of their properties and behaviours. The tables 3.1 a)..e) give some general properties for many types of materials [3.1, 3.2].

3.2 INORGANIC MATERIALS

3.2.1 Metals

Metals are used for their good electrical and thermal conductivity. They also serve as mechanical construction materials. Copper is a particularly important element in electronics because of its very high electrical and thermal conductivity and is used in foil conductors, lead frames in component packages, thick film conductor materials, heat sinks in power electronic modules, etc. Aluminum has similar advantages, as well as low weight and price. Aluminum is commonly used for mechanical carrying structures, heat sinks, cooling towers. In semiconductor components it is used for bonding wires and circuit metallisation, etc.

The pure metals have thermal coefficient of expansion (TCE) 15 - 30 ppm per degree centigrade, much higher than the semiconductors and most ceramics. Chemical reactivity varies from very low (Noble metals like gold and platinum), to highly reactive. Mechanical properties also vary widely: pure gold, silver and indium are soft, while some of the others are very hard. Mechanical properties may depend on the processing (heat treatment, rolling, etc.), and change with small amounts of additives from other elements.

Table 3.1 a): Properties of some important materials in electronics: Conductors[3.1].

Metal/Conductor	Melting Point [°C]	Electrical Resistivity [10^{-8}Ohm•m]	Thermal Exp. Coeff. [10^{-7}/°C]	Thermal Conductivity [W/m·°K]
Copper	1083	1.7	170	393
Silver	960	1.6	197	418
Gold	1063	2.2	142	297
Tungsten	3415	5.5	45	200
Molybdenum	2625	5.2	50	146
Platinum	1774	10.6	90	71
Palladium	1552	10.8	110	70
Nickel	1455	6.8	133	92
Chromium	1900	20	63	66
Invar	1500	46	15	11
Kovar	1450	50	53	17
Silver-Palladium	1145	20	140	150
Gold-Platinum	1350	30	100	130
Aluminium	660	4.3	230	240
Au-20%Sn	280	16	159	57
Pb-5%Sn	310	19	290	63
Cu-W(20%Cu)	1083	2.5	70	248
Cu-Mo(20%Cu)	1083	2.4	72	197

Table 3.1 b): Properties of important materials in electronics: insulators [3.1].

Non Organics	Relative Dielectric Constant	Thermal Exp. Coefficient [10^{-7}/ °C]	Thermal Conductivity [W/ m·°K]	Approximate Processing Temp.[°C]
92% Alumina	9.2	60	18	1500
96% Alumina	9.4	66	20	1600
Si3N4	7	23	30	1600
SiC	42	37	270	2000
AlN	8.8	33	230	1900
BeO	6.8	68	240	2000
BN	6.5	37	600	>2000
Diamond - High Pressure	5.7	23	2000	>2000
Diamond - Plasma CVD	3.5	23	400	1000
Glass-Ceramics	4-8	30-50	5	1000
Cu Clad Invar (10%Cu)/ (Glass Coated)	-	30	100	800
Glass coated Steel	6	100	50	1000
Organics				
Epoxy-Kevlar(x-y) (60%)	3.6	60	0.2	200
Polyimide-Quartz (x-axis)	4.0	118	0.35	200
Fr-4(x-y plane)	4.7	158	0.2	175
Polyimide	3.5	500	0.2	350
Benzocyclobutene	2.6	350-600	0.2	240
Teflon (™DuPont Co.)	2.2	200	0.1	400

Table 3.1 c): Properties of ceramics, Si, Si_3N_4 and SiO_2 and polyimide.

Characteristic	Al_2O_3	AlN	SiC	Si	SiO_2	Si_3N_4	Polyimide
Specific Resistance (Ohm•cm)	$>10^{14}$	$4x10^{11}$	10^{13}	10^{-4} 10^{+4}	10^{6}	10^{12}	10^{16}
Relative Permittivity	9.8	10	15 45	11.9	3.9	7.5	3-4
Thermal Conductivity (W/m °K)	10 35	140 170	270	150	1.5	10 40	0.4
Thermal Expansion Coefficient (10^{-6}/°K)	5.5	2.65	3.7	2.6	0.3 0.5	2.5 3	20 70
Breakdown Field Strength (V/cm)	10^{5}	10^{5}	700	10^{5}	10^{6} 10^{7}	10^{6} 10^{7}	10^{6}
Loss Factor (tan δ)	$3x10^{-4}$	$5x10^{-4}$ 10^{-3}	$5x10^{-2}$	$4x10^{-3}$ $4x10^{-2}$	$3x10^{-2}$	–	–
Modulus of Elasticity (kN/mm^2)	300 380	300	380	170	70 72.5	280 320	3

Table 3.1 d): Elastic modules and thermal conductivity of some materials [3.1].

Material	Modulus of Elasticity E [GPa]	Thermal Conductivity k [W/cm °C]	Application
90-99% Al2O3	262	0.17	Substrate
Beryllia (BeO)	345	2.18	Substrate
Common Cu alloys	119	2.64	Leadframe
Ni-Fe Alloys(42 alloys)	147	0.15	Leadframe
Au-20% Sn	59.2	0.57	Die bond attach and lid sealant
Au-3% Si	83	0.27	Die bond attach
Pb-5% Sn	7.4	0.63	Flip chip bonding
Silicon	13.03	1.47	Electronic circuit
Au	78	3.45	Wire metallurgy
Ag-loaded epoxy	3.5	0.008	Die bond adhesive
Epoxy (Fused silica filler)	13.8	0.007	Moulding Compound

Table 3.1 e): Properties of low temperature ceramics [3.2, pages 461 and 465].

Burnout and firing conditions

System	Matrix	Filler	Metallisation	Burnout [$^oC/h$]	Firing [$^oC/h$]	Atmosphere	Shrinkage [%]
High-temperature cofired ceramic							
IBM	Alumina	…	Molybdenum	…	1560/33	H_2/N_2	17
Low-temperature cofired ceramic							
Asahi glass	Ba-$Al_2O_3SiO_2$-B_2O_3	Al_2O_3 Forsterite	…	…	900/1	Air	12
DuPont	Alumina silicate	Al_2O_3	Silver, Gold	350/1	850/0.3	Air	12
Fujitsu	Borate glass	Al_2O_3	Copper	…	950 to 1000/-	Reducing	.....
Matsushita	0.35$NaAlSi_3O_8$-0.65$CaAl_2Si_2O_8$	…	Copper	550/4(a) (in air)	900/0.3	Nitrogen	.....
Murata	BaO-B_2O_3-Al_2O_3-CaO-SiO_2	....	Copper	…	950/-	Reducing	13.5
Narumi	CaO-Al_2O_3-B_2O_3-SiO_2	Al_2O_3	Silver, gold(top)	…	880/0.3	Air	16
NEC	Lead borosilicate	Al_2O_3	Silver, palladium	…	900/-	Air	13
Shoei	$BaZr(BO_3)_2$	SiO_2	Copper	600/- (in air)	980/2.5	Nitrogen	12
Taiyo Yuden	CaO-MgO-Al_2O_3-SiO_2-B_2O_3	…	Copper	…	950/-	Reducing	.....

(a) Followed by a reduction step in N_2/H_2, 350°C, 0.3h

Physical properties

System	Dielectric constant	Dissi-pation factor	Insulation resistance, [Ohm•cm]	Coefficient of thermal expansion [10^{-6}/°K]	Thermal Conduc-tivity [W/m°K]	Fracture trength [MPa]	Breakdown voltage [kV/mm]
High-temperature cofired ceramic							
IBM	9.4		$>10^{14}$	6.5	16.7	275	
Low-temperature cofired ceramic							
Asahi glass	6.3	0,001	…	3,8-6,8	…	245	…
DuPont	7.8	0,002	$>10^{13}$	7,9	2,9	206	40
Fujitsu	4.9			4,0	…	…	50
Matsushita	7.4	0,002	10^{14}	6,1	2,9	245	
Murata	6.1	0,0007	$>10^{14}$	8,0	4,2	196	20
Narumi	7.7	0,0003	10^{14}	5,5	2,5	196	88
NEC	7.8	0,003	$>10^{14}$	7,9	…	343	…
	3.9	0,003	$>10^{13}$	1,9	…	137	…
Shoei	7.0	0,001	$>10^{14}$	7,7	3,3	196	…
Taiyo Yuden	6.7	…	…	5,8	6	245	…

Alloys have poorer conductivity, both electrical and thermal. They are used to achieve better mechanical properties, or often to custom-tailor a desired thermal expansion coefficient: Invar, Table 3.1 a), (64 weight % Fe, 36 weight % Ni) has TCE of only 1.5 ppm/°C, Kovar (53 Fe:17 Co:29 Ni) has 5.3 ppm/°C, matched to glass, "Alloy 42" (42 Ni: 58 Fe) has 4.9 ppm/°C, close to that of silicon, and it is used for lead frames in component packages, etc. Alloys also have a lower melting point than the elements in them and they are used as soldering metals.

Most common is the solder metal that is a eutectic mixture of tin (approximately 63 %) and lead (37 %). Figure 3.1 shows the phase diagram for Sn/Pb.

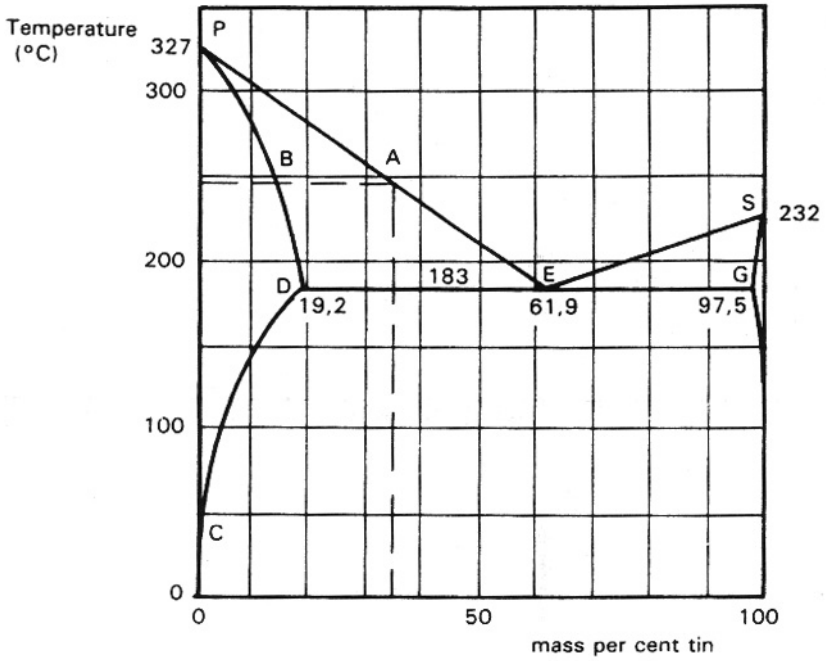


Fig. 3.1: Phase diagram for Sn/Pb. The eutectic mixture 63%/37% has a melting point of 183°C [3.13].

3.2.2 Semiconductors

The semiconductors that are most common, Si and GaAs, also have high thermal conductivity. They have very low TCE. Their electrical conductivity may be changed over many orders of magnitude by controlled doping. Silicon can be "machined" in very interesting ways by anisotropic etching. It has many exciting possibilities as a "mechanical" material. The material keeps its elastic properties practically until it breaks. It is also important for Si that it makes an oxide with very good properties, SiO_2 [3.3].

3.2.3 Inorganic insulators, ceramics and glasses [3.1, 3.2, 3.4, 3.5]

Ceramics

Ceramics are defined as "inorganic and non-metallic materials that are artificially manufactured, by high temperature reactions" (>600 °C). Among those most interesting for electronics are alumina (Al_2O_3), aluminium nitride (AlN), beryllia (BeO), silicon carbide (SiC), and glass ceramics.

Ceramics are made by the powder method: The material is made into a powder, mixed with glass particles, organic binders and solvents, by pressing or a special casting process "tape casting". Afterwards the material is sintered (heat treated) at temperatures 800 - 1600 °C. During the sintering the binder and solvents are evaporated and the powder particles are bound together (molten, in case of glasses). During the process the material typically shrinks 15 - 20 % linearly.

The tape casting process [3.1] is used for manufacturing of thin layers of ceramic. From a slurry of for example alumina powder, glass, solvents and binders a thin soft layer is made in the desired width as the material moves through an opening in the bottom of the slurry container, down on a moveable transport band. The distance between the bottom of the opening in the container and the band is controlled with great precision, and it determines the thickness of the layer of ceramic. The consistency is soft and pliable, and the ceramic in this form is called "green tape". After being cut to desired lengths, the material is further processed, by metallisation, punching of holes, etc. Often many layers are laminated on top of each other under pressure, and they are sintered at high temperature, as mentioned above. The material gets a hard brittle consistency after sintering. This process, used for multilayer ceramic substrates, will be further discussed in Chapter 8.

Ceramics are brittle and crack easily. They may have high electric resistivity and some of them have very high thermal conductivity. The relative dielectric constant may vary from 4-5 to many thousands, please refer to Tables 3.1 c) and 3.2. They are chemically stable and have a good stability in their mechanical properties up to high temperatures. However, they are often difficult to machine after sintering, and they tolerate little mechanical shock.

An important electrical parameter for non-perfect dielectric materials is the dielectric loss. This may be characterised by the loss angle δ. Tan δ is the ratio between resistive and capacitive current, and assuming we have the circuit model of Figure 3.2 with the parallel resistance Rp as the only parasitic, it may be written:

$$\tan \delta = (1/R_p)/\omega C_p = 1/ \omega R_p C_p = 1/Q,$$

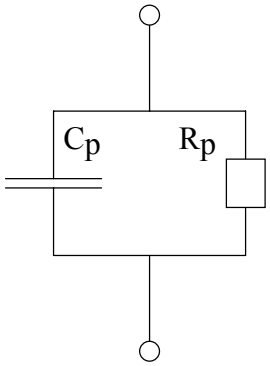


Fig. 3.2: Circuit model for dielectric loss.

Where R_p is the ohmic resistance, $1/\omega C_p$ is the capacitive impedance at frequency ω, Q is the ratio between stored energy and dissipated energy in a capacitor based on the dielectric. Tan δ is related to the complex dielectric constant:

$$\varepsilon = \varepsilon_0(k' - jk'')$$

by

$$\tan \delta = k''/k'.$$

Tables 3.1 c), 3.2, 3.4 and 3.5 show tan δ for some ceramic and other materials.

Table 3.2: Relative dielectric constant (and tan δ) for ceramics and other materials [3.4].

Material	Dielectric Constant
Teflon	2.1
Silica glass	3.8
PVC	4.6
Al_2O_3	9.9
$MgTiO_3$	20
TiO_2	100
$CaTiO_3$	160
$SrTiO_3$	320
$BaTiO_3$	1000-2000
$Ba(TiZr)O_3$	10,000
$Pb(Mg_{1/3}Nb_{2/3})O_3$	18,000

	Dielectric Constant (1Mhz)	Dissipation factor (1Mhz)
Borosilicate-E-glass	6.33	0.001
Fused Silica	3.7	0.0001
Aluminium oxide 99.5% (sintered)	9.4	0.0001
Beryllium oxide 99.5% (sintered)	6.8	0.0003
Epoxy resin	3.3-4	0.03-0.05
FR4 Laminate	4.3	0.019

Electronic uses of ceramics are, among other things, as substrates in hybrid technology, for component packages, base material in surface mounted resistors, dielectric in capacitors, piezoelectric components, magnet cores (ferrites), etc. In the future it is anticipated that superconductive oxide ceramics will play a very important role in electronics.

Table 3.1 c) shows some material parameters for some important ceramics. Alumina (Al_2O_3, 90 - 99 %) dominates as substrate for thick film and thin film hybrid circuits and hermetic component packages. The high thermal conductivity compared to organic substrate materials is very favourable. Low thermal coefficient of expansion gives a good thermal match to Si. AlN, BeO and SiC have higher thermal conductivity, and they are used in applications where the power dissipation is particularly high. However, BeO is very poisonous and AlN is more difficult to process than Al_2O_3. SiC has a very high dielectric constant. AlN, BeO, SiC are costly materials compared to Al_2O_3.

Used as a high frequency component substrate or dielectric the high dielectric constant in most ceramics may be unfavourable. For dielectric in capacitors, however, we need the high dielectric constant, and for example bariumtitanate in mixtures with other elements is used, please refer to Chapter 4.

During the last 5-6 years new ceramic materials have been developed, especially suitable for multilayer ceramic circuits. They are based on glass (calcium-, magnesium-, and silicate-), alumina and other materials, see Table 3.1 e), and they have the following advantages:

- Lower process temperature than alumna (ca. 800 °C compared to 1700)
- Lower dielectric constant (e_r down to 4 - 5)
- Thermal expansion almost equal to that of Si and GaAs

- Compatibility to noble metal metallisation (see Chapter 8).

A disadvantage is a lower thermal conductivity than for high temperature ceramic materials. Additional information is given in Chapter 8.

Glasses

A glass is an amorphous, supercooled liquid, i.e. it normally has no regular crystalline structure, and it becomes fluid when re-heated. Some materials called devitrifying glasses, or glass ceramics, convert to a crystalline state after heating, but do not reflow upon reheating.

Among the uses of glass materials are as matrix in thick film pastes (lead borosilicate, $PbO.B_2O_3.SiO_2$; cadmium borobismuthate $CdO.B_2O_3.Bi_2O_3$; bismuth sesquioxide, Bi_2O_3, etc.) [3.8]. Glasses are also used for low temperature multilayer ceramic substrates, most often in combination with the ceramics mentioned above. (See Table 3.1 e) and [3.1 p. 50 and 3.2]).

Glasses made from K-, Na-, Pb- and other metal silicates are used for hermetic, electrically insulating metal seals, providing good match of the TCE of various metal alloys. In low power thin film circuits glass is often used as substrate material.

Other insulators

Important insulating materials on the Si chips are SiO_2 and Si_3N_4, Table 3.1 c).

3.3 ORGANIC MATERIALS, PLASTICS [3.1, 3.2, 3.6]

Plastic (Greek: "plastikos", which means shaping or forming), is a large group of organic materials that harden and keep their shape after a moulding or forming process with heat and pressure [3.6]. They can be custom tailored to give good electrical, mechanical, and chemical properties, and great progress is taking place for these materials in electronic applications.

Many types of plastics are used in electronics as structural materials (boxes, component substrates, connectors, etc.), for thin dielectric layers, encapsulation of components, etc. Plastics are also used in electrically conducting or insulating glues, as process materials in production processes (photoresist, etch resist, etc.), and as binder for printing pastes in hybrid technology. A summery is given in Table 3.3. The materials can be reinforced for better mechanical strength. The many different types of plastics have properties that are becoming increasingly important to understand and use in modern electronics.

Some of the requirements for the plastics may be:

- High electrical resistivity, high breakdown field, low dielectric losses, low dielectric constant
- Thermal and mechanical stability up to the working temperature of the electronics
- Thermal expansion compatible with other materials (Si, metals,..)
- High mechanical strength for certain applications, softness and flexibility for other applications

- Chemical resistance to solvents, etc.
- Good adhesion to other materials
- Ease of processing
- Low water absorption and small change of the properties during the effect of moisture

Table 3.3 a): Plastics in various types of electronics applications.

Integrated circuits, transistors, diodes, and other discrete devices	Transfer moulding compounds, injection moulding compounds, castings, potting, dip and powder coating compounds, and die attach adhesives. Photoresists. Junction coatings.
Wires and cables	Sleevings, coatings, varnishes, intermetal dielectrics.
Connectors	Transfer moulding, injection moulding, compression moulding compounds.
Hybrids	Conductive and non conductive adhesives, sealants, conformal coatings.
Transformers, coils, bushings	Transfer moulding compounds, coatings, potting compounds, coil impregnates, wire insulation.
Printed circuit boards	Laminates, conformal coatings, solder masks, masking tapes, component attachment adhesives, and vibration dampers. Photoresists.

Table 3.3 b): Types of plastics for various purposes.

USE	SUITABLE MATERIALS
Transfer moulding	Epoxides, silicones, phenolics, polyimides.
Injection moulding	Polyethylene, polypropylene, polyphenylene sulphide.
Encapsulation/casting	Epoxides, polyurethanes, silicones.
Adhesives	Epoxides, polyimides, cyanoacrylates, polyesters, polyurethanes.
Coatings	Silicones, fluorocarbons, epoxides, polyxylylenes, polyurethanes, polyimides.
Films	Polyesters, polypropylene, polystyrene, polyimides.
Sealants	Silicones, polysulphides, polyurethanes, epoxide-polyamides, and fluoro-silicones.

3.3.1 Basic composition

Plastics are synthetic polymers. They consist of very long and complex organic molecules. A basic building block normally is the benzene molecule, see Figure 3.3. By replacing an atom in an organic molecule (built from carbon and hydrogen) with a benzene ring, one can make other molecules, which are often called monomers, please refer to Figure 3.4. When such monomers are bound together in a periodic structure, in a "polymerisation process", we get the analogous polymer composition. If we replace another atom in the same basic molecule, we get another monomer (and another polymer). By addition of smaller amounts of other elements or compositions, selected properties can be changed and improved considerably.

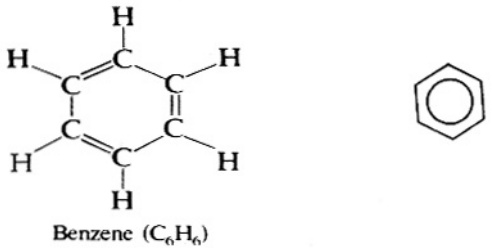


Fig. 3.3: Benzene molecule, its chemical structure and symbol.

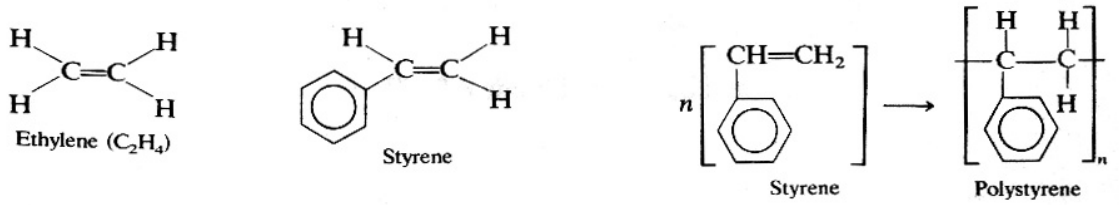


Fig. 3.4: If an H-atom in ethylene is replaced by benzene, we get styrene monomer, which can be converted to polystyrene.

The polymers may be linear, branched, or cross-linked, Figure 3.5. The cross-linking gives the best chemical stability. Two important groups of plastics are the thermoplastic and the thermosetting materials, see Figure 3.6. The first type melts when it is heated in a reversible process. Teflon (PTFE), polysulfones, polyesters are examples of thermoplastic materials. The thermosetting materials are irreversibly cross bound during the polymerisation process, and they can not be brought back to their original state.

Some examples of monomers/polymers are shown in Figure 3.7.

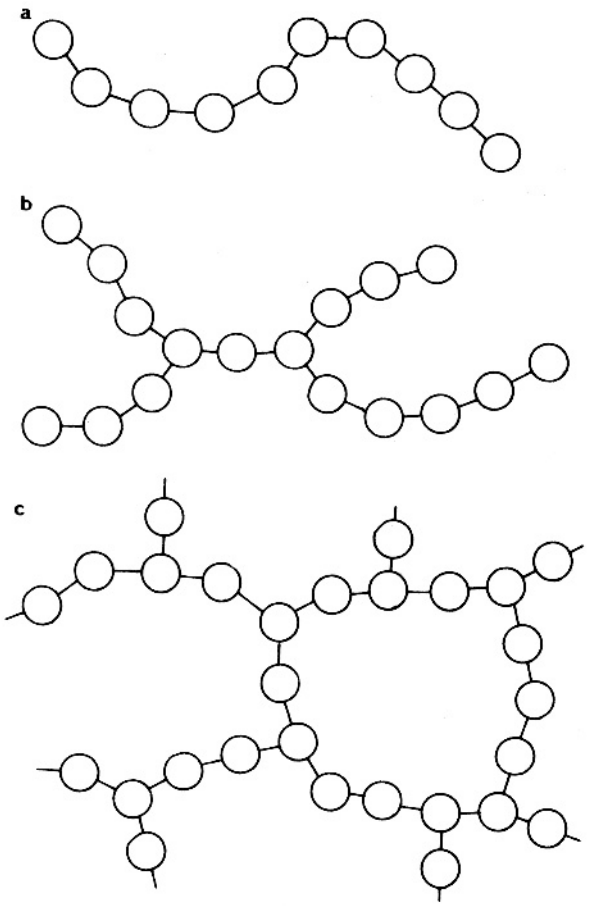


Fig. 3.5: Linear, branched and cross-linked structures in polymers.

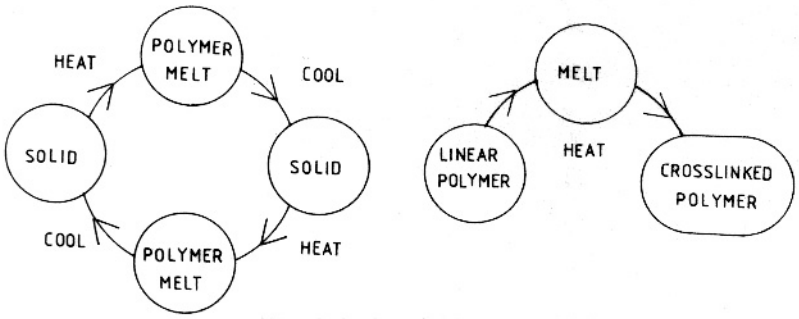


Fig. 3.6: The effect of heating on thermoplastic and thermosetting materials.

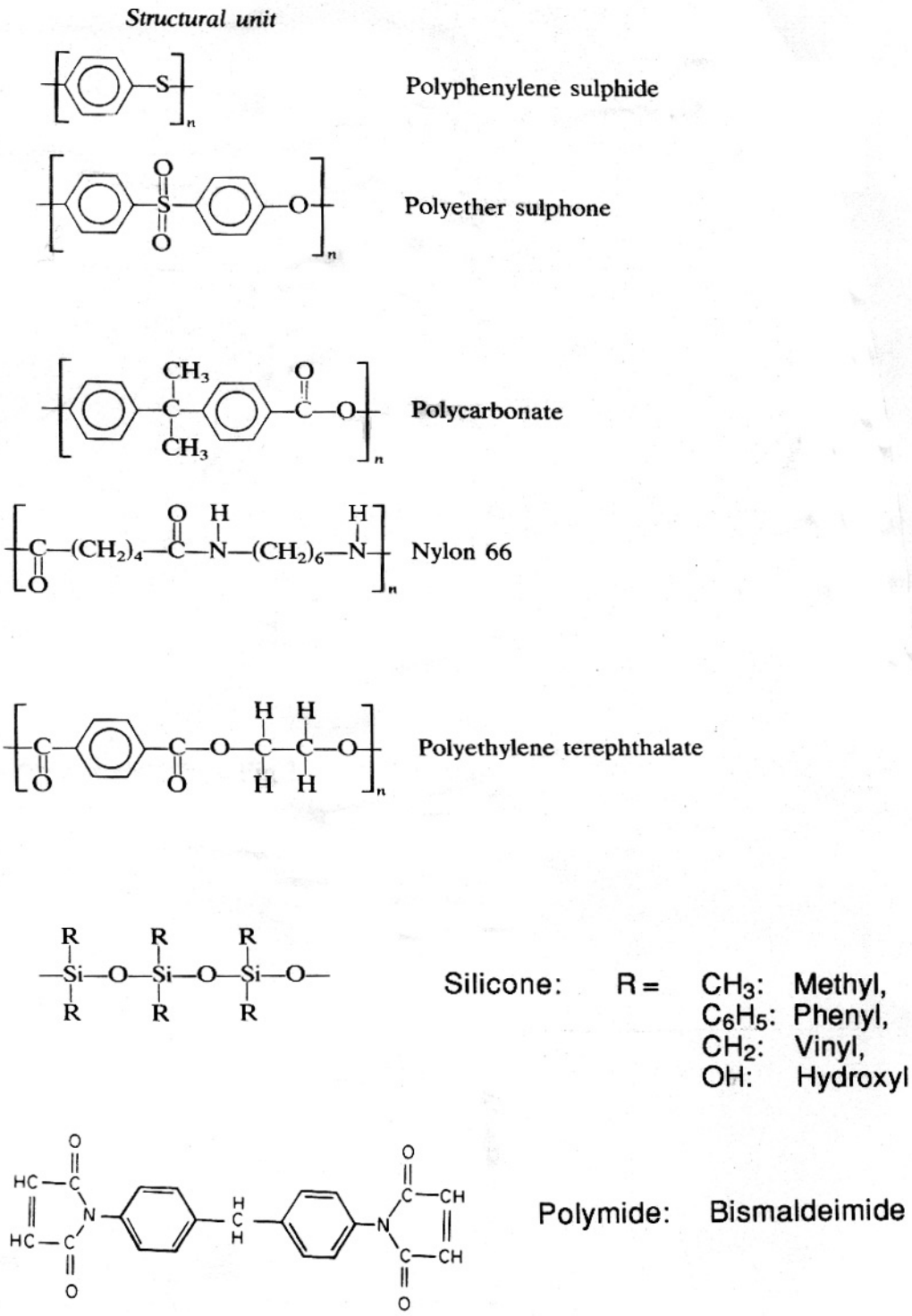


Fig. 3.7: The structural unit of certain monomers/polymers.

3.3.2 The polymerisation process

In some materials the polymerisation takes place during heat and some times pressure, for example for phenolics and epoxy. Other materials polymerise by exposure to UV-radiation. Often two components are stored separately, and the curing starts immediately when they are mixed, even at room temperature (two component system).

The polymerisation process may take place in several steps and may be quite complex. As an example we shall mention the process for phenolic resin, that is

used in low price printed wiring board laminates [3.7]. The starting materials are phenolic and formaldehyde. In the first stage of polymerisation the formaldehyde molecules react with the aromatic rings in the phenolic. Water is lost, and we have "A-stage" phenol resin. Further reaction gives off more water, and we get "B-stage" material, which can still melt, and which is still soluble in suitable solvents.

When the B-stage material is exposed to more heat and more pressure, in the presence of suitable activators, more water is given off. The resin hardens to a stage where it will no longer melt, and it is not soluble in ordinary solvents. In this process the long macro-molecules from the B-stage resin are cross-linked, such that the whole body of material may be treated as one big macro-molecule.

3.3.3 Electrical properties

Plastics are often used as dielectric, electrically active materials, because of their high electrical resistivity, low dielectric constant, low dielectric losses, and high dielectric strength. Values of these parameters for certain plastic materials are given in Table 3.4.

Table 3.4: Electronic properties of plastics [3.6].

Polymer	Permittivity ε_r	Tan δ	Dielectric strength [MV cm^{-1}]	Volume resistivity [Ohm•cm]
Polyethylene	2.3	-10^{-3}	5.3	$>10^{16}$
Polypropylene	2.3	$3x10^{-4}$-10^{-3}	0.24	10^{16}-10^{17}
Polymethyl methacrylate	3.6	0.62	0.14	$>10^{15}$
Polyvinyl chloride Unplasticised	3.5	0.031	0.24	10^{15}
Plasticised	6.9	0.082	0.27	10^{13}
Polystyrene	2.5	$1.5x10^{-4}$	0.2-0.3	10^{17}-10^{19}
Polyethylene terephthalate	3.3	$2.5x10^{-3}$	2.95	10^{18}
Nylon 6 (dry)	3.5	$6.5x10^{-3}$	1.5	10^{15}
Nylon 66 (dry)	3.6	$8.5x10^{-3}$	1.5	$>10^{15}$
Polytetra-fluoroethylene	2.1	$2x10^{-4}$	0.18	$>10^{15}$
Phenol-formaldehyde resin General purpose	6-10	0.1-0.4	0.06-0.12	10^{10}-10^{12}
Low electrical loss	4-6	0.03-0.05	0.1-0.14	10^{11}-10^{14}
Typical epoxide	4.5-5.5	0.01-0.02	0.2	10^{14}-10^{15}
Silicone rubber	3.6	$2x10^{-3}$	0.2	10^{16}

3.3.4 Mechanical, physical and chemical properties

Polymers are not perfectly elastic, and they are called "visco-elastic". Their hardness and strength vary greatly. Generally they are highly resistant to inorganic chemicals. However, exposed to water and organic chemicals they may change important parameters and they may swell, soften, crack, etc. Many polymers are hygroscopic, and water will penetrate into the material over time.

As structural materials plastics have the advantage of low weight (density typically 1.0 - 1.5 g/cm^3). Low thermal conductivity is a disadvantage when they are used as component substrates, but it may be an advantage for other applications. A typical range of values is 0.2 - 0.4 W/°C m, please refer to Table 3.1, but it can be increased by addition of metal-, ceramic- and other types of particles. The thermal coefficient of expansion is in the range of 30 - 300 ppm/°C, significantly higher than for metals and semiconductors. This may give high material stress and possibly cracking. The thermal coefficient of expansion may be reduced by additives.

3.3.5 Glass transition temperature

It is typical of many polymers in their cured form that important properties change above a characteristic temperature, the "glass transition temperature", T_g. Here the polymer changes from its glass-like state to a softer rubber-like state. The material does not melt, but T_g is the temperature where the molecular bonds are weakened. For electronic applications T_g should not be exceeded over long periods of time (many minutes), otherwise the material properties may be damaged permanently. As an example we show in Figure 3.8 the thermal expansion below and above T_g for epoxy and for other types of plastics. The changes may cause cracks, delamination and other reliability problems (for example: plated via-holes in very thick printed wiring boards).

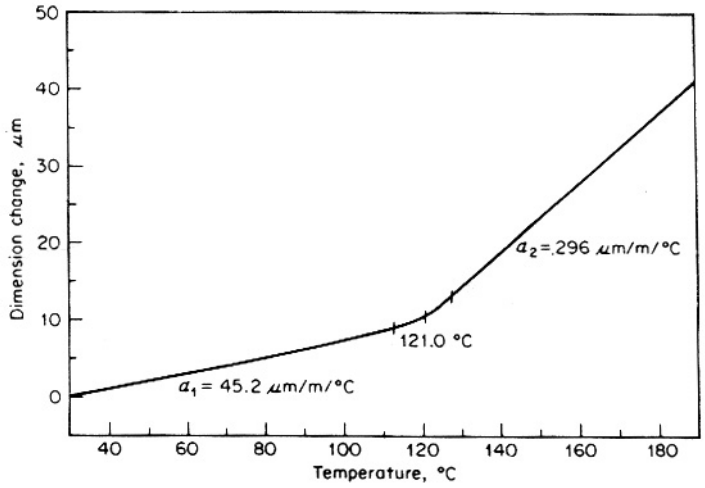


Fig. 3.8 a): Thermal expansion below and above the glass transition temperature, T_g, for epoxy [3.6].

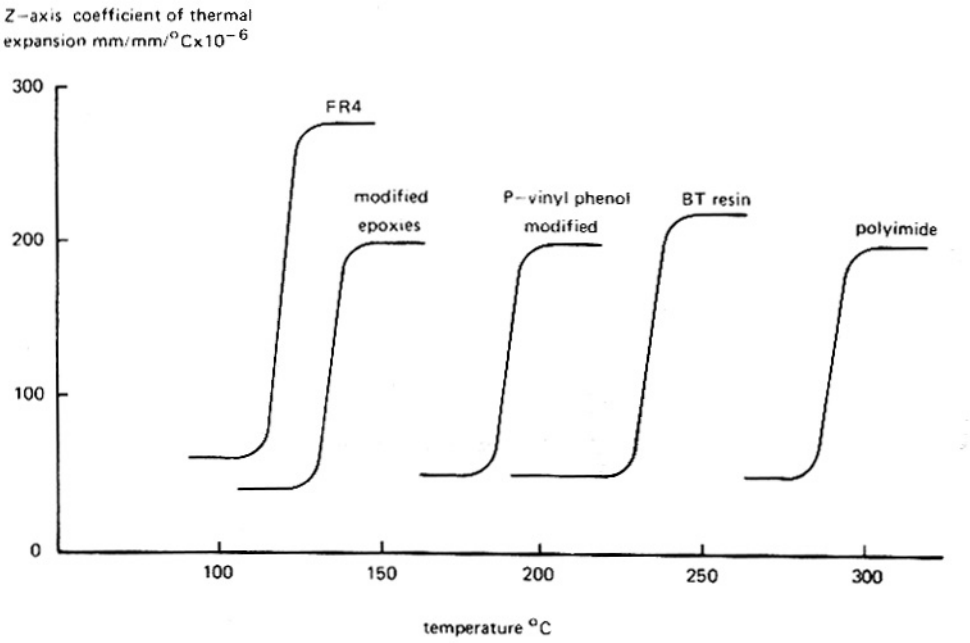


Fig. 3.8 b): The thermal coefficient of expansion below and above T_g for various types of plastics [3.23].

3.3.6 Specific materials [3.1, 3.2, 3.6, 3.8]

Below we will highlight some important groups of polymers. There are many types with varying properties within each group.

Epoxy

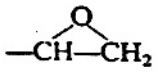
Epoxy has a wide range of molecule structures and properties, but all with epoxide atom groups. Please refer to Figure 3.9 a). 90 % of printed wiring board laminates used today are epoxy based. Bisphenol epoxy is used the most, with addition of epoxy novolac, see Figure 3.9 b). Also adhesives, structural plastics, etc. are made from epoxy. For moulded plastic encapsulation of components, epoxy of the type novolac is the most used. [3.2, p.474]

Moisture will penetrate epoxy over time and may cause corrosion in the presence of alkali ions. As hardener epichlorohydrin is often used. It can leave chlorine in the cured epoxy. Together with moisture this gives HCl, which creates corrosion and reliability problems over long time. Low chlorine content (a few ppm) is therefore a common requirement for epoxy in electronic applications. Silica particles are added to the epoxy to reduce the thermal coefficient of expansion from 40 - 50 to approximately 20 ppm/°C. This will reduce the thermal stress near the silicon chip and the metal in the package. Br is added as a flame retardant, but it also gives corrosion when moisture is present.

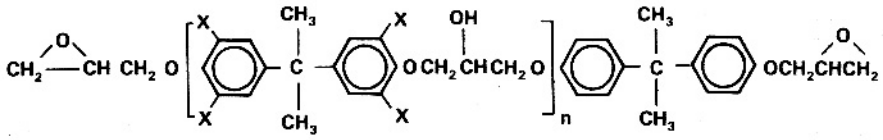
Epoxy normally is strong and hard. For certain applications it should be soft to reduce mechanical stress. This can be achieved by adding special oils, elastomers of the type akrylonitrile-butadiene-styrene, silicone or polyurethane, before the curing.

Many other modifiers and additives are used to optimise epoxy for various applications.

a)

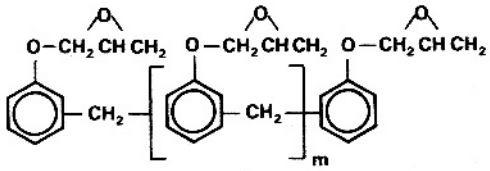


b)



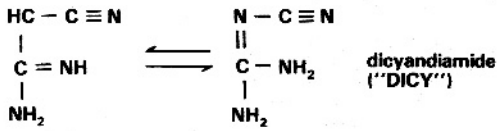
Bisphenol A (X = H) and Tetrabromobisphenol A (X = Br) copolymer. Br content 15%-20% of resin weight for adequate fire retardance in glass cloth/epoxy resin composites.

c)



Epoxy novolac resin. Added 10-20% of total epoxy resin weight to increase crosslink density.

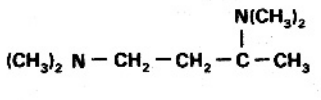
d)



dicyandiamide ("DICY")

Curing Agent Dicyandiamide

e)



tetramethyl butane diamine, 1,3 bis (dimethyl amino) butane (TMBDA)

Catalyst, Accelerator

Fig. 3.9: a):The epoxide group, which is the building block in epoxy, b) - e): Starting materials for epoxy: b): Bisphenol A, which constitutes most of the starting material. The H-atoms in the places X are often replaced with Br to reduce the flammability; c): Epoxy novolac; d): The hardener dicyandiamide; e): The catalyst [3.1].

Phenol

Phenol is used for low price printed wiring board laminates with relaxed environmental and performance requirements (consumer products). Phenol is also the matrix for several materials that are screen printed in polymer thick film technologies (see Chapter 8), and for adhesives.

Polyimide

Polyimide is a group of plastics in rapid development. Among the applications are high performance printed wiring boards, dielectric films for insulation in thin film hybrid circuits and silicon integrated circuits, flexible printed circuit board substrates (e.g. known under DuPont´s trade mark Kapton). Polyimides are strong and mechanically stable. High T_g permits a high working temperature. They are suitable for high frequency dielectrics because of low dielectric constant and low dielectric losses. Many polyimides have the disadvantage that they are hygroscopic and absorb up to 2 % moisture. Electrical and mechanical properties change in the presence of moisture, and corrosion can occur.

Teflon

Teflon (Polytetrafluorethylene, PTFE) is extremely resistant against chemicals. It is used, among other things, as dielectric in high frequency substrates because of its low dielectric constant ($e_r = 2.1$) that is nearly independent of frequency and temperature. The loss tangent is also low. Because the material is so chemically inert and has poor adhesion to almost all materials (please refer to the use of Teflon coating in household frying pans), it is difficult to process [3.6]. Teflon is a thermoplastic material.

Polyester

Polyester (polyethylene terephthalate, PET) is a thermoplastic material melting around 260 °C. It has good dimensional stability below T_g that is at approximately 70 °C, but it shrinks above T_g. Polyester has good chemical resistance, high mechanical strength, favourable electrical properties and low price characterises polyester. It is used for low price flexible substrates, (membrane switch panels, etc.), printing screens, dielectric in capacitors, moulding material, surface protection material ("conformal coating"). It is not usable at temperatures for normal soldering processes because of uncontrolled shrinkage. Polyester is made by DuPont under the trade name Mylar.

Silicone

Silicone has the structure shown in Figure 3.7, where R can be similar or dissimilar organic groups, often methane (CH_3) or phenyl (C_6H_5). Some types of silicone are flexible over a large temperature range. They are hygroscopic, but they can be made with very high purity (below 5 - 10 ppm halogen content). Their high dielectric strength and high electrical resistivity are also useful. However, they have a high thermal coefficient of expansion, low mechanical strength and -stability, and they are not especially resistant against solvents and other chemicals. Often they have poor adhesion to other materials, and they may be costly. Silicones are made as liquid, as "grease", gel or elastomer (rubber like). They are used for passivating by conformal dip coating or as deposited, thin layers. They give very good environmental protection. Power electronic modules often have epoxy on top of a layer of silicone gel to give mechanical strength (the epoxy) as well as environmental protection and low stress on the chip (the silicone) [3.24]. Before curing the silicone adheres and spreads very easily and it can contaminate soldering areas and ruin the solderability in PWBs, etc. Silicones can be made to cure at room temperature, at high temperature, or under UV-exposure.

Polyurethane

Polyurethane gives good adhesion, it cures fast, it is flexible at low temperatures, and has low moisture penetration. However, the thermal coefficient of expansion is high, it is difficult to remove and it shrinks at curing. Its uses are primarily as moulding material for mechanical protection.

Parylene (paraxylylene)

Parylene is used for dip coating as protection. Good resistance against solvents and low water penetration characterise Parylene. Certain properties for parylene and other materials for dip coating are given in [3.2, p. 783, 3.8, p. 225].

Acrylic

Acrylic of suitable composition cures in UV-radiation. Various types of acrylic are used for photoresist, UV-curing adhesives, in addition to dip coating, etc.

Table 3.5: Properties of high temperature moulding plastics [3.6, page 307].

Property	Poly-sulphone (Udel)	Polyether sulphone (Victrex)	Poly--phenylene sulphide (Ryton)	Polyether--imide (Ultem)	Ultem +20% glass reinforced
Flexural strength [$x10^{-3}$psi]	15.4	18.6	25	21	30
Flexural modulus [$x10^{-6}$psi]	0.39	0.37	1.7	0.48	0.9
Tensile strength [$x10^{-3}$psi]	10.2	12.2	16.2	15.2	20
Dielectric constant [1 MHz, 25^{o}C]	3.03	3.45	3.8	3.1	3.5
Dissipation factor [1 MHz, 25^{o}C]	0	0.008	0.0014	0.006	0.0015*
Volume resistivity [$x10^{-17}$ Ohm•m]	50	100	45	6.7	0.7
Electrical strength [kV/mm]	17	16	17.7	28	26.5
Deflection temperature [^{o}C] at 264 psi	174	202	243	200	209
Thermal expansion coefficient [ppm/^{o}C]	56	55	40	56	25
Water absorption [%] (24h)	0.3	0.4	0.05	0.25	0.26
Maximum continuous temperature [^{o}C]	160	170-200	170	170	170

* 1kHz

Polysulphone, polyethersulphone, polyetherimide

These are high temperature thermoplastic materials with good thermal and mechanical stability, favourable electrical properties, but limited chemical resistance to certain solvents. They are used for moulding structural materials and for printed wiring board materials. These materials are increasingly being

used for 3-dimensional PWBs, please refer to Section 5.13 .Their properties are shown in Table 3.5 [3.1, 3.6, p. 308].

BASIC PROCESSES

3.4 TRANSFER OF PATTERNS BY PHOTOLITHOGRAPHY [3.8, 3.9]

Photolithography is used for transfer and definition of patterns. Accuracy and resolution down to 0.2 μm can be achieved, with improvement of resolution as a main bottleneck challenged by the IC industry.

The starting point is a pattern generated from a CAD system or similar, on a photographic film, the photomask or artwork. The film substrate is a plastic foil, or a glass plate when high precision is required. The pattern on this film is made by exposure with a computer controlled photo plotter, laser (or a computer controlled electron beam, for sub-micron resolution), see Chapter 5.

Figure 3.10 shows the procedure for transfer of the pattern. A thin layer of photosensitive material, photoresist, may be deposited on the object surface by spinning. This process consists of depositing a few drops of photoresist by dispenser. Then the object is rotated fast, and the resist is spread over the surface by the centrifugal force. Alternative methods are spraying, screen printing (see below), or laminating on the resist in the form of a dry film. The surface is illuminated through the photo mask. Afterwards the resist is developed and cured by heating.

Two classes of photoresist behave differently: Positively and negatively acting resist. The negative resist is dissolved by the developer where it is <u>not</u> illuminated (Figure 3.10). Thus we remain with hardened resist in the reverse (negative) pattern relative to what is black on the photo mask. The positive resist behaves the opposite way: We get the same resist pattern remaining on the substrate or wafer as the black areas on the photomask. Positive resists generally give the best definition, but they are more costly than the negative ones.

The cured resist is resistant to many etchants, and it protects the material underneath from the etchant. Thus, when we want to etch a metal layer, the photoresist may be used as etching mask. When the etching process is completed the rest of the photoresist is dissolved in a suitable solvent.

Photolithography is used for printed wiring boards, in hybrid technology and on semiconductor wafers. In addition to etch masking, it is also suitable as a mask during plating, and in the fabrication of screens for screen printing.

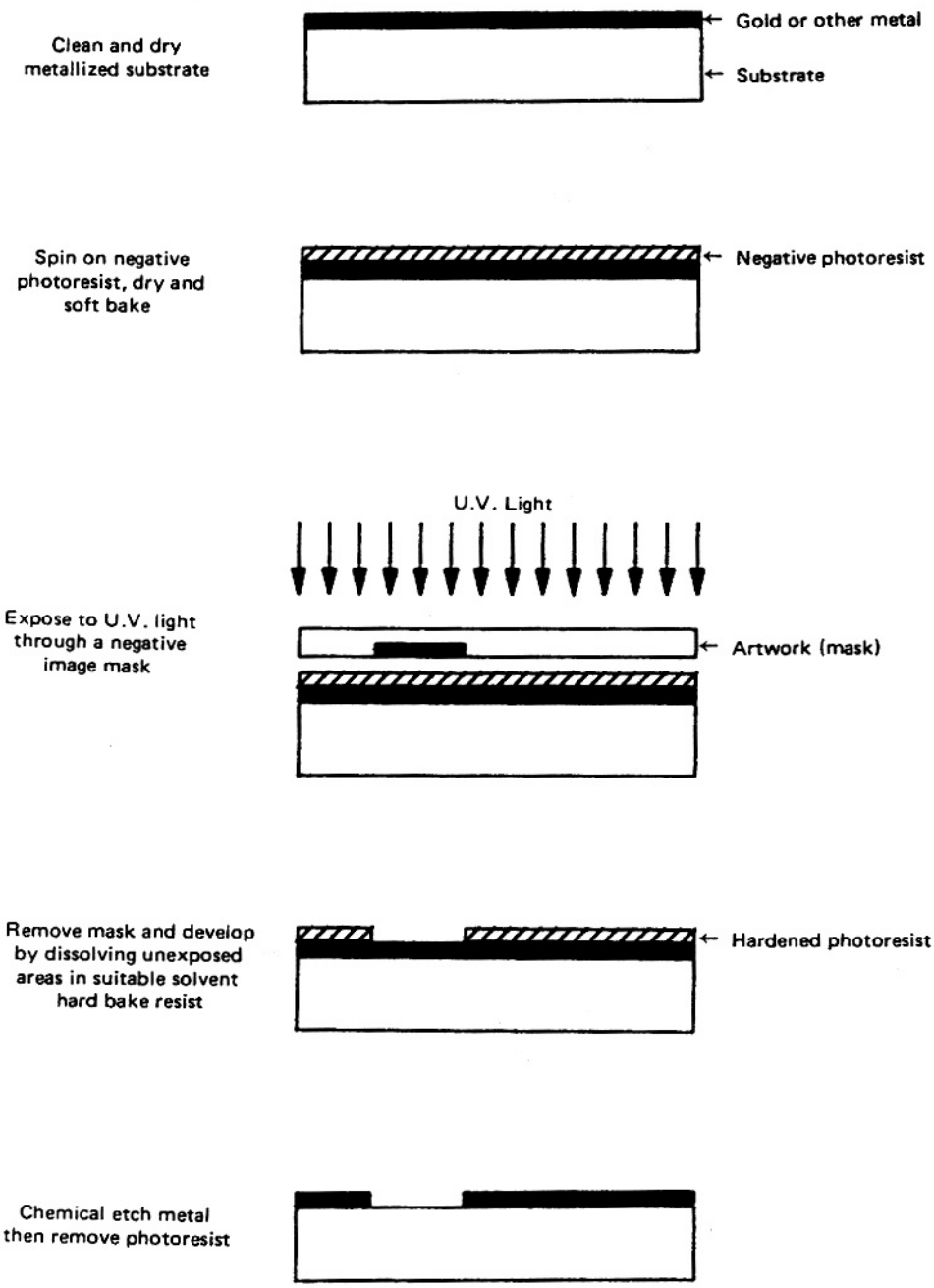


Fig. 3.10: The steps in photolithographic transfer of patterns and the subsequent etching of metal films with negative photoresist. If positive resist is used, it is the illuminated part of the photoresist, which is removed during the development.

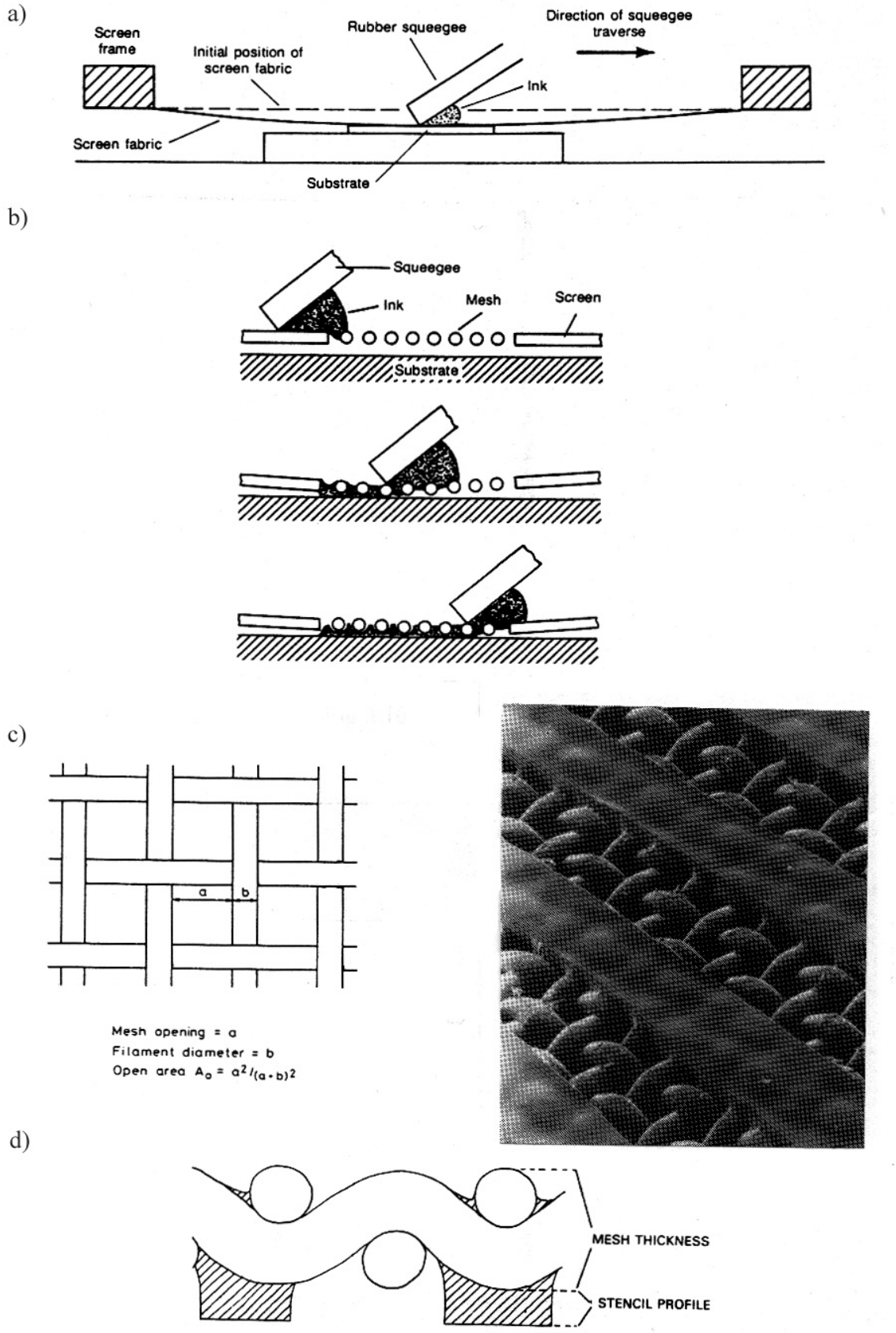


Fig. 3.11: Screen printing: a) and b): Printing process, c) and d): Details of the screen [3.2, 3.11].

3.5 SCREEN PRINTING AND STENCIL PRINTING

Transfer of patterns and deposition of materials by screen printing, or "silk" printing, consist in pressing material in paste form through the openings in a printing screen. This is analogous to the process used in reproduction of art. Earlier a screen of silk was used and the name is still left, even though woven screens today are made from polyester filaments or metal wires. The screen is stretched and tensioned on a metal frame, as shown in Figure 3.11.

The preparation of the printing screen consists of depositing a photo sensitive film (emulsion) with desirable thickness on the screen. The emulsion may be polyvinyl alcohol or -acetate, made light sensitive by additives, e.g. sodium bicarbonate. It softens in water and penetrates into the woven structure. After drying it is exposed through a photomask with the desired pattern, dried, developed and cured like the resist in photolithography.

The paste that is to be printed is forced over the screen by a squeegee, as seen in Figure 3.11, which is made of polyurethane rubber or similar material. Normally there is a distance of a few millimetres between screen and substrate ("snap-off"), and the screen is forced into contact with the substrate by the pressure of the squeegee. Where there are openings in the resist on the screen, the paste is pressed down onto the substrate.

Screen printing is a craftmanship that requires experience and knowledge to give good and reproducible results. The process can also be modelled theoretically by hydrodynamic theory [3.10].

Important factors for good definition, accurate pattern placement and correct amounts of paste are, among others:

- Fineness of the screen and the wire (the number of wires per unit length, "mesh", and the wire diameter)
- Thickness of the resist, Figure 3.11 d)
- Squeegee hardness, angle and speed of motion
- Tension in the screen and snap-off
- Viscosity and printing properties ("rheology") of the paste

Certain materials are added to the paste to give high "thixotropy", in the same way as in modern paints. This means that the paste will flow easily under the pressure of the squeegee, but it has high viscosity without pressure [3.2, p. 838, 3.11]. With high thixotropy narrow printing patterns will get steep walls after printing. This makes it possible to print patterns down toward 0.1 mm widths and distances. The dimensional control is limited by the wires in the weaving, the screen deformation during the printing and the accuracy in the registration of the mask relative to the substrate.

The amount of paste that is printed, is the gross area multiplied by the fraction that is not covered by wires, Figure 3.11 c), and the thickness of the mask.

Screen printing is used in the production of printed wiring boards, thick film hybrid circuits, printing of solder paste for surface mounting, etc. Typical screen parameters for thick film hybrid technology are 80 - 400 mesh (number of wires per inch), wire diameter 20 - 100 μm. For solder paste printing 40 - 120 mesh is

typically used, with wires 60 - 120 μm diameter, and approximately 50 % open area. With this information, and screen thickness, the volume of solder paste can be calculated.

High mesh count, thin wire and thin emulsion will give high resolution but a thin printed layer and a more fragile screen that is easily damaged. Details are found in [3.8, page 80, 3.11, page 173, and 3.12].

For printing of solder paste to high precision, the printing screen is replaced with a thin plate of metal or plastic. The openings are etched in a photolithography process, or they are punched, see Section 7.3. Such printing stencils have better dimensional stability and better wear properties than woven screens. However, one cannot make enclosed patterns or long patterns with short widths, and printing stencils are not suitable for printing of conductor patterns.

3.6 ETCHING [3.7]

3.6.1 Wet, chemical etching

The most common method for making conductor patterns is to first cover the whole board area with conductor metal. Then, masking by screen printing or photolithography, and removing the metal where it is not desired by dipping the sample in a chemical bath that dissolves the material, with the other parts of the surface being covered with an etch resist that is not attacked by the etchant. The etchants normally are aqueous acidic or alkaline solutions. This is called subtractive processing. The etchant can also be sprayed on to the surface to get good circulation and uniform etching. The speed of etching depends on the temperature, the composition and concentration of the etchant, how long the etching bath has been in use, circulation, etc. Control and reproducibility may be critical.

The choice of etch composition depends on what is to be etched and what is not to be etched, namely the etch resist. Some examples of etching reactions can be given:

Etching of copper: Several etching compositions are used. One of them is iron chloride, with the following reactions:

$FeCl_3 + Cu \rightarrow FeCl_2 + CuCl$

In addition the following reaction takes place:

$FeCl_3 + CuCl \rightarrow FeCl_2 + CuCl_2$

This etchant does not attack organic films that may be used as etch resists. However, tin/lead is etched and is therefore not usable as "masking" for pattern definition, as is common (please refer to Sections 5.5 - 5.6). Regeneration of the etchant is difficult, and the bath has to be discarded when its composition gets out of the specified range, giving a pollution problem. Other possibilities are sulphuric acid/peroxide, copper chloride, sodium chloride, and ammonium persulfat. For details see [3.7, p. 283].

Etching of gold: Potassium iodide and iodine are common etchants:

$Kl + I_2 \rightarrow Kl_3 + Kl$ (surplus)
$3\ Kl_3 + 2\ Au \rightarrow 2\ KAul_4 + Kl$

This etchant is used for thin film metallisation by gold on top of nickel/chromium (Chapter 8). To avoid that the etchant also attacks NiCr, one adds inhibitors of ammonium phosphate, etc. [3.8, page 74].

3.6.2 Dry etching

Wet, chemical etching is normally isotropic, which means that it etches in all directions with approximately the same speed. If we are to etch through a 10 μm thick layer, it also etches approximately 10 μm in the horizontal direction. The smallest lateral dimensions that can be etched are therefore in the same order of magnitude as the thickness. "Dry" plasma etching, or reactive ion etching, may give anisotropic etching, with an etching speed that is substantially greater vertically than laterally. Such etching is done with an etching gas in plasma form. The etching gas is ionised at low pressure in a closed etching chamber with a vacuum pumping system and controlled supply of gas. Reactive ion etching is done with a chemically active gas. The ions react with the surface and generate reaction products in gas form, which are pumped away. By means of electrodes and an electric field in the chamber one manages to get the ions to hit the surface with a preferred direction, which gives anisotropy in the etching. Under suitable conditions one can also etch in a sputter chamber "sputter etching", see Section 3.8.2.

3.7 PLATING [3.7]

Plating is building of conductive materials by an electrical process, in which ions of the material in a solution (electrolyte) are deposited and give off their ionic charge when they hit the object that is to be plated. There are two main types: Electrolytic and chemical ("electrolyses").

3.7.1 Electrolytic plating

By electrolytic plating the current passes through the object, the electrolyte and an external circuit. The deposition only takes place on conductive surfaces that are connected to the external circuit. By chemical plating it is the electrochemical conditions in the electrolyte and in the surface of the object that cause the ions to deposit on the surface. Chemical plating may be done both on conducting and insulating surfaces.

As an example of the electrolytic plating we will describe the deposition of copper: The object is immersed into an electrolyte that contains Cu^{2+} ions, for example $CuSO_4$ dissolved in H_2SO_4. The object forms the negative electrode (cathode), and a metallic copper plate forms the positive electrode (anode) in an electrolytic cell. Copper is dissolved on the anode:

$Cu \rightarrow Cu^{2+} + 2e^-$.

The reaction at the cathode is the reverse:

$Cu^{2+} + 2e^- \rightarrow Cu$

Thus, metal is removed from the anode and deposited on the object. (The cathode)

Electrolytic plating normally is a simple process. It can give a high rate of deposition (tens of µm per hour). The structure in the deposited material depends of the speed of deposition (current density), temperature and type of plating bath.

3.7.2 Chemical plating

To make the chemical plating process act on an insulating surface or parts of an insulating surface, they must be "sensitised" and "activated". We will describe the main steps in standard chemical plating of copper as an example. The whole process is relatively complicated [3.7, page 262].

The sensitising consists in dipping the object in a solution containing Sn^{2+} ions, to increase the sensitivity of the surface. Sn^{2+} ions are adsorbed on the surface. The activation takes place in an acidic solution of palladium chloride, which is transformed to metallic Pd. The reaction is the following:

$Sn^{2+} + Pd^{2+} \rightarrow Sn^{4+} + Pd$.

In the plating process (see below) Pd is a catalyst for the deposition of copper. (There is still doubt about the details of this process [3.7].)

The plating process continues as follows: The object is immersed into a reducing bath that contains Cu^{2+} ions, for example in the form of dissolved $CuSO_4$. Formaldehyde, HCHO, is the most common reducing agent. In this bath Cu^{2+} is reduced to Cu, which covers the whole surface, even where the surface is electrically insulating. At the same time formaldehyde is oxidised into acetic acid.

Chemical plating is a critical process, if we are to achieve good adhesion and controlled deposition. The composition of the solutions is complex, and if the composition, temperature, "bath loading" (the ratio between plated area and the volume of the bath) drifts outside the acceptable values, Cu^{2+} may be reduced to metallic Cu in the bath itself, which is thereby destroyed.

3.8 VACUUM DEPOSITION AND SPUTTERING [3.8]

3.8.1 Vacuum deposition

Thin metal films on hybrid substrates and semiconductor wafers are normally deposited by vacuum evaporation or by sputtering. Vacuum evaporation takes place in a chamber, Figure 3.12, which is evacuated to a vacuum of typically 10^{-6} Torr. The metal that is to be deposited is placed in a recess in a plate of high temperature melting metal, e.g. W, the "boat". The boat is heated by passing a high current through it (resistance heating), until the metal evaporates and its molecules spread out upwards in all directions in the vacuum chamber. The molecules hit the substrate that is located on the substrate holder above. A different way to heat the metal is to bombard it with an electron beam that is accelerated in an electric field with the boat as anode.

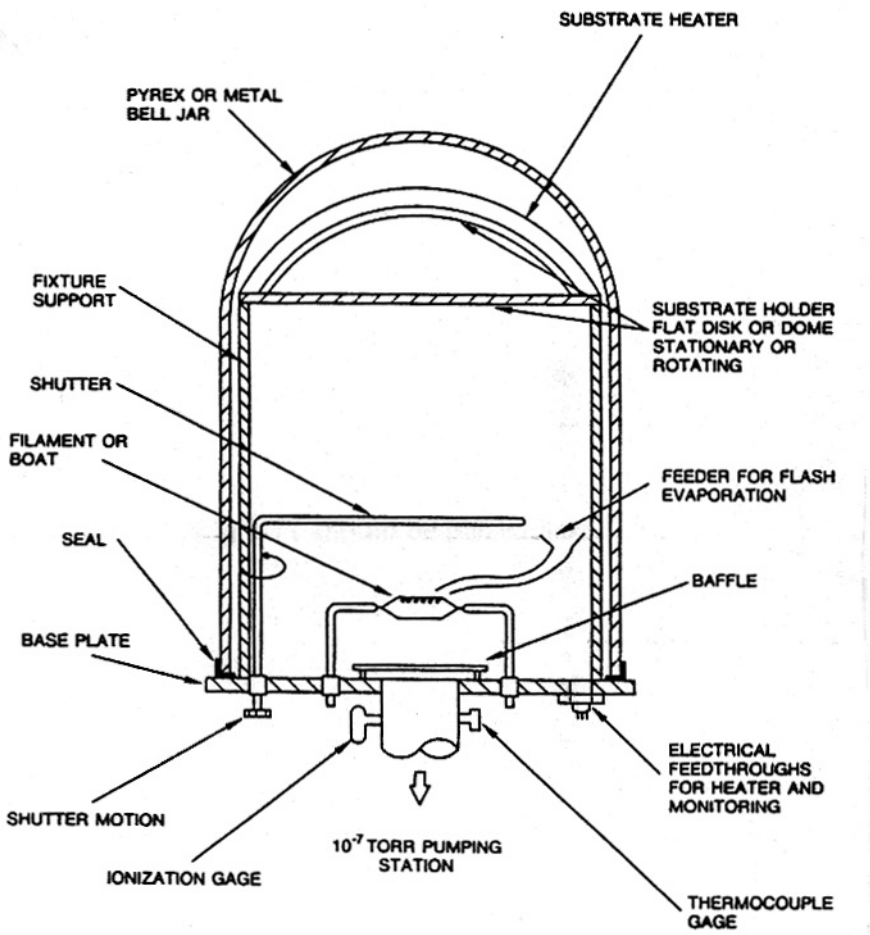


Fig. 3.12: Vacuum evaporation.

3.8.2 Sputtering

Sputtering is a process under low pressure where a "target" is bombarded by energetic positive ions. When the ions hit and give off their energy, particles are ejected from the target. These "sputtered" particles hit the substrate that is to be covered. The simplest version is DC sputtering, Figure 3.13. The plasma may be a noble gas, for example argon, at pressure 10^{-3} - 10^{-1} Torr. The gas is ionised in the strong electrical field, obtained by having 1000 - 2000 V between the target and the anode. A glow discharge is created in the argon gas, which is

decomposed into positive ions and free electrons. The ions are accelerated toward the cathode (target), they give off their charge by receiving electrons and are again neutral. Target material is torn off by the energy released. Energetic secondary electrons interact with neutral Ar atoms that are again ionised. Typical deposition rates are 100 - 1000 Å per min. Film thickness by sputtering, as well as by vacuum deposition, is limited to a few μm.

Electrically insulating target materials are not suitable for DC-sputtering, because they will be electrically charged and then disturb the glow discharge. Then AC radio frequency is used on the target holder electrode. Other types of sputtering are reactive sputtering and magnetron sputtering, which have other advantages.

Metals as well as alloys, oxides, glass and organic materials can be deposited by sputtering, by choosing a target made of the desired material. By placing the substrate as a cathode and masking selected areas, we may sputter etch, when the positive ions bombard the substrate surface and tear loose particles from the uncovered areas.

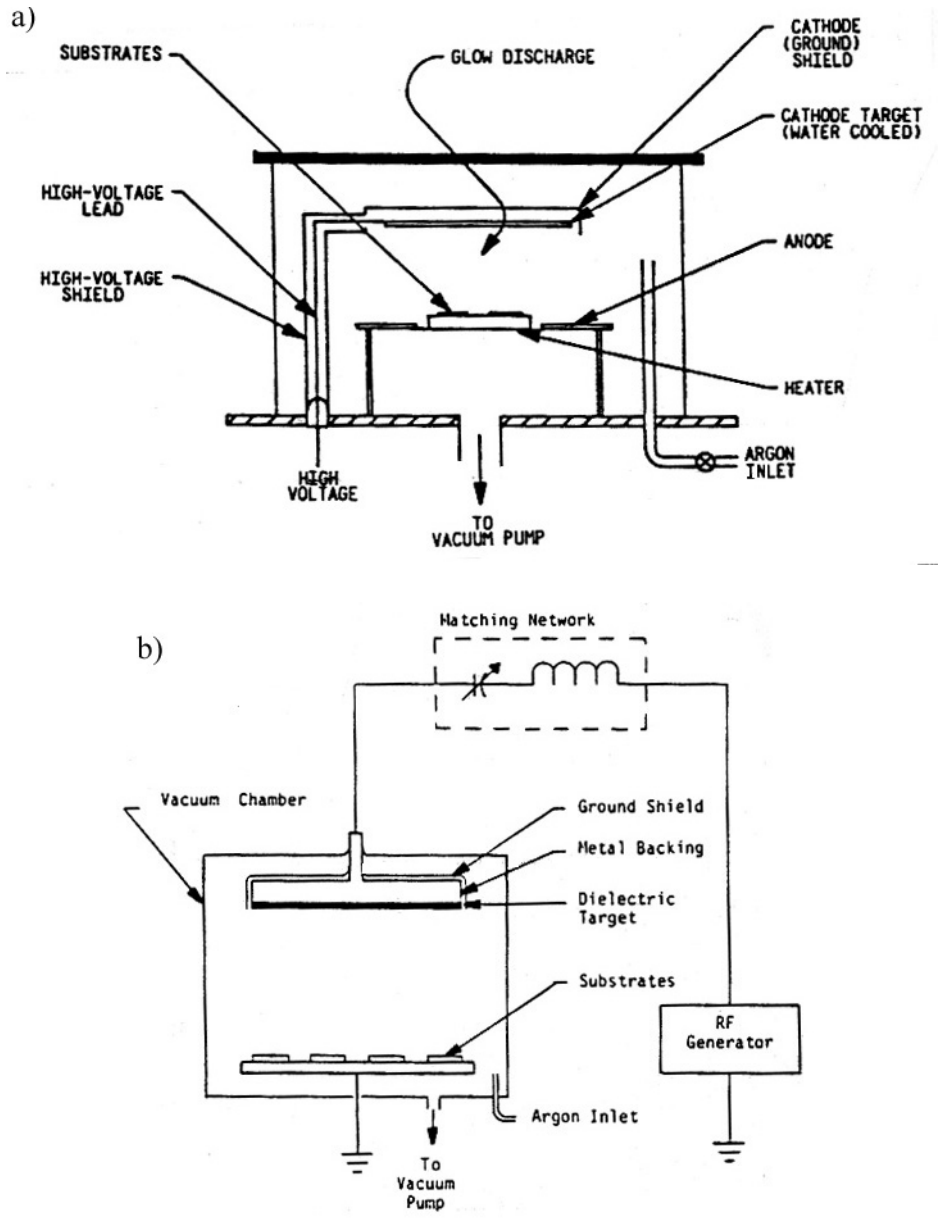


Fig. 3.13: Sputtering: a): DC sputtering, b): Radio frequency AC sputtering [3.8].

METHODS FOR ELECTRICAL AND MECHANICAL CONTACT

3.9 GENERAL

In this section we describe basic methods and processes for providing mechanical and electrical contact in electronics.

Soldering and gluing are used to hold parts together as well as to give electrical contact, whereas bonding only serves for electrical contact (except for die bonding).

3.10 SOLDERING [3.7, 3.13]

Soldering is the dominating method for electrical connection of electronic components. It is also important for mechanically assembling and to establish good thermal contact. It may be defined as "establishment of a metallic bond between two metallic surfaces by use of a different liquid (solder-) metal".

Soldering consists in wetting the surfaces that are to be joined by the molten solder metal and cooling until it solidifies. Soldering with high melting alloys is called hard soldering or brazing, and it is used mainly for connecting structural mechanical parts. In electronics, soft soldering with tin/lead alloys, with melting point around 180 °C, dominates. The materials are cheap, the process can easily be automated, and the parts may easily be taken apart for repair.

Yet soldering is the source of a large fraction of the faults in the electronics, during production as well as during the field life of the product afterwards.

Some factors that determine solder quality:
- Metallurgical and mechanical properties of the solder metal and compatibility with the metal on the surfaces to be joined
- Wetting
- Surface properties
- Grain structure in the solder metal.

3.10.1 Wetting

With poor wetting the solder metal will tend to contract into a spherical shape, seeking the minimum surface area because of surface tension in the solder metal, γ_l, Figure 3.14. If we have good wetting the surface tension between the liquid and the base material, γ_{ls}, dominates and stretches the drop out. The drop and the base material will minimise the free energy that also includes the surface tension in the base material, g_s. This can be described by Young's equation [3.13]:

$$\gamma_{ls} + \gamma_l \cos \Theta = \gamma_s$$

The surface properties that determine the wetting depend on many parameters. The combination of materials is of great importance. Purity is important, an oxide layer on top of copper or solder metal for example, may ruin the wetting. The surface structure and the roughness, are also important. In a good solder

joint the atoms diffuse from the solder metal into the surface of the base material down to 0.1 - 1 µm. In order to improve the wetting fluxes are used, as described in section 3.10.3 in this chapter.

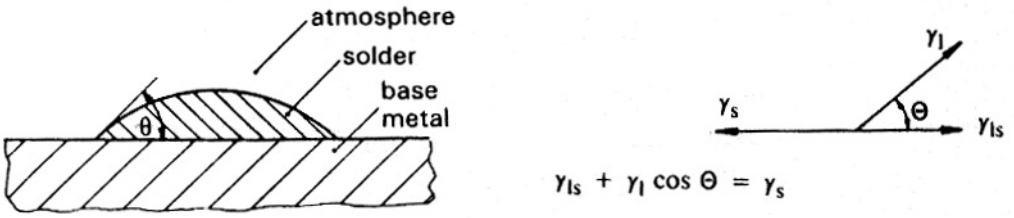


Fig. 3.14: Wetting in soldering.

3.10.2 Solder metal

It is most common to have a eutectic mixture of Sn/Pb: around 63 % Sn/37 % Pb (weight %). The melting point is 183 °C, see Figure 3.1. Some properties of solder metal are given in Table 3.6. Due to high price of tin a higher percentage of lead is often used. That will raise the melting temperature and it makes the wetting properties inferior. Even small concentrations of other elements change the properties.

Table 3.6: Properties of solder alloys 63 Sn:37 Pb or 60 Sn:40 Pb (weight %) [3.13, page 162].

	Temp. [°C]	Value	Unit
Electrical resistivity, ρ	25 100	0.17 0.32	µOhm•m "
Thermal conductivity, °K	25 100	51 49	W/m°K "
Thermal coeff. of expansion, α		24.5	ppm/°C
Specific heat		46 000	J/kg°K
Modulus of elasticity, E	25	32 000	N/mm^2
Density, ρ		8.5	g/cm^3

The mechanical properties of solder metal change strongly over the normal temperature range of operation of electronics, see Figure 3.15. This is because the highest temperatures approach the melting point. Below 0 °C the solder metal behaves elastic, whereas at the temperatures above room temperature it is plastic. That means that the mechanical built-in stresses, due to thermal mismatch with the other materials will relax and vanish over time. However, cyclical plastic deformations change the grain structure, weaken the solder fillet and can lead to fatigue. Such deformations occur e.g. in SMT (Surface Mount Technology) assemblies, please refer to Figure 3.16. The time until the solder fractures, depends on relative deformation (strain), temperature, frequency of deformation, etc., see Figures 3.17 a) and b). A simplified relationship is given by the Coffin-Manson´s formula [3.13]:

$N^{0.5} \times g_p = \text{constant},$

Where N is the number of cycles until fracture, and g_p is the relative deformation amplitude. In practice the relations are more complex. This can be explained by

the temperature changes that give rise to the deformations, and the material is plastic part of the time and elastic part of the time.

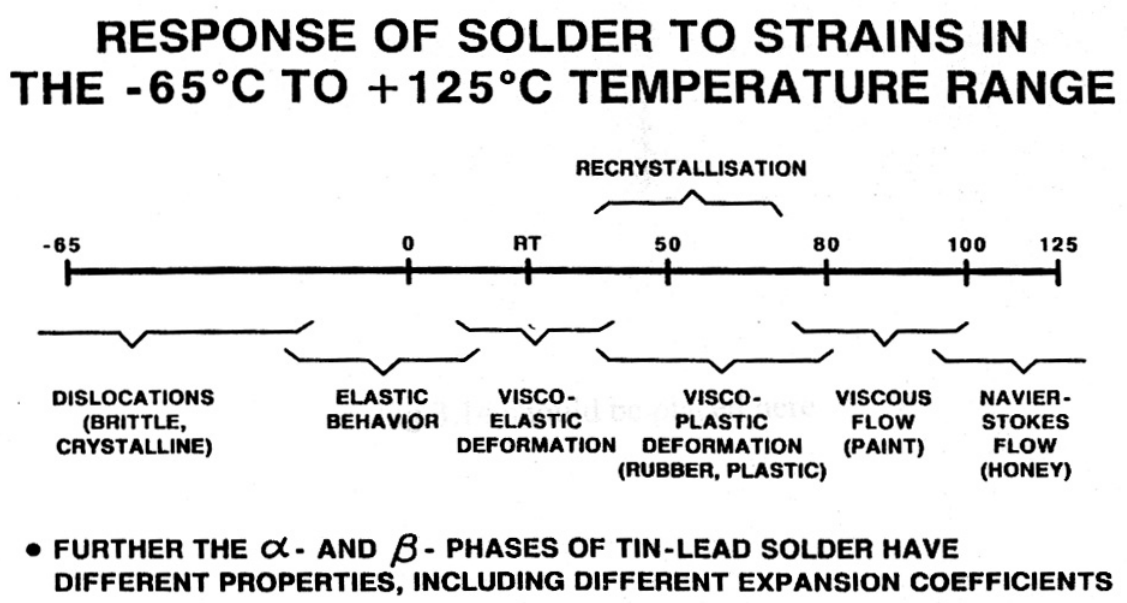


Fig. 3.15: Behaviour of solder metal at different temperatures, schematically. [W. Engelmaier].

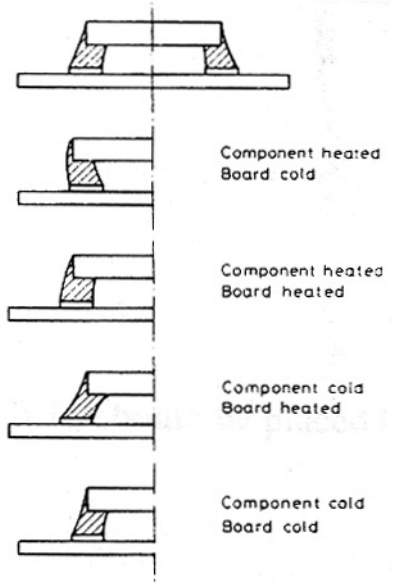


Fig. 3.16: Solder joint fatigue in surface mounted assemblies is often caused by power cycling.

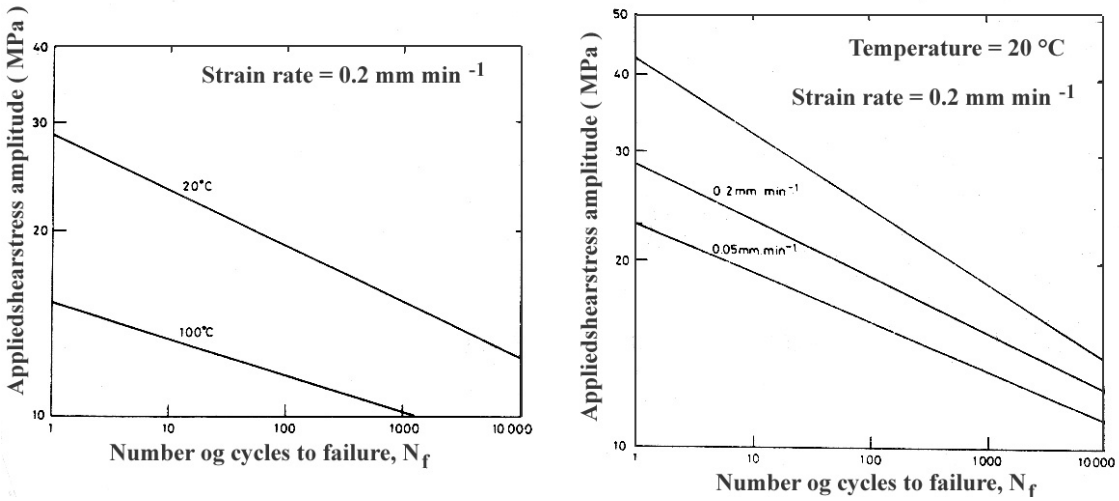


Fig. 3.17: Experimental data for fatigue in Sn/Pb solder fillet by cyclical mechanical stress. High temperature and low cycling frequency gives the fastest failure, because the grain structure relaxes most and is damaged [3.11].

SMD (Surface Mount Devices) resistors and capacitors often have silver in their terminals (please refer to Chapter 4), and the dissolution of the termination metal ruins the metallurgical and the electrical properties ("leaching" [3.11, p. 165]). For surface mounting it is therefore common to add 2 % Ag in the solder metal to impede the dissolution of silver into the solder metal, Figure 3.18. Another way to reduce the solubility is to alloy Pd or Pt into the silver in the component terminals.

Au in the solder metal may arise from Au component termination in certain component packages, please refer to Chapter 4. Gold dissolves very rapidly, as shown in Figure 3.18. It gives brittle, inter metallic $AuSn_4$ in the form of needles which weaken the mechanical strength in the solder fillet when the concentration is above 4 %.

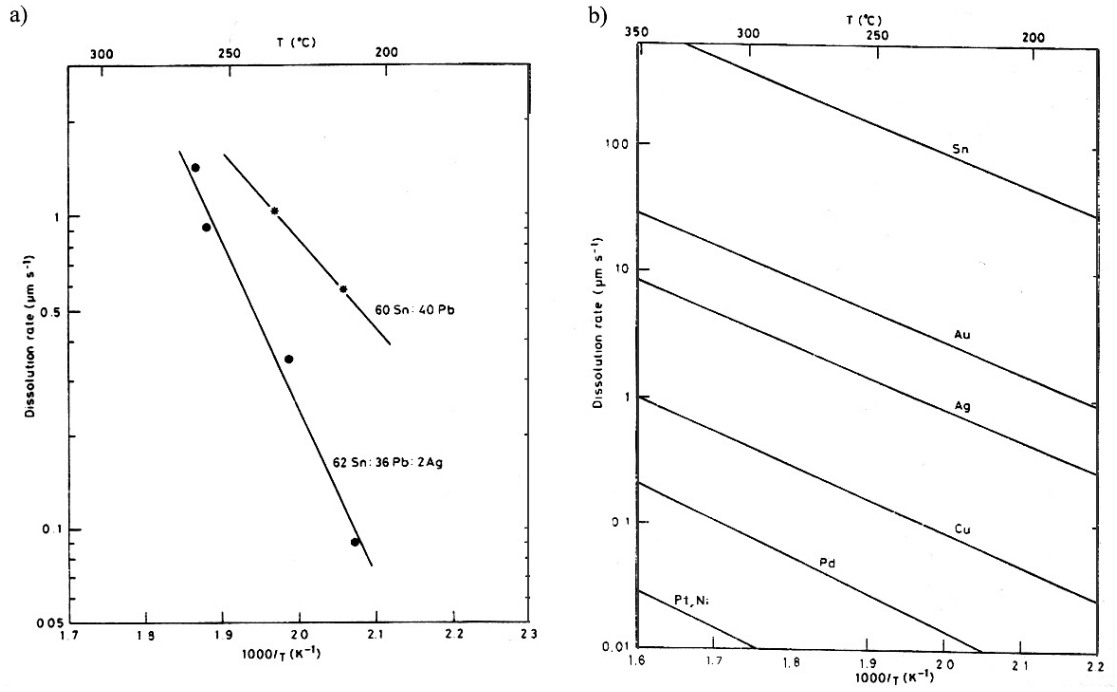


Fig. 3.18 a) Left: Dissolution rate of Ag in solder metal, and in solder metal with 2 % Ag, as function of temperature; b) Right: Dissolution rate of various metals in solder alloy [3.11].

Solder baths for mass soldering must be analysed periodically. Impurities such as Al, Zn, Cd change the properties of the solder metal and are not permitted above approximately 0.005 %. As, S, P are also harmful. Polluted solder metal is re-refined and used again.

For surface mounting solder metal in paste form is used for reflow soldering. This is described in Chapter 7.

Solder metal with a higher melting point may be useful for example for soldering of Si-chips (see below), when other components are to be soldered afterwards without melting the chip attached. 96.5 Sn:3.5 Ag, with a melting point of 221 °C is much used, and 5 Sn:95 Pb.

Solder metals with a low melting point can be obtained by adding In. They are also softer than normal Sn/Pb alloy, and they have better mechanical properties during thermal cycling. Properties of some important solder alloys are given Tables 3.6 and 3.7.

Table 3.7: Alloys for soft soldering [3.11]

Alloy System [mass%]						Code	Melting Temperature [°C]		Shear Strength at 1 mm min^{-1} [Nmm^{-2}]	
Sn	Pb	Ag	Sb	In	Bi		Solid	Liquid	20°C	100°C
100						Sn	232		22,1	19,0
63	37					Sn63	183	183	-	-
60	40					Sn60	183	188	33,6	21,6
50	50					Sn50	183	216	30,0	24,0
40	60					Sn40	183	234	34,3	13,7
10	90						275	302	28,9	14,7
5	95						310	314		
62	36	2				Sn62	179	179	43,0	18,6
10	88	2					268	299	-	-
5	93,5	1,5					296	301	23,8	15,7
96,5		3,5				Ag3,5	221	221	37,7	22,5
95			5			Sb5	236	243	37,2	21,1
	40			60		In60	174	185	-	-
	50			50		In50	180	209	-	-
37	37			25		In25	138	138	-	-
42					58	Bi58	139	139	50,0	19,5
15	33				52	Bi52	96	96	-	-
34	42				24	Bi24	100	146	34,3	17,5
43	43				14	Bi14	143	163	-	-

3.10.3 Flux and cleaning [3.11, 3.13, 3.14, 3.15]

Fluxes are used to improve the soldering and have several functions:
- Dissolve and remove harmful surface layers (oxide, etc.)
- Protect the surface against new oxidation
- Improve the wetting

Many types of flux are used. They consist of active ingredients dissolved in a liquid. They are of two main categories:
- Soluble in organic liquids
- Water soluble

The category determines how one will be able to clean the flux residues.

The common fluxes are also characterised as:
- Organic resin fluxes ("rosin")
- Organic non resin based fluxes
- Inorganic fluxes

Resin fluxes are most used and they contain natural resin from (pine-) trees, dissolved in alcohol, etc. It has a certain effect without additives, but it is normally "activated" by adding an organic chlorine compound: Dimethyl-ammonium chloride (DMA-HCl) or diethyl-ammonium chloride (DEA-HCl). The effect of the chlorine added is shown in Figure 3.19, while wetting of pure copper takes 6 seconds without activation, the time is below 1 sec. with 1 % Cl^- - content.

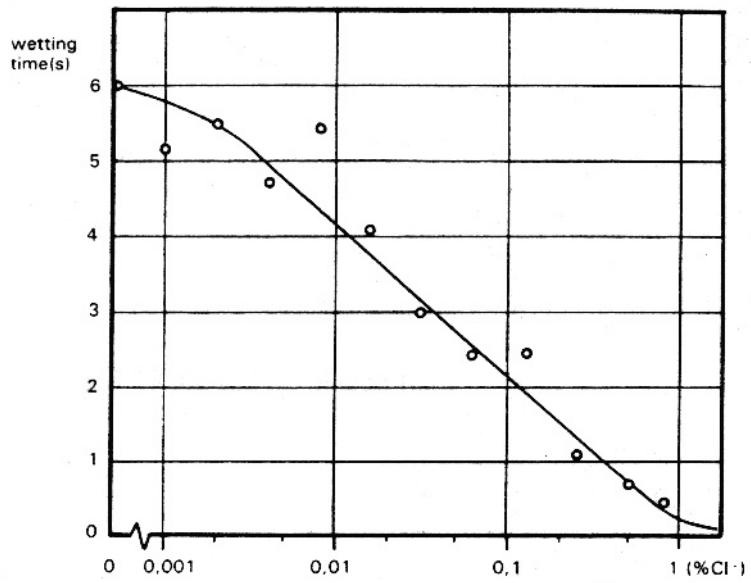


Fig. 3.19: Time for solder alloy to wet a pure Cu surface, depending on the activation of the solder flux. The degree of activation is given by the concentration of Cl^- ions in the flux (temperature: 230 °C) [3.13, page 232].

The following symbols/designations characterise the fluxes:

- R (Rosin, non-activated): Resin flux without chlorine added. It acts because of weak acids in the resin
- RMA (Rosin mildly activated): Up to 0.5 % Cl content
- RA (Rosin, activated): Higher content of chlorine

Chlorine is strongly corrosive, and if it remains on the surface after the solder process is completed it may give reliability problems later. A suitable cleaning process after soldering removes the residues. In many types of products it is accepted to use R and RMA flux without washing, but RA flux must be removed. All inorganic flux residues must also be removed.

Popular organic cleaning agents have been trichloro-trifluoro-ethane (Cl_3CCF_3 also designated TCTFE) mixed with an alcohol. One type is made by DuPont under the name Freon [3.13, page 45]. TCTFE has many good properties: It is efficient, does not burn, it is not poisonous and is chemically inert to most materials in electronics.

Like many other chlorine-fluorine-carbon combinations (CFC) TCTFE is very stable. Due to its low boiling point the vapour will spread in the atmosphere and the chlorine combinations will over long time break down the ozone layer [3.13, 3.14, 3.15].

TCTFE and similar combinations are now prohibited from use in most countries (the Montreal accord). Cleaning agents based on alcohol, cleaning with soap, etc. are replacements, and an extensive development work is taking place in fluxes that do not need to be removed. For certain purposes the soldering is performed in an inert or reducing atmosphere, without use of flux that has to be removed.

3.11 GLUING [3.11]

Gluing is used in electronics to:

- Assemble mechanical parts and keep electronic components in place
- Give electrical connection, as a replacement for soldering
- Give good thermal contact

The types of adhesives used are polymers, that generally are electrically and thermally insulating, often epoxy (or acrylic, phenolic, polyimide, etc.). Electrical conductivity and better thermal conductivity is achieved by adding conductive particles to the epoxy, most often silver (typically 85 weight %). It gives electrical resistivity in the region 1 - 10 x 10^{-6} Ohm•m, compared to 0.17 x 10^{-6} Ohm•m for the Sn/Pb solder alloy (room temperature). Improved thermal contact may also be achieved by mixing ceramic particles (Al_2O_3, AlN) into the adhesive. Thermal conductivity for epoxy without additives typically is 0.2 W/°C • m, and silver filled epoxy has up to 10 x higher value, see Tables 3.1, 3.4, Figure 3.20, and [3.16].

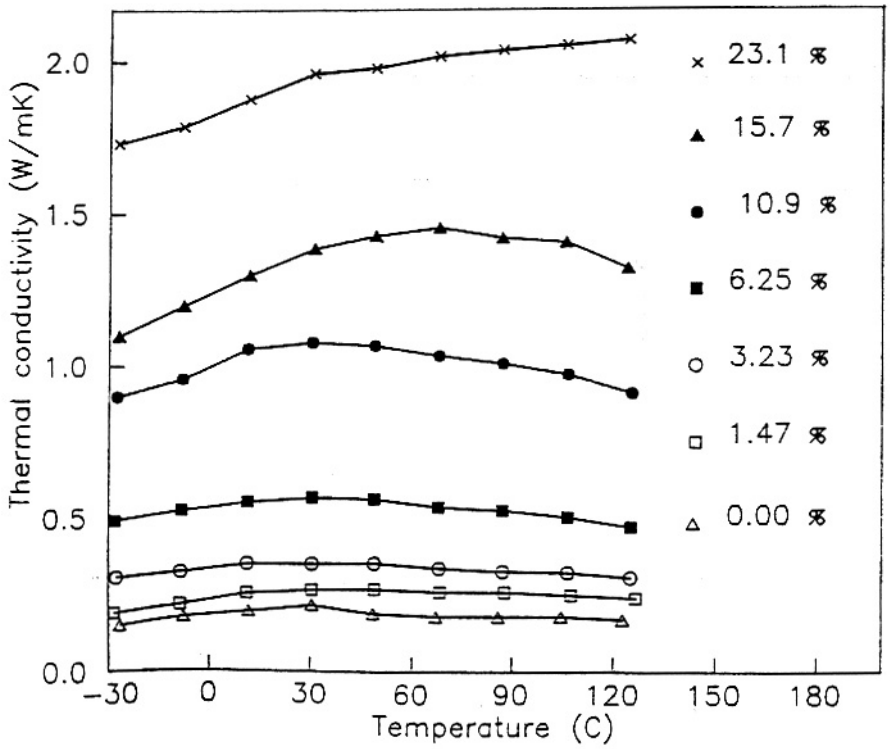


Fig. 3.20: Thermal conductivity of epoxy adhesive with various amounts of Ag [3.16 a)]. The concentration is in volume % Ag. (23 vol. % corresponds to approximately 80 weight %).

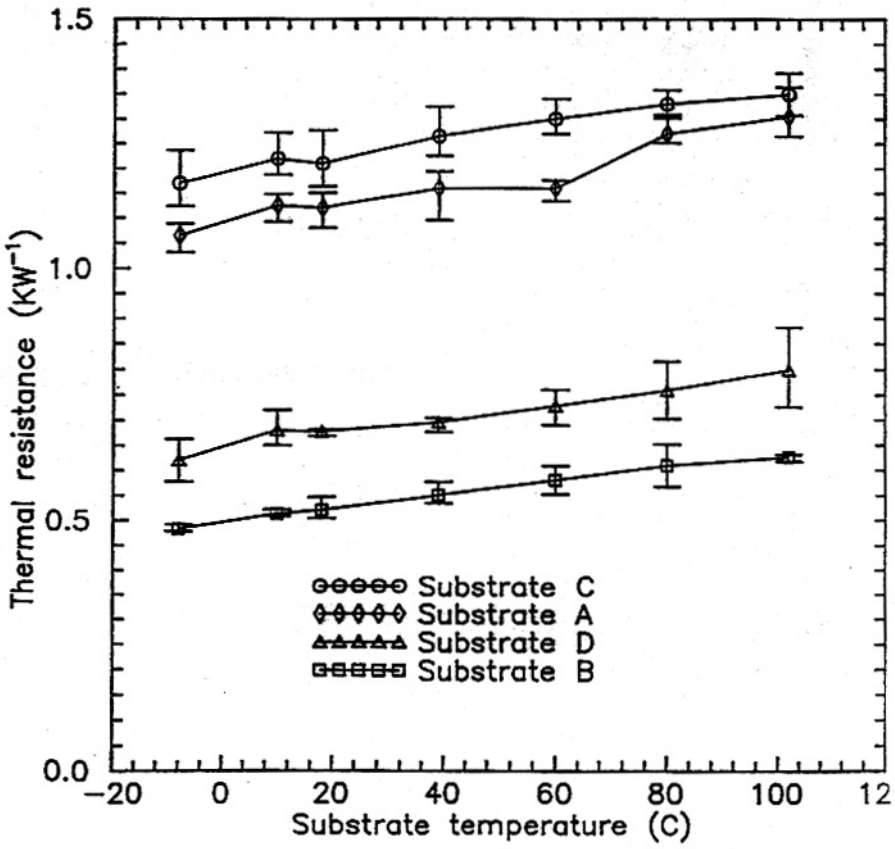


Fig. 3.21: The thermal resistance from the electronically active part, on top of the Si chip (¨junction¨) through a bonding layer of glue or soft solder and a thin alumina ceramic layer covered with Cu (¨direct copper bonding¨, please refer to Chapter 8) to heat sink. The samples with chips bonded by gluing, C and A, have approximately twice as high total thermal resistance as those which are soft soldered, D and B. Details are described in [3.16 c]

The adhesive is deposited by screen printing, dispensing, or in the form of a partly cured dry film cut to the right size, "preform". The curing takes place with heat, or by UV-radiation for certain types.

Replacement of component soldering by use of electrically conductive adhesives is an active topic of research. Gluing requires lower process temperature with less stress on the components and substrate, and we avoid the use of flux, cleaning and poisonous lead. Many researchers believe that better long term reliability can be achieved, because the adhesive is more elastic and deforms less than the solder metal. This work os not yet conclusive and gluing is not yet extensively used.

On the other hand the absorption of moisture in the adhesive polymer may reduce its strength as well as cause migration of the silver. Fine silver threads "grow" out from the silver particles in the presence of an electric field, and they can short circuit conductors in the neighbourhood.

For components with many closely spaced terminals the gluing may give lower failure rate than soldering during the mounting. "Anisotropically conductive adhesive" is used, screen printed over the whole area under the component. The adhesive has a low concentration of conductive particles, Figure 3.24, so that the probability of a short circuit horizontally between two terminals is negligible, but vertical contact between terminal and the substrate, through at least one particle, is virtually certain to occur. An interesting alternative method of contacting is to use insulating instead of conductive adhesive, please refer to Figure 3.24. By use of mechanical pressure during the curing, the adhesive is pushed away, and we get direct physical contact between terminal and substrate at points on the slightly non-uniform surfaces. The polymer shrinks during the curing and causes a permanent force that holds the materials together with good reliability [3.17]. These methods are particularly suitable for components with low current (such as LCD-displays).

3.12 MOUNTING OF THE SEMICONDUCTOR CHIPS: DIE BONDING

Before electrical connections are made to the chip, the chip must be mounted on the base by "die bonding". That takes place by a eutectic bonding, soft soldering or gluing. Important points with the die bonding are: High electrical conductivity if current runs from the chip to the substrate, good thermal conductivity if the chip dissipates much heat, mechanical strength and reliability. Die bonding may be a critical point in demanding applications.

3.12.1 Eutectic die bonding

Eutectic bonding takes place when an eutectic alloy is created between silicon and a metal system deposited underneath (or with a preform placed between the chip and the substrate). The melting point for the eutectic composition is much below that of the pure elements. Au/Si alloy is often used (melting point 363 °C at 96.7 Au:3.3 Si, while Au melts at 1063 °C, Si at 1412 °C) or 80 Au:20 Sn (melting point 280 °C).The process takes place in an inert atmosphere. Eutectic bonding gives very good electrical and thermal contact and high mechanical strength. However, it is very brittle and when the chips are large the thermal mismatch may cause the chip to crack during the bonding process or during thermal cycling later. Use of gold-rich alloys also makes it costly.

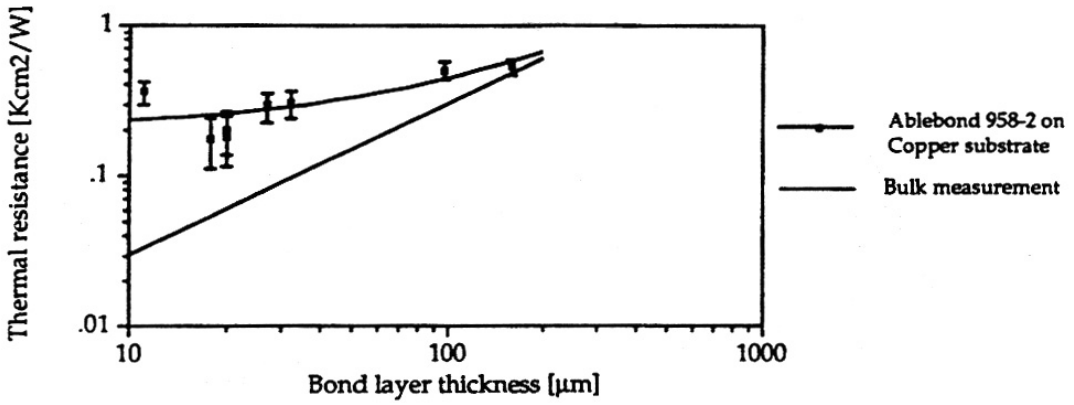


Fig. 3.22: Thermal resistance from junction to heat sink through adhesive of various thicknesses. For thick layers the resistance approaches the value calculated, based on the bulk thermal conductivity of the adhesive. For thin layers the resistance is higher, approaching a constant value, which indicates an "interface thermal resistance" caused by defects in the adhesive layer. For details, please refer to [3.16 b)].

3.12.2 Soft soldering

Soft soldering is used for large chips, particularly in power electronics, where good thermal and electrical conductivity is important. PbSn, AgPb, SnAgIn and other alloys are used. They are softer than the SiAu eutectic, the temperature in the process is lower and they can take up thermal mismatch by plastic deformation. They are more robust against fatigue than the common SnPb eutectic, but after many thermal cycles the soldering still may fracture due to fatigue.

The soldering of chips is made by screen printing of solder paste or by use of a solder preform. It takes place in inert or reducing atmospheres, without flux, to avoid gas pockets or flux residues that may corrode during long term use or which may cause hot spots in high power chips.

3.12.3 Gluing

Gluing is the dominating method of mounting. It is normally made with electrically and thermally conductive epoxy, see above. Cracks and damage due to thermal mismatch may be a problem with epoxy, but one can obtain soft types that are suited for large chips. One limiting factor for high power chips may be the poor thermal conductivity of the glue, see Figures 3.20 and 3.21, from [3.16 a) and c)]. Even when the adhesive thickness is made very thin there is evidence for an interface thermal resistance due to damage caused by the thermal mismatch between substrate and the Si chip, please refer to Figure 3.23 [3.16 b)]. During thermal cycling the adhesive will crack or lose its adhesion to the substrate and the Si chip, please refer to Figure 3.24 [3.16 d)], and the thermal resistance will increase further. The severity depends on chip size, temperature excursion and thermal mismatch between chip and substrate material, as well as the elastic modules and other properties of the adhesive. A different kind of chip gluing is done with silver filled low melting glass.

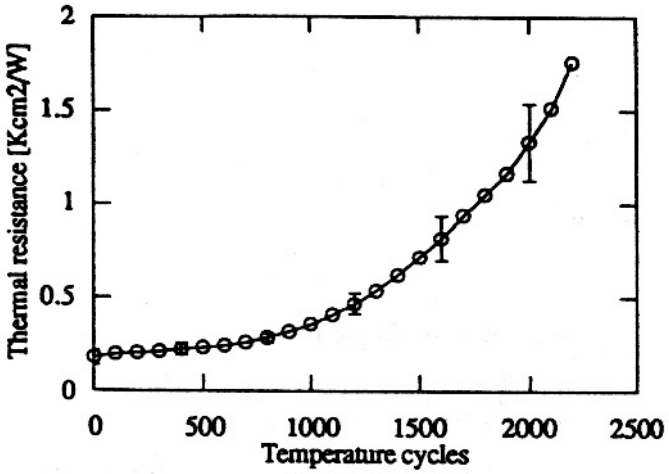


Fig. 3.23: Thermal resistance through an adhesive die bond between an Si chip and a Cu substrate, as a function of the number of thermal cycles between 10 °C and 150 °C. The increasing resistance is evidence of defects developing in the adhesive due to cyclic stress [3.16 d)].

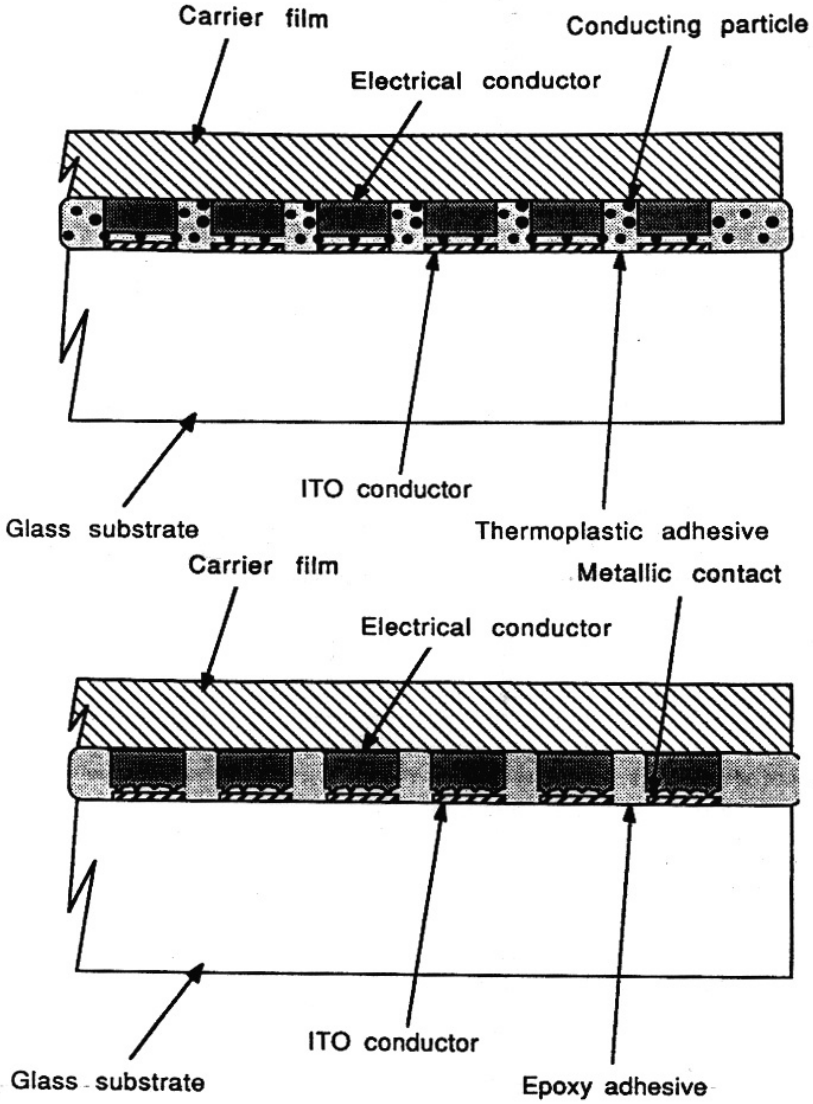


Fig. 3.24: Use of adhesive for contacting IC-chips with small pitch, schematically [3.17]: a): Anisotropic conductive adhesive, the conduction is through the metal particles in the adhesive; b): Electrically insulating adhesive, the conduction is through point contacts where the adhesive has been squeezed out.

3.13 WIRE BONDING

The most common methods for electrical connections to the semiconductor chip are mentioned in section 2.6: Wire bonding, tape automated bonding (TAB) and flip chip, see Figure 2.8. (In addition beam lead has been used for special purposes for many years [3.2].) Wire bonding is the dominating, well-established method and we will start describing this method.

Thin metal wires are connected one by one between the contact points on the semiconductor chip and the corresponding contact point on the substrate outside the chip. The wires normally are made of gold or aluminium, 0.025 - 0.5 mm in diameter. Al bond wire with rectangular cross section is also used. The substrate surface is normally covered on the bonding pads by soft (high purity) gold, deposited by plating or screen printing. The bonding wire is stretched out through the hole in a capillary tube. The connection to the chip is made by pressing the wire down onto the Al metallisation on the bonding area of the chip, against the edge of the capillary. There are several processes:

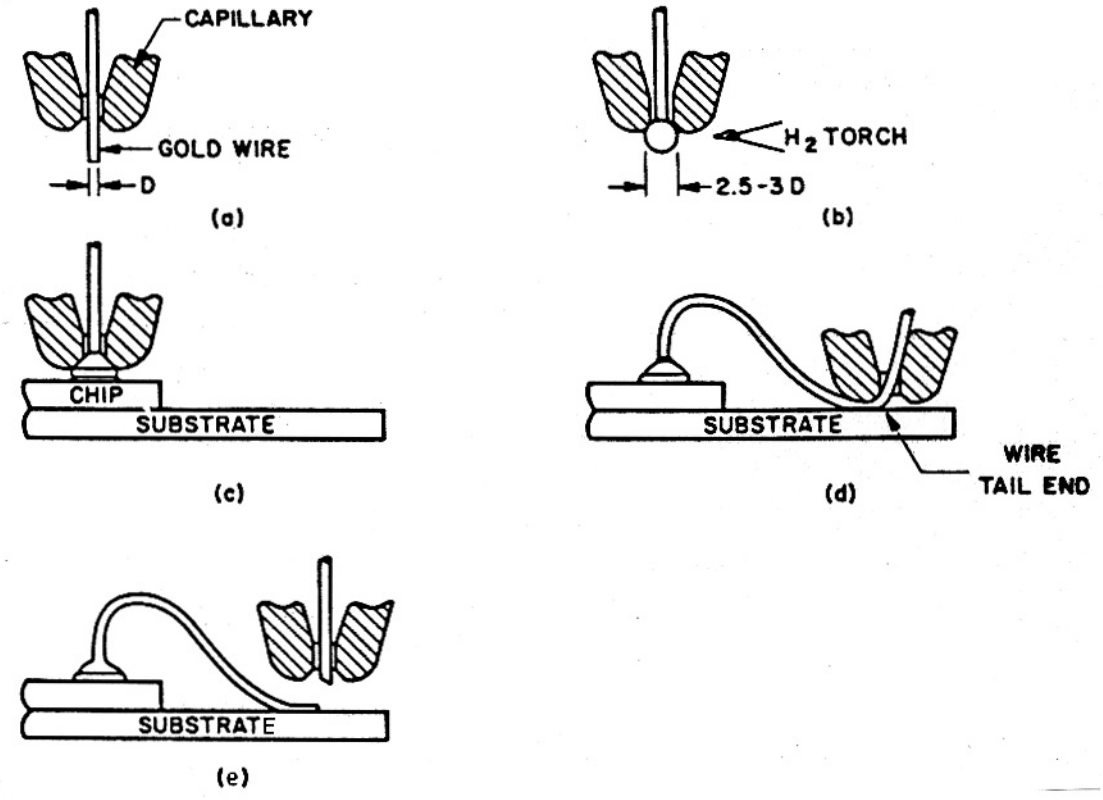


Fig. 3.25: The steps in wire bonding. a): The gold wire comes out of the capillary. b) A ball is created by melting the tip of the gold wire with a hydrogen flame. c) The ball is bonded to the Si chip with heat, pressure and possibly ultrasound vibration. d) The conductor is stretched and bonded to the substrate. e) The wire is torn off when the capillary is pulled up while the wire is held firmly inside the capillary.

- Ultrasonic bonding: Here the capillary vibrates with high frequency during the bonding, and the wire is cold-welded to the base by a combination of pressure and vibration. In addition to the softening of the gold, the vibrations also break up surface oxide layers. The technique is

used most for aluminium wire with flat ends on both sides ("wedge - wedge" bonding).

- Thermocompression bonding: The substrate and chip are heated to about 150 °C during the bonding process. This process is mainly used for gold wire, forming a gold ball at one side and a flat compressed wire end at the other side ("ball - wedge" bonding).

- Thermosonic bonding is a combination of the two previous methods.

The process steps in ball - wedge bonding are shown in Figure 3.25. The end of the gold wire that sticks out of the capillary is brought to melting with a hydrogen flame and it creates a small spherical ball. The capillary is moved down onto the aluminium bonding area on the Si chip, and it is pressed down, making the soft gold flat and sticking to the Al surface. The capillary is pulled up and it is moved over to the substrate bonding area, where it is pressed down and the bonding wire is squeezed flat. Then the capillary is pulled up, while the wire is held firmly inside the capillary and is torn off. The capillary is moved to the next terminal and the cycle is repeated.

Bonding machines are available as manual, semi-automatic and completely automatic units. The automatic machines have a camera for pattern recognition. Two registration marks on the chip are recognised by the camera and it tells the machine exactly where the chip is located. Two other registration marks on the substrate define exactly the position of the substrate relative to the chip. Teaching of the machine takes place in advance, whereby one programmes the co-ordinates for the registration pattern, and manually bonds one chip. The machine then learns the position of each bonding area relative to the registration patterns on both chip and substrate. The speed of machines used today is up to 10 bonds per sec. The failure rate may be less than 0.1 %.

Normal dimensions of the bonding areas are approx. 100 x 100 μm, and centre to centre distance 200 μm (pitch). It is possible to get down towards 60 μm pitch. Normally the bonding areas are in one row along the edges of the semiconductor chip, but it is possible to have two staggered rows without short circuiting the bonding wires. With a typical maximum chip size of today (over 20 mm side), there is an upper limit of approximately 1000 terminals for wire bonding.

A comparison between the properties for wire bonding, TAB and flip-chip is shown in Table 3.8.

Table 3.8: Comparison of wire bonding, TAB, and flip chip soldering [3.22]

Bonding technology	*Wire Bond*		*TAB*	*Flip-Chip*
Material(s)	Al	Au	Cu	Pb-Sn
Melting temperature [°C]	660	1064	1084	310
Bonding geometry	25 µm diameter x 2,5 mm length		25x100 µm tape x 2,5 mm length	125 µm diameter 100 µm height
Typical pitch [µm]	170 µm perimeter		200µm perimeter	250 µm area
Minimum Pitch [µm]	60 µm perimeter		70 µm perimeter	50 µm area
Strength per bond [gram]	6	10	50	30
Lead resistance [mOhm]	142	122	17	1,2
Interlead capacitance [pF]	0,025	0,025	0,006	<0,001
Lead inductance [nH]	2,6	2,6	2,1	<0,2
Thermal resistance [°C/mW] per bond	80	52	8	0,5
No. of I/Os per chip				
Typical pitch 8 mm chip size	184		160	1024
Minimum pitch 8 mm chip size	266		400	15150

3.14 TAPE AUTOMATED BONDING (TAB) [3.1, 3.2, 3.17]

When tape automated bonding is used a conductor pattern has been made in advance, fitting the semiconductor chip and the substrate bonding pad patterns, as described in Section 2.6, Figure 2.8. The conductor foil is on a carrier of polyimide film, please refer to Figure 3.26. The conductors are bonded to Au bumps on the chip.

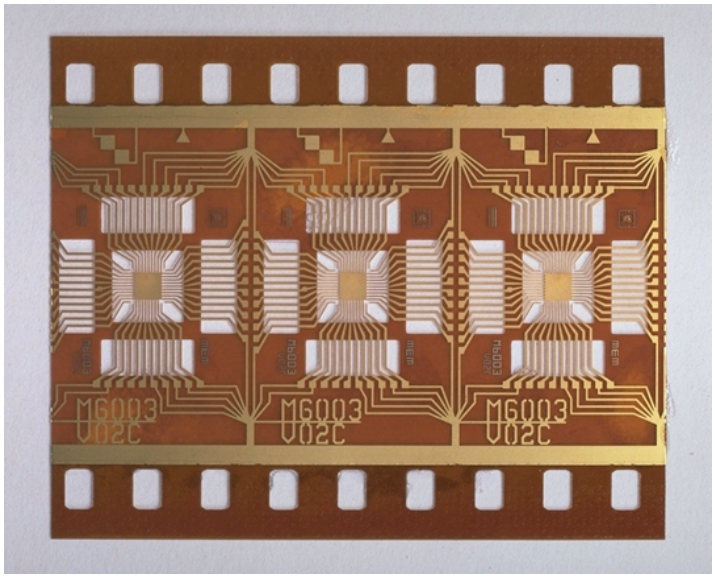


Fig. 3.26: A picture of a TAB film with the Cu pattern, as well as the holes in the film for excising the circuits, and the sprocket holes for moving the film during processing.

3.14.1 Process

There are a number of different varieties of TAB and TAB processes. Below we describe the most common type, please refer to Figure 3.27. Other alternatives will be commented on afterwards.

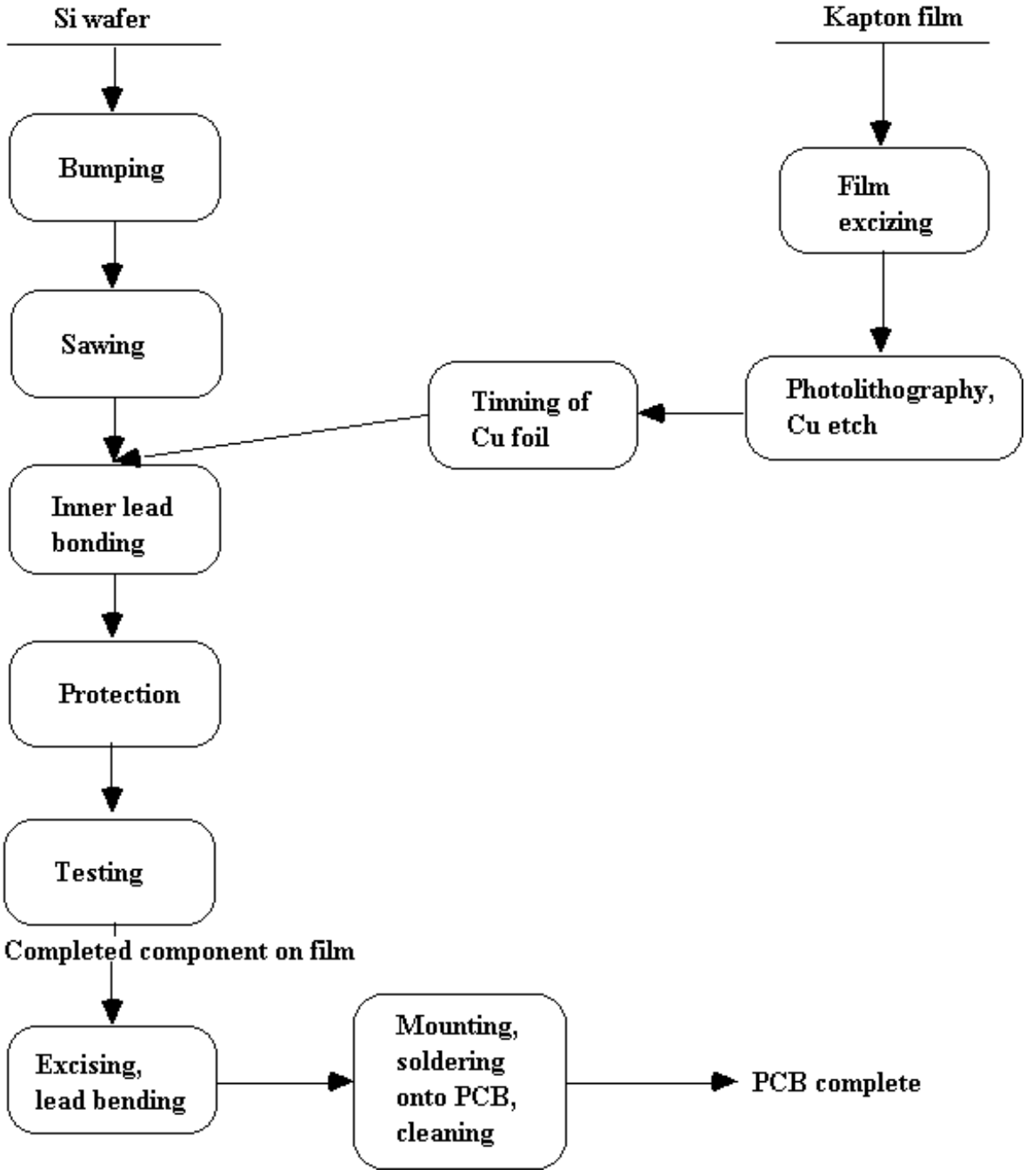


Fig. 3.27: The main steps in TAB processing.

Fabrication of gold bumps

Gold bumps are formed on processed Si wafers, please refer to Figure 3.28. First a metal system is deposited having the following functions:

- Covers the Si surface with a conducting layer, such that electrolytic plating can be used
- Prevents gold from diffusing into Al and Si (diffusion barrier)
- Gives better adhesion for the gold

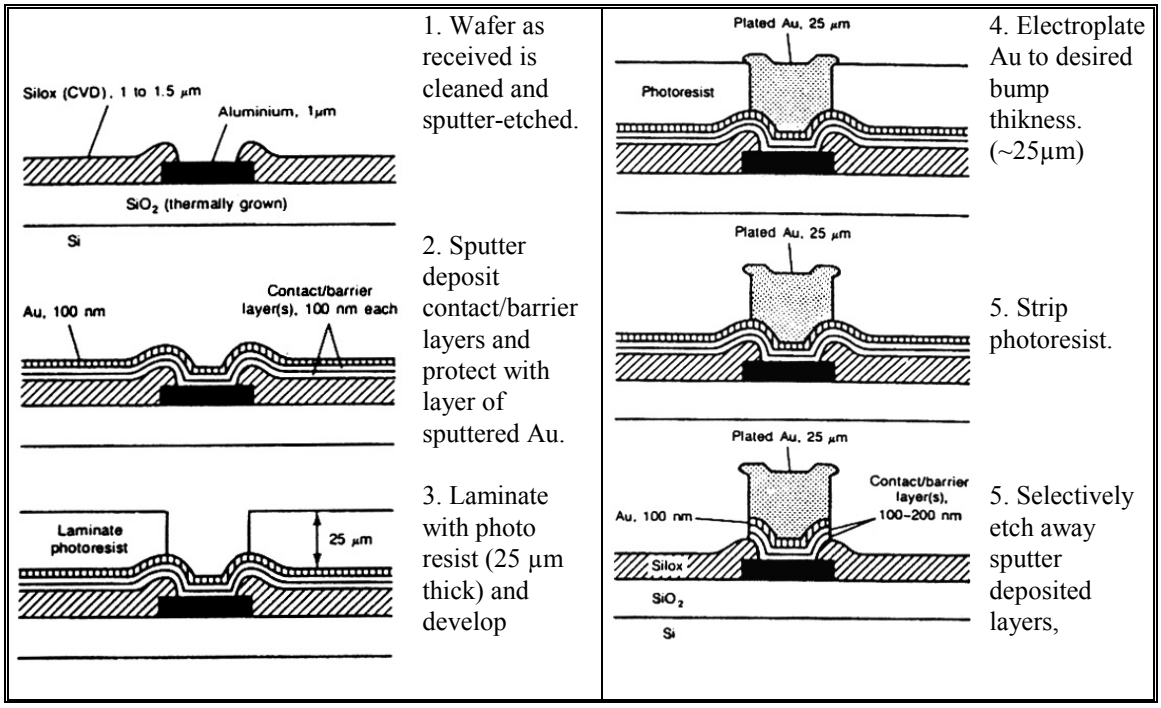


Fig. 3.28: The process for fabricating TAB bumps on the semiconductor chip [3.18].

For this the metal system Ti/Ni/W often is used (Approximately 1000 Å of each metal that is sputtered on).

Afterwards a layer of thick photoresist is deposited, openings at each bonding area are then made by photolithography and approximately 25 μm of high purity (soft) Au is electroplated with the photoresist as plating mask. Often the photoresist is thinner than this, and the gold bumps grow laterally and become greater at the top, in a characteristic mushroom shape. Then the photoresist is stripped, and the barrier metal system is etched off outside the gold bumps.

Then the wafers are cut into individual chips. The chips are now ready for inner lead bonding (ILB) of the TAB film with Cu pattern, which is made by its own process.

Fabrication of TAB film

The starting material for normal 3-layers TAB film is polyimide (often designated Kapton, which is DuPont´s trademark). Sprocket holes for handling, analogous to those on camera film, are punched along the edges of the film, as well as windows for the Si chip. Copper foil is laminated onto the polyimide, with an adhesive layer between. The conductor pattern in the Cu foil is defined by photoresist that is illuminated through a photo mask with the pattern on it.

Then developing follows and etching of the foil. The conductor pattern is tinned or gold plated. An example of such a pattern is shown in Figure 3.26.

35 mm wide film is the most common, with standard dimensions like for camera film. Also 8,16 and even 70 mm wide films are in use.

Inner lead bonding (ILB)

Inner lead bonding is the mounting of the semi-conductor chip onto the TAB film. It is normally performed by thermocompression bonding. The bonding tool, the thermode, see Figure 3.29, is of hard metal or diamond. It is pressing all Cu ends against the soft gold bumps simultaneously, "gang bonding". The process takes approximately 1 sec, at a temperature of 300-400 °C. A drop of epoxy is applied on to the chip for mechanical protection and environmental protection encapsulation. The chips may be tested with probes that contact the test points on the Cu conductor pattern on the TAB film.

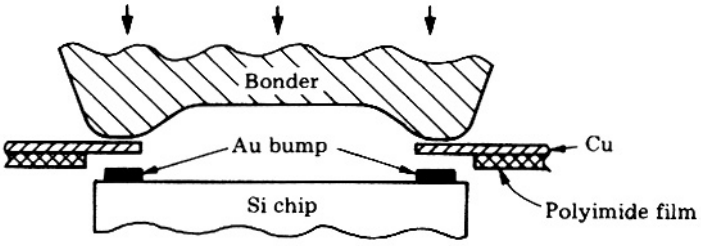


Fig. 3.29: Inner lead bonding.

The film with Si chips is rolled on to a reel. This is the stage where most users of TAB circuits buy them, regardless of whether they are standard or custom designed circuits.

Mounting, outer lead bonding (OLB)

The mounting of the TAB circuit on the printed circuit board consists of three steps:

- Excising of Si chip with short Cu conductors from the TAB film with a cutting tool that is made for the dimensions of that particular circuit.
- Bending of the leads, so that the outer ends are in the plane of the underside of the Si chip ("lead bending"), also with a dedicated bending tool.
- Placement of the chip on the printed circuit board and soldering the outer ends of the Cu leads.

The connections on the printed circuit board are normally made by pressing the copper lead ends down into solder paste or reflowed solder metal on the board. The soldering is most frequently performed with a "solder-iron" in the form of an electrically heated frame, this tool is also called thermode, for outer lead bonding. The frame solders TAB chips individually by pressing the Cu leads down into the solder metal and supplies heat by a pulse that lasts a few seconds. The process is called thermode soldering, impulse soldering or hot bar soldering, see Figure 3.30. The OLB thermode is cooled below the melting point before it is lifted up. The complete cycle takes 10 - 20 seconds.

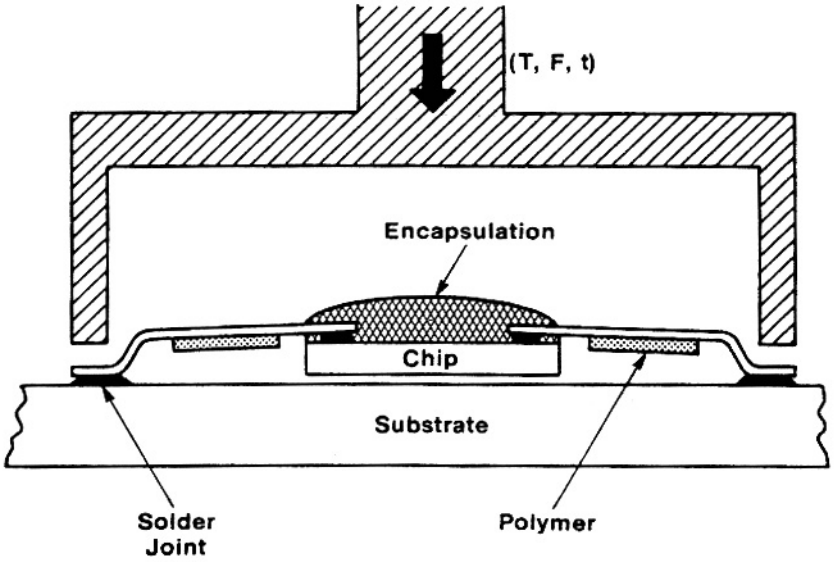


Fig. 3.30: Outer Lead Bonding (OLB) by thermode soldering.

3.14.2 Advantages and disadvantages of TAB technique

Some of the advantages of TAB are the following:

- It requires less bonding area for each contact on the semi-conductor chip, and smaller distances between the terminals than wire bonding. It therefore saves chip area at the same time as it makes it possible to interconnect chips with a larger number of terminals (up to approximately 1000).
- The outer lead bonding requires considerably less space on the printed circuit board than the same chip in a regular package and often less space than the same chip connected with wire bonding. The mounting is simpler and more robust than wire bonding.
- The gold bump on each bonding area gives a hermetic enclosure of the Al metallisation underneath. This reduces the possibility of corrosion, and the reliability is improved. Therefore TAB is suitable for use without additional encapsulation. (The epoxy drop mentioned above is still the most common.)
- The gang bonding operation is a more efficient process than wire bonding that is made one bond at a time, and has a higher production yield.
- TAB film can also be used as a separate, flexible little printed circuit board, on which it is possible to mount other components as well. (This is made e.g. in the Swiss Swatch watches, where all the electronics is on one TAB film.)

TAB is not yet extensively used, for the following reasons:

- It requires non-standard process of the Si chips (deposition of the gold bumps).
- It requires special fabrication of carrier film and conductor pattern that is costly and takes time.
- The mounting on the PCB requires special mounting equipment, and a separate tool for each individual component geometry. Individual mounting/soldering of each component is time consuming and costly.
- Repair (replacement of a defect component) on the PCB is demanding.

- Few standard circuits are available in TAB form. Few firms supply production on a subcontractor basis.
- There is little standardisation of dimensions and tooling, which increases the costs.

3.14.3 Alternative processes

Among the many alternative forms of TAB we may mention:

- The bumps can be made on the TAB film by plating ("bumped tape"), instead of on the Si chips ("bumped chip"). This simplifies the wafer processing, but the bumps of hard copper gives a more demanding inner lead bonding process and is a non-hermetic enclosure of the bonding area. It is also possible to make the Au bumps separately and transfer them to the wafer ("transfer TAB")
- One or two layer films: One layer film is only an etched Cu foil. It is not possible to test on the film, because all conductors must necessarily be interconnected and short circuited. One layer film has been in use for simple low price circuits for many years by National Semiconductor. Two layer film does not have a layer of adhesive. The Cu foil is plated on to the polyimide film instead of being laminated on.
- "Single-point bonding": For chips with a large area and many inputs and outputs a non uniform pressure on the contact points during gang bonding is a problem. This can lead to damage of the chip during inner lead bonding, or unreliable soldering for some of the terminals during outer lead bonding. Single-point bonding may be of help. The equipment for such bonding has a thermode that only touches and bonds one terminal at a time, then it moves to the neighbouring terminal. That also gives more process flexibility, because it can be programmed to bond accordingto the geometry of a new chip, without fabrication of a new thermode. However, the bonding requires long time and is very time consuming in large volume production.
- Area-TAB: Normally all contact points are along the periphery of the chip. For chips with many in-/outputs it may be very space saving to have contacts also at the inner parts of the chip area. This has been demonstrated for TAB, but it has not come into much practical use, because of process difficulties with the Inner Lead Bonding.
- Alternatives for Outer Lead Bonding: In addition to thermode soldering, IR soldering, vapour phase soldering, laser soldering and welding are used. Gluing is also used, please refer to Section 3.11.

Using the tape automated bonding technique one can easily process chips with less than 100 x 100 μm Al bonding areas, and 100 μm separation. With vertical walls on the Au bumps and advanced processing TAB technology has been demonstrated for a pitch between bonding areas of 50 μm, and more than 1000 terminals on the chip.

3.15 FLIP CHIP SOLDERING [3.1]

Direct soldering between the electrical contact points on the semi-conductor chip and points on the component substrate is designated "flip chip" because the chip is turned upside down, please refer to Section 2.4. "Solder bump" or C4 for "Controlled Collapse Chip Connection" (IBM's terminology) are other designations.

With this technology a bump of solder metal is formed on each bonding area on the silicon chip, please refer to Figure 3.31. The wafer is heated to reflow the solder metal and the chips are separated. Each chip is turned upside down and placed very accurately in position on the corresponding solder areas on the substrate. Then one heats up until reflow of the solder metal takes place again.

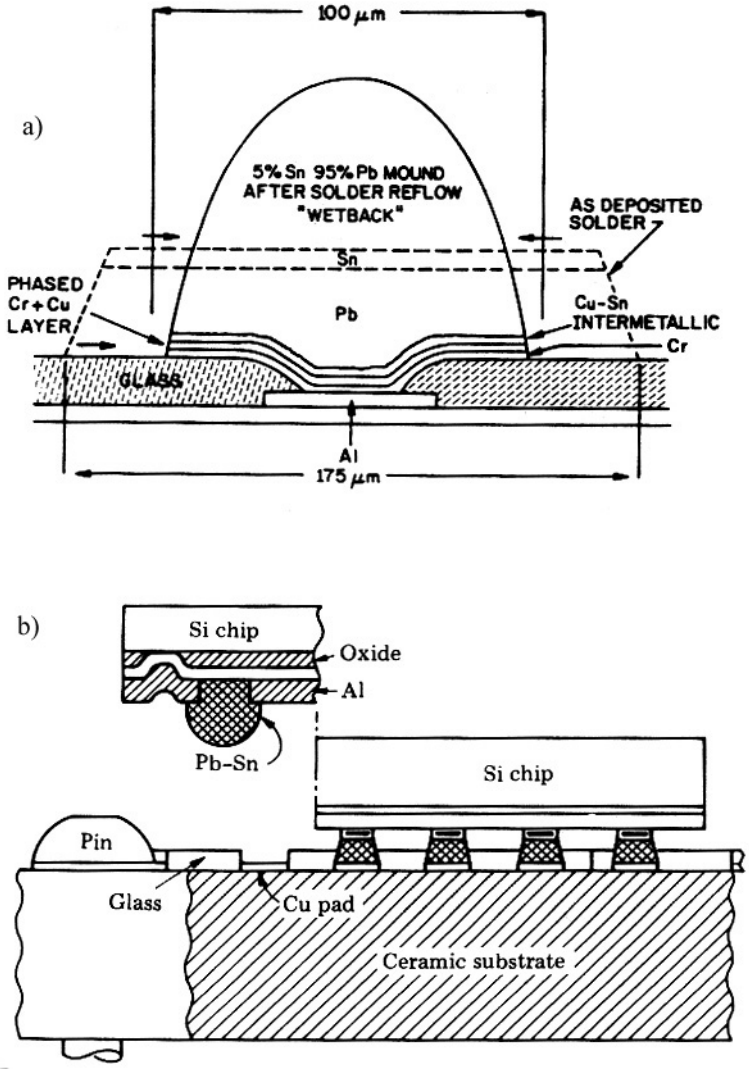


Fig. 3.31: Flip chip soldering: a): The metals for the solder bump before reflow (dashed lines) and after reflow; b): Bump before the soldering of the chip onto the substrate and after soldering.

A great advantage of flip chip is that one gets a placement on the substrate that does not require more space than the chip itself. In addition one can have terminals everywhere on the chip area, not only along the periphery. Flip chip soldering of chips with 10 000 terminals has been demonstrated. The electrical

properties are better than for other mounting methods, with low electrical resistance and low inductance, see Table 3.8.

The fabrication of the bumps takes place before the silicon wafer is cut. First a metal barrier layer is deposited, for example thin films of Cr/Cu/Au. Cr gives adhesion to the passivation on the Si chip around the Al metallisation. Cu gives a solderable surface, and a thin layer of Au prevents oxidation of the Cu. The solder metal may be 95 % Pb/5 % Sn (melting point approximately 305 °C), or an In alloy. It is deposited on the chip by sputtering or vacuum deposition through a metal mask with an opening for each bump, or by photolithography and electroplating, analogous to Au bump forming in TAB. For prototypes it is possible to place spheres of solder metal on to each terminal manually.

After deposition the solder metal is reflowed in a hydrogen atmosphere. This is done to homogenise the composition of the alloy, and to let the surface tension generate a spherical shape of the bumps. The reducing atmosphere removes oxides, which will otherwise ruin the solder ability. The bumps typically have diameter 100 μm.

The Si wafer is cut, and the chips are ready for mounting. That is done by turning them upside down as mentioned, and placing them accurately on the substrate, which is heated to reflow again. Water- or resin-based flux is used, but the subsequent cleaning is very critical. A certain amount of self-alignment is achieved because of the surface forces in the molten solder metal, which try to move it to the location where the total surface in all solder joints is a minimum. That is where the position is perfect.

A problem with flip chip soldering is the lack of thermal flexibility, because of the short "conductors" between chip and substrate. Therefore it is best suited for silicon substrate or for small chips on Al_2O_3 or AlN substrate. The heat conduction is not so good, unless one also has a thermal contact to the back side of the Si chip, please refer to Chapters 4 and 8.

IBM has used flip chip soldering since 1964, but few other companies have used the method in volume production until the last years. Areas of application today are mostly for multichip modules in computer- and telecommunication applications where extreme performance and minimum space are required.

3.16 PLANAR BONDING WITH ADAPTIVE ROUTING [3.2, 3.21]

For future complex semiconductor circuits there is a need for several thousand in- and outputs with a higher density than even flip chip can provide. An interesting method that is under development is called "planar bonding". In one version [3.2, page 308] a silicon wafer with crystallographic orientation (100) is used as substrate, see Figure 3.32. Holes are made in the wafer by anisotropic etching for all the ICs that are to be mounted. The chips are glued in from the back side, such that the surface with the conductor pattern is planar with the substrate surface. (Alternatively a ceramic substrate may be used with holes or cavities.) Thereafter a polyimide film is deposited all over the surface, via holes to the chip pads are laser "burned", and thereafter a conductive layer of titanium or chromium is deposited by sputtering.

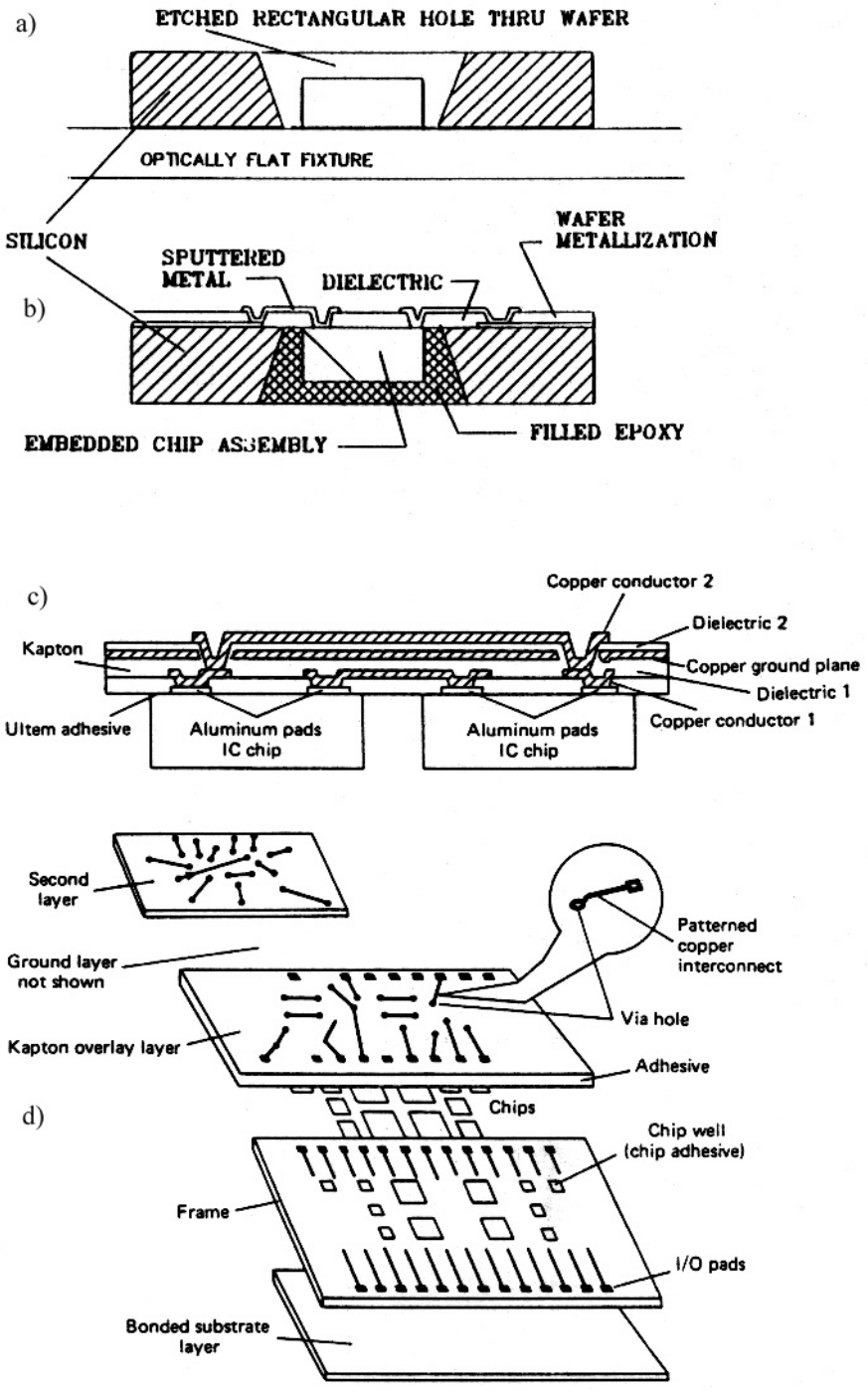


Fig. 3.32: Planar bonding with laser-assisted adaptive conductor routing. The top two figures a) and b) show a substrate cross section with details of the mounting of the chip in an etched through-hole. Figure c) shows the conductor layers and polyimide insulation on top of the substrate. The bottom figures show an exploded view of all the layers [3.20, 3.21].

Electroplating of copper is then performed to increase the thickness of the conductive layer, and the conductive paths are patterned by photolithography by direct laser writing. Photolithography and etching of the conductor pattern must be adjusted to each chip and each substrate because of the deviation in the IC chip placement. That is done as follows: The wafer is covered with positive

photo resist. An electronic vision system recognises the substrate interconnection points and the IC interconnection points, and gives information to a laser that illuminates selectively the path from each substrate interconnection point to the corresponding chip interconnection point. The photo resist is cured where the laser has illuminated it, and removed by the development process elsewhere. In the subsequent etching process the metallisation is removed on the rest of area. This is called "adaptive routing".

A second layer of conductive paths can be implemented by spin coating of polyimide with laser burning of vias and deposition of a new conductive layer, which is then patterned. This can be repeated for new layers until the required interconnect routing is achieved.

This method is under development at Auburn University, General Electric and other places and may be capable of giving interconnections with a pitch of a few tens of μm. It has the potential to be both flexible in production, give excellent electrical characteristics and give high packaging density.

REFERENCES

[3.1] R.R. Tummala and E.J. Rymaszewski: "Microelectronics Packaging Handbook". (van Nostrand Reinhold, 1988.)

[3.2] ASM International: "Electronic Materials Handbook, Vol. 1, Packaging". (1989.)

[3.3] S.M. Sze:
a): " Technology". (McGraw Hill, 2nd Ed.1988.)
b): "Physics of Semiconductor Devices". (Wiley, 2nd Ed. 1981.)

[3.4] R.C. Buchanan: "Ceramic Materials for Electronics". (Marcel Dekker, 1986.)

[3.5] L.M. Levinson: "Electronic Ceramics". (Marcel Dekker, 1988.)

[3.6] M.T. Goosey: "Plastics for Electronics". (Elsevier, 1985.)

[3.7] G. Leonida: "Handbook of Printed Circuit Design Manufacture, Components and Assembly" (Electrochemical Publications, 1981.)

[3.8] J.J. Licari and L.R. Enlow: "Hybrid Microcircuit Technology Handbook". (Noyes Publications, 1988.)

[3.9] D.P. Seraphim et at.: "Principles of Electronic packaging". (McGraw-Hill, 1989.)

[3.10] See e.g.: D.E. Riemer: "Analytical engineering model of the screen printing process", parts I and II. Solid State Technology Aug. and Sept. 1988.

[3.11] C. Lea: "A Scientific Guide to Surface Mount Technology". (Electrochemical Publications, 1988.)

[3.12] C.I. Wall: "Screen printing in the Printed Circuit Board Industry". Circuit World vol. 12, No. 3, 1986, page 36.

[3.13] R.J. Klein Wassink: "Soldering in Electronics". (Electrochemical Publications, 2nd Ed., 1989.)

[3.14] B.N. Ellis: "Cleaning and Contamination of Electronics Components and Assemblies". (Electrochemical Publications 1986.)

[3.15] a): Truls Koch et al.: "Methods for Clean Electronics". EPF report R-45 (Feb. 1991, in Norwegian.)
b): C. Lea: "After CFCs - Options for cleaning electronic assemblies". (Electrochemical Publications 1991.)

[3.16] A. Bjørneklett, L. Halbo and H. Kristiansen:
a): "Thermal conductivity of epoxy adhesives filled with silver particles". Int. J. of Adhesion, vol. 12, no. 2, April 1992, p. 99.
b): "Investigation of the Thermal and Mechanical Properties of Die Bonding Adhesives". Proceedings IEPS 1992, p. 509.
c): "Hybrid Substrates for Power Electronic Applications: An Investigation of Thermal Resistance and Mechanical Stress". Hybrid Circuits, vol. 30, Jan. 1993.
d): "Thermal Resistance, Thermomechanical Stress and Thermal Cycling Endurance of Silicon Chips Bonded with Adhesives". Proceedings Semitherm 1993.

[3.17] H. Kristiansen and A. Bjørneklett: "Fine pitch connection of flexible circuits to rigid substrates using non-conductive adhesives". Proceedings IEPS 1991, p. 795.

[3.18] J.H. Lau et al.: "Overview of Tape Automated Bonding Technology". Circuit World, vol. 16, no. 2, 1990, p. 5.

[3.19] L. Halbo:
a): "Tape Automated Bonding", EKF report R 44 (1986, in Norwegian).
b): "Tape Automated Bonding - Analyses and Case Studies", Nordic Industry Fund report (March 1987, in Norwegian).

[3.20] R.C. Landis: "Electronic packaging for the year 2000". Proceedings IEPS 1990.

[3.21] See e.g.:
a): R. Hartley et al.: "Rapid prototyping using high density interconnect". European Design Automation Conference, Glasgow, March 1990.
b): R.O. Carlson & al.: "A High Density Copper/Polyimide Overlay Interconnection". Proceedings IEPS 1988, p. 793.

[3.22] S. T. Riches: "Packaging Options for High Lead Count ASIC Devices". Hybrid Circuits, vol. 23, Sept. 1990, p. 14.

[3.23] F.N. Sinnadurai: "Handbook of Microelectronics Packaging and Interconnection Technologies". (Electrochemical Publications, 1985.)

[3.24] C. P. Wong et al.: "Understanding the Use of Silicone Gels for Nonhermetic Plastic Packaging". IEEE Trans. CHMT, vol. 12, no. 4, Dec. 1989, p.421, and IEEE Gel Task Force Reports in IEEE Trans. CHMT.

CHAPTER 4

COMPONENTS FOR ELECTRONIC SYSTEMS

4.1 INTRODUCTION

The components and the component technology are of great importance for performance, reliability, space needed, and cost of electronic systems. They also are important in determining the production process for modules and PCBs(Printed Circuit Boards). In this chapter we shall describe the properties of the most important passive components and IC packages. The electronic functions of ICs, however, are outside our scope.

The American organisation JEDEC (Joint Electronic Device Engineering Council) has recommended standard dimensions for many components. Standardisation is extremely important.

4.2 RESISTORS

4.2.1 Hole mounted resistors

Hole mounted resistors generally have cylindrical body, with axial leads, Fig. 4.1. There are three main types:

- Carbon composite, with a massive body of conductive carbon in a matrix of insulating material. Resistor values are between 1 ohm and 100 Mohm, maximum power dissipation 1/8 - 2 Watt, depending on the physical size. The temperature coefficient of resistance is high (~500 ppm/°C), the stability is low, and the resistance tolerance is 5, 10 or 20%.
- Wire wound, with insulating body. Metal wire, e.g. NiCr, is wound on the body and covered by insulation. Range: 1 - 100 Kohm, low temperature coefficient (~70 ppm/°C), tolerance 0.1 - 0.5 %, high stability.
- Film layer resistors have a thin film of metal, tin oxide or carbon, possibly with a spiral cut to increase the resistance. Resistance values ≤ 1 ohm to ≥ 1 Mohm, temperature coefficient 20 - 250 ppm/°C. Low tolerance can be obtained by trimming.

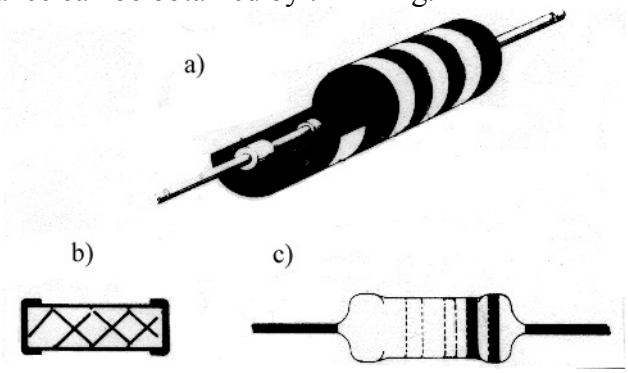


Fig. 4.1: Hole mounted resistors: Carbon composite, wire wound and metal film types.

4.2.2 Surface mounted resistors

SMD resistors normally have a rectangular body made of ceramic, Fig. 4.2 a). The resistor material may be ruthenium oxide. It is printed on in paste form and cured at high temperature by thick film methods (Chapter 8), and laser trimmed to correct value. On top is a protective layer of insulating glass. The component has no leads but electrical terminals at the ends. The inner electrode material is Ag or Au. The outside electrode material is AgPd or a diffusion barrier of Ni with SnPb solder on top, Fig. 4.2 b). The manufacturing process is described in [4.3, 4.4]. The purpose of the Ni layer is to prevent Ag from being dissolved in the outer metal, as Ag dissolves fast in Sn and Sn/Pb solder, please refer to Chapter 3.

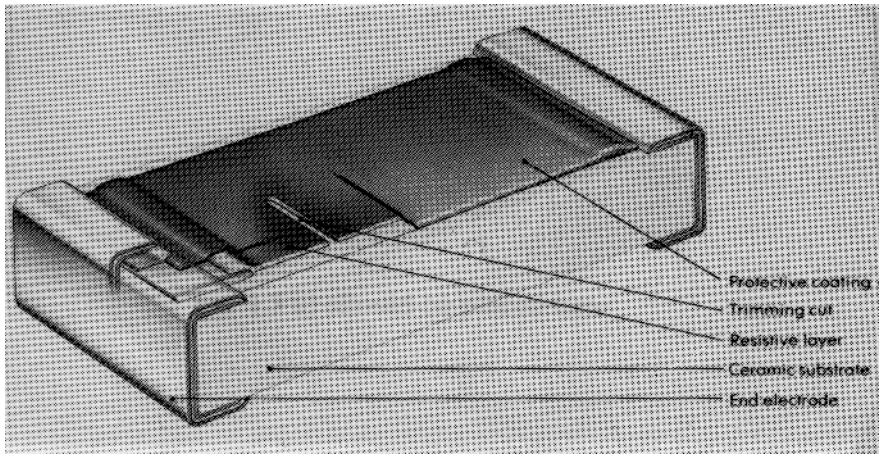


Fig. 4.2 a): Surface mounted resistor, rectangular shape.

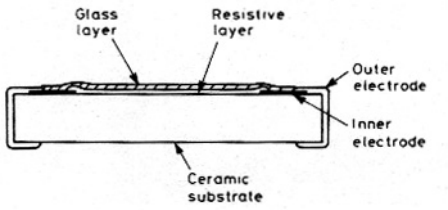


Fig. 4.2 b): Metal system for termination on SMD resistors.

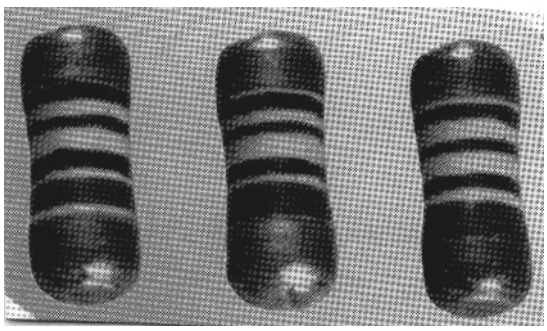


Fig. 4.2 c): MELF-resistors have cylindrical body.

SMD resistors are also made in cylindrical form, called MELF (metal electrode face bonding), see Figure 4.2 c). This component has metal plates at the ends, coated with solder.

The temperature coefficient of resistance is typically below +/- 200 ppm per °C, tolerance +/- 1 - 20 %. The most common rectangular sizes are denoted 1206 (0.12" x 0.06 ", or 3.2 x 1.6 mm) and 0805. There are smaller sizes: 0603 is extensively used, and 0402 is emerging. Maximum power dissipation for 1206 is 1/8 or 1/4 Watt. Higher power resistors have larger bodies. Resistor values range from < 1 ohm to approximately 10 Mohms. A "zero ohm" component has resistance around 50 Mohms and is used as a "jumper" to contact two conductors on the PCB with other conductors between.

Typical properties of SMD resistors are shown in Table 4.1.

Table 4.1. Properties of SMD resistors (Philips).

Resistance range and tolerance	10 ohm to 1 Mohm (E24* series) ± 2% 1 ohm to 10 Mohm (E24 series) ± 5% 1 ohm to 10 Mohm (E12 series) ±10%
Dimensions	3,2 x 1,6 x 0,6 mm
Operating temperature range	-55°C to + 155°C
Temperature coefficient (-40°C to 125°C)	$<+200 \times 10^{-6}/K$
Absolute max. dissipation at T_{amb}= 70°C	0,25 W
Maximum permissible voltage	200 V (r.m.s.)
Climatic category (IEC68)	55/155/56
Jumper resistance	≤ 50 mohm
Maximum current	2 A

*See Table 4.2

Table. 4.2: The resistance series E24, E12 and E6. The numbers mean that for example in series E6 there are 6 resistance values for each decade: 10, 15, 22, 33, 47 and 68 $x10^n$ ohms.

E24	10	11	12	13	15	16	18	20	22	24	27	30	33	36	39	43	47	51	56	62	68	75	82	91
E12	10		12		15		18		22		27		33		39		47		56		68		82	
E6	10				15				22				33				47				68			

4.3 CAPACITORS

In addition the capacitance, the following properties are important for the area of application of capacitors:

- Maximum voltage rating
- Temperature dependence of the capacitance (temperature coefficient)
- Loss tangent (tan δ), see below
- Equivalent series resistance
- Long term stability and ageing phenomena
- High frequency properties
- Leakage current
- Ability to withstand various production processes (high temperature, etc.)
- Price, physical size, etc.

There are many types of capacitors, and the choice depends on the relative importance of these factors for the given application.

4.3.1 Electrical model

An ideal capacitor consists of two electrodes of area A, with a perfect insulator between them, of thickness d and relative dielectric constant ε_r :

$$C = \varepsilon_o \varepsilon_r \times A / d$$

Practical capacitors can be described by models like the one in Fig. 4.3. Deviations from the ideal are represented by series resistance R_s, parallel resistance R_p, and inductance L. The various parasitics dominate at different frequencies.

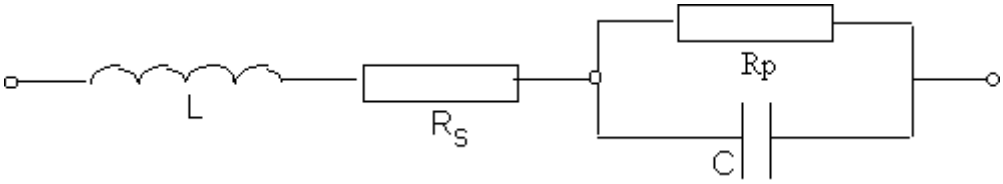


Fig. 4.3: Electrical equivalent model for capacitor.

If R_p can be neglected the impedance is given by:

$$/Z/ = [R_s^2 + (\omega L - 1/\omega C)^2]^{1/2}.$$

Examples of the frequency dependence are shown in Figure 4.4. It shows a resonant behaviour with Z_{min} at the frequency where $\omega L = 1/\omega C$. Above this frequency the capacitor behaves more like an inductor.

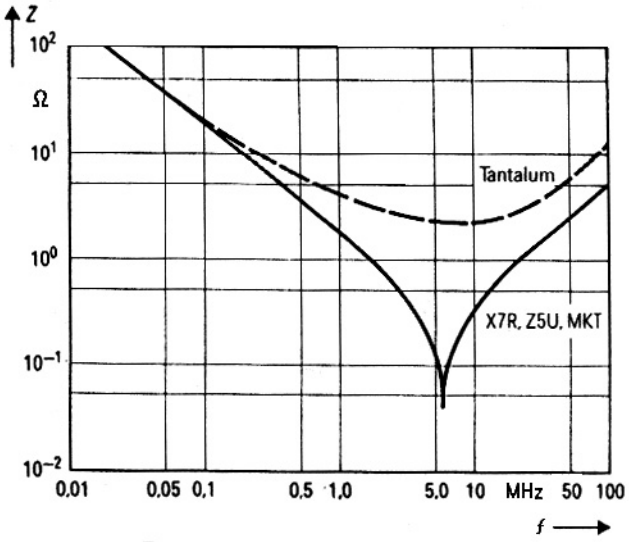


Fig. 4.4: The frequency dependence of impedance for multilayer ceramic capacitors (below) and tantalum electrolytic capacitors (top), all having 100 nF capacitance value [4.5].

The loss tangent is of special importance. It is defined as the ratio between the resistive and reactive parts of the impedance (please refer to Section 3.2.3):

$$\tan \delta = R \,/\, /\mathrm{Im}\, Z/ = [R_p + R_s\,(\,1+(\,\omega C R_p)^2)\,] \,/\, (\,\omega C R_p^2 - \omega L\,(1+(\,\omega C R_p)^2)\,].$$

Schematically tan δ will depend on the frequency as shown in Figure 4.5. Most capacitors have a constant loss tangent over a large frequency interval, where they are normally used.

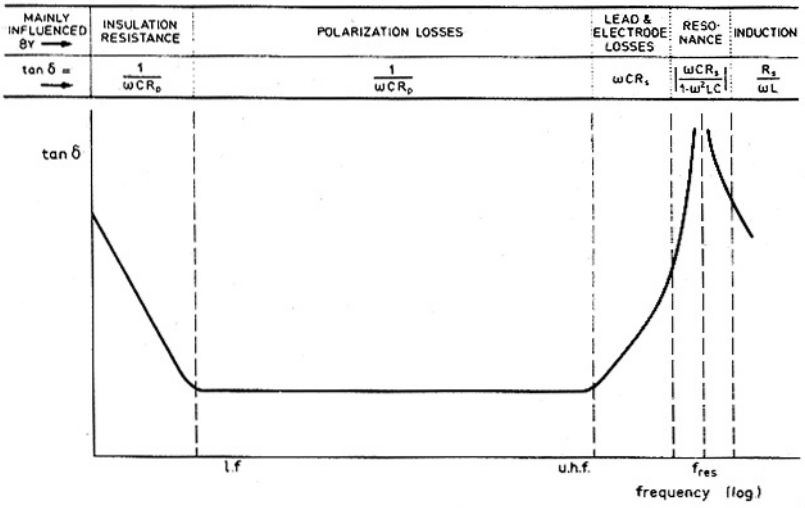


Fig. 4.5: Frequency dependence of the loss tangent tan δ schematically (Philips data book).

4.3.2 The main types of capacitors

Capacitors are of the following types:

- Ceramic multilayer
- Electrolytic, dry and wet
- Metallised plastic film dielectric (polyester, polystyrene, etc.)
- Mica.

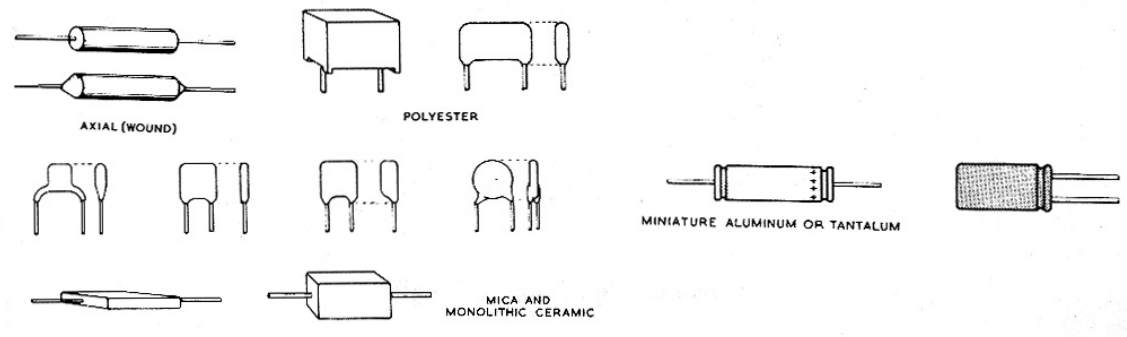


Fig. 4.6: There is a large spectrum of hole mounted capacitors. To the left some types of dry capacitors: axial metal/plastic film, ceramic, mica, and to the right aluminium and tantalum electrolytic capacitors.

All types are made in hole mounted as well as surface mounted (SMD) versions. The main difference is the body shape and the electrode form. We shall focus on the SMD versions. However, Figure 4.6 shows some examples of the shapes of hole mounted capacitors.

4.3.3 Multilayer ceramic capacitors

Ceramic multilayer capacitors, see Figure 4.7, are the dominating type for SMD. They are composed of a number of metal electrodes, isolated from each other by thin layers of a ceramic dielectric. Every other electrode is connected to the end termination on the left and the right side. The dielectric layers are only of the order 20 μm thick, and the dielectric may have a very high relative dielectric constant. Thus, one achieves very high capacitance to volume ratio. The capacitors are manufactured by processes similar to those used for making multilayer ceramic packages and multichip modules, please refer to Chapters 3 and 8 and [4.2, 4.3, 4.6, 4.8]. Due to the high temperatures used during sintering the inner electrodes are normally made of the noble metals Pt or Pd, which have a high melting point. The end electrodes are AgPd or Ag, see Figure 4.7, and a diffusion barrier of Ni outside it, and on top of that, a eutectic composition of SnPb solder. See also Section 4.7.

The ceramic dielectrics are of different types. Designations and compositions vary between manufacturers, but properties are similar. The dielectrics are divided into classes according to relative dielectric constant and other properties. The ceramic is often based on barium- or strontium titanate with additives. These materials are ferroelectric, therefore the high dielectric constant, please refer to Figure 4.8. Near the Curie temperature ε_r is strongly temperature dependent, and the purpose of the additives is to move the Curie point or in other ways reduce the temperature dependence in the temperature region of use.

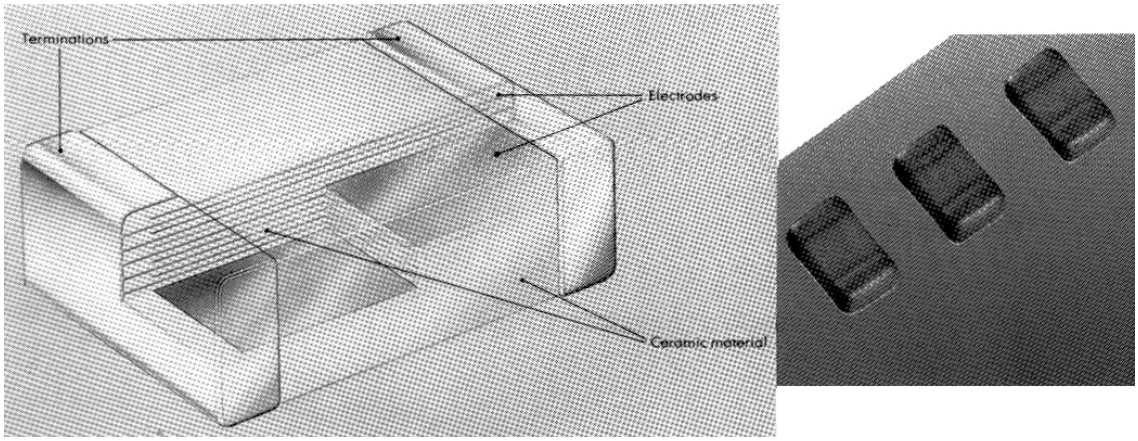


Fig. 4.7 a): SMD multilayer ceramic capacitor.

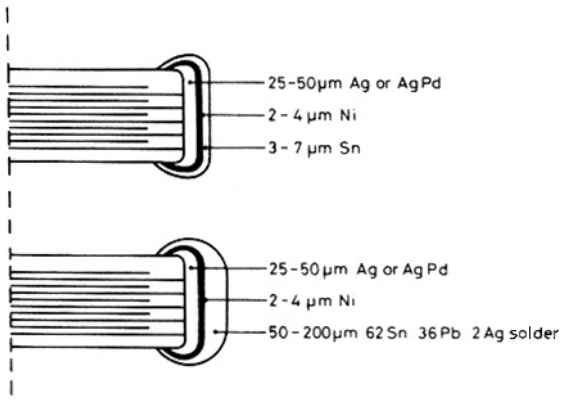


Fig. 4.7 b): Metal system for the end termination of multilayer ceramic capacitors.

There are two main classes of ceramic capacitors [4.8]:

Class 1: Capacitors with low capacitance values, dielectric with $\varepsilon_r < 100$, low dielectric losses, low temperature coefficient. Ceramics composed of $MgTiO_3$, Mg_2SiO_4, $BaTiO_3$ and various other materials are used for Class 1 capacitors, which are designated NP0, N220, N750, COG, etc.

Class 2: Capacitors of higher capacitance values, based on ceramics with ε_r up to about 15 000. The capacitance varies strongly as a function of temperature and voltage. Tan δ is higher than for Class 1, and the properties change in time. Dielectric designations are X7R, Z5U, etc.

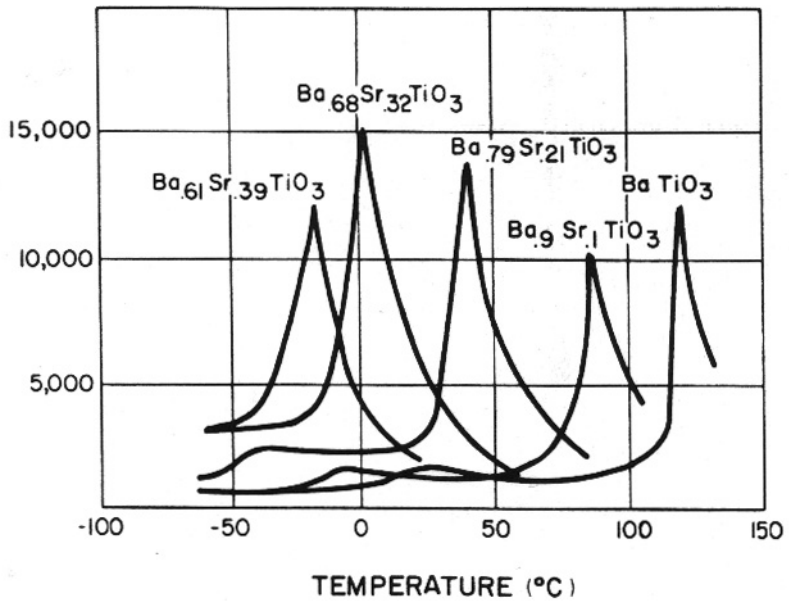


Fig. 4.8: Relative dielectric constant for ferroelectric ceramic compositions, as a function of temperature, near the Curie point [4.10].

Ceramic multilayer capacitors are available in the range between 1pF and several µF, maximum voltage 50 to over 500 V (power capacitors up to several kV), tolerance ±5 - 20 %. The sizes are standardised, the dominating ones being 0805

and 1206. 1210, 1808, 1812, 2220 are also common. The thickness of the chip varies depending on the number of layers, i.e. the capacitance value. The development moves toward smaller sizes; 0603 is in use and 0402 in development. They will require significant changes in mounting and soldering/gluing technology and equipment.

Some characteristic properties of capacitors of Classes 1 and 2 are shown in Figure 4.9. The voltage dependence as well as temperature coefficient and loss tangent are most favourable for NP0, least for Z5U. However, Z5U is a good choice for decoupling and other less critical applications that require high capacitance-to-volume ratio.

Ceramic capacitors - particularly Class 2 - have some inherent failure mechanisms that must be kept in mind: Low voltage failures, dielectric absorption [4.10], crack formation [4.11], and silver electromigration. The failures often occur gradually and may lead to high leakage current and change in capacitance value after some time.

Crack formation is the most troublesome failure type. It is caused by rapid temperature changes combined with thermal mismatch between the materials: The ceramic (thermal coefficient of expansion (TCE): α= 9.5 - 11.5 ppm/^{o}C for barium titanate), the terminal metals (15 ppm/^{o}C for nickel, 27 for solder), and the substrate (12 - 16 for fibre glass epoxy, and 5 - 7 for alumina ceramic). Figure 4.10 illustrates the most sensitive regions for crack formation. The cracks may start during the rapid temperature changes of the solder processes: The stress depends on the shape of the solder fillet and the capacitor, and the materials combination. The shape of the solder fillet again depends on the solder process, and the shape and location of the solder land. Thus, the reliability is determined by the design rules and technology choices made by the designer. It is characteristic for a ceramic that it can withstand more compression than tension. When the heating is uniform there is more tendency towards cracking when the substrate TCE is greater than that of the capacitor (e.g. organic substrates), than the opposite (e.g. alumina substrate). When self-heating of the capacitor is dominant the opposite is the case: The crack formation is more pronounced when the substrate TCE is smaller than that of the capacitor.

The crack formation is normally not visible or measurable at once. However, humidity and impurities will enter the crack and cause deterioration over time. The electrode materials will migrate into the crack, particularly when there is an electric field present. Furthermore, the component is mechanically weakened, and thermal cycling during the field life of the product will make the crack grow. Then tan δ and C will also change.

Class 2 capacitors change their capacitance over time by "ageing", according to a logarithmic time dependence.

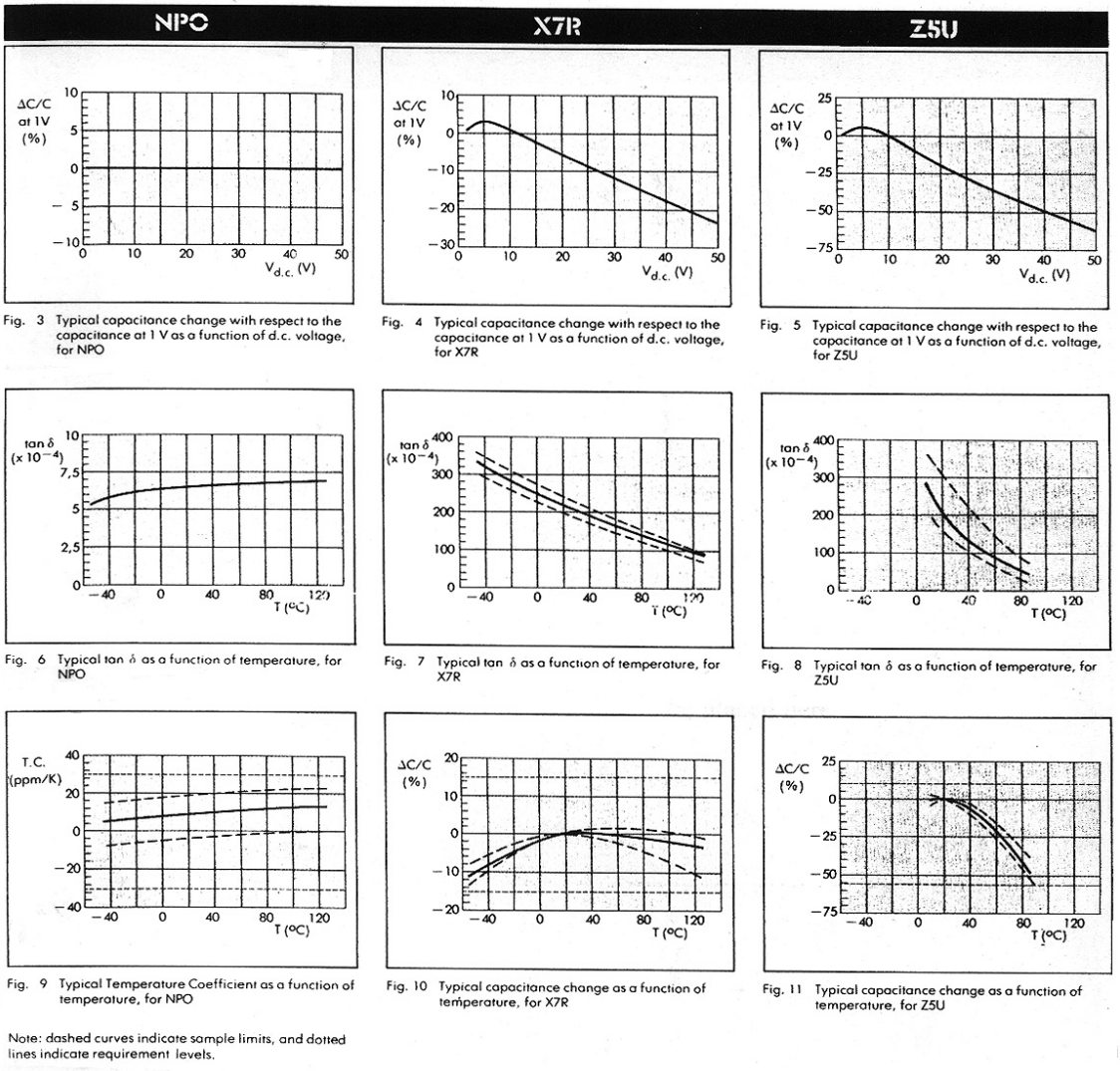


Fig. 3 Typical capacitance change with respect to the capacitance at 1 V as a function of d.c. voltage, for NPO

Fig. 4 Typical capacitance change with respect to the capacitance at 1 V as a function of d.c. voltage, for X7R

Fig. 5 Typical capacitance change with respect to the capacitance at 1 V as a function of d.c. voltage, for Z5U

Fig. 6 Typical tan δ as a function of temperature, for NPO

Fig. 7 Typical tan δ as a function of temperature, for X7R

Fig. 8 Typical tan δ as a function of temperature, for Z5U

Fig. 9 Typical Temperature Coefficient as a function of temperature, for NPO

Fig. 10 Typical capacitance change as a function of temperature, for X7R

Fig. 11 Typical capacitance change as a function of temperature, for Z5U

Note: dashed curves indicate sample limits, and dotted lines indicate requirement levels.

Fig. 4.9: Properties of dielectrics of the types NP0, X7R and Z5U in SMD ceramic multilayer capacitors. Top: The voltage dependence of capacitance; in the middle loss tangent as function of temperature; and at the bottom the temperature coefficient of the capacitance (Philips).

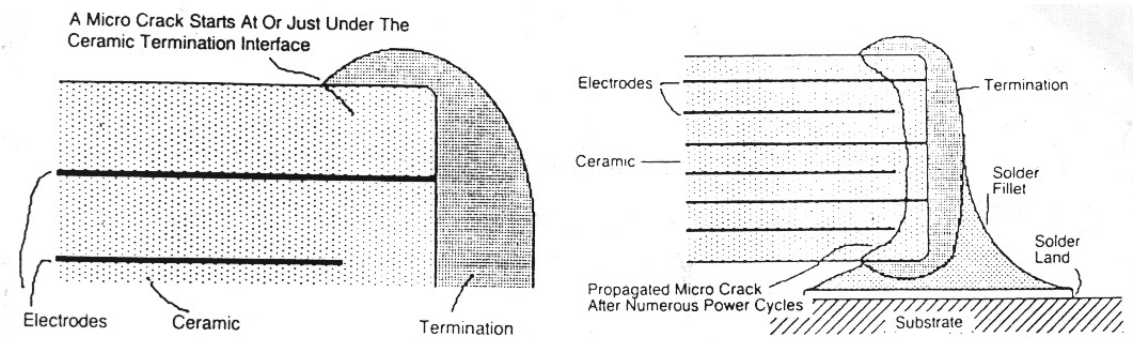


Fig. 4.10: Crack formation because of thermal stress in ceramic capacitors [4.11].

4.3.4 Electrolytic capacitors

Dry and wet electrolytic capacitors have a very high capacitance to volume ratio, due to a high effective area and a very thin dielectric. For this reason, they can withstand only low voltages. Due to their structure they can operate with voltages of only one polarity and are damaged by voltages of the other polarity, through destruction of the dielectric.

The most common dry type is the tantalum capacitor, Figure 4.11 a). It has tantalum as one electrode (anode), a thin layer of tantalum oxide as dielectric, and manganese dioxide as the other electrode (cathode). Its manufacturing process is described in [4.2, 4.6].

Tantalum electrolytic capacitors have good electrical properties, but so far, a high price and they lack standardisation between manufacturers. Available capacitance values are typically between 0.1 and 100 μF, maximum voltage 2 - 50 V, please refer to Fig. 4.11 b). A common fault is short circuit due to changes in the crystal structure of the dielectric for very high AC currents [4.14].

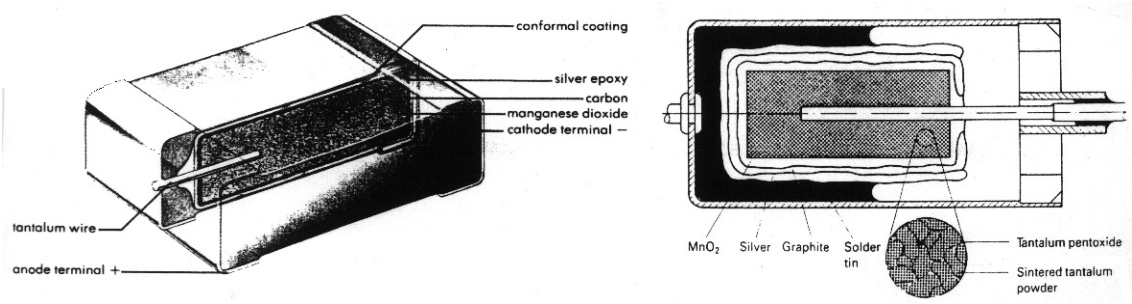


Fig. 4.11 a): Tantalum SMD electrolytic capacitor (Philips), hole mounted tantalum capacitors (Siemens [4.14]).

Dissipation factors vary with temperature: Maximum values which are not exceeded by any capacitor ar as follows.

Temperature	-55°C	25°C	85°C	125°C
Rated Voltage 4 to 10 V d.c.	10%	12%	12%	12%
Rated Voltage 15 to 50 V d.c.	8%	6%	6%	6%

The d.c. leakage current (at rated voltage) is within the limit set below

25°C <	0,01 µA/µFV	or	<	1 µA	whichever is greater
85°C <	0,10 µA/µFV	or	<	10 µA	whichever is greater
125°C <	0,125 µA/µFV	or	<	12,5 µA	whichever is greater

Fig. 4.11 b): Electrical properties of tantalum electrolytic capacitors (Philips).

Wet aluminium electrolytic capacitors are manufactured by anodic oxidation of Al [4.2]. The Al foil has been etched to give a rough surface with very high effective area. The wet electrolyte forms one electrode, the cathode, and Al the other electrode, the anode. Fig. 4.12 shows geometry and some electrical data. Wrong polarity of the voltage will ruin the dielectric and short-circuit the capacitor. Positive hydrogen ions will drift through the dielectric, become neutralised at the Al electrode and form hydrogen gas that breaks the dielectric and gives shortages.

When the temperature changes the wet electrolyte must "breathe", and the component cannot be sealed. This means that wet electrolytic capacitors cannot withstand long time in wave- or reflow solder processes. In these processes the component life will be reduced - in the worst case high pressure will build up in the electrolyte, which "boils" and may leak out, ruining the component.

Some aluminium electrolytic capacitors are made with a solid electrolyte, very often MnO_2 is used.

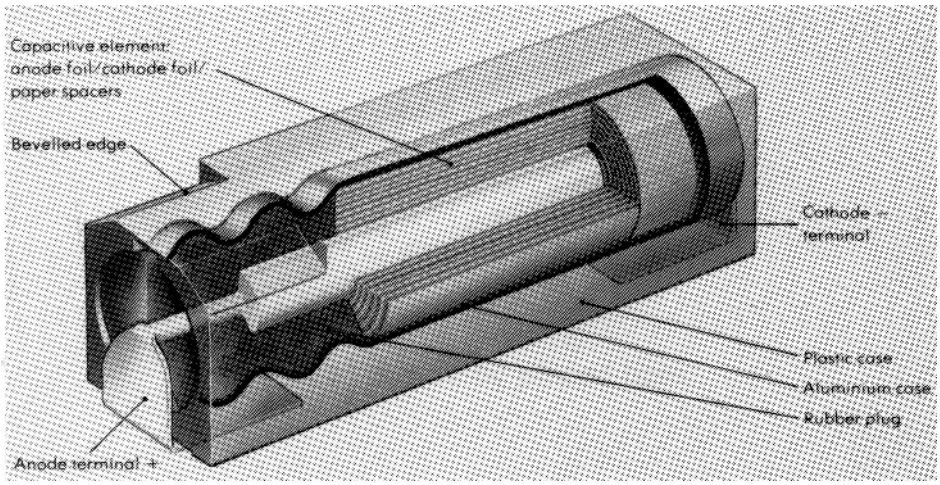


Fig. 4.12 a): Aluminium electrolytic capacitor for SMD mounting (Philips).

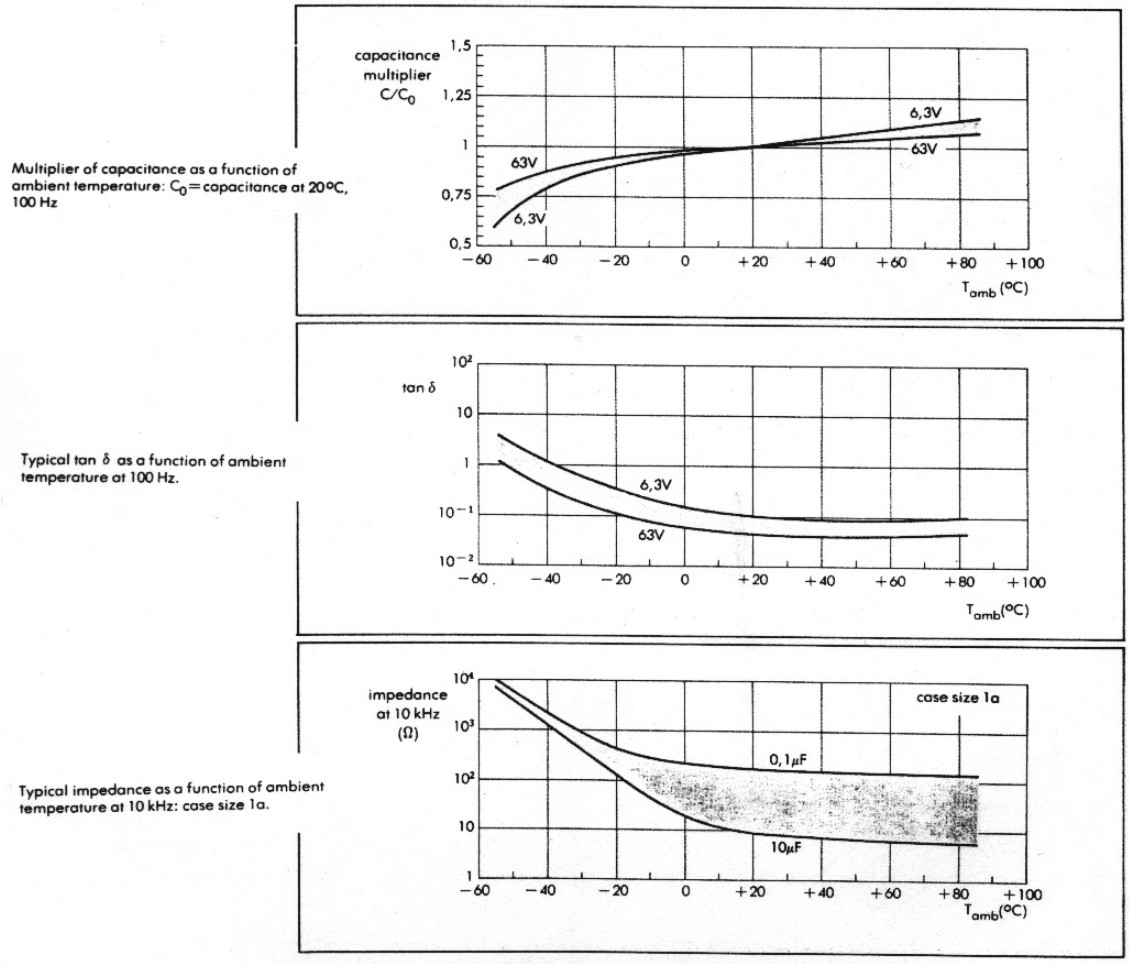


Fig. 4.12 b): Aluminium electrolytic capacitor properties (Philips). The top figure shows temperature dependence of the capacitance, relative to the value at 20 °C, the middle figure shows temperature dependence of tan δ, and the bottom figure shows temperature dependence of impedance at a frequency of 10 kHz.

4.4 DIODES AND TRANSISTORS

The packages for diodes and transistors depend on the component power, frequency of operation, reliability required, etc. For hole mounted diodes axial packages are most common, the semiconductor chip being mounted in a body of glass or ceramic, please refer to Figure 4.13. Power diodes have metal housing and screw mounting for better thermal coupling. The cathode of the diode is grounded to the can.

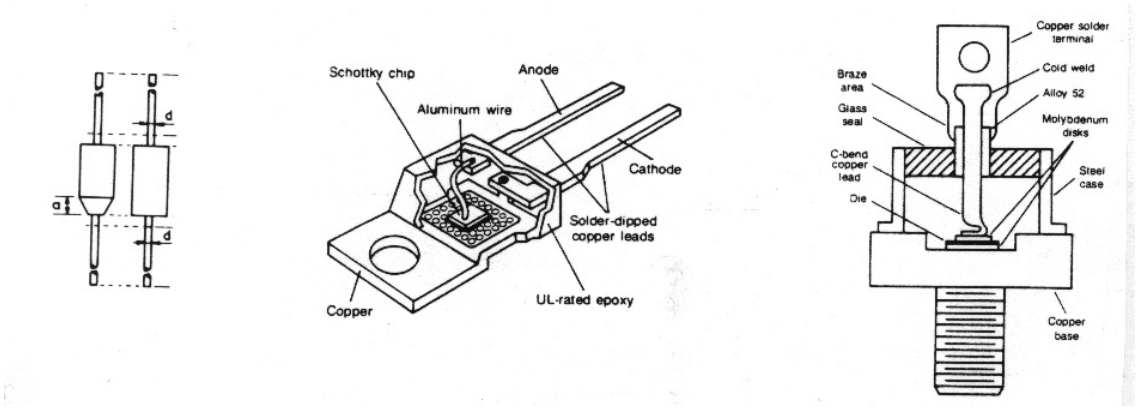


Fig. 4.13: Axial, plastic encapsulated, hole mounted diodes to the left. In the centre, a plastic can with metal base for power diodes. It can be hole mounted or surface mounted, depending on how the leads are bent. The base is screwed to the substrate. To the right, a higher power diode in a metal can, which is also screw mounted to the substrate for efficient thermal contact.

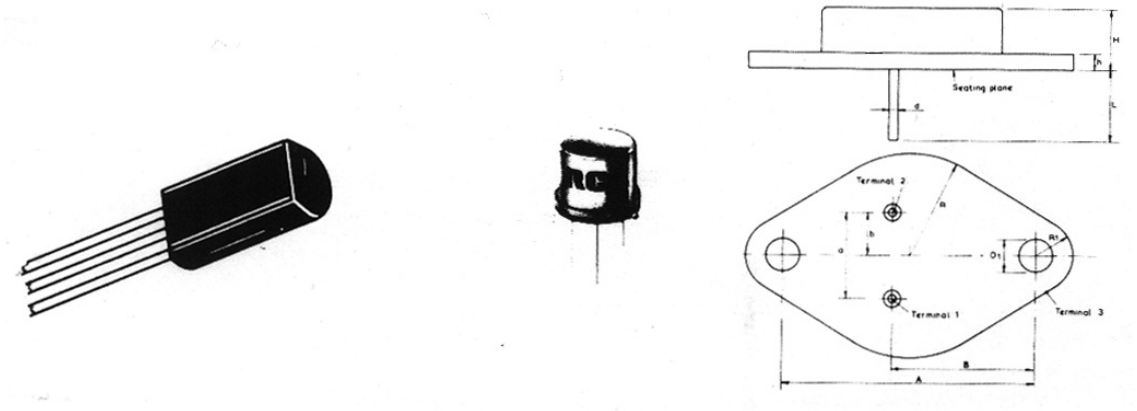


Fig. 4.14: Various types of hole mounted transistor packages: a) Plastic packages, b) Low power metal packages, c) Metal package for high power transistors. For the high power package, the collector is connected to the metal body.

Hole mounted transistors have a number of package forms, see Figure 4.14. Most are plastic. Metal housing is used to get hermeticity and the highest reliability. Power transistors have metal housings that are screw mounted on to the substrate for good thermal contact. The electrodes run through the metal base in a glass seal, with TCE matched to the metal.

For active SMD components, the semiconductor chip is normally the same as in the hole mounted equivalent, but the package is different. SMD diodes use two main package forms: MELF and SOT (Small Outline Transistor). For the MELF (Metal Electrode Face Bonding) version SOD-80 is the normal size, Figure 4.15. (SOD stands for Small Outline Diode.)

The more common type is SOT packages. They have rectangular plastic bodies and 3 or 4 leads, see Figure 4.16. In an SOT-23 package, there may be one diode with the third lead floating, or two diodes with one common terminal. The SOT-143 will contain two independent diodes. These packages have a maximum power rating of 0.1 - 0.3 W. SOT-89 has very good thermal contact to the substrate and can dissipate up to 1 W.

Hermetic SMD transistor packages made of ceramic exist, see Figure 4.16, but are not much used.

A transistor package with dimensions even smaller than those of the SOT-23, the SOT-323 has also been introduced: "Mini SOT" or SOT-323, with over-all dimensions 2.0 x 1.25 x 0.9 mm.

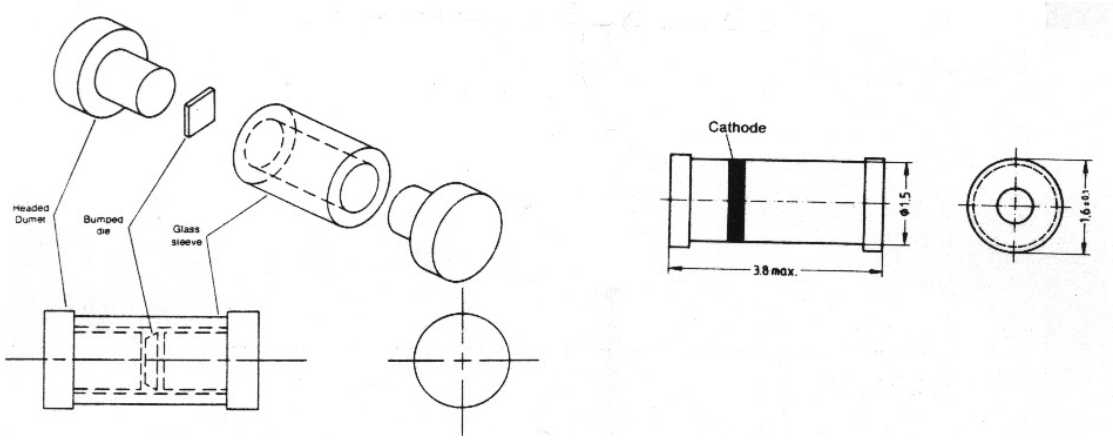


Fig. 4.15: MELF-package for SMD diodes. The standard size is designated SOD-80, with dimensions shown to the right.

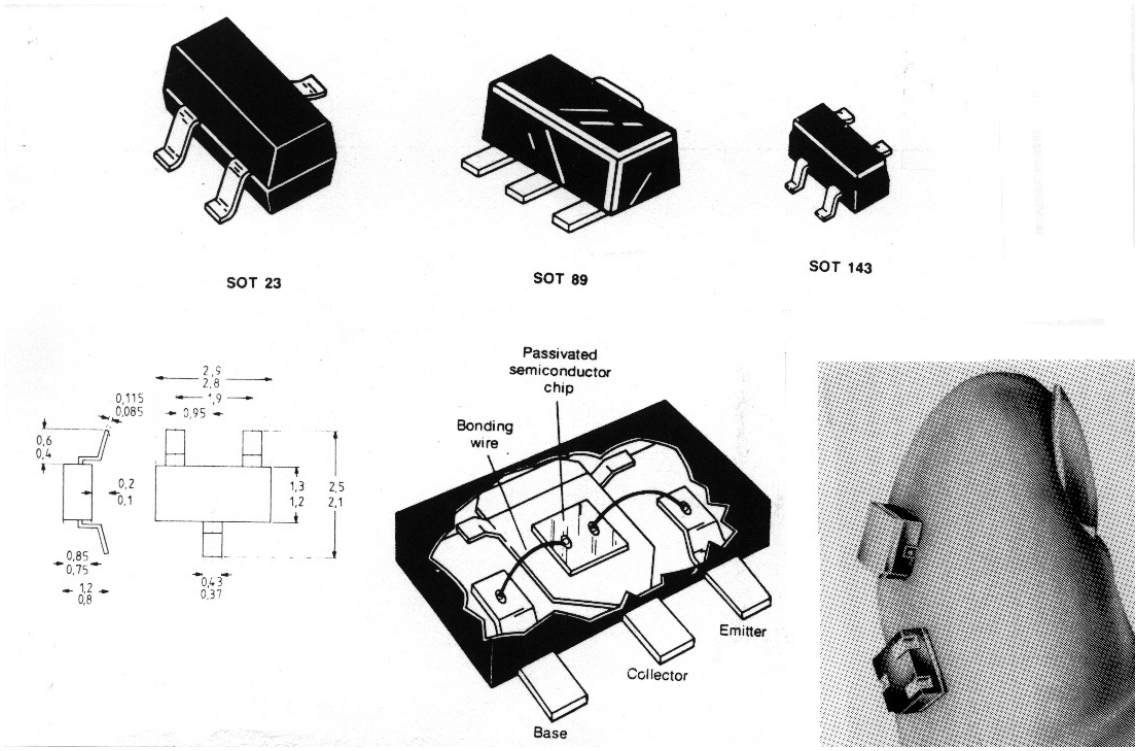


Fig. 4.16: SOT-packages for SMD diodes and transistors: The most common, SOT-23 top left, SOT-89 for power transistors in the middle, and SOT-143 with four terminals to the right. The dimensions for SOT-23 are shown bottom left, and a cut-through SOT-89 in the middle. Ceramic SMD transistor packages with terminal placement like for SOT-23 are shown bottom right.

4.5 MONOLITHIC INTEGRATED CIRCUITS

4.5.1 Plastic or ceramic packages: Advantages and disadvantages

Plastic and ceramic IC packages are both used. Each type has advantages and disadvantages, and the application determines the choice. We list some characteristics of both types.

Plastic:

- Not hermetic.
- Low price in large component quantities.
- High initial cost for tooling etc., not suitable for prototypes of custom circuits.

- Poor thermal conductivity of the plastic (0.2 W/°C·m, somewhat higher with special additives).
- Tolerate only limited time at high temperature (SMD soldering processes).
- High thermal expansion coefficient (25 - 50 ppm/°C) and thermal mismatch to Si chip and to metals. This is important for large Si chips and large packages.
- High demands on plastic quality and moulding process. If not satisfied, the long-term reliability will suffer.
- Not suitable for high frequency circuits which require controlled characteristic impedance.
- Special failure mechanisms (please refer to Section 3.3 and Chapter 9).

Ceramic:

- Hermetic, give good reliability.
- Costly, even in large volume, but Si chips can easily be mounted into pre-made packages, important for prototyping.
- Good thermal conductivity (15 - 30 W/°C·m for alumina).
- Low thermal coefficient of expansion (5 - 7 ppm/°C for alumina), gives thermal mismatch to organic substrates. This can be serious for leadless packages.
- Leadless packages have gold metallisation, which must be removed before soldering (see Section 4.7).
- Can be manufactured with well-defined high frequency properties.

Plastic packages dominate for ordinary uses. Ceramic is used for critical military and telecommunication systems, where hermeticity is required to get supreme long term reliability. They are also used for electrically and thermally demanding systems, see later (and in Chapter 6).

During the last years the reliability of good plastic packaging has improved much and is used increasingly even in the most demanding telecom- and military equipment.

4.5.2 Standard packages for hole mounted ICs

The DIP package

"Dual-in-line" packages (DIP), as seen in Figure 4.17, dominate for hole mounted ICs. For plastic DIPs the silicon chip is alloyed, soldered or glued to a metal plate, the leadframe, which is often an alloy of Fe/Ni 42/58 ("alloy 42") with low TCE to reduce the mismatch to Si. Components with high heat dissipation have Cu leadframe. Thin gold or aluminium bonding wires provide electric contact between chip and leads.

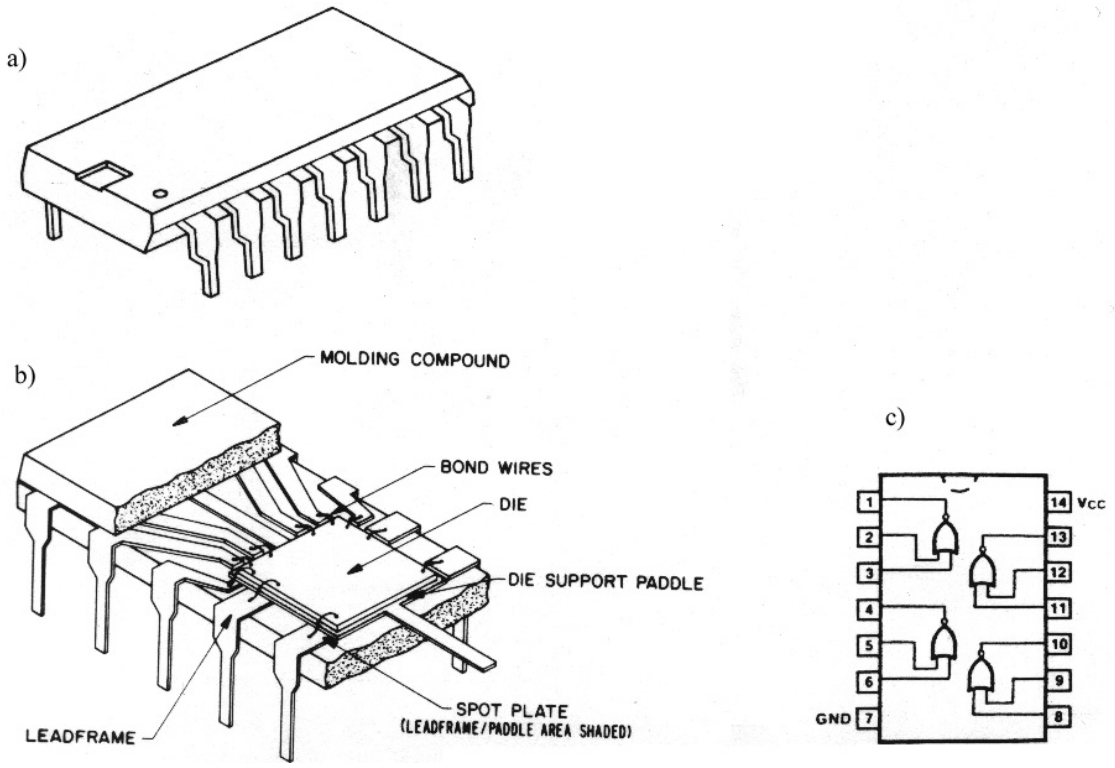


Fig. 4.17: a) DIP IC package. b) Partly cross-sectioned DIP package which shows the silicon chip, bonding wires, lead frame and plastic body. c) The terminal organisation for 4 two-input NOR gates in a 14 pins package.

The leads are in two rows. The dimensions are standardised on a grid of 0.1 " (100 mils) distances. The lead separation is 100 mils and the distance between the lead rows is 300 - 600 mils.

DIP packages are made with 8 - 64 leads. For small circuits with few I/Os several circuits are often made on the same piece of silicon and packaged in the same package, see Figure 4.17 c).

Ceramic DIP packages with a cavity for the chip are also common. The simplest is called CERDIP, and has two ceramic parts with glass sealing between them. The more advanced 3-layer ceramic package is made by multilayer ceramic technology, with metallisation between the layers (see Chapters 3 and 8). It normally has a metal lid that is soldered on after the component has been evacuated and filled with inert gas.

DIP packages can be surface mounted if necessary, by butt soldering the leads, or by bending them out in "gull wing" shape like for the SO package (see below).

Cylindrical metal cans with axial lead terminals are still used for some hole mounted ICs. They are not suitable for automatic mounting and high volumes.

The Pin Grid Package

Large VLSI circuits often have more than the maximum 64 I/Os available as a DIP. The largest hole mounted IC package is the pin grid, with leads on a grid of 100 mils lead separation, please refer to Figure 4.18. The pin grid is most frequently made of alumina ceramic, with up to 400 - 500 leads. There may be up to 6 - 10 layers of ceramic. Pin grid packages are made "cavity down" or "cavity up", depending on whether the heat should be removed down into the substrate or up, into a cooling fin (see Chapter 6). They use the board area better than the DIP and have very good thermal performance, but they are expensive. Once they are soldered onto the board, it is difficult to de-solder and remove them (repair). Therefore, they are often mounted in a socket. Routing the wiring to a pin grid package normally requires more than two layer boards.

Some standard products are supplied in plastic pin grid packages.

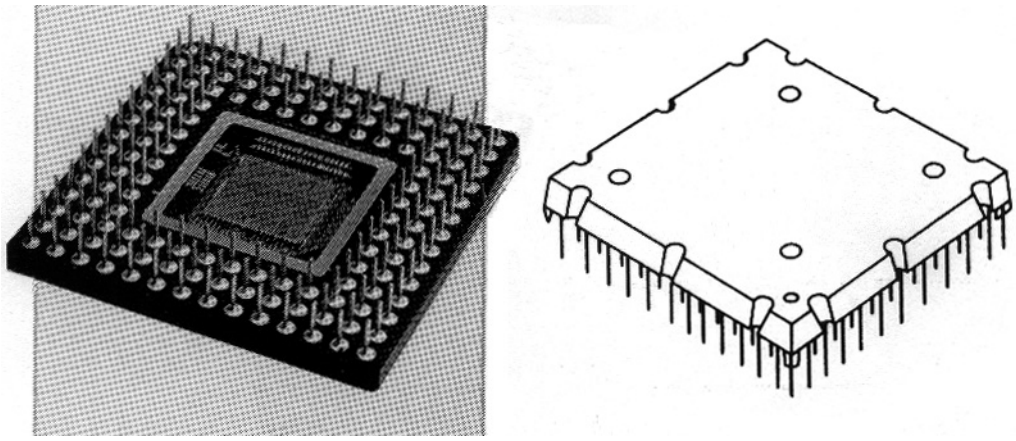


Fig. 4.18: Pin grid packages: To the left a cavity up ceramic package, and to the right a plastic moulded package.

4.5.3 Standard packages for SMD

SO and VSO

Between 8 and 28 terminals the Small Outline (SO) package, please refer to Figure 4.19, is the most common SMD package for ICs. They are similar to a small version of the DIP, thus the name. The lead separation is 50 mils, and the leads are bent out in "gull wing" form. Philips introduced the SO package, as well as the "Very Small Outline" (VSO) package with 40 and 56 leads, with separation 30 mils and 0.75 mm respectively. The VSO has not become widely used.

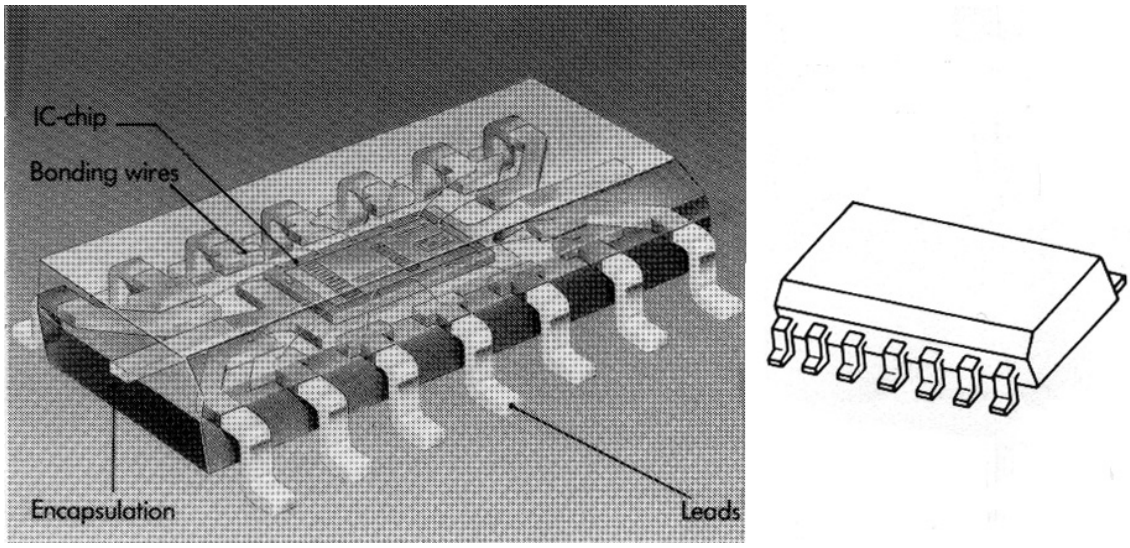


Fig. 4.19: Surface mounted SO (Small Outline) IC package (Philips).

Table 4.3: Dimensions for SO- and VSO packages. Centre-to-centre lead distance is normally 50 mils, except for VSO-40 with 30 mils and VSO-56 with 0.75 mm.

Outline	Encapsulation		Maximum width
SO	Maximum width	Maximum length	Lead end to lead end
	[mm]	[mm]	[mm]
SO-8	4,0	5,00	6,2
SO-8	7,6	7,6	12,4
SO-14	4,0	8,75	6,2
SO-16	4,0	10,00	6,2
SO-16L	7,6	10,5	10,65
SO-20	7,6	13,0	10,65
SO-24	7,6	15,6	10,65
SO-28	7,6	18,1	10,65
VLO-40	7,6	15,5	12,8
VSO-56	11,1	21,6	15,8

Normally the SO packages are plastic, but ceramic versions exist.

A similar package, much used for memory circuits, is the "SOJ", which has its leads bent underneath the body, similarly to the PLCC, see below and Figure 4.20a).

PLCC and LLCC

Two dissimilar packages are called "chip carriers". One of them is the Plastic Leaded Chip Carrier, (PLCC), Figure 4.20 a), with leads on all four sides. The leads are folded under the body in J-shape to conserve board area. They have 50 mils pitch and are used for 18 - 84 terminals. The largest type is less used, because of reduced reliability due to thermal mismatch problems. The PLCC was introduced by Texas Instruments and is the most common SMD package for 28 - 68 terminals.

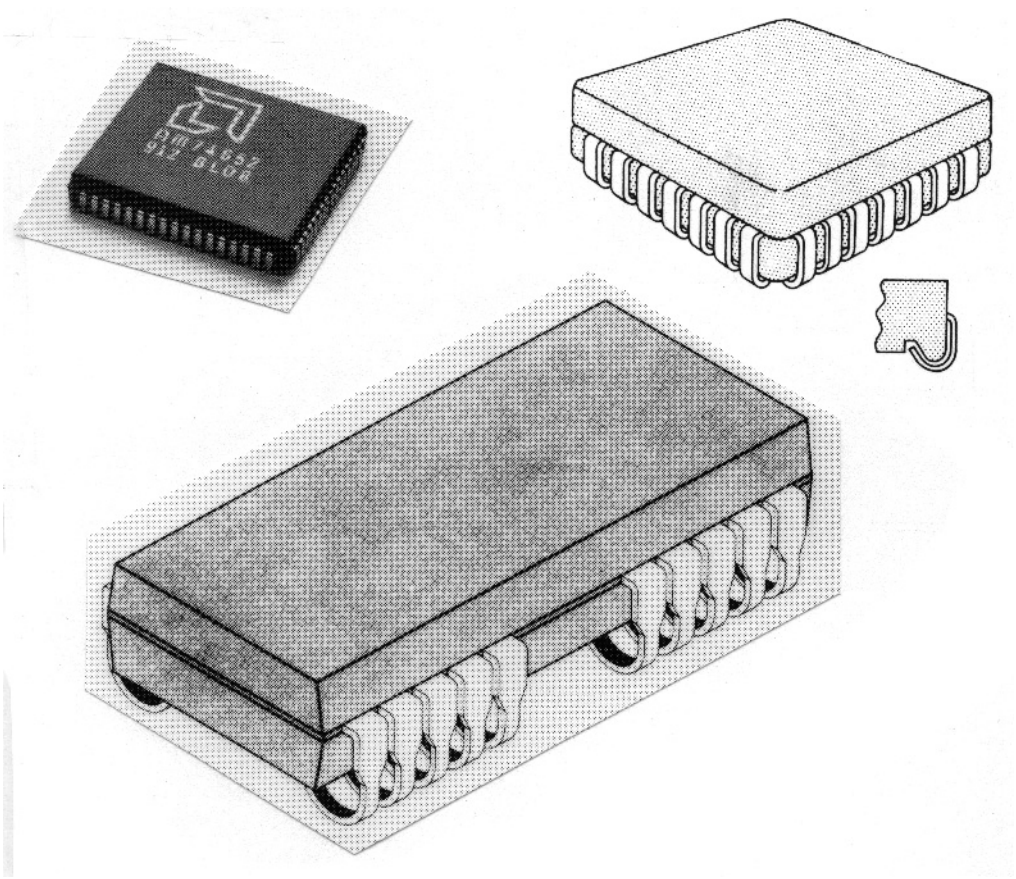


Fig. 4.20: Plastic chip carrier with leads (PLCC). They are normally square with an equal number of terminals on all four sides (top). For large DRAMs, the package has terminals on only two sides, also being called SOJ. The bottom figure shows a 1 or 4 Mbit DRAM package.

Table 4.4 Dimensions for PLCC packages. Format means the number of terminals on two neighbouring sides.

Leads	Format	Lead pitch [mm]	Maximum body dimensions [AxB] [mm]	Maximum Device Dimensions (LxW) [mm]	Typical Height (C) [mm]
20	5x5	1,27	9,1x9,1	10,1x10,1	3,5-4,7
28	7x7	1,27	11,6x11,6	12,6x12,6	3,5-4,7
44	11x11	1,27	16,8x16,8	17,8x17,8	3,5-4,7
52	13x13	1,27	19,3x19,3	20,3x20,3	3,5-4,7
68	17x17	1,27	24,4x24,4	25,4x25,4	3,5-4,7
18	5x4	1,27	10,9x7,5	11,9x8,5	3,5-4,7
28	9x5	1,27	14,1x9,0	15,1x10,0	3,5-4,7
32	9x7	1,27	14,1x11,6	15,1x12,6	3,5-4,7

The other type of chip carrier is ceramic and has no leads, thus the name Leadless Chip Carrier (LLCC), Figure 4.21 and Table 4.5. The terminals are metallised areas on the ceramic body. The ceramic makes the package hermetic, and it has thermal properties much superior to the plastic IC packages (Chapter 6) when they are soldered to the substrate.

However, the missing flexible leads give a disadvantage: Thermal mismatch to organic PCBs. The TCE for glass epoxy laminates is 12 - 16 ppm/°C, whereas the alumina ceramic has 6 ppm/°C. When the temperature changes during soldering processes and operation, this mismatch will give mechanical stress and in time possibly broken solder fillets. This is particularly a problem for the larger LLCCs and has reduced the usage of LLCC. Some types are made for socket mounting, or a set of leads can be soldered onto the LLCC. For leaded packages, stress due to the thermal mismatch normally is negligible.

Fig. 4.21 shows all the standard forms of chip carriers. A - D are LLCCs, type C is the most common for direct soldering on a substrate. It is made with three layers of ceramic. The other types are primarily for socket mounting or soldered-on leads. The components normally have metal lids that are soldered on with a solder alloy of high melting temperature, so it does not fall off during the component soldering. Alternatively, the lid may be ceramic too.

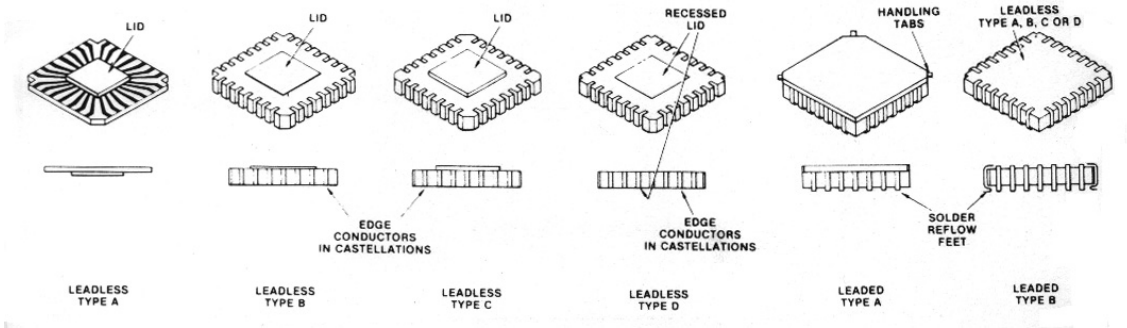


Fig. 4.21 a): The various types of ceramic chip carriers [4.15]. Types A -D to the left are leadless (LLCC), whereas types A and B to the right are meant for mounting leads (LDCC).

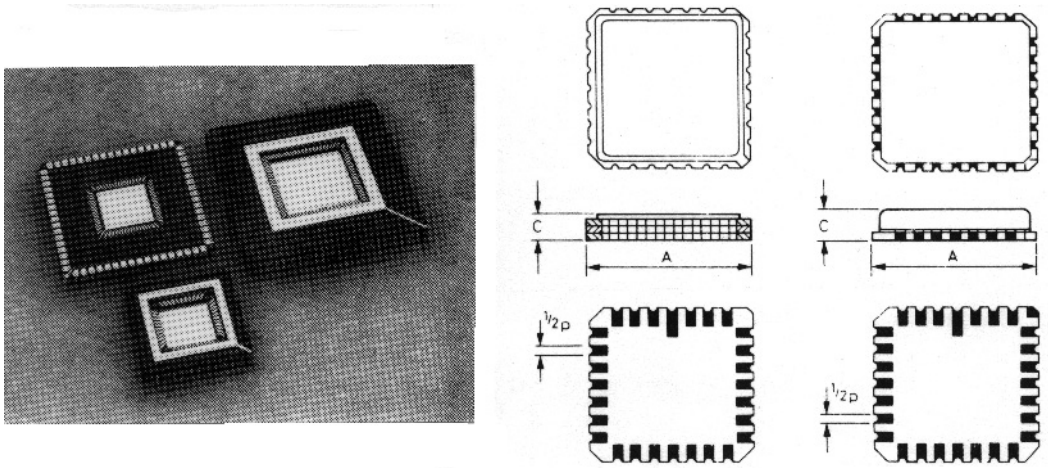


Fig. 4.21 b): LLCC packages, additional details. The longest terminal is to designate electrical terminal number 1 in the circuit.

Table 4.5. LLCCs, dimensions.

Leads	Format	Pad Pitch (p) [mm]	Maximum Dimension (AxB) [mm]
20	5x5	1,27	9,1x9,1
28	7x7	1,27	11,6x11,6
44	11x11	1,27	16,8x16,8
52	13x13	1,27	19,3x19,3
68	17x17	1,27	24,4x24,4
84	21x21	1,27	29,6x29,6
18	5x4	1,27	10,9x7,5
28	9x5	1,27	14,1x9,0
32	9x7	1,27	14,1x11,6

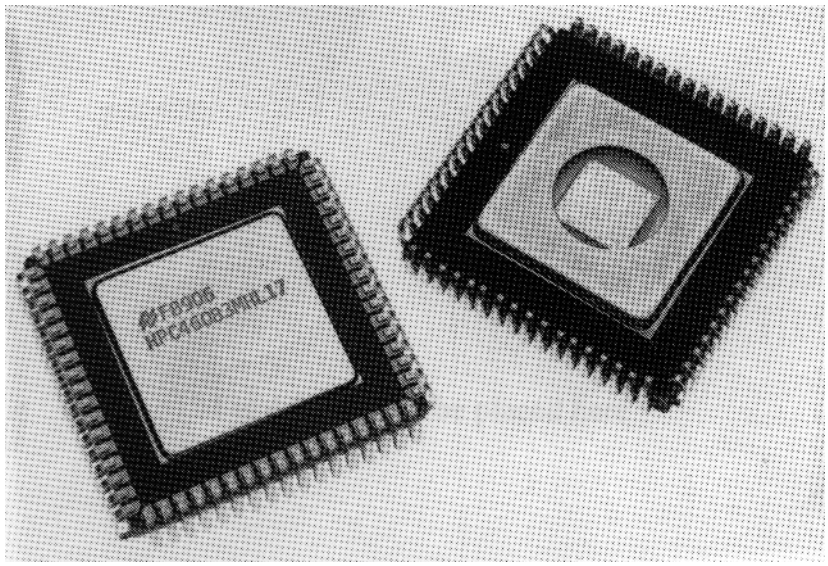


Fig. 4.22: Leaded ceramic chip carriers.

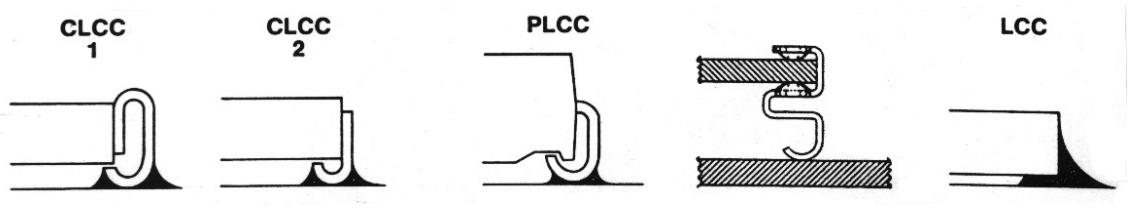


Fig. 4.23: Various shapes of the leads, and leadless termination for comparison.

Leaded ceramic chip carriers (LDCC), see Figure 4.22, with gull wing or J-shape leads are in limited use. The leads have various shapes, giving high or low flexibility, see Figure 4.23.

A plastic type of leadless chip carrier has been developed in the United Kingdom under the name EPIC [4.16]. The body is machined from glass/epoxy, giving perfect thermal match to glass/epoxy PCBs. The idea seems good, but the package is not much in use.

Flatpacks and mini-flatpacks

Flatpacks have been used in hybrid technology for many years, also for packages for a complete hybrid circuit (See Chapter 8). They are made out of plastic or ceramic (and metal for hybrid circuit packages). Some have leads on two sides and some on four (Quad flatpacks), see Figure 4.24. Often the leads come out from the central plane of the body, and end in a shorting frame or ring that protects the leads from being bent, as well as protecting the IC (see Section 4.8). When they are mounted the ring must be cut off, and the leads bent to a gull wing shape if the component is mounted on a flat surface.

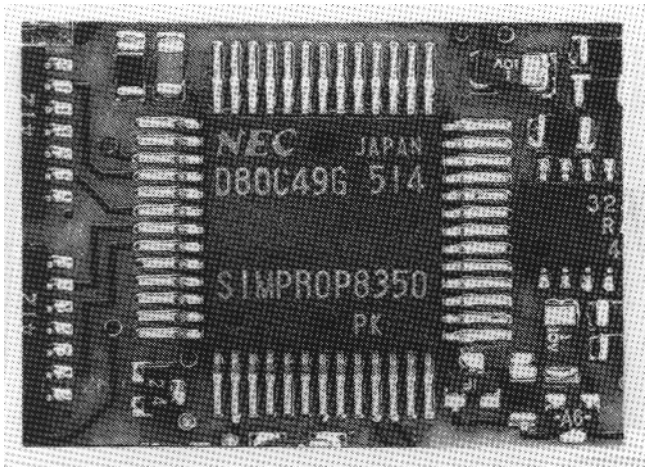


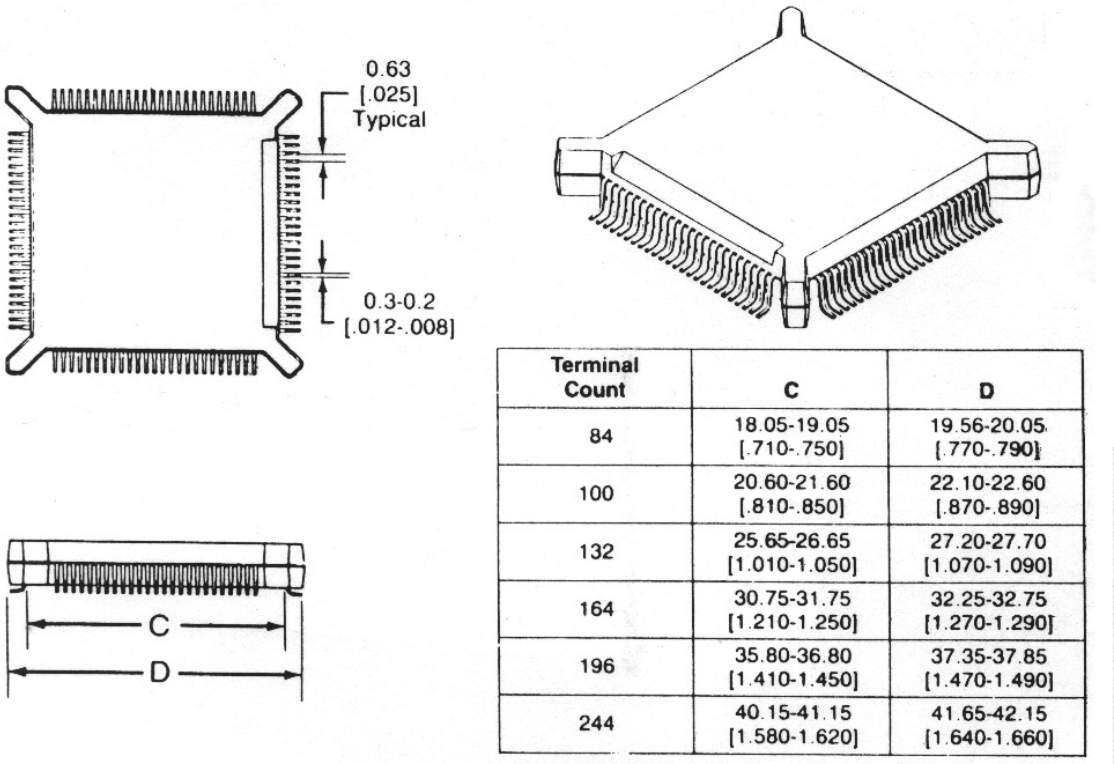
Fig. 4.24: Quad flatpack with leads on all four sides.

Many sizes and lead pitches are used for flatpacks. In the USA 50 mils, 25 and 20 mils dominate, in Japan 1.25, 1.0, 0.8, 0.65 mm. Up to 300 terminals are available for plastic or ceramic flatpacks.

One type of plastic package is called Fine Pitch Quad Flatpack or Mini-flatpack.This package has been accepted by JEDEC as a new industry standard for 84 - 244 terminals and a pitch of 25 mils, see Figure 4.25. It has a gull wing lead shape. Because they are thin, the leads are very vulnerable to deformation during transport and handling. As protection, the package has a characteristic protuberance at each corner. The transport tube is formed such that the protuberances touch the walls, but not the leads.

4.5.4 TapePak and moulded carrier ring packages

National Semiconductor has developed a compact and elegant plastic package "TapePak", that is on its way to become another industry standard for demanding applications [4.17]. The IC is moulded into the central plastic body, see Figure 4.26. The connections to the chip are made by Tape Automated Bonding (TAB) using one-layer tape (Chapter 3), that serves as leadframe. The TAB leads stick out of the central body, at a pitch of 20 mils or less. Further out there is a plastic ring for protection, and the leads go through it too, ending in test points for component testing. The test points have a pitch of 50 mils, making it possible to have a simple and rugged test fixture. During mounting, the leads are cut inside the outer ring in an excising operation, and they are bent to gull wing form, in a combined cut-and-form tool. Then the mounting is done, all in the same automatic machine.



Terminal Count	C	D
84	18.05-19.05 [.710-.750]	19.56-20.05 [.770-.790]
100	20.60-21.60 [.810-.850]	22.10-22.60 [.870-.890]
132	25.65-26.65 [1.010-1.050]	27.20-27.70 [1.070-1.090]
164	30.75-31.75 [1.210-1.250]	32.25-32.75 [1.270-1.290]
196	35.80-36.80 [1.410-1.450]	37.35-37.85 [1.470-1.490]
244	40.15-41.15 [1.580-1.620]	41.65-42.15 [1.640-1.660]

Fig. 4.25: Mini flatpack.

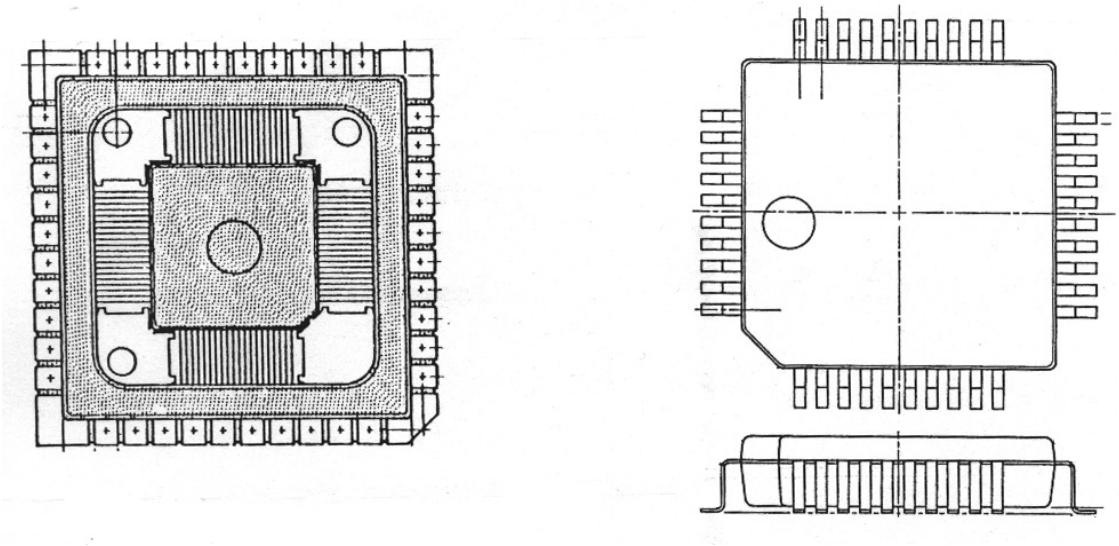


Fig. 4.26: National Semiconductor´s TapePak component packages are specified with terminal numbers between 40 and close to 600. To the left we see a 40 leads TapePak in the form it is received by the user with a protective ring around it, and test points outside the ring. To the right is TapePak 40 after excising and lead bending, seen from above and from the side.

TapePak has standardised dimensions for components with between 40 and about 600 leads. Pitch for the smaller packages is 20 and 15 mils. For the larger packages it is metric, down to 0.25 mm.

The concept has many advantages for compact packaging of complex circuits: They take up very little board space (similar to TAB circuits), They are rugged during transport and testing, and the testing is easy. Finally, TapePak has the possibility of a larger number of I/Os than any other standard package.

A major problem is that expensive equipment is needed for the mounting, including the cut-and-form tool that is specific for each size. Mounting and soldering are challenges requiring refined processes. The mounting equipment needs electronic vision to achieve the necessary accuracy.

Around one dozen companies use TapePak today, for special high volume circuits. Some component manufacturers make a modified version of TapePak, called "Moulded carrier ring". It looks similar to TapePak but uses a regular leadframe and wire bonding for electrical contacts to the chip.

4.5.5 High performance packages

The most demanding electronic systems have components that operate at clock frequencies 100 MHz – 1 GHz, (higher in the future) dissipating a power of 2 - 10 Watts and more, some have several hundred in- and outputs. Standard component packages cannot satisfy such demands.

To improve the ability to remove the heat, one can mount cooling towers on both plastic and ceramic packages and cool with fans (please refer to also Chapter 6, thermal design). Some plastic and ceramic packages are made with a metal plate or metallised via holes underneath the semiconductor chip, through the bottom, and the package can be soldered to the component substrate at these points, to use the good thermal conduction of the metals. This is designated "thermal vias", see Figure 4.27.

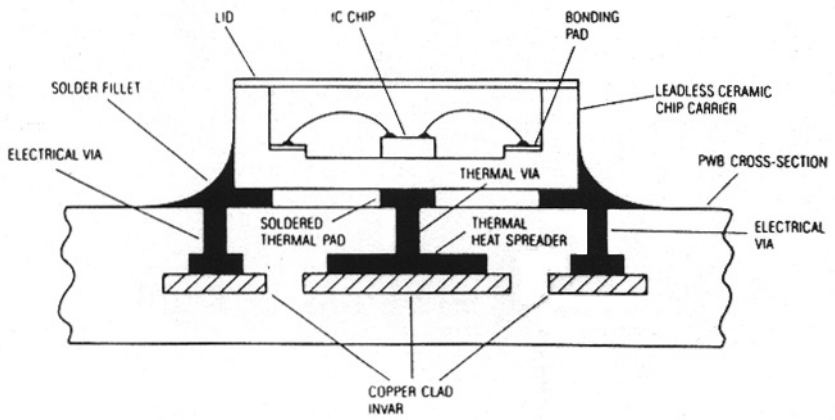


Fig. 4.27: Thermal via-holes in the printed circuit board, for better heat conduction.

Packages for power electronics, demanding computer circuits, etc., are in some cases made with AlN ceramic, which has thermal conductivity one order of magnitude better than Al_2O_3. Another advantage with AlN is low thermal coefficient of expansion. However, until now the material has been very costly, and special processing is required to get the conductor materials to give good adhesion, please refer to Section 8.6.

Special high frequency packages must have a controlled characteristic impedance for all critical signal paths, and it is important to have decoupling capacitors close to the power terminal for the Si- or GaAs chip (please refer to Chapter 6). Such packages are often designed especially for the circuit. They are built from many layers of ceramic, with separate metal layers for ground and power plane, and signal layers between, with transmission line geometry (Chapter 6). Figure 4.28 shows such a component, made by Triquint Semiconductor. On top of the package there are soldering terminals for mounting of decoupling capacitors/termination resistors.

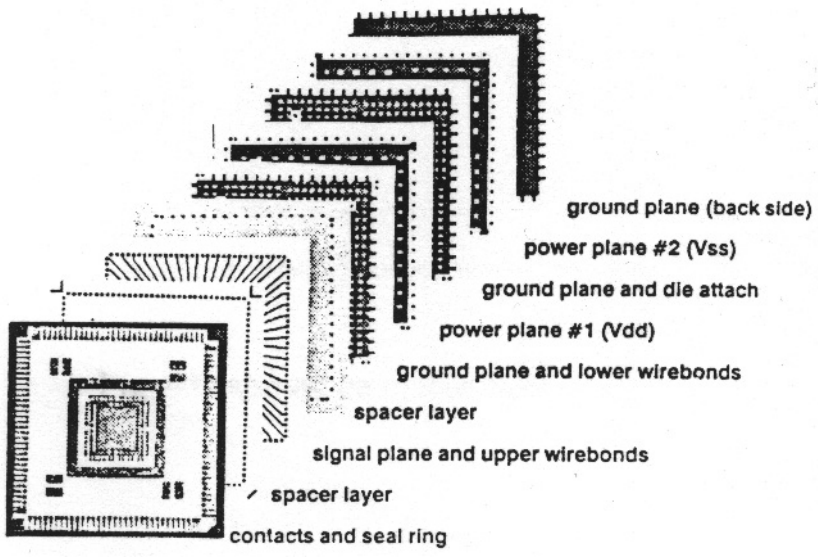


Fig. 4.28: Multilayer package for high frequency GaAs circuits with 3 ground planes, 2 voltage planes, 1 signal layer and a top conductor layer for contacts and sealing (Triquint).

The company Gigabit Logic has chosen a different solution for their GaAs circuits. Here the chip is mounted on a Si substrate, where the decoupling capacitors and termination resistors are made by monolithic technology in the substrate.

Figure 4.29 shows a module with several ECL chips for Hitachi computers. Here the Si chips are mounted with flip chip on Si substrate. The package has a bottom of SiC for good heat conduction to a cooling fin.

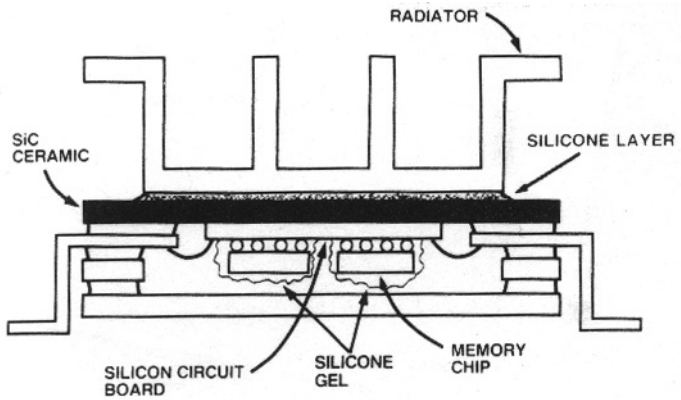


Fig. 4.29: Multichip package for memory module in a Hitachi high-performance computer [4.18]. The module contains 6 ECL chips, mounted by flip chip.

The last examples show packaging of several chips in the same package, and use of Si as substrate for IC circuits. Such multichip modules will be discussed in more detail in Chapter 8.

4.5.6 Future trends

The development of electronic systems tends toward denser packaging, higher working frequency, and higher power generated per unit volume, as mentioned earlier (Chapter 2). This gives constantly increasing demands on the component technology and packaging. The use of compact forms of packages is increasing. Figure 4.30 shows the area required for an IC with approximately 64 terminals, in different forms of encapsulation.

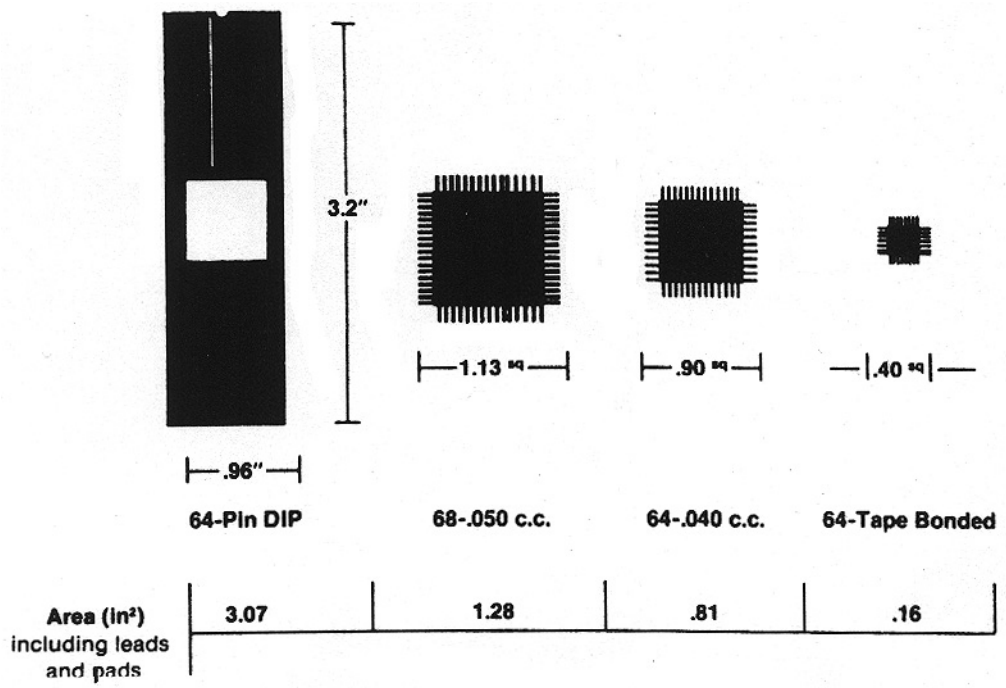


Fig. 4.30: Comparison between the size of various package forms for an integrated circuit with approximately 64 terminals.

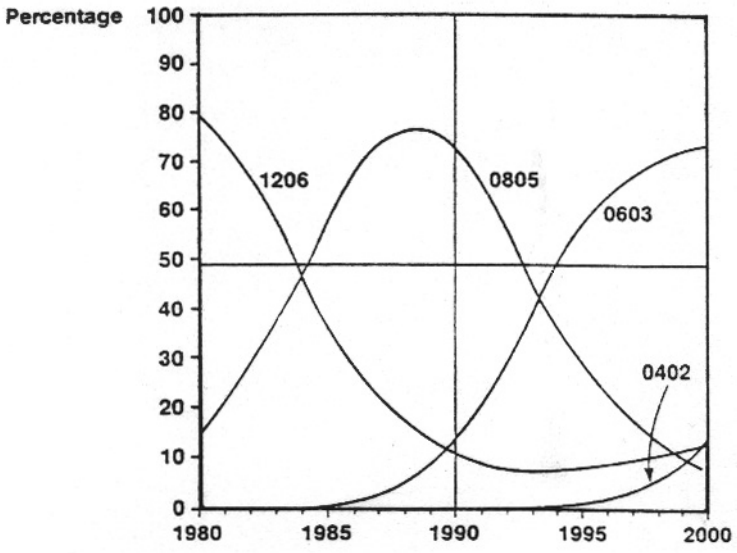


Fig. 4.31: History and prognosis for the use of various sizes of passive SMD components, in percentage of the total number (K. Wassink, ISHM Nordic).

A prognosis for the use of DIP, SMD and TAB packaging was shown in Figure 2.3, indicating an increasing use of more compact packages or chip on board. Fig. 4.31 shows a prognosis for the use of passive components in different sizes, also demonstrating a trend toward more miniaturisation. The development toward smaller packages will give major challenges to the component producers and to the electronic systems producers.

4.6 VARIOUS COMPONENTS

The components discussed until now are the most common categories, both for digital and analogue circuits. However, for the complete system special components are often required, such as:

- Connectors
- Potentiometers
- Inductors
- Transformers
- Crystals
- Switches
- Sockets
- Displays, etc.

They are often termed "odd" components. There are so many types of them and there is so little standardisation, that it is outside the scope of this course to treat them all. They often complicate the mounting and soldering processes. They may give high cost, because they must be mounted and soldered manually in many cases. They require special consideration in the development and design phase of the electronic product.

Mechanical components that provide the mechanical support of the electronics are also important, and they also require special consideration in the design phase. These components are made of metal, plastic and other materials. They may represent a major part of the system cost.

4.7 TERMINAL METALLISATION, SOLDERABILITY AND RELIABILITY

The metal layer on the leads/terminals areas where the components need to be soldered or glued is important for the solderability and for long term reliability of the soldering.

The components may be stored several months. Spare parts are often stored many years before they are mounted and soldered into the system. Also then, the solderability must be good. The metallurgy is particularly important for SMD components because the solder joints serve as electrical connections as well as mechanical support to the component. In addition, the dimensions of the solder joints are small. The components experience great thermal stress during the solder processes, when the whole component gets a thermal shock.

4.7.1 Passive components

For SMD resistors and multilayer ceramic capacitors, silver or a silver alloy is used closest to the ceramic, because it gives good adhesion. However, silver has very high solubility and high speed of solution in solder metal, as pointed out in

Section 3.10. Thus, we risk that the silver is dissolved during the solder process ("leaching") or diffuses in the solid phase during the normal operation of the equipment. This may give electrical discontinuity, or the component may even fall off. Several alternatives are used to avoid this [4.3, 4.4, 4.7]. One alternative is to alloy the silver with up to 20 - 35 % palladium or possibly platinum, that reduces the solubility. By using a small percentage of silver in the solder metal, the solubility is further reduced, see Figure 3.17.

Alternatively, a layer of nickel is deposited outside the silver (the silver alloy), as a diffusion barrier.In addition, it is common to use tin or a eutectic mixture of tin/lead, to avoid oxidation of the nickel during soldering. This is done to ensure a good solderability.

If the components are to be glued (e.g. in thin film hybrid circuits), there must be no Sn/Pb in the outer layer. The electrically conductive adhesives contain silver, which will in that case be dissolved.

Nickel is harder than the other metals, and it gives mechanical stress during quick changes of temperature because of this. The noble metals used on the terminations are quite costly. What type of termination is most suitable depends on environmental requirements, area of application and the sensitivity to price for the components and for the system.

4.7.2 Integrated circuits

During their processing ceramic DIP packages or LLCC packages get a thin layer of high purity, soft gold on the metallised areas, both inside, where the bonding wires from the silicon chip are connected, and outside, where the package is to be soldered to the substrate. The gold is good for bonding and also has the advantage that it does not corrode during long time storage. However, gold in mixture with solder metal gives poor strength in the solder fillet, and it gets brittle, see Figure 4.32. That is because of the generation of inter-metallic mixtures of gold and tin/lead: $AuSn_2$, $AuSn_4$, and others |4.21]. For demanding applications it is required that the gold on the component soldering areas is removed by dipping the component in a molten solder alloy. The gold is rapidly dissolved in the solder alloy, and instead the component gets a layer of solder alloy. (There is a debate about how much gold is needed to harm the solder fillet [4.4, 4.19, 4.20]. A standard requirement is that there should be less than 0.5 % gold in the solder bath and less than 1 % in the solder fillet.)

For integrated circuit packages with leads, the lead frame metal - "alloy 42" or pure copper - is coated with solder alloy by plating or dipping into a solder bath.

Control of the termination metallisation and solderability is an important part of quality control (see Chapter 9).

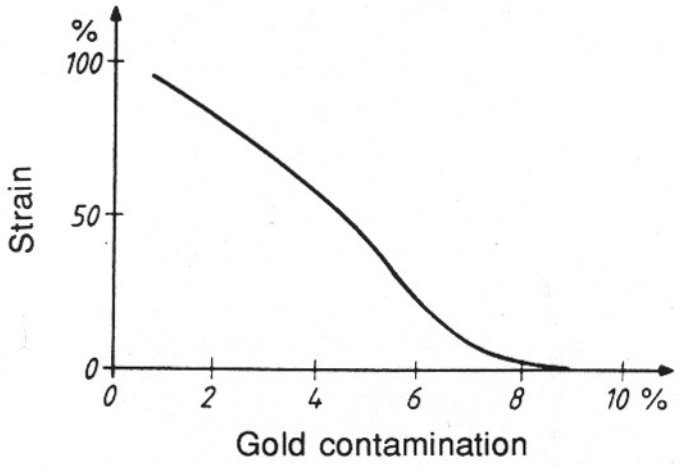


Fig. 4.32: Strain at fracture of solder fillet as function of gold concentration in the solder metal, relative to value without gold [4.20].

4.8 ELECTROSTATIC DISCHARGES - COMPONENT DAMAGE AND PRECAUTIONS

Electrostatic discharge (ESD) is today assumed to be the most important single source of damage of active electronic components, which costs billions of dollars annually. A part of the problem is that ESD is so difficult to document, and it is very difficult to show that a demonstrated damage is caused by ESD. We shall briefly describe how ESD arises, its effect on semiconductor circuits, and how one can take precautions to protect the circuits and avoid damage. Details are given in [4.21].

Tribo-electricity is electric charging by friction. Humans who walk on carpets made of synthetic materials, or who pat a cat, can be charged up to 10 - 20 000 V. The charge is in the range of a few tenths of microJoule, but it can give instantaneous power dissipation of kW during a fraction of a microsecond. Most people have experienced this by the shock they can get by touching a grounded doorknob afterwards. The electronic components may be charged up analogously, either because people handle them, or because of friction against unsuitable plastic packaging, containers, etc. A component that has been exposed to voltages on some of its terminals, while other terminals are grounded will be destroyed instantaneously.

Let us take for example an MOS-transistor, see Figure 4.33. The gate oxide typically is between 20 and 1000 Å thick, and it has a break down field strength 800 kV/mm if the oxide is perfect. That means that if the voltage on the gate is made greater than 1,6 - 80 V, the oxide will break down. This happens by impact ionisation or avalanche breakdown and the subsequent melting of Si, see Figure 4.34, or by destruction of the oxide. The damage may be latent, such that the component still works, but it has been weakened against new ESD. Alternatively, cracks can be created where moisture and impurities accumulate, and the component will be harmed by these elements or materials during exposure over longer periods of time.

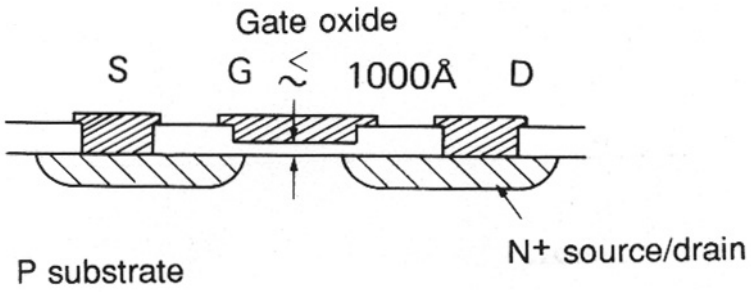


Fig. 4.33: MOS transistor schematically.

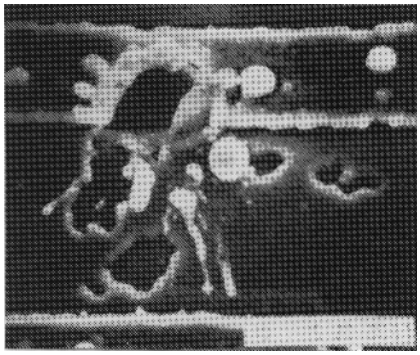


Fig. 4.34: CMOS circuit exposed to electrostatic damage: silicon has molten in a small area (5000 x).

Even bipolar components are sensitive. The P/N junctions in components made by today's technologies are a fraction of a μm deep, with high gradients in the doping concentrations. When voltages of 10 - 50 V are reached the breakdown field strength in Si is exceeded, both for P/N junctions and Schottky barrier junctions.

To increase the tolerance of the components to ESD, modern IC components are made with protection circuits at the in- and outputs, see Figure 4.35. The purpose is to conduct the current from the discharge to the power supply or to ground by diodes that are in the conducting direction for voltages above V_{cc} or below ground level (or below the level of the most negative voltage in the circuit). The protective circuits reduce the performance of the circuit by parasitic capacitances at the inputs, etc., and they require much valuable chip area. It is therefore limited how good the protection is made but with protective circuits components of today typically tolerate 500 - 8000 V discharges.

Additional protection must be made by using suitable component packaging, see below, and by a suitably shaped working area with grounding of operators and equipment, see Chapter 7. Today it is accepted that all components should be treated as if they where electrostatically sensitive to get a total working discipline. Control of the humidity is also of importance since the ESD is worser at very dry conditions.

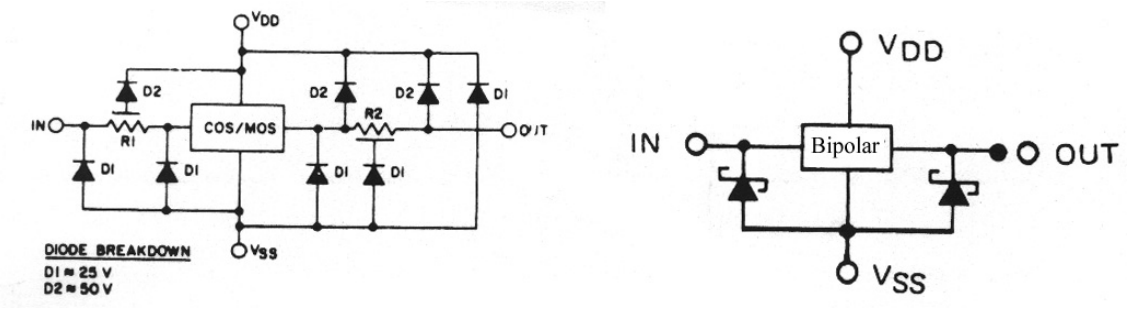


Fig. 4.35: ESD protection circuit at in- and outputs for MOS and for bipolar circuits.

4.9 COMPONENT PACKAGING FOR AUTOMATIC PLACEMENT

It is important for an efficient production process that the components can be bought in a form of packaging which makes handling efficient and that is adapted to automatic placement machines with little or no adjustments.

Hole mounted axial components (resistors, capacitors) are supplied on paper tape. The ends of the components are held between two layers of sticky tape, and the tape is rolled on to a reel. Radial components (capacitors, transistors) are supplied on similar tape. When the components are to be removed from the tape, the leads are cut in the placement machines or in the sequencing machines (see Chapter 7).

The most efficient form of packaging for small surface mounted components (resistors, capacitors, transistors, small integrated circuits, etc.), is the so-called "blister tape", please refer to Figure 4.36. Each component is in a recess in a tape, which is normally made of plastic. A thin protective film is on top, sticking to the tape, so that the components do not fall out.

The blister tape comes in standard formats, of width 8, 12, 16, 24 mm, depending on the component sizes. For the smallest chip components there are 4.000 or 10.000 per reel.

Conductive, metallised plastic tape, or tape made of aluminium, is used for components that are sensitive to electrostatic discharges.

The blister tape is especially well suited for pick-and-place machines mounting SMD components.

For DIP integrated circuits plastic "stick magazines" are the most common form of packaging, see Figure 4.37. Sticks are also much in use for surface mounted integrated circuits. The plastic has an anti static coating to avoid generation of static electricity. Metal sticks are also used to some extent. Even this packaging form is well suited for automatic mounting.

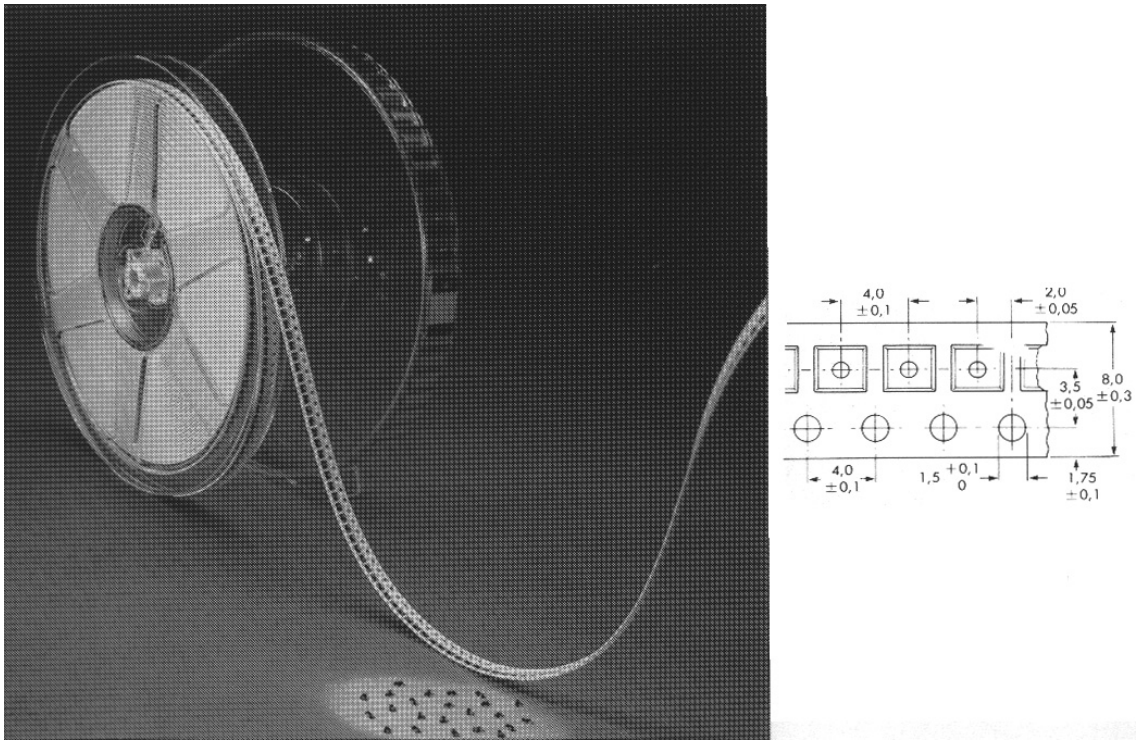


Fig. 4.36: Blister tape for surface mounted components. Standard dimensions for 8 mm wide tape.

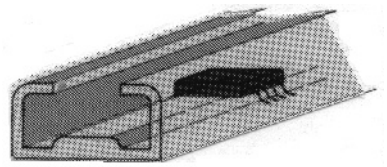


Fig. 4.37: Plastic sticks as packaging for SMD integrated circuits.

For flat packs the so-called "waffle trays" are much used, see Figure 4.38. Here, the components are lying side by side in recesses in a plastic sheet, like chocolate pieces in a box. The sheets are placed layer upon layer on top of each other.

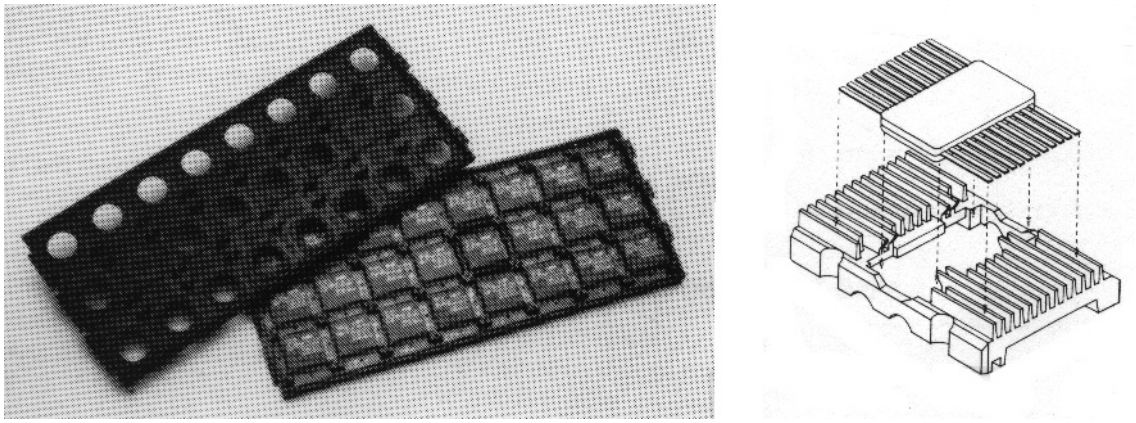


Fig. 4.38: Waffle trays packaging for flatpacks to the left, frame for stacking of single component to the right.

The waffle tray packaging is less suitable for mounting with the ordinary pick-and-place machines (Chapter 7). However, programmable mounting robots can pick components efficiently from such packaging.

Another packaging form for flatpacks is individual plastic frames that can be stacked on top of each other in a magazine, "stack magazines", during transport and mounting.

Components in small quantities are often supplied in bulk, i.e. packed only in a plastic bag. When these components are to be mounted automatically, they have to be oriented in a vibration feeder.

Special components are delivered in many forms of packaging. For nearly all of them, it is a fact that they are poorly adapted to automatic production of the printed circuit boards.

REFERENCES

[4.1] S.M. Sze: "VLSI Technology." (2nd Ed., McGraw-Hill, 1988)

[4.2] G. Leonida: "Handbook of Printed Circuit Design, Manufacture, Components and Assembly." (Electrochemical Publications 1981)

[4.3] J. F. Pawling: "Surface Mounted Assemblies. " (Electrochemical Publications 1987, p. 49.)

[4.4] C. Lea: "A Scientific Guide to Surface Mount Technology." (Electrochemical Publications 1988.)

[4.5] Siemens Components 1989, no. 5, p. 175.

[4.6] D.M. Trotter: "Capacitors". Scientific Am. July 1988, p. 58.

[4.7] H. Hvims: "Effects of terminal metallization on SMT soldering." ElektronikCentralen, ECR-242, 1990. (In Danish.)

[4.8] R.C. Buchanan: "Ceramic Materials for Electronics." (Marcel Dekker, 1986.)

[4.9] L.M. Levinson: "Electronic Ceramics." (Marcel Dekker, 1988).

[4.10] J.E. Buchanan: "Chip Capacitors and Dielectric Absorption." Electronic Production, May 12, 1983, p. 107.

[4.11] J. Maxwell: "Surface mount Soldering Techniques and Thermal Shock in Multilayer Ceramic Capacitors." Component Technical Information, AVX Corporation.

[4.12] H. Danielsson, Proc. ISHM-Nordic.

|4.13] Component data book, Siemens.

[4.14] F. Hilbert: "Tantalum Electrolytic Capacitors without Series Resisto." Siemens Components XXV (1990) no. 5, p. 181.

[4.15] IPC CM-782.

[4.16] N. Sinnadurai: "Handbook of Microelectronics Packaging and Interconnection Technology." (Electrochemical Publications 1985.)

[4.17] L. Halbo and A. Bjørkløf: "TapePak Evaluation." Report to Nordic Industry Fund, 1990.

[4.18] a): A. Bar-Cohen: "Thermal Management of Air- and Liquid-Cooled Multichip Modules. "IEEE Trans Comp. Hybr. and Mfg Tech. CHMT-10 no. 2, June 1987, p. 159.
b) Siemens Components 1983 no. 5 p. 191.

[4.19] S. Ohlsson: "The Effect of Pretinning on the Strength of a Chip Carrier Solder Joint." Quality and Reliability Engr. Int., Vol. 4, p. 215 (1988).

[4.20] K. Wassink: "Soldering in Electronics." (Electrochemical Publications, 2nd Ed. 1989.)

[4.21] L. Halbo: "Electrostatic Discharges - the Component Killer." Elektro 1985: no. 4, p.30, no. 8, p.38, no. 10, p. 41. (In Norwegian.)

CHAPTER 5

PRINTED WIRING BOARDS

5.1 INTRODUCTION

The substrate on which the components are mounted has several purposes:
- Mechanical support for the components.
- Electrical interconnection, "wiring", between components and other parts of the system.
- Conduction of the heat from the components.

The component carrier for printed circuit boards is generally designated printed wiring board. Many people, even with no components mounted often call it printed circuit board. This is confusing and should be avoided. Bare board is also used to some extend. For hybrid circuits and multichip modules it is called substrate (see Chapter 8).

5.2 PRINTED WIRING BOARDS, GENERAL

Strict demands are posed on the properties of the printed wiring board, such as:
- Good electrical properties: High insulation resistance, high break down field strength, low dielectric constant, low dielectric losses.
- Mechanical strength and dimensional stability, under high temperature processing and in field use.
- Chemical resistance against solvents, solder fluxes, and aggressive atmospheres during use.
- Not flammable, even during solder processes at 200 - 260 °C.
- Favourable mechanical processing ability: Easy to drill, mill, and punch.
- Good adhesion between the different materials in the wiring board.
- Low moisture absorption.

The starting material for printed wiring boards is called the laminate, and it consists of many laminated layers of binder and reinforcement. Common binders are epoxy, and for low price consumer products with low requirements on reliability, phenolic. For high performance and demanding applications polyimide and other materials are used, see Sections 5.10 and 5.11. Common forms of reinforcement are woven glass fibres, see Figure 5.1, and paper for low price laminates. Quartz and aramid (Kevlar) are used to a limited extent, they are costly and difficult to process [5.4]. Table 5.1 shows different types of conventional printed wiring board materials. Various other materials are under development for high performance boards, see Sections 5.10 and 5.11.

Today, glass/epoxy laminates are the most common; particularly the type that is designated FR-4. FR means flame retardant, contrary to the earlier materials that might start burning during the wave solder process or during other unfavourable conditions.

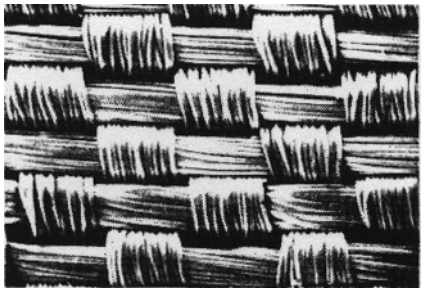


Fig. 5.1: Woven glass fibre for printed wiring board reinforcement.

Table 5.1: Conventional laminates for printed wiring boards. (The designations are according to National Electrical Manufacturers Association, NEMA, USA.)

	Resin			Reinforcement				Flame
Grade	Epoxy	Polyester	Phenolic	Cotton paper	Woven glass	Mat glass	Glass veil	retard-ant
XXXPC			*	*				
FR-2			*	*				*
FR-3	*			*				*
FR-4	*				*			*
FR-5	*				*			*
FR-6		*				*		*
G-10	*				*			
CEM-1	*			*	*			*
CEM-2	*			*	*			
CEM-3	*				*	*		*
CEM-4	*				*	*		
CEM-5		*			*	*		*
CEM-6		*			*	*		
CEM-7		*				*	*	*
CEM-8		*				*	*	

Figure 5.2 shows the composition of printed wiring boards, of various degrees of complexity. The simplest type, see Figure 5.2 a), has only one layer of copper metal foil for conductors, on one side of the board. Surface mounted components are mounted on this side, whereas hole mounted components are mounted on the opposite side, with leads passing through holes in the board. For boards that are more complex, we need wiring on both sides. It is common to have conducting connections between the two sides in plated through via holes, see Figure 5.2 b). The surface of the conductor pattern may be copper or alternatively tin/lead solder metal, which is also plated. Both types have advantages and disadvantages, see Section 5.6.2.

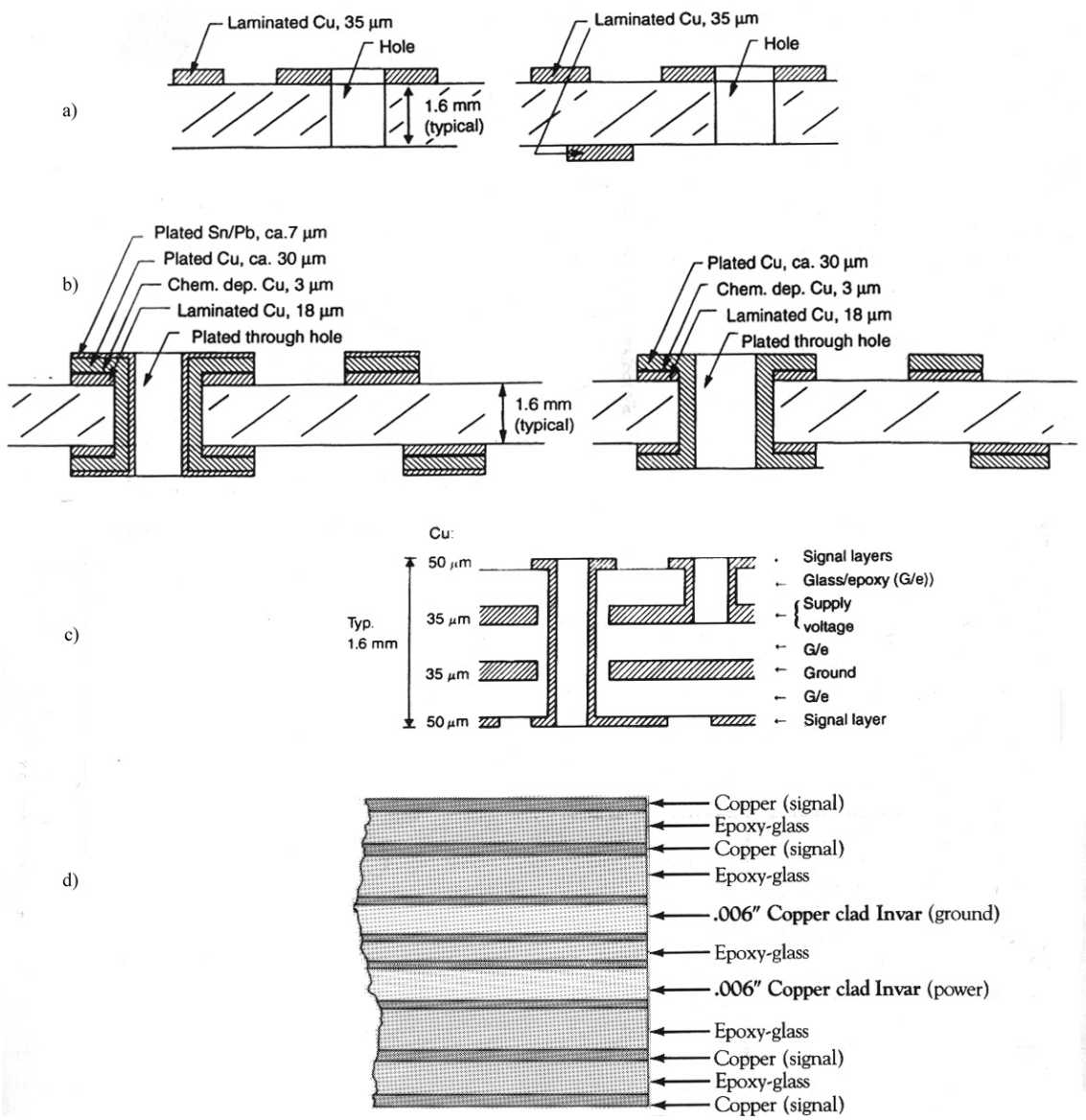


Fig. 5.2: Printed wiring board structures with varying complexity:
a) Single sided and double sided.
b) Double sided through hole plated with bare Cu or Sn/Pb surface.
c) Four layer board.
d) Six layer board with two Cu/Invar/Cu cores.

More complex circuits with a very dense component placement and VLSI components with many inputs and outputs, often require more than two layers of

interconnect wiring, and it is necessary to use multilayer wiring boards, see Figure 5.2 c). They have plated through via holes through the whole board, but they may also have via holes through parts of the board, see Section 5.7. For circuits with high heat dissipation one or more thick metal cores are used, each metal core may be composed of several laminated sheets of metal, see Figure 5.2 d). This composition has several advantages, see Section 5.9.

5.3 GENERATION OF DESIGN DATA, PHOTO- OR LASER PLOTTING

The wiring board design, from net list and schematics to conductor pattern layout is normally made on a computer assisted design system (CAD), where detailed component information is stored, including geometrical information about the solder lands for each type of component (see Chapter 6). The CAD system also has stored information about minimum conductor distances, minimum conductor width and other design rules, and it gives a warning if the designer attempts to break these rules. The designer enters net list and component placement into the CAD system, he generates the circuit diagram, performs simulation and routing of the conductor pattern. The routing may to a large extent be done automatically, but the designer can choose to specify critical paths manually.

The layout consists of information about:

- Component placement.
- Conductor pattern between the components, in one or more wiring layers, solder lands and hole pads.
- Holes for component leads, via holes for electrical contact between different conductor layers, registration holes for accurate positioning of the circuit board during solder processing and component mounting.
- Contour of the board.
- Printing mask for solder resist and solder paste printing, etc.

The information in the CAD system is post-processed to a format suitable for the further processing, which is photo- or laser plotting. One also obtains information for numerically controlled drilling and milling machines that are needed for production of the wiring board, pick-and-place machines, testing and test fixtures, component listing for purchase, drawings and other documentation.

The photo plotter, please refer to Figure 5.3, generates photographic films that correspond to the different patterns on the wiring boards: Conductor patterns with solder lands, solder resist, solder paste print, component marking for the mounting, etc.

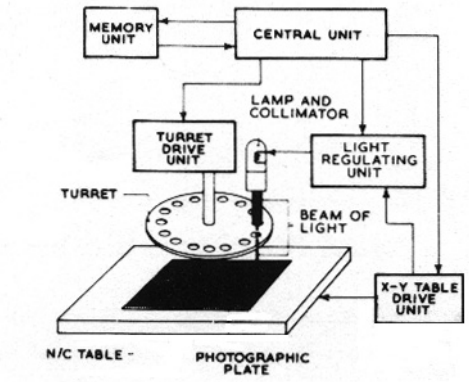


Fig. 5.3: Photo plotter, schematically.

The film that is to be plotted in the photo plotter, lies on moveable a table, which can be moved in the x- and y-direction, controlled by the data from the CAD system. A light source illuminates the film over a small area at a time, through a so-called plot wheel. The wheel has openings of different sizes, so it is possible to choose the size of the film area that is illuminated at any time. We can illuminate lines with constant width by moving the x - y table while the light goes through a particular opening. The width of the conductor can be changed by rotation of the wheel, bringing a different opening into position. A single flash illuminates a circular area, and areas of complex form are made by moving the table back and forth and "paint" with a small light spot. The whole illumination process is done automatically. Then the film is developed.

The laser plotter is on its way to take over from the photo plotter. In the laser plotter a laser beam sweeps across the film, line by line, while it is turned on and off depending on whether the points on the line are to be blackened on the film or not.

5.4 FABRICATION OF GLASS/EPOXY WIRING BOARD LAMINATES

Epoxy resin is generally made from ethylene chlorohydrin and bisphenol-A [5.1, 5.3, 5.9 b, 5.21]. When the material is heated under pressure, the process called polycondensation takes place between these materials and the cross-linking of the polymer starts. It is still not completely cured, but in the so-called B-stage (see Chapter 3). The material melts at high temperature, and in this state it is soluble in suitable chemicals.

The laminate is made from many layers (typically 7-10) of woven glass fibre that are saturated with resin in the B-stage. They are placed layer upon layer in a lamination press, with one layer of copper foil on one or both sides, depending on what sort of wiring board is being made. High pressure and high temperature in the lamination process cause the resin to melt and create a uniform material. At that time the rest of the polymerisation process to the C-stage takes place, and we get a complete glass/epoxy material that is highly resistant to chemicals and climatic exposure.

The most common thickness of the laminate is 1.6 mm, with 18 or 35 µm Cu foil (also called 1/2 or 1 ounce, because of the weight per square foot of the copper foil). The metal is rolled or electrolytically deposited.

This process is only done by a few large specialised firms. For one or two layer wiring boards, a laminate with copper foil in large panels is the starting material for the wiring board producer. For production of multilayer boards the producer of the wiring boards must also do a laminating process, see Section 5.7.

5.5 SINGLE SIDED WIRING BOARDS

The simplest way to define the conductor pattern on single sided wiring boards is the so called print and etch process [5.1], that is suitable for coarse conductor pattern.

We start with a laminate of paper/phenolic, glass/epoxy or a mixture. After cutting to suitable standard sizes, the main steps of the "print and etch" processes are as follows, please refer to Figure 5.4:

1. Drilling or punching of registration holes.

2. Panel cleaning: Mechanical brushing or chemical rinse (light etch) to remove oxide, grease etc.

3. Printing of etch resist: An organic material that is resistant to the etch bath for the subsequent etching process is screen printed on to the surface through a printing mask with the correct conductor pattern, see Chapter 3. The etch resist is cured at elevated temperature or with UV illumination.

4. Etching: This takes place by dipping the panel into an etch bath, or using an etching machine that sprays etchant uniformly over the whole surface, until all copper has been dissolved where it is not covered by etch resist. Common etchants are solutions of $CuCl_2$ or $FeCl_3$. Then the panel is rinsed.

5. Stripping: The etch resist is dissolved in a suitable solvent.

6. Printing of solder resist: An electrically insulating, organic layer (for example an epoxy), is screen printed on top of the conductor pattern, with openings for the solder lands and hole pads for the component holes.

7. Curing of the solder resist, in heat or in UV light, to evaporate the solvents and increase the resistance to chemicals and thermal and electrical stress.

8. Cleaning of the copper solder areas: At this stage of the process, the copper is oxidised, and the panel is exposed to a mild micro etch with subsequent cleaning, to get good solderability.

9. Deposition of solder coating: To avoid oxidation of the copper and to protect the solderability during storage, a thin solderable layer (about 1 μm thick) of organic material is often deposited by dipping or by roller coating.

10. Punching of holes and edge contour, or drilling/milling: Paper/phenolic and certain other materials can be punched, which is the most efficient method at high production volumes. Glass/epoxy will quickly damage the punching tool, therefore holes are instead drilled and the edge contour is milled by numerically controlled drilling and milling machines.

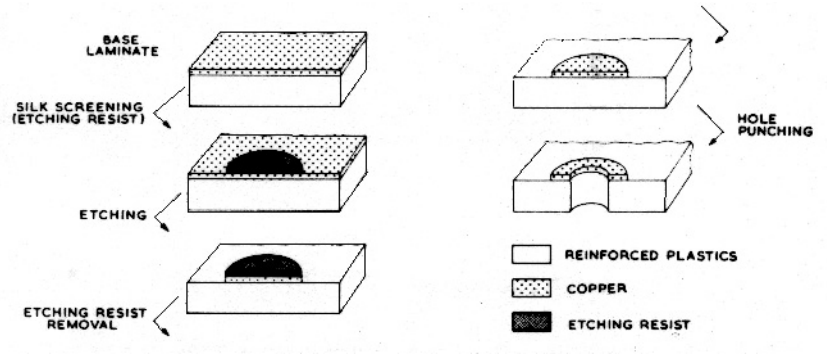


Fig. 5.4: Process steps of "print and etch" process.

This is a subtractive process. That means that the conductor pattern on the boards is defined by removing material (etching of the copper). Additive processing, where one builds up the conductor pattern, is described in Section 5.8.

There are several modifications of this process, such as the following in step 3: To fabricate narrow and complex conductor patterns the pattern is defined photographically (please refer to Section 3.4), instead of screen printing. A photo sensitive dry film resist is laminated on to the panel. It is negative, meaning that after illumination the non-illuminated parts of the resist are removed. The panel is illuminated through a negative film, meaning that the conductor pattern on the film is transparent, while the rest is black. The dry film remaining after development serves as an etch mask.

A third alternative for etch resist is to use plated metal instead of organic material, and in this case tin/lead is selectively plated. The process is described in Section 5.6.

5.6 DOUBLE SIDED THROUGH HOLE PLATED BOARDS

Double sided, through hole plated wiring boards are the most common used type for industrial electronics. They are normally made from glass/epoxy. A key factor is that we have conducting connections from one side to the other side of the board through via holes. Many different versions of the process are available to make such boards. Here we will describe two of them: Panel plating and pattern plating. (A thorough description is given in [5.1, 5.3, 5.21]).

5.6.1 Process

We start with a glass/epoxy laminate with double sided Cu foil, normally 18 μm thick. The process for panel plating is as follows, please refer to Figure 5.5:

1. Drilling of registration holes, component holes and via holes.

2. Cleaning of the surface and holes ("deburring"), and a mild etch to ensure adhesion in the subsequent steps 3 and 4.

3. Activation for chemical plating: The panel is dipped into a solution containing Sn^{2+} ions, to increase the sensitivity of the surface. The Sn^{2+} ions are adsorbed on the surface. The activation takes place in an acidic solution of palladium chloride, that is transformed into metallic Pd. Reaction:

   $$Sn^{2+} + Pd^{2+} \rightarrow Sn^{4+} + Pd.$$

   In the plating process, Pd catalyses the deposition of copper. (There is still some doubt about the detailed mechanism, see [5.2]).

4. Chemical plating [5.1, 5.2] of Cu: The panel is dipped into a reducing bath containing Cu^{2+} ions for example in the form of dissolved $CuSO_4$. Formaldehyde, HCHO, is the common means of reduction. In this bath, Cu^{2+} is reduced to Cu that covers the whole surface, including the holes, also where the surface is electrically insulating. At the same time formaldehyde is oxidised into acetic acid.

   The plated thickness is approximately 3 μm. The purpose is to create an electrically conducting surface everywhere, for the subsequent step.

   The chemical plating is very critical. The composition of the bath is complex, and if the composition, temperature, "bath loading" (the ratio between plated area and bath volume) is outside acceptable values, Cu^{2+} may be reduced to metallic Cu in the bath itself, which is then ruined.

5. Electrolytic plating of Cu: The panel is dipped into an electrolyte that contains Cu^{2+} ions, such as $CuSO_4$ dissolved in H_2SO_4. The panel forms the negative electrode (cathode), and a metallic copper plate forms the positive electrode (anode) of an electrolytic cell. At the anode copper is dissolved:

   $$Cu \rightarrow Cu^{2+} + 2e^-.$$

   The reaction at the cathode is the following:

   $$Cu^{2+} + 2e^- \rightarrow Cu,$$

thus, metallic copper is deposited on the panel. Approximately 25 – 30 μm Cu is normally plated, in order to get good coverage in the via holes.

6. Pattern definition: Dry film photoresist is laminated on to both sides, normally negative resist. The resist is illuminated through a positive photographic mask and is developed. The pattern is therefore black on the photomask, and the photoresist will dissolve where there is a pattern, during the development.

7. Tin/lead plating for etch masking: The panel is connected to the cathode of an electrolytic bath containing Sn^{2+} and Pb^{2+} ions. The anode is metallic Sn/Pb alloy. The electrolyte is based on fluoroboric acid, HBF_4. The ratio between the concentration of the ions in the bath and on the anode, is such that the deposited layer of metal on the panel will be approximately the eutectic mixture 63Sn/37Pb (percent by weight). The normal thickness is about 7 μm. After this the photoresist is dissolved in a suitable solvent, for instance methylene chloride.

8. Etching: The Cu foil is etched simultaneously on both sides, analogous to step 4, Section 5.5, but with an ammonia-based etch bath, which does not attack Sn/Pb. The plated Sn/Pb serves as an etch resist. After the etching, the Cu is covered with Sn/Pb where we want conductor pattern and solder lands, as well as in the holes through the board.

9. If it is desired to have Sn/Pb on the completed board, a "fusing" step follows. It consists in heating of the board to a temperature where the alloy melts and changes its crystalline structure. It flows and covers the nearly vertical edges of the etched copper. We get an intermetallic copper/tin interfacing layer. The heating may take place in hot air or oil, by IR radiation heating, etc.

The tin/lead layer serves two purposes: It is both an etch mask and it makes a durable, solderable surface.

If one wishes clean copper surface on the completed boards, a new etching step replaces step 9. In this step the Sn/Pb is removed.

Finally, organic solder resist is deposited, as described in steps 6-7 in Section 5.5. For boards with pure copper surface, a solder coating may also be deposited.

In a slightly different process, pattern plating, the pattern is defined with photoresist after drilling of the holes and activation, step 3, see Figure 5.5. The copper is then plated only at the desired conductor pattern and in the holes. Then tin/lead is deposited and the photoresist is stripped. The copper is etched, but in this process it is only the original thickness (17 μm) which has to be etched away. In this way, waste is reduced and improving pattern definition is obtained by reduced underetch (Section 5.8.1). This process dominates today.

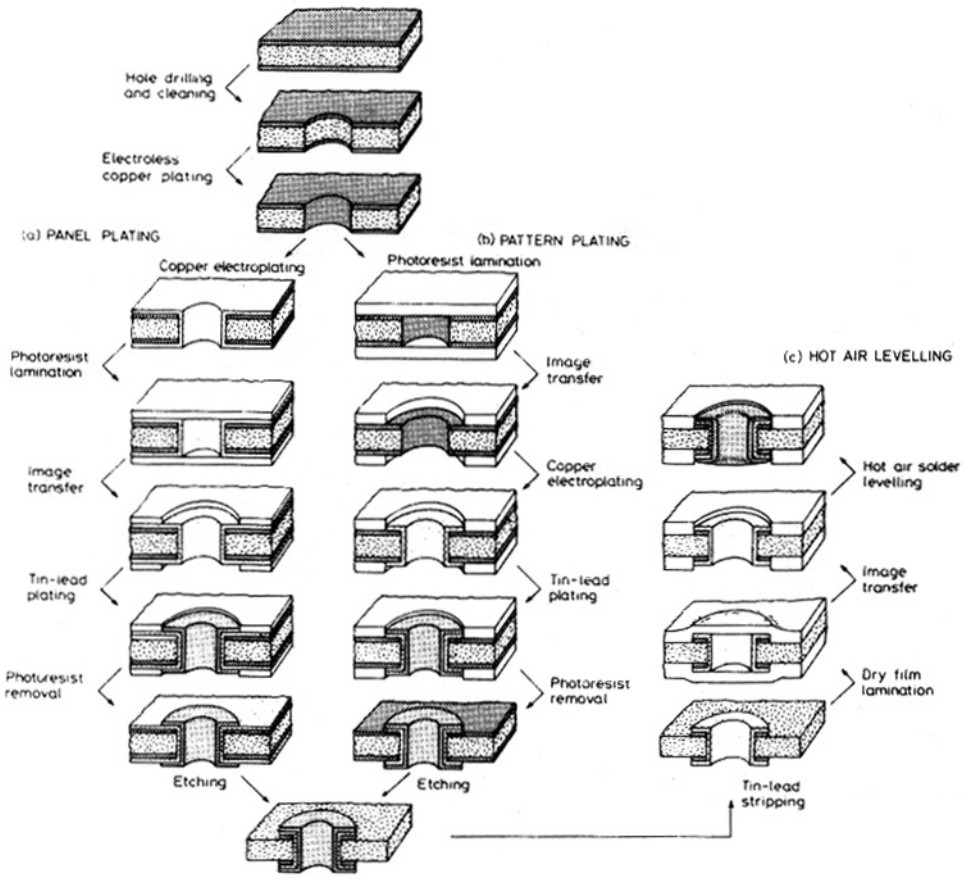


Fig. 5.5: Through hole plated PWB, process steps: a) panel plating, b) pattern plating, c) hot air levelling.

5.6.2 Choice of surface metallisation and solder resist

A tin/lead layer on the surface will react with the copper underneath, during long time storage before component mounting and soldering. An intermetallic compound is created, which is not solderable. If this has occureded, the wiring boards must be discarded. It is customary to allow a maximum storage time of one year, which is rarely a limitation nowadays, since all storage is attempted to be reduced to a few days. (The storage time may still be of importance for spare boards for repair.)

A drawback of greater practical importance shows up after assembly and soldering of the components: All the tin/lead layer melts during the soldering process, even that which is on the conductors underneath the solder resist. At extended conductor areas for ground planes and wide, high current conductors, the solder metal is re-distributed and it will create big wrinkles, drops and "bags". This is normally not acceptable for aestetic reasons. Another potential problem arises when conductors are located close to one another. Between the neighbouring conductors, there may be small openings underneath the solder resist, and the tin/lead may create short circuits when it melts. For this reason, a bare Cu surface underneath the solder resist is required in many cases.

Bare Cu on the solder areas has another handicap: It will oxidise and give a reduced solderability. Particularly for surface mounting of components with small/narrow component terminals, the demands for good solderability are very rigid.

In addition to the two main types of surface, tin/lead all over or bare copper all over, we have a third type with tin/lead deposited only on the component solder pads and in the component holes: Selective tin/lead deposition or "hot air/hot oil levelling", see Figure 5.6. In this process the panels with bare Cu, and solder resist deposited, are dipped in to a bath of molten solder alloy, so that tin/lead wets all copper areas that are exposed. The hot, strong air (or oil) stream blows off superfluous tin/lead on the surface and in the holes, so only a layer 20 - 100 μm remains. Normally this is considered the best type of surface metallisation.

The printing process for solder resist gives relatively poor dimension control, typically 0.3 - 0.5 mm. Often smaller distances than this are needed between the solder lands and electrical insulation on the surface, by high component density and high conductor density. Then an organic, photosensitive solder resist is used which is deposited all over the board area. One type is a relatively thick foil (typically 75 μm), that is laminated on the board in vacuum. It is designated dry film. Another type is printed on in liquid form, but also over the whole area. It is called wet film. In both cases the solder resist is exposed through a photographic film to make openings for solder lands, etc. Then it is developed and cured. With such photo-processable solder resist, the distance to the solder lands can easily be reduced to 0.1 - 0.15 mm (see Chapter 6, Figure 6.4). The thick dry film may in certain instances give problems with soldering of SMD components: Instead of getting contact between the terminals and the solder lands and solder paste, the component body may "ride" on the dry film, and the solder metal may melt without soldering the terminals. This can be avoided by a suitable design of the printing stencil for the solder paste, in a way that ensures that the solder paste is deposited with sufficient thickness.

The dry film on the other hand has an advantage: it may cover via holes such that they are plugged ("tenting process"), see Figure 5.6. We avoid then getting solder alloy into the holes during wave soldering, which may create problems. We also get the advantage of "vacuum-tight" holes during testing, when the boards are sucked to the test fixture (see Section 7.6).

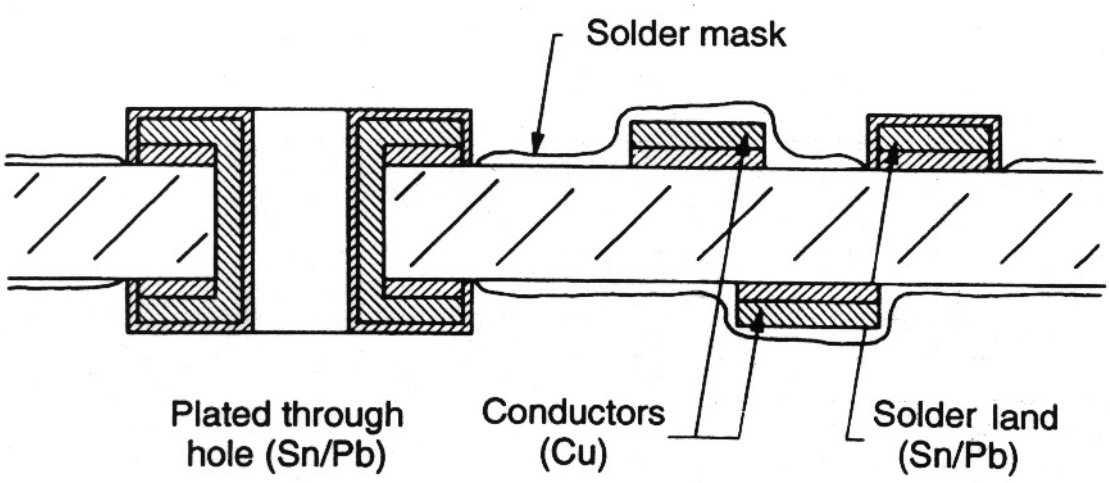


Fig. 5.6.a: Selective Sn/Pb surface coverage with hot air levelling. The alternatives, bare Cu or Sn/Pb on all Cu surface, are shown in Figure 5.2 b).

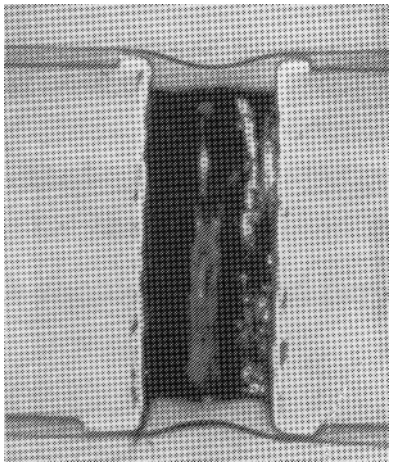


Fig. 5.6.b: "Tenting", i.e. covering of the via holes by dry film solder resist.

5.7 MULTILAYER PRINTED WIRING BOARDS

Multilayer printed wiring boards are laminated together by several double sided boards, inner layer and outer layer, with "prepreg" between. For glass/epoxy based boards the prepreg material is glass fibre impregnated with epoxy, then cured to the B-stage.

The most common types of multilayer boards only have via holes that run all the way through the whole laminate. For a 4-layer board the process is as shown in Figure 5.7:

1. Drilling of registration holes in all layers. Chemical/mechanical rinse.

2. Conductor patterns on the panels with inner layers are defined by photo processing.

3. Conductor patterns on the inner layers are etched, and the panels are rinsed.

4. "Black" or "brown"-oxidation of the Cu-surfaces: These are special oxidation processes in high temperature, which have the purpose of giving a rough surface and improving the adhesion in the lamination process following later.

5. Baking: Heating of the panels to evaporate water and solvents.

6. Lamination: The panels are placed on top of each other with accurate registration by guiding pins in the registration holes, with a single sided panel for outer layer on top and at the bottom, and prepreg between each panel. The stack is pressed together in a lamination press typically at 10 - 25 atmospheres of pressure at 170 °C, for 30 - 90 min. In this process the epoxy softens in the prepreg material, fills all non-uniformities, and polymerises completely to the C-stage.

7. Drilling of via holes through the board for subsequent through hole plating. The drilling process is more critical than for double sided boards, because here we must have electrical contact between the hole plating and the inner layer conductor layers at certain places. Often the epoxy softens and creates an insulating layer on the walls of the holes ("smearing"). To remove this layer, an etch process is used, often plasma etching ("de-smear").

The subsequent processing for pattern definition on the outer layers, through hole plating, etc., is similar to that for double layer through hole plated boards, Section 5.6.

"Buried via holes" are plated holes that connect inner layers, without appearing at the surface, please refer to Figure 5.8 b. Such holes occupy space only on the layers where they have the electrical function to connect neighbouring layers. However, making them require that the inner panels are processed as complete double layer through hole plated boards before the lamination process. The completed boards will be denser, but more expensive. "Blind via holes" connect an outer layer to an inner layer, please refer to Figure 5.8 c). They may be made with precise laser- or regular drilling after the lamination has been carried out, see Figure 5.8 d.

Multilayer boards permit complex interconnection patterns. Normally we put voltage supply and ground on separate inner layers with extra thick Cu foil (typically 70 μm). This way of design gives significantly better noise properties for the completed circuit; both reducing sensitivity to external electromagnetic fields and reducing radiation ("electromagnetic compatibility", EMC). This is of special significance for circuits with high signal frequencies and digital circuits

with short pulse rise- and fall time. For such boards a controlled characteristic impedance is also needed, see below, Sections 5.11 and 6.7.

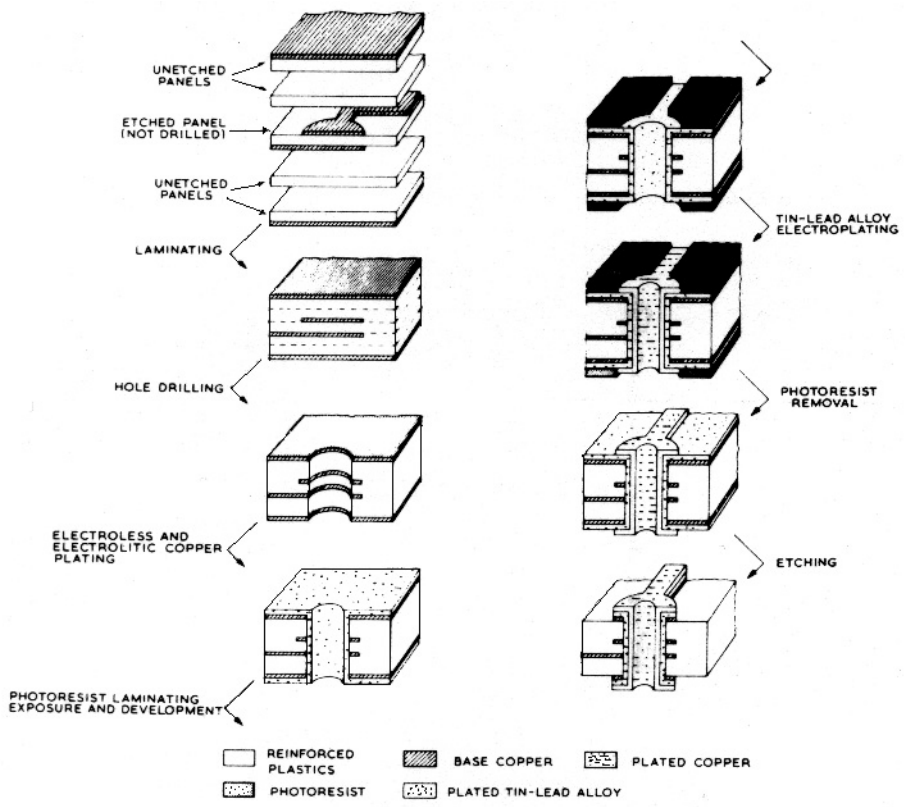


Fig. 5.7: Process steps for multilayer printed wiring boards with holes only through the board.

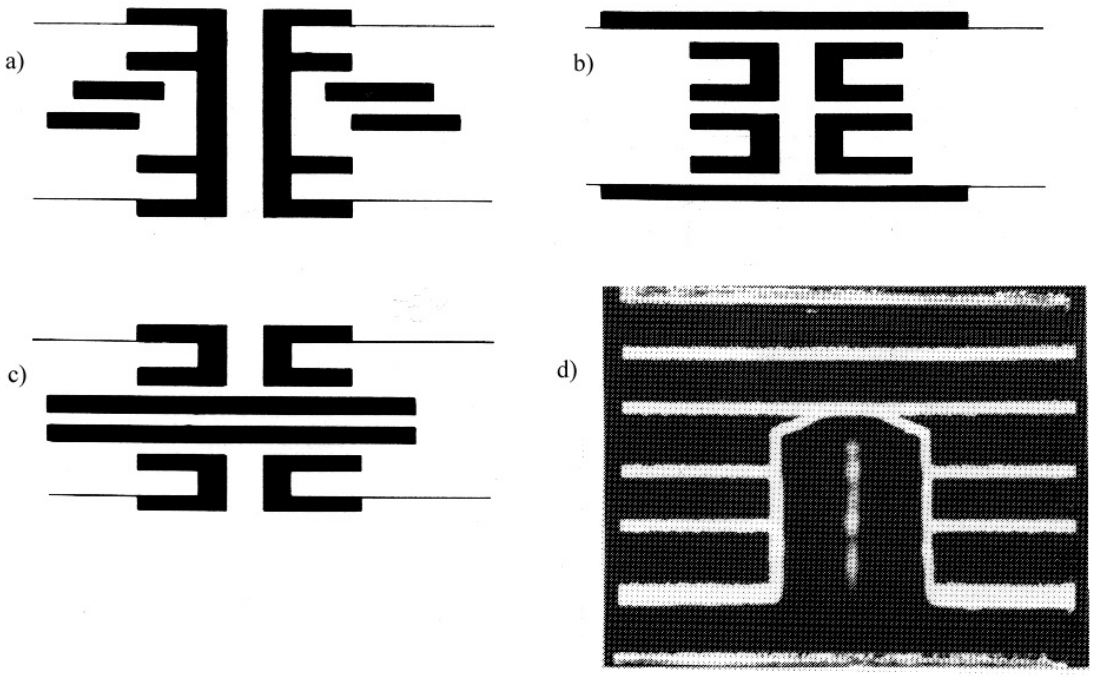


Fig. 5.8: Types of via holes: a) Through hole. b) Buried hole. c) Blind hole. Figure d) shows a microscope section of a drilled blind via. (Contrave´s "Denstrate" process).

Multilayer boards with 12 - 16 layers are quite common, with up to 40 - 50 layers being made. However, the process becomes very costly, and the production yield becomes low, particularly when the conductor widths and the via pads at the same time are small, and the aspect ratio for the via holes (the ratio of hole length to hole diameter) is high.

5.8 FINE LINE WIRING BOARDS, ADDITIVE PROCESS

The demand for high component density and high density of conductors on the printed wiring boards is steadily increasing. While advanced boards in 1965 could be made with 0.3 mm conductor width, today we are below 0.1 mm, see Figure 5.9 a). The limitations are in the etching and other parts of the process.

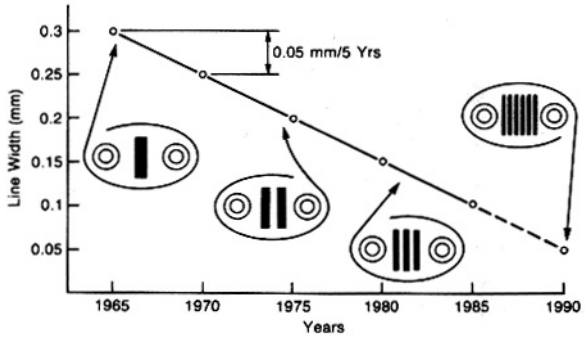


Fig. 5.9 a): The development of minimum line width from 1965 until 1990. The figures in the ovals tell how many conductors can be positioned between the leads of DIP-components with a lead pitch of 0.1" (number of "channels").

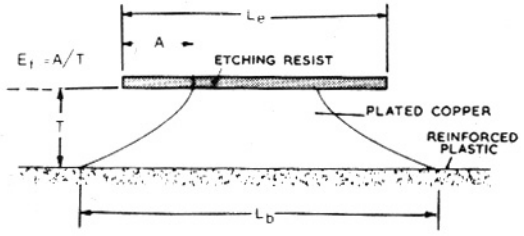


Fig. 5.9 b): Underetch and etch factor.

5.8.1 Limitations in dimension control due to etching

By etching of copper foil we get an undesirable lateral etching at the same time as the etch dissolves copper downwards. This is called underetch, see

Figure 5.9 b). Please refer to also Figure 2.10, Chapter 2. The degree of underetch may be defined by an etch factor E_f:

$E_f = A/T$,

where A = sideways etching and T = the thickness of the copper foil. In practice E_f is between 0.7 and 3, the lower the better. At the bottom the conductor normally becomes wider than the nominal width, $L_b > L_e$.

There is always some uncertainty in the etching speed of the bath. Therefore, we need to use a longer etching time than the ideal time to be sure to etch through the thickness of the foil. This gives an increased underetch. To some extend it can be compensated for by designing the conductors somewhat wider than what we need in the completed wiring board.

Control of the conductor width is important: With too much underetch we get, in the worst case, a discontinuity of the conductor. If the conductor is too narrow, the conductor resistance increases and the maximum current carrying capacity of the conductor is reduced (see Section 6.3). For high frequency circuits with constant characteristic impedance, the conductor width is one of the dimensions that determines the impedance (see Section 6.7). Variations in the conductor width on the wiring board therefore will give variations in impedance and poor high frequency performance of the circuit.

These factors limit how narrow conductors we can make in a subtractive process, particularly when the foil is thick. To make the conductors narrower, the foil that is to be etched must be thinner, or a fully additive technique must be used.

5.8.2 Fine line wiring boards

As the electronics gets more complex, the need for high conductor density increases. By use of smaller conductor widths and distances, we can also manage with fewer conductor layers in a multilayer wiring board. To utilise the space we save, the via holes must also be smaller.

Conductor widths and distances below approximately 150 µm are called "fine line" dimensions, as opposed to the normal 0.2 - 0.4 mm. While normal via holes are 0.5 - 1 mm in diameter (Section 6.3), "mini-via" holes are made with diameter down to 0.3 mm and below. They may also be made without the Cu pad around them, to save even more space.

Fine line processing uses Cu foil with thickness down to 5 - 10 µm, to reduce the underetch. Careful process control and extreme cleanliness are needed, including an accurate control of temperature and humidity to avoid uncontrolled thermal expansion during the processing [5.5]. High precision films for patterning are needed, and the illumination must be done with collimated light under clean-room conditions, see Figure 5.10. Alternatively, the photoresist is illuminated on each laminate directly with a controlled laser, without use of a photo mask.

The production yield becomes lower the smaller the line widths are. The practical limit today is 75 - 100 μm, without resorting to more untraditional processes. Holes down to 0.2 mm diameter have been used in Japan.

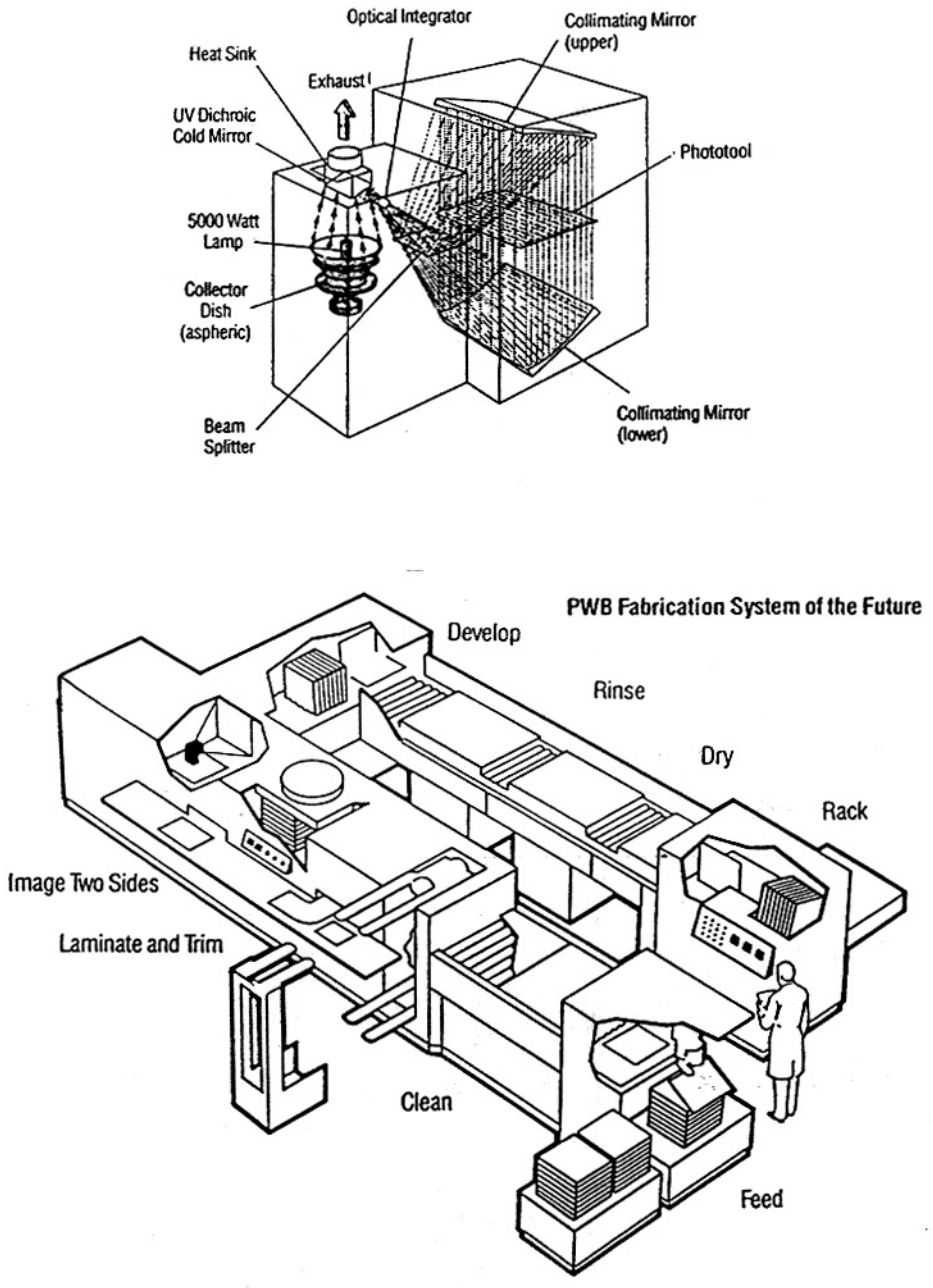


Fig. 5.10: Top: Machine for double sided illumination with parallel light, for pattern transfer from photographic film for fine line printed wiring boards. Bottom: Automatic in-line system for lamination of photoresist, illumination and development, in an enclosed clean room atmosphere [5.5 b].

5.8.3 Additive process

The conductor pattern is defined by etching in subtractive process, as discussed above. The plating is an additive process, meaning that material is built up. The procedure described in Section 5.6 is a combination of the two.

It is also possible to generate conductor pattern in a completely additive processing [5.1, 5.2]. In this case we start with a bare laminate, without Cu foil on top of it. Cu is deposited selectively, only where we need wiring pattern. To achieve this, chemical plating must be used throughout, because we can not obtain external electric contact to all leads as required for electrolytic plating.

The advantages of additive processing are:
- Finer patterns (smaller conductor widths and distances) are obtainable, because we have no underetch.
- There will be less waste of raw materials (copper, etching chemicals), and less environmental problems.

The disadvantages are:
- The processing is slow, more complex and more costly.
- Proper adhesion between Cu and the laminate may be difficult to achieve.

To achieve good adhesion small quantities of metal salts and oxides are added in the base laminate to catalyse the plating process. Alternatively, one can deposit a layer of a special coating on the surface, or treat the laminate chemically to roughen the surface.

The main steps in such a process are, see Figure 5.11:

1. Drilling of holes.

2. Surface treatment: etch in H_2SO_4 or similar.

3. Activation for chemical plating.

4. Pattern definition: Photoresist application, exposure through photo mask, developing.

5. Chemical plating: The plating is selective, on the activated surfaces that are not covered by photoresist.

6. Stripping of the photo resist.

7. Printing of solder resist. (Alternatively: Use of photo-processed solder resist).

As previously mentioned the chemical plating is a sensitive and slow process. The "semi-additive" process is somewhat less sensitive. Here the chemical plating (approximately 5 μm) is done uniformly over the area before step 4, and electrolytic plating is used in step 5. After step 6 approximately 5 μm are etched from the whole surface, so that we end up with Cu only on the desired pattern.

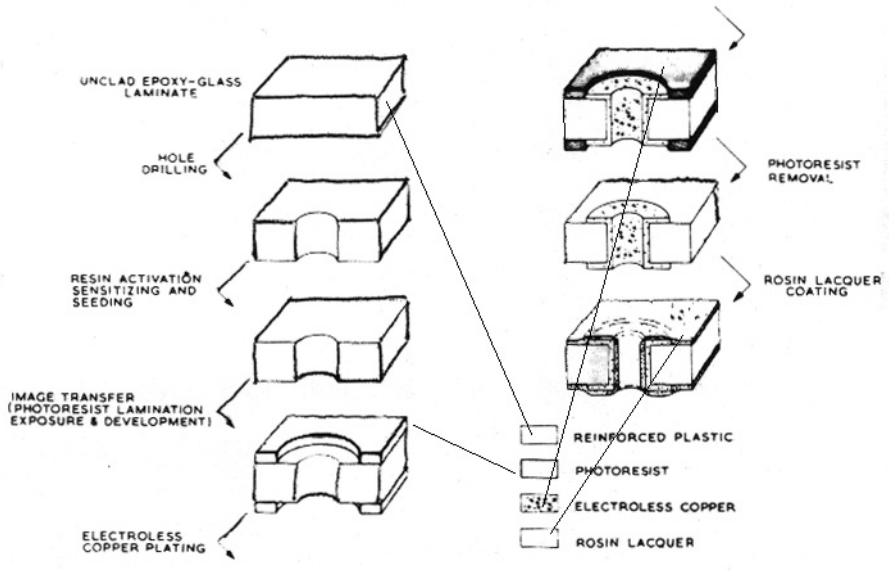


Fig. 5.11: Additive process: process steps.

5.9 METAL CORE BOARDS

For surface mounted printed circuit boards with large leadless chip carrier packages we need thermal compatibility, meaning nearly the same thermal coefficient of expansion (TCE) for substrate and component. This can be obtained by one or two metal cores in the wiring board, composed of a combination of metals with low TCE: "metal core boards", see Figures. 5.2 d) and 5.12 a) - b). The most common metal core combination is a copper/Invar/copper structure, (copper clad Invar) for example 12.5/75/12.5 % thickness ratio, see Figure 5.12 b). Invar has TCE 1.7 ppm/°C [5.3], which is lower than ceramic. By choosing the thickness of each layer of the laminate correctly, one may "design in" the desired TCE for the complete wiring board. If a thick core is used, the expansion of this core will determine the expansion of the whole wiring board. If not, we also have to take into consideration the glass/epoxy and the Cu foil in the other layers. Due to the temperature variation of the properties of the materials and due to standardisation of the thicknesses available, the match will not be ideal [5.6], but it will be good enough even for very demanding requirements. More details about thermal design will be discussed in Section 6.6.

Another advantage of the metal core board is that the thick metal gives excellent thermal conductivity and effectively spreads the heat away from components with high power dissipation. The boards will however be much more costly than ordinary FR-4 boards (typically 4 - 5 times price difference).

The production of metal core boards is similar to that of ordinary multilayer boards. The holes in the core may be drilled or etched before the core is laminated together with the other layers.

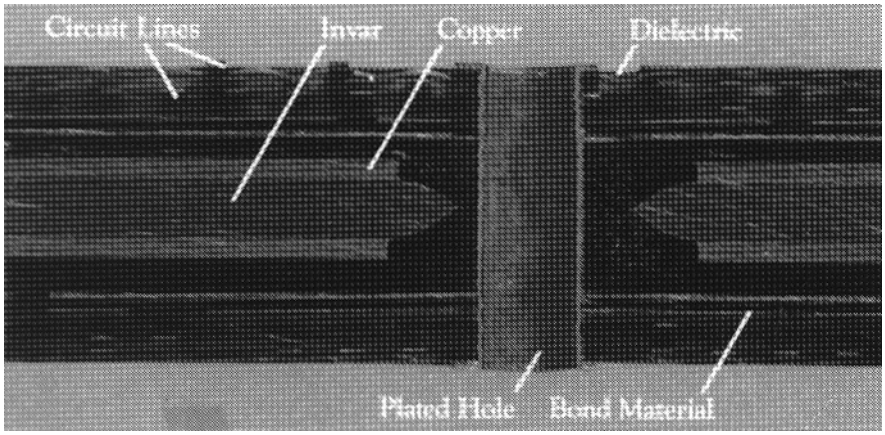


Fig. 5.12 a): Cross section of metal core board with one Cu/Invar/Cu core (Texas instruments).

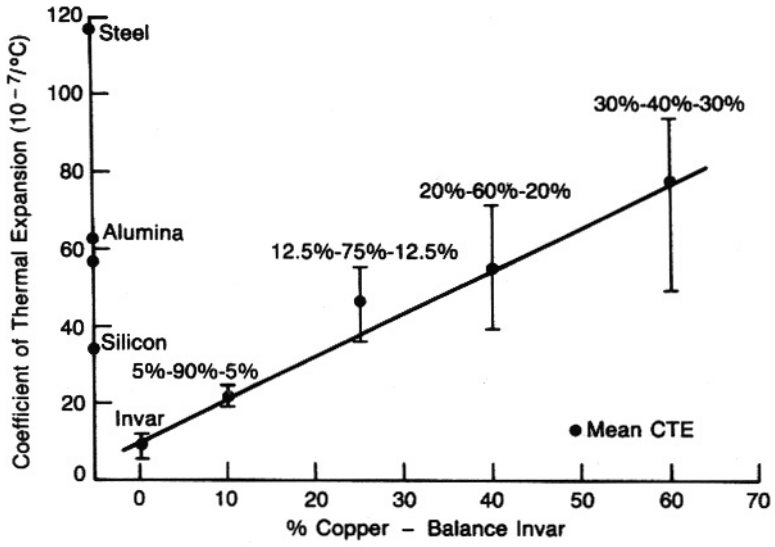


Fig. 5.12 b): Thermal coefficient of expansion of Cu/Invar/Cu, as function of the composition (Texas instruments).

Many other materials have been used for making surface mounted circuit boards with adjusted thermal coefficient of expansion and better properties at high temperature than glass/epoxy: Kevlar/epoxy, kevlar/polyimide, quartz/polyimide, metal core boards with molybdenum, tungsten, etc. instead of Invar. There are positive and negative properties to be found in each of them and have not found very broad use as of today [5.4].

For power electronics that dissipate very high power but are normally simple in their circuit function, a thick aluminium core, insulated with an anodic aluminium oxide layer and a layer of epoxy is often used, please refer to Chapter 8.

5.10 NEW MATERIALS FOR DEMANDING WIRING BOARDS

When thermosetting polymer materials are heated to temperatures above their glass transition temperature T_g, non-reversible material changes occur after a short time (see Section 3.3), which may damage the materials and the wiring boards. The thermal coefficient of expansion is drastically changing when T_g is past, see Figures 3.7 and 5.12. At the same time the polymer softens.

Epoxy with fibreglass reinforcement in the x-y direction is anisotropic, see Figure 5.13. The thermal coefficient of expansion, $\alpha_{FR\text{-}4}$ in the x-y direction is a weighted average of the value for glass fibre (α_{gf} = 3 - 5 ppm/°C), and epoxy. Below Tg (≅ 120 °C) the expansion coefficient of the epoxy is α_{ep} ≅ 40 - 60 ppm/°C, and $\alpha_{FR\text{-}4}$ ≅ 12 ppm/°C (slightly different in the x and the y direction due to the direction of the weaving of the fibreglass). In the z-direction, the coefficient of expansion generally is determined by the epoxy, because the glass fibre does not limit expansion of the epoxy in the z-direction.

When T_g is exceeded, α_{gf} will dominate strongly in the x-y direction, because the epoxy is soft, and $\alpha_{FR\text{-}4}$ is reduced, see Figure 5.13 a. In the z-direction, however, $\alpha_{FR\text{-}4}$ will increase correspondingly as for the epoxy alone, see Figure 5.13 b.

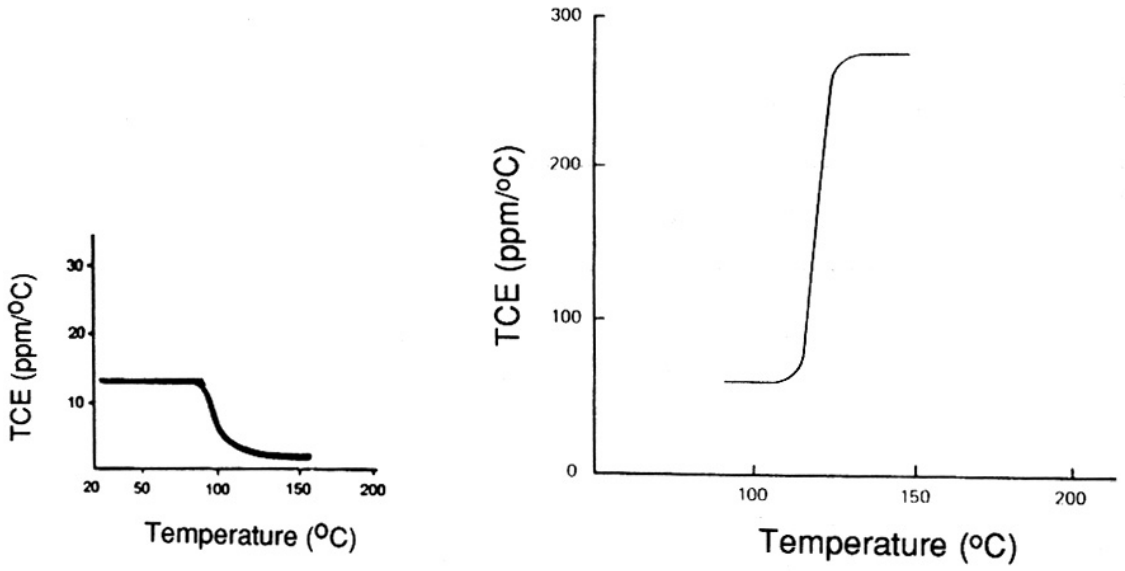


Fig. 5.13: TCE for FR-4 below and above T_g in a): the x or y direction, b): the z-direction [5.2].

The large expansion in the z-direction may cause fracture of the copper plating in the via holes during the soldering process and during high temperature use, as copper has a TCE that is only 17 ppm/°C. Alternatively there may be latent damage in the plastic with warpage, bowing and dimensional changes. This is most harmful when the board has large SMD components with rigid demands on planarity (Chapter 9).

These problems are more pronounced at lower T_g and have excluded paper/phenol laminates for other than cheap consumer electronics. Improved types of epoxy have been developed with higher T_g and better dimensional stability. Among them are "multifunctional epoxy", "tetrafunctional epoxy", and the combination bismaldeimide triazin (BT)/epoxy [5.7, 5.3]. Table 5.2 shows some important properties for these materials and other high performance materials that are discussed in the next paragraph. The TCE for some materials was shown in Figure 3.7 b).

Table 5.2: Material parameters for polymers for printed wiring boards [5.7, 5.3]

Material	ε_r	Tan δ (at 1 MHz)	α ($T < T_g$) [ppm/ ^oC]	T_g [^oC]
Paper/phenolic	4.7	0.025		95
Bisphenol epoxy (FR-4)	4.3 - 5	0.02	33 -60	130
Multifunctional epoxy	4.3 -4.5	0.02	140	145 - 180
Tetrafunctional epoxy	4.3 -4.6	0.02	55	> 150
BT/epoxy	3.5 - 4.2	0.012	100	185 - 225
Cyanate ester	2.8 - 3.6	.002 - .005	50 -100	250 -290
Polyimide (Pi)	3.0 - 4.6	.002 - .01	35 - 80	230 - 315
PTFE (Teflon)	2.1	.001	70 - 120	250 *)

*) Melts, no regular glass-transition

5.11 WIRING BOARDS FOR HIGH FREQUENCIES

5.11.1 Demands on high frequency circuit boards

The developments in monolithic IC technology give possibilities of circuits that operate at steadily higher frequencies. The clock frequencies for microprocessors, signal processors and custom designed circuits increase to 50, 100 MHz and even higher frequencies. The bandwidth in electronics must be significantly higher, to maintain short rise- and fall times. For radio- and microwave circuits, the frequency is up to 10 GHz and above.

This poses new demands on the substrate. It often needs to have:
- Controlled characteristic impedance
- Multilayer structure
- Low relative dielectric constant
- Low dielectric losses

In addition, we have other requirements, applying also to boards for low frequency circuits:
- High thermal conductivity
- Thermal compatibility to ceramic components
- Fine line dimensions
- Simple processing
- Low price

The demands mentioned in Section 5.2 are equally important.

Which factors are most important depends on the application but today's standard material, glass/epoxy (FR-4), and today's standard processes and structures do not suffice [5.9]. In this section, we will discuss some of the important properties, and some types of high performance wiring boards that are commercially available.

5.11.2 Important properties and parameters, new materials

For high frequency use, we need to have a controlled characteristic impedance, Z_0, as mentioned above (see Section 6.7 and [5.24]). This implies that there must be a ground/voltage plane between every signal layer. Conductor widths and thicknesses in the dielectric must be controlled to small tolerances. ε_r must be close to a constant, independent of temperature, moisture content, and frequency.

The dielectric attenuation needs to be low. It is given by (see Section 6.7):

$$\alpha_d = \pi \varepsilon_0^{1/2} \varepsilon_r^{1/2} \tan \delta \, f/c.$$

Here ε_0 is the dielectric constant, ε_r = the relative dielectric constant, tan δ = dielectric loss tangent (please refer to Sections 3.2.3 and 4.3.1), f = frequency, and c is the speed of light.

For the high frequency wiring boards it is therefore important that ε_r of the dielectric is low, as well as the loss tangent, particularly for big wiring boards with long signal paths. Low ε_r also gives the high signal speed, low parasitic capacitance, and less crosstalk. It gives the possibility to use thinner dielectric and achieve higher conductor density [5.8], please refer to Section 6.7.

FR-4 has not got good properties at high frequency, please refer to Table 5.2. The loss tangent is high, furthermore ε_r varies with frequency, please refer to Figure 5.14 so Z_0 becomes frequency dependent [5.9].

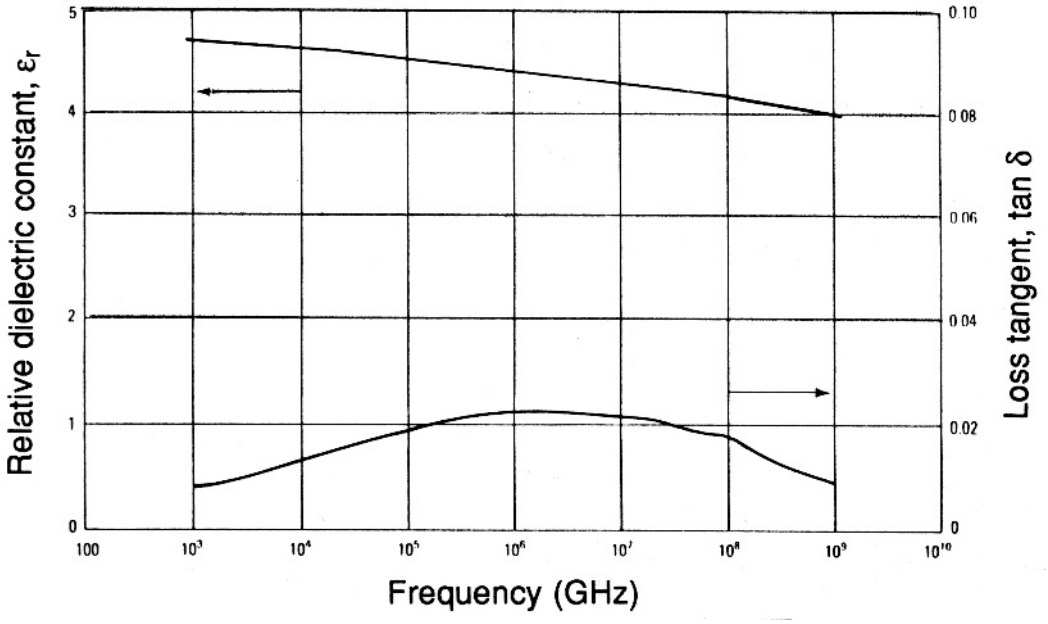


Fig. 5.14: Frequency dependence of ε_r and tan δ for FR-4 [5.9]. Relative dielectric constant, ε_r Loss tangent, tan δ

The "ideal dielectric" is air, with $\varepsilon_r = 1$ and $\tan \delta = 0$. Of the practically useful material PTFE (Polytetrafluorethylene, Teflon) is the closest, see Table 5.2. It can also withstand high temperatures but the material is soft, and it bends easily. It is so chemically inert that it is difficult to process, and Cu conductor foil has poor adhesion to it. With certain additives PTFE has for many years been in use as a microwave "soft substrate", under names such as Duroid from Rogers Corp. Normally there is a ground plane on one side of the soft substrate, and one conductor layer with "microstrip" geometry (please refer to Section 6.7) on the other side. Several types of multilayer circuit boards from several manufacturers are based on PTFE as dielectric, see below.

Various types of polyimide also have low dielectric constant, low loss and high glass transition temperature. Polyimide has been combined with aramid (Kevlar) or quartz fibres instead of glass fibre, to obtain lower loss and lower ε_r but there are problems in machining Kevlar and quartz, making such laminates costly. Polyimide can also be used on substrates of metal, ceramic or silicon without fibre reinforcement. An important handicap of most polyimides is that the materials are hygroscopic and absorb several percent moisture. That may create problems during soldering as well as during operation of the complete product: ε_r will change with the moisture content, and corrosion will increase.

A new class of materials with the potential to be the next generation of standard dielectrics, are cyanate esters [5.3, 5.10, 5.11]. These materials have high T_g, low thermal coefficient of expansion, relative low ε_r and low loss, good adhesion to Cu, and good chemical stability.

5.11.3 Commercial products

Many companies are in the process of introducing new and improved types of laminates/materials on the market. We shall only mention a few examples. Rogers Corp. offers a fluoropolymer composite, structured as shown in Figure 5.15 a). The printed wiring board with RO2800 gives good high frequency properties, Table 5.3. However, it requires non-standard PWB processing [5.8, 5.13]. The surface needs to be treated with the poisonous sodiumnaphtalene to improve the adhesion to Cu, and lamination takes place at 350 °C, (as opposed to 175 °C for glass/epoxy multilayer boards, Section 5.7). Rogers also has one type suitable for flexible boards or cables, RO2500, with similar properties.

Gore Corp. (which also markets Goretex-materials for raincoats, etc.), has developed prepreg materials based on Teflon with air pores. Some properties are shown in Table 5.3. The material may be laminated together with FR-4, as shown in Figure 5.15 b), and gives a combination of conventional processing, yet low effective dielectric constant and low losses in the dielectric between signal conductors and the corresponding ground plane [5.14].

Fortin Industries offer laminates based on cyanate ester, with low ε_r and high T_g, Table 5.3. The processing is similar to that of FR-4.

Table 5.3: Materials parameters for important materials combinations and some commercial products for high performance printed wiring boards.

Material	ε_r	tan δ at 1 MHz)	K [W/m ^oC]	α (T<T_g) x-y (and z) [ppm/^oC]	T_g [^oC]
FR-4	4.6	.02	0.2	12-16	125
				(60)	
PTFE/glass	2.35	.001	0.26	24	250
				(260)	
Pi/glass	4.4 -4.8	.01 -.015	0.35	11-14	220 - 270
				(60)	
Pi/quartz	3.4 - 4	.005	0.13	6-8	270
				(34)	
RO2800	2.8	.0014	0.44	16-19	327*)
				(24)	
RO2500#)	2.5	.0025			
Fortin/CE	2.8-3.6	.003-.009	0.3	ca. 15	110 - 250
				(50-350)	
Gore	2.4 -2.6	.01	ca. 0.2	12	120 -180
				(50)	
Alumina	10	.0001	30	5-7	-

*) Melting point

#) Used for flexible boards and high frequency flat cables.

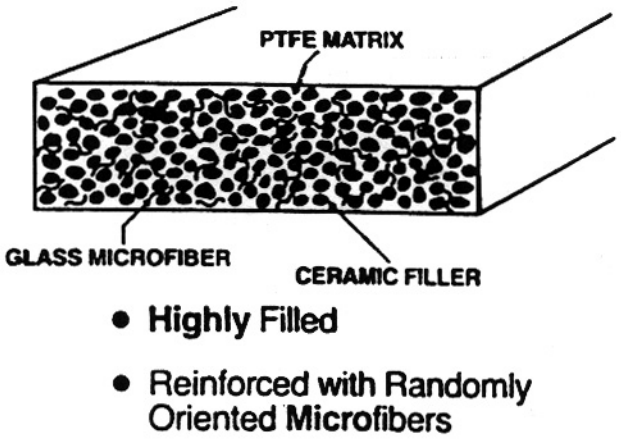


Fig. 5.15 a): Structure of Rogers material RO2800.

Measured attenuation for some new types of high frequency PWB materials are shown in Figure 5.16.

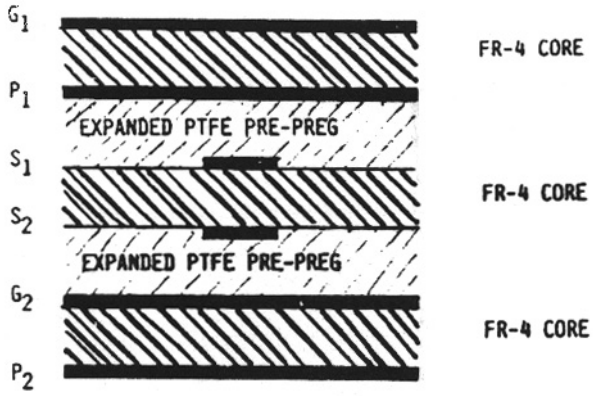


Fig. 5.15 b): Combination of Gore-Ply and FR-4 gives a simple process, and at the same time low dielectric losses and reduced capacitance to ground.

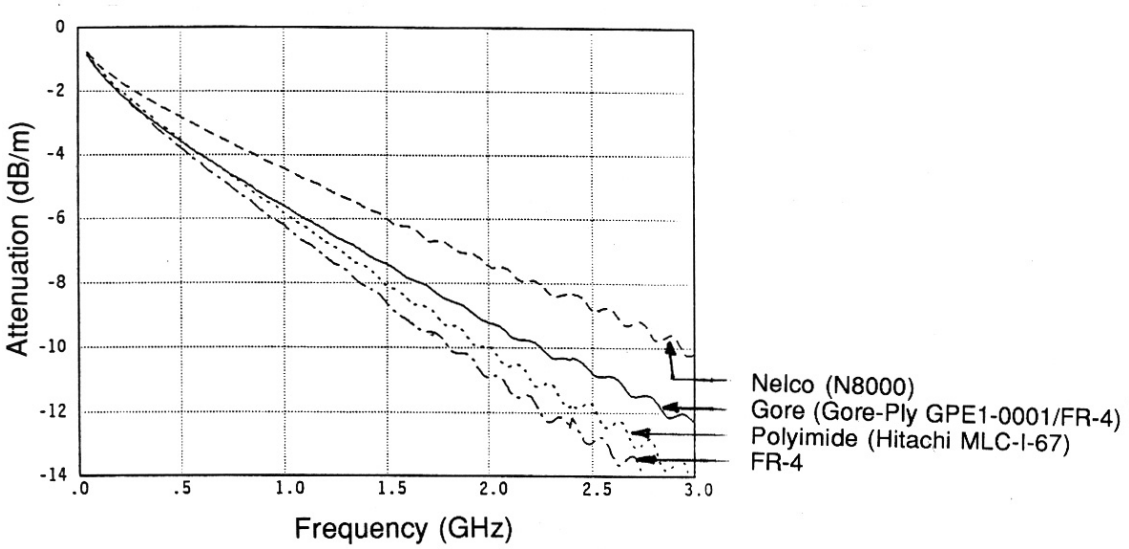


Fig. 5.16: Attenuation in (dB) as function of frequency for a one meter long stripline, for the high performance materials Gore, Nelco and polyimide, compared to FR-4 [5.24].

More complex processes have been tested by Martin Marietta [5.14], Ericsson [5.15] and other companies.

A special process that gives extremely high performance is "Multiwire" and "Microwire" from the US company PCK, see Figure 5.17 [5.16]. A Cu/Invar/Cu core forms the ground plane. The dielectric and a layer of adhesive are laminated on top. Then insulated conductors are placed in the layer of adhesive one by one, with a computer controlled tool, see Figure 5.18. First one conductor layer is placed primarily in the x-direction, then one layer that is primarily along the y-direction. Thereafter a dielectric layer is again deposited, and if necessary, the structure is repeated by a new ground plane and new layers of conductors. On the surface, Cu is plated for solder lands. Contacts between the conductor layers and between conductor and solder lands are obtained by "burning" via holes by laser. The laser evaporates the dielectric and the insulation on the conductors. Subsequently Cu is plated in the via holes to obtain contact. Controlled characteristic impedance and very high conductor density characterise "Microwire", but there are few producers, and the technology is expensive.

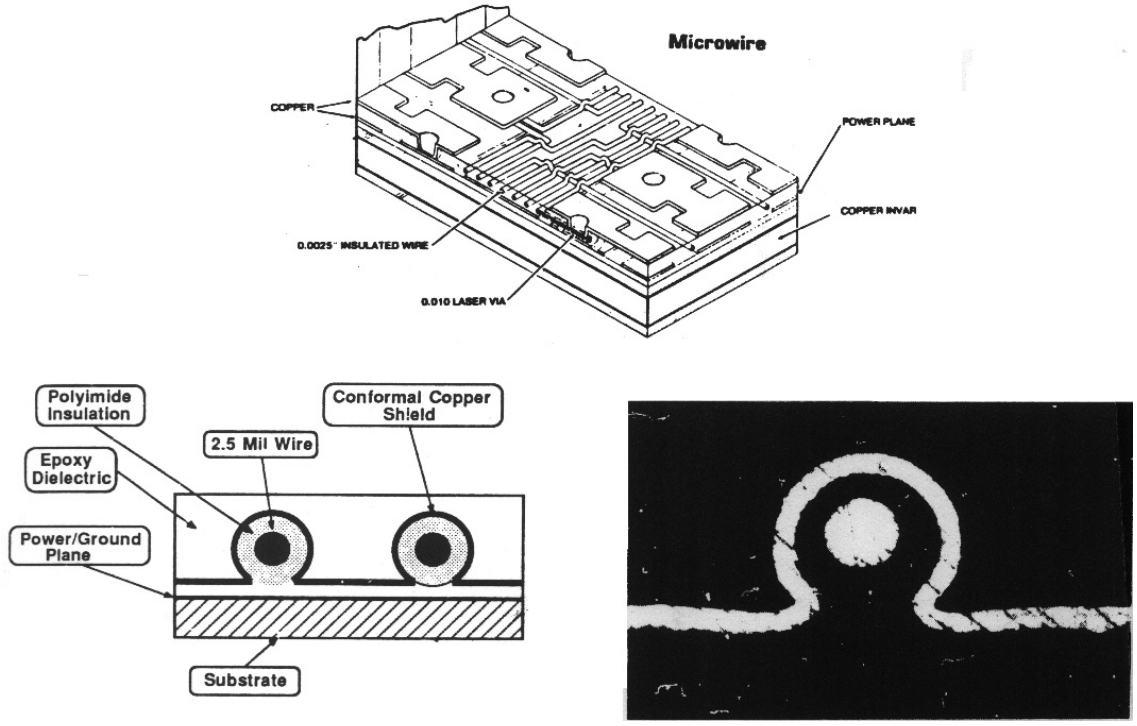


Fig. 5.17: Top: Microwire from PCK, with conductors insulated with organic insulation, and a metal foil as ground plane. Bottom: Next generation technology, where each conductor has its own metal shield [5.16].

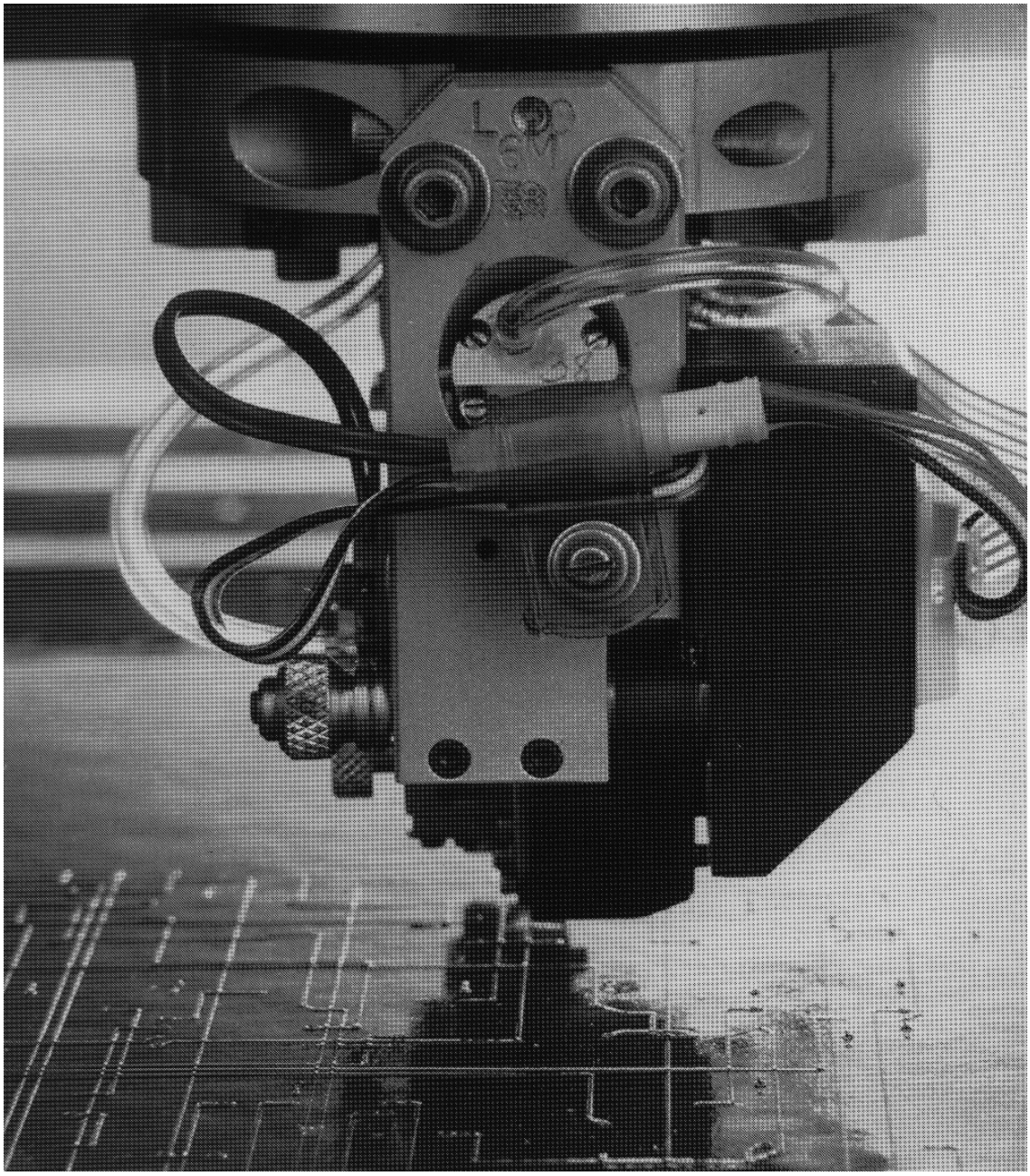


Fig. 5.18: The equipment head that deposits the conductors on the laminate for Microwire.

5.12 FLEXIBLE PRINTED WIRING BOARDS

Flexible wiring boards are used in products that are moveable during use (dynamic): Disk drives for computers, printers, etc., or static, where the board is bent in the right shape and remains in this position during operation. Examples of this are cameras, see Figure 5.19 and other compact products with circuitry

packed into odd-shaped volumes. A special type of flexible boards is the membrane switch panel. Even if membrane switch panels are not carrying components in the normal sense, we shall describe them here.

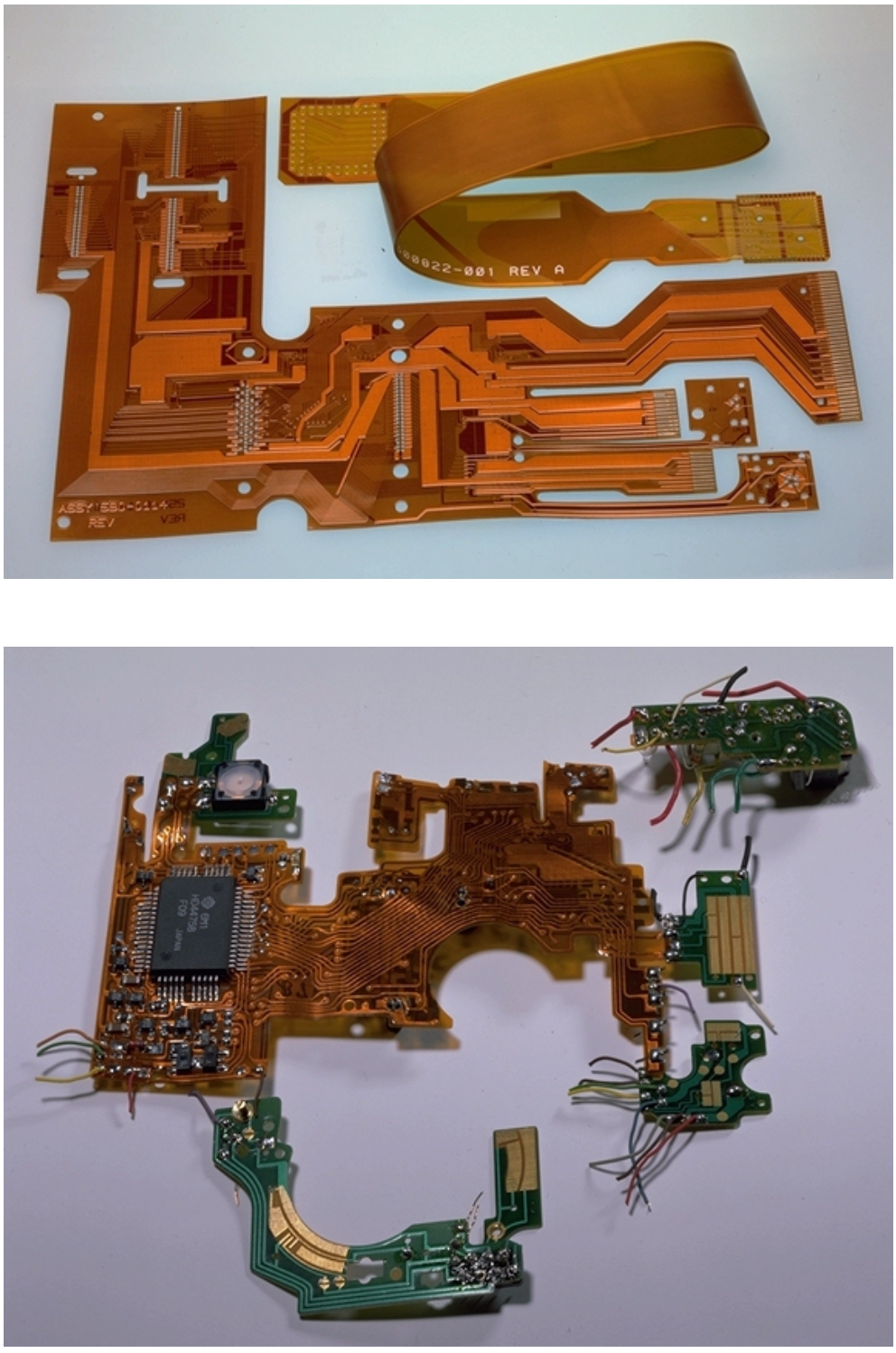


Fig. 5.19: Flexible printed wiring boards. Bottom: Most of the electronics in Minoltas camera Maxxum 9000 is on two flexible printed circuit boards.

Flexible PWBs are made primarily from polyester and polyimide (specially known under DuPont´s trademark Kapton). Thin glass/epoxy is also used to some extent, and PTFE for microwave frequencies. Some characteristic properties are given in Table 5.4. For regular circuits, polyimide is used the most. (Similar polyimide foil is also normally used as the base material of the film for tape automated bonding (TAB), see Chapter 3.) Polyester is particularly used for membrane switch panels.

Table 5.4: Properties for materials used for flexible printed wiring boards. (Data: Schoeller Elektronik).

Typical values	Unit	Glass Epoxy	Polyester base laminate	Polyimide base laminate
Solderability	°C/s	260/10	230/1	260/10
Max. continuous operating temperature	°C	150	110	220
Tensile strength	kp cm^{-2}	1750	1500	1700
Peel strength to copper	kp	4,5	1,8	1,3
Moisture absorption	%	0,5	0,8	2,5
Coefficient of linear expansion	$°C^{-1}$	$1{,}1\ 10^{-5}$	$1{,}5\ 10^{-5}$	$2{,}0\ 10^{-5}$
Etch shrinkage: Machine direction /transverse direction	%	0,2 - 0,8	1,0 - 0,55	0,45 - 0,25
Dielectric constant (60 Hz)		3,4	3,25	3,5
Dissipation factor (1 kHz)		0,037	0,006	0,003
Resistivity	ohm cm	$1{,}6\ 10^{13}$	10^{17}	$4\ 10^{16}$
Cost ratio (laminate only)		1,4/2	1	2/3
Comments		Not suitable for continuous folding use. Max. peel strength to copper and minimum elongation.	Sensitive to solder heat. Lowest cost. Good physical and electrical properties	Non-flammable. Outstanding physical and electrical properties.

The dimensional stability of these materials is not so good as for example in FR-4. This must be considered during the design. High absorption of moisture in polyimide is also of importance.

5.12.1 Regular flexible boards

The thickness of the polyimide layer may be 0.05 - 0.2 mm, and the substrates may have single sided or double sided conductor pattern, possibly with through hole plated via holes. This gives the structures shown in Figure 5.20. Multilayer structures are also made. The combination of flexible parts and rigid parts, "flexi-rigid" is common. The rigid parts may be passive stiffeners without conductor pattern, or they may be laminated together with a flexible part, through hole plated, with components mounted, and become the part of a complex multilayer flexi-rigid structure.

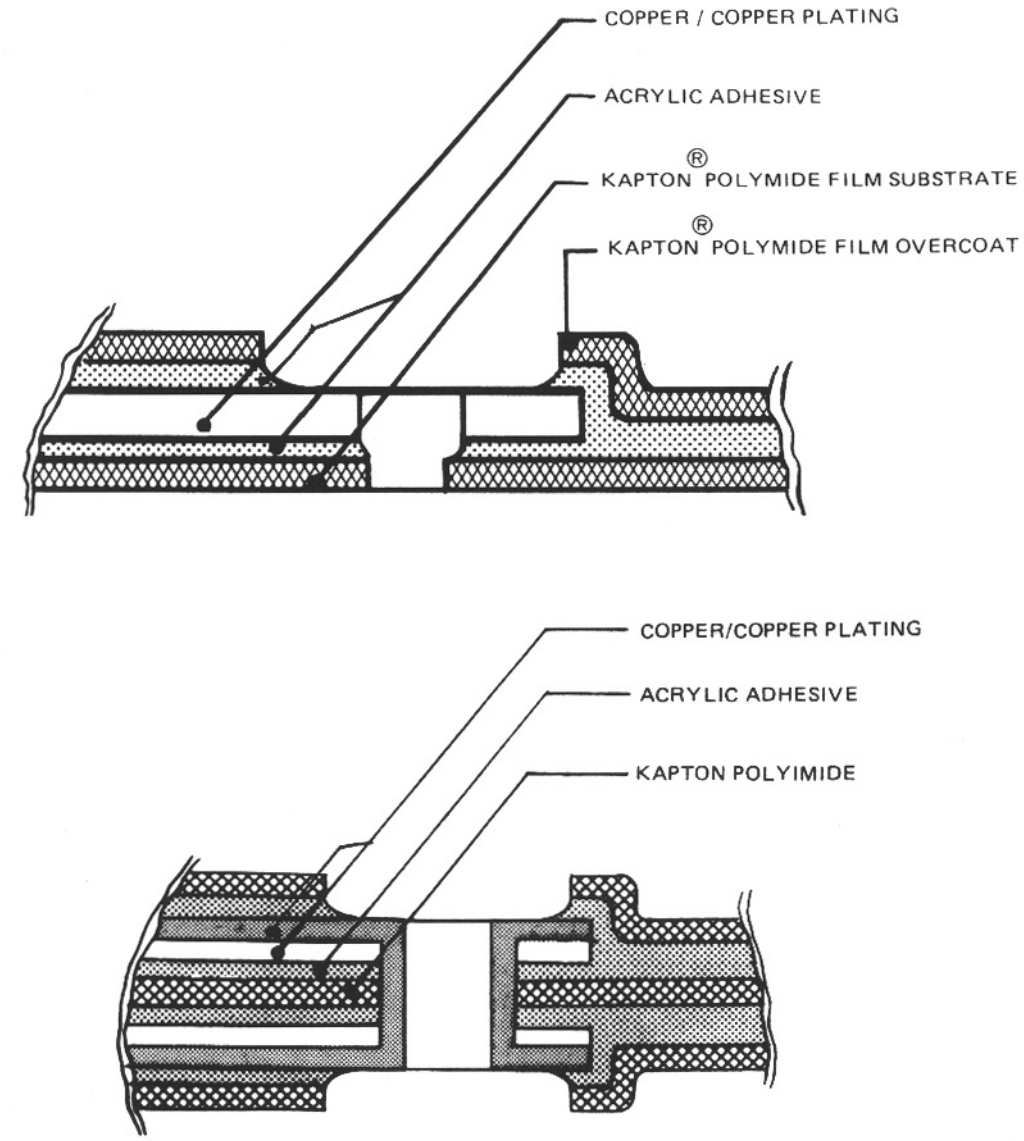


Fig. 5.20: Cross section of flexible PWB: Top: Single layer conductor foil, bottom: Double layer conductors with through hole plating.

The processing of flexible boards is similar to that of rigid boards [5.3, 5.17, and 5.18]. To get the copper foil to adhere, in case of a polyimide based board, an adhesive layer of epoxy or acrylic is used between the polyimide and the copper

foil. A cover layer serving as solder resist is normally laminated on top with a layer of adhesive underneath. Printing, photo processing, plating and etching takes place from roll to roll. That is, the process takes place while the film moves through the machines and the process baths. Holes are punched, and edge contours are punched or cut with a computer controlled knife.

5.12.2 Membrane switch panels

Membrane switch panels are used as replacement for ordinary low current switches or keyboards [5.20]. In addition, they may be shaped as informative and decorative fronts for instruments, consumer products, etc. The structure is shown schematically in Figure 5.21. All the switching elements are defined on plastic foil (normally polyester) by screen printing of the conductor patterns. The two contact points in each switching element are kept apart by a spacer layer. When the contact is pressed, the two parts touch and give a short circuit.

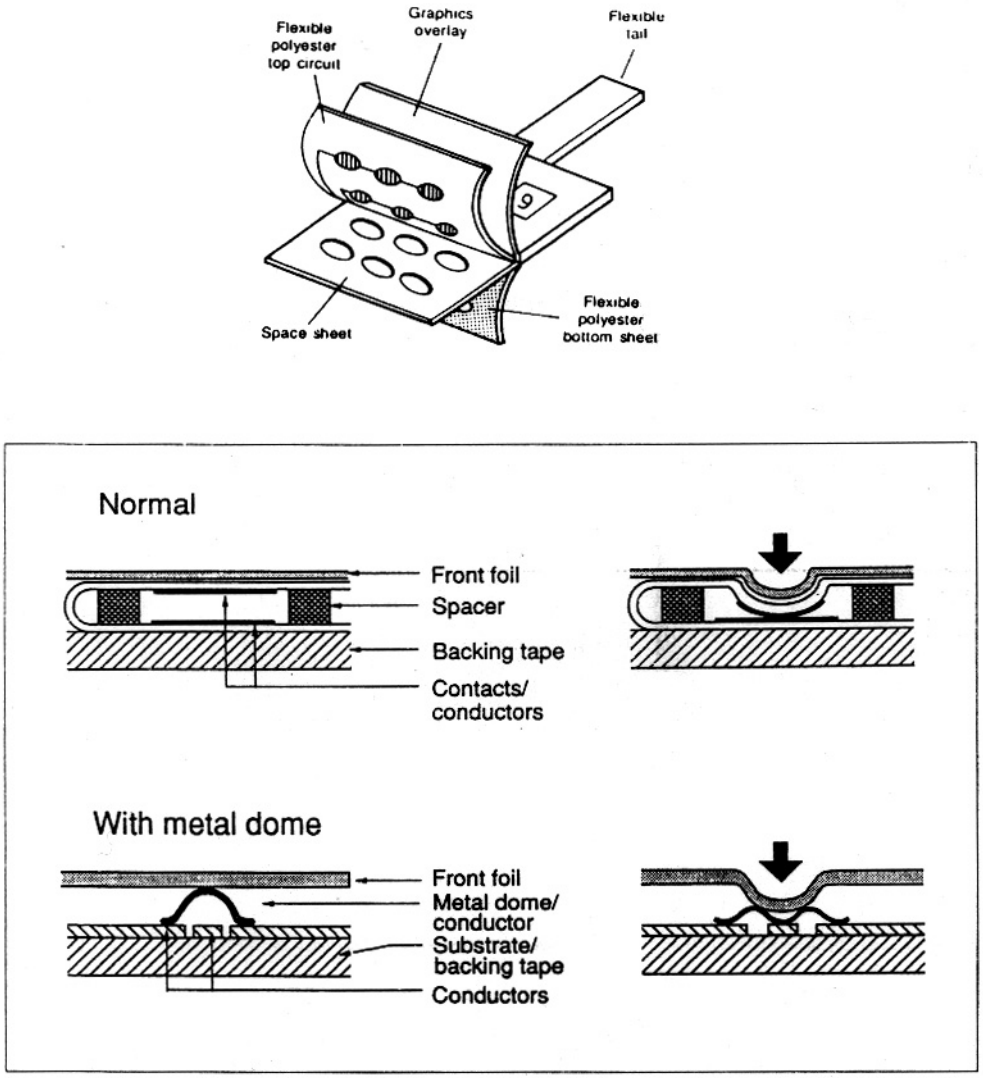


Fig. 5.21 a): Membrane switch panel, schematically. Top: Structure, bottom: Cross section of a normal panel and a panel with metal dome [5.20].

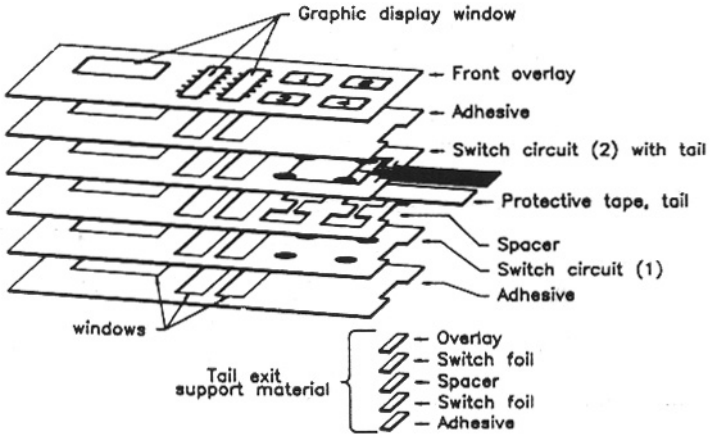


Fig. 5.21 b): Exploded view of simple switch panel [5.20].

The complete panel is composed of 5 - 10 laminated foil layers, Figure 5.21 b), see also Section 6.9 and Figure 6.39.

To obtain a direct "finger feeling" of a closed contact one may use a metal membrane ("dome") as a part of each contact point, see Figure 5.21 a). One may also have transparent areas, with light and information behind, see Figure 6.40.

The production of membrane switch panels is based on screen printing of the pattern and information on the front plate, screen printing of conducting polymer pastes for conductors and switch contact areas (see details in Section 8.3 about polymer thick film technology), punching of contours and lamination of the foil layers with adhesive layers between them. Polyester is used the most for the layers containing the conductor pattern. However, this material can not withstand normal soldering temperatures.

5.13 MOULDED BOARDS IN THREE DIMENSIONS

Printed wiring boards are generally planar and laminated from thin layers of epoxy or other polymers with reinforcement and with Cu foil for conductor layers, as described previously. Mechanical, structural parts holding batteries, electrical components of odd shapes, etc., are made as separate parts that are screwed or glued together. Around the printed circuit board, there is normally a chassis or box of some kind.

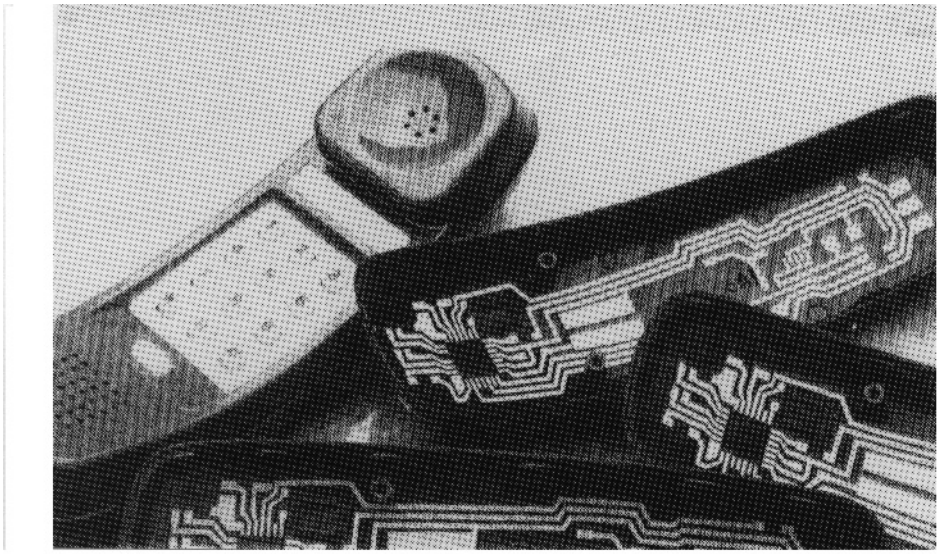
Using suitable materials and technology, it is often possible to combine the wiring board and structural parts in one moulded part, please refer to Figure 5.22 [5.25]. Such substrates may be 3-dimensional, having integrated conductors, and the components mounted directly on them by soldering, gluing or wire bonding. The moulded carrier may also have integrated connectors, knobs, pressure contacts and structures that make automatic component mounting and subsequent assembly particularly simple. The technology for 3-D moulded

boards may simplify the structure and the production of simple electronic circuits substantially.

The plastic materials that are used for this type of substrates are called engineering plastics and they are high quality thermoplastic polymers (i.e. they may be heated repeatedly to over the glass transition temperature (please refer to Section 3.3). This makes it possible to recycle the waste material after the moulding process and avoid material loss that we get by ordinary PWB production. The materials used are polysulphone, polyethersulphone, polyetherimide, and others [5.20], see Tables 3.5 and 5.5. These polymers have high glass transition temperature, high mechanical strength and dimensional stability, they are chemically resistant, and absorb little moisture. However, they have low thermal conductivity and high thermal coefficient of expansion, like other polymers. To improve the thermal conductivity and reduce the thermal expansion it is possible to mix in ceramic particles such as Al_2O_3, AlN, SiC, or use a metal core [5.3].

Table 5.5: Materials used for moulded circuit boards, and their properties, compared to epoxy and polyimide [5.3, page 945].

Polymer types	Epoxy	Polyimide	Poly-sulphone	Polyether-sulphone	Polyether-imide
Manufacturer	3M Co.	E.I.Dupont	Union Carbide	ICI America	G.E.Co
Trade name	Scotchcast 5133	Pyralin	Udel	Victrex	Ultem
Thermal conductivity (W/m°C)	0,40	0,15			0,22
Glass transition temperature [°C]	110-125	260	190	230	215
UL listed temperature [°C]	130	NA	150	180	170
Coeff. of thermal expansion [10^{-7}/°C]	600	200-400	-	-	560
Dielectric const. @1 MHz	6,2	3,50	3,10	3,50	3,15
Dissipation factor @1 MHz	0,02	0,002	0,004	0,006	0,002
Dielectric strength [V/mm]	20000	45000	48000	-	33000



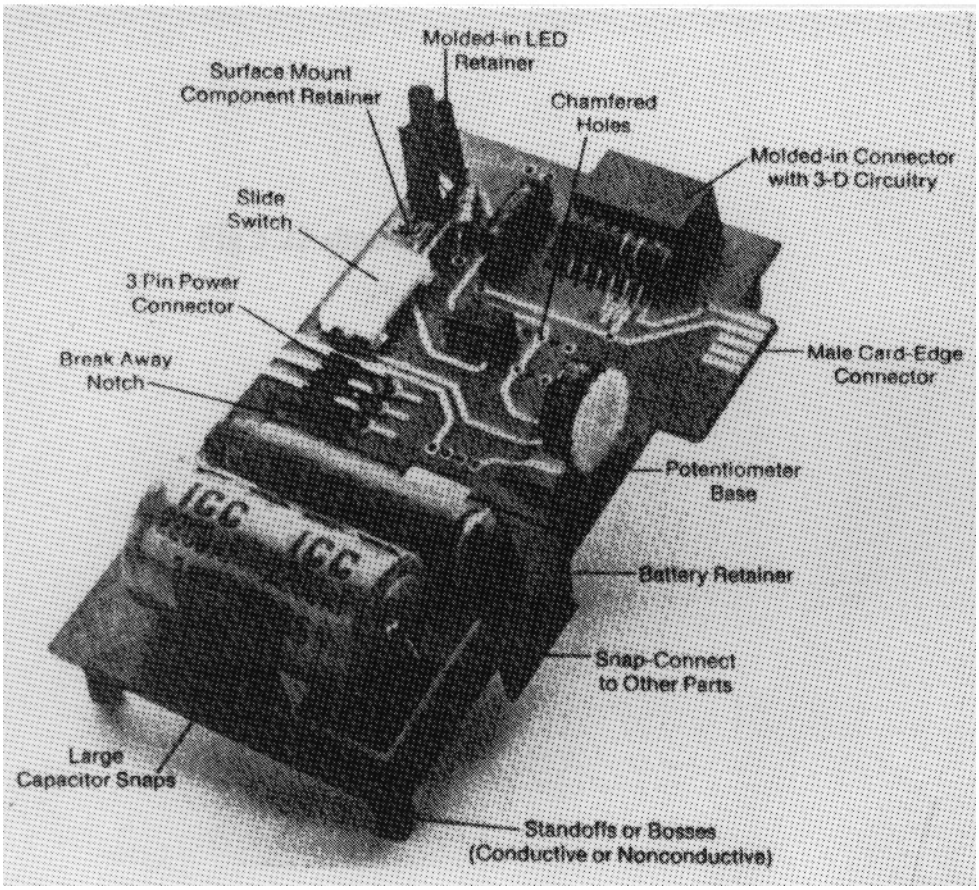


Fig. 5.22: 3 dimensional moulded component carriers, applications [5.23].

The shaping of the plastic is done by injection moulding, analogous to that used for plastic component packages. There are several ways to produce the conductor pattern, such as [5.3, 5.19, and 5.20]:

- Chemical plating (fully additive or semi-additive process), possibly after local photo-sensitising with a guided laser.
- Screen printing of polymer thick film conductors [5.20].
- Special moulding, after deposition of conductor pattern on a temporary foil, please refer to Figure 5.23.

- Two-step moulding process, one with a plastic that is"sensitised" for chemical plating, please refer to Figure 5.24.

The productions of moulding tools and start-up of the process are specific for each product, they take time, and are costly. The technology therefore has little flexibility and is not suitable for changes and modifications. It is suitable for coarse patterns, and simple products in high production volumes. It is believed that 10 - 30 % of electronics will use moulded component substrates some years from now.

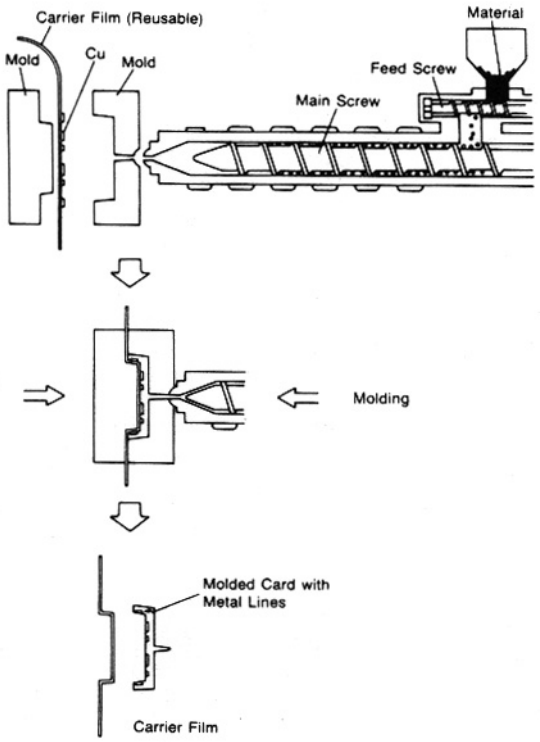


Fig. 5.23: The process for moulding of a 3-dimensional substrate with Cu conductor patterns deposited on a temporary film [5.3].

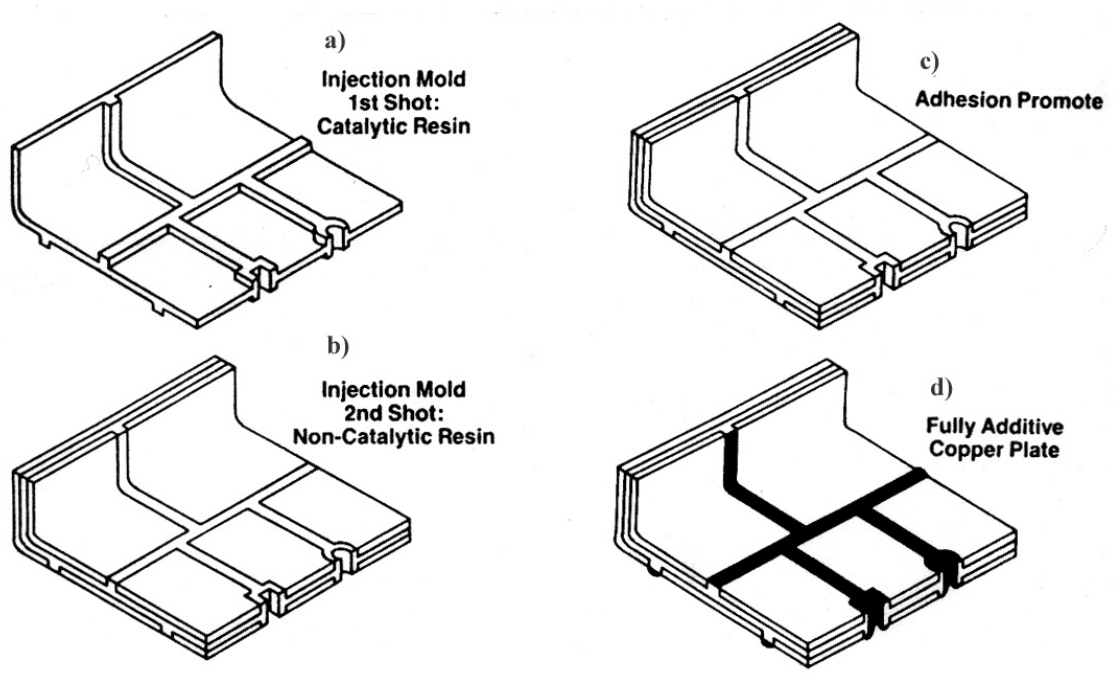


Fig. 5.24: Two steps moulding process for preparation for chemical plating of the conductor pattern on 3-D component substrates. The first moulding is done with a catalytically activated plastic, the second with "passive" plastic, where chemical plating is not sticking. (PCK, USA).

REFERENCES

[5.1] a) G. Leonida: "Handbook of Printed Circuit Design, Manfacture, Components and Assembly". (Electrochemical Publications, 1981).
b) C.F. Coombs: "Printed Circuits Handbook". (3rd Ed., McGraw Hill, 1988.)

[5.2] F.N. Sinnadurai: "Handbook of Microelectronics Packaging and Interconnection Technologies". (Electrochemical Publications, 1985.)

[5.3] R. Tummala and E.J. Rymaszewski: "Microelectronics Packaging Handbook". (van Nostrand, 1989.)

[5.4] IPC-CM-78: "Guidelines for Surface Mounting and Interconnecting Chip Carriers". (IPC 1983).

[5.5] a) S. Spitz: "Fine lines: Tweaking the process or a quantum leap?" Electronic Packaging and Production, Jan. 1989, page 58.
b) J.C. Carroll: "The fine line challenge". PC Fab, June 1989, page 48; L.R. Wallig: "Perspective on cleanrooms". PC Fab, June 1989, page 58.

[5.6] L. Halbo et al.:
a) "Environmental test of SMD PCBs". EPF report R 13, Dec. 1987 (in Norwegian);
b) "Second generation SMD components, PWBs, assembly, soldering". EPF-report R 29, April 1989 (in Norwegian).

[5.7] a) S.L. Spitz: "Specialty Laminates Fill Special Needs". Electronic Packaging and Production, Feb. 1989, page 108.
b) M. Cygon: "High Performance Materials for PCBs". Circuit World vol. 19 No. 1, 1992, p.14.

[5.8] J. Balde and G. Messner: "Low Dielectric Constant - The Substrate of the Future". Circuit World, vol. 14, no. 1, 1987, page 11.

[5.9] a) S.J. Mumby and J. Yuan: "Dielectric Properties of FR-4 Laminates as a Function of Thickness and Frequency". Jour. of El. Materials, vol. 18 no. 2, 1989, page 287.
b) "Electronic Materials Handbook, Vol. 1: Packaging". ASM International, 1989, page 597.

[5.10] J.R. Paulus: "High performance Laminate Systems for High Speed Electronics Applications". Circuit World vol. 15, no. 4, 1989, page 19.

[5.11] J. Murray: "The FR-4 of the 1990s". Circuits Manufacturing, June 1988, page 18.

[5.12] a) Data sheets for RO 2800 and RO 2500, from Rogers Corporation, USA, and D.B. Noddin: "Fabrication of High Performance Multilayer Boards Using RO-2800 Fluoropolymer Composite Materials". (Rogers, 1989).
b) Data sheets for Goreply and Goreclad, Gore Corporation, Scotland.
c) Data sheets for Fortin X-0096 and L-1084 from Fortin Industries, USA.

[5.13] I. Henne, L. Halbo et al.: "Multichip modules for Gigabit per sec. Electronics". EPF-report, March 1990 (in Norwegian).

[5.14] R.C. Landis: "High Speed Packaging for GaAs Interconnection". 35th Electronic Components Conference, May 1985.

[5.15] "Mekankonferens" March 1988, Stockholm, Sweden.

[5.16] Microwire datasheet, and information from PCK Corp.

[5.17] S. Gurley: "Flexible Circuits". (Marcel Dekker, 1984).

[5.18] J.J. Miniet: "End User´s Guide to Innovative Flexible Circuit Packaging". (Marcel Dekker, 1986).

[5.19] M. Whelan: "Three-dimensional Moulded Printed Circuits". Circuit World, vol. 16 no. 2, 1990, page 25.

[5.20] L. Halbo (Ed.): "Polymer Thick-Film Technology (PTF). Design Guidelines and Applications". (Lobo, 1990).

[5.21] C.F. Coombs: "Printed Circuits Handbook". (McGraw-Hill, 1988).

[5.22] EPF reports on PTF, 1988-1990. (In Norwegian).

[5.23] R. Keeler: "Molded Circuit Boards Compete for High Volume Markets". Electronic Packaging and Production, June 1986, page 54.

[5.24] T. Gleditsch, K. Edvardsen og B.E. Flaten: "Design of high frequency PWBs. Handbook for Designers". EPF-report R-38, March 1990, and unpublished results. (In Norwegian)

CHAPTER 6

PRINTED CIRCUIT BOARD DESIGN

6.1 INTRODUCTION

The designers are key personnel in the development of a new electronic product but they are not the only ones. A successful product depends on an intimate co-operation between specialists from many fields. Their common goal is to make a product with the right quality at the right price.

General circuit design is outside the scope of this book. However, we shall discuss those aspects of the design connected to choice of technology, components, PWB layout and production on PCB/hybrid circuit level. (For hybrid circuit design, including polymer thick film circuits, see also Chapter 8.)

The design is generally performed on a CAD system. After entering the netlist and the components, the circuit diagram is worked out. Information and symbols for each component are stored in the CAD system component library. Instead of experimenting with hardware models more and more is done by computer simulations, as the circuit complexity and speed of operation increases.

The layout or PWB design is simplified by more or less automatic routing performed by the CAD system. Still, critical information about placement of certain components, electromagnetic compatibility (EMC), thermal limitations, etc., is manually entered by the designer.

From the CAD system we get the schematic, assembly drawings and other documentation, data for photo- or laser plotter to manufacture photographic films for the PWB production, data for the printing mask for solder resist and solder paste printing, data for numeric drilling and milling machines, placement information for pick and place machines, data for test fixtures and the testing machine, etc. (Please refer to. Section 5.3).

6.2 GENERAL GUIDELINES

6.2.1 Right quality

It is essential to design for right quality. This implies that the product must satisfy all specifications regarding electrical performance, reliability and product operating lifetime, ergonometry, etc. but the product should not be over-specified and thus unnecessarily costly. To achieve this it is important to:

- Choose the best suitable technology or combination of technologies, and an optimal partitioning
- Choose components with the right reliability and suitable packaging
- Design for manufacture
- Design for testability
- Design for ease of repair, etc.

The contact between the designers, testing people and the production department is formalised in "design review", after which the test specialists have accepted the design concerning testability, the production people have taken part in planning how the product will be produced and accepted the design concerning manufacturability in the available production line, etc. If the PWBs or printed circuit boards are to be produced by subcontractors, they must also participate in the planning, to insure that the product is fit for their production equipment. Otherwise, modifications or a re-design may be needed later, resulting in delays and extra cost.

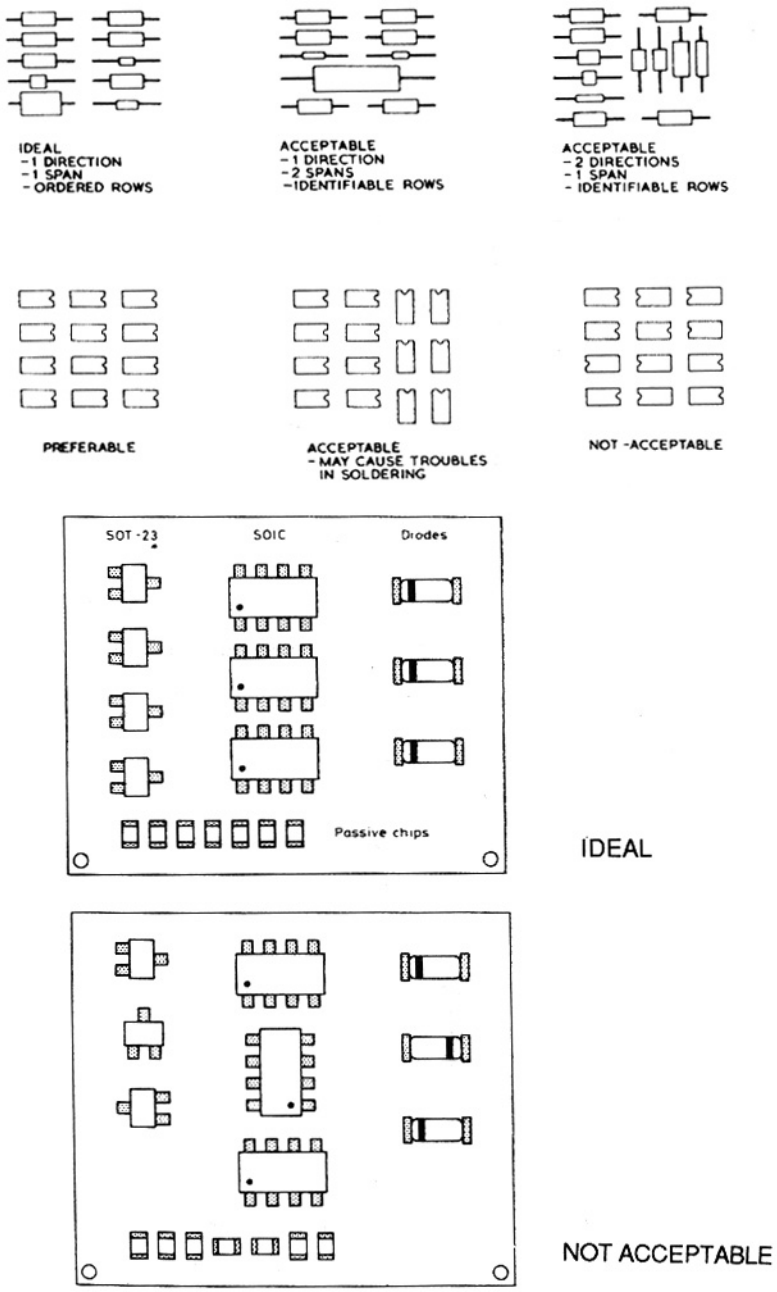


Fig. 6.1: Proper component placement for hole- and surface mounted components [6.1, 6.2].

6.2.2 Design for manufacture

By "manufacturability" we also mean that it is fit for robot mounting if it is planned, that components and materials can withstand the solder processes to be used, etc.

High yield, low cost production requires, for example:
- As few conductor layers as possible in the PWB.
- As coarse conductor pattern as possible (no fine line).
- As few component types as possible (standardisation).
- Robust electrical design (no tight tolerances).

Standardisation of the PWB sizes is of importance, to make them fit into standard cabinets, and to utilise the panel sizes effectively.

The components should be placed orderly, polarised components (diodes, electrolytic capacitors, ICs, etc.) oriented the same way when possible, see Figure 6.1. This gives the highest component density and most efficient assembly process, and it makes visual inspection easier.

6.2.3 Electromagnetic compatibility (EMC)

Wires and current loops on the PCB and in the electric system will act as antennas, emitting electromagnetic radiation that may interfer with radio communication and other electronic equipment. Likewise, the same elements of a system will act as receiver antennas for radiation, and incoming radiation may disturb the functioning of the system. It is essential that electronics are designed for low electromagnetic emission and high immunity. Besides radiation, the equipment must also be designed for low emission of noise on the power grid as well as high immunity for incoming noise. These factors are called ElectroMagnetic Compatibility (EMC), and disturbances called ElectroMagnetic Interference (EMI).

There are a number of international EMC standards that must be met by electronic equipment [6.0].

The emission is often caused by [6.0]:
- A conductor loop on a PCB, acting as a magnetic antenna, generating a field proportional to the current and the area of the loop.
- A conductor with a voltage drop, acting as a rod antenna.

Good EMC design is a large field and the reader should consult the specialised literature. However, some basic rules should be considered:
- Use a ground plane.
- Use compact component technology (SMT) and compact layout to reduce current loop areas.
- Do not use fast component technology (short rise-/fall times) and high clock frequency unless necessary.
- Use decoupling capacitors where appropriate.

Modifications of existing equipment to fulfil EMC standards are a lot more expensive and time consuming than making a good EMC design from the start.

6.3 HOLE AND SURFACE MOUNTED PCBs

6.3.1 Minimum dimensions

The conductors cross sectional area determines the maximum current in a conductor without excessive heating of the conductor and the PCB. Figure 6.2 shows the temperature increase as a function of current and conductor cross section. The data is based on convection heat transfer to the surrounding air, and lateral heat conduction primarily in the Cu foil.

The voltage drop in a long narrow conductor may also be of importance. It is given by (Figure 6.3):

$$R = \rho \times L/(t \times b)$$

where ρ is the resistivity in the copper layer, approximately 2.0×10^{-8} ohm m for rolled copper at room temperature.

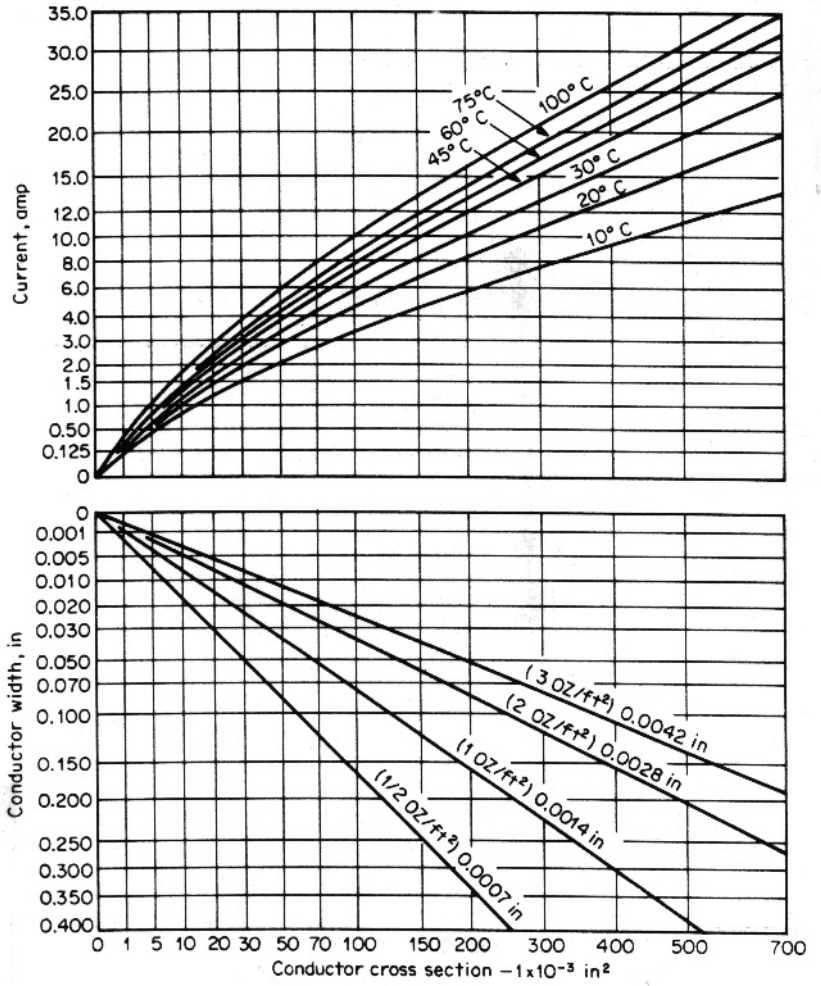


Fig. 6.2: Current capacity and temperature increase in conductors on PCBs [6.1, 6.3]. The lower figure shows the conductor cross-section (along the x-axis) as a function of the conductor width for different Cu-layer thicknesses. The upper figure shows the temperature increase (labels on each curve) at different combinations of cross-sections and currents).

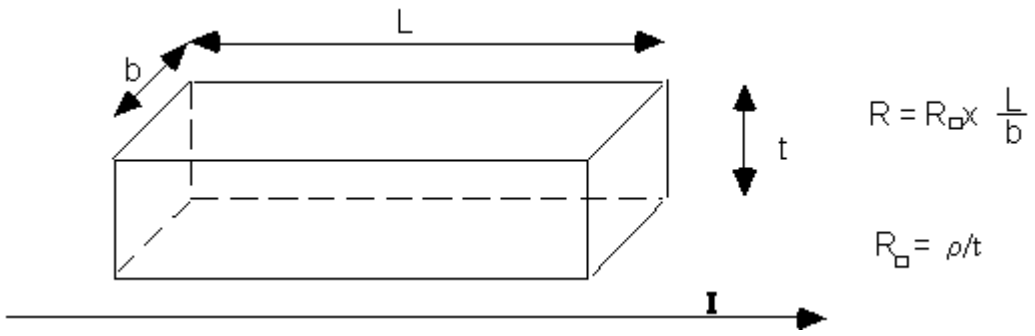


Fig. 6.3: Calculation of resistance in conductors; the parameter sheet resistance R_{sq}.($R_{\square}$).

The quantity ρ/t is called R_{sq}, or the sheet resistance, with unit ohm or ohm/square. Physically it is the resistance of a square sheet, irrespective of the size of the square. If t varies over the width of the conductor (which is normal in narrow conductors and in screen printed conductors in hybrid technology), R_{sq} means the average value of ρ/t.

Then:

$R = R_{sq} \times L / b$

In an 18 μm thick copper sheet $R_{sq} \sim 1$ mohm/sq
In a 35 μm copper sheet $R_{sq} \sim 0.5$ mohm/sq.

Table 6.1: Examples of minimum dimension and PCB classes [6.1, 6.2, and 6.5]. The class indicates how many conductors can pass between the solder pads of a DIP package (no. of channels), and typical corresponding minimum dimensions in mm. When two figures are given for hole diameters, they are for component- and via holes respectively.

Class	0	1	2	3	5 *)	7 *)
Conductor width, b	0.4	0.3	0.22	0.15	0.13	0.10
Conductor separation, I	0.5	0.3	0.2	0.17	0.12	0.10
Hole diameter, d	0.9	0.8/0.5	0.8/0.5	0.8/0.3	0.8/0.2	0.8/0.1
Hole pad diameter,D	1.8	1.5	1.3/1.0	1.3/.65	0.6 0)	0.4 0)

*) Toshiba development work 1992 [6.34]

0) Via hole only.

Characteristic dimensions on the PCB such as conductor width and separation between different conductors have standardised minimum values, depending on the number of "channels", i.e. how many conductors that can pass between the leads of a Dual In line Package (DIP) or between via holes with 100 mils separation. We shall designate this as layout "Class". Thus, Class 3 means that 3 conductors may be routed between neighbouring mounting holes for a DIP package. The exact figures may vary slightly from one company to another, but typical figures are given in Table 6.1. It is

important to make a distinction between the dimensions defined in the CAD station and the dimensions on the PCB. This is due to underetching (see Section 5.8).

Larger dimensions than the minimum values should be used whenever possible in order to raise the production yield.

Figure 6.4 shows the separations between solder area and solder resist. The solder resist is usually screen-printed for layout in Classes 0 and 1. Therefore, it is necessary to have a relatively large separation due to the limitations in the screen printing process. In class 2 or higher, a photo-processed solder resist is used (see Section 5.6). Photo-processed solder resist must be used if conductors are to pass between the terminals of a surface mount component. If a dry film is used it may be advantageous to cover the vias, ("tenting", see Figure 5.6 b) in order to prevent the solder from entering the vias [6.1].

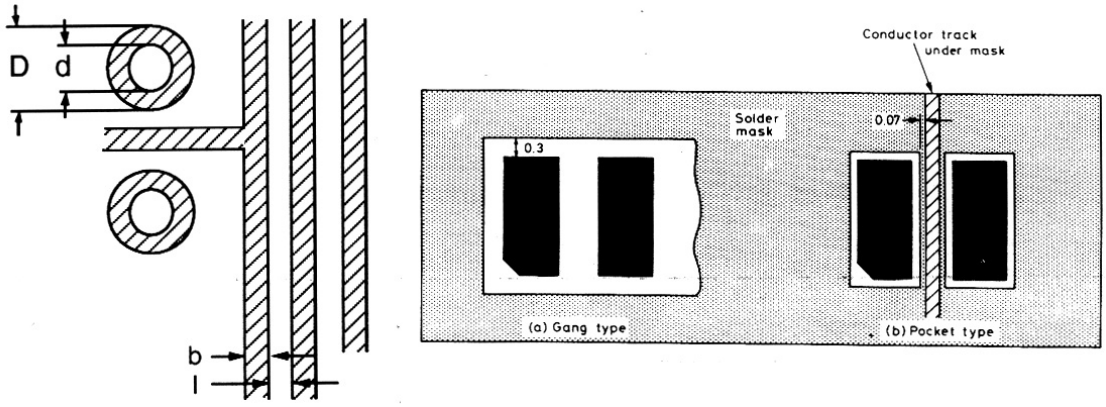


Fig. 6.4: a): Parameters in layout dimensions used in Table 6.1. b): Minimum dimensions for solder mask for surface mount PWBs. Left: Dimensions for screen printed solder mask, with one common opening for all solder lands of an IC package, right: photoprocessible solder mask with a "pocket" for each terminal, permitting conductors between the solder lands [6.2].

6.3.2 Different PCBs and limitations on components and solder process's

The most common combinations of components on the two sides of hole- and surface mounted PCBs are shown in Figure 6.5. The components are soldered by a combination of reflow- and wave solder processes. Wave soldering may be done on the secondary side only.

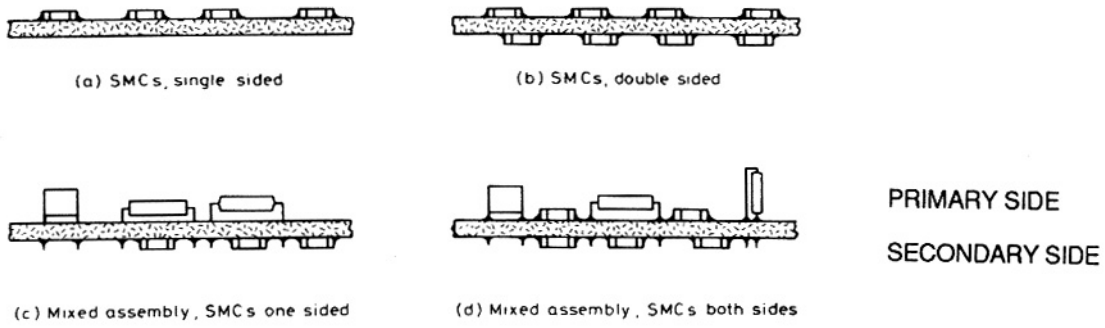


Fig. 6.5: Common types of SMD- and mixed SMD-/hole mount PCBs.

Not all surface mount components can withstand the thermal shock represented by a solder wave. Furthermore, solder bridges between the leads may be encountered due to the lead shape, component body shape or small lead pitch. It is therefore recommended that all SMD ICs are reflow soldered, or at least LLCCs and the other packages with terminals on all four sides. Special types of wave soldering equipment may enable wave soldering on different types of SMD ICs, such as SO packages (please refer to Section 7.3).

Through hole mounted components normally cannot withstand the temperature of wave soldering. They are therefore mounted on the primary side only, or they are manually mounted and manually soldered after machine soldering is completed. Neither can they withstand the reflow soldering process, and therefore the wave soldering must be done after the reflow soldering.

These constraints must be considered during the design process. Some of the production process details for the different PCB configurations will be discussed in Sections 7.3 and 7.5.

SMD components that are wave soldered have a preferred orientation with respect to the solder wave, see Figure 6.6. Solder bridges, non-wetted areas and the effect of "shadowing" are reduced in this way (see Section 7.3). The shadowing effect is more pronounced for tall packages. There should be a minimum distance between components, see Figure 6.7. The reasons are:

- Reducing solder bridging
- Take care of tolerances in component size
- Necessary space for the mounting head of the pick and place equipment
- Tolerances in the placement accuracy
- Ease of repair, visual inspection, space for de-soldering equipment, etc.

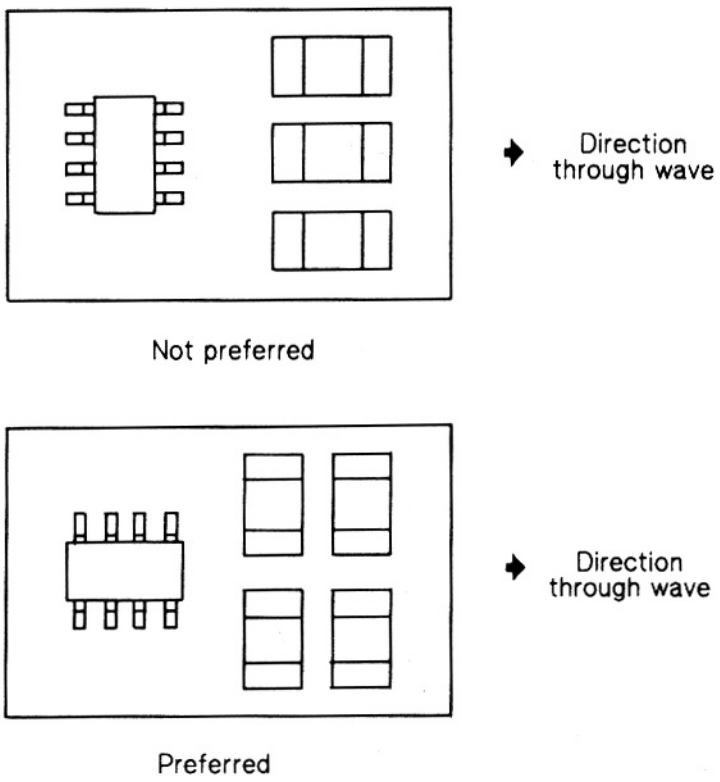


Fig. 6.6: Preferred and not preferred directions of SMD components during wave soldering.

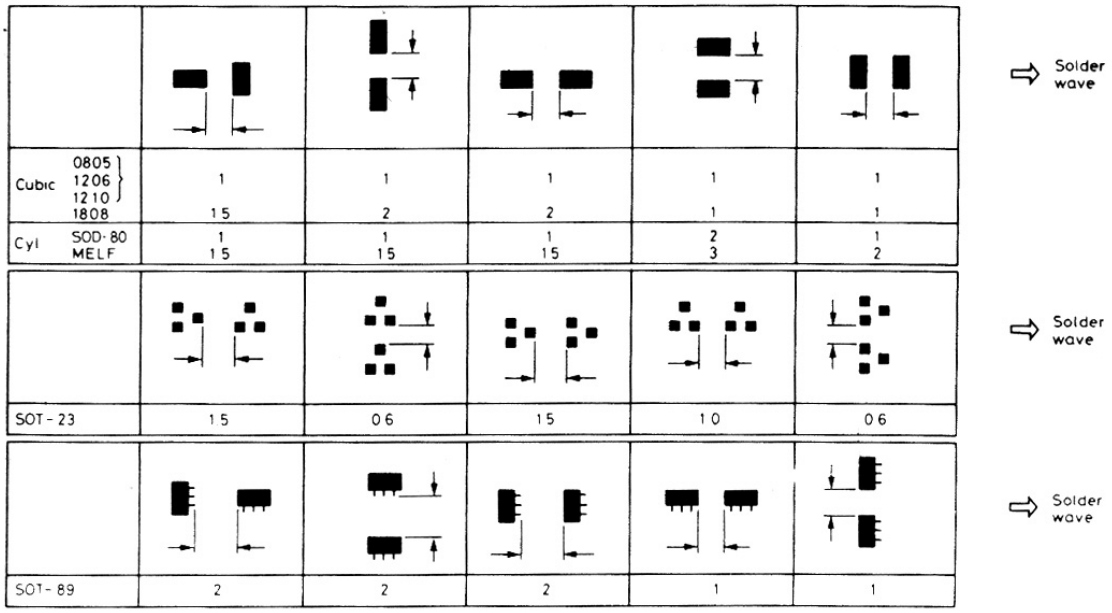


Fig. 6.7: Minimum separation between SMD components during wave soldering [6.2].

6.3.3 Some general rules

The PWB should include 2 - 3 guiding holes and registration marks for accurate positioning in the production equipment.

Solder lands should be thermally isolated from large Cu-foil areas by limiting their extension as shown in Figure 6.8. The solder mask should cover all area except the solder lands (and hole pads), to prevent the solder from spreading during reflow. Tracks should approach the solder lands symmetrically and perpendicularly (90^{o} angles).

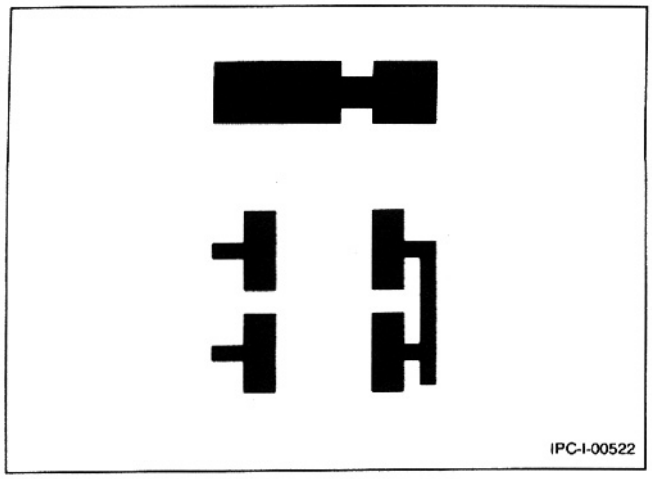


Fig. 6.8: Solder lands for SMD components should be separated from heavy copper areas by narrow constrictions. Conductors should preferably leave the solder lands of one component symmetrically.

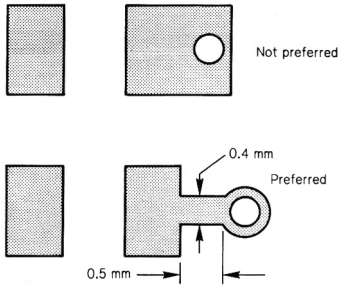


Fig. 6.9: Via holes should be separated from solder lands.

Via holes should be located separate from solder lands to prevent the solder from spreading into the via holes, see Figure 6.9. Via holes underneath SMDs should be covered by a dry film solder mask to prevent trapping of solder flux from wave soldering.

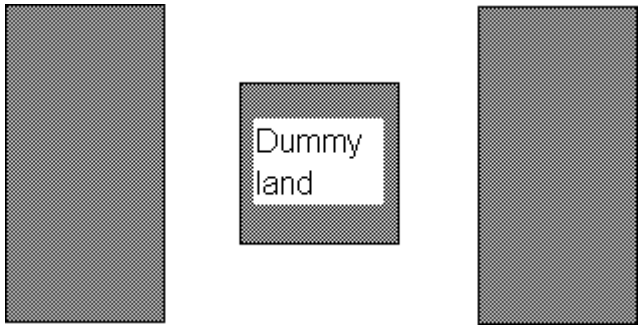


Fig. 6.10: Dummy land for better control of the amount of adhesive in wave soldering process.

If SMD resistors and capacitors are to be bonded by adhesive then a “dummy land” or "dummy pad" of copper should preferably be located beneath the component, see Figure 6.10. This will give better control with the distance between component and board surface, and reduce the needed amount of adhesive. The dummy pad is not relevant if there is a conductor track underneath the component.

If SO- or VSO packages are to be wave soldered there is a risk for formation of solder bridges between the two last leads. This risk is substantially reduced if "solder thieves" are located as shown in Figure 6.11. This also applies to hand soldering of SOs, VSOs or flatpacks.

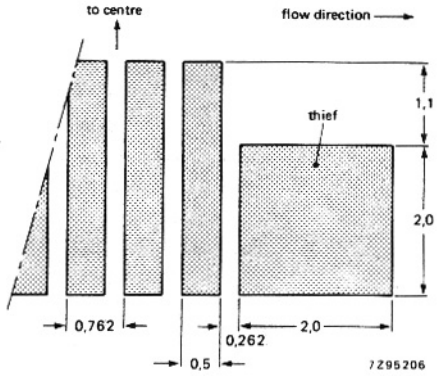


Fig. 6.11: "Solder thieves" are areas in the Cu layer to reduce bridging in wave soldering [6.6].

6.3.4 Dimensions of solder lands

It is important to use optimal dimensions and positions for the solder lands to minimise solder defects and optimise strength and reliability in the solder joints.
The optimal choice depends on a number of parameters, such as:

- Adhesive- and solder process and equipment, dimensions of the components and their tolerances (typically +/- 0.1 - 0.2 mm).
- Dimension tolerances in PWB (0.05 - 0.15 mm), and in the solder printing process.
- Conductor line widths and tolerances (0.1 - 0.2 mm).
- Pick and place equipment and placement tolerances (0.05 - 0.2 mm).
- Visual inspection.
- Density of components.
- Repair procedures.
- CAD equipment, standardisation, etc.

The importance of some of these tolerances is reduced if electronic pattern recognition is used. Many of these parameters are different for different manufacturers and even between different products and production lines for the same manufacturer. The dimensions for a specific component may vary considerably between different manufacturers.

One may therefore frequently encounter different recommended design rules for each specific component, (see, e.g. [6.2, 6.4-6.9]).

Rectangular solder lands or rectangular lands with rounded corners are used for SMDs. Rounded corners are preferred for photo plotting because a larger aperture may be used. In the wave solder process larger solder lands are used than for reflow soldering, to improve wetting and prevent the shadow effect (Section 7.3). It is common practice, in wave soldering, to use solder lands slightly wider than the component itself for narrow components. Some manufacturers use solder lands considerably narrower than the component, however. This gives a smaller solder fillet with less mechanical stress and improved reliability, but it requires more accurate component placement. For wide components narrow solder lands should always be used to avoid excessively big solder fillets.

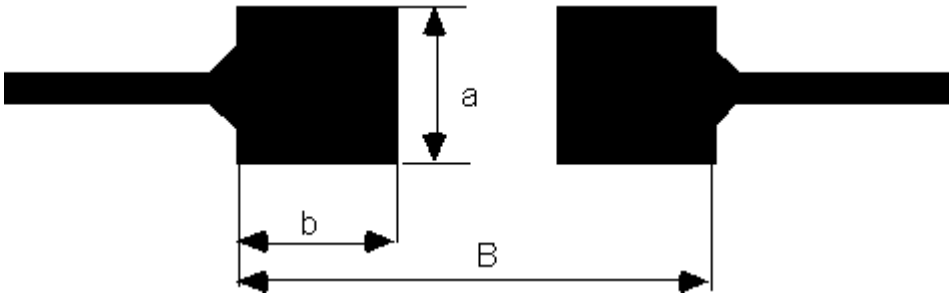


Fig. 6.12: Parameters defining solder land dimensions for SMD resistors and capacitors, please refer to Table 6.2.

Figures 6.12 and 6.13 show some different parameters describing the PWB layout for passive components and Table 6.2 shows recommended dimensions. These and the following recommendations are based on [6.2, 6.4 - 6.5] and the experience from ABB plants. In the case of components with known dimensions, not shown in the table, the following empirical expressions may be employed, see Figure 6.13 [6.4, 6.8]:

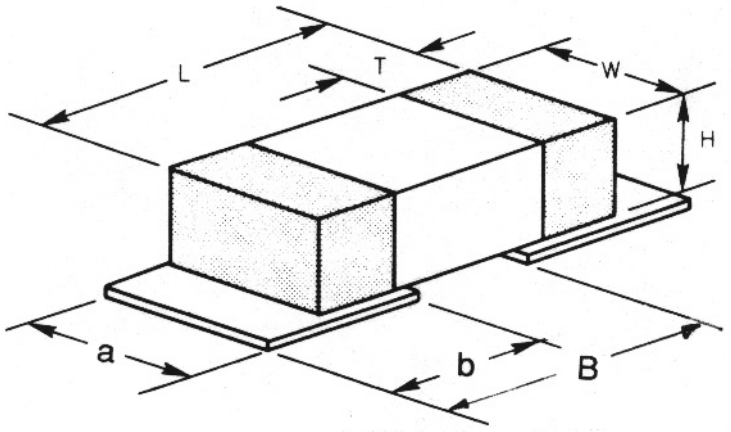


Fig. 6.13: Additional dimensions of SMD component and solder lands.

Table 6.2: Solder land dimensions for SMD resistors and capacitors (mm), please refer to Figure 6.12.

		Wave soldering			Reflow soldering		
Type	Size	a	b	B	a	b	B
	0603				0.9	0.8	2.3 *)
Chip	0805	1.45	1.2	3.65	1.45	0.8	2.65
resistors	1206	1.7	1.4	4.85	1.7	1.0	3.65
and	1210	2.75	1.4	4.85	2.75	1.0	3.6
capacitors	1808	2.25	1.5	6.45	2.25	1.1	5.2
	1812	3.25	1.5	6.45	3.25	1.1	5.2
	2220	5.3	1.6	7.6	5.3	1.2	6.2
Al electrolytic	1a	2.5	2.0	10.0	2.5	3.0	9.0
capacitors (Philips)	1	2.5	2.0	14.0	2.5	3.0	12.0
Tantalum	a	1.5	2.0	5.0	1.5	1.1	3.2
electrolytic	b	1.5	2.0	6.3	1.5	1.1	4.5
capacitors	c	1.5	2.0	7.55	1.5	1.1	5.75
(Philips)	d	2.75	2.0	6.3	2.75	1.1	4.5
	e	2.75	2.0	7.55	2.75	1.1	5.75
	f	3.65	2.2	8.45	3.65	1.3	6.65
	g	3.0	2.5	9.15	3.0	1.6	7.35
	h	4.0	2.5	9.65	4.0	1.6	7.85

*) Solder land dimensions of 0603 components are discussed in [6.35]

Width of solder land: $a = W_{max} + K$

Length of solder land:

- Reflow soldering: $b = H_{max} + 2T_{max} + K$
- Wave soldering: $b = H_{max} + 2T_{max} + 2K$

Total length: $B = L_{max} + 2H_{max} + 2T_{max} + K,$

Where the subscript maximum means the maximum component dimension inside the tolerance and K = 0.25 mm. Recommended layout for diodes and transistors is shown in Figure 6.14.

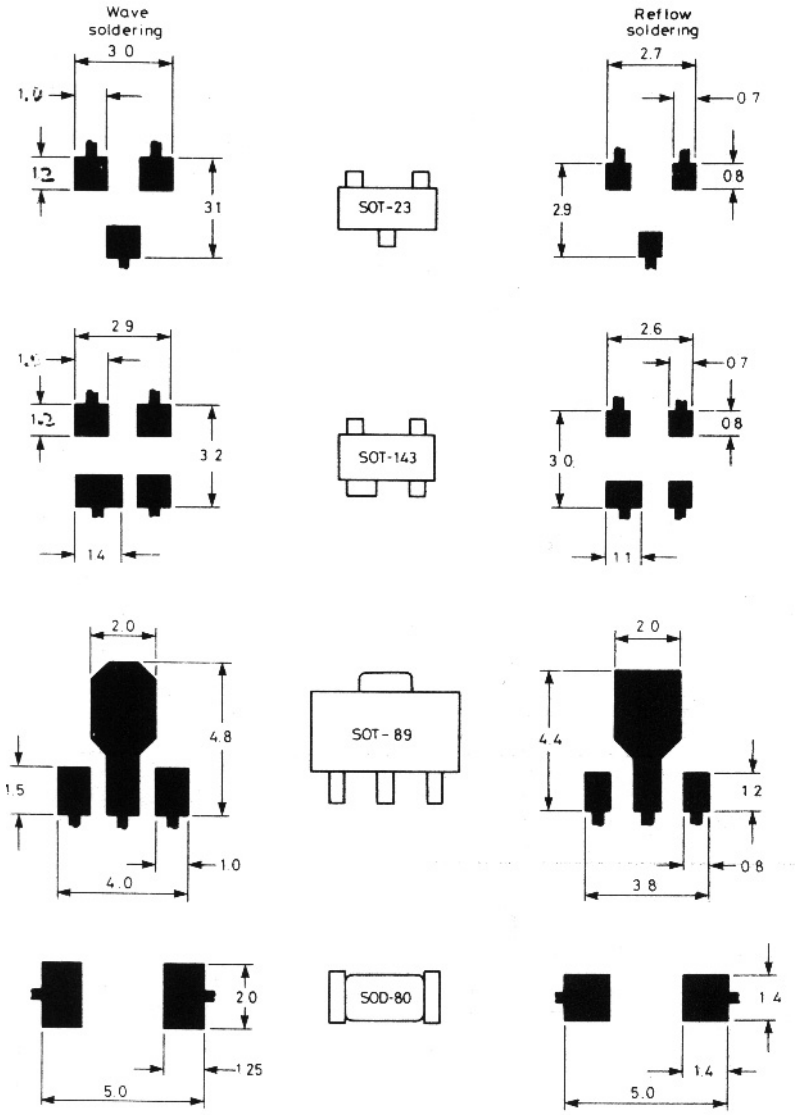


Fig. 6.14: Solder land dimensions for SMD transistors and diodes [6.2].

Table 6.3: Solder land dimensions for SO or VSO components (mm), please refer to Figure 6.15.

Package	Pitch, P	a	b	A
SO-8 to -16	1.27	0.63	1.5	7.2
SO-16L to -28	1.27	0.63	1.8	11.6
VSO -40	0.76	0.4	2.7	13.6

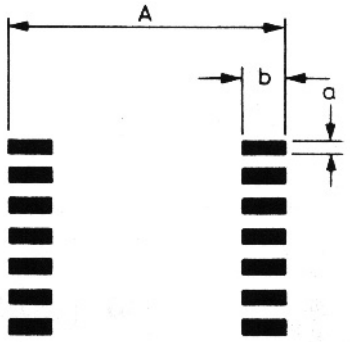


Fig. 6.15: Solder land dimensions for SO and VSO packages, please refer to Table 6.3.

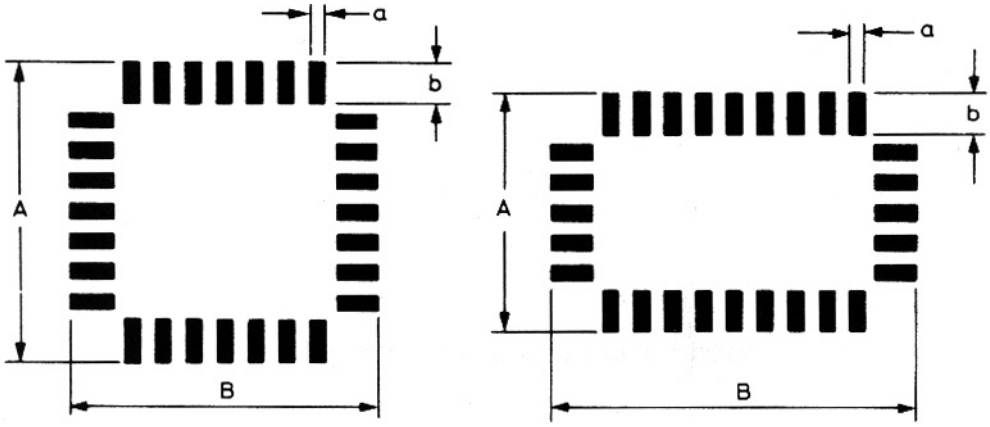


Fig. 6.16: Solder land dimensions for PLCC, LLCC and flatpacks, please refer to Tables 6.4 - 6.7.

Table 6.4: Solder land dimensions for PLCC (mm), please refer to Figure 6.16.

Pitch, P = 1.27 (0.050") a = 0.63 b = 2.0

Number of terminals	18	20	22	28	32	44	52	68	84
(on side A/B)	(4/5)	(5/5)	(4/7)	(7/7)	(7/9)	(11/11)	(13/13)	(17/17)	(21/21)
A	9.0	9.4	13.4	10.8	13.3	18.4	21.0	26.0	31.1
B	12.6		14.6		16.0				

Table 6.5: Solder land dimensions for LLCC (mm), please refer to Figure 6.16.
Pitch, P = 1.27 (0.050") a = 0.63 b = 2.5

Number of terminals	16	20	24	28	44	52	68	84
A = B	9.8	11.1	12.4	13.6	18.8	21.3	26.4	31.5

Table 6.6: Solder land dimensions for flatpacks (mm), please refer to Figure 6.16.
b = 2.5

Number of terminals	44	48	52	54	64	70	80	100
(on side A/B)				(13/14)	(13/19)	(11/24)	(16/24)	(20/30
A					19.4	17.0	18.5	18.5
	15.0	18.0	22.0	15.0				
B					25.4	29.2	24.5	24.5
P	0.8	0.8	1.0	0.65	1.0	0.8	0.8	0.65
a	0.4	0.4	0.5	0.35	0.5	0.4	0.4	0.35

Table 6.7: Solder land dimensions for square miniature flatpacks (mm), please refer to Figure 6.16.
Pitch, P = 0.63 (0.025"), a = 0.3, b = 1.5

Number of terminals	84	100	132	164	196	244
A = B	20.5	23.0	28.0	33.2	38.2	42.5

Layout for SO- and VSO packages are shown in Figure 6.15 and Table 6.3, and layout for PLCC, LLCC and flatpacks are shown in Figure 6.16 and Tables 6.4-6.7.

The following empirical formula may be used for flatpacks with known dimensions, see Figure 6.16 [6.8]:

$a = B_{max} + 0.1$ mm
$b = F_{max} + 0.4$ mm
$A,B = E_{max} + 0.8$ mm,

Where:
B = width of the lead
F = length of the footprint of the lead
E = separation between lead ends on opposite sides of the package.

Recommended solder land dimensions for Tape Automated Bonding (TAB) components are shown in Figure 6.17.

More details are given in the references, especially [6.4].

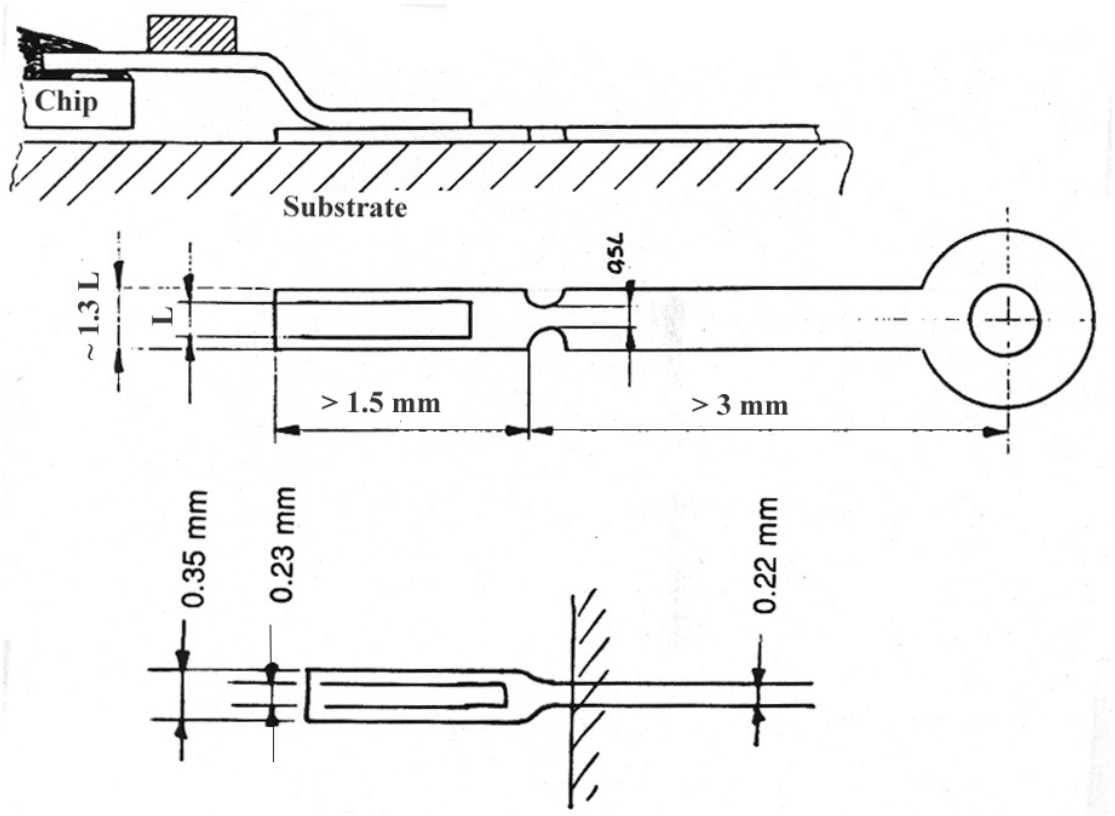


Fig. 6.17: Solder land dimensions for TAB [6.10].

6.3.5 Design of printing screens for solder paste

The correct amount of solder paste is important for strength and reliability of the solder joints. A suitable amount of solder paste for discrete components and IC's with 50 mil pitch is obtained by depositing a 175-200 μm high layer of solder paste over the whole solder land area. It may be an advantage to use a thicker layer over a reduced area, if a thick dry film solder mask is used.

A smaller amount of solder paste should be used on ICs with finer pitch to avoid solder bridges [6.11]. Either a reduced area of the screen opening may be used, or a thinner screen. See also Section 7.3. In the thermode soldering process (Section 7.3) less solder should be used than in the normal reflow soldering process.

If TAB circuits are used, the solder is normally applied by electroplating [6.10, 6.11].

6.4 DESIGN FOR TESTABILITY

Careful production testing is important to avoid sending faulty products onto the market, which may lead to great expenses and loss of reputation and market share. For complex products the testing may be time consuming and cost nearly as much as the rest of the production. Still it may not be practical to have a test that will detect all possible faults. The test effectiveness is described by:

$$DL\ (ppm) = 1 - Y^{(1-T)} \times 10^6$$

where :

DL = Defect level: the fraction of delivered products that contains faults.
Y = Yield = 1 - (Probability of producing a faulty product).
T = Fault coverage: The probability that an existing fault is detected in the testing.

Thus, to minimise the defect level it is important to have a high production yield (few faults produced), and a test procedure giving a high fault coverage. Designers and test specialists should co-operate intimately during product design to develop a good test strategy.

There are two main test principles: Functional test and in-circuit test.

6.4.1 Functional test

In this test method electrical signals typical of the operation of the circuit are applied to the connectors on the PCB. The responses to these signals are recorded and compared to the correct response.

Advantages of functional test:
- The components are tested in their operating environment.
- Design faults may be found.
- Timing problems may be found.

Disadvantages of functional testing:
- Necessary software development is time consuming.
- Requires highly skilled personnel.
- Will normally not localise the fault.
- Long testing time.
- New faults may be generated in the test.
- Limited fault coverage.

6.4.2 In-circuit test

In this test method each component is tested individually with test probes. Neighbouring components must be isolated by guarding techniques in analogue circuits or latching in digital circuits [6.3].

Advantages of in-circuit testing:
- Short testing time: The test localises the fault.
- Many faults may be found simultaneously.
- Less time consuming software development.
- The PCB does not need to be powered up, and the danger of generating faults by the test is reduced.

Disadvantages:
- Time consuming test.
- The interactions between components are not tested.
- Require expensive test fixture.
- Access to all nodes in the circuit is necessary.

The circuit complexity and production volume are important factors in the decision of test method. Therefore the typical extra board area needed for the test points for in circuit testing is less than 5 %, and the cost of area is rarely an important argument against in-circuit test. A combination of the two methods is also common: Smaller functional blocks may be functionally tested, and critical components may be in-circuit tested.

6.4.3 Design for improved testability

The testing time may be reduced and the fault coverage increased by designing in additional electronic functions on the board, explicitly for optimising the testing. Among the methods are "Level sensitive scan design", "Scan path", "Boundary scan", "Built-in self test" [6.12, 6.14].

6.4.4 Guidelines

Some guidelines for test strategy:

- Use single sided testing if at all possible. Double sided test fixtures (see Section 7.6) are expensive and less robust.
- The testing should be made on separate test points, not on the component leads or solder lands, please refer to Figure 6.18.
- The test points should preferably be located on a 0.1" grid, please refer to Figure 6.19. They ought to be 0.9 mm or more in diameter. Test probes for 0.05" pitch test points are easily damaged during the testing. False faults will be recorded, and the test fixture must be frequently repaired. If it is necessary to use 0.05 "pitch testing, it should be limited to the minimum necessary test points.
- The test points should be covered by solder to obtain reliable contact, and not be covered by solder mask.
- The height of high components on the testing side of the board must be considered when the test fixture is designed.

The testing is a major cost in complex products and it is good practice to plan test procedures early in the product development phase. Production volumes, expected type of faults, test software and hardware development costs and board time in the test equipment are important issues to consider. A computer integrated interface between test development and other design activities will lead to cost reduction and fewer errors in information exchange between different design and development activities. This is a part of computer integrated manufacturing (CIM).

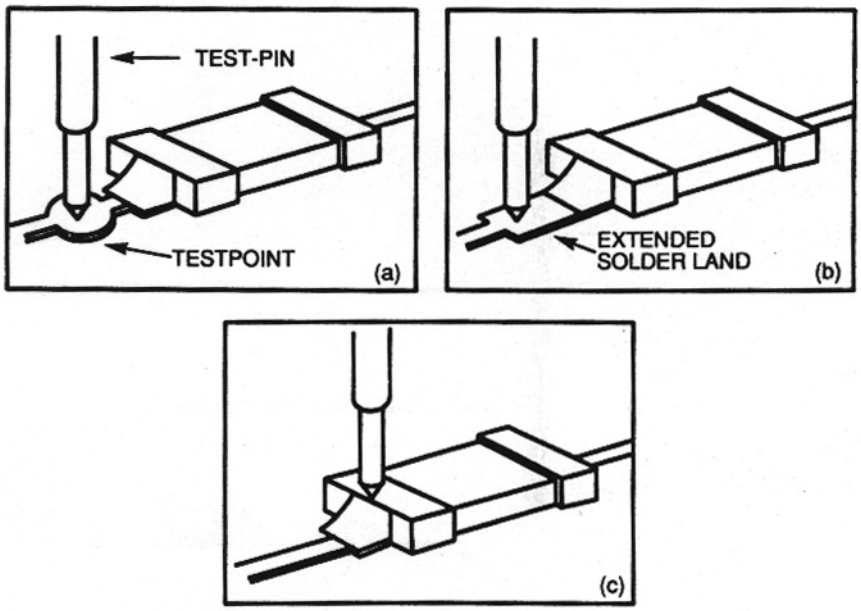


Fig. 6.18: a): Correct position of test point, separated from solder land. b): Test points on solder lands are not recommended. c): Testing on components or component leads should be avoided.

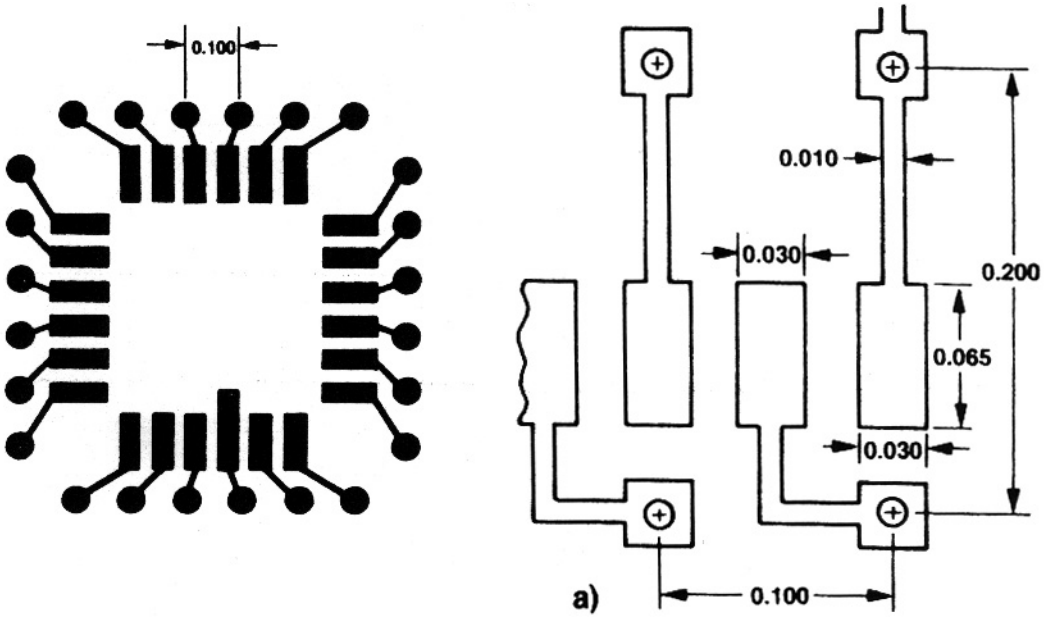


Fig. 6.19: Examples of test point placement on a grid with 0.1" spacing, for testing of SMD components with 0.05" pitch [6.4].

In addition to the product test described, a new design will be stress tested for verification of the reliability of the design. This will be described in Chapter 9.

6.5 MATERIALS CONSIDERATIONS FOR THERMAL COMPATIBILITY

Combinations of materials with different TCEs may give rise to strain and mechanical stress. The problem increases with the size of the components, the magnitude of the difference in the TCEs, and the temperature variations, Figure 6.20.

SMD resistors and many capacitors have bodies of ceramic. Due to their small size they may normally be soldered onto organic substrates (PWBs) without thermal mismatch problems. Leadless ceramic ICs (LLCCs) with sides less than approximately 10 mm (28 terminals or less), may be soldered onto organic boards in less demanding environments. For larger LLCCs we have the following alternatives:

- Socket mounting
- Soldering of leads onto the components (provided it is suitable for it, please refer to Section 4.5)
- Use of PWB with a compliant organic surface layer (marginal improvement only)
- Use of PWB with low TCE metal core (please refer to Section 5.9)
- Use of ceramic substrate (daughter board/thick film hybrid circuit).

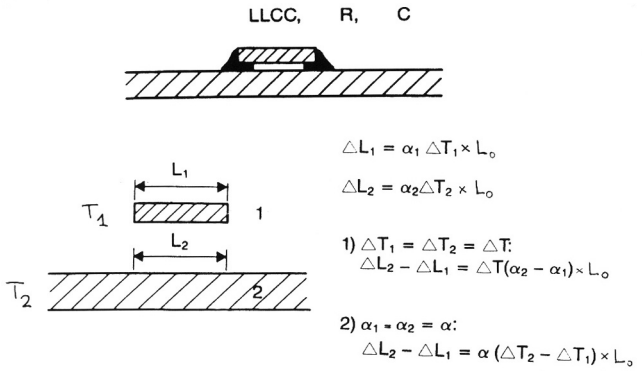


Fig. 6.20: Mechanical strain is caused by difference in coefficient of thermal expansion (TCE), and changes in temperature. The magnitude of the corresponding stress depends on dimensions, temperature difference/change, and the elastic moduli of the materials.

In many cases it is possible to use leaded IC packages as an alternative to LLCCs (Section 4.5).

6.6 THERMAL DESIGN

6.6.1 Why thermal design?

Miniaturisation is a major trend in current electronic design. In most cases this results in higher heat dissipation per volume and higher temperatures in the components unless thermal design is emphasised.

The essence of thermal design is to assure, during the design phase, that all components operate within specified temperature limits. Selection of components, packages, component layout, PWB materials, cooling fins, fans, etc. is part of the thermal design.

An important reason for doing thermal design is the fact that increasing operating temperature results in shorter expected operating life.

Typically for electronic products, a 10°C temperature increase reduces the life length by 50%. This is often discussed in terms of Arrhenius equation [6.16 - 6.18].

For materials with thermal mismatch the time to failure will often decrease when cyclic temperature variations increase.

The main purpose of thermal design is to obtain a sufficiently high reliability at the lowest possible cost.

6.6.2 Heat transport

Heat generated in the components must be transported away to the ambient environment. There are three fundamental modes of heat transportation: conduction, convection and radiation, Figure 6.21. The two first modes are most important, and for SMDs the heat conduction dominates (unless forced air circulation is used).

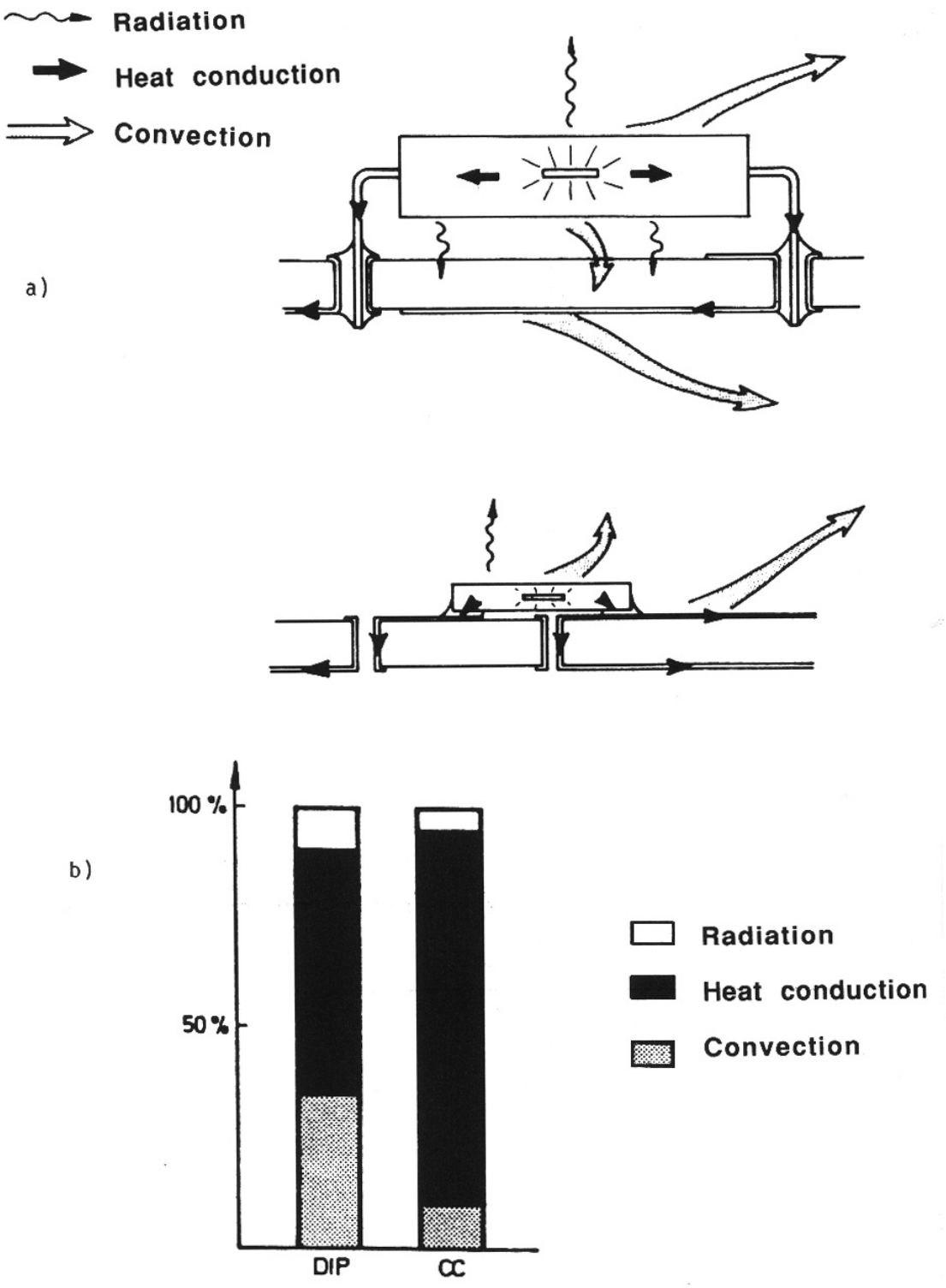


Fig. 6.21: a): Heat flow from hole mounted and surface mounted components on a PCB. b): Relative amount of heat removed by conduction, convection and radiation, from DIP hole mounted components and SMD LLCC components - typical values.

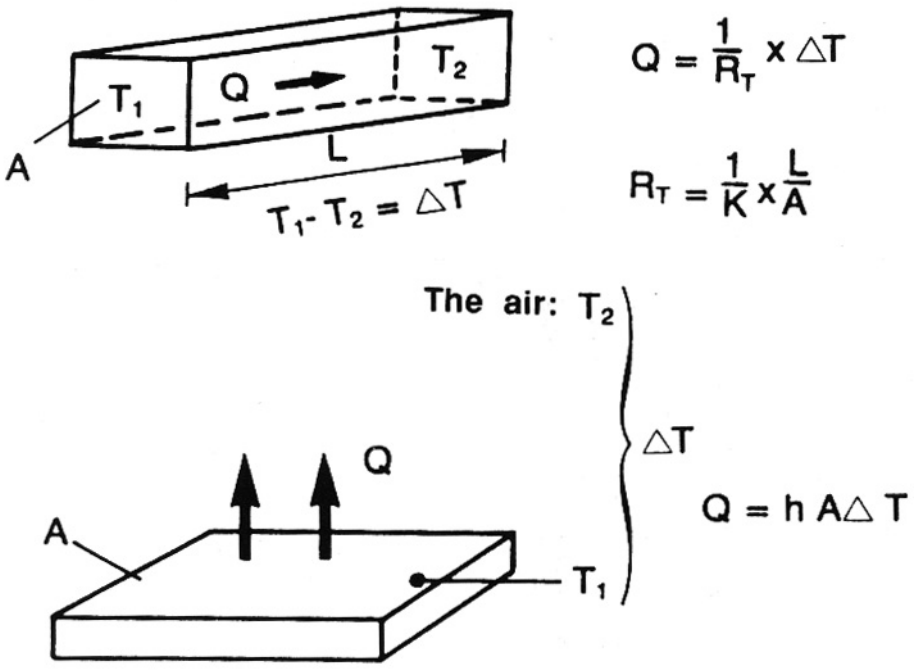


Fig. 6.22: a): Heat flow due to conduction - Fourier´s equation. b): Heat flow due to convection.

Fourier´s law describes heat conduction, see Figure 6.22:

$Q = \Delta T/R_T$

Where:
$R_T = 1/K \times L/A$, and:

Q = Heat flow (W)
ΔT = Temperature difference (°C)
R_T = Thermal resistance (°C/W)
K = Thermal conductivity (W/m°C)
L, A = Length and cross-sectional area of the thermal conductor

Fourier´s law is equivalent to Ohm's law for electrical conduction:

$I = \Delta U/R_{el}$

Where:
$R_{el} = 1/\sigma \times L/A$

Heat transport by convection is described by:

$Q = h \times A \times \Delta T$

Where:

h = convection coefficient ($W/m^2 \times {}^oC$).

6.6.3 Thermal modelling and material properties

Thermal design is often simplified by considering the analogy between thermal and electrical conduction. The different paths for heat transport in a component may be represented by a small number of "thermal resistors". Figure 6.23 shows the thermal resistance's from junction to case R_{jc}, from junction to lead R_{jl} and from junction to ambient R_{ja}. The model is inaccurate and the parameters are interrelated.

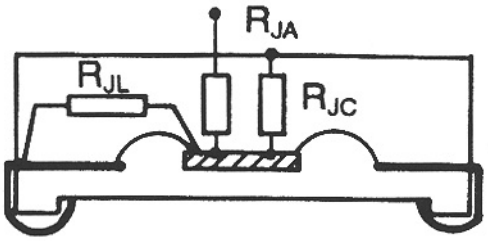


Fig. 6.23: Thermal model of an IC and package.

If the ambient temperature T_a and R_{ja} are known, then the junction temperature is found by:

$$T_j = T_a + P \times R_{ja} .$$

The thermal resistance of a specific component depends on the material and the geometry of the lead frame, material and geometry of the package, the number of terminals and the size of the silicon chip. Some typical figures are shown in Table 6.8, but manufacturers' data should be used in specific cases. It is also important to check that the measurement conditions under which the manufacturer's data have been obtained are similar to the conditions of interest for the user.

The effective thermal resistance for intermittent or cyclically varying power dissipation needs special methods of calculation [6.18].

Most of the heat flows from the chip to the leads and into the PCB or substrate. Furthermore, the heat flows laterally in the PCB and into the surrounding air by convection. The thermal conductivity of the PCB is therefore an important parameter.

Polymer materials commonly used in PCBs have a low thermal conductivity of approximately 0.2 W/m°C, Table 6.9. However, the high thermal conductivity of the copper conductors, typically 350 W/°Cm, increases the effective thermal conductivity above this figure. Because a PCB is a layered structure the thermal conductivity will be different in the directions perpendicular and parallel to the surface (lateral).

Table 6.8: Typical thermal resistances for various package types (°C/W). (Data from manufacturers` data books and [6.36].)

Package type			R_{JC}	R_{JA}
	SOT -	23	50 - 300	300 - 500
		89	30 - 60	50 - 300
	SO -	8	30 - 50	150 - 250
		16,16L	25 - 40	80 - 180
		28	15 - 30	60 - 100
	PLCC-	20	25 - 40	70 - 100
		44	15 - 25	40 - 70
		84	10 - 25	30 - 40
	LLCC-	20	15 - 25	
		44	10 - 20	
		84	10 - 20	
	DIP -	8	30 - 50	80 - 150
		16	30 - 40	70 - 100
		28	15 - 30	40 - 80
		64	15 - 20	30 - 50

Table 6.9: Typical values for the effective thermal conductivity of different types of PCBs.

Type	Effective thermal conductivity (W/m °C)
FR-4 without Cu	0.2
1 Cu conductor layer, 35 µm	1.7
2 layers, 35 µm	3.1
4 layers, 2 x 35 µm, 2 x 70 µm	15 - 25
Metal base board, 0.5 mm core	50 - 100

The effective thermal conductivity in the lateral directions is given by a "parallel connection" of all the layers:

$$K_{eff} = \text{SUM}\,(k_i t_i)/t_{tot}$$

where:
k_i = thermal conductivity of layer i.
t_i = thickness of layer i.
t_{tot} = total PCB thickness.

If only a fraction b_i of the surface of layer i is covered by conductors then:

$$k_i = b_i K_i$$

where:
K_i = thermal conductivity of the conductor material (copper).
b_i = fraction of the PCB surface covered by conductors, "fill fraction".

As the thermal conductivity of copper is so much higher than that of the polymers, the thermal conductivity is primarily determined by the conductor layers, their thickness and fill fractions. PCBs with four or more layers have ground and power planes with very high fill fraction and the thermal conductivity of these PCBs are enhanced. Thick metal cores used for thermal expansion control also increase the thermal conductivity greatly. Some figures are shown in Table 6.9.

The thermal conduction vertically through the board can be calculated as a series connection of all layers. However, with many metallised via holes through the board the thermal conduction is normally so high that we can assume the same temperature on both sides of the board.

6.6.4 TCE design of metal core boards

As mentioned, metal core boards offer the possibility of tailoring their thermal coefficient of expansion (TCE).

The resulting TCE, a, can be calculated from the following formula:

$$\alpha = \text{SUM} (\alpha_i E_i t_i) / \text{SUM} (E_i t_i)$$

Where:
t_i = thickness of layer i.
α_i = TCE of the material in layer i.
E_i = Elastic modules for material in layer i.

Values of α and E for the most important materials are given in Table 6.10.

An example of dimensions for such a board is shown in Figure 6.24 a) [6.15]. The goal was to achieve an over-all TCE of 6 - 7 ppm/° C, to accommodate large LLCC packages. Compromises have to be made in thicknesses, due to standard laminate- and metal core thicknesses available. The dimensions used are given in the figure.

Table 6.10: Material parameters for calculating TCE and effective thermal conductivity of metal core boards.

Parameter	Copper	Invar	Glass/epoxy
α [ppm/°C]	16	1.7	12
E [10^9 N/m^2]	110	140	19
K [W/ m x °C]	350	10	0.2

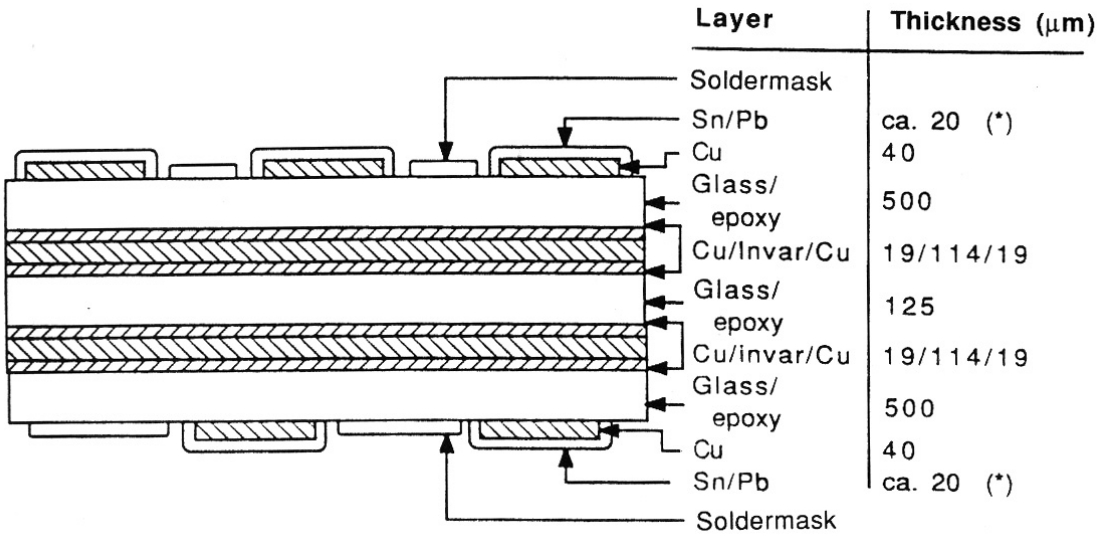


Fig. 6.24: Cross section and thicknesses for a practical PWB with two Cu/Invar/Cu cores [6.15]. The thicknesses were designed to get an over-all TCE of 7.5 ppm/°C x m. The achieved value was measured to be 9.3 ppm/°C x m. Calculated effective thermal conductivity in the x - y directions was 21 W/ °C x m.

6.6.5 Convection and improved cooling

Calculations of convection are generally difficult. A number of practical rules for specific cases and geometries exist in the specialised thermal design literature [6.17, 6.18]. Narrow horizontal or vertical passages between boards and surrounding structures may give complex air flow. The temperature of the surrounding air may not be very well defined and may cause uncertainties in such calculations. For an ideal case the convection coefficient is:

h = 4.5 W / m^2 x °C for convection from one side of the board,
h = 9.0 " " " both sides " .

Cooling fins can be used to increase the convection from high power dissipation components. The fins increase the effective surface area exposed to the air. A further increase in cooling efficiency may be obtained by using a fan to enforce air circulation around the component, see Figure 6.25. The convection coefficient typically increases with air velocity, v, as v^n, where the exponent n increases from 0.33 for v > 1 m/sec (laminar flow) to 0.8 at v < 5 m/sec (turbulent flow) [6.18]. The thermal contact from component packages to the heat sink can be greatly improved by soldering at "thermal vias", i.e. metallised holes from the surface of the PWB to metal core inside, Figure 6.26. Similar thermal vias or metal pillars are used inside ceramic or plastic packages to improve thermal contact from the Si chip to package surface.

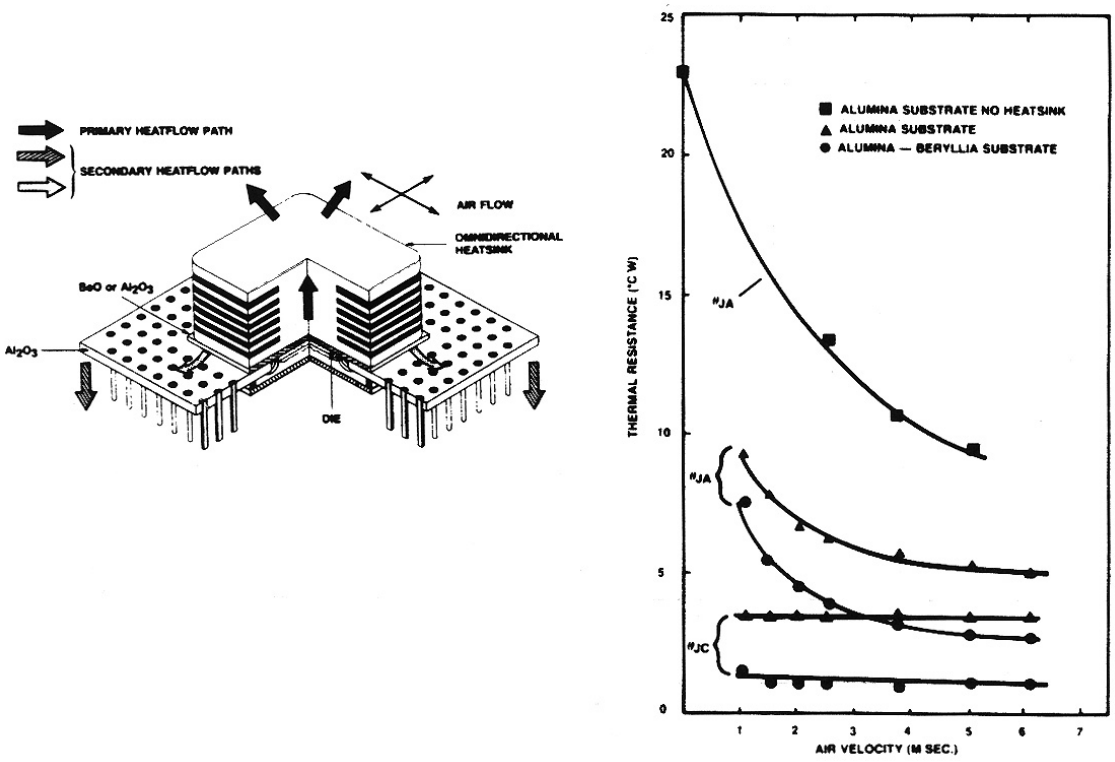


Fig. 6.25: a): Pin-grid package with cooling fins. b): Measured thermal resistance in the component with forced air cooling [6.15].

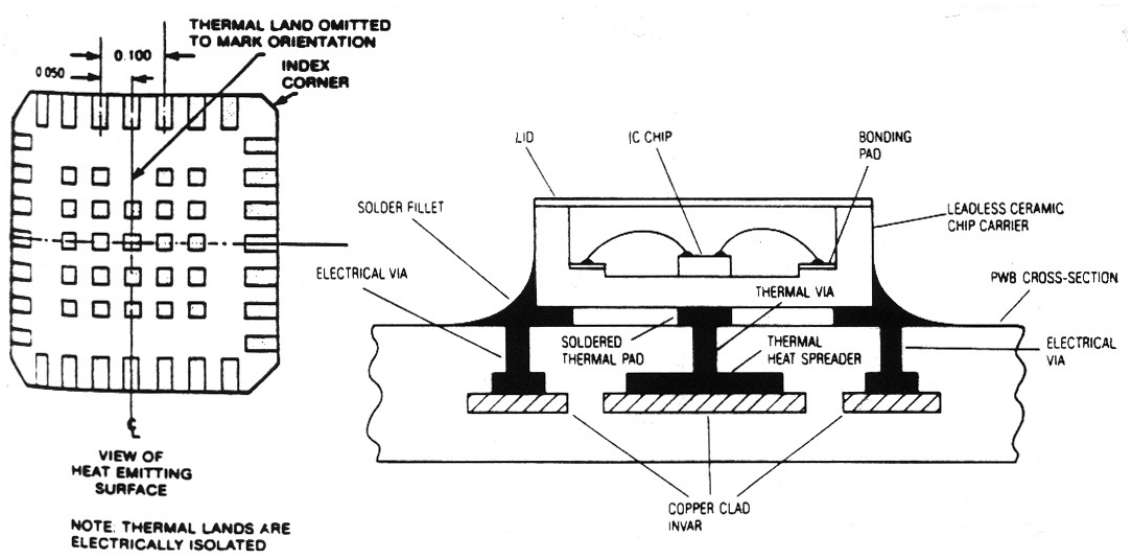


Fig. 6.26: LLCC package with thermal solder lands and thermal vias connected to a metal core in the PCB.

In power electronic applications the component packages are often attached directly to a massive metal cooling fin. A layer of thermal grease or other terminally conducting layer is used between the component and the cooling fins to improve the thermal conduction. See also Section 8.6 on power electronic modules.

More sophisticated cooling technologies utilise other media than air. Helium or fluorocarbon vapour are gases with better cooling properties than air. Liquids such as water, fluorocarbons and oils are used for cooling the backside or edges of the PCB, see Figure 6.27. Evaporation cooling (boiling) with fluorocarbon liquids is the ultimate cooling technology used in some high end computer applications. The convection coefficient obtained is 3 orders of magnitude larger than for air convection, see Figure 6.28. Fluorocarbon liquids with different boiling temperatures are available. The fluorocarbon may either cool the substrate or be in direct contact with the chip surface. Some issues in this technology such as the effect of contaminations in the liquid and corrosion effects are not fully investigated [6.15-6.21].

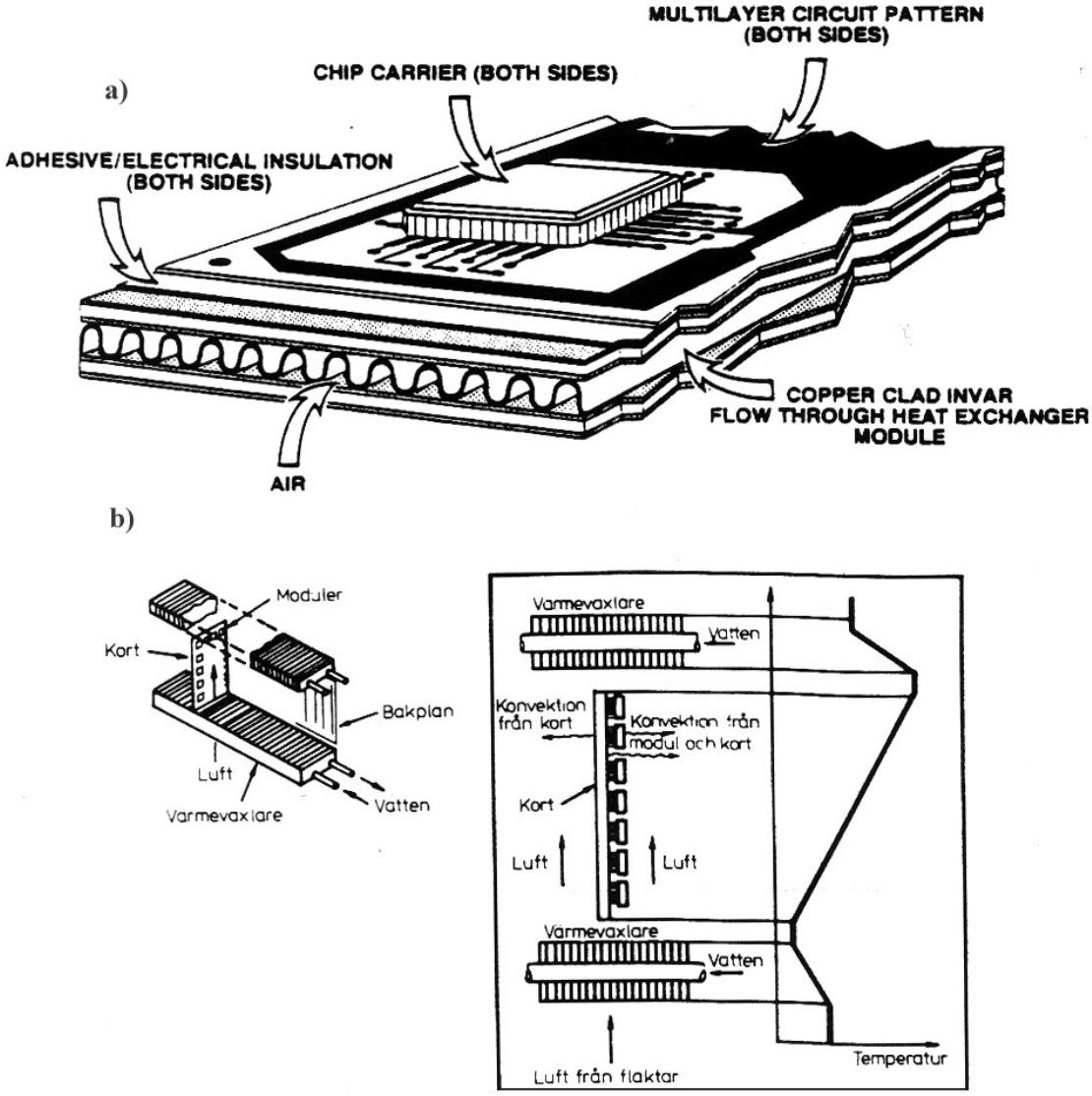


Fig. 6.27: a): Forced air convection in a channel between two PCBs (Texas Instruments),
b): water-cooled heat exchanger for edge cooling of PCBs and temperature distribution (qualitative) [6.18].

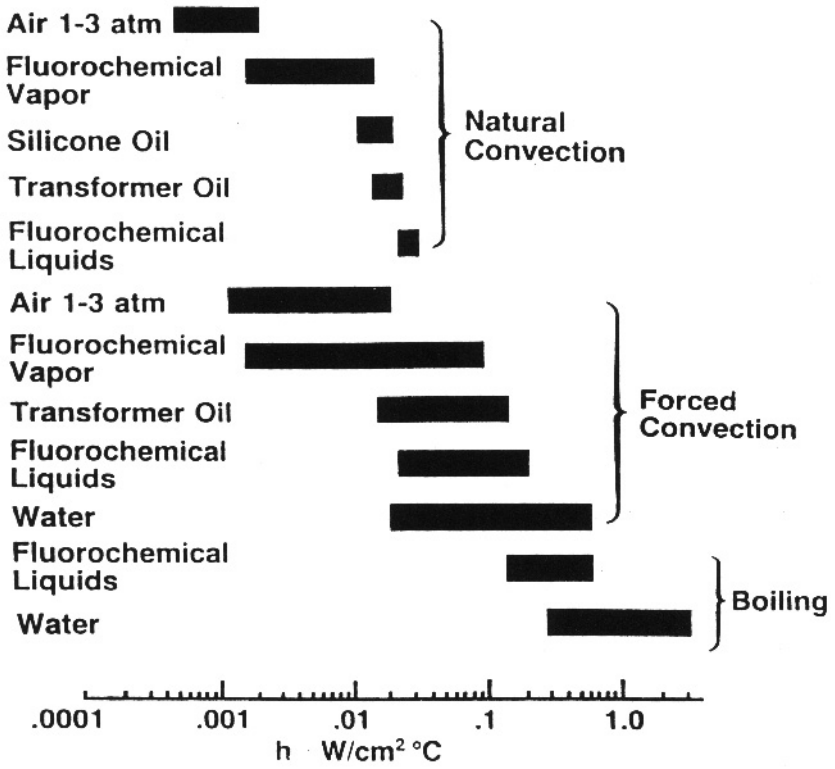


Fig. 6.28: Heat convection coefficient in different cooling media for natural convection, forced convection and boiling [6.15].

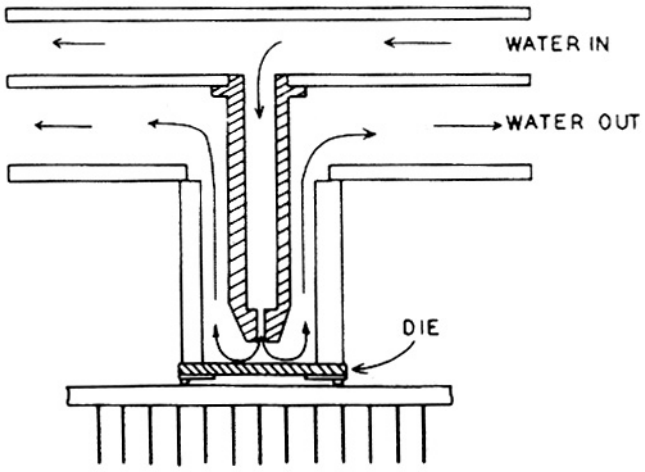


Fig. 6.29: "Microbellows cooling": A jet of water or other cooling liquid impinges on the backside of the chip. The bellow structure is necessary to accommodate thermal expansion [6.32].

Direct liquid cooling by the "microbellows" principle is shown in Figure 6.29. Here a jet of cooling liquid hits the backside of the chip. Thermal resistances of approximately 1 °C/W x cm^2 can be achieved.

An extreme form of cooling, demonstrated in a research environment [6.22], is shown in Figure 6.30. Microscopic grooves are made in the silicon chip from the backside by anisotropic etching. A cooling liquid is forced through the channels, and the liquid is contained in the channels by a cover plate. By this method, thermal resistances in the range of 0.1 °C/W x cm^2 were obtained, and 1 kW power could be removed from a

chip of area 1cm^2. Etching the grooves in a passive Si chip and replacing the cover plate with the active chip only gave a slight reduction in the cooling efficiency.

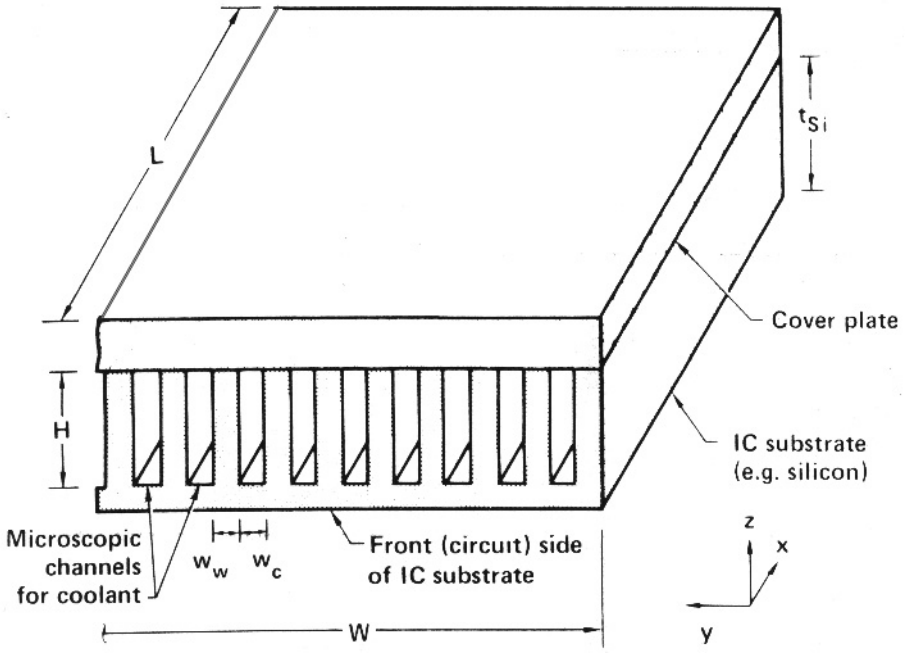


Fig. 6.30: Cooling by forcing liquid through microscopic, etched channels in the semiconductor chip [6.32]. The channels are approximately 400 μm deep and 100 μm wide.

6.6.6 Thermal simulation and measurement

There are many software packages available for numerical simulation of the thermal behaviour of electronic systems. Some of these programs are general thermal simulation programs, others are specialised for electronics [6.15,6.18]. The general programs usually require more effort from the designer during the input of geometry data and material properties than the specialised programs. However, a general program may offer more design freedom and possibilities for special analysis.

The input data to thermal simulation programs may be divided into three groups: Geometry data, boundary conditions and material properties. Geometry data are generated by defining points, curves, surfaces and volumes in a thermal CAD system. The geometrical model has to be divided into nodes and elements. This is usually done automatically in modern programs and is otherwise very time consuming.

Boundary conditions are convection coefficients and heat sink/ambient temperatures. Material properties are often contained in a material library in the program. A common source of error in thermal simulation is the use of erroneous input parameters such as an effective convection coefficient or material property. The latter is often due to the fact that bulk material properties are different from the thermal properties of the specially processed materials encountered in electronic packages and substrates. In addition, the interfaces between different materials are difficult to model properly in these programs. Some experimental data and experience are usually required in order to obtain satisfactory results when material interfaces make a significant contribution to the thermal resistance.

Presentation of the results is usually done by showing the model on a computer display with different colours representing different temperature ranges, showing isothermal lines or temperature bars at selected points, see Figure 6.31.

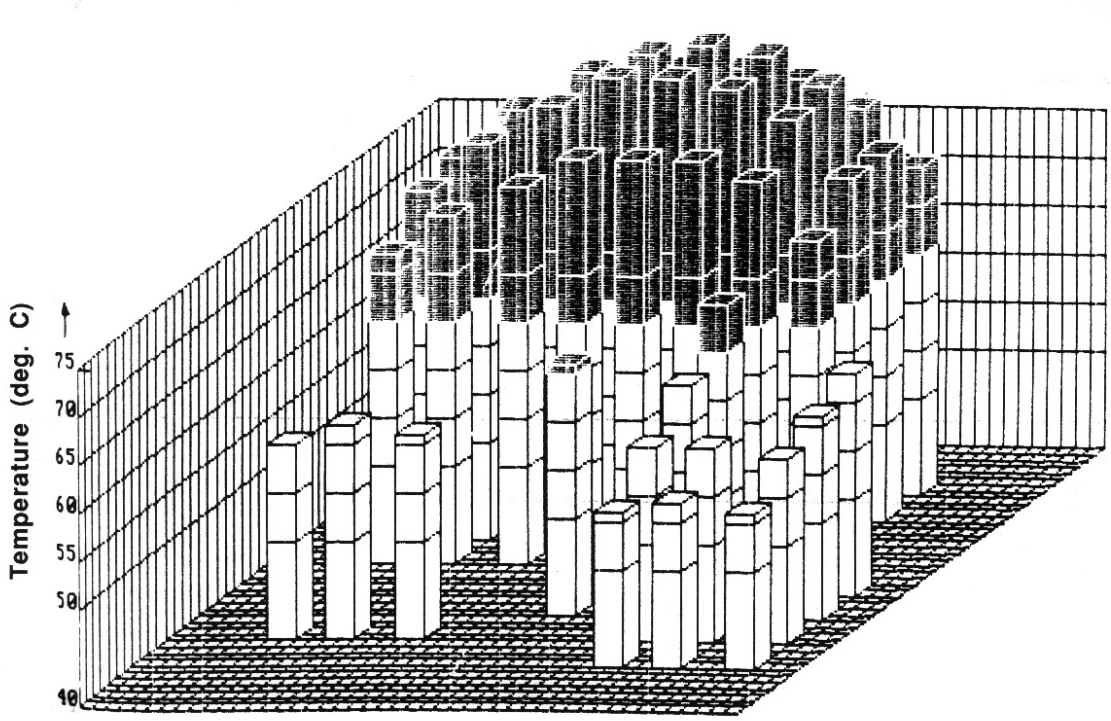


Fig. 6.31: Bar diagram for calculated temperatures on each component chip by the thermal simulation program TMOD [6.18].

Results from thermal simulations may be checked by using an infrared imaging system. When using such a system care should be taken to calibrate it properly, because the different materials have different optical emissions. The temperature may also be measured at specific positions by using thermistors or thermocouples.

6.6.7 Selection of cooling methods

Insufficient cooling of electronic systems leads to problems with low reliability and reduced lifetime. On the other hand a complicated cooling systems may be very costly.

Some cooling methods arranged according to increasing cost and complexity are:

- Use of low power components (CMOS) and design methods.
- Optimal placement of high heat dissipating components.
- Cooling fins on single components.
- Improved thermal properties of the substrate: Metal core board, heat sinks along edges, change to alumina/thick film module.
- Forced air cooling with fan.
- Indirect liquid cooling.
- Direct liquid cooling with components immersed in the liquid.

More details of thermal design are given in [6.15-6.18].

6.7 HIGH FREQUENCY DESIGN

Transmission line- and other high frequency design principles are gaining increasing importance due to the increasing speed of integrated circuits. Only a brief summary of the basic principles will be given here due to the size and complexity of this field. Thorough treatments can be found in [6.16, 6.22, and 6.32].

High frequency design should be employed if the cycle time of analogue signals, or rise time of digital signals, t_r, is comparable to t_f. Where t_f is the time-of-flight delay of a signal over the length l of the critical paths on the board/circuit. As a rule of thumb transmission line phenomena become significant when [6.32]:

$$t_r < 2.5\ t_f. \qquad \text{Eq. 6.1}$$

where t_r = 10 - 90 % rise time, and $t_f = l/v$

and v is the propagation speed for the signal.

The high frequency design methods are based on calculation of the electromagnetic field in the vicinity of the electrical conductors, solving the "Telegrapher's equation" [6.32]. The conductors are modelled by distributed electrical inductance, capacitance and resistance, see Figures. 6.32 - 6.33. The distributed electrical parameters depend on the geometry of the conductor and its position relative to ground and power planes, besides the materials used.

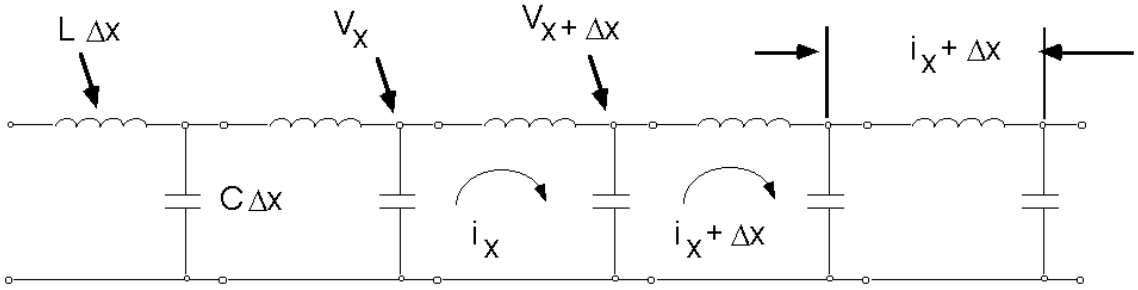


Fig. 6.32: Distributed parameters in a model of a loss free transmission line. C and L are capacitance and inductance per m length.

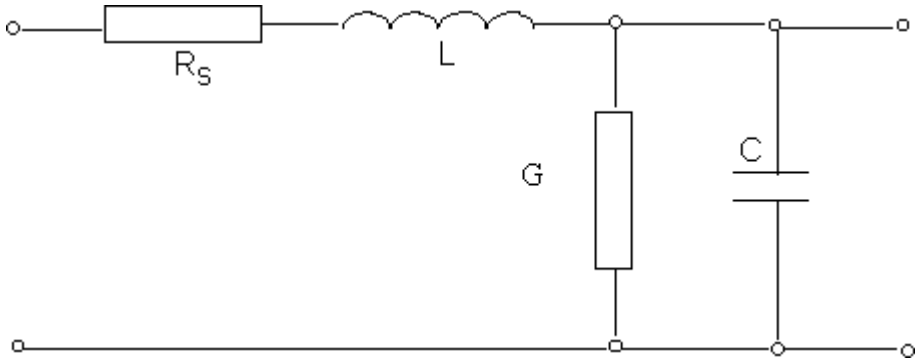


Fig. 6.33: The analogous lossy line contains a conductor series resistance R and dielectric loss conductance G, both per m length.

If a step voltage with respect to ground propagates along an infinitely long, uniform signal line, the transmission speed is given by:

$v = c/\varepsilon_r^{1/2}$

where c is the speed of light in vacuum, ε_r is the *effective* relative dielectric constant of the media surrounding the conductor, see below. Table 6.11 shows how far a signal travels in 1 nanosecond in different media.

Table 6.11: Signal propagation speed in different media.
$v = c_0/(\sqrt{\varepsilon r}) = 30$ (cm/ns)/$\sqrt{\varepsilon r}$

Dielectric	Relative dielectric Constant (ε_r)	Propagation Speed (v) (cm/ns)
Polyimide	2,5 - 3,5	16 - 19
Silicon dioxide	3,9	15
Epoxy glass (PC board))	5,0	13
Alumina (ceramic)	9,5	10

The current I and the voltage V are related by:

$V = Z_o I$.

The fundamental quantity Z_o is the characteristic impedance:

$$Z_o = ((R + j\omega L)/(G + j\omega C))^{1/2}$$

where:
ω = angular frequency
R = resistance of the conductor per unit length
L = inductance per unit length
C = capacitance per unit length
G = loss conductance in dielectric per unit length.

In a loss free medium:

$$Z_o = \sqrt{L/C}\ .$$

An electrical signal travelling through a discontinuity between media 1 and 2 is reflected with a coefficient of reflection given as:

$$R = (Z_1 - Z_2)/(Z_1 + Z_2)$$

where Z_1 and Z_2 are the characteristic impedances in the two media. When the reflected signal reaches a discontinuity in the other end, it is reflected again. These superimposed reflected signals may lead to a logical error at worst, see Figure 6.34.

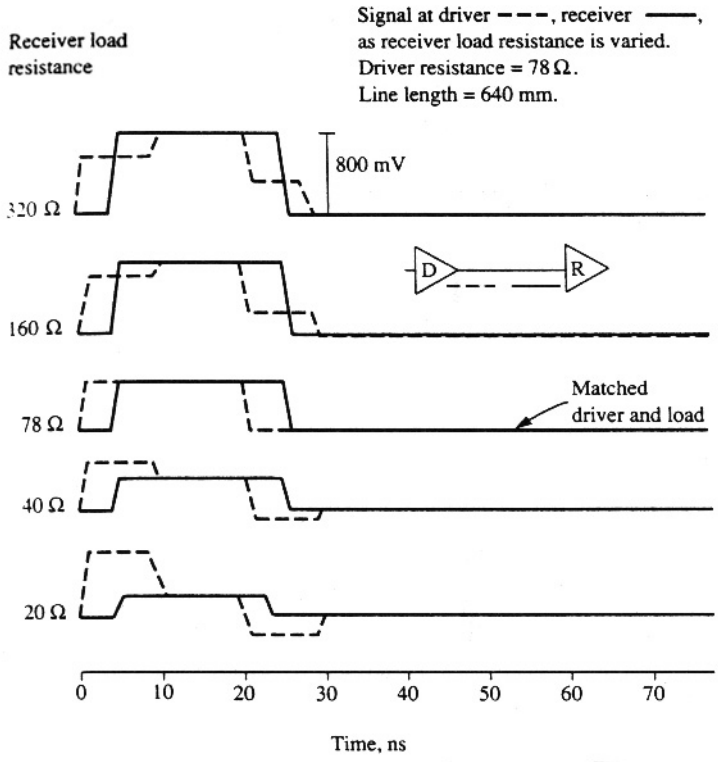


Fig. 6.34: Distorted signal as a function of time when the transmitter has 78 ohms impedance and the receiver has different impedances as indicated. If the receiver also has 78 ohms impedance the signal at the receiver is a time delayed replica of the transmitted signal [6. 22 b)].

An electrical conductor should be treated as a transmission line if the condition of Eq. 6.1 applies. On PCBs this is typically the case for clock frequencies above 50-100 MHz. It also depends on conductor lengths and materials. The effects may have to be considered in circuits operating at lower clock frequencies for fast ICs with steep pulse flanks. At even higher frequencies also sharp bends on cables, and via holes, may affect the transmission of signals.

An un-terminated conductor should normally be terminated by a resistor with the same resistance as the characteristic impedance and as close as possible to the end of the conductor.

Common geometries for transmission lines are cylindrical and rectangular coaxial structures, coplanar, microstrip, stripline, and derived structures, see Figure 6.35. In all the geometries, one or two ground plane(s) will be located close to the signal conductor in order to confine the electrical field. Capacitance and inductance are related to geometrical dimensions and material properties in a complex manner for most geometries. The effective relative dielectric constant is determined by the dielectric underneath the conductor as well as the air, in case of microstrip geometry. Usually numerical calculations are necessary to calculate the Z_o but some approximate analytical results are available, see Figure 6.36 and [6.22 - 6.23]. The relationship between Z_o and other parameters is shown in Figure 6.37. Z_o may also be frequency- and temperature dependent due to temperature dependence of the dielectric properties, please refer to Figure 5.14. In a production environment tolerances in Z_o must be considered, due to limited standard values in thicknesses, and tolerances in linewidths, thicknesses, dielectric constant, etc.

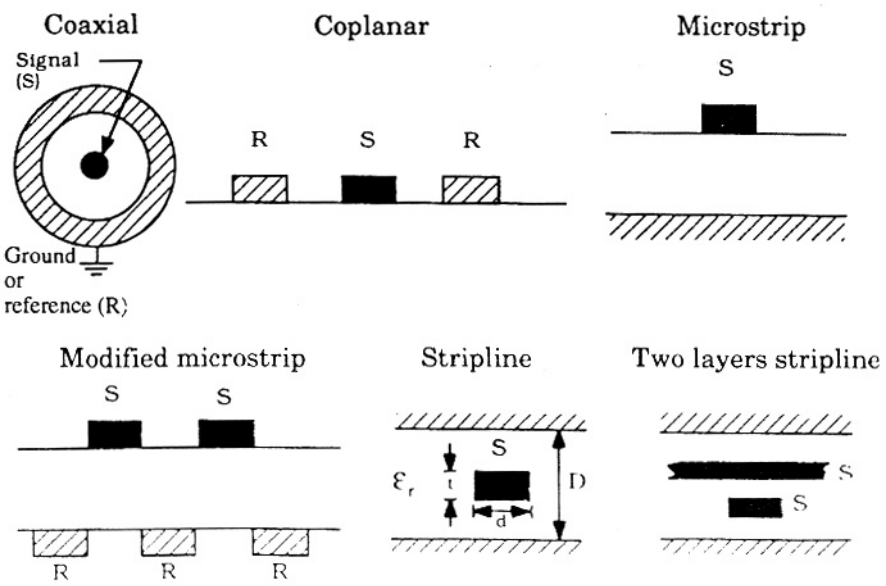
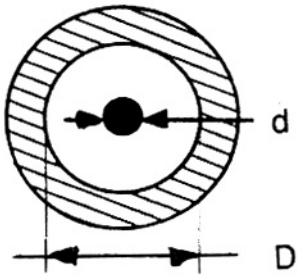


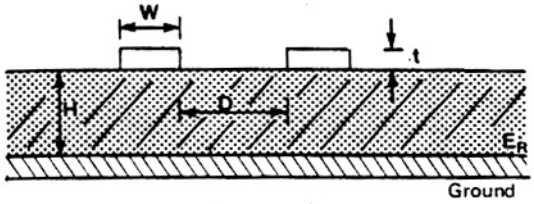
Fig. 6.35: Geometries for obtaining a controlled characteristic impedance.

The typical configuration in a multilayer PCB or hybrid module is microstrip outer signal layer and buried microstrip or stripline inner layers with possibilities of using two signal layers between a set of ground planes. Standard values, most often used for characteristic impedance, are 50, 75 and 95 ohms.



COAXIAL

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \frac{D}{d}$$



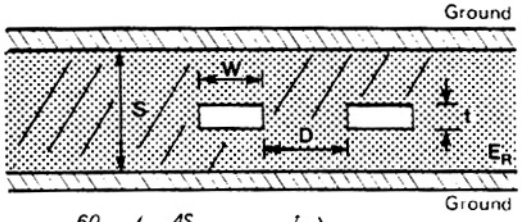
MICROSTRIP

$$Z_O = \frac{87}{\sqrt{E_R + 1.41}} \ln\left(\frac{5.98H}{0.8W + t}\right) \Omega$$

$$T_{PD} = 0.08471\sqrt{0.475E_R + 0.67}\ \text{nsec/in}$$

$$C_O = \frac{T_{PD}}{Z_O}\ \text{pF/in}\quad T_{PD}\ \text{in nsec/in}\quad Z_O\ \text{in K}\Omega$$

$$X_{TALK} \alpha \frac{1}{D} \cdot H$$



STRIPLINE

$$Z_O = \frac{60}{\sqrt{E_R}} \ln\left(\frac{4S}{0.67\Pi w}(0.8 + \frac{t}{w})\right) \Omega$$

$$T_{PD} = 0.08471\sqrt{E_R}\ \text{nsec/in}$$

$$C_O = \frac{T_{PD}}{Z_O}\ \text{pF/in}\quad T_{PD}\ \text{in nsec/in}\quad Z_O\ \text{in K}\Omega$$

$$X_{TALK} \alpha \frac{1}{D} \cdot S$$

Fig. 6.36: Expressions for characteristic impedance, Z_o, signal propagation speed, T_{PD}, capacitance per unit length, C_o, and crosstalk, X_{Talk}, in different geometries: a) coaxial, b) microstrip, c) stripline [6.22 a)]. The expression for coaxial geometry is exact, the others are approximate and valid only in certain parameter ranges.

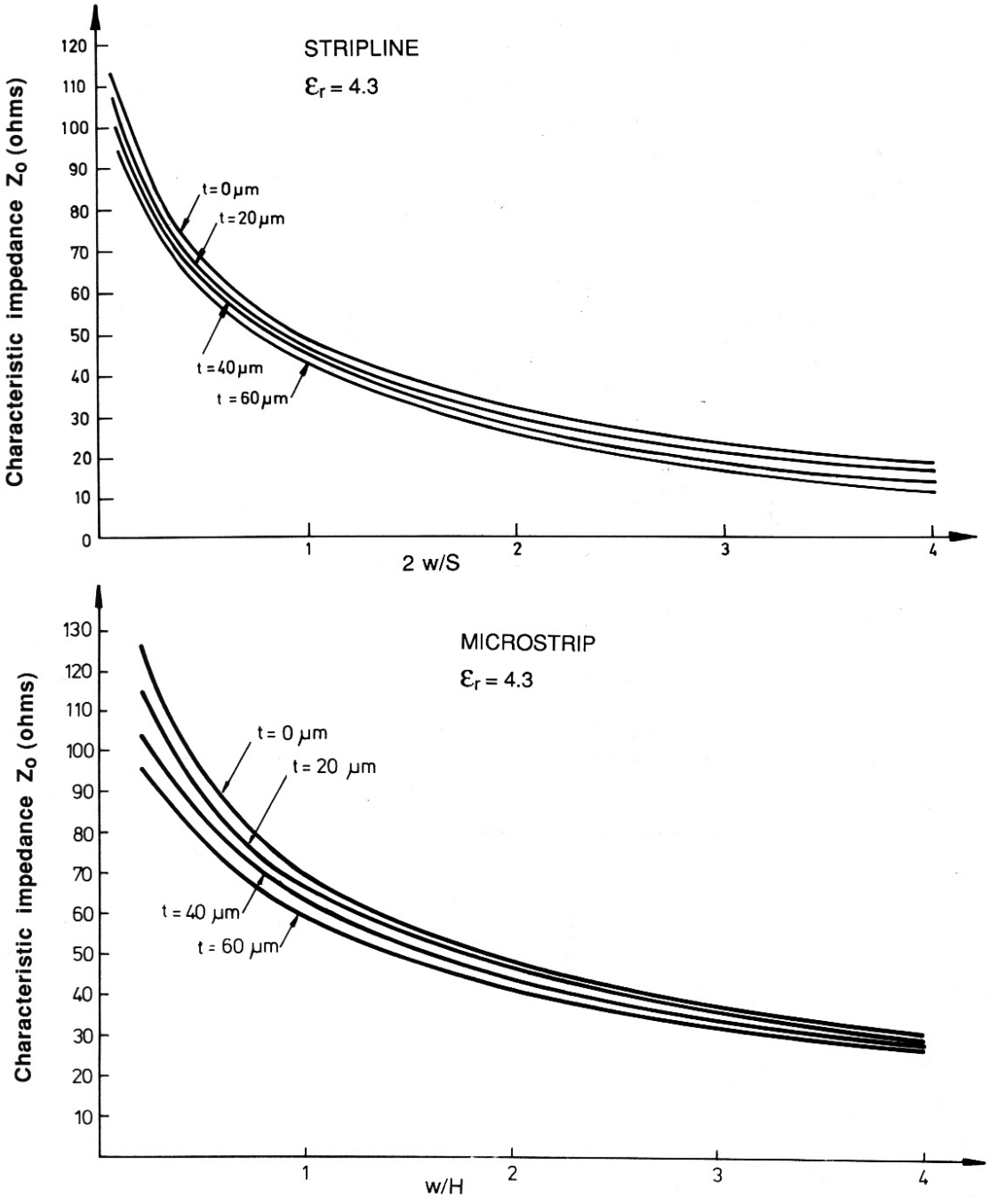


Fig. 6.37: Dependence of the characteristic impedance on geometric dimensions, for a) stripline and b) microstrip. w is the signal conductor width, S is the distance between ground planes for stripline, and H the distance between signal conductor and ground plane for microstrip (please refer to Figure 6.35). Curves are shown for different signal conductor thicknesses, t [6.9].

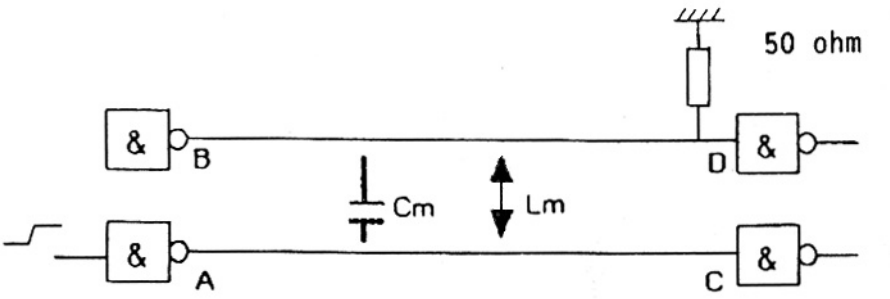


Fig. 6.38: Cross talk: A signal from A to C is transmitted to the B - D line and gives noise in B (backward or near end cross talk) and in D (forward or far end cross talk).

Small spatial separation between conductors results in capacitive and inductive coupling between the conductors and potential problems with cross talk, see Figure 6.38. Cross talk is the main consideration when defining minimal line separation for high frequency circuits. Forward cross talk is propagated in the same direction as the source signal and backward cross talk in the opposite direction, Figure 6.39 [6.16, 6.22 b]. Cross talk and reflections are different types of noise.

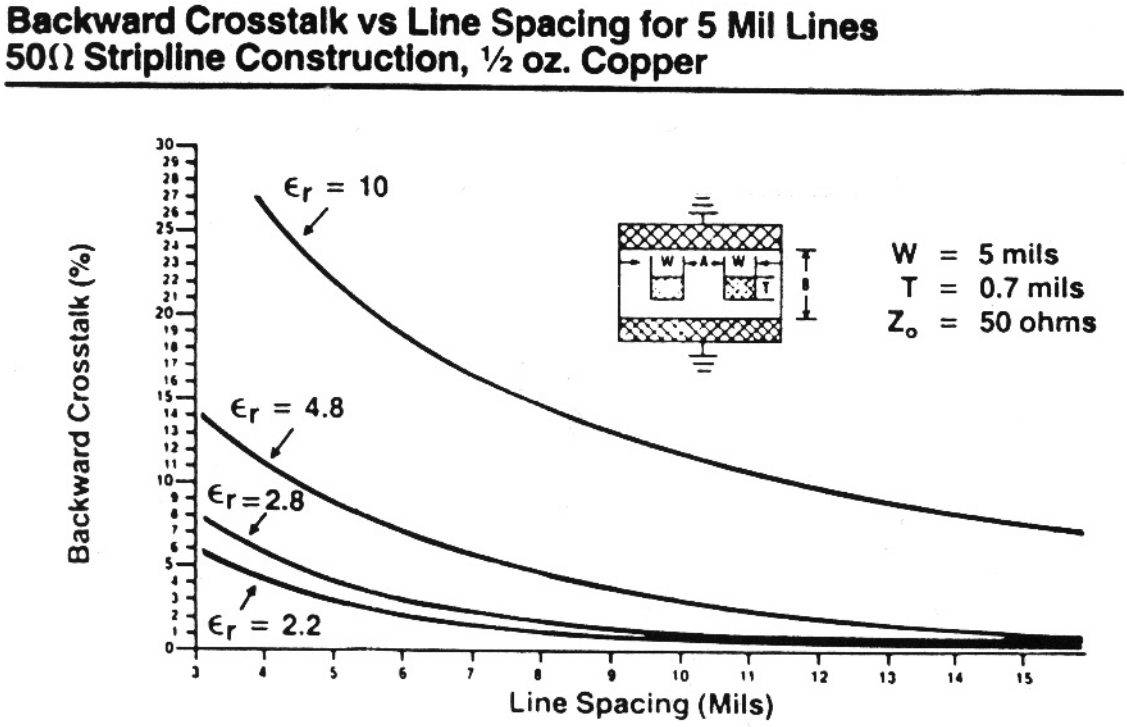


Fig. 6.39: Backward cross talk as a function of conductor separation in stripline geometry in different dielectrics. The effect increases with increasing ε_r and decreases with increasing conductor separation [6.24].

A third kind is switching noise. If the electrical current in a component is suddenly changed there will appear a transient signal on the power supply line due to the inductance in it. This type of noise may also lead to logical errors or delays [6.16]. It is important to ensure a high electrical conductivity in ground planes and power supply conductors [6.16, 6.33]. Decoupling capacitors between ground and power supply close to critical components are also important, to absorb current spikes without corresponding voltage spikes.

Losses also have to be considered. The losses may be described by the attenuation of the signals [6.16]. The signal attenuation between points a and b, separated by a distance l of the conductor, is given as:

$$V_b = V_a \exp(-\alpha l)$$

where α is the attenuation coefficient.

The attenuation is related to ohmic-, skin- and dielectric losses (with attenuation coefficients α_r, α_s, α_d respectively).

$$\alpha = (\alpha_r, \alpha_s) + \alpha_d .$$

In the parenthesis α_r dominates at low frequencies. α_s dominates at very high frequencies (GHz) where the skin depth d_s is much smaller than the conductor cross section. Simplified expressions for each parameter are [6.32]:

$$\alpha_r = R / (2Z_o)$$
$$\alpha_s = (\pi \mu_o f \rho)^{1/2} / (w Z_o) \qquad \text{for } \delta_s = (\rho / \pi f \mu_o)^{1/2} << t$$
$$\alpha_d = \pi (\varepsilon_o \varepsilon)^{1/2} f \tan\delta / c$$

where:
R = ohmic resistance per unit length,
ρ = electrical DC resistivity in the conductor,
$\tan\delta$ = dielectric loss tangent (please refer to Section 3.2.3),
w =conductor width, and t = conductor thickness.
c = speed of light ($3 \cdot 10^8$ m/s)

An increased rise time for a step signal is also among the consequences of lossy lines, because the high frequency signal components are attenuated more than the low frequency components, as shown in the expressions for α_d and α_s. Figure 6.40 shows the skin effect in copper conductors and Figure 6.41 shows a comparison between conductor- and dielectric losses in multilayer thin film multichip modules (MCMs).

High frequency design of PCBs and hybrid modules presents new demands on designers and manufacturers. The layout of the PWB must be properly controlled. CAD software for high frequency design is still in its infancy. Materials and dimensions must be selected and controlled in close co-operation with the manufacturer.

Manufacturing of high frequency PCBs gives tough demands on tolerances for conductor width and thickness of dielectric layers between conductors and ground

planes. These dimensions determine the characteristic impedance and its tolerances. It is necessary to use materials with lower dielectric constant and loss than FR- 4. Special methods are used to obtain fine lines with high accuracy. They were briefly described in Chapter 5.

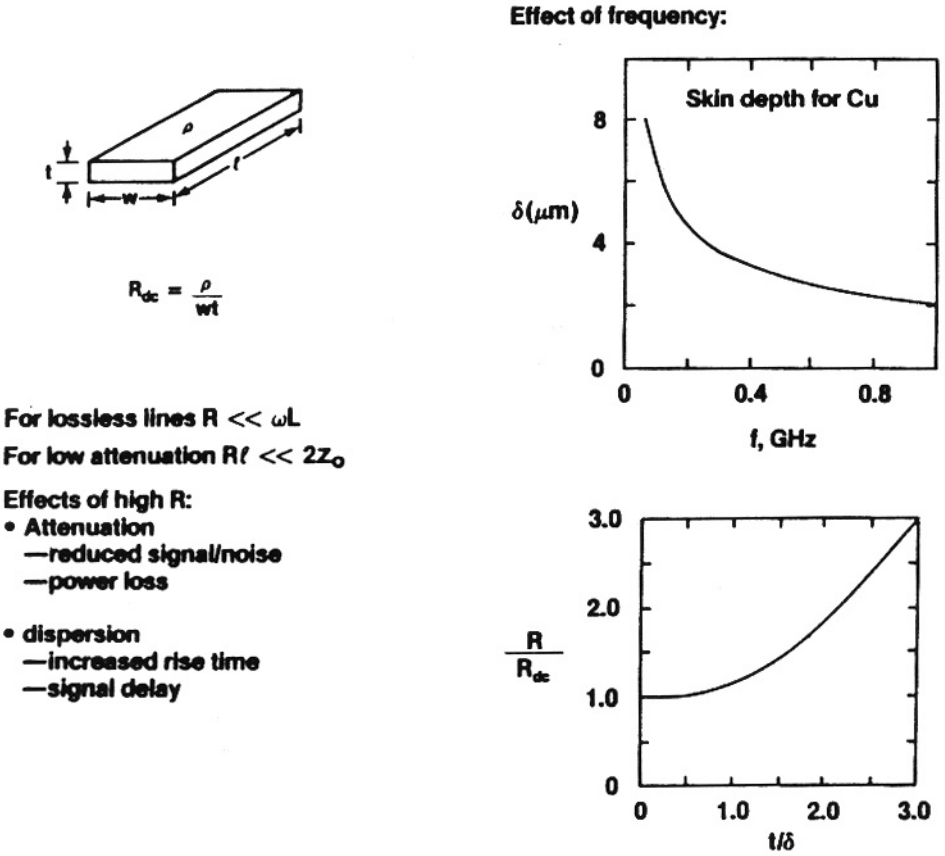


Fig. 6.40: High frequency skin depth for copper, and conductor resistance due to skin effect, relative to the DC resistance [6.19]. The resistance has increased by approximately a factor 2 when the skin depth δ is one half of the conductor thickness t.

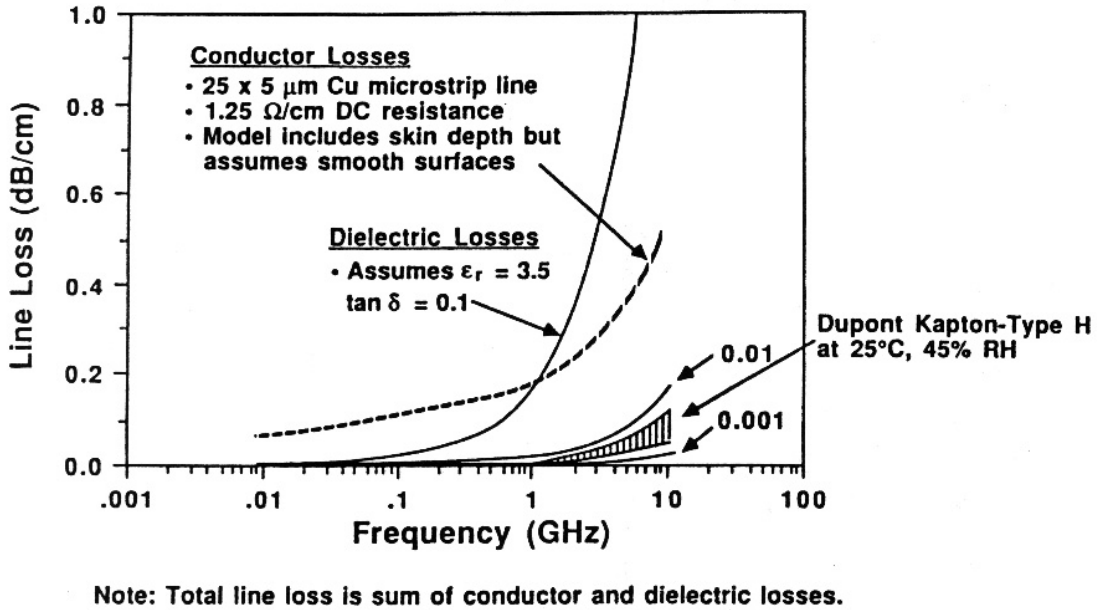


Fig. 6.41: Conductor- and dielectric losses as functions of frequency for multilayer thin film modules [6.19].

6.8 DESIGN OF FLEXIBLE PRINTED CIRCUITS

As mentioned in Section 5.12 the primary applications of flexible printed circuits are compact packaging in 3 dimensions, interconnection to moving parts, advanced flat cables, membrane switch panels. Design of regular flex boards is discussed below, membrane switch panels are described in Section 6.9.

The base material for flex boards is normally polyimide. Polyester may also be used if soldering can be avoided. These materials were briefly discussed in Section 3.3, and some data for the base materials were shown in Table 5.4.

Direct conversion of rigid PCBs to flex boards is usually not an optimal design procedure. The 3-dimensional aspect should be considered from the beginning of the design. Simple models cut from a piece of paper may be helpful for visualisation of the shape.

The flexible materials will typically shrink 0.2 % during processing compared to 0.05 % for FR-4. This has to be considered during the design work.

Determination of minimum dimensions of conductors with large current loads was shown in Figure 6.2 for ordinary PWBs and is also valid for flexible PCBs (flex prints). The adhesion between copper foil and base material is not so good as than for rigid PCBs and is further reduced for conductor widths below 0.5 mm. Generally, as wide conductors as possible should be used in order to ensure the best possible stability and production yield.

Sharp bends will reduce the reliability due to fatigue in the copper, Figure 6.42. The minimum bending radius depends on whether the flex print will be bent only once during installation (e.g. electronics of a compact camera) or if the bends are dynamic (such as the writing head of a typewriter or in a computer printer. If possible, only one conductor layer should be used in the bending zone and the copper layer should be in the middle of the flex print. In a multilayer flex print the copper layers should not be directly on top of each other in the bending zone [6.25-6.26]. Conductors should be oriented perpendicularly to the bend.

The flex print is shaped by cutting with a numerically controlled knife or with excising, depending on production volumes. Sharp corners on the copper foil or base material may lead to tearing of the foil and should be avoided, Figure 6.43.

If through hole mounted components are attached to flex prints then a rigid material should be used beneath the component to increase strength and solderability. Such rigid sections are also used for other purposes. They may simply be pieces of rigid plastic sheets or single- or multilayer boards. The flexible parts may be simple interconnection parts or they may be complete wiring boards. Components should not be attached to the moving parts of a flex print.

Configuration of conductors	Cycles to failure		
	Radius of curvature		
	R = 5 mm	R = 10 mm	R = 20 mm
	140	380	1800
	220	700	4000
	80	250	800
	140	400	1800

Fig. 6.42: Bending of double layer flexible print with different conductor layout. The Figure shows the number of cycles before failure with 5, 10 and 20 mm bending radius and 180° angel of bending. (Data: Schoeller Elektronik). If the copper layer in the bending zone is strained 16 % or more it is likely to fail during the first cycle.

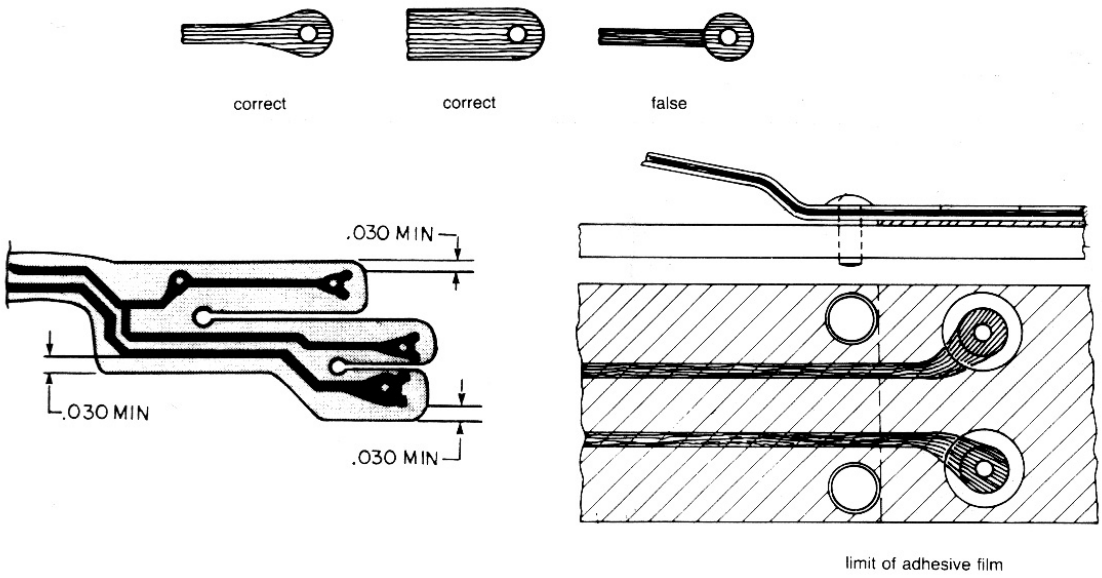


Fig. 6.43: a): Solder lands on flexible prints should be rounded in order to reduce the possibility for failures, b): The contour of the board should be rounded in order to reduce possibilities for tearing (dimensions in inches). The "rabbit ears" on the ends of the metal foil is for obtaining better adhesion to the polyimide. c): Plastic rivets should be used to avoid sharp bends in the interface between the flexible and the rigid parts of the PCB.

The polyimide flex prints can be soldered by wave-, reflow- or hand soldering. Soldering and positioning of components usually require special tooling that must be considered during the design work.

Interconnection of flex prints is done by spring loaded mechanical connectors, soldering or use of conductive adhesives.

Vibration testing is often important because the flex prints are usually free to move during operation.

Flex prints typically have a 2 - 3 times higher cost than comparable rigid PCBs.

More details regarding applications, design and fabrication are given in [6.3 and 6.25 - 6.28].

6.9 DESIGN OF MEMBRANE SWITCH PANELS [6.31]

A printed keyboard or membrane switch panel (please refer to Section 5.12) is a part of the interface between the electronic equipment and the user. The main electrical function is switching, but it may also include an LCD display or light emitting diodes (LED's) for information to the user. Design and production of these panels is a speciality and there should be a close co-operation between the designer and the manufacturer.

It is important to define user specifications such as: indoor/outdoor use, minimum and maximum operating temperatures, reliability requirement, atmospheric conditions, etc. These specifications influence the selection of materials and design rules. If displays, back lighting (Figures 6.44, 6.45), windows, etc. are needed then this should be considered from the beginning of the design.

The standard parts of a membrane switch panel were shown in Figure 5.21, and a more complex type is shown in Figure 6.44. The panel is attached to the front panel of the equipment with an adhesive bottom foil. The top layer includes informative text and graphical information made by screen printing. The two electrically active layers are made by screen printing of electrical conductors and contact pads with a silver based polymer thick film technique (see Section 8.3). The electrical layers are separated with spacers. Normally, such a switch panel will endure some 5 million activation's of any switch. If metal domes are used for the switches the expected lifetime will typically be 1-2 million activation's [6.31].

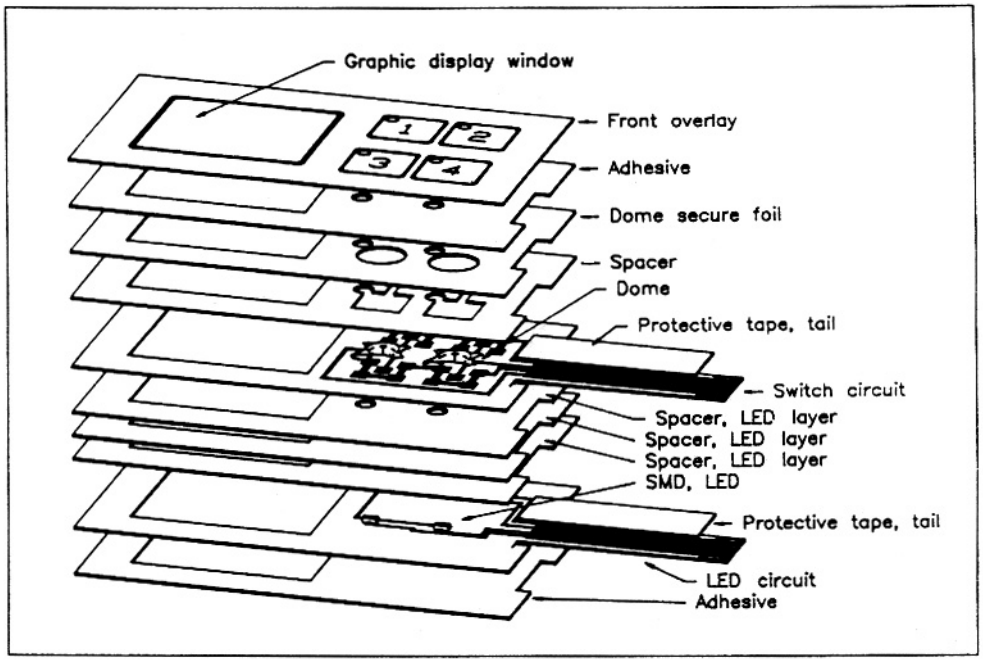


Fig. 6.44: Detail of a membrane switch panel. The tail with interconnections to the panel is protected with a laminated foil. Light emitting diodes may be attached with conductive adhesive. Screen printed polymer thick film series resistors may be used [6.31].

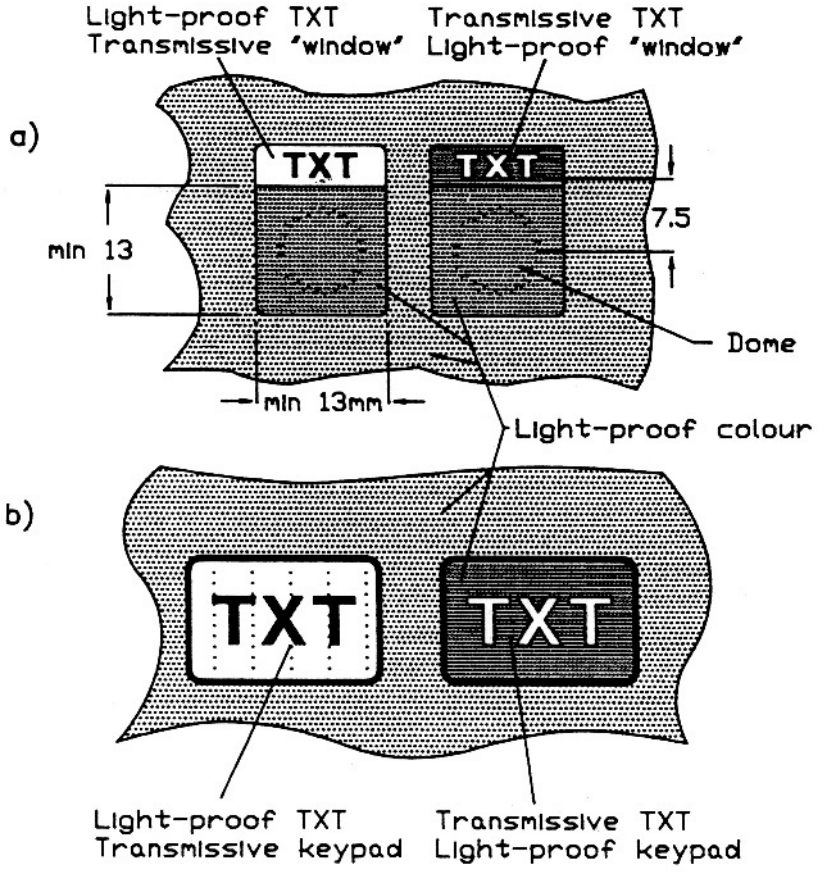


Fig. 6.45: Contact areas of membrane switch panel with back lighting and window. Examples of lighted text on a dark background and the opposite combination. If a metal dome is used the information has to be next to the key and not underneath it [6.31].

If necessary, several layers of electrical conductors may be printed on top of each other with electrical insulation in between (Section 8.3).

The most common cause of failure is mishandling. Short circuits due to silver migration [6.31] may also occur if humidity is penetrating into the switch panel. The panel itself is well protected by many protective layers outside the electrically active layers. However, the "tail" or connector between the panel and the outside world, see Figure 6.44, is a weak point.

LED's may be included in the keys for information purposes. The LED's are attached with conductive adhesive because the polyester material will not withstand the temperatures of a soldering process.

Further details of membranes with panel technology and design are given in [6.31].

6.10 SYSTEM LEVEL MODELLING

In the early phase of the development of a complex electronic product the emphasis is on over-all specifications and performance of the system, division into suitable subsystems and choice of packaging technology for each subsystem. Computer models have been developed to simulate the whole system, with the freedom to test out various technologies for each subsystem and change the content in each subsystem. We shall only briefly mention one such model, SUSPENS [6.32]. Each IC technology is defined by parameters describing delay, minimum dimensions, line resistance and capacitance, power per gate, etc. Chip architecture is also characterised. Based on the number of logic gates per chip the no. of I/Os and the average interconnection length are calculated via Rent's rule. The chip size can be calculated, as well as maximum clock frequency, power consumption, etc. Module- and board technologies, likewise, are defined by their characteristic parameters.

In this way a hierarchical model is built. "What if "- questions can be tested by changing an important technology parameter (e.g. CMOS minimum line width) changing technology for a block in the model (e.g. replace thick film hybrid technology by thin film MCM technology), etc. The consequence for the over-all system performance can be analysed by comparing for various conditions such parameters as maximum system clock frequency, computational capacity, packing density, power dissipation density and over-all power dissipation, cost indicators, etc. Figure 6.46 shows the SUSPENS model schematically. This kind of system simulation is expected to gain increasing importance.

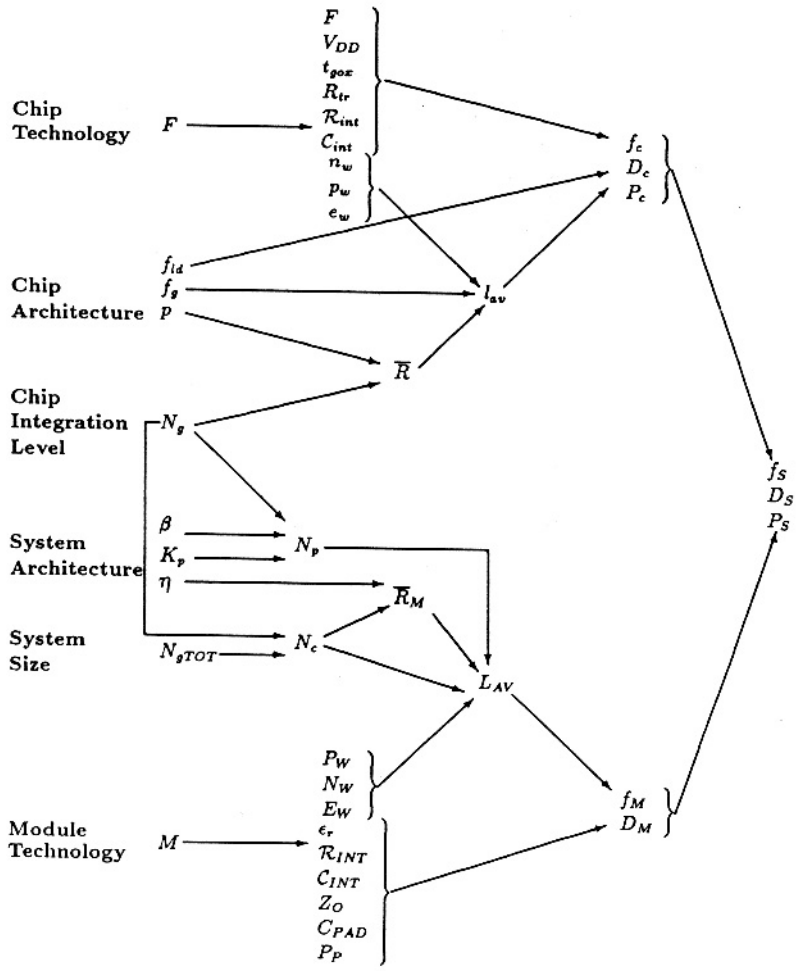


Fig. 6.46: The SUSPENS model for the different levels in an electronic system. The symbols are parameters characterising the system and different technologies of the system. They are quantified and used to compare or optimise different possible versions of the system in computer calculations [6.32].

REFERENCES

[6.0] Among the large number of EMC standards we shall just mention:
a) CISCR, Publication 22: "Limits and methods of measurements of radio interference characteristics of information technology equipment". The European norm EN 55022 is based on this standard. They cover emission.
b) IEC Publication 801 - 1 to - 5, as well as EN 55020: "Immunity from radio interference of broadcast receivers and associated equipment" cover immunity.
c) EEC Directive KOM (87) 527 and KOM (88) 548 final (2) cover both emission as immunity.
d) CENELEC TC 110 is responsible for further standards.
e) Some principles of EMC design are described in P. Krebs and H. G. Nissen: "EMC handbook part 3: EMC considerations in PWB layout". Technical report, ElectronikCentralen ECR-224, 1989 (in Danish).

[6.1] G. Leonida: "Handbook of printed circuit design, manufacture, components and assembly". (Electrochemical Publications, 1981.)

[6.2] C. Lea: "A scientific guide to surface mount technology". (Electrochemical Publications, 1988.)

[6.3] C. F. Coombs: "Printed circuits handbook". (3rd Ed., McGraw Hill, 1988.)

[6.4] ANSI/IPC-SM-782: "Surface Mount Land Patterns". (IPC, March 1987.)

[6.5] L. Halbo m. fl.: "Handbook for design and production of surface mounted PCBs". (ABB Handbook, 1986, in Norwegian.)

[6.6] "SMD-Technology: Guidelines for Footprint Design". (Philips Components, 1989.)

[6.7] "An Introduction to Surface Mounting", and "PCB Layout Recommendations". (Siemens, 1986.)

[6.8] S. Hinch: "Handbook of Surface Mount Technology". (Longman, 1988.)

[6.9] C. G. Bergendahl og H. Svard: "SMT Handbook, Chapter 3: Design". (IVF-report 87606, Sveriges Mekanforbund 1987, in Swedish.)

[6.10] "Tape Automated Bonding at EM Marin". Design rules, 1987.

[6.11] L. Halbo m. fl.: "Second Generation SMT". EPF-report R 29, 1989. (In Norwegian.)

[6.12] A. Gabrielsen m. fl.: "In-circuit test of SMT PCBs". EKF-report R 60, December 1987. (In Norwegian.)

[6.13] J. Wangensteen: "SMT testing". EKF-report R 43, March 1986. (In Norwegian.)

[6.14] a): G. Stensjø: "SMT Handbook Chapter 5: Control and testing." (IVF-report 87620, 1987. In Swedish.)
b): COMETT INSIGHT course: "Modern Trends in Digital Testing". J. McClean, Heriot-Watt University 1993.

[6.15] L. Halbo et al.: a): "Termal design of PCBs". EKF-report R 42, 1986. b): "Environmental tests on surface mount PCBs of different structures". EPF-report R 19, 1987. (In Norwegian.)

[6.16] R. Tummala and E. J. Rymaszewski: "Microelectronics Packaging Handbook". (Van Nostrand, 1989.)

[6.17] a): G. Ellison: "Thermal computations for Electronic Equipment". (van Nostrand, 1984.)
b): A. D. Krauss and A. Bar-Cohen: "Thermal analysis and Control of Electronic Equipment". (McGraw-Hill, 1983.)
c): D. J. Dean: "Thermal Design of Electronic Circuit Boards and Packages". (Electrochemical Publications, 1985.)
d): F. Rasmussen et al.: "Thermal design", EKF-report R 69, 1989. (In Norwegian.)

e): L. Jensen et al.: "Thermal conduction in electronics". EKF-report R 55, 1988. (In Norwegian.)

[6.18] a): G. Floodman and A. Sihlbom: "Handbook for thermal design". IVF-report 88822, 1989. (In Swedish.)
b): A. Sihlbom og H. Svard: "Mätteknik for measuremen of temperature in electronics". IVF-report 87615, 1987. (In Swedish.)

[6.19] R. Jensen: "Materials and Processes for Thin Film Multilayer Multichip Packaging". Presented in CEI-Europe Elsevier "Course on Advanced Semiconductor Packaging", Garmish, November 1988.

[6.20] T. Dewey: "Developments in Liquid immersion Cooling". Electronics Packaging and Production, April 1988, p. 59.

[6.21] P. Øhlckers: "Thermal design". Technical report, 1989. (In Norwegian.)

[6.22] a): G. Ginsberg: "Surface Mount and Related Technologies". (Marcel Dekker, 1989.)
b): D. R. Seraphim et al.: "Principles of Electronic Packaging". (McGraw-Hill, 1989.)
c): T. Gleditsch et al.: "Design of high frequency PCBs, a handbook." EPF-report R-38, March 1990. (In Norwegian.)

[6.23] H. Svärd and A. Sihlbom: "High frequency electrical design". IVF-report 88622, 1988. (In Swedish.)

[6.24] D. J. Arthur: "Electrical and Mechanical Characteristics of Low Dielectric Constant PCBs". Proc. IPC Conference, Boston 1986, 0179-027-1.0C.

[6.25] S. Gurley: "Flexible Circuits". (Marcel Dekker, 1984.)

[6.26] J. J. Miniet: "End User´s Guide to Innovative Flexible Circuit Packaging". (Marcel Dekker, 1986.)

[6.27] W. S. Rigling: "Rigid-Flex Printed Wiring Design for Production Readyness". (Marcel Dekker, 1988.)

[6.28] ANSI/IPC-D-249: "Design Standard for Flexible Single- and Double-Sided Printed Boards". (January 1987.)

[6.29] Mil. Std. 2118: "Flexible and Rigid-Flex Printed Wiring for Electronic Equipment".

[6.30] J. C. Fjelstad: "Design guidelines for Flexible Circuits". Electronic Packaging & Production August 1988, p.32.

[6.31] L. Halbo (Ed.): "Polymer Thick-Film Technology (PTF) - Design Guidelines and Applications". (Lobo 1990.)

[6.32] H. B. Bakoglu: "Circuits, Interconnections and Packaging for VLSI". (Addison Wesley 1990.)

[6.33] O. Pedersen et al.: "Modelling of Power and Ground Planes". Circuit World, Vol. 18, no.3, 1992, p. 30.

[6.34] H. Hamano, Toshiba, private communication.

[6.35] R. J. Klein Wassink: "Foot prints of fine-pitch SMDs". Philips report SAQ-p238, May 1991.

[6.36] P. Melville: "Thermal resistance of SO and PLCC packages". Electronic Components and Applications, vol. 7, no. 4, 1986.

CHAPTER 7

PRODUCTION OF PRINTED CIRCUIT BOARDS

7.1 INTRODUCTION

The completed PCBs will normally represent the greatest part of the value of the electronic system hardware. An efficient and defects free production is essential. The process is increasingly automated, but generally there still is needed some additional handwork.

7.2 PRODUCTION OF HOLE MOUNTED PCBs

In this section we shall describe the process for purely hole mounted boards, with emphasis on the automated parts. Figure 7.1 shows the process schematically.

7.2.1 Component mounting

Sequencing and mounting of axial components:
Axial components for automatic mounting are usually delivered on a tape (please refer to Section 4.9). The first step in the mounting of axial components is to make a new component tape, specifically for the most efficient mounting of a given type of PCB. In the new tape, the needed component types are placed in the order that makes the subsequent placement optimised, as illustrated in Figures 7.2 a) and b). In the sequencing machine, all needed component tapes are stored, please refer to Figure 7.3. In the example the machine cuts out one component of type 5 and places in the new tape, then one of type 14 and so on, covering all components needed for one board. Then it starts over, mounting the same series of components for the next board, etc. Figure 7.3 shows a sequencing machine, with capacity of some 80 component types, and speed up to approximately 5000 components per hour.

The new tape is placed in the axial insertion machine, see Figure 7.4, that will mount typically 3 - 5000 components per hour. The process, see Figure 7.5, includes cutting the component out of the tape, forming the leads to fit in board holes, mount, and then cut and clinch the leads to avoid that the component falls out during handling.

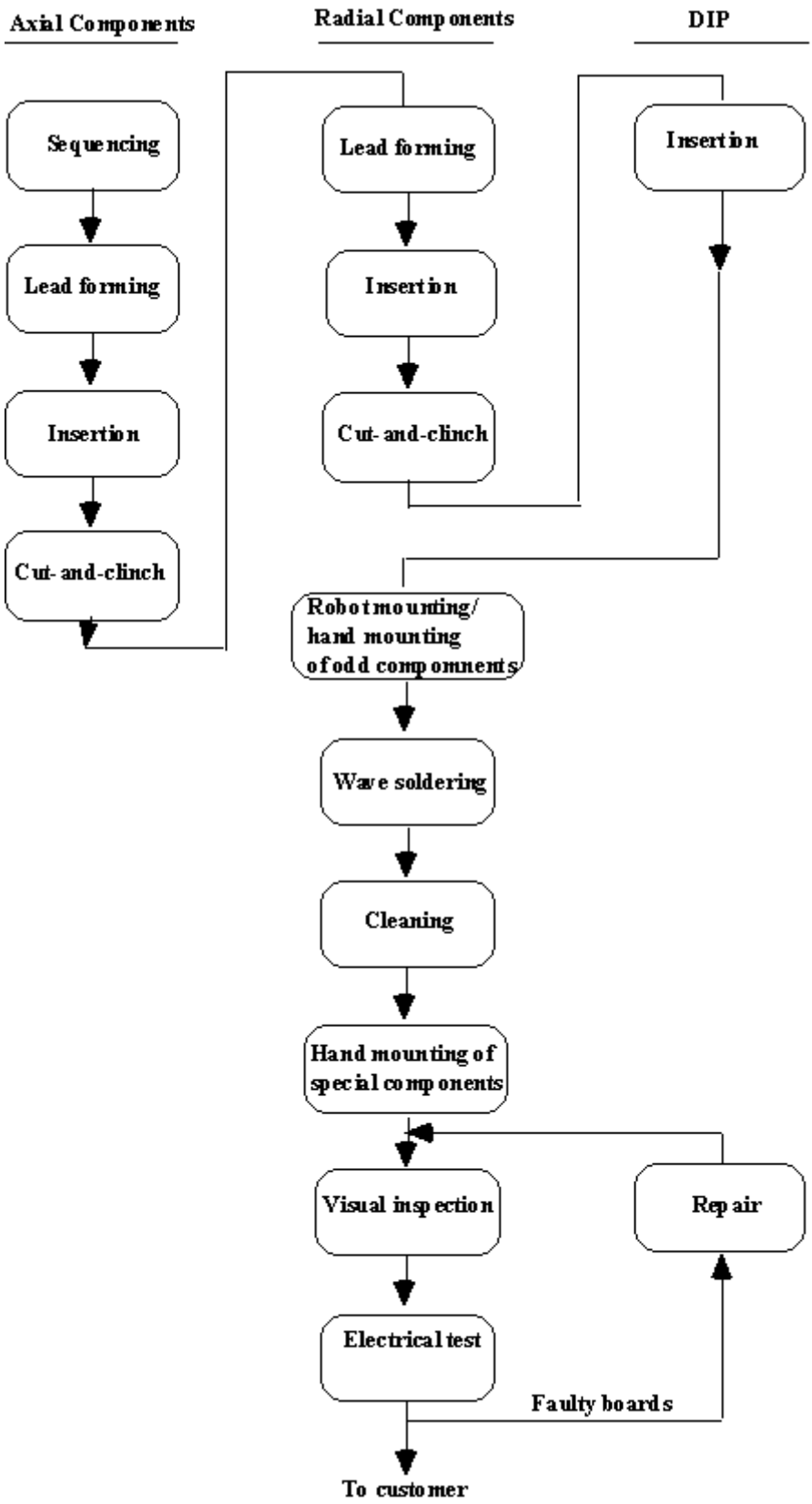


Fig. 7.1: The process for production of hole mounted PCBs.

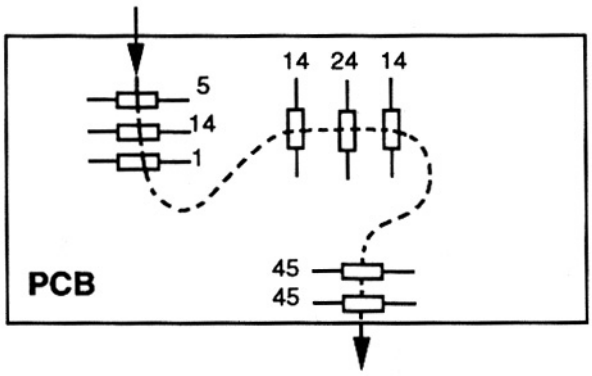


Fig. 7.2 a): Schematic example of the most efficient sequence of mounting the components of a particular PCB.

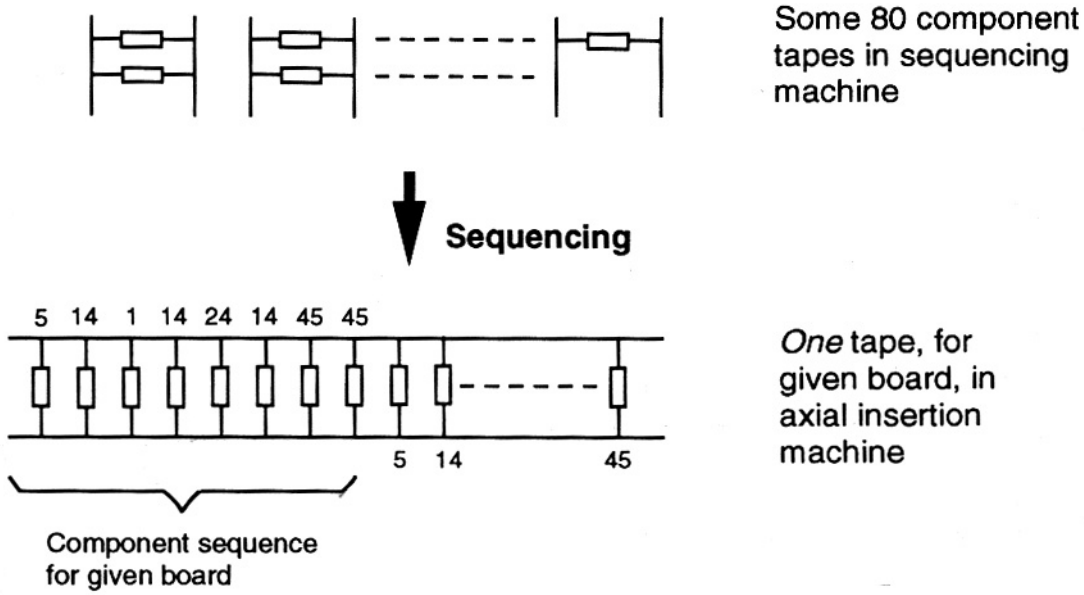


Fig. 7.2 b): The principle of sequencing.

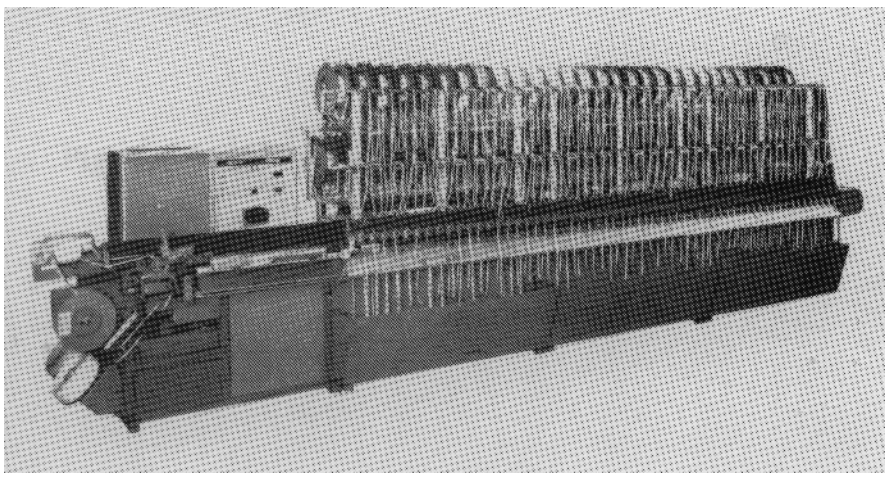


Fig. 7.3: Sequencing machine.

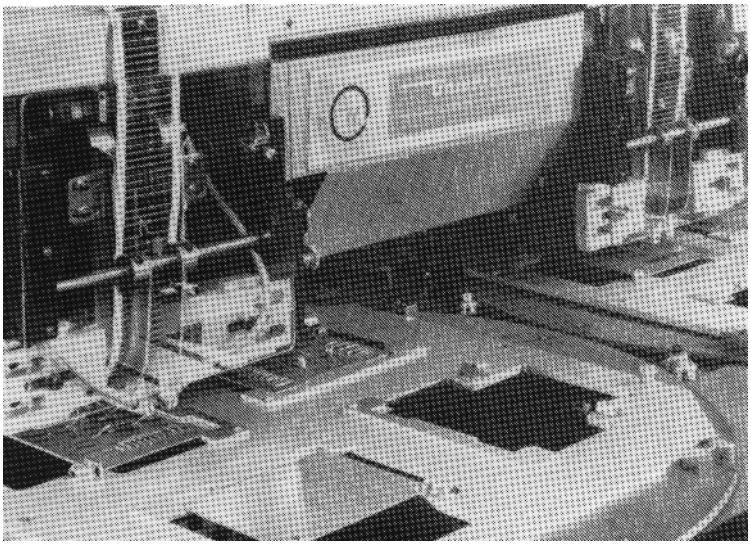


Fig. 7.4: Axial inserter with two mounting heads.

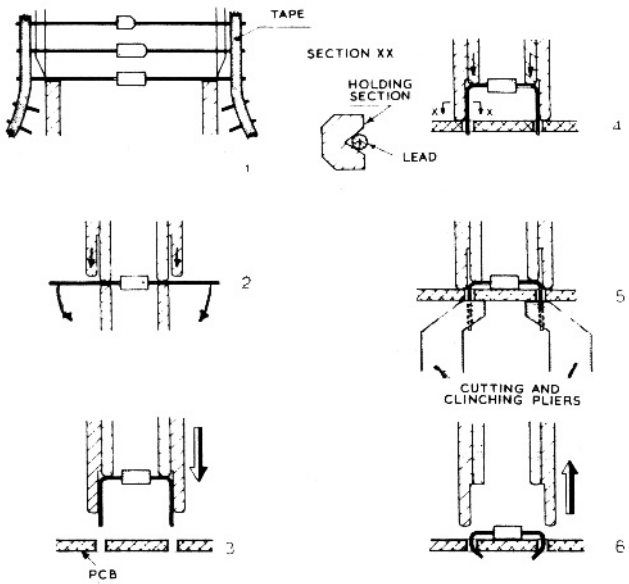


Fig. 7.5: Simplified process in the axial inserter: a): Cutting the components from the tape, b): Lead bending, c) - d): Insertion, e): Cut and clinch, f): Return to starting position.

Radial and DIP IC mounting

For radial components, sequencing is not used. The machine for radial insertion will often have stored the tapes with all components needed, and a transport mechanism ("pater noster" transport band) bringing each component from tape position to insertion position.

DIP ICs are normally delivered in plastic tubes, sticks, which are stored in a separate DIP inserter, see Figure 7.6. The holder of the tubes moves back and forth, to place the right stick in position for mounting. At the same time, the PCB is moved to get the location of the component in the right place underneath.

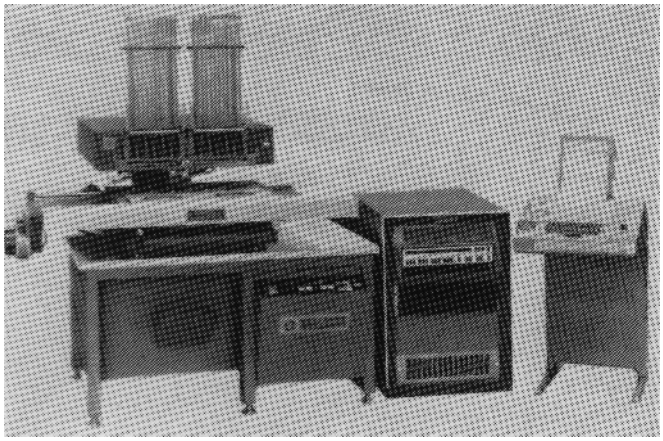


Fig. 7.6: DIP inserter.

Manual and semi-manual mounting

For odd component types and for prototype series hand mounting is still used. "Light boards" are also used, see Figure 7.7. A light board has stored a set of boxes containing the needed components for manual picking by an operator. A computer controlled lamp above the board focuses a light spot on the PCB, while the correct box of the component to be mounted is marked by the light from an LED. When the component is manually placed, the operator pushes a pedal, and the computer shows next component and place on the PCB where it should be placed. A trained operator can mount some 100 components per hour with this aid, with considerably reduced fault frequency.

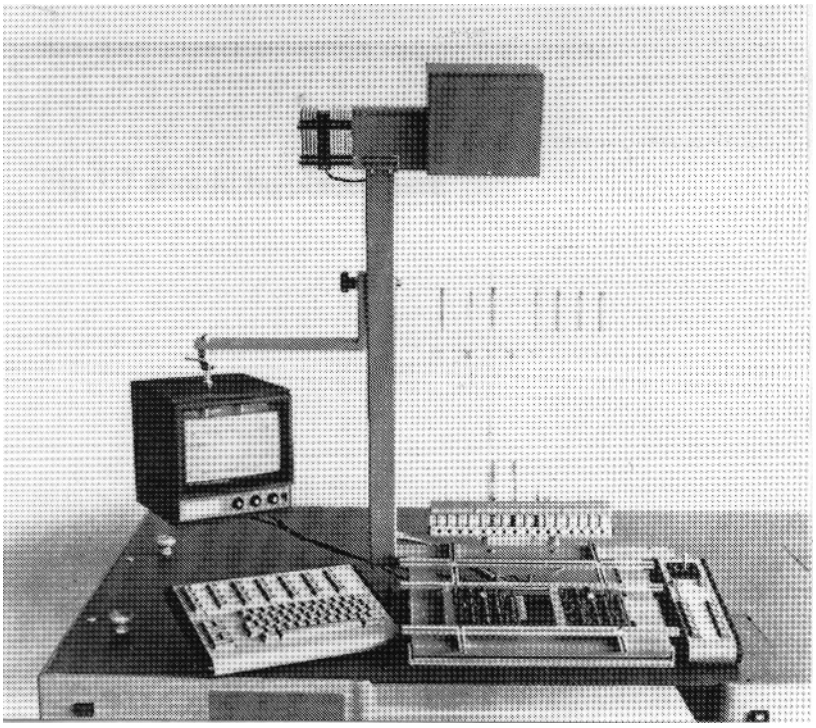


Fig. 7.7: Manual mounting board with light guide.

7.2.2 Wave soldering

Mass soldering of hole mounted board is normally done by wave soldering. Figure 7.8 shows a wave soldering machine.

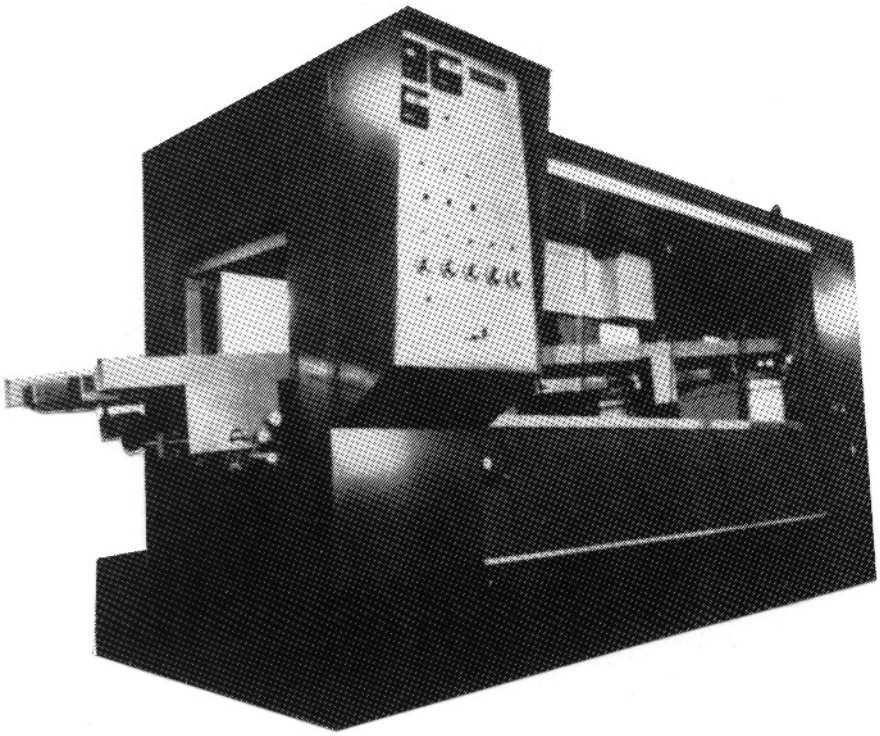


Fig. 7.8: Wave soldering machine.

A conveyor transports the PCB through the machine. The boards of different sizes are placed in jigs of one standard size. First, the board will pass through a fluxing unit. Here solder flux is applied to dissolve oxides and improve wetting and solderability, please refer to Section 3.10. Most commonly, the flux is pumped up together with air, making a foam that hits the underside of the board, please refer to Figure 7.9 a). The flux contains alcohol or an other solvent to give the right viscosity. The solvent in the supply evaporates in time and is automatically replenished to keep the density of the flux bath constant, see Figure 7.9 b).

Then the board passes over a preheating zone where the board is heated by a hot metal plate underneath through radiation and convection, to approximately 100 °C. The purpose of this is:

- To activate the chemically active parts of the flux (chlorine is dissociated from the organic component of the flux)
- To evaporate the chemically inactive solvents
- To heat the board slowly to avoid thermal shock in the subsequent solder bath.

After the preheating the board goes through the solder zone, passing a wave of molten solder, see Figure 7.10. The solder is normally close to a eutectic composition of tin and lead, 63 % / 37 % by weight, as described in Section 3.10. The melting temperature is ca. 180 °C, but a typical solder bath temperature is 230 - 250 °C.

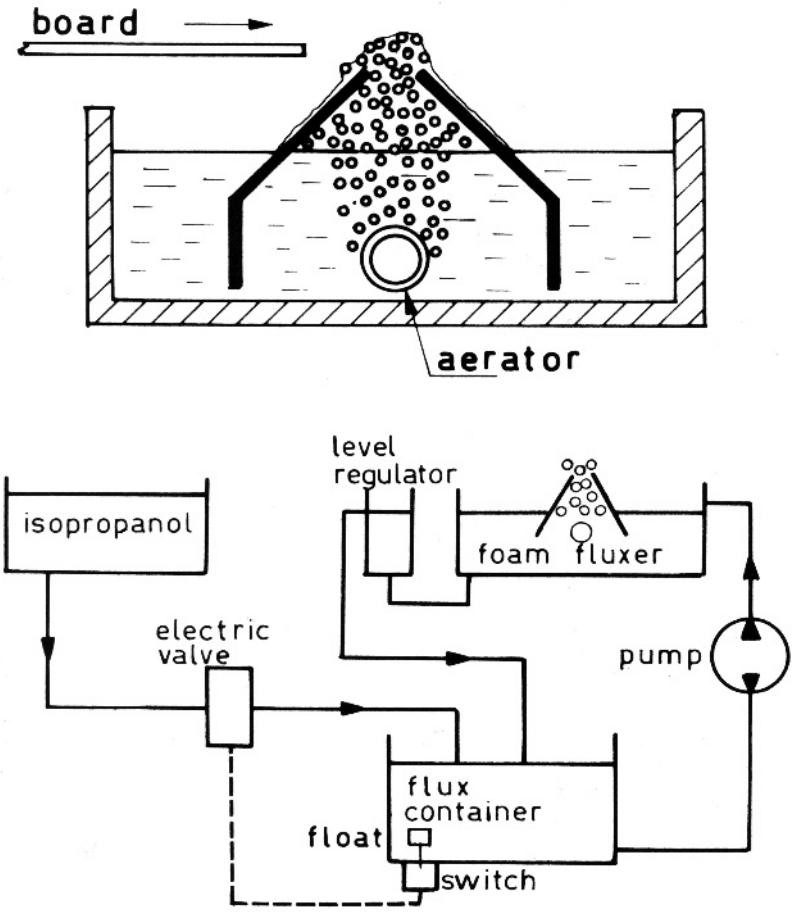


Fig. 7.9: a): Principle of foam fluxer, b): Control system for density and level of the flux bath.

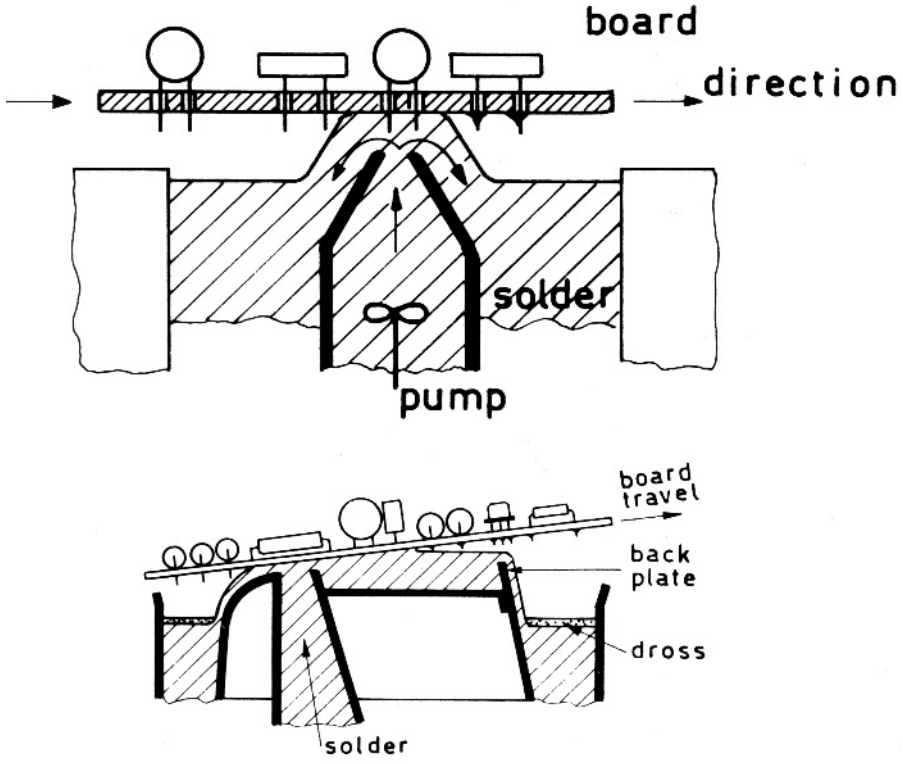


Fig. 7.10: a): Principle of wave soldering, b): The real shape of the wave.

The solder is located in a container. A pump forces it up through a slit, forming a wave at right angle to the motion of the board. The shape of the wave is important for the solder quality, and so is the speed of board motion, the contact time and the solder temperature.

The wave is adjusted such that the component lead ends and the under side of the board are wetted by the wave. The solder is also pulled up into the component holes by capillary forces.

7.2.3 Cleaning

After soldering, the board may pass directly into an in-line cleaning machine, see Figure 7.11 a), if cleaning is needed. This depends on the type (activity) of flux used and the required quality of the product for which the board is to be used. Strong fluxes leave corrosive residues that need to be cleaned, please refer to Section 3.10. Previously freon was the cleaning agent of choice for rosin flux on most products. It is now abandoned due to its harmful effect on the ozone layer of the atmosphere, after it evaporates and escapes. Instead alcohol may be used, water (with detergent), or newly developed cleaning agents. More efficient cleaning is obtained by ultrasound agitation of the cleaning bath. Vapour cleaning after immersion is also used, see Figure 7.11 b).

7.2.4 Repair

Removal of faulty components is done by firstly removing the solder. It can be done by manually heating each solder joint above melting temperature, and then sucking away the solder by a special suction tube on the solder iron, connected to a vacuum pump. After removing of the component a new part will normally be mounted and soldered in place manually.

7.2.5 ESD precautions

Precautions against electrostatic discharges (ESD) must be taken when ICs and some transistor types (MOS) are handled, please refer to Section 4.8. Today ESD protection is considered necessary throughout the production process, from test of incoming components to repair and packing of finished boards, or systems in some cases. The main precautions are:

- Conductive materials in floors
- Grounded equipment
- Grounded personnel.

An ESD protected working place is shown in Figure 7.12. It has grounded, conductive mats on the floor, on the seat of the chair and on the working bench, grounded soldering iron, etc., a grounded wrist band for the operator. The grounding is made through a resistor (typically 1 Mohm) to avoid big current spikes that may harm the operator. The operator is also grounded by wearing conductive shoes or conductive tape inside and outside the shoes. ESD protected packing of the components and board was described in Section 4.8 - 4.9.

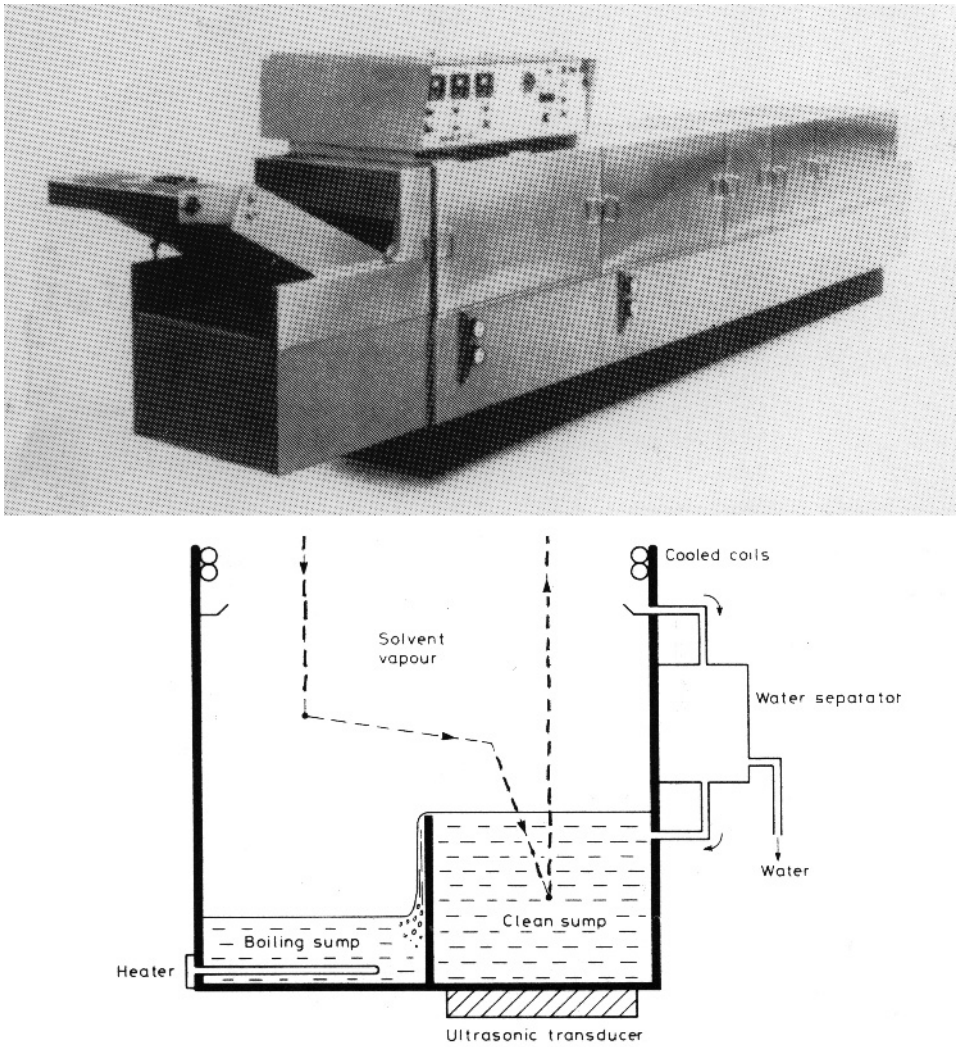


Fig. 7.11: a): Industrial in line cleaning machine, b): the principle of ultrasound and vapour cleaning.

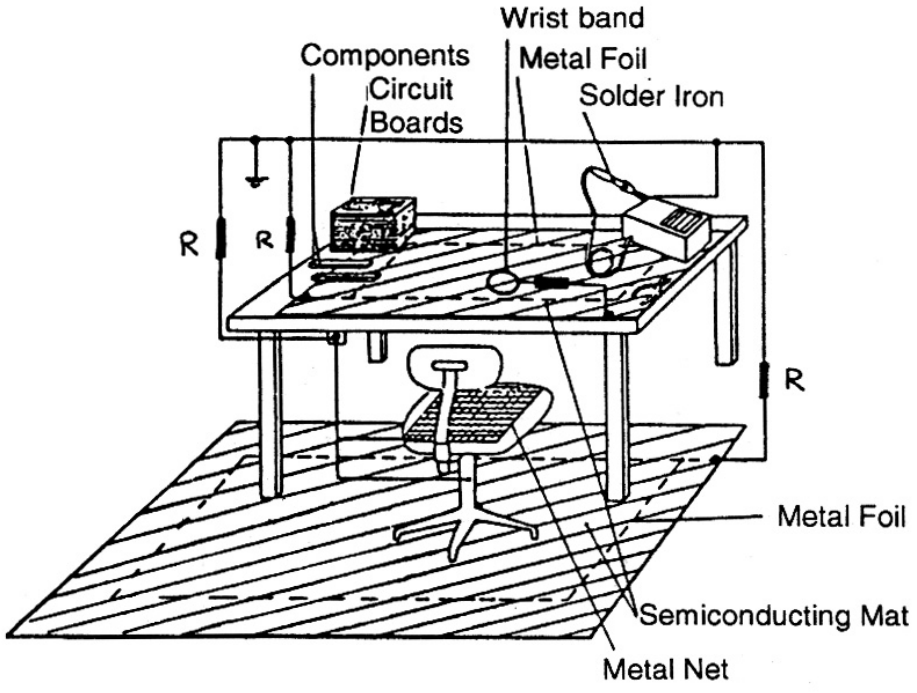


Fig. 7.12: An ESD protected working space. The resistors R normally are 100 Kohm - 1 Mohm.

7.3 PRODUCTION OF SURFACE MOUNTED PCBs

The use of surface mounted components requires a more complex production process than pure hole mounting. There are different possible alternatives of components on one or both sides of the board, please refer to Figure 6.5. Most often we have a combination of SMDs and hole mounted components. The production sequence must be carefully considered and chosen already in the design phase. Here we show the basics of the wave soldering and preceding gluing process as well as several reflow soldering processes. Then component mounting will be described. In Section 7.5 we shall return to the complete processes for different types of SMD or mixed SMD/hole mounted boards.

7.3.1 Gluing and wave soldering of SMD components

Gluing

When the SMDs are wave soldered they are hanging underneath the board and must be fastened in advance by an adhesive. There are three main methods of applying the adhesive, Figure 7.13:

- Screen printing
- Application by dispenser
- Pin transfer.

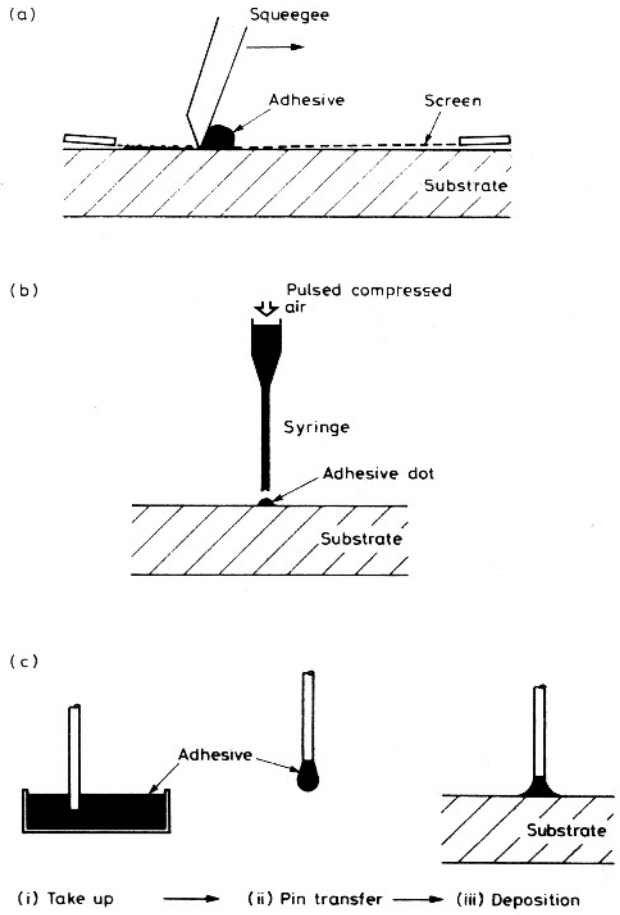


Fig. 7.13: Application of adhesive for SMD mounting by a): Screen printing, b): Dispensing and c): Pin transfer.

Screen printing of adhesive is done in a manner similar to printing of solder paste, see below. A stencil of 0.5 mm Teflon is often used. The holes may be drilled by a numerically controlled drill, with drill information for position and size of the holes from the CAD system. The size should be bigger for heavy components and components with high stand-off, needing more adhesive. This way of adhesive application is efficient, as all adhesive dots are placed simultaneously. However, the board surface must be plain, and this process must be done before any component is mounted.

The most used method is application by dispenser. The syringe may be mounted on the pick-and-place machine, and a controlled pressure is applied in the dispenser each time a glue dot is placed. The amount of glue is controlled by the time and pressure.

Pin transfer consists of a pin that is first dipped into a pot of adhesive, then touching the board and leaving an adhesive dot at the point where the component will be mounted. Pin transfer is suited for very high volume production. In that case, a jig is made with a matrix of pins in the positions of all components to be glued. The jig is lowered into a big pot of glue and all adhesive dots are then deposited simultaneously.

The demands on the adhesive and the gluing process are high. The adhesive must not flow onto the solder pads, otherwise the solderability is ruined. It must wet the component well and immediately hold the component sufficiently well for the handling necessary until curing of the adhesive. It must have a long shelf life with stable viscosity, yet cure fast for a high volume production. Viscosity and rheology must be stable, assuring reproducible amounts of deposited adhesive. When repair is needed, the adhesive must soften during the repair processing (see below).

The adhesives are one- or two component heat curing epoxy, UV curing acrylic or epoxy. A problem with two component adhesives is that the curing proceeds fast when the components are mixed. Storage time for mixed adhesive is short (a couple of days). Therefore, one component adhesives are used the most.

Heat curing often takes place in an IR in-line furnace, of the type used for IR reflow soldering (see below). Typical curing conditions are 150 °C for 1 - 2 min. UV curing takes place in an in-line equipment, containing a powerful UV lamp. For UV curing to be possible, parts of the adhesive dots must "see" the UV light. The curing takes only a few seconds.

Wave soldering

Wave soldering is done in the same way as for hole components, but it is more critical. Problem areas are: not wetted surfaces, generation of solder bridges and thermal stress on the components.

The component bodies cast shadows for themselves and their neighbours, see Figure 7.14, and the simplest solder machines give unreliable contact between the solder areas and the wave. To remedy this, many machines have two waves, see Figure 7.15. The first is a turbulent wave, reaching and wetting all corners and crevasses. However, it will create solder bridges. The second, called the

"lambda wave" is a gentle wave that removes the superfluous solder. In addition to the solder process conditions, also the dimensions of the solder pads are very important for defect free soldering.

There are several other principles for SMD wave soldering machines. The "jet wave" moves in the opposite direction to the board at high velocity. In some machines, a vibration is generated in the solder. Solder bridges may be blown off with a stream of hot air, "air knife", and oil can be mixed with the solder to reduce dross formation.

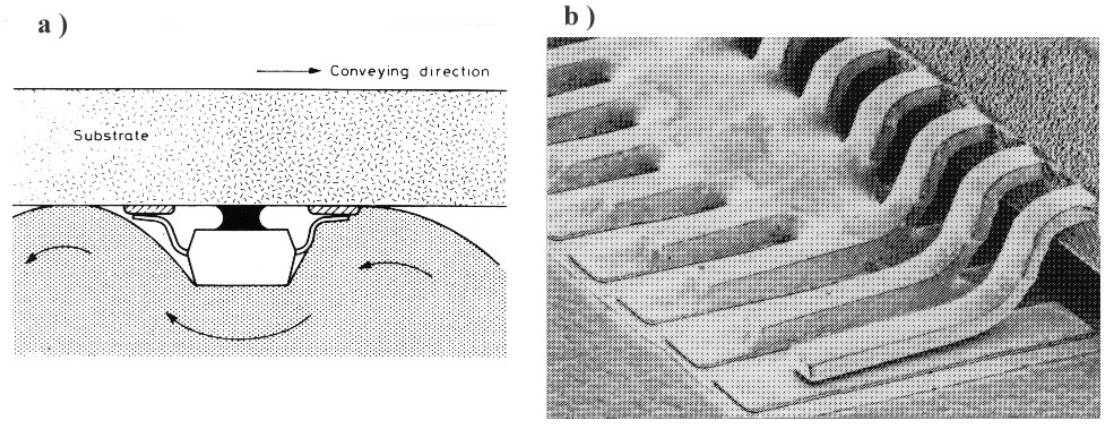


Fig. 7.14: a): Shadowing in SMD wave soldering, b): Solder bridging on fine pitch package.

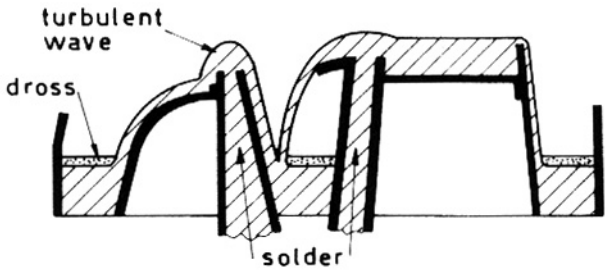


Fig. 7.15: Double wave for SMD soldering.

Figure 7.16 shows a typical temperature profile in a double wave solder process, as measured inside an SMD. The peak temperature is 230 - 250 °C, and the time during which the component is above 200 °C is 5 - 10 sec.

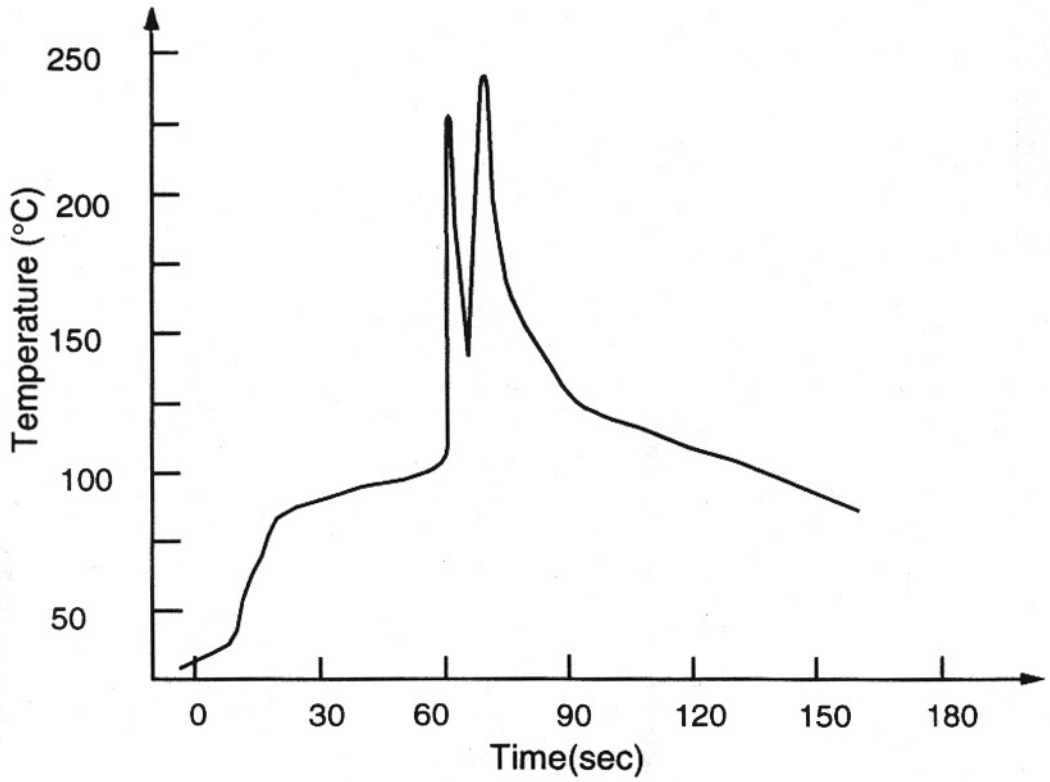


Fig. 7.16: Temperature profile during wave soldering in a double wave machine.

Limitations to wave soldering of SMDs

The shadowing effect depends on the shape of the component and its orientation with respect to the direction of motion. Not all components are suitable for wave soldering. IC packages with terminals on all four sides - flatpacks and chip carriers - should not be wave soldered. SO packages should only be mounted with their axis of symmetry along the direction of motion during soldering, or preferably not at all. High passive components should have their length axis perpendicular to the direction of motion, please refer to Figure 6.6. Other details are also given in Section 6.3.

As the SMDs are submerged in the molten solder, they are exposed to a tough thermal stress. Not all component can stand this, and the information from the component manufacturer should be consulted.

7.3.2 Solder paste deposition and reflow soldering

For reflow soldering the solder metal is first deposited on the PWB, localised to the solder lands. The solder lands should preferably be covered by a thin layer of solder metal from plating or hot air levelling in advance, to obtain good wetting please refer to Section 5.6. Then additional solder metal is applied in the form of screen printed paste. After component mounting (see below) on the solder paste the soldering is done by heating until the solder melts and wets component terminals and PCB solder lands. Various methods are used for the heating. We shall start describing the solder paste and deposition.

Solder paste

The paste, see Figure 7.17, consists of:

- Solder particles
- Flux
- Solvents.

The metal content of the paste is 85 - 90 % by weight. The alloy in the solder particles is the same as desired in the solder fillet, e.g. Sn 63 / Pb 37 % by weight. It is common to have 2 % Ag in the solder to reduce leaching of Ag from capacitor component terminals, please refer to Sections 3.10 and 4.7. The particles are sifted to give large or small average size, depending on the components to be soldered. For standard SMD ICs and passives larger than 0603 50 - 75 μm average size is used. For fine pitch components smaller particles are preferred. However, they have a larger surface-to-volume ratio and tend to oxidise more, giving poorer wetting and solder balling (see below) unless a stronger flux is used.

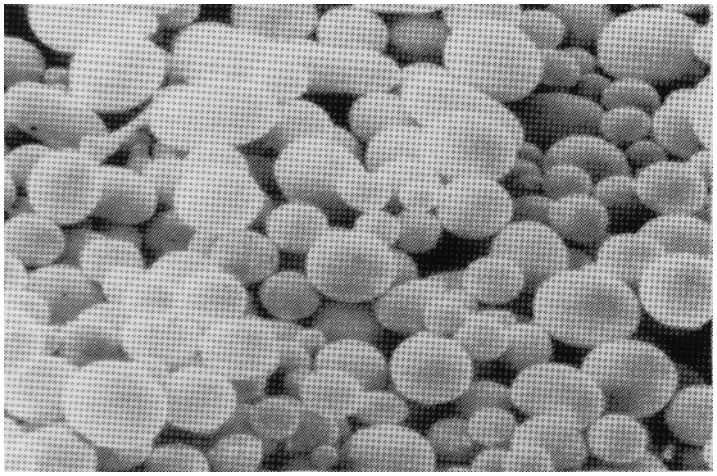


Fig. 7.17: Microphotograph of Multicore solder paste type Sn 62 RMA B 3. The designation means 62 % by weight of Sn, 35.7 % Pb, 2 %, Ag, 0.3 % Sb, RMA flux, 75 μm average particle size, 85 % metal content, viscosity 400 000 - 600 000 centipoise.

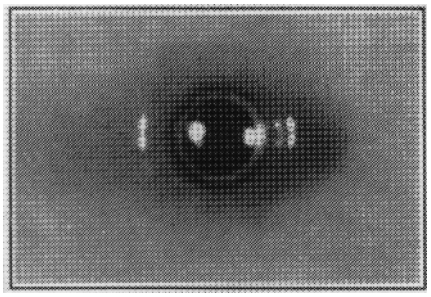


Fig. 7.18: Test of solder paste: The paste is printed through a circular opening with a diameter of 5 mm, in a 200 μm thick stencil. After reflow, the paste should melt into one body, without any particles spreading out.

The solder paste changes rheology and other properties in storage and has a limited shelf life. It may be tested by printing through a circular hole in a plate.

After reflow all solder should melt together, with no solder balls outside, see Figure 7.18.

The printing screen or stencil

The most common way of applying solder paste is by screen printing through a screen or a stencil, see Section 3.5. The screen is made of woven stainless steel filaments or polyester. The screen is covered by an organic film, with openings where the paste is to be deposited. The patterning of the organic film is done by photolithography, see Section 3.5.

Woven screens are simple and cheap, but they have some drawbacks: Due to the filaments, see Figure 7.19, and the slight deformation when the screen is pushed down by the squeegee, the definition is limited. Fine screens with thin filaments and a high mesh count must be used for high definition screens. They are easily broken, giving delay and extra cost in the production. For large areas, the screen tends to stretch unevenly during printing, also limiting the precision of paste deposition near the edges.

The volume of paste deposited depends on the thickness of the organic film, the opening area, and the fraction of the screen that is covered by the metal wire, please refer to Section 3.10. This volume is important, determining if the solder fillet will be lean or rich.

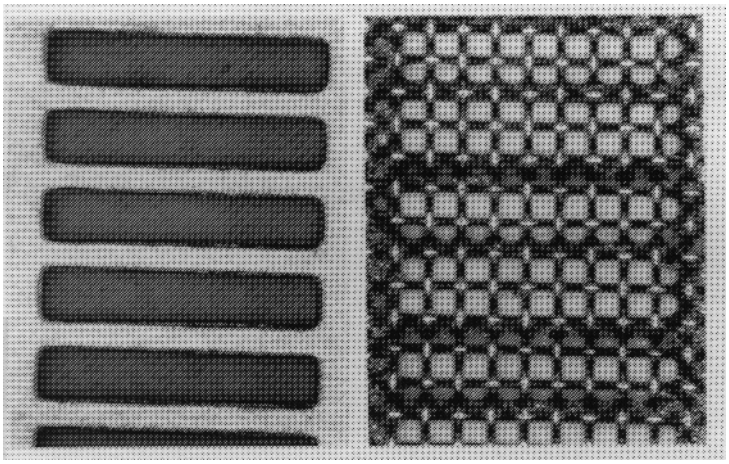


Fig. 7.19: Detail of printing screen and printing stencil with fine line printing pattern.

Use of a thin metal foil for solder stencil gives significantly better precision and reproducibility in the solder printing, and the stencil lasts many more prints. The openings are normally etched out. Typically the thickness is 150 or 200 μm. To reduce overetch the etching is done simultaneously from both sides, see Figure 7.20. The openings are the same size as the solder lands for large solder lands, somewhat smaller than the lands for fine pitch components. An alternative is to thin down the stencil over areas where there are fine pitch components, see Figure 7.21. The holes may also be drilled.

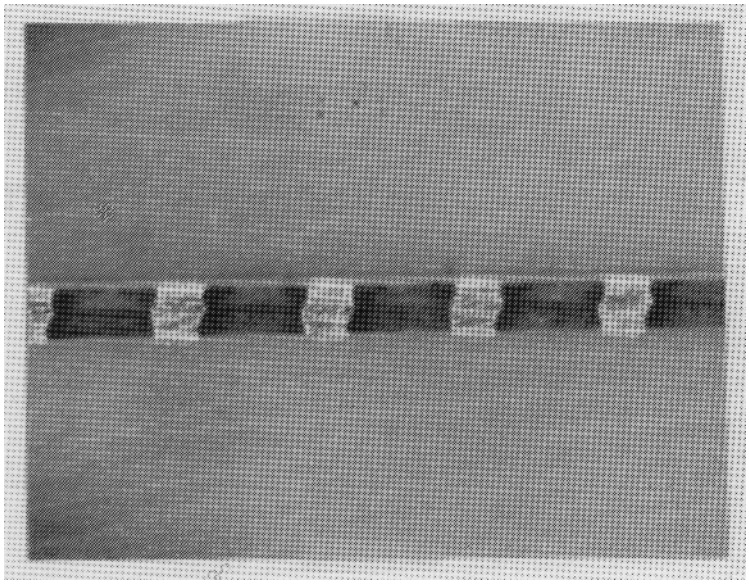


Fig. 7.20: Detail of printing stencil with fine pitch printing pattern: cross section of a stencil etched from both sides, with an acceptable, small amount of offset (40 x magnification).

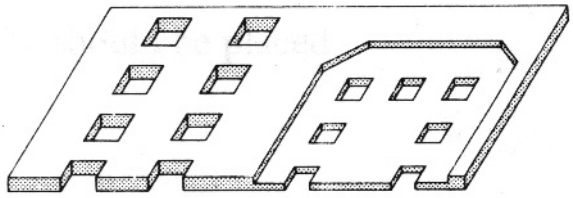


Fig. 7.21: Two steps printing stencil.

Brass, stainless steel and beryllium copper are the materials most used. The latter is best and most expensive. Alternatively the stencil may be made out of polyester (Mylar) or Teflon, see Figure 7.22, and the holes may be drilled or punched by a numerically controlled punching tool.

The printer and printing process

Figure 7.23 shows a relatively simple equipment for printing solder paste. The boards are manually placed in the printer, their position is determined by holes and guiding pins, or by the contour of the boards and guiding edges. Bigger printers are automatic, with cassette-to-cassette feeding, or in-line, so that the boards go on directly to component mounting. Advanced printers have an electronic vision system, recognising a set of fiducial marks etched in the copper. The position of each board is then adjusted very accurately relatively to the screen.

For prototypes, the solder paste is most often placed by a manual dispenser. A computer controlled solder paste dispenser may also be part of the pick-and-place machine.

After the deposition of solder paste and placement of the components, the paste should be dried, to activate the solder flux, and to evaporate solvents to make the paste more tacky. It takes place in a heating cabinet or in the entrance of an in-line solder furnace, at around 100 °C.

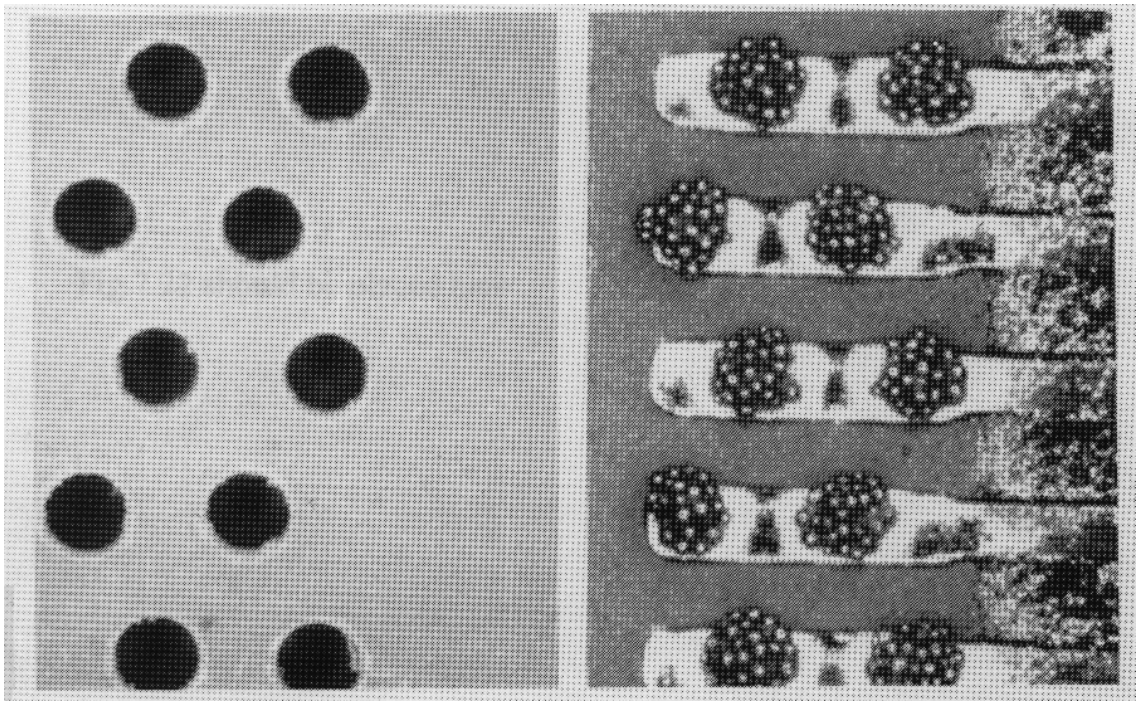


Fig. 7.22: Printing through 0.3 mm diameter holes with Mylar stencil. To obtain the correct amount of solder paste two or three small holes may be used for each solder land.

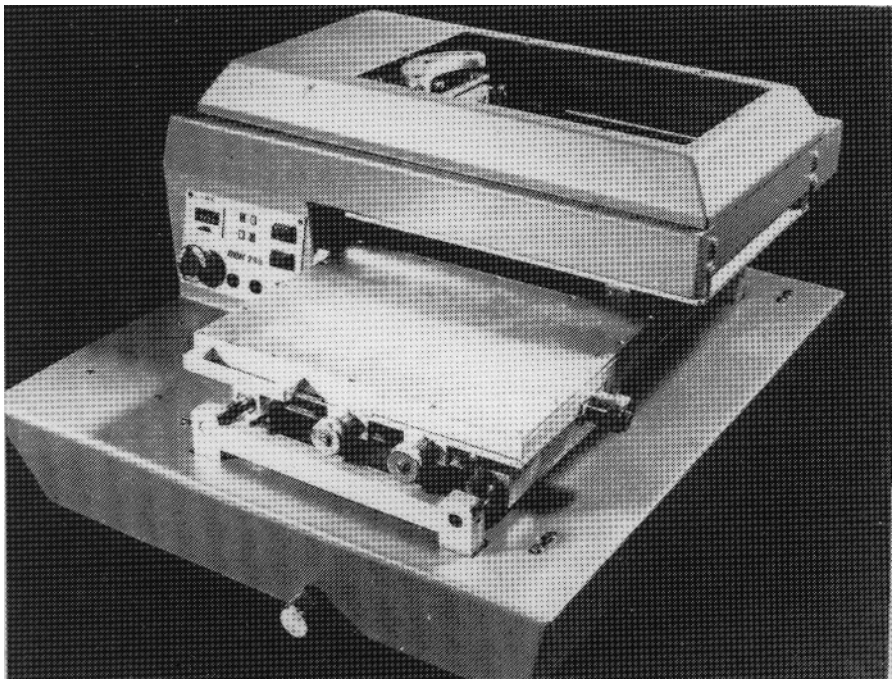


Fig 7.23 a): Screen printer.

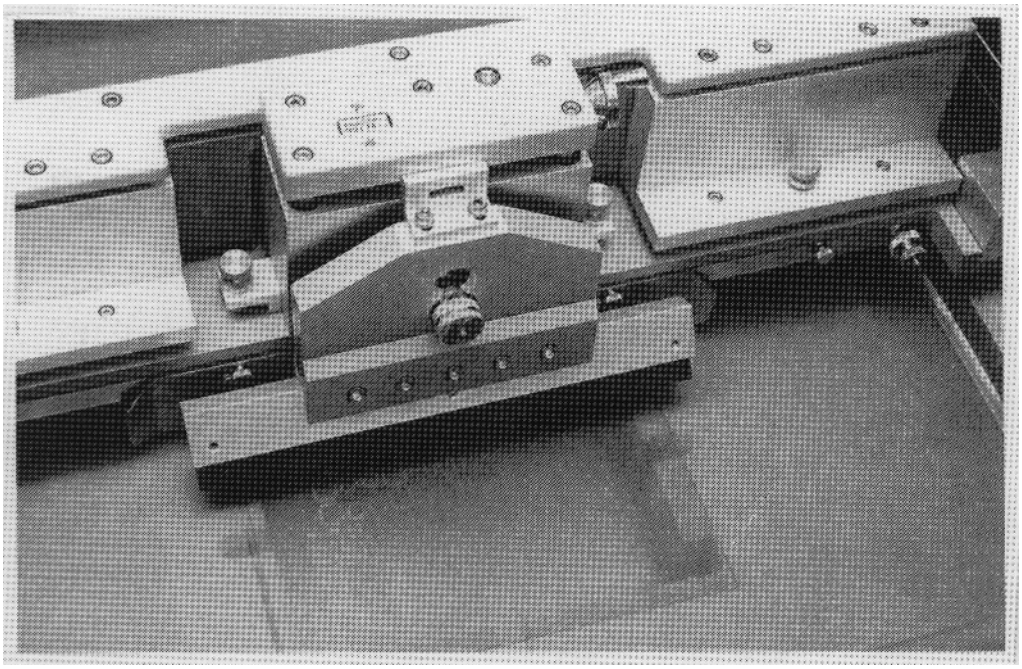


Fig. 7.23 b): The squeegee (DEK).

The IR soldering process

The most common process for reflow soldering is heating by infrared radiation (IR). It takes place in an in-line furnace, see Figure 7.24. In the furnace there are 8 - 14 heating panels, generating the radiation.

The radiation follows Planck's law [7.6], with maximum radiation intensity at a wavelength λ proportional to 1/T (Wien´s law):

$$\lambda max = k/T.$$

The amount of radiation absorbed by components and substrates depend on the emission coefficient of the materials. Originally quartz lamps were used in IR furnaces, with temperatures around 1100 °C. At this temperature electronic materials have very different emission coefficients, and were not evenly heated. The plastics in boards and component packages were often overheated. Today's furnaces use large area, low temperature, long wavelength heater panels, see Figure 7.24. This radiation also heats up the air in the furnace, and the board heating is provided by a mixture of air convection (30 - 60 %) and IR radiation. This gives a much more uniform heating. Details are discussed in [7.6].

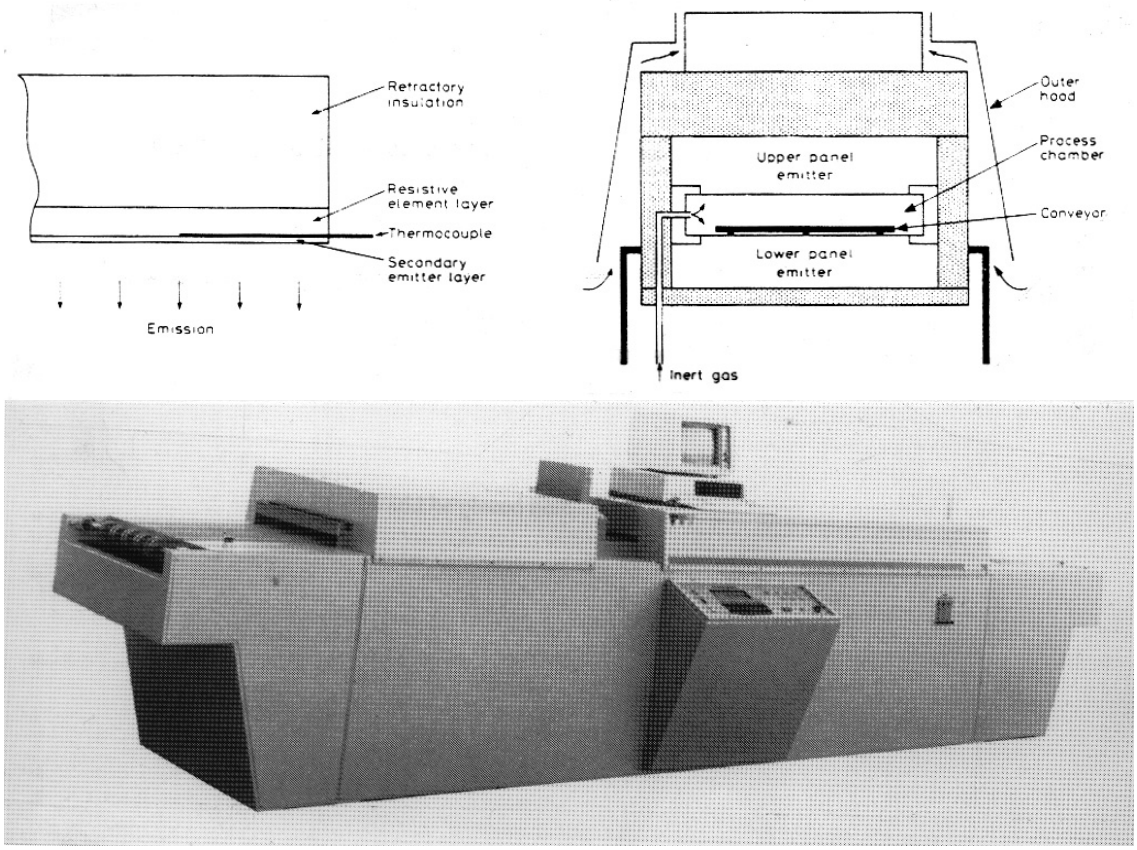


Fig. 7.24: IR furnace. a): Schematically with low temperature "area emitter". b): Industrial furnace.

Having typically 4 - 7 heater panel above as well as below the transport tunnel, the temperature profile can be adjusted to each type of board. A typical profile is shown in Figure 7.25. The first two elements give heat for the activation of the flux, and for a gradual temperature rise to avoid thermal shock. In the end, the temperature is above the solder melting point only for a short time, to reflow the solder on the board and the component terminals. The temperature profile must be re-adjusted for boards of different size and thermal mass. The temperature profiles for previously manufactured types of boards can be stored in the computer controlling the furnace.

Vapour phase soldering

Two types of vapour phase furnaces exist: in-line and batch machines. The principle of the in-line furnace is shown in Figure 7.26. The central part is a heating vessel where a fluorocarbon-based liquid is heated to boiling. Different liquids are used, with different boiling points, but the most common boiling point is 215 °C.

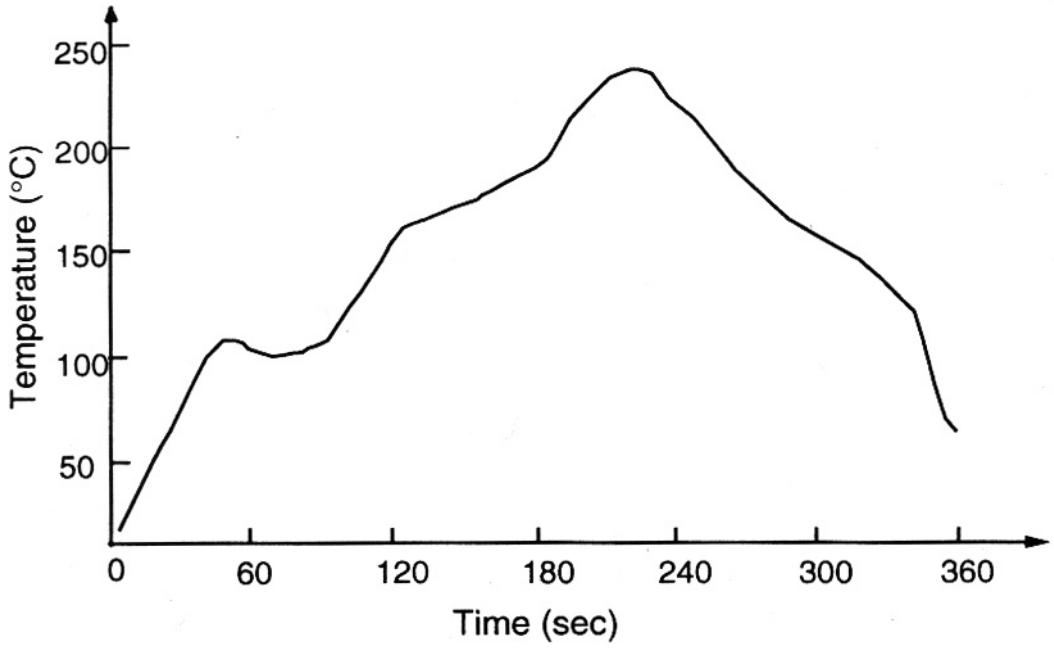


Fig. 7.25: Typical temperature profile for IR furnace.

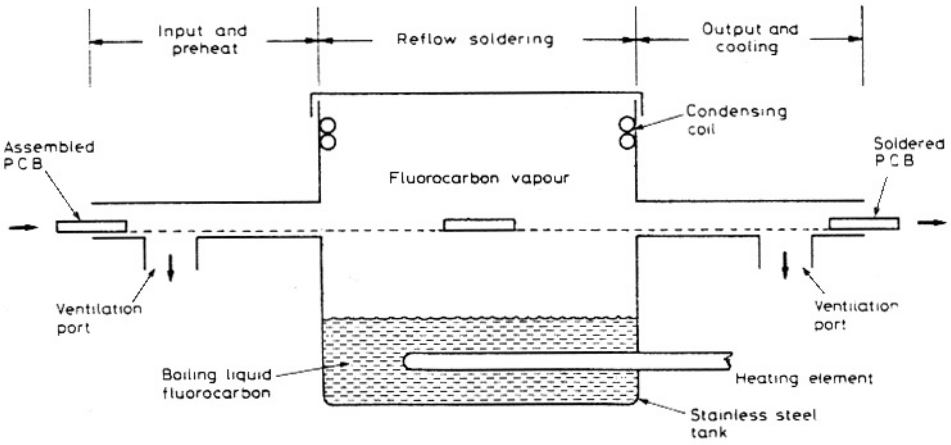


Fig. 7.26 a): Principle of in-line vapour phase soldering machine.

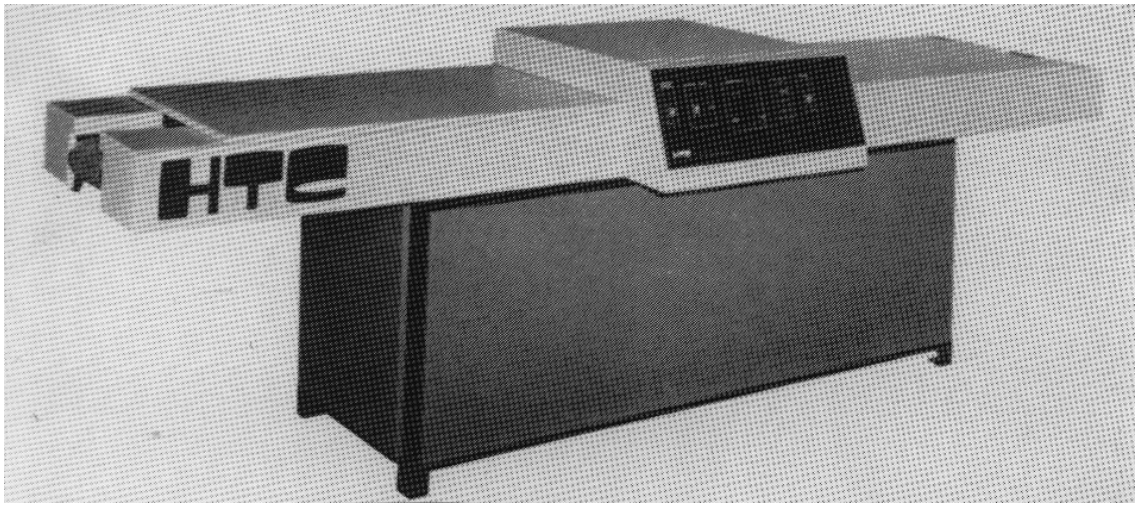


Fig. 7.26 b): Industrial in-line vapour phase soldering machine.

The boards pass through the vapour above the boiling liquid. Vapour will condense on the cold boards and transfer its heat of condensation, heating the board. After a short time, the board reaches the boiling temperature of the liquid, melting the solder. This heat transfer mechanism is extremely efficient, as discussed in Section 6.6. The heat transfer coefficient for condensing fluorocarbons is more than two orders of magnitude higher than that of air with natural convection, see Figure 7.27. A typical temperature profile, as seen by a component on the board, is shown in Figure 7.28.

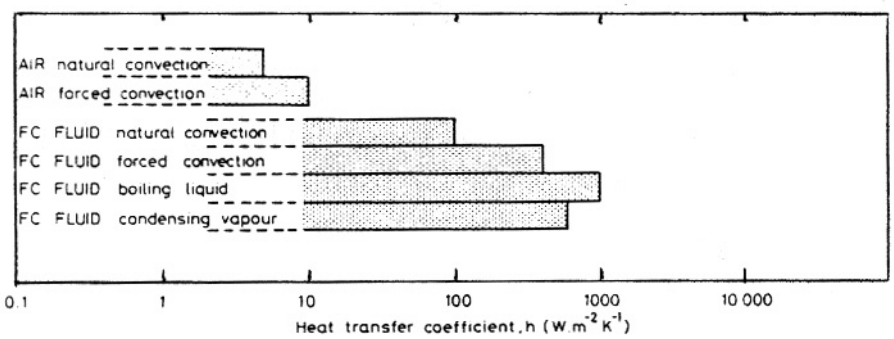


Fig. 7.27: Heat transfer coefficient for air and fluorocarbons. Boiling fluorocarbons, at the bottom, give 200 - 400 times more efficient heat transfer than air.

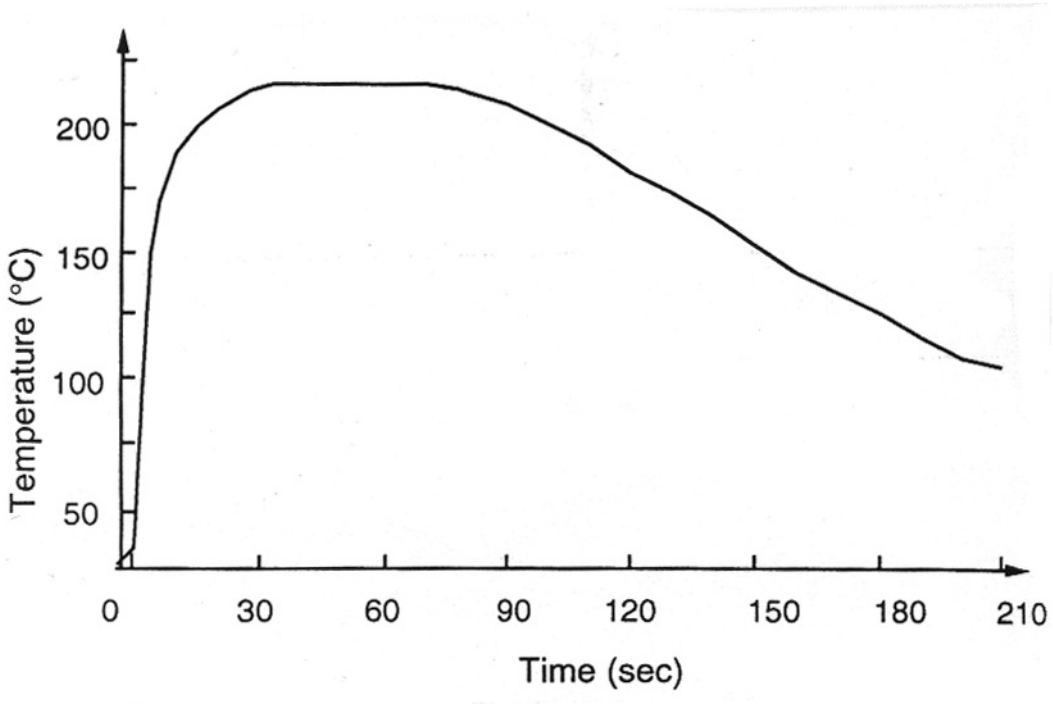


Fig. 7.28: Temperature profile through in-line vapour phase soldering machine.

The liquids used for vapour phase soldering are developed from common organic compositions by replacing hydrogen atoms by fluorine, as illustrated in Figure 7.29. They are very inert, thermally stable when they boil, and very expensive. An early liquid, FC - 70, Table 7.1, had the potential hazard that it could decompose into poisonous gasses if overheated to high temperature. Improved liquids without this problem have now replaced it.

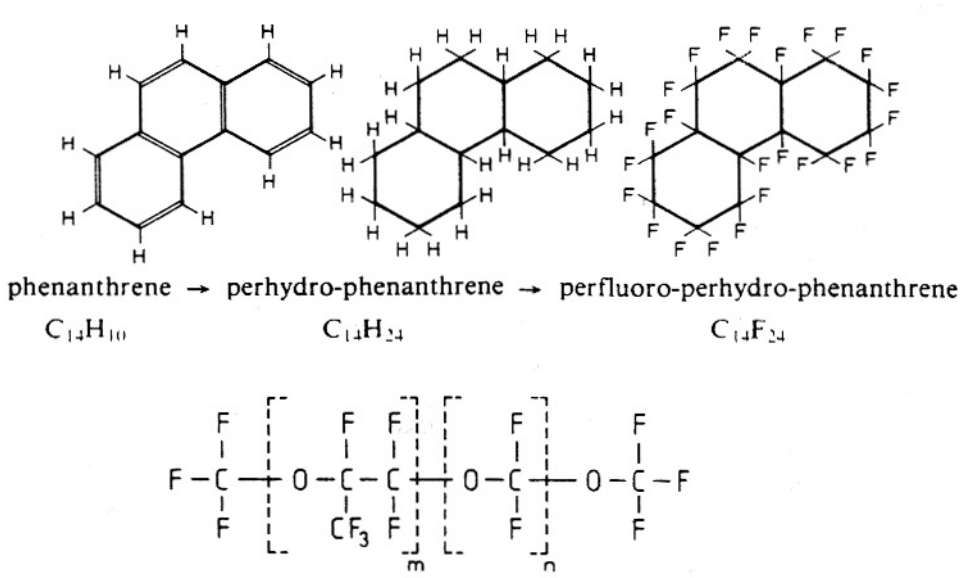


Fig. 7.29: Chemical composition of fluoro carbons for vapour phase soldering. Top: The liquid FC-5311 (3M): C14 F24 is derived from C14 H10. Bottom: The liquid LS 230 (Galden).

Table 7.1: Physical properties of some primary vapours for reflow soldering.

Property	*Units*	*R113*	*FC-70*	*FC-5311*	*LS230*
Boiling point or range	°C	47,6	215	215	230±5
Molecular weight	-	187	821	624	~650
Pour point	°C		-25	-20	-80
Density of liquid at 25°C	g cm^3	1,57	1,93	2,03	1,82
Density of saturated vapour at BP	mg cm^3	7,38	20,3	15,6	19,5
Viscosity of liquid at 25°C	cP	0,7	27	16	8
Surface tension of liquid at 25°C	mN/m	19	18	19	18
Specific heat of liquid at 25°C	J/gK	0,95	1,05	1,07	1,00
Thermal conductivity at 25°C	mW/mK	74	70	53	70
Electrical resistivity	Ohm cm		$2\ 10^{15}$	$>10^{15}$	10^{15}
Heat of vaporisation, at BP	J/g		67	68	63

To avoid loss of the expensive vapour outside the furnace there are cooling/condensation coils at the entrance and exit of the furnace. Still there is a certain loss, making this a more costly soldering method than IR.

The activation of the flux must be done in a separate furnace. In some large in-line machines, there is an IR preheating unit integrated with the vapour phase heating.

Another type of vapour phase furnace is the batch type, see Figure 7.30. A tray of boards is lowered into the vapour and kept there until soldering is completed. Above this "primary vapour" there is a blanket of a lighter (and cheaper) "secondary vapour" from a liquid of lower boiling point. 112-trichloro-trifluoro-ethane is used for this. It is heated by the primary vapour and boils at 48 °C. The batch machine is suitable for smaller production volumes and is less costly to use than the in-line machines.

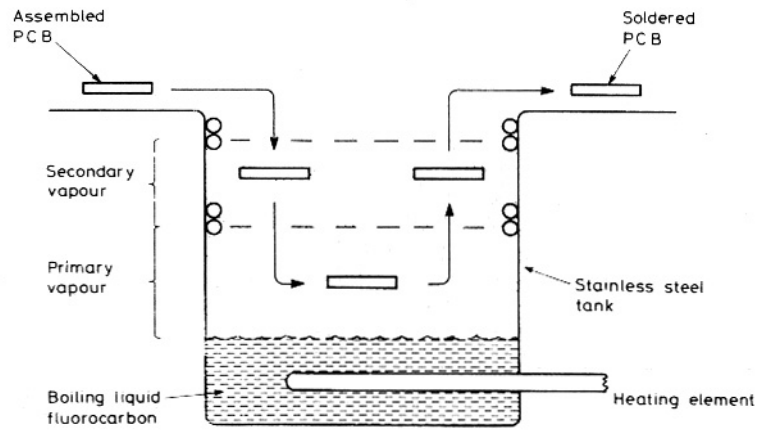


Fig. 7.30: Batch type vapour phase soldering machine.

One of the advantages of vapour phase soldering is the inert atmosphere in which the soldering takes place, giving less oxidation of the solder and the copper foil of the PCB. There is less heat damage to the polymer in the PCB, and all boards and components are sure to reach the same temperature, without special adjustment. A good discussion is given in [7.6].

Other soldering processes

Heating only in a stream of hot air is used, particularly in repair equipment, see Section 7.3.4 below.

Thermode soldering, also called impulse soldering or hot bar soldering, is used particularly for fine pitch flat packs, TAB circuits, etc. (Please refer to Section 3.14).

By this method the components are soldered one by one, in the same operation as they are placed on the PCB, on which solder is already deposited by printing, plating or hot air levelling. The mounting tool, see Figure 7.31, has a suction cup to hold the component, and a metal frame touching the outer parts of the leads (see also Figure 3.29). The frame is resistance heated by a high current through it, heating the leads to melt the solder while the component is pressed down. A typical temperature profile is shown in Figure 7.32.

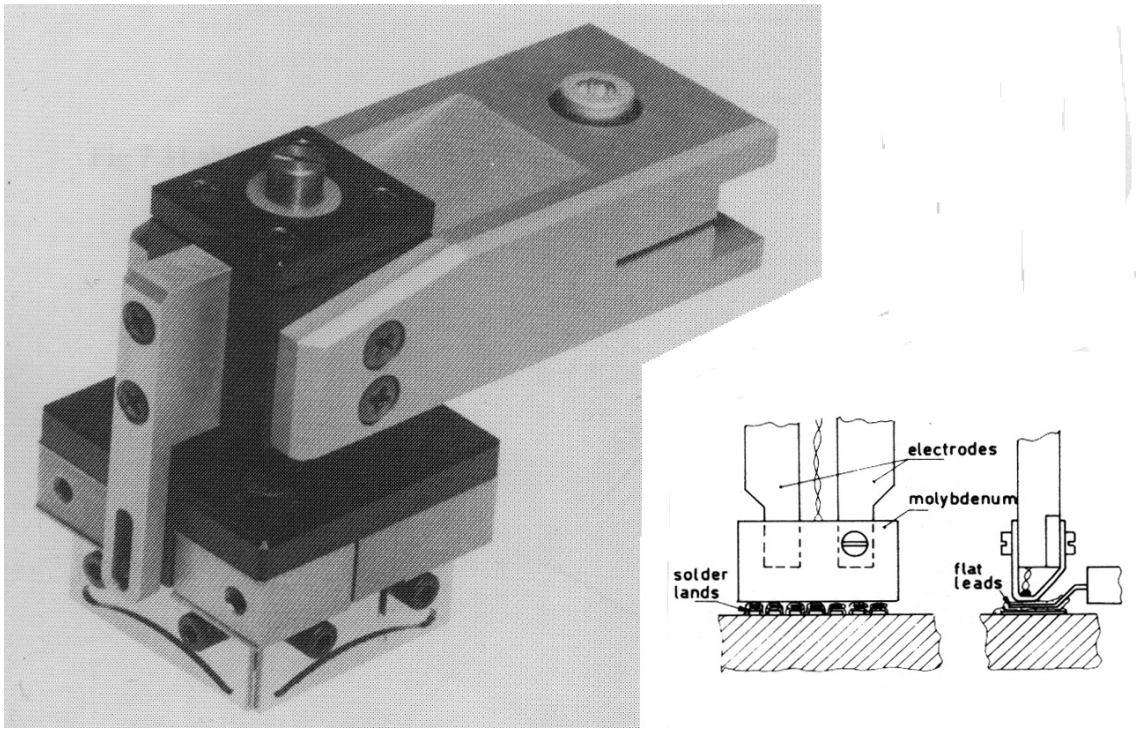


Fig. 7.31: Two types of thermodes for thermode soldering.

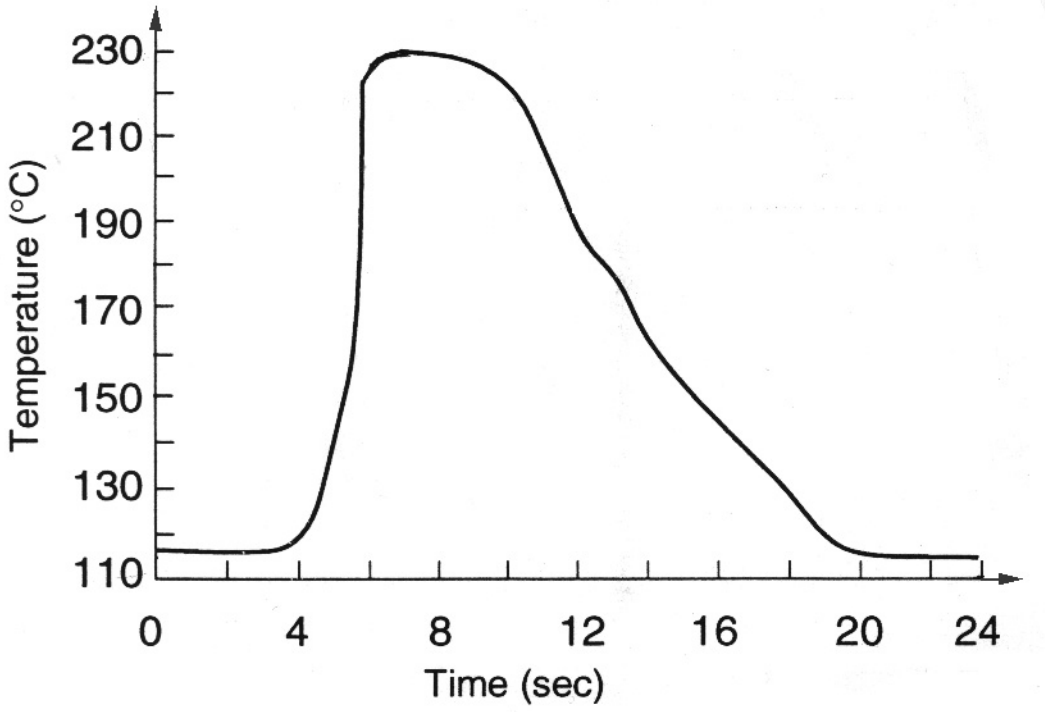


Fig. 7.32: Temperature profile for thermode soldering.

Some of the advantages of thermode soldering are:

- The component is held firmly during placement / soldering and cannot move out of position

- The leads are pressed down, and deviation from coplanarity is not critical
- Only leads and solder lands are heated, giving little thermal stress to the component body.

Disadvantages:

- The method is time consuming, as the components are soldered one by one
- One thermode is required for each component size. The thermodes are expensive and thermode change in the placement machine is time consuming.

Laser soldering uses a powerful, focused (CO_2 -) laser that can heat each solder joint by a system of movable mirrors. The mirrors are controlled by a computer, with CAD information on component location, laser energy needed to melt the solder in each joint, etc. The method is slow (maximum some 10 joints per second), the equipment is expensive, and laser soldering is not yet much used.

7.3.3 Component mounting

SMDs are usually mounted automatically, except for prototyping. Pick-and-place machines are normally used for the mounting.

The Siemens machine in Figure 7.33 illustrates the principles of a pick-and-place machine. The PWBs are fed from the magazine at the left. The boards move through the machine on a rail. They stop at two locations, underneath placement heads nos. 1 and 2. These heads are mounted on a common arm that moves synchronously in the x- and y direction. On head no. 1, there may be an adhesive dispenser (for wave solder process) or a component picking tool. On head no. 2, there will always be a component picking tool. Head no. 2 may pick and mount components, while head no 1 may put adhesive dots on the next board.

The picking tool is most often a small vacuum pipette, with computer control of the vacuum. Alternatively, there may be 2 or 4 small gripper arms, "claws", see Figure 7.34 a). Such tools can be used for coarse electrical testing of two-terminal components while they are mounted. Because of the big difference in component sizes, some machines have several picking tools that can interchange automatically during operation.

Different types of component feeders are placed in the component storage area. They may be modules for component tapes, component sticks, vibration feeders, see Figure 7.34 c), etc.

Figure 7.34 b) shows details of the component tape during mounting. The protecting cover over the components is removed over the one component in place for mounting. When the component is removed the tape moves to bring the next component into place.

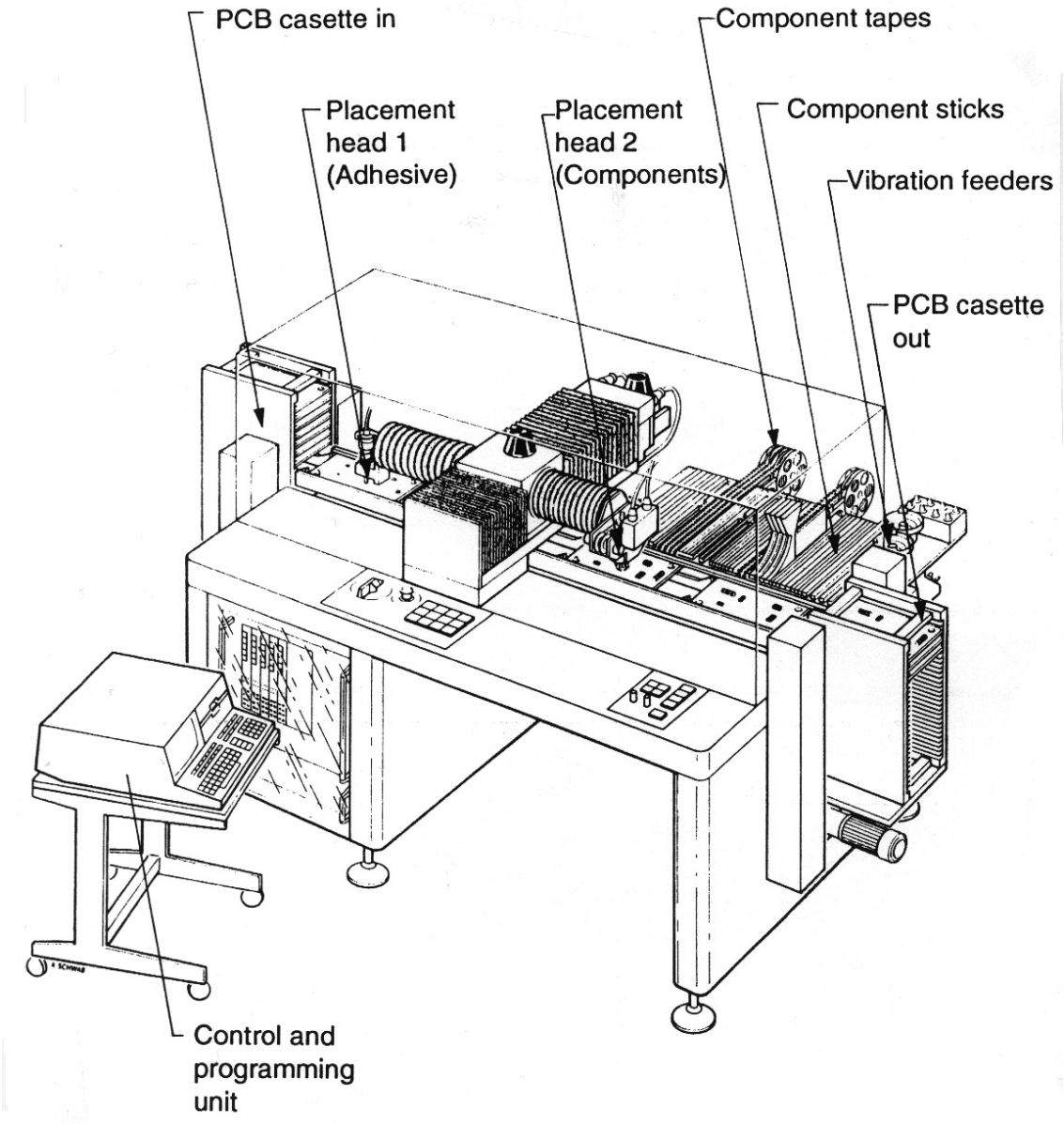


Fig. 7.33: SMD pick-and-place machine (Siemens).
The mounting head may also include an electronic vision system for very accurate placement of fine pitch components.

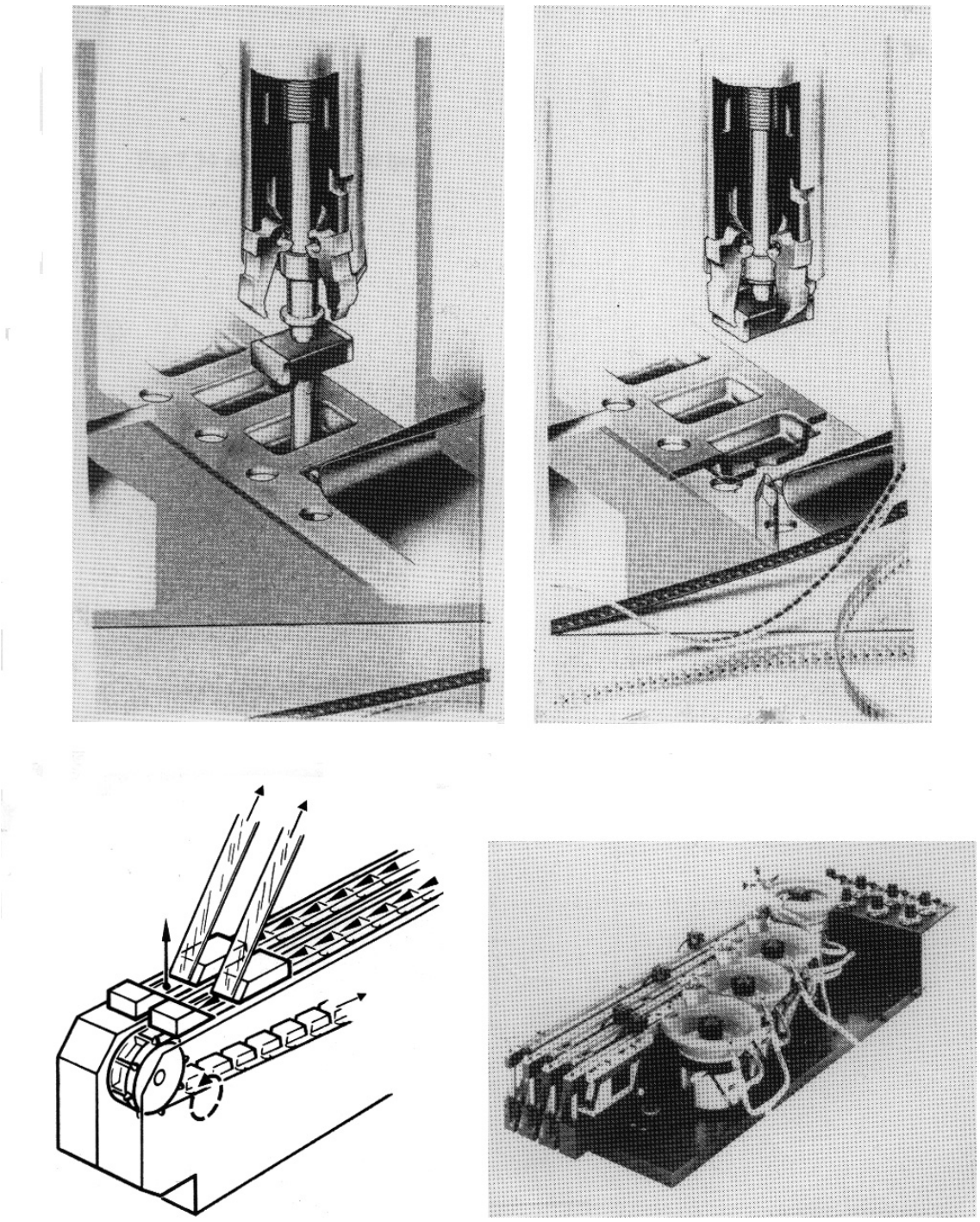
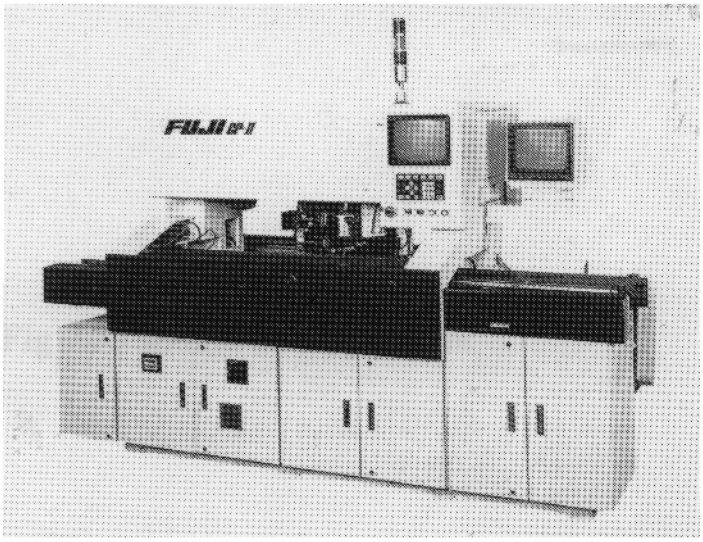


Fig. 7.34: a): Mechanical gripper in pick-and-place machine. b): Detail of the component tape when a component is in position for picking. c): Vibration feeder.

The machine is computer controlled. The information to the control system may be generated in the CAD system, with appropriate post processing. Alternatively,

it may be off-line programmed. Some very high volume machines have many grippers, firmly mounted in the right positions for components to a given type of board. Then all components are mounted simultaneously. These machines are said to be hardware controlled, rather than the more common programmable, software controlled machines.

Other examples of pick-and-place machines are shown in figs. 7.35 - 7.36. Typical placement capacity for software controlled machines is 2000 - 15000 components per hour. Placement accuracy: 0.05 - 0.2 mm.



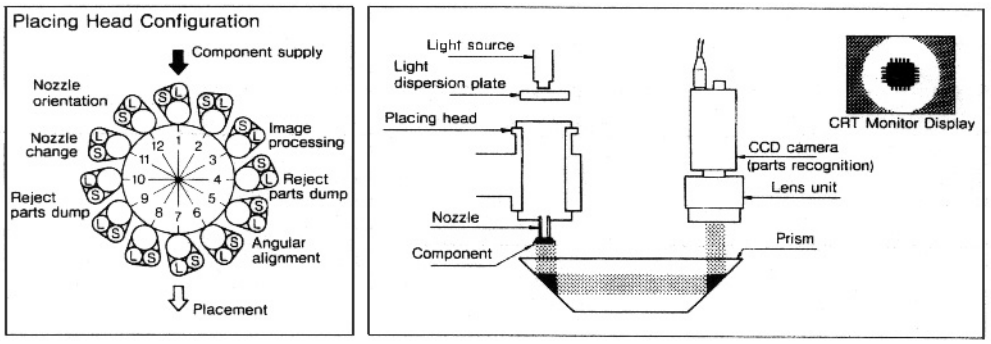


Fig. 7.35: Fuji CP-II pick-and-place machine. The machine has magazine for over 100 types of small components, nominal speed up to 15 000 components per hour, placement accuracy 0.10 mm. It has a rotating head with 12 positions, bottom figure, and two alternative tools at each position. There are components at all 12 positions at any time, with a separate operation being performed. A CCD camera shows the accurate position and orientation on a CRT screen (Fuji).

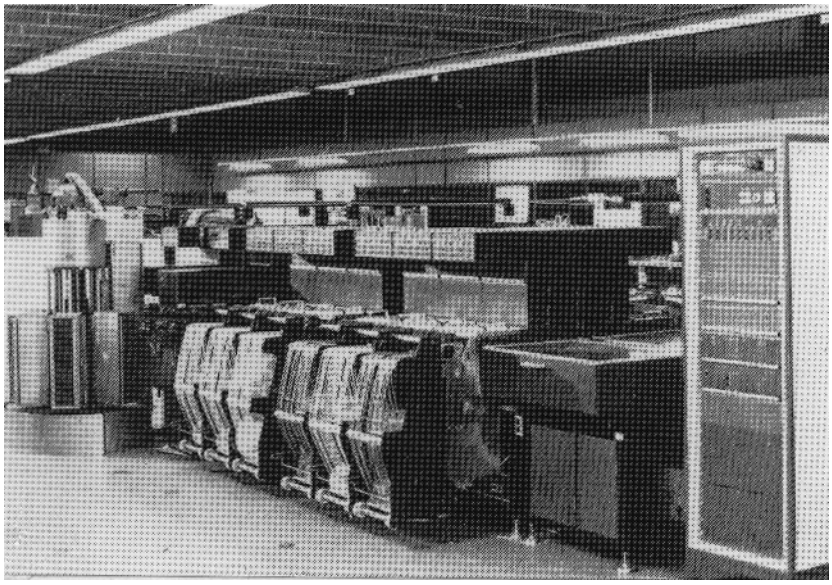


Fig. 7.36: Philips large hardware controlled pick-and-place machine.

7.3.4 Repair

Removal of soldered SMD components is done by heating to melt the solder by specially heated tweezers or "tongs", see Figure 7. 37 a), for small components. For ICs, a hot-air equipment is generally used. An early version is shown in Figure 7. 37 b). It has one air blower from underneath and one from above. The air temperature can be separately controlled for the two. Nozzles are mounted at the end of the air outlet, to limit the heated area. When the solder melts, the component is manually removed by tweezers.

More modern equipment has air nozzles that only blow the hot air at the terminals and solder lands, limiting the heated area and reducing the thermal stress on neighbouring components.

Remaining adhesive and solder must be removed and additional solder added if need be, before flux is added and a new component soldered in by a small solder iron/heating torch or with the same repair tool.

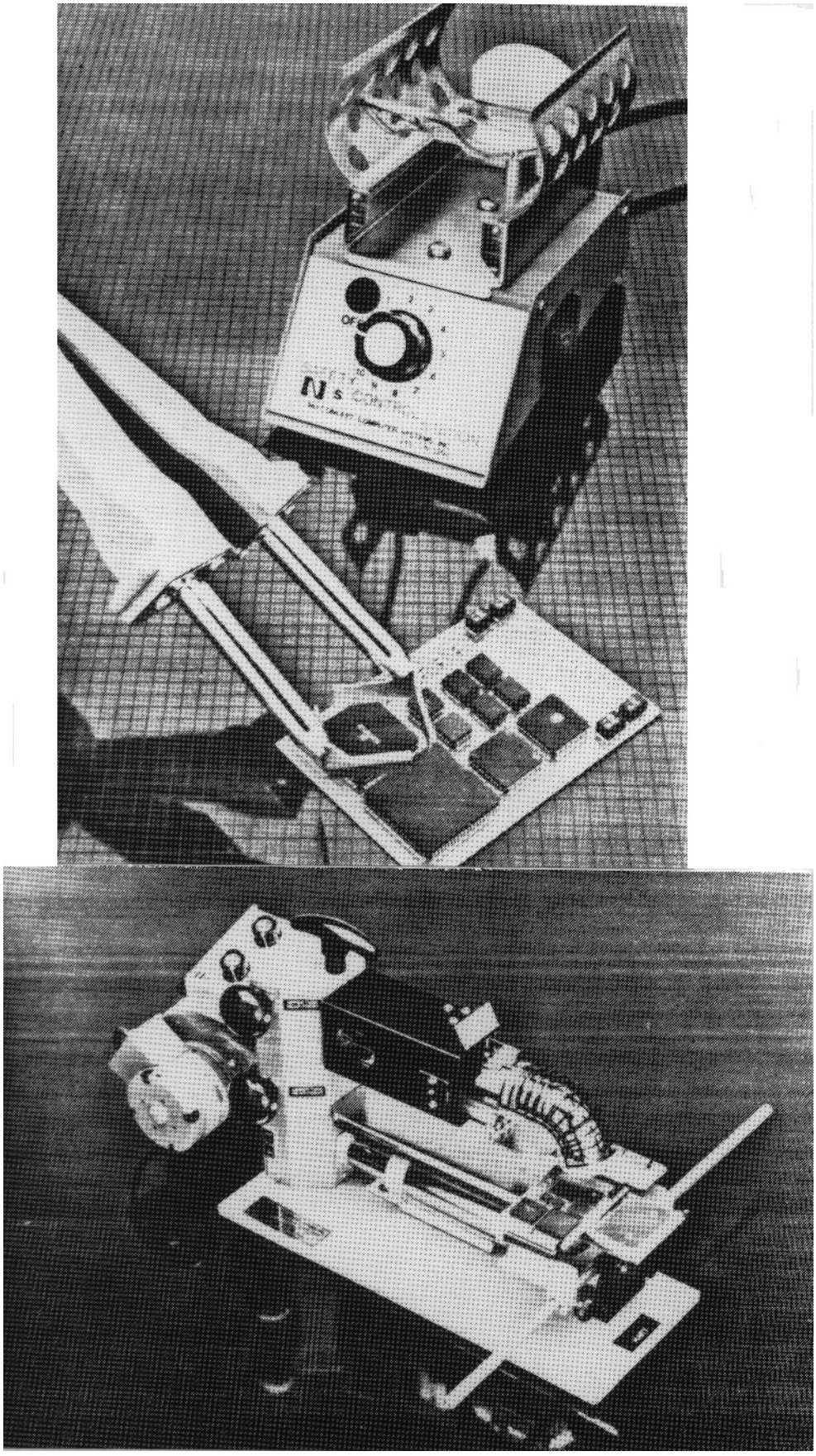


Fig. 7.37: Repair equipment for SMDs. a): Heated tweezers for de-soldering of PLCC packages. b): Hot air blower (HART).

7.3.5 Solder faults

The most common faults in wave soldering, particularly for surface mounting, are the following:

- Solder bridges, shorting terminals or neighbouring components.
  Possible reasons:
  * Incorrectly adjusted solder machine (or unsuitable machine)
  * Bad design; incorrect dimensions on solder pads, components too close, component oriented wrong way
  * Component not suited for wave soldering.

- Dry solder joints.
  Possible reasons:
  * Poor wetting or poor solderability on PCB or component
  * Shadowing
  * Contaminated solder
  * Adhesive on solder land
  * Too weak flux
  * Too low pre-heat temperature.

- Components missing.
  Possible reasons:
  * Too little adhesive
  * Adhesive too dry when component mounted
  * Adhesive too low viscosity
  * Mounting error.

The most common faults in reflow soldering are the following:

- Short circuit between components/terminals.
  Possible reason:
  * Solder balls. This means that the whole amount of solder paste on one solder land has not melted into one sole solder fillet, but some individual solder particles have spread out on the board in an uncontrolled manner, possibly causing shorts at once or at a later time.
  * Too much solder paste
  * Incorrect placement of board during printing.

- Visible solder balls. This is always a reason for board rejection, because of the possibility that the balls will move and cause a short circuit later.
  Possible reasons for solder balls:
  * Oxidised solder paste
  * Too rapid heating
  * Insufficient drying of solder paste before reflow soldering.

- Dry solder joints.
  Possible reasons:
  * Poor solderability
  * Not being coplanar of terminals of IC.

- "Manhattan-" or tombstone-" effect: This means that some small passive components have risen on edge during soldering, see Figure 7.38. It may take place because the solder on one terminal melts before the solder on the other terminal. The molten solder pulls the component up because this minimises the surface forces in the solder.
  Possible reasons:
  * Poor solderability on one of the solder lands
  * Poor layout, giving more heat flow to one solder land, and the temperature reaches the melting point of the solder first on this component end (please refer to Section 6.33).

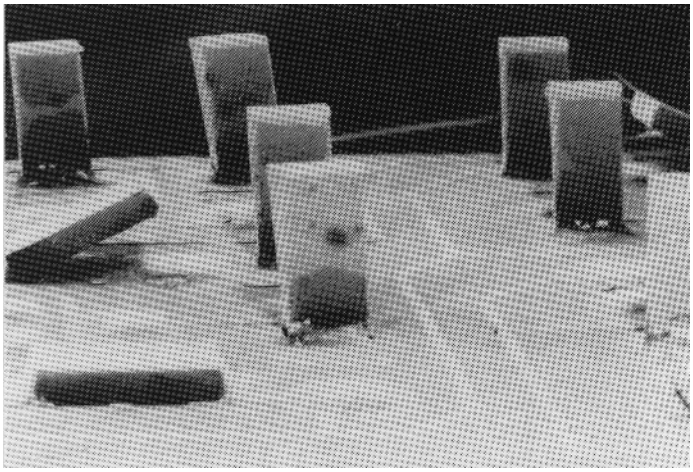


Fig. 7.38: Small SMDs standing on edge due to the "Manhattan-" or "tombstone-" effect.

7.4 ROBOT MOUNTING

Automatic component placement has been common in the electronics industry for some 15 years, based on dedicated machines, made for one type of components or component packages, as described above. Now the use of flexible, programmable robots is rapidly increasing, see Figure 7.39.

An industry robot may be defined as "a re-programmable multi-functional handling machine which, without continuous supervision, can place tools, components or materials in one or more pre-determined patterns of motion, in order to perform different tasks. It can have some amount of "intelligence" which permits it to detect and respond to its environment."

A robot may handle many types of components, and it can fetch the components from many types of feeders or magazines. It can automatically change between different types of tools, suitable for the different component types. These changes are programmed.

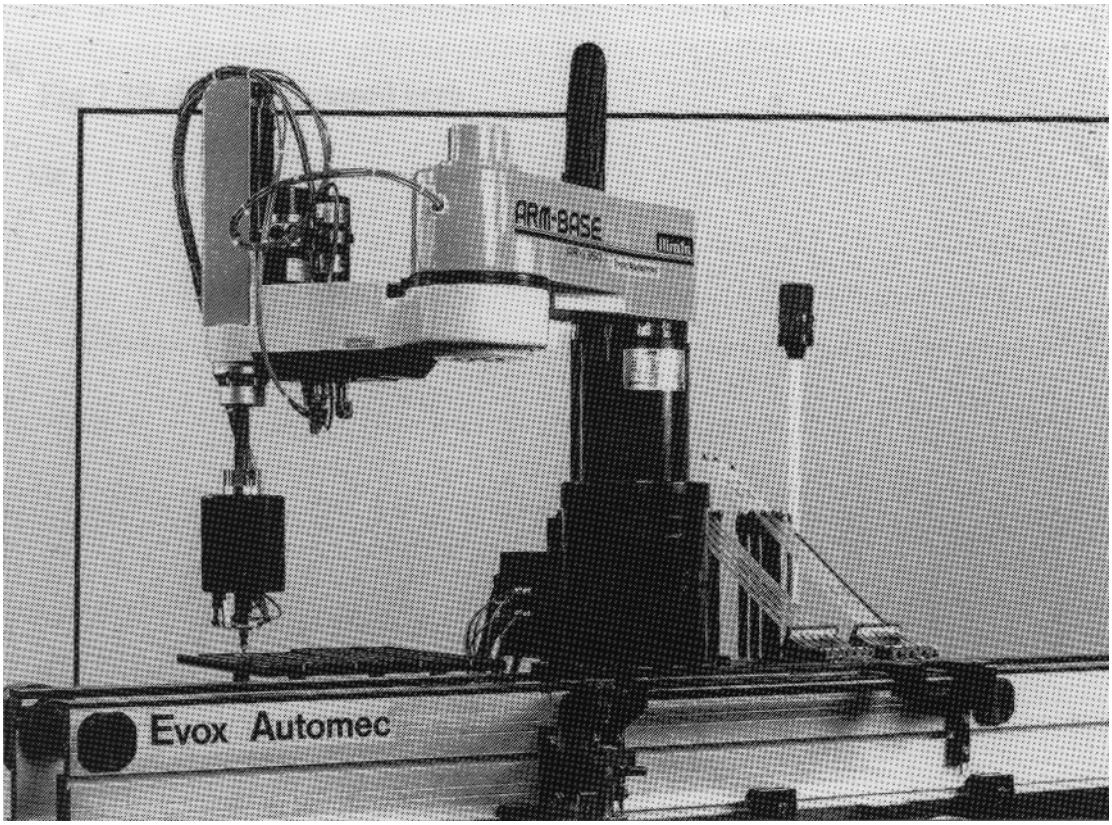


Fig. 7.39: Example of a programmable placement robot for electronics: the SCARA robot.

There are several advantages in using robots for mounting, compared to other methods:

- Flexibility, as mentioned. Once the robot has been installed and programmed, one can change between many types of boards and achieve the same productivity regardless of the number of boards of each type - down to one.
- Uniform product quality: Once the robot has been set up for a task, it will repeat it much more reliably than any human.
- Accuracy: Tolerances in placement position can be 0.02 mm or better (at reduced placement speed).
- Unattended operation is possible over long periods of time (e.g. over night).
- The robot can work in hostile and dangerous environments.
- Robots equipped with sensors can perform useful controls, and tests can be integrated into the production process.

Even if the robot gives the possibility of a high degree of flexibility, much planning is needed before it can be used for a new type of task. A suitable tool is needed for each type of component - even those with odd shapes. The feeder arrangements must be carefully planned, possibly be custom made. There are

often bigger costs connected to the surrounding equipment than to the robot itself.

Although a robot will generally work much faster than humans doing manual mounting, it is much slower than a dedicated pick-and-place machine doing the same operation.

7.4.1 The components of the robot system

Normally the robot system consists of the following parts, see Figure 7.40:

- The manipulator:
  This is the mechanical part that physically performs the task.
- The "learning box":
  From it, the commands and positions are programmed.
- The control cabinet:
  The cabinet contains computer power supply and computer to control I/Os and emergency functions. It sends all command signals to the manipulator and receives signals from the learning box.

The manipulator, or robot arm, consists of joints that have linear or rotary motion. To enable the robot to place an object at an arbitrary position the arm needs at least three joints - linear or rotary. If the object also needs an arbitrary angular position, six joints are needed, of which three must be rotary.

The four main types of robot arms are the following (see Figure 7.41):

- Cartesian arm with three linear joints.
- Cylinder co-ordinates arm with two linear and one rotating joint.
- Spherical co-ordinate arm, with one linear and two rotating joints.
- "Human-like" arm with three rotating joints.

A special type of cylinder co-ordinates arm is the "SCARA" (Selective Compliance Arm Robot Assembly) with two rotating joints in the same plane, and one linear joint in the plane perpendicular to that plane, see Figure 7.39. They are much used in assembly and mounting operations, and they are fast and accurate.

Robots are driven pneumatically (by air), hydraulically (by liquid) and/or by electric motors.

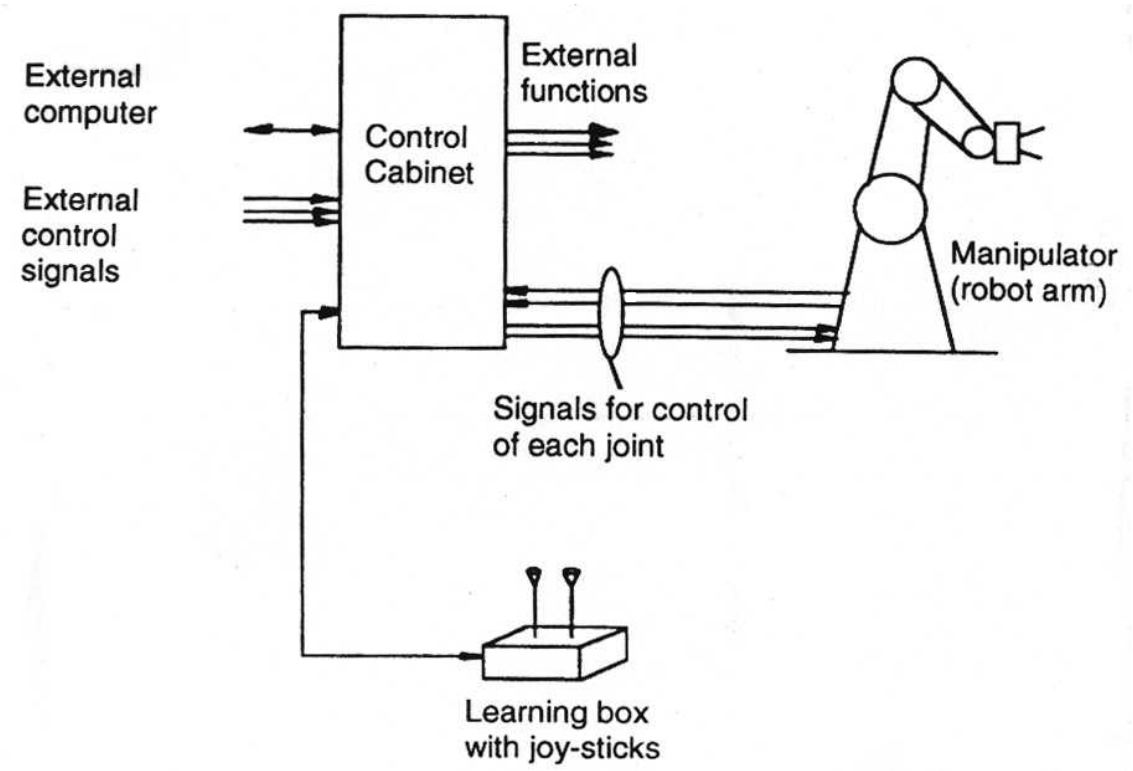


Fig. 7.40: The main components of a robot system.

7.4.2 Programming

The programming takes place in several ways:

- "Guide - and - learn":
  The robot is guided through the desired path by guiding the tool on the robot arm. The control system automatically reads the positions along the path and remembers the co-ordinates.
- "Jog - and - learn":
  The robot arm is moved along the desired path by commands from joysticks and control switches.
- "Synthetic programming":
  The co-ordinates for all the points in a program are written directly into the memory of the control system by off-line programming. When the robot is to mount components on a PCB, this can be done automatically from information generated in the CAD system that is used for lay-out of the PCB.

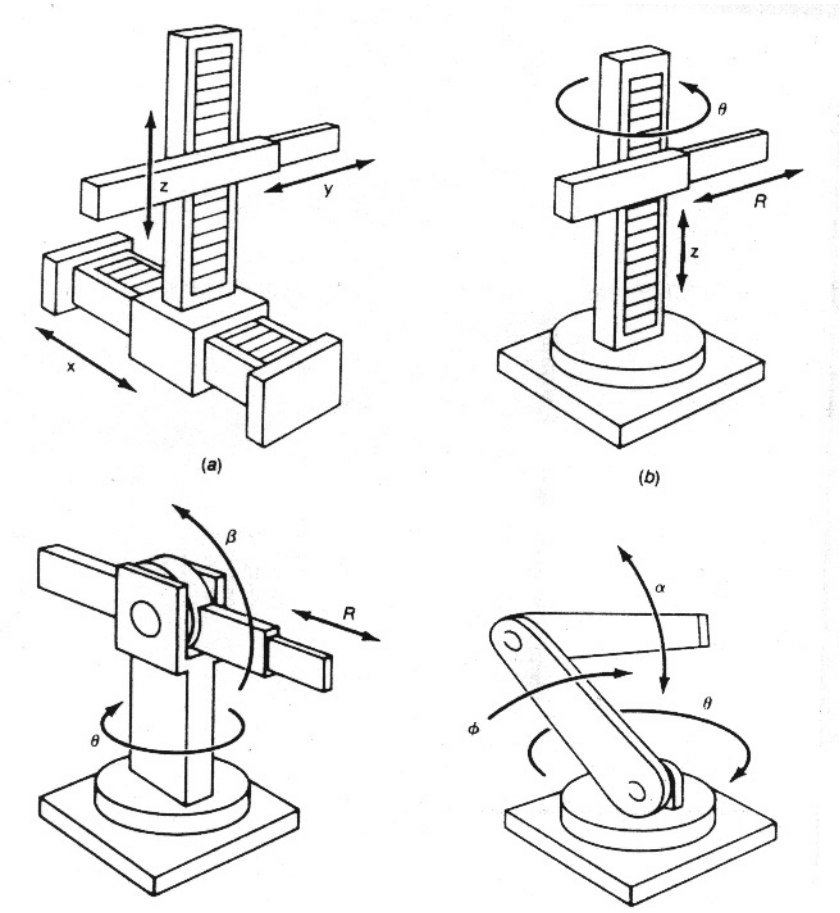


Fig. 7.41: Types of robot arms: a): Cartesian motion, b): Cylindrical, c): Spherical, d): "Human like". The SCARA robot is a special version of the cylindrical type.

7.4.3 Auxiliary equipment in the system

Auxiliary equipment is everything in the robot system that is not directly part of the manipulator and control system. It may include:

- Picking tools
- Feeders
- Sensors and actuators
- Special equipment.

The most common types of picking tools are mechanical and vacuum tools, similarly to those used in pick-and-place machines for SMD placement. The robot may also change tool automatically, or have a multi-tool head, see Figure 7.42.

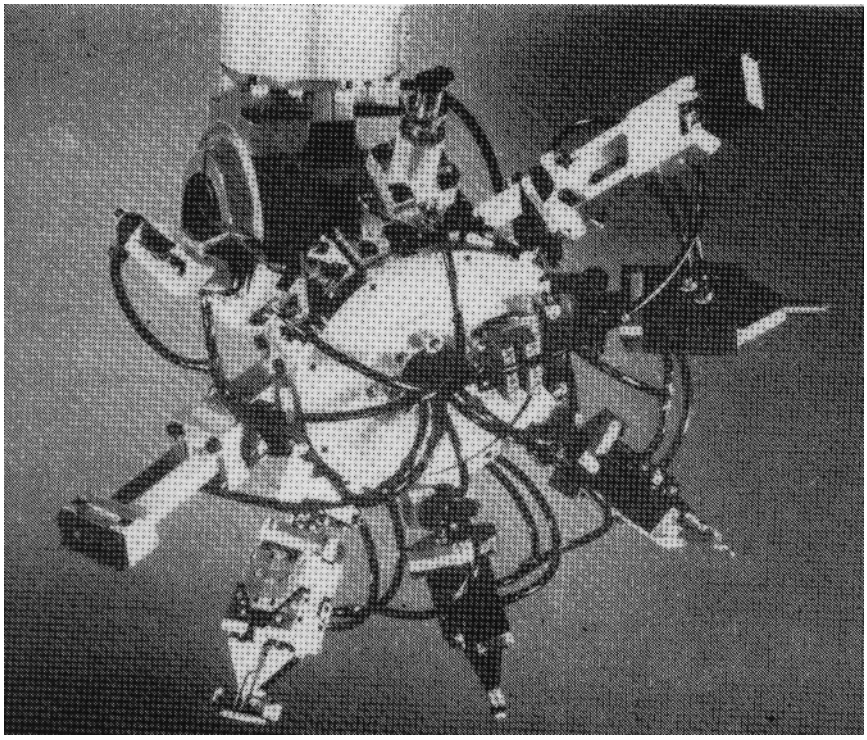


Fig. 7.42: Multi gripper head.

A simple robot cell for component placement is shown in Figure 7.43.

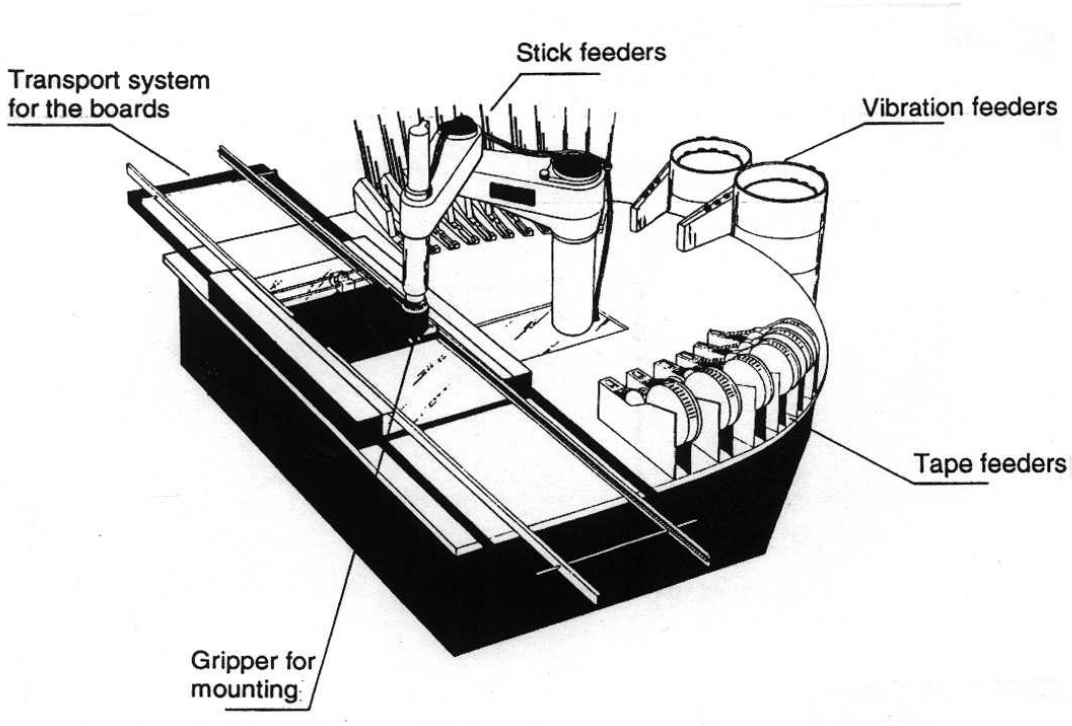


Fig. 7.43: Robot cell for electronic component placement (Adept).

Special equipment is tailored to each task. For an example, solder equipment can be mounted on the robot arm, as well as a solder paste dispenser or an adhesive dispenser. The robot can place the component in a special cut-and-clinch tool for component terminals and pick up the component after the operation has been performed, etc.

If the robot is equipped with sensors and actuators, it can perform additional useful functions such as:

- Provide safety for the user
- Control the manipulator (position- or force sensors, etc.)
- Avoid collision
- Inspection (pattern recognition, "vision system")
- Detect and automatically react to fault situations,
- etc.

The use of sensors can improve the robot capability, but it may increase the cost of the system significantly.

Modern robot control systems can work on several tasks at the same time: control the manipulator, feeders and operator communication, react on sensor signals, etc.

7.4.4 Areas of application for robot mounting

Robots are useful, among other things, for the following tasks in electronics production:

- Component mounting
- Handling of boards/components during testing
- Automatic trimming during testing
- Screwing and gluing operations
- Soldering, etc.
- Production of special components (e.g. winding coils)
- Final assembly of board/rack/chassis.

Products should be designed for robot mounting, i.e. already in the development phase components, placement, fastening method, etc. should be chosen for an optimal use of the robot.

7.5 SEQUENCE IN THE PROCESS OF SMD- AND MIXED SMD/HOLE MOUNTED PCB's

For surface mounted boards and boards with mixed SMD/hole mounted components, several mounting and soldering processes are included. The sequence is not arbitrary, and it must be planned in the design phase. It must also be planned on what side each component is to be mounted, considering that soldering/heating processes it will be exposed to. As mentioned previously, not all components can withstand the wave soldering process, some components are not suitable for it (due to generation of solder bridges, etc.). Some components cannot stand the heat of any mass solder processes and may have to be hand mounted and hand soldered later in the process.

In Figure 6.5, the main types of boards were shown. Figure 6.5 a) showed SMDs on one side of the board only. Normally solder paste printing and reflow soldering will be used for such a board. Figure 6.5.b) showed SMDs on both sides. Two reflow processes may be used. Figure 6.5.c) showed hole components on one side, SMDs on the other. In this case, all components may be soldered simultaneously by wave soldering. In Figure 6.5.d), we had SMDs on both sides and hole components on one side. A combination of reflow soldering and wave soldering is used.

Figure 7.44 a) - d) show process sequences for various types of boards. When the board has SMDs on both sides, see Figure 7.43 b), the adhesive step may often be omitted. In an IR furnace, the heat below the board may be reduced such that the solder on the top surface melts while the solder on the bottom side remains solid.

7.6 TESTING OF PCB's

Testing takes place at various stages in the development of a product. Here we are concerned with volume testing during the production process, which normally consists of visual tests (which for very high volume production may be replaced by electronic inspection using vision systems) and electrical tests. The testing is done several times, at different level: component-, board-, module-, and system test.

7.6.1 Component testing

Previously an incoming test of components when they arrived was common. Today it is more common to purchase components on a "ship-to-stock" or "ship-to-line" basis. In this case, the component manufacturer does the testing, and test documentation can be supplied to the customer.

7.6.2 Mechanical parts for the PCB testing

The functional test and in-circuit test principles were described in Section 6.4. Here we shall only discuss the fixture and mechanical parts needed for in-circuit testing.

Most commonly, the board has wiring and components on both sides. If possible, the testing should be done on one side only. Two methods to achieve this are shown in fig .7.45. Fig .7.46 shows a "bed of nails" test fixture for the in-circuit testing. Figure 7.47 shows details of single sided and double sided test fixtures and Figure 7.48 shows test pins used.

Normally the board will be pressed against the fixture by over pressure. This must be planned during the design (position of high components, holes in the board, etc.). The double sided fixture is mechanically complicated and expensive. The test pins are pressure loaded and normally dimensioned for placement on a matrix of minimum 0.1" distances. Pins for 0.05" distances are available, but they are mechanically less robust.

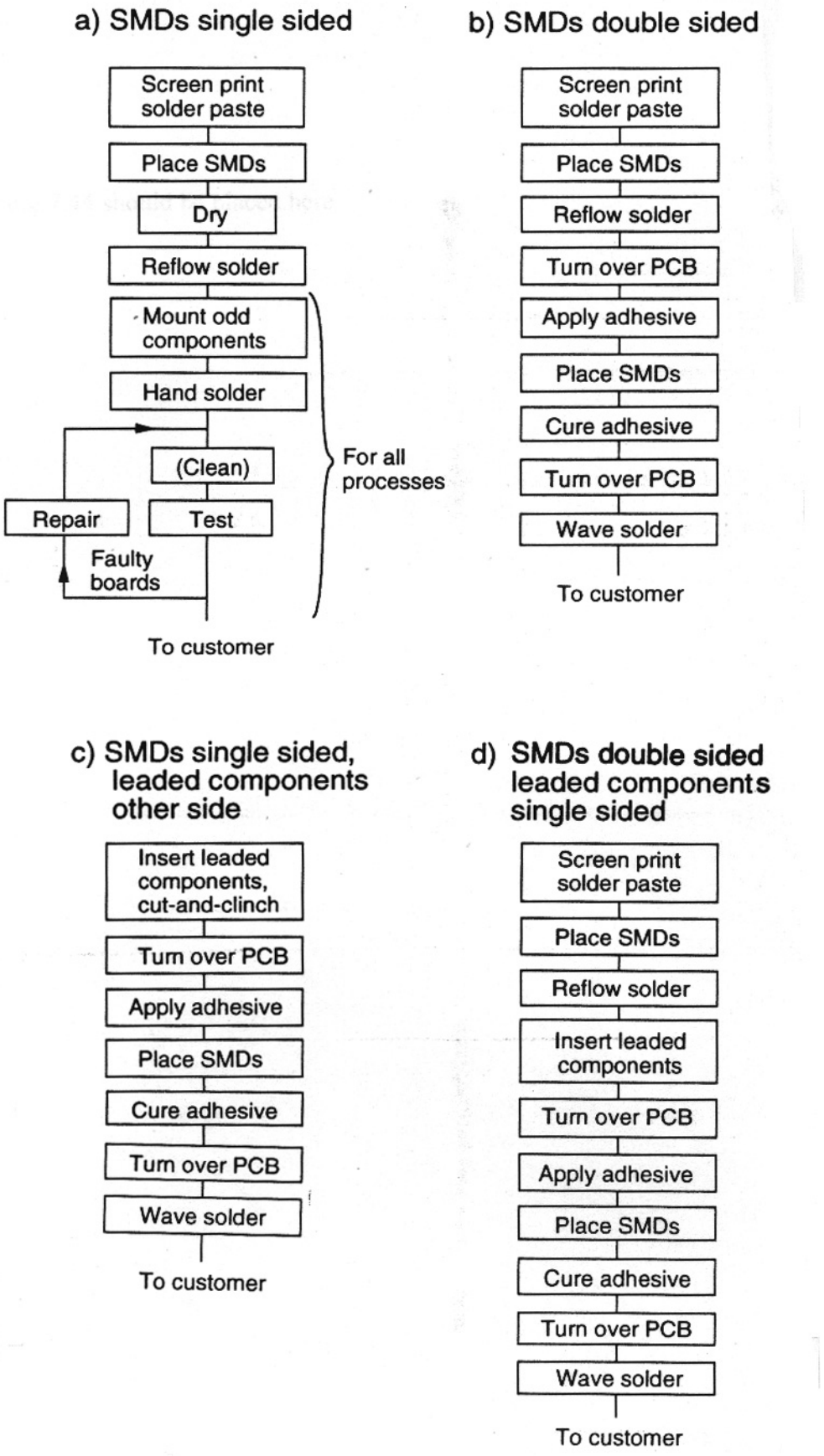


Fig. 7.44: Process sequences for boards with different types of components on the two sides. The steps marked "For all processes" on figure a) are not repeated on the other figures.

Placement of the test points is an important part of the design, please refer to Section 6.4. Figure 7.49 shows an example of a poorly designed test point, on a component lead. If the solder contact is bad the test probe will press the lead down to make contact, and the fault is not detected.

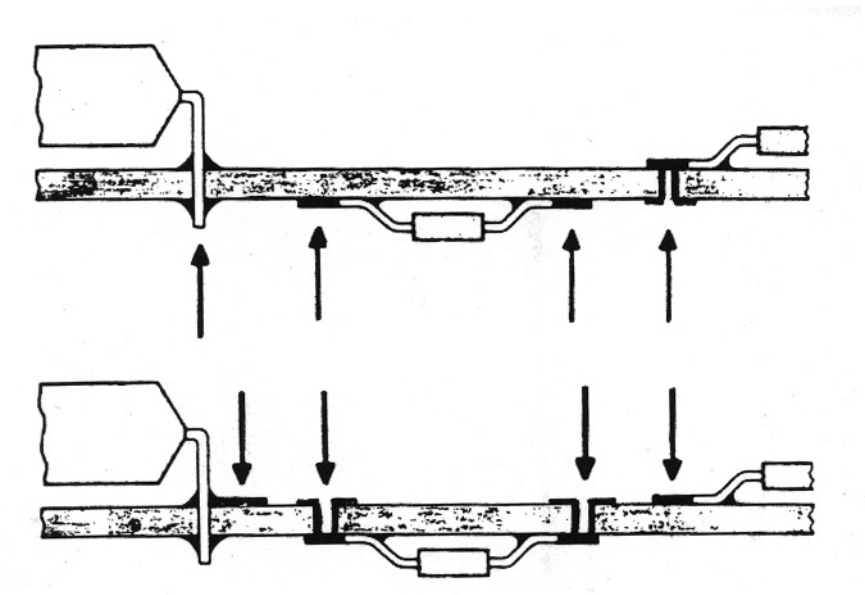


Fig. 7.45: Two methods for single sided test of a board with components on both sides.

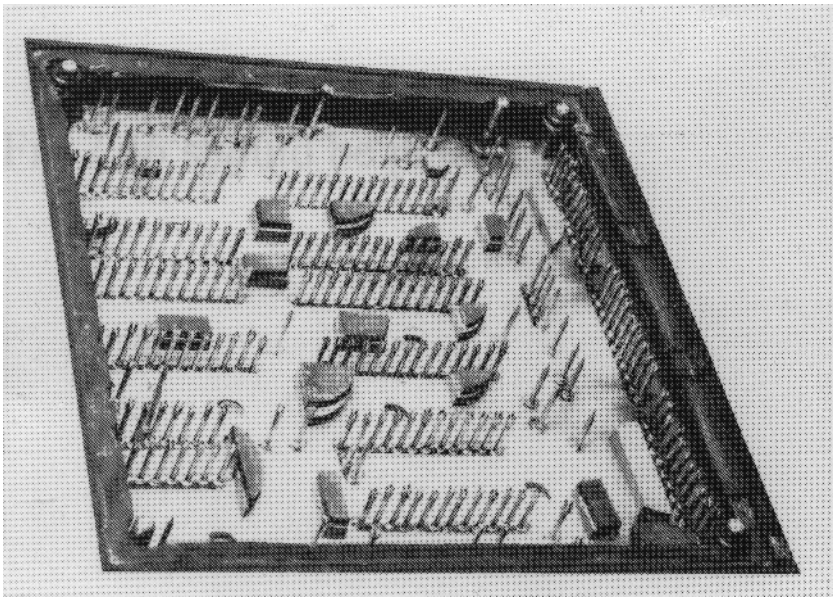


Fig. 7.46: Bed-of-nails test fixture.

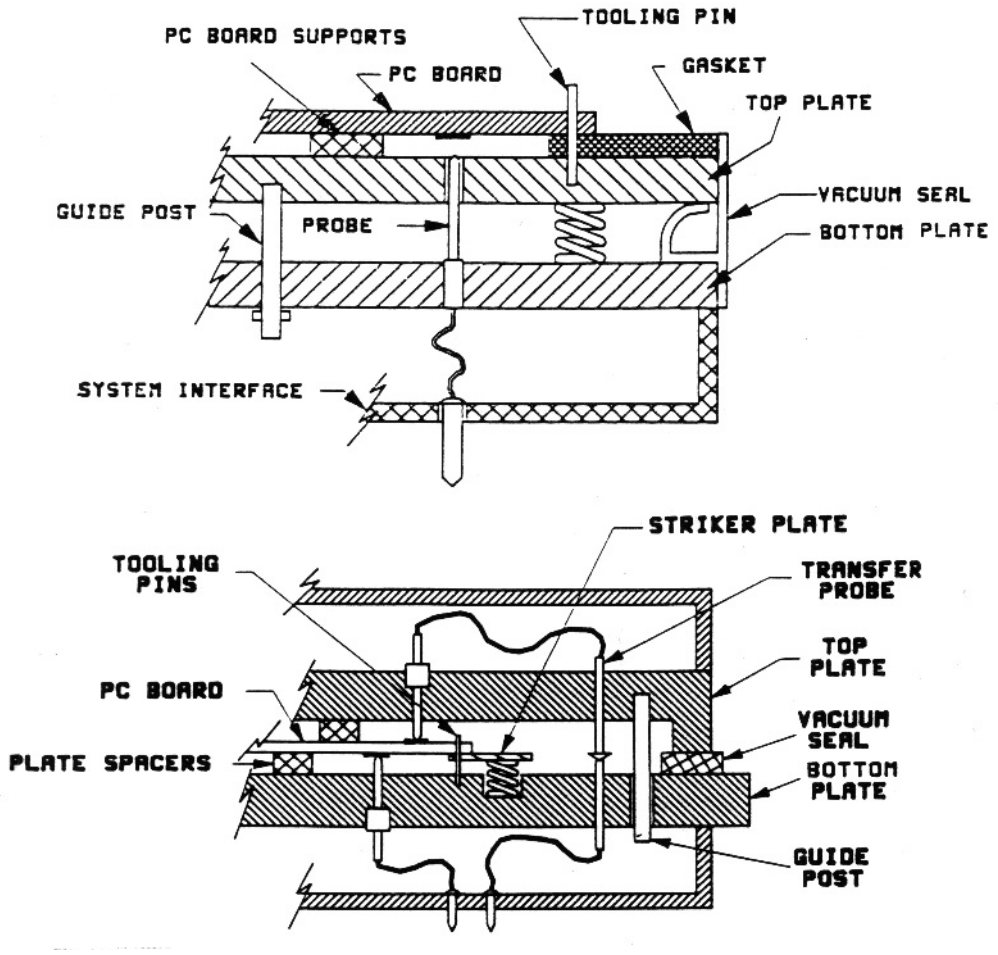


Fig. 7.47: a) Detail of single sided test fixture, b) double sided fixture.

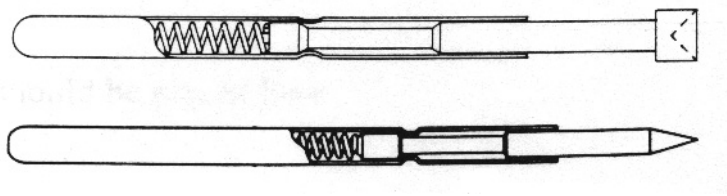


Fig. 7.48: Two types of test pins.

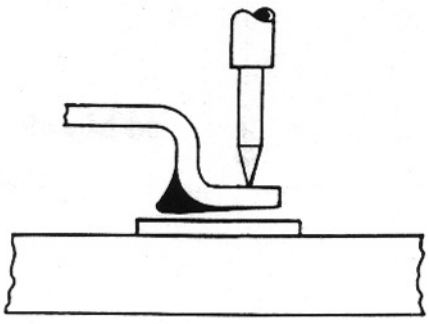


Fig. 7.49: Unacceptable testing. The test point should be on the Cu foil on the board, not on the component lead.

7.6.3 "Zero defect" philosophy

After each step in the production process, the value of the product increases. Repairs and changes may be more complicated to perform. Discarding a faulty product is more costly the later in the process it happens. Therefore, it is important to detect faults as soon as possible after they have been made and make the test strategy accordingly.

Earlier it was normal to accept a high fault rate, repair the faults and test again. Today the goal is that faults should not occur. Repairs are costly, and it is likely that other units just passing the test may fail later, in the field, where the consequences are much worse. Faults tell that there is something wrong with the process, the components, or the design. The correct procedure is to remove the cause of the fault. "Fix the process, not the product" is the principle today.

REFERENCES

[7.1] G. Leonida: "Handbook of printed circuit design, manufacture, components and assembly". (Electrochemical Publications, 1981.)

[7.2] R.J. Klein Wassink: "Soldering in Electronics" (Electrochemical Publications, 1984).

[7.3] "Robots for electronics production". EPF Workshop October 1988,
and: EPF-report R 20: "Robot systems for electronics production", February 1988.

[7.4] L. Halbo et al.: "Second generation SMT: Components, substrates, mounting and soldering". EPF-report R 29, 1989.

[7.5] C. F. Coombs: "Printed circuits handbook". (3rd Ed., McGraw Hill, 1988).

[7.6] C. Lea: "A scientific guide to surface mount technology". (Electrochemical Publications, 1988.)

[7.7] G. Ginsberg: "Surfacemount and related technologies". (Marcel Dekker, 1989.)

[7.8] ANSI/IPC-CM-770C: "Printed circuit board component mounting". (The Institute of Interconnecting and Packaging Electronic Circuits, 1987.)

[7.9] J. F. Pawling: Surface mount assemblies". (Electrochemical Publications, 1987.)

[7.10] J. Wangensteen: " Testing of surface mounted PCBs". EKF report R 43, March 1986.

[7.11] A. Gabrielsen et al.: "In-circuit testing of surface mounted PCBs". EKF report R 60, December 1987.

CHAPTER 8

HYBRID TECHNOLOGY AND MULTICHIP MODULES

8.1 INTRODUCTION

Hybrid means composite. In the context of hybrid technology, we mean a mixture of integrated components: conductors, resistors, capacitors, etc., that are manufactured as part of the substrate - and discrete components that are soldered or bonded on top of the substrate.

The traditional types of hybrid technology are thick film- and thin film hybrid technologies, that have been used since early in the 1960´s. Later polymer thick film technology (PTF) has appeared. During the last years multilayer ceramic and new forms of multilayer thin film technologies have received much attention for multichip modules (MCMs) [8.21].

The main goal of using hybrid circuits (apart from PTF), is saving space, volume and weight compared to ordinary printed circuit boards. However, we can also achieve superior high frequency properties and very high reliability. This makes hybrid circuits suitable for demanding military systems, space applications, medical electronics, as well as computers, telecommunication equipment, etc.

8.2 THICK FILM HYBRID TECHNOLOGY

8.2.1 Substrates

Important properties of thick film substrate materials are:

- Good dimensional stability during high temperature processing
- Good adhesion between substrate and printed materials
- High thermal conductivity
- A thermal coefficient of expansion matching that of other materials in the circuit
- High electrical resistivity that gives isolation between components
- Low dielectric constant
- Low dielectric loss tangent (for microwave circuits)
- Good machinability
- Low price.

No single material will satisfy all these requirements.

Various types of ceramic are used as thick film substrate materials, with 96 % Al_2O_3 (alumina) as the dominant one. Alumina has many good electrical and mechanical properties, please refer to Table 8.1. It has good dimensional stability, but because it shrinks close to 20 % during the fabrication, the dimension control is limited to typically 0.5 - 1 %.

Table 8.1 Properties of substrate materials for hybrid technology, and other important properties (In: inorganic, Semi: semiconductor, P: plastic) [8.3]

Material	Relative permit-ivity ε_r	Dielectric Loss Factor (at 10 GHz, 25°C), tan δ_ε	Specific Thermal Conduct-ivity K_{th} [W/cm °K]	Linear Thermal Expansion Coefficient (at 25°C) $\Delta l/l/\Delta T$ [10^{-6}/°K]	Temper-ature Coefficient of ε_ρ $\Delta\varepsilon/\varepsilon\Delta T$ [10^{-6}/°K]	Type	Remarks
Al_2O_3 ceramic (99.5% pure)	9,8	0,0001	0,37	6,3	+136	In	
Al_2O_3 ceramic (96% pure)	9,4	0,001	0,35	6,4		In	
Sapphire	9,4; 1,6	0,0001	0,42	6	+110 +140	In	Aniso-tropic
Quartz glass	3,78	0,0001	0,017	0,55	+13	In	
Corning glass	5,75	0,0036	0,012	4,6		In	
Beryllium oxide Ceramic (BeO) (98%)	6,3	0,006	2,1	6,1	+107	In	Dust is poison-ous
Semi-Insulating GaAs	12,9	0,002	0,46	5,7		Semi	
(High-resistive) Silicon ($\rho=10^3$ ohm cm)	11,9	0,015	1,45	4,2		Semi	
PTFE	2,1	0,0003	0,002	106	+350	P	
Polyolefin (Glass reinforced)	2,32	0,0007	0,005	108	+480	P	
PTFE	2,55	0,001	0,003	16-100		P	
Aluminium			2,2	23,8			For
Copper			3,93	17			comp-
Invar				1,5			arison

It is brittle, and this limits the maximum size to 10 - 15 cm. After the material has been sintered, it is not easy to shape it. However, it can easily be cut by breaking after a partial cut is made by a high power laser. For small circuits, it is common to print and mount components on many substrates that are produced together and then broken apart in the end, to make a rational production process. Holes through the substrate may also be made by laser, but it is simpler to form the substrate contour and punch holes while the ceramic is pliable, before the sintering. Please refer to Sections 3.2.3 and 8.5 below.

The thermal conductivity of 20 - 30 W/ ^oC is approximately 100 times better than for organic substrate materials, and the low thermal coefficient of expansion, 6 ppm/^oC, is advantageous for the mounting of ceramic components and semiconductor chips.

For circuits with very high power dissipation AlN substrates are used today, with 5 times or higher thermal conductivity than Al_2O_3. Many properties are similar to those of Al_2O_3. The thermal coefficient of expansion is somewhat lower, 4.5

ppm/°C. This, and different surface properties, give a need for special printing pastes on AlN, to avoid flaking off during the high temperature processing. BeO has even higher thermal conductivity than AlN. However, its use is limited by the fact that dust and vapour from BeO are very poisonous. High price is also connected to this fact.

For high volume products with lower electrical demands, enamel coated metal is used as substrate, to some extent. Big circuits can be made, and we achieve electrical grounding in the substrate. For details see [8.1].

8.2.2 Materials for conductors, resistors, dielectrics

Conductors, resistors and dielectric materials are applied in paste form by screen printing and they are transformed/sintered by heating to high temperature, "firing". The pastes have three main ingredients:

- Functional element (metal-, alloy- or oxide particles)
- Matrix or "binder" (glass particles)
- Organic solvents and "temporary binder".

The organic, temporary binders are polymers that give control over the printing properties. They decompose and evaporate early in the firing process, together with the solvents. The glass particles melt in the firing process, adhere to the substrate, bind the active particles together and give stability for the circuit. The high firing temperature, typically 800 - 900 °C, see Figure 8.1, is important for the long term stability and reliability.

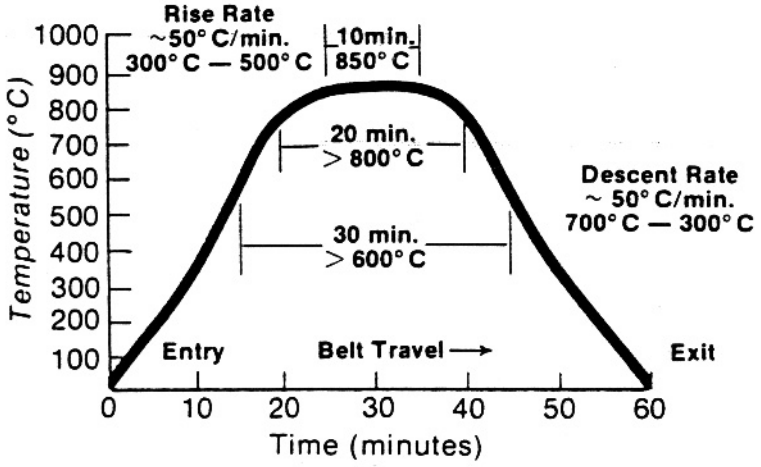


Fig. 8.1 Typical temperature profile for thick film firing [8.1]

Conductors

The conducting pastes should give:

- High electrical conductivity
- Strong adhesion to the substrate
- Excellent solderability for soldering of packaged components
- Reliable bondability for wire bonding of naked IC chips.

Price is also an important parameter.

Normally one conductor paste can not satisfy all these criteria, and it is necessary to make several conductor prints.

The most used conductor systems are gold, copper, alloys of palladium/silver, palladium/gold and platinum/gold, with properties shown in Table 8.2. Noble metal systems are used because the heat treatment takes place at above 800 °C, where other metals are ruined by oxidation. However, gold and platinum are expensive materials, so the material cost is an important factor in the final price of the circuit. Gold is very well suited as basis for bonding, but it is not suitable for soldering. This is because gold is very quickly dissolved in solder metal during the soldering process, and it gives a brittle intermetallic composition with poor reliability properties. Pure silver has a strong tendency for migration [8.1], which may cause reliability problems after some time. However, silver/palladium gives little migration, it is excellent for soldering, and is well suited for making contact areas for printed thick film resistors. Therefore, this alloy is the most used as conductor material, although it has lower conductivity than the pure elemental conductors. Silver is also used in alloys with platinum.

Copper has high conductivity and low price. However, strong oxidation in air at high temperature makes it necessary that copper must be fired in a neutral nitrogen atmosphere. That gives a more complicated and costly process and has impeded the use of copper conductors.

Nickel is also used to some extent, but it has lower electrical conductivity than the other materials.

Typical thicknesses for the conductors are 5 - 10 μm after firing. The sheet resistivity is typically between 2 and 25 mohm/sq, please refer to Table 8.2.

Table 8.2 Properties of thick film conductor systems [8.2]

Comparison of Parameters for Thick-film Conductors			
	AgPd	*Cu*	*Au*
Sheet Resistivity (mohm/❒)	25	1,8	2,5
Breakdown Current (mA/mm width)	3000	10000	10000
Thickness	10-20	15-30	5-15
Minimum With (μm)	150	150	50
Through-hole Diameter	0,4-1,5	0,4-1,5	-
Number of conductor layers	1-3	1-5	1-5
Substrate Area (cm^2)	0,2-100	0,2-200	0,2-50
Substrate Thickness (mm)	0,6-1	0,6-1	0,25-1
Tin-Lead Soldering Properties on Thick Film Conductors			
Parameter	*AgPd*	*Cu*	*Au*
Solderability	Good	Good	Unsolderable
Wetting	Good	Good-excellent	-
Leach Resistance	Fair-good	Excellent	-
Adhesion	Excellent	Excellent	-
Visual Quality	Good	Excellent	-

Resistors

Important properties of thick film resistors are:

- Large range of available resistor values
- High stability
- Low thermal coefficient of resistivity, with little spread over the substrate
- Low voltage dependence of the resistance
- Good noise properties.

The resistor pastes consist of the same three main ingredients as the conductor pastes, but the active elements have lower electrical conductivity. They are most often based on various types of oxides of ruthenium: RuO_2, $BaRuO_3$, $Bi_2Ru_2O_7$. In addition, oxides of iridium, rhodium and osmium are used. They may be produced with sheet resistance down to approximately 1 ohm/sq, and up to 10^9 ohm/sq, for a 25 μm thick print. The sheet resistivity is determined by the active material in the paste, the amount of glass matrix mixed in, and the details in the processing. The tolerance in achieved resistance is lowest for the intermediate values of sheet resistivity.

We obtain termination of the resistors by printing a conductor underneath or on top of the ends of the resistor, see Figure 8.2.

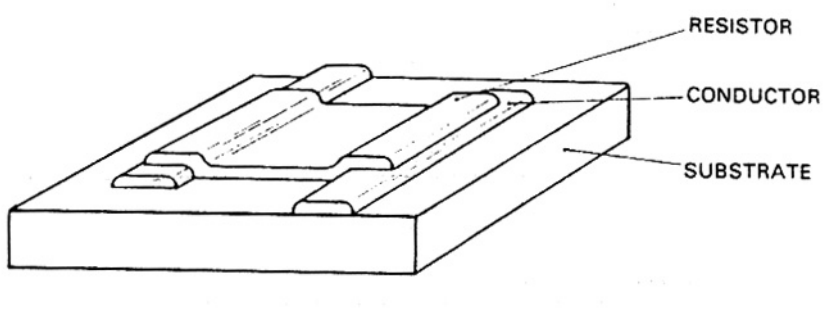


Fig. 8.2 Thick film resistor with termination.

Some typical resistor properties are shown in Table 8.3. Resistance drift lower than 0.5 % under harsh climatic conditions over long periods of time makes thick film hybrid technology attractive for demanding applications. The difference in drift between several resistors on the same substrate is typically 0.1 %. The temperature coefficient of resistance depends on the material, and it is typically in the range +/- 100 - 700 ppm/°C, with variation over a circuit, for resistors printed with the same paste, below +/- 15 ppm/°C.

The tolerance in absolute resistance after printing and firing is typically +/- 10 - 20 %, and the relative tolerance between resistors on the same substrate one order of magnitude lower. However, by laser trimming one can achieve tolerances down to approximately 0.5 % absolute, and 0.1 % relative value.

Table 8.3 Typical properties of thick film resistors [8.1]

Tolerances as fired	±10 – ±20%
Tolerances, laser trimmed	±0.5 - ± 1%
TCRs:	
5 to 100K ohm/sq (-55° to 125°C)	±100 - ±150 ppm/°C
100K to 10M ohm/sq (-55° to 125°C)	±150 - ±750 ppm/°C
Resistance drift after 1,000 hr at 150°C no load	+0.3 to -0.3%
Resistance drift after 1,000 hr at 85°C with 25 watts/in^2	0.25 to 0.3%
Resistance drift, short term overload (2.5 times rated voltage)	<0.5%
Voltage coefficient	20 ppm/(V) (in)
Noise (Quan-Tech):	
At 100 ohm/sq	-30 to -20 dB
At 100 Kohm/sq	0 to +20
Power ratings	40-50 watts/in^2

Dielectrics

Dielectric materials are printed to obtain insulation between various layers of conductors, to produce capacitors, and as passivating cover on top of the whole circuit. For insulation, low capacitance between conductors is desirable and we use materials with low dielectric constant. For capacitors, materials with high dielectric constant are used, to achieve high capacitance with little area consumption. Important properties of dielectric materials:

- High insulation resistance
- High breakdown field
- For insulators: Low dielectric constant
- For capacitors: Suitable dielectric constant, low temperature coefficient and low voltage coefficient of dielectric properties
- Low loss tangent
- Low porosity

For insulation layers, aluminium oxide is the common functional element, together with glass. The glass melts and crystallises during firing at 850 - 950 °C, but it does not melt if heated again. The relative dielectric constant is typically ε_r = 9 - 10, and breakdown field strength 20 V/μm.

The dielectrics for high value capacitors consist of ferroelectric materials with ε_r up to above 1000, similarly to ceramic multilayer capacitors, please refer to Chapter 4. However, the properties of these materials change drastically near the Curie temperature, see Section 4.3 and [8.1]. Barium titanate is used, with additives of strontium, calcium, tin or oxides of zirconium to change the Curie temperature and to reduce the temperature coefficient in the temperature range of use. That gives ε_r = 1000 - 3000 and temperature coefficient up to approximately +/- 5000 ppm/°C. For small capacitors the pastes of magnesium titanate, zinc titanate, titanium oxide, and calcium titanate are used, with ε_r = 12 - 160, and temperature coefficient +/- 200 ppm/°C.

Table 8.4 Typical properties of printed and discrete capacitors [8.2]

Capacitor	Capacitance range	Absolute Tolerance [%]	ε	Isolation Resistance [Mohm]	Tan δ [%]	TCC [ppm/°C]	Voltage Range
Thick-film I	2 pF/mm^2	5 - 20	12	>10^6	<0.25	45	50-200
Thick-film II	8 pF/mm^2	10 - 30	50	>10^4	<1.5	500	50-200
Thick-film III	50 pF/mm^2	10 - 30	500	>10^4	<2.0	2000	50-200
Thick-film IV	150 pF/mm^2	10 - 30	2000	>10^3	<4.0	-400	50-200
Ceramic-chip NPO	1 p F - 4 nF	1 - 10	10	>10^5	<0.1	±30	50-200
Ceramic-chip X7R	0.1 - 1.5 nF	3 - 20	1200	>10^5	<2.5	800	50-200
Tantalum-chip	0.1 - 100 μF	5 - 20	25	Maximum leakage current 0.5 - 3 μA	<6.0	500	4 - 50

Capacitors are not suitable for laser trimming. That, in addition to the above mentioned disadvantages, is the reason why printed capacitors are used only in small values and for uncritical purposes (decoupling capacitors, etc.). Some properties of printed and discrete capacitors are compared in Table 8.4.

Pastes for the protection layer on top of thick film circuits are composed such that they may be fired at lower temperature, approximately 500 °C, and affect the previously printed layers as little as possible.

8.2.3 Production process

The layout of the circuit is made by CAD tools, photo plotting or laser plotting, analogous to the ones used for layout of multilayer PCBs in Chapter 5. Photographic films are produced for the pattern of each layer. From these films, screens for screen printing are produced, using a photolithographic process.

When a print has been made the circuit is dried in an in-line furnace at typically 100 - 150 °C. Then the firing is done in a different furnace at 700 - 1000 °C. The process is repeated for each layer, but all resistor layers are fired in the same process step, after the conductor layers. To achieve good reproducibility for resistors the temperature profile, the top temperature and the time have to be very precisely controlled, maximum deviation in temperature is below 1 °C.

The smallest conductor width that can be achieved with ordinary printing technique is approximately 100 μm. (Using an extra photolithography and etch step this may be reduced to 50 μm.)

It is possible to make conducting contact between the top side and the bottom side of the substrate by printing through holes in the substrate. This is done by sucking the paste through the hole by use of vacuum on the bottom side of the substrate while the printing on the top side is done. To achieve reliable contact the substrate is then turned around and the paste is printed again from the other side in combination with the vacuum. It is common to have all the conductors

and discrete, surface mounted components on one side and the resistors on the other for easy laser trimming.

Figure 8.3 shows the typical process flow for a simple circuit with two conductor layers and one resistor layer. Dielectrics are normally printed twice to avoid pinholes that may cause short circuit faults through the insulating dielectric.

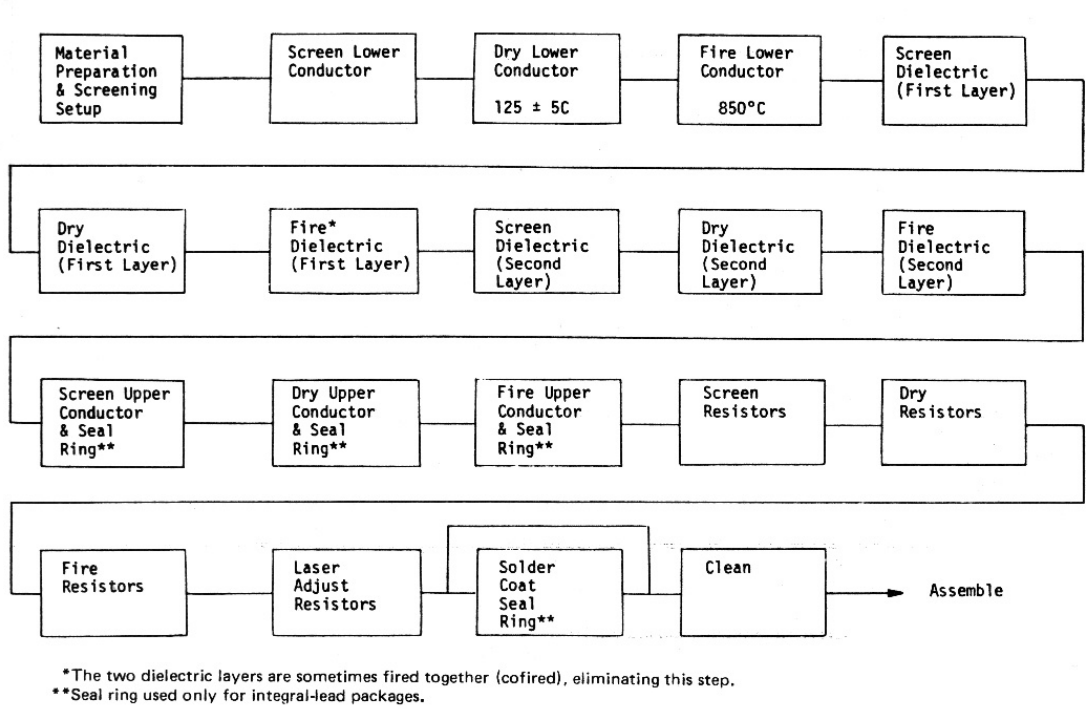


Fig. 8.3 Process flow for production of thick film circuits [8.1]

Testing is normally done on the substrates before component mounting, as well as on the completed circuits with the components mounted. Test probe-cards, as shown in Figure 8.4, are used for the contacting. During the testing the resistors are adjusted by laser trimming (previously sandblasting). It is done by a powerful pulsed YAG-laser automatically focused on one spot of the resistor, evaporating the resistor material, while the resistance value is measured. The laser focus is moved and it removes material along a track, until the resistance value is inside the desired tolerance. The resistance will always increase by the trimming; therefore the resistance after printing is made 20 - 30 % lower than the desired end value. Three normal trim geometries are shown in Figure 8.5. With an L- cut the coarse trimming is done with a track perpendicular to the resistor length, and the fine trimming to accurate value is done by the track along the direction of the current. Digital trimming gives the best stability and noise properties but occupies more substrate area.

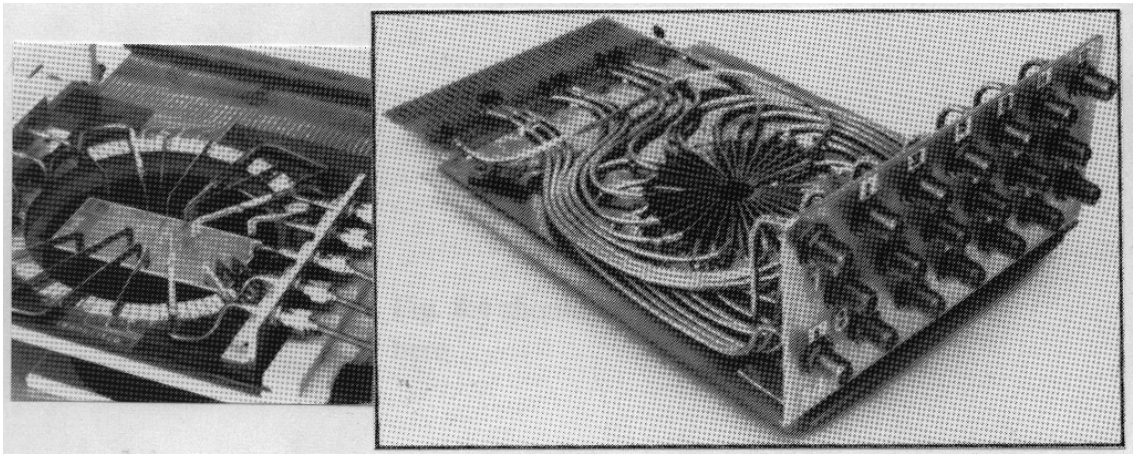


Fig. 8.4 Probe card for testing of thick- and thin film hybrid circuits. Coaxial probes are used for high frequency signals.

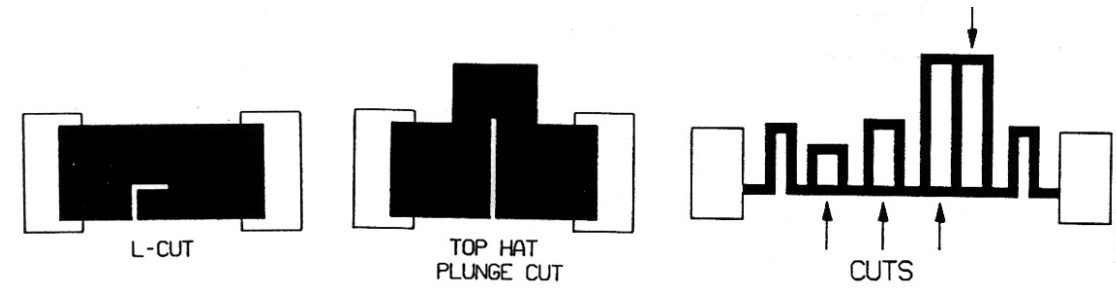


Fig. 8.5 Laser trim cut forms: a): L-cut, the most common, b): Top hat plunge cut, c): Digital trimming, which is most used for high precision thin film resistors

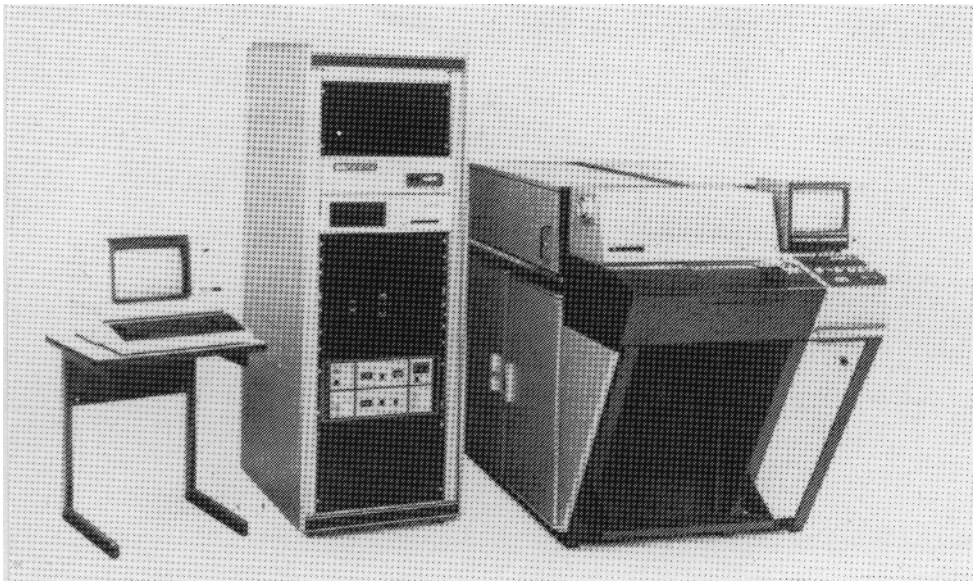


Fig. 8.6 Laser trimmer for thick film hybrid circuits, ESI Model 44

Alternatively active functional trimming may be performed. Then one measures a circuit function (the frequency of an oscillator, the amplification of an amplifier, etc.), and the value for the critical resistor is trimmed until the correct value of the measured parameter is achieved.

After completing the trimming of a resistor, the X - Y table on which the circuit is placed is automatically moved and the next resistor is trimmed. A laser trimmer is shown in Figure 8.6.

8.2.4 Component mounting, encapsulation

Soldered, encapsulated ICs, as well as wire bonded naked chips, are used on thick film hybrids. SMD passive components are soldered by using solder paste and reflow soldering, or they are glued with electrically conductive adhesive. Reflow soldering is done with a hot gas convection belt furnace, an IR. (infrared) furnace or vapour phase furnace. The process for "chip-and-wire" mounting and for soldered hybrid circuits is shown in Figure 8.7. Normally, soldered SMDs are not used on circuits together with wire bonded chip-on board, because of the danger of contamination from the solder process. This may make the surface unsuitable for wire bonding and/or give poor long term reliability. Conformal coating is an extra protection by an organic material over the components and substrate, for example Parylene. Conformal means a coating covering all surfaces. It gives mechanical and environmental protection and binds loose particles.

The hybrid circuits may be used unencapsulated or they may be mounted in metal- or ceramic flatpack packages. Circuits with naked ICs are encapsulated hermetically or the naked chips may be protected by drops of epoxy ("glob top" encapsulation).

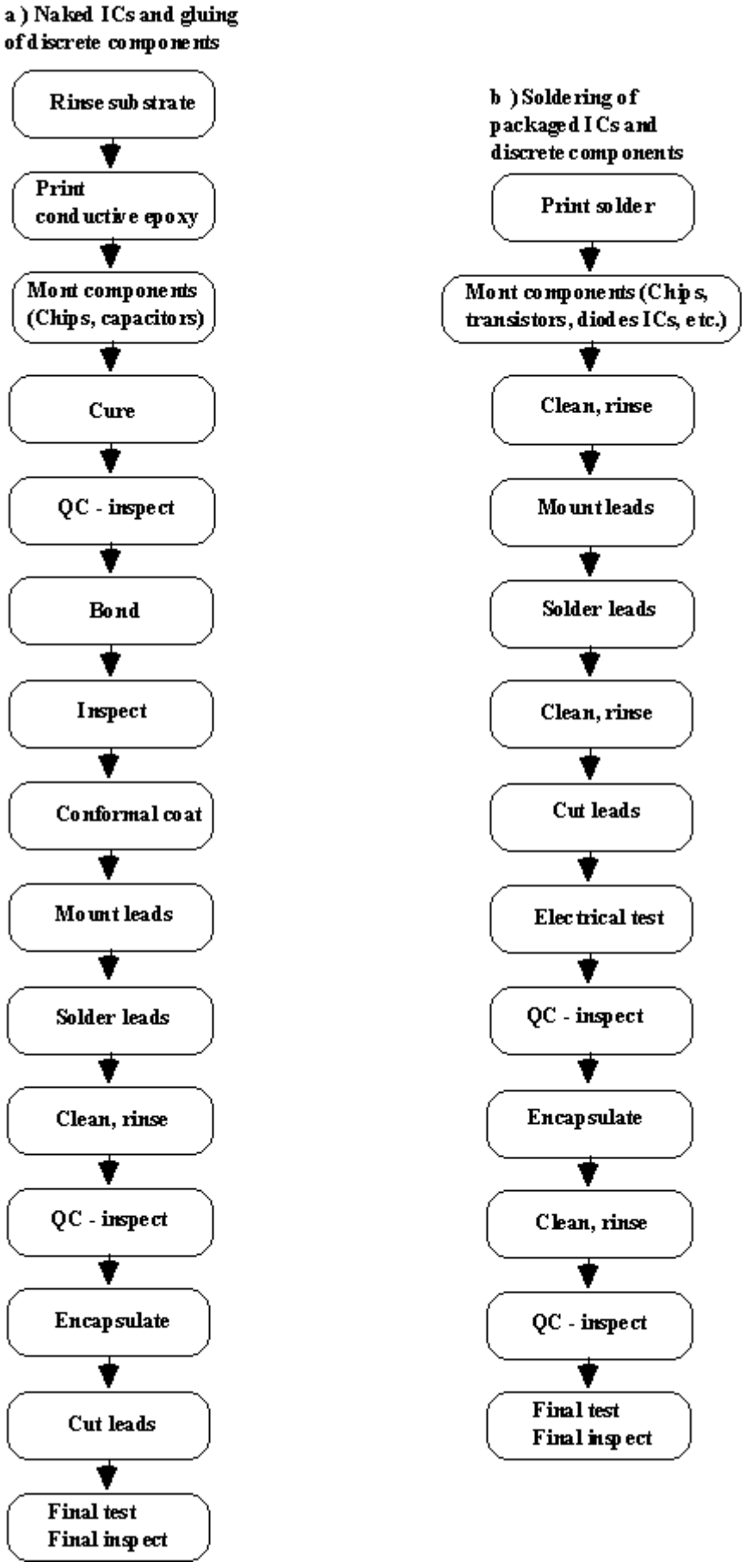


Fig. 8.7 Process flow for mounting of thick film hybrid circuits based on:
a): Naked ICs and gluing of discrete components.
b): Soldering of packaged ICs and discrete components [8.7]

8.2.5 Design rules

Some of the general design guidelines for PCBs, given in Chapter 6, also apply for hybrid circuits. The smallest conductor widths and distances are normally 0.2 mm. The resistances in conductors and in resistors are calculated like in Section 6.3.1. The demands for low voltage drop in high current circuits may cause the need for wider conductors.

The smallest length and width for resistors are 0.5 - 1 mm. The ratio between length and width should be between 0.1 and 10. For resistors that dissipates much power the resistor area should be increased such that the dissipation is maximum 100 mW/mm^2.

The same dimensions as given in Section 6.3.4 may normally be used for solder lands in reflow soldering.

An efficient ground plane is achieved by metallising the complete underside of the substrate.

Detailed design guidelines are given in [8.1 - 8.4].

8.3 POLYMER THICK FILM TECHNOLOGY AND MEMBRANE SWITCH PANELS [8.5]

8.3.1 General

In polymer thick film hybrid technology (PTF) conductors, resistors and insulating layers are made in several layers on ordinary printed wiring board laminates, flexible substrates and injection moulded plastic materials that can serve as combined printed circuits and chassis [8.5 a)].

The main purpose of PTF is to achieve lower cost than what is achievable with conventional PCB technology or with high temperature thick film hybrid technology. In certain cases, one can achieve technical properties that are difficult to obtain with conventional technology. PTF, on the other hand, has disadvantages that limit its use.

PTF is used ordinarily on substrates of paper/phenolic or glass/epoxy, when ordinary stiff printed circuits are to be made, or polyimide or polyester for flexible boards or membrane switch panels. The starting material for conductors, resistors and insulation is in paste form, and the transfer takes place by screen printing, like in high temperature thick film hybrid technology. The curing processes are also analogous to those of high temperature thick film, but they are performed at considerably lower temperatures. After the printing of a layer, it is dried to evaporate the solvents. Then it is cured by heat or irradiation.

The design of PTF-based printed circuits is similar to that of high temperature thick film design.

The most important advantages of PTF are the following:
- Low price.
- Simple processes.
- Quick production of prototypes and full production volumes.
- PTF is well suited for repair/modification of regular printed wiring boards.
- Printed resistors can be made.
- Additive technology, little waste and environmental problems.
- Substrates: Regular printed wiring board laminates.
- Specialities:
  * Membrane switch panels.
  * Low price contacts for keyboards and for contact points to elastomeric contacts for LCD displays.

Important limitations of PTF:
- PTF circuits satisfy only moderate environmental requirements.
- Only moderate complexity can be achieved.
- High sheet resistivity in the conductors (> 10 x that of Cu foil), except when plated conductors are used (please refer to Section 8.3.2, on platable Cu paste).
- Special design rules.
- Limited solderability.
- The materials have limited shelf life before they are used.
- Limited availability (i.e. few producers).

Varieties of PTF technology

The most used varieties of PTF technology on rigid substrates are the following:

1. Simple carbon technology for keyboards, contacts, sliding potentiometers, please refer to Figure 8.8.

2. Membrane switch panels, please refer to Figure 8.9.

3. PTF for a limited number of simple conductor crossings. Most of the conductors are in copper foil, but PTF makes an additional conductor layer, with insulation under each conductor, for crossing over copper foil conductors. This version of PTF is often used for repair/modifications.

4. One complete PTF conductor layer in addition to Cu foil. PTF insulation is printed all over the board, except on contact areas, Figure 8.10 a). This is an extension of type 3.

5. Multilayer boards, Figure 8.10 b) and c): Double sided PTF, normally also with Cu foil conductors on one or both sides. One can have electrical contact through holes by PTF through hole printing, to avoid copper through hole plating.

6. Printed PTF resistors, in combination with the types above, please refer to Figure 8.10 d).

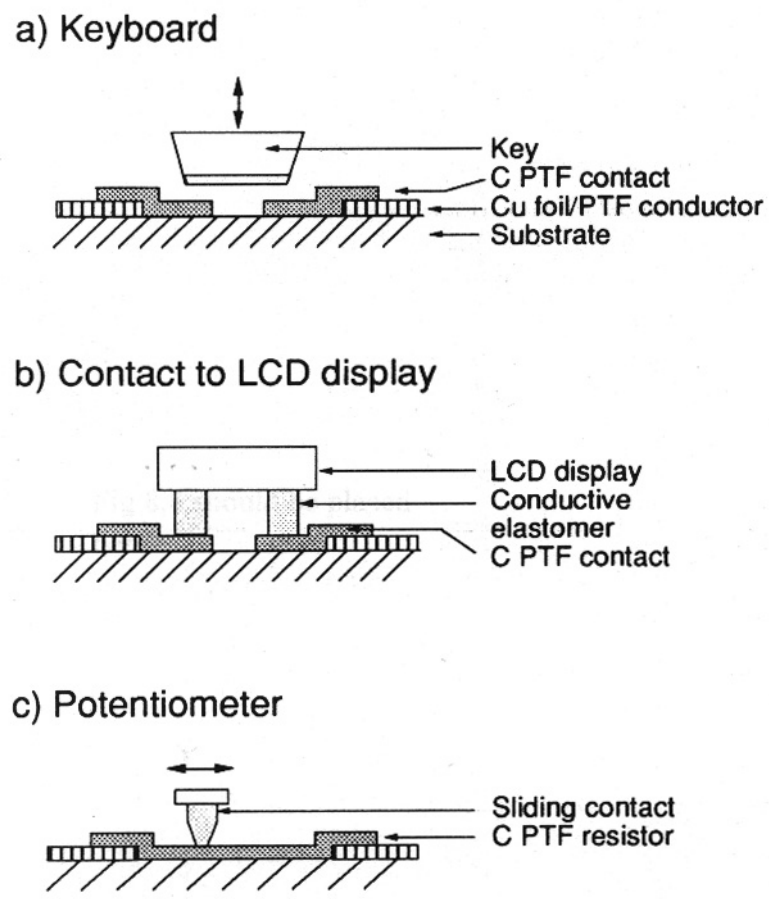


Fig. 8.8 Polymer Thick film (PTF) carbon technology, for:
a): Keyboard contacts.
b): Contacts of LCD-displays.
c): Sliding potentiometer [8.5].
CPTF means carbon type PTF

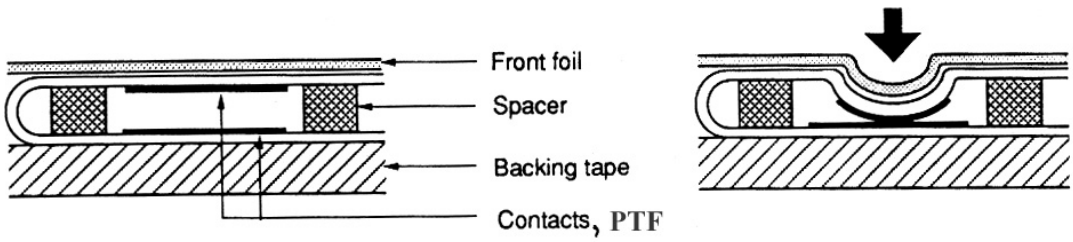


Fig. 8.9 Membrane switch panel, principle [8.5]

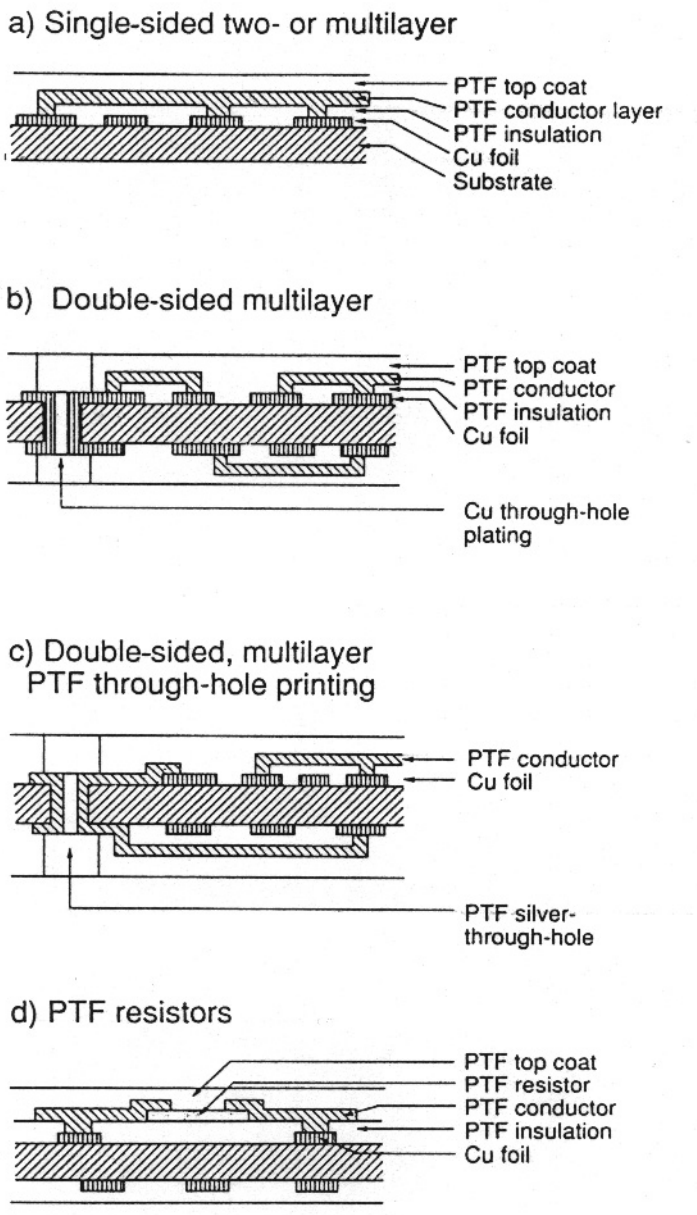


Fig. 8.10 PTF based printed wiring boards:
a): Single sided board with PTF for one complete conductor layer on top of one Cu foil conductor plate.
b): Double sided, through hole plated board with one extra PTF conductor layer on each side.
c): Double sided board through hole printed PTF conductor, instead of through hole plating d): PTF resistor [8.5].

PTF is much used for membrane switch panels, as mentioned above. To some extent ordinary, flexible boards of types 1 - 3 are also made.

The simpler varieties of PTF are used extensively in consumer electronics from the Far East. Its use in the USA and Europe is considerably less, but Finland has been a European pioneer country.

8.3.2 Materials

The conductor pastes and the resistor pastes consist of conducting particles in a matrix of polymers that serves as a binder and in addition to give adhesion to the substrate. Solvents are added to give the desirable printing properties. The insulating pastes have no conductive particles.

The polymer matrix

Thermoplastic as well as thermosetting polymers are used, please refer to Chapters 3 and 5. The first type is completely cured before use. The desired viscosity for printing is achieved by adding solvents, and the polymer solidifies by evaporation of the solvent.

The thermoplastic materials have lower strength as binders, and (often) poorer adhesion to the substrate. In addition, this type of polymers will have poor resistance to various solvents. On the other hand, they are very simple to use. Thermoplastic materials are used primarily for membrane switch panels.

Most PTF pastes for rigid boards are composed of thermosetting polymers. Cross linking takes place during the curing process, and the matrix becomes stronger. The most common types are phenol-, epoxy- and polyimide based. Various types of polymers may be in a mixture.

The curing is done in a regular convection furnace, by IR heating, microwave heating or vapour phase condensation heating, analogous to the vapour phase reflow soldering. The two first methods are the most common.

Many pastes have UV cured polymers. Such pastes are often solvent free. This gives certain advantages regarding dimensional stability from the printing to the completely cured product. Such pastes contain substances that catalyse the polymerisation process when the paste is irradiated with UV light. They are primarily used as dielectrics.

Active ingredients

Silver is used the most as conductive element, but also copper or carbon. The choice of the best suited active material depends on the requirements for the conductors. Silver has high electrical conductivity and gives no problems with regard to oxidation of the surface. However, silver based pastes give migration problems. Furthermore, they normally require plating of another metal on top to be solderable. Copper has approximately the same electrical conductivity as silver and gives considerably less migration problems. However, copper may give problems with oxidation of the surface, poor solderability and high contact resistance. There are also copper pastes that are directly solderable.

Asahi Chemical, in Japan, produces a copper paste that is close to insulating after being printed. Metallic copper is plated on top of the printed pattern by chemical plating (without external current, please refer to Chapter 3). Then the sheet resistance is the same as for Cu foil of the same thickness.

Carbon has considerably poorer conductivity than silver and copper and is suitable only for special conductors, such as keyboard contacts with low current. However, carbon gives neither migration nor oxidation problems, and it is so stable that it is normally unnecessary to cover it with an insulating top layer. Carbon is also used as the dominant active ingredient in resistor pastes.

In addition to the electrically conducting ingredients, we often have additives that contribute to give the right consistency and colour, particularly in the dielectrics. These may be of different types, for example ceramic particles.

The homogeneity of the paste mixture is of great importance for the result. A certain degree of sedimentation will always take place during storage, and good mixing is necessary before use. For resistor pastes this may reduce the predictability and repeatability of the resistor values at printing. Japanese producers often make their own resistor pastes immediately before use, in order to avoid this problem. However, normally the commercially available resistor pastes may be used with good results.

8.3.3 Typical process

Below we give a typical process for types 2 - 4 boards (Section 8.3.1). The starting material is a laminate with a single sided etched conductor pattern in Cu foil.

1. Cleaning of the board
2. Printing of PTF insulation layer, 2 prints, drying in between
3. Drying
4. UV curing
5. Printing of PTF conductor
6. Drying
7. Curing in IR in-line furnace
8. Chemical plating of metal (Optional)
9. Printing of top layer
10. Drying
11. Curing in IR furnace.

It is most common for PTF conductors to use Ag-based or Cu-based conductor material. Step 8, chemical plating, may be done on top of Ag in order to improve the solderability of the PTF conductor on the solder lands. It is also used on Cu platable conductor paste, as mentioned earlier. The process for the chemical Cu plating is similar to that which is used in production of through hole plated printed wiring boards. The details are given in Chapter 5 and [8.18].

Detailed design rules are given in [8.5 b)].

8.4 THIN FILM HYBRID TECHNOLOGY

8.4.1 Conventional thin film technology: Substrates and materials

Thin film circuits consist of conductor layers, resistor layers and dielectric layers, similarly to thick film circuits. However, the thin film thicknesses are normally 1 μm or less, an order of magnitude less than for thick film. Processes from silicon technology are used for deposition and definition of patterns. That gives higher circuit density than in thick film. The materials are also generally different. In this section, we shall concentrate on the form of thin film hybrid technology that has been in use since the 1960´s, with one layer of conductor, one layer of resistor and an inorganic dielectric.

The substrate materials that are used the most, are glass and 99.6 % alumina. The fine conductor dimensions in thin film require a smoother and more uniform surface underneath, so the substrates are polished. For high frequency use, low losses are important and the purer quality alumina, used in thin film circuits, has lower tan δ than the substrates used in thick film technology, Table 8.1.

The metals that are used the most for thin film conductors are gold and aluminium. Gold is chemically stable, it has high electrical conductivity and good bondability. However, as previously mentioned, gold diffuses very fast into many other conductor and insulating materials. Together with gold special elements are used as diffusion barriers, and in addition as adhesion layers, because gold has poor adhesion to many materials. Nickel is suitable for diffusion barrier, a nickel/chromium alloy improves the adhesion, and it is also suitable as resistor material, see below. The much used Au - NiCr system is deposited by vacuum evaporation or by sputtering, please refer to Chapter 3. Gold may also be electrolytically plated, particularly for microwave circuits, where a 5 - 10 μm thick layer gives low conductor resistance, which is important to achieve low high frequency loss. (Please refer to Section 6.7).

Aluminium is used much as electrode material for thin film capacitors. Various materials are used for dielectric depending on whether one wants to make capacitors, multilayer insulation or passivation. For passivation SiN_3 is well suited. SiO_2 is used much for insulation between conductor layers, because it has low dielectric constant ($\varepsilon_r = 4$), and high breakdown field strength (10^6 V/cm). Both are produced by chemical vapour phase deposition. For capacitor dielectric SiO is used, or SiO_2, Al_2O_3, Ta_2O_5. They are produced by vacuum evaporation, or chemical deposition, or anodic oxidation [8.2].

Resistors are made, as mentioned, from NiCr, as well as Ta_2N, by vacuum evaporation or by sputtering.

While we can achieve over 6 decades of variation in sheet resistivity in thick film hybrid technology, the range we achieve with practical thicknesses in thin film technology is only between approximately 10 and 1000 ohm/sq. Some properties are shown in Table 8.5, and more details about all thin film materials and deposition processes are given in [8.1 - 8.3].

Table 8.5 Properties of thin film resistors
(δ: skin depth. Evap: Vacuum evaporation. Sp: Sputtering) [8.3]

Material	*Specific Surface Resistance ($t << \delta$), $R_f = \rho / t$ (in ohm)*	*Temperature Coefficient of the resistance, $\Delta R/(R\ \Delta T)$ (in $10^{-6}/°K$)*	*Stability $\Delta R/(R\ \Delta T)$ (in %/1000h)*	*Production method*
NiCr (nickel-chrome)	40 - 250	-100 - +100	<0,2 good	Evap
Cr (chrome)	10 - 500	-300 - +300	medium	Evap
Ta (tantalum)	40 - 200	-200 - +200	<1 medium	Sp
Ta_2N (tantalum-nitride)	10 - 100	-60 - +30	<0,2 good	Reactive sp
Ti (Titanium)	5 - 2000	-500 - +500	medium	Evap
Cr-SiO Cement	500 - 2000	-250 - +250	<0,5 medium	Flash sp

8.4.2 Production process

Figure 8.11 shows the process steps for the most common form of thin film circuits, with one conductor layer and one resistor layer. In the first step, the resistor layer is deposited all over the substrate. If the circuits are small, many circuits are made on the same substrate, and they are separated at the end of the production process. A diffusion barrier is deposited and then the conductor metal. It is preferably done in the same vacuum chamber, in order to have a clean surface and good adhesion. These are standard processes that require special equipment and clean room facilities, normally smaller thin film circuit producer companies will buy the substrates processed to this stage.

Conductor and resistor geometries are defined by photolithography and etching. A few drops of photoresist are deposited and spread by the centrifugal force when the substrate is rotated on a spinning table. The conductor pattern for circuits is defined by exposing the resist through a photo mask, development and curing. Then the gold is removed by etching where it is not wanted. A solution of potassium iodide may be used, without dissolving the NiCr layer. If the need exists for conductor widths less than 2-3 μm, the etching is done by reactive ion etching, which etches fast vertically, but more slowly horizontally, and thus reducing the underetching.

A new step of photoprocessing is done to define the pattern of the resistors, and the diffusion barrier and the resistor films are etched where they are to be removed, for example with nitric acid. (Where the circuit has conductor pattern, there is still the resistor layer underneath the conductor material, see Figure 8.12.)

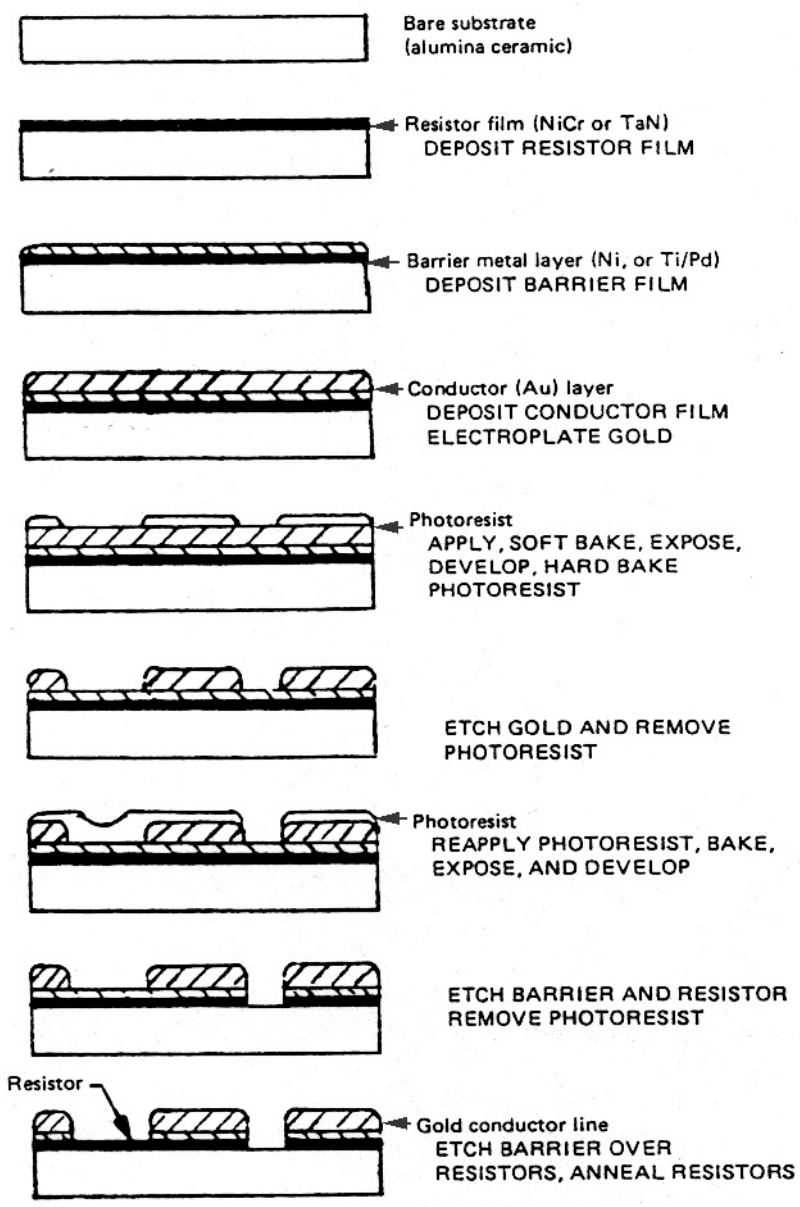


Fig. 8.11 Process flow for production of thin film hybrid circuits

Finally, the circuit is cured in air at 250 - 350 °C for some hours, to make a passivating layer of chromium-oxide to protect and stabilise the resistors.

An example of a microwave circuit that has plated gold conductors and capacitors is shown in Figure 8.13.

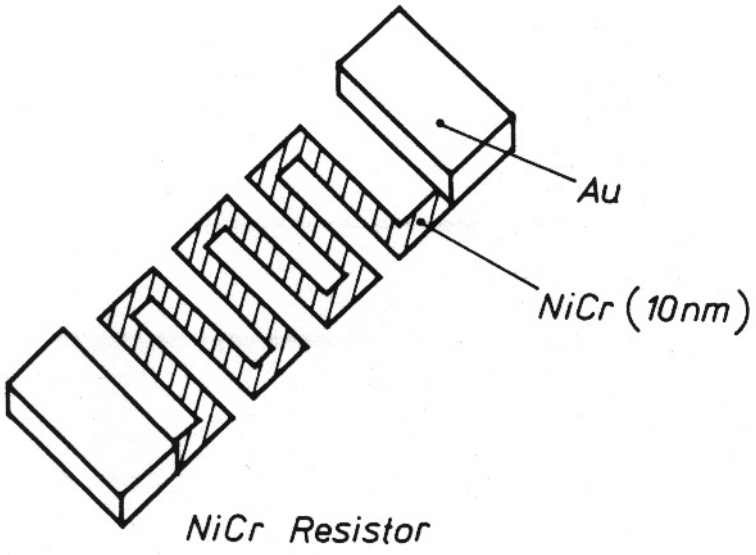


Fig. 8.12 Structure of thin film resistor with gold termination.

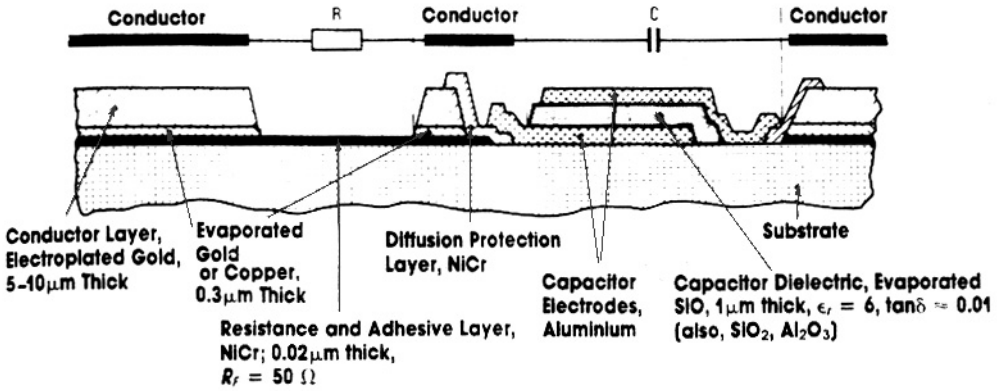


Fig. 8.13 Thin film microwave circuit, schematically [8.3].

Thin film components

A type of "components" that is very suitable for being made by thin film technology is precision R/C networks. They are also available as off-the-shelf components for mounting on other thin- or thick film substrates.

Diodes and transistors can also be fabricated. Large thin film diodes made from Cu_2S/CdS hetero-junctions give low price solar cells, and thin film transistors have been under development for 10 - 15 years. A matrix of thin film transistors is of great interest for the control of big LCD screens for flat televisions, etc. The structure is similar to Si -MOS transistors, see Figure 8.14, and CdSe as well as Si/H are used as the semiconducting material.

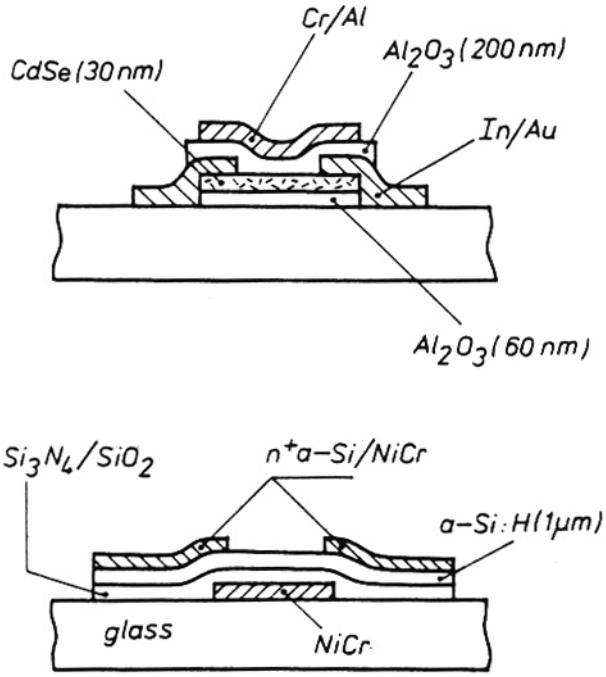


Fig. 8.14 Thin film transistors, structure [8.2]

The complete thin film circuit

When the thin film substrate has been completely processed, resistors may be laser trimmed like in the case of thick film circuits. After this, components will be mounted on the substrate. Integrated circuits are normally mounted in the form of naked chips that are glued on to the substrate and wire bonded. Discrete resistors and capacitors are normally mounted with conductive adhesives for electrical and mechanical contact and not soldered. In most cases, the complete circuit will be mounted in a hermetic package that is made of ceramic, or in most cases of metal. Terminal points on the substrate will be connected to the leads of the package by wire bonding. A welded or soldered metal lid on the package ensures hermeticity and good reliability.

8.4.3 Multilayer thin film, multichip modules

This is an extension of conventional thin film technology, but with many conductor layers, that makes it possible to achieve a very high circuit density. We may also achieve a controlled characteristic impedance and good high frequency properties. Multilayer thin film is one of the technologies for multichip modules, MCM-D, as mentioned in Section 2.7.

The normal substrates are either 99.6 % alumina or silicon wafers. Figure 8.15 shows a cross section. The dielectric most often used is polyimide, approximately 10 µm thick. Al, Cu, and Au are used as conductor metals. IC process technology makes it possible to achieve a minimum conductor width/distance of 25 µm or less, i.e. a higher conductor density than any other

substrate technology (except full wafer scale integration). AT&T has been a pioneer in this technology. Over 100 companies and research labs had this technology under development/production in 1992 and it will be a mainstream technology for high performance systems during the coming years. One high performance product employing the technology is the mainframe computer VAX 9000, of Digital Equipment Corporation. Si substrates are used and TAB-mounted Si chips [8.16].

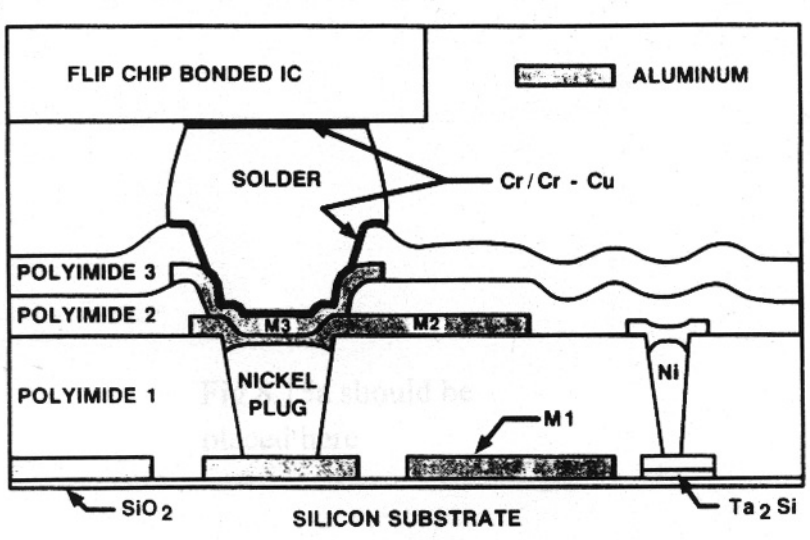


Fig. 8.15 a): AT&T´s structure for multilayer thin film [8.25]. See also Figure 2.13 [8.7]

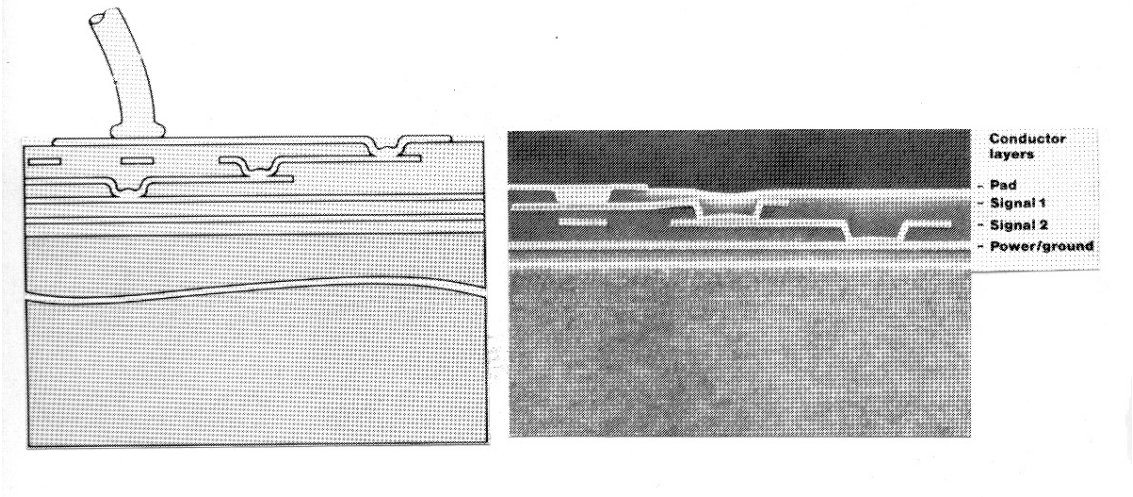


Fig. 8.15 b): Cross section of Raychem´s High Density Interconnect (HDI) schematically and observed through microscope

A typical process is as follows:

1. Spinning of polyimide insulation
2. Deposition of Al metallisation (sputtering, 5 µm, R=6 mohm/sq)
3. Photolithography and wet etch of conductor pattern
4. Spinning of polyimide
5. Etching of via holes. Several methods are used, this is a critical point.
6. Repetition of steps 1 - 5 for multilayer
7. Metallisation and etching of the surface metal (5 µm Al or 2 µm Au).

Some design rules for Raychem´s "High density interconnect" (HDI) technology are shown in Figure 8.16 [8.8]. The characteristic impedance as a function of the ratio conductor width/dielectric thickness is shown in Figure 8.17. Tan ∂ of the dielectric and typical attenuation as function of the frequency are shown in Figure 8.18. We see that all the way up to 10 GHz the losses in the conductor dominate, the dielectric loss is negligible. The dielectric constant depends on the moisture absorption in the polyimide: ε_r = 3.4 (dry) and 4.5 (maximum moisture content, 3.5 %). Much work is in progress to develop new types of polyimide and alternative materials that are less hygroscopic.

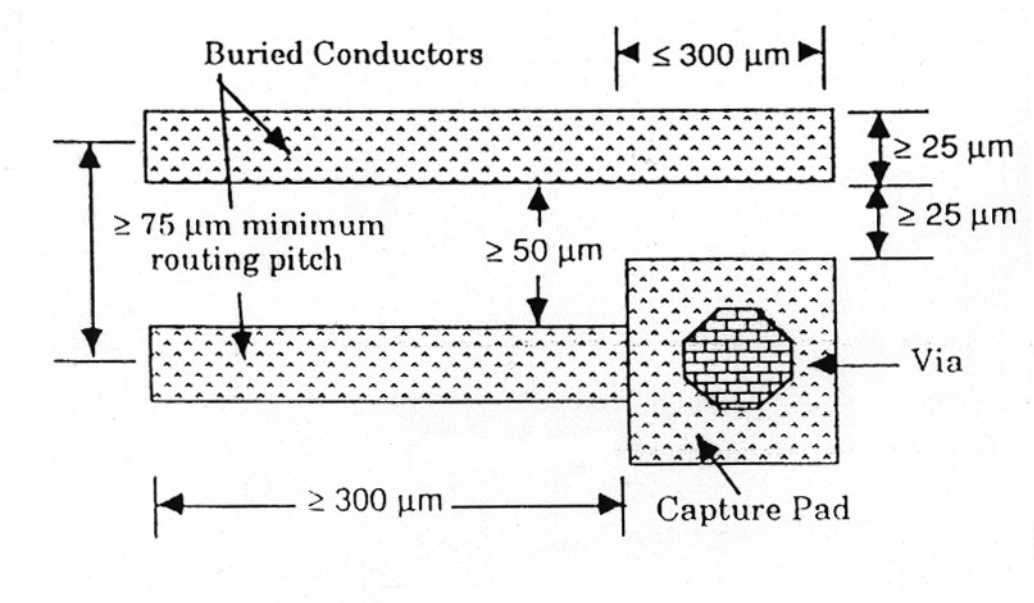


Fig. 8.16 Elements of the design rules for Raychem´s HDI technology [8.8]

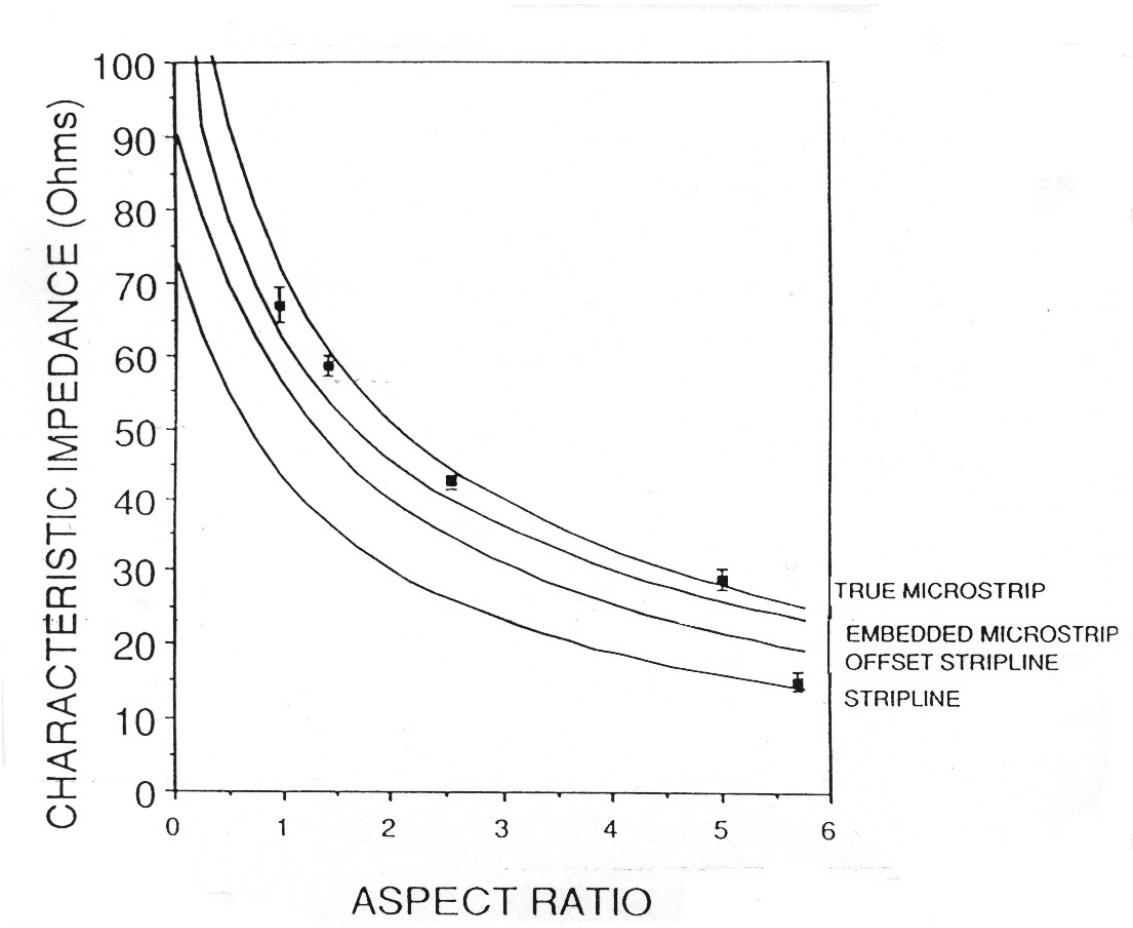


Fig. 8.17 Characteristic impedance for Raychem´s HDI as function of the ratio between conductors width and dielectric thickness.[8.8]

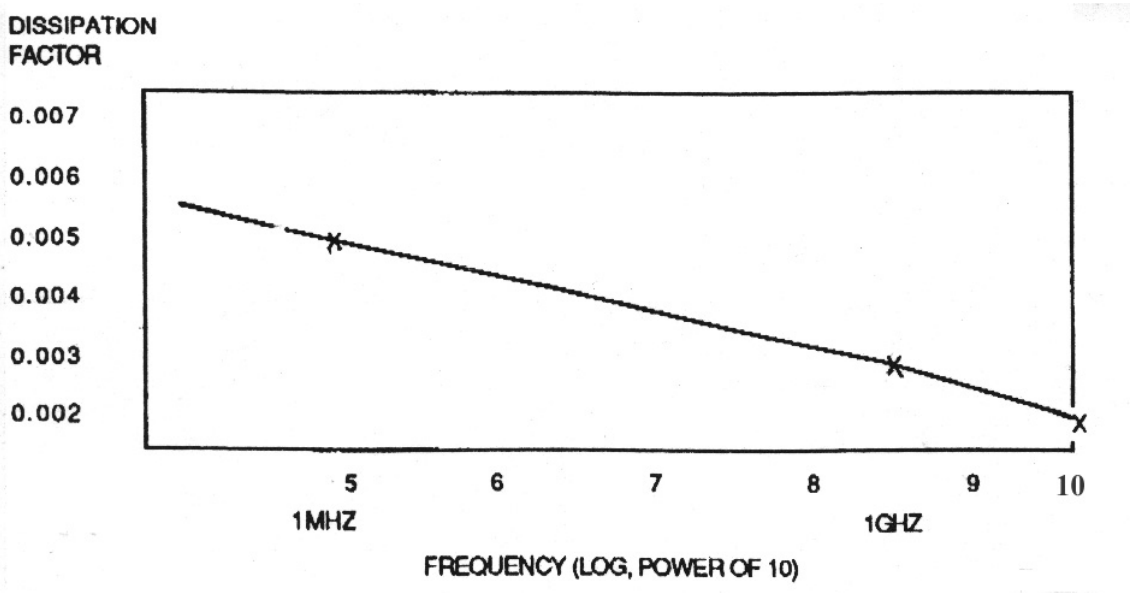


Fig. 8.18a): Dissipation factor for Raychem´s HDI [8.8]

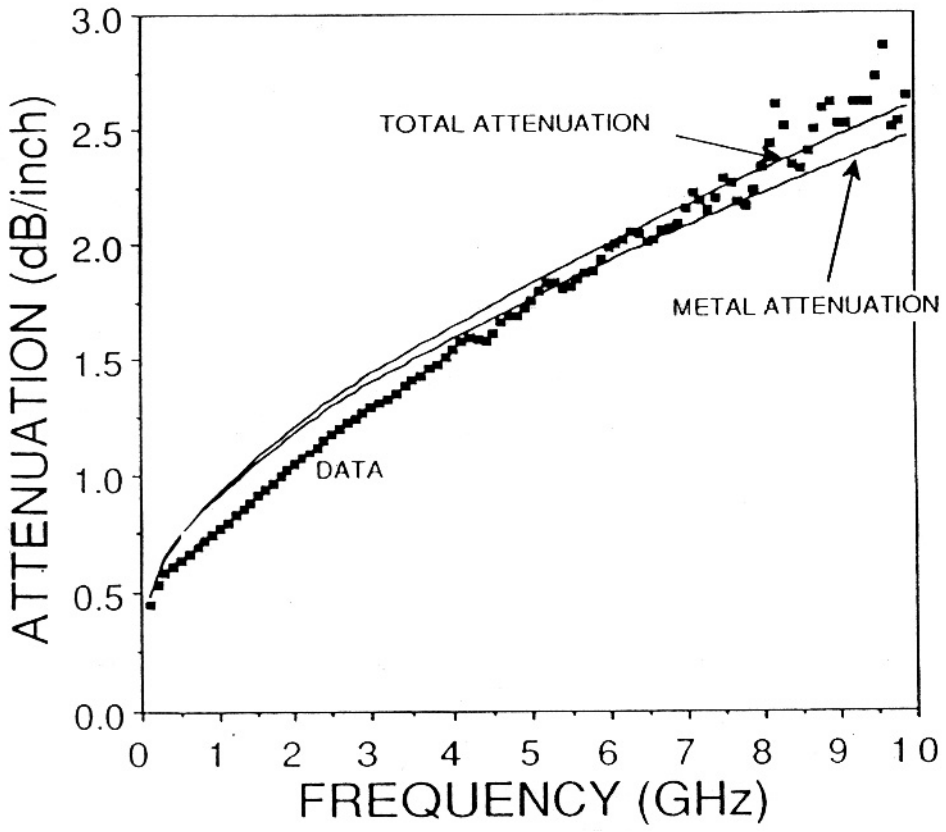


Fig. 8.18. b): Typical attenuation, as function of frequency, for Raychem´s HDI [8.8] Even at 10 GHz attenuation in the conductor metal dominates

For ICs with high dissipation it is possible to make a "thermal well", by mounting the chip directly on the substrate, without the polyimide. This is used in the VAX 9000 computer, where ECL technology gives high power dissipation.

Some advantages of multilayer thin film with Si substrates:
- Optimal thermal match between Si substrate and Si chip components
- Very good thermal conductivity in Si substrate: 150 W/°C m
- Termination resistors and decoupling capacitors may be integrated in the substrate
- Compatibility with wire bonding, TAB and flip chip. Also with gluing of discrete components
- Very high conductor density and package density
- Very good high frequency properties due to short wire lengths, low ε_r and low losses in the dielectric
- Very good mechanical properties in the Si substrate materials
- High reliability when it is hermetically encapsulated.

Some disadvantages:
- Thus far; low availability and high cost
- Polyimide is hygroscopic, and the moisture uptake may give swelling and corrosion over long time. Hermetic encapsulation is necessary.
- Immature technology.

8.5 MULTILAYER CERAMIC MODULES

8.5.1 High temperature ceramics

High temperature multilayer ceramic technology has been used for many years for ceramic capacitors and for IC packages. For packages and multichip modules, Al_2O_3 and AlN (BeO and SiC to a smaller extent) are used. For multichip modules, alumina is the most used material, with 92 - 96 % Al_2O_3 content. The structure consists of many layers of ceramic, with metallisation between the layers, and via holes through the layers for electrical contact. The best known application of large modules with many layers of ceramic is IBM´s pioneering product "thermal module" [8.6] for mainframe computers, already in 1983. The module had over 30 layers, and about 100 ECL silicon chips were mounted by flip chip soldering. Later various mainframe computer makers have used analogous technology, based on materials with even better thermal conductivity.

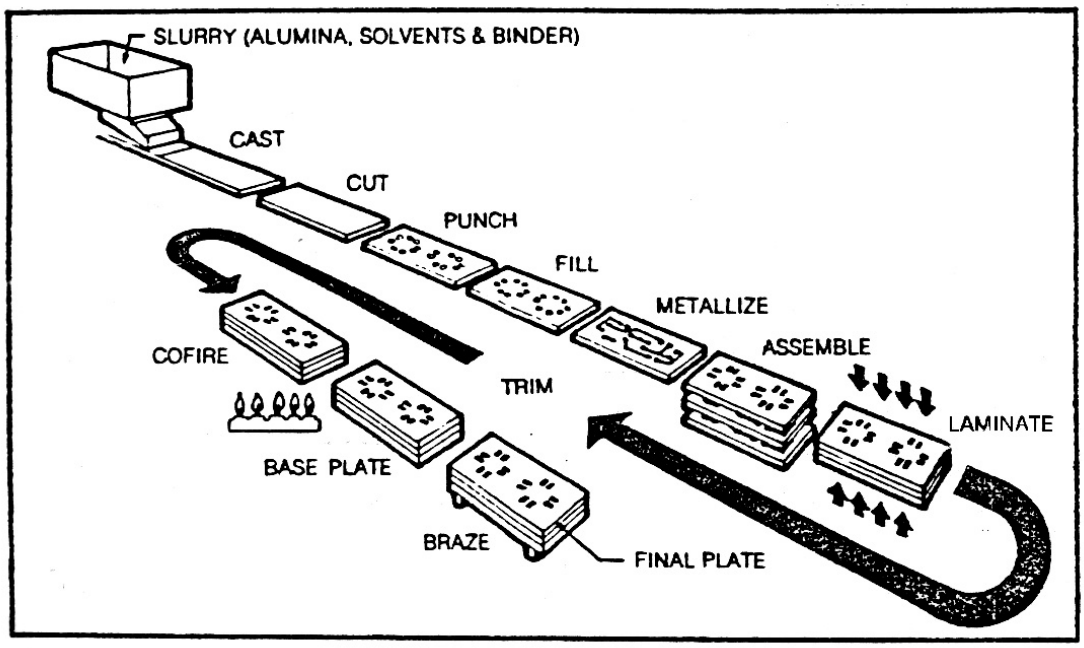


Fig. 8.19 Production process for multilayer ceramic, schematically

Fabrication

The fabrication of multilayer ceramic modules by "tape casting" is shown schematically in Figure 8.19. The non-sintered, pliable ceramic consists of alumina powder, organic binders and solvents. The material is spread from a container down on a transport carrier underneath. The ceramic "tape" ("green sheet"), is given the appropriate thickness on the transport carrier by passing underneath a "doctor blade" in a precisely controlled distance. The tape is cut to correct size, and holes and component cavities are punched out with a numerically controlled punching tool or with a permanent, product specific punching tool for high production volume of a given product. Metallisation of the via holes and fabrication of conductors is done by screen printing of tungsten (or molybdenum). These are the only metals that can withstand the high process temperature later. All layers are laminated together under hydrostatic (or uniaxial) pressure at elevated temperature, to evaporate the binder and solvent. Then the whole structure is sintered at 1500 - 1700 °C, 30 - 50 hours, in hydrogen atmosphere. For small circuits, many circuits are made on one laminate, and the individual circuits can be parted by breaking the substrate at the end of the process. Then the external contacts are brazed to the substrate and finally gold may be plated on the surface with nickel as diffusion barrier on top of the tungsten. The plating is preferably done electrolytically to achieve sufficient thickness and good conductivity, if one can make electrical contact to all parts of the conductor pattern. Otherwise, chemical plating is used.

During the process, the ceramic shrinks approximately 18 % linearly. This has to be taken into consideration during the design of the circuit, both sideways and in thickness (which affects the characteristic impedance). Normally the designer will operate in correct dimensions and the producer will scale the CAD information up by the necessary amount for production of printing screens and punching tools. The shrinkage is material- and process dependent, so the finished circuits typically have linear dimensional tolerances 0.5 - 1 %.

Properties

Some electrical, physical and mechanical properties are shown in Figure 8.20. Black ceramic is used the most, the white material has somewhat higher purity and better properties at high frequencies, but it is transparent in a range of light wavelengths and is more expensive.

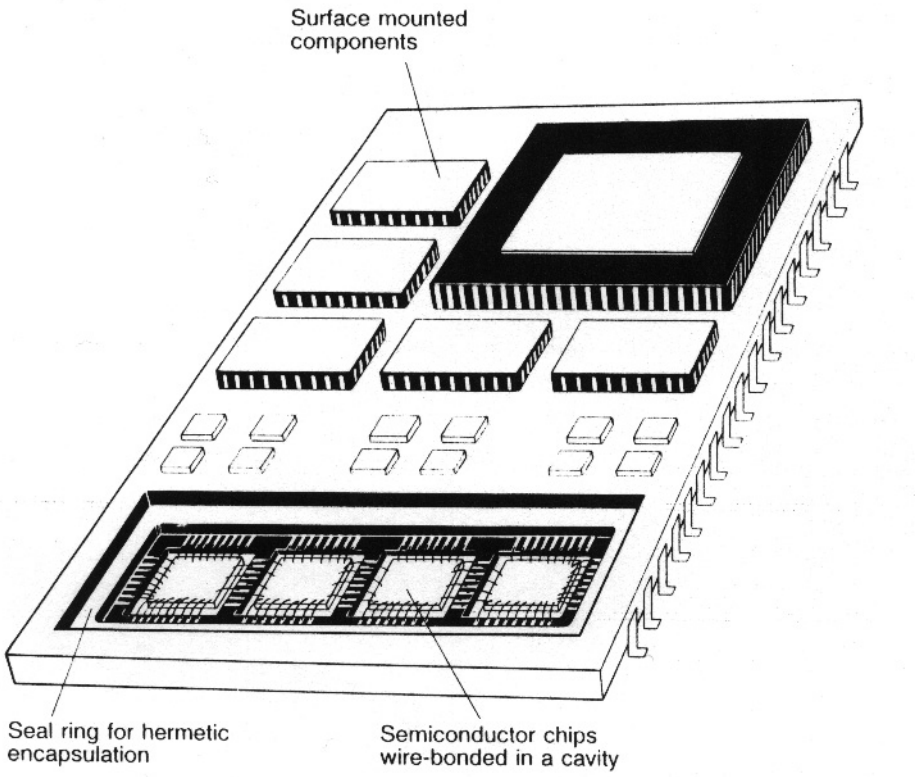


Fig. 8.20 Combination of naked chips in cavities and soldered, packaged SMD components on multilayer ceramic module [8.11].

The minimum conductor widths and conductor distances are typically 0.15 - 0.2 mm, diameter of via holes 0.1 - 0.2 mm. Extended ground planes are made as grids of printed lines rather than continuous, due to the dissimilar thermal properties of metal and ceramic during sintering. The typical thickness of the printed W conductor layer is 15 µm, for electrolytically plated Au on the surface it is 2 µm or more, with a 2 µm Ni barrier/adhesion layer between the Au and W.

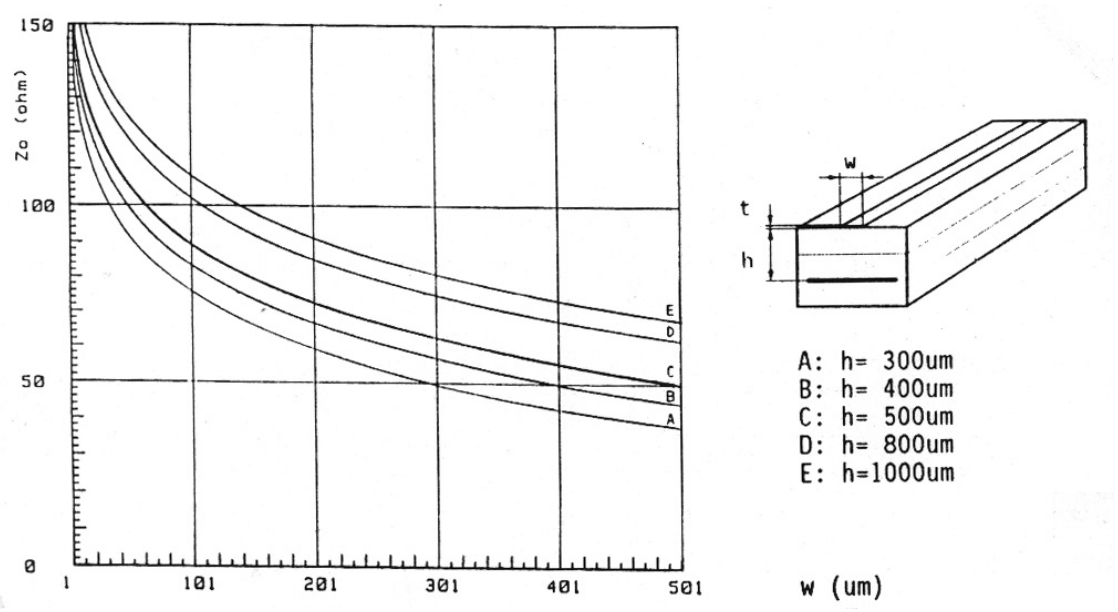


Fig. 8.21.a Characteristic impedance for typical geometries and dimensions, Al_2O_3-based multilayer ceramic: a): Open microstrip.[8.11]

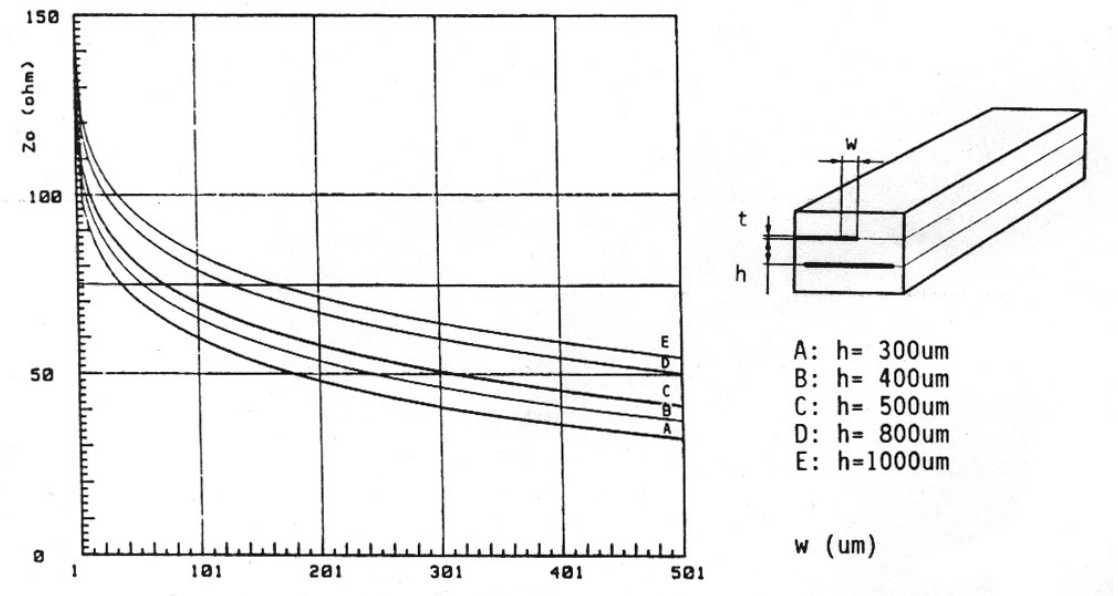


Fig. 8.21,b Characteristic impedance for typical geometries and dimensions, Al_2O_3-based multilayer ceramic: b): Buried microstrip.[8.11]

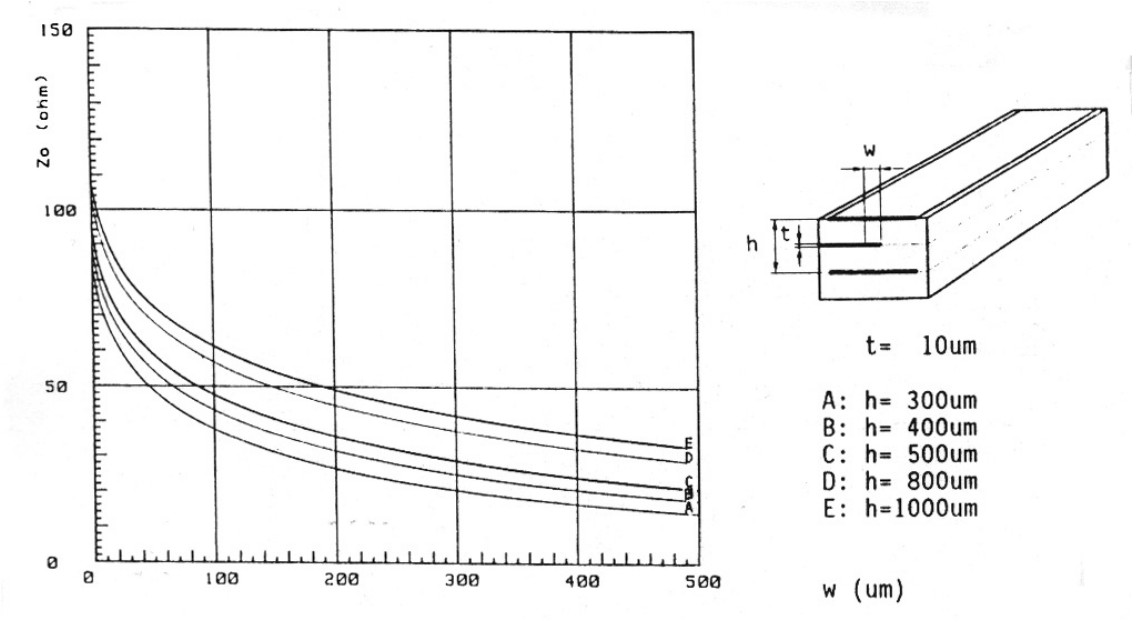


Fig. 8.21.c Characteristic impedance for typical geometries and dimensions, Al_2O_3-based multilayer ceramic: c): Stripline.[8.11]

The characteristic impedances for the common conductor geometries of multilayer ceramics are shown in Figure 8.21.

Among the advantages of high temperature multilayer ceramic are the following:

- High thermal conductivity
- Low TCE, good thermal match to Si and GaAs as well as to leadless SMD components
- Good control over characteristic impedance, good high frequency properties
- Both soldering of encapsulated components, TAB bonding of naked chips and flip chip mounting of smaller Si chips can be used (although there is not a perfect thermal match to flip chip soldered Si chips)
- Complete hermetic encapsulation is possible, or hermetic encapsulation of local areas, by using a lid over individual ICs in cavities, see Figure 8.21. High reliability.
- Many conductor layers are possible, with high production yield. This is because each layer can be inspected before the lamination, and faulty layers be discarded (contrary to thick film where one fault in one layer will ruin the whole circuit)
- Easy to mount edge contacts, coaxial contacts, etc.

Among the disadvantages are the following:

- Low electrical conductivity in the inner layers (sheet resistivity 15 mohm/sq)
- High dielectric constant gives delay, inferior pulse rise time and increased power loss and cross talk at very high frequencies
- The producers generally make standard packages in large volumes, and have high start-up cost for custom circuits.

Table 8.6: Properties of alumina-based high temperature multilayer ceramic [8.11].

Ceramic		Colour	
Property	Unit	Black	White
Al_2O_3 content	%	90	92
Density	g/cm^3	3,60	3,60
Rel. dielectric const. (1 MHz)		9,5	9,0
Loss tangent (1 MHz)	%	1,3	0,3
Breakdown field	kV/mm	10	10
Resistivity	ohm cm	10^{14}	10^{14}
Thermal coeff. of expansion (0-100°C)	ppm/°C	5,0	5,0
Thermal coeff. of expansion (0-300°C)	ppm/°C	6,5	6,5
Thermal conductivity	W/m x °C	15	17
Specific heat	W s/g x °C	80	84
Module of elasticity	N/mm^2	$3x10^5$	$3x10^5$
Conductors Property	Unit	Value	
Tungsten Sheet resistivity (0.1 mm con. width) (0.2 mm - " -) (0.3 mm - " -)	 mohm/□ 	 20 14 12	
Thermal coefficient of resistance	ppm/°C	4300	
Plated (W + Ni + Au) Sheet resistivity	 mohm/□	 3-4	

8.5.2 Low temperature multilayer ceramic

DuPont, IBM and others have introduced multilayer ceramic based on glass compositions similar to those used in thick film dielectrics, instead of alumina [8.12, 8.6, 8.21]. The fabrication is made in a process similar to that used for high temperature ceramic. The advantage of the low temperature technology is primarily that the sintering takes place at around 850 °C, 15 min., normally in air atmosphere (after a burnout at 350 °C to remove the organic binders and solvents). The effect of this is that the metal systems used in ordinary thick film technology are suitable for inner layers, with much better electrical conductivity than tungsten. Thick film firing furnaces may be used for the process. Resistors may also be printed in the inner layers. Materials in the substrate are mullite, corderite, lead borosilicate glass and others [8.21].

DuPont, one of those making the base materials, is promoting the technology among the thick film producers. The tape casting of the tape materials is done by DuPont and the user buys the tape mounted on a Mylar foil that is removed before the punching and printing. In Europe some three producers make custom designed low temperature ceramic circuits (1992), and many companies are testing out the technology. Several producers in the USA and Japan are making low temperature multilayer ceramic circuits, primarily for internal use.

Table 8.7 Electrical and physical properties of low temperature multilayer ceramic [8.12 a]

a): Electrical properties.

	Resistance [mohm/sq]	Fired Thickness [μm]
Inner Layer (Co-fired)		
Gold	5	7
Silver	5	8
Silver/Platinum	20	8
Top Layer (Post fired)		
Gold	4	8
Platinum/Gold	80	15
Silver/Palladium	20	15
Silver	4	15

b): Resistor Performance - Resistance and TCR

	Over Tape		Over Thick Film Dielectric	
	R [ohm/sq]	HCTR [ppm/°C]	R [ohm/sq]	HCTR [ppm/°C]
100 ohm/sq	122	+20	102	+65
10 Kohm/sq	10,0 k	+71	12,5 k	+41
100 Kohm/sq	92,4 k	+75	95,7 k	+73

c) Physical Properties

Thermal expansion	
Fired dielectrics	7,9 ppm/°C
96% alumina	7,0 ppm/°C
Fired density	
Theoretical	3,02 g/cm^3
Actual	>2.89 g/cm^3 (>96%)
Camber	
Fired	±75 μm (±3 mil.)
68 x 68 mm^2 (2.7 x 2.7 in^2)	
Surface smoothness	
Fired dielectric	0,8 μm/50mm
50 x 50 mm^2 (2 x 2 in^2)	(Peak to peak)
Thermal conductivity	
Fired dielectric	15 - 25% of alumina
Flexure strength	
Fired dielectric	2,1x10^3 kg/cm^2 (3,0x10^4 psi)
96% Alumina	3,8x10^3 kg/cm^2 (5,6x10^4 psi)
Flexure modulus	
Fired dielectric	1,8x10^6 kg/cm^2 (2,5x10^7 psi)
96% Alumina	0,9x10^6 kg/cm^2 (1,3x10^7 psi)

Many properties are similar to those of the high temperature system, but the thermal conductivity is about 5 times lower for the low temperature materials. The shrinkage is only approximately 12 %. The materials are more brittle than alumina, and they must be handled with caution. Some parameters are given in Table 8.7

Typical conductors minimum width and separation are 0.15 - 0.2 mm, diameter of the via hole 0.15 - 0.2 mm, and distance between via holes 0.25 - 0.4 mm. The DuPont tape is made in two standard thicknesses: 90 and 250 μm (after sintering). The surface roughness is approximately 1 μm, lot-to-lot variation of the shrinkage: 0.2 %. The relative dielectric constant ε_r = 7.5 - 8.0 (but materials with lower ε_r are available), tan δ = 0.2 - 1 %. Thermal conductivity K = 2 W/m °C. Buried, silver based conductors have quite good migration properties, and the resistors have properties similar to those of thick film resistors. Circuits with 20 layers of ceramic have been demonstrated, the potential is said to be over 40 [8.12].

Some advantages compared to high temperature multilayer ceramic technology are:

- Low process temperature, normal process atmosphere, requires low investments for thick film producers to start their own production ($ 100k - 200 k).
- Flexibility in choice of conductor materials, low sheet resistivity
- Plating is not necessary, bondable gold can be screen printed
- Resistors may be screen printed internally and on the surface
- Dielectric materials with relative dielectric constant down to 4 - 5 are used.

Disadvantages:

- New, immature technology
- Low thermal conductivity
- Brittle material, mechanically less robust
- So far, low availability.

A "transfer tape" version is also available, which is fired for each layer [8.14].

Various MCM technologies are compared in [8.22], and extensive treatment is given in the selected key reprints in [8.21].

8.6 TECHNOLOGY FOR POWER ELECTRONIC MODULES

8.6.1 General

In power electronic circuits and modules each transistor may over short periods of time conduct up to 100 A and more and occupy several square cm of silicon. Some of the major challenges are:

- Spread the heat from the silicon chip through a good thermal conductor underneath and reduce the total thermal resistance between chip and a good heat sink
- Reduce thermal stress due to material thermal mismatch
- Provide electrical insulation for voltages up to 2.5 kV and more
- Design for electromagnetic compatibility, particularly reduce the inductance to avoid large voltage spikes when large currents are switched on and off.

- Higher integration: Combining power and control on the same Si chip or on the same substrate, "smart power".

Technologies used for power circuits and modules include the following:
- Polymer on metal substrate technology
- Thick film technology
- Plated ceramic substrate technology
- Direct copper bonding (DCB) technology.
- Plasma sprayed dielectric on metal base.

8.6.2 Modest power levels

The polymer on metal technology is used for relatively low power and low voltage circuits. An Al or Cu plate is used for heat sink. It is oxidised to improve adhesion to the insulation that is organic, with additives to improve the thermal conductivity. A 35 or 70 μm Cu foil is laminated on top to provide wiring. Packaged chips are soldered on, or alternatively naked chips may be mounted with silver loaded adhesive or soldered, and wire bonded.

The thick film hybrid technology is similar to the technology described in Section 8.3, with especially wide and thick printed conductors and Al_2O_3 or AlN substrates.

In plated ceramic technology the substrate is first chemically etched in order to roughen the surface. Then a thick Cu conductor layer is plated by chemical and then electrolytic processes, and the conductor pattern is etched [8.27].

8.6.3 High power modules

Direct copper bonding (DCB) substrates have alumina or AlN ceramic insulator, typically 0.6 mm thick, and a 0.3 mm thick Cu foil on both sides [8.19]. The oxidised Cu is bonded to the ceramic by heating to a temperature slightly above 1065 ^{o}C, 20 °C below the melting point of copper. At 1065 ^{o}C a eutectic composition of Cu and 1.6 % CuO has its melting point. The molten phase wets alumina and creates a strong bond to the ceramic upon solidifying, by penetrating into the molecular structure of the ceramic. Since the copper itself does not melt, a pre-structured pattern of the foil will be maintained after the bonding process. Alternatively a uniform Cu foil may be bonded and patterned by etching. In case of AlN, a pre-oxidation step transforms the AlN surface layer into Al_2O_3 and the interface layer will be the same as for alumina ceramic [8.20]. It is important to have Cu on both sides of the ceramic, to equalise the thermal stress and reduce bowing of the substrate.

The thermal resistance is reduced by using thick Cu layers. This, however, will increase the thermal coefficient of expansion for the composition, see Figure 8.22 a), and increase the thermal mismatch to Si chips. The reliability of the DCB structure under temperature cycling will also be reduced, see Figure 8.22 b).

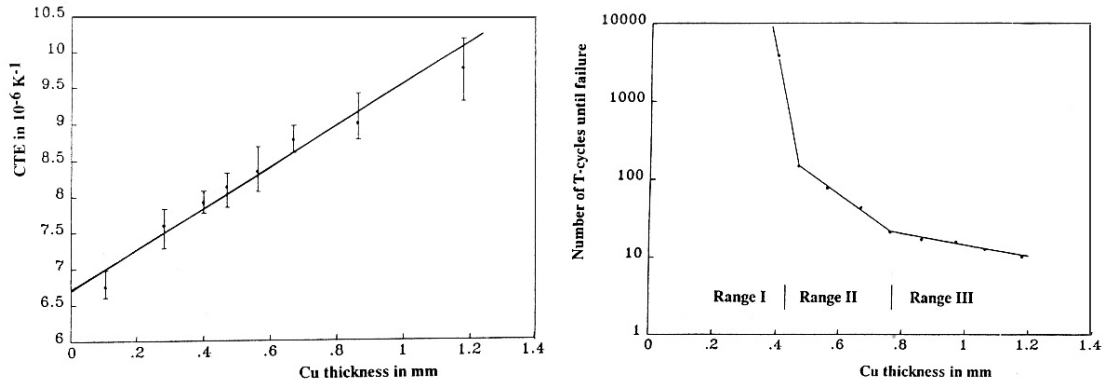


Fig. 8.22 a): The coefficient of thermal expansion for direct copper bonding (DCB) substrates with a layer of 0,6 mm alumina sandwiched between Cu layers of various thicknesses as given in the figure.
b): The number of thermal cycles to fracture for DCB substrates with varies Cu thickness. The cycles were in the temperature interval -40 - + 110°C [8.19]

The silicon chips are soldered to the substrates by high melting point solder in an inert or reducing atmosphere, and electrical connections are made by heavy Al wires. Many wires are used for each contact to reduce resistance and inductance.

In some modules the substrate is soldered to a heavy Cu plate, see Figure 8.23, for further heat spreading.

The complete modules are mounted to the heat sink below by screws. A thin layer of thermally conducting grease between module and heat sink will add significantly to the thermal resistance.

To improve the heat spreading in the substrate AlN with thermal conductivity up to 270 W/^{o}C m has been developed [8.28]. Even better thermal conductors than alumina and AlN are desirable for the dielectric in power modules. A big research effort has been started for deposition of diamond layers, with thermal conductivity of 1 000 - 2 000 W/^{o}C x m [8.29].

To reduce the cost and to facilitate production of high power modules with larger area than the DCB modules, a technology based on plasma spraying of alumina ceramic on aluminium base plates or heat sinks has been developed [8.30]. On top of the ceramic, it is then possible to spray Cu metallisation through a metal mask, providing the conductor pattern. The thermal properties are not so good as those of DCB, due to porosity of the ceramic. Furthermore, the Si chips are mounted with adhesive, giving additional thermal resistance [8.31].

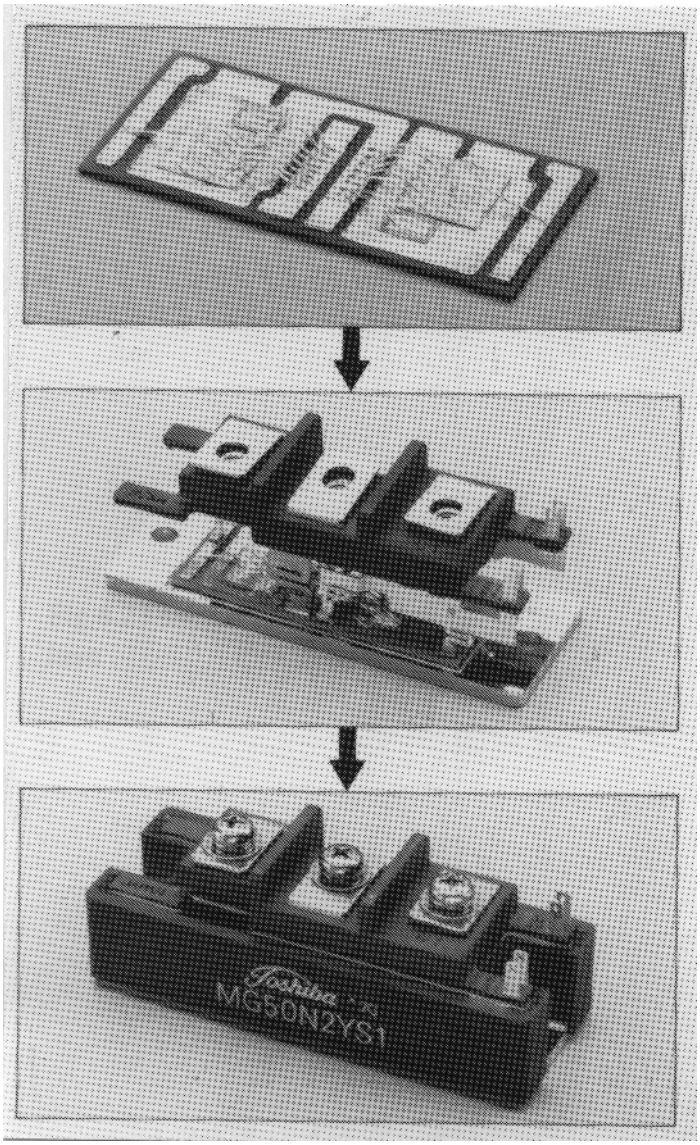


Fig. 8.23 Power electronic module [Toshiba data sheet]. The substrate (top) is DCB with AlN insulation. It is soldered to a heavy Cu plate, environmentally protected with silicone gel and mounted in a plastic package with heavy screw terminals. Each of the transistor chips and diode chips conducts up to 50 A current.

8.7 COMBINATION TECHNOLOGIES

8.7.1 Multilayer thin film on multilayer ceramic

The combination of multilayer thin film on top of multilayer ceramic is used for certain super computers, see Figure 8.24. It combines many of the advantages of both technologies. IBM has recently made a "thermal module" based on 63 layers low temperature ceramic and multilayer thin film on top [8.23].

These types of technologies are not available on the open market.

8.7.2 Thin film on thick film

AME in Horten, Norway, has developed a combination of regular thick film and regular thin film technology, see Figure 8.25. All slow and non-critical signals, in addition to ground and power planes, are made in thick film. On top are a ground plane, printed dielectric and one layer of thin film conductors for high speed signals with transmission line dimensions.

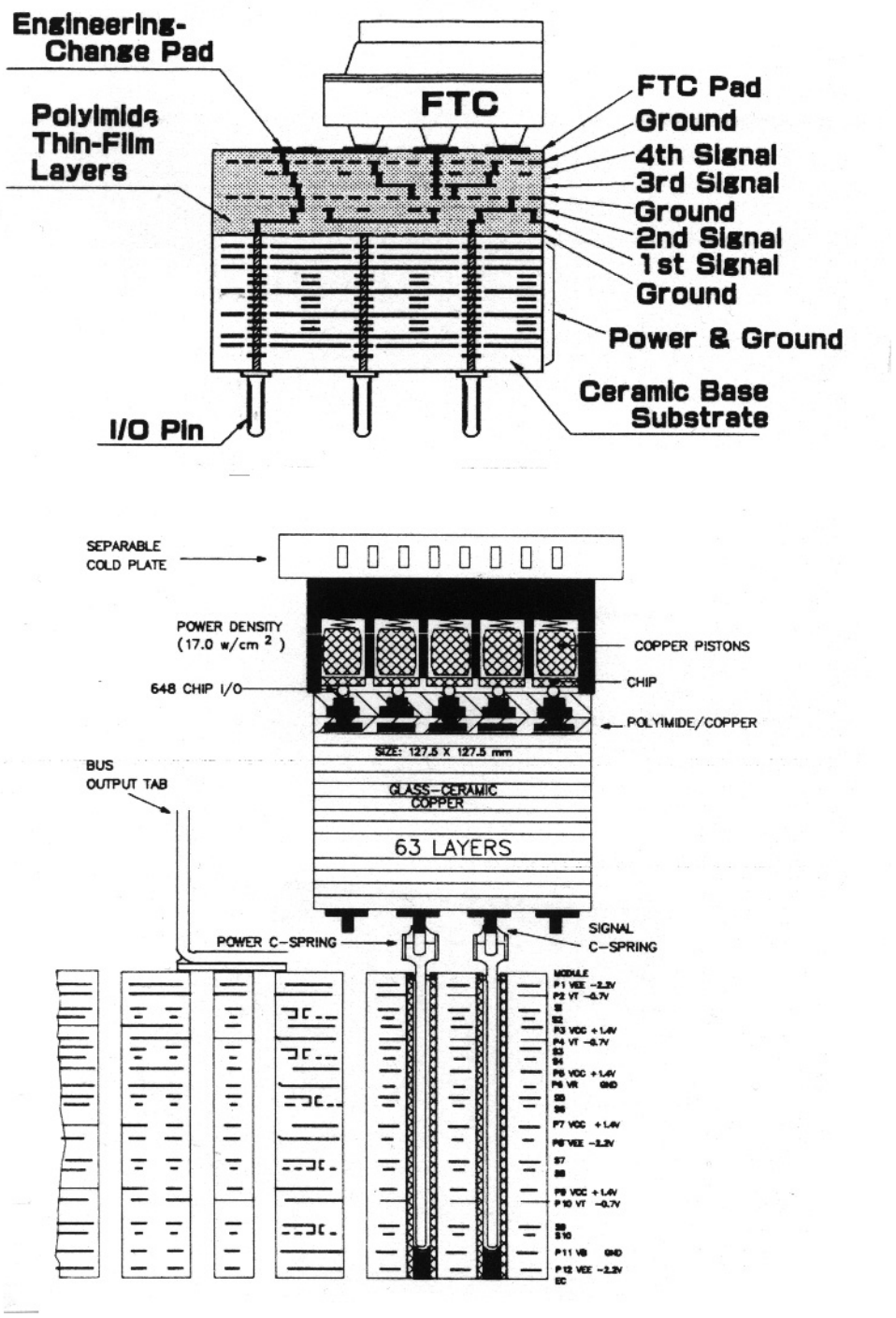
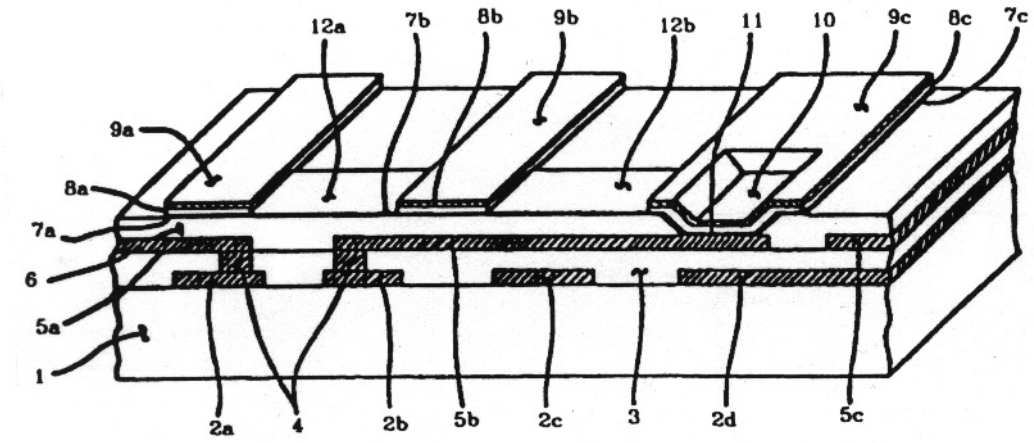


Fig. 8.24 High performance modules made in a combination of multilayer thin film and multi layer ceramic technology: a): NEC Corporation computer SX-3 [8.24] using flop TAB carrier on thin film and alumina based substrate, and b): IBM Enterprise System/9000 packaging hierarchy [8.23] using flip chip, polyimide/copper thin film on 63 layers glass ceramic substrate.



1	Alumina substrate.
2	a,b,c,d:Printed conductor on first layer.
3	Printed dielectric film.
4	Optional compensation printed in vias.
5	a,b,c: Printed conductor on second layer.
6	Glass based dielectric.
7	a,b,c,d: Tantalum nitride resistive layer.
8	a,b,c,d: Molybdenum diffusion barrier.
9	a,b,c: Thin film gold lines.
10	Via hole between thin film and thick film conductive layer.
11	Contact area in thick film. Gold-platinum or gold-palladium.
12	a,b: Resistor in thin film made by selective etching in thin film structure.

Fig. 8.25 AME´s combination technology combining thick film and thin film, cross section [8.25].

REFERENCES

[8.1] J. J. Licari and L.N. Enlow: "Hybrid Microcircuit Technology Handbook". (Noyes Publications 1988).

[8.2] F.N. Sinnadurai: "Handbook of Microelectronics Packaging and interconnection Technologies". (Electrochemical Publications 1985).

[8.3] R.K. Hoffmann: "Handbook of Microwave Integrated Circuits". (Artech House 1987).

[8.4] "Hybrid Microcircuit Design Guide". ISHM-1402/IPC-H-855, 1982.

[8.5] a): L. Halbo (Ed.): "Polymer Thick Film Technology (PTF) - Design Guidelines and Applications". (Lobo, 1990. Available from ElektronikCentralen, Denmark).
b): L. Halbo, C. W. Nielsen and S. Nørlyng: "Design Guidelines for Polymer Thick-Film Technology", Circuit World Vol. 17 No. 3, 1991.

[8.6] R.R. Tummala and E.J. Rymaszewski: "Microelectronics Packaging Handbook". (van Nostrand, 1989).

[8.7] IEEE Trans. Comp., Hybrids, and Mfg. Techn. vol 12 no. 2, 1989: Special section on Multichip Packaging, p. 161 ff.

[8.8] E. Bogatin, Raychem: "Beyond PCB densities: A new commercial multichip packaging technology", and technical data sheets from Raychem, 1989.

[8.9] R. Jensen at CEI Elsevier "Advanced Semiconductor Packaging Course", Garmisch-Partenkirchen, November 1988.

[8.10] a): W. G. Burger and C. W. Weigel: "Multilayer Ceramic Manufacturing". IBM Journal of Res. and Dev. vol. 27, no. 1, Jan. 1983.
b): A. J. Blodgett: "Microelectronic Packaging". Scientific American July 1983, p.86.

[8.11] a): "MLC Design guidelines", Ericsson Components, 88 - 05.
b): I. Henne, L. Halbo et al.: "Multichip modules for Gigabit-per- sec. electronic circuits". EPF-report, March 1990 (in Norwegian).

[8.12] a): J.I. Steinberg et al.: "Low temperature cofired tape dielectric material system for multilayer Interconnects". Hybrid Circuits, no 9, Jan. 1986.
b): A.L. Ustice et al.: "Low temperature cofirable ceramics". 1986, p. 49.
c): M. Massiot: "Low temperature cofiring technology - an industrialization example". ISHM meeting Hamburg, 1989.

[8.13] Siegert data sheet.

[8.14] C.G. Connitzer et al.: "Tape transfer technology for multilayer circuits". Hybrid Circuit Technology, August 1989, p. 39.

[8.15] J.K. Logan: "Fixed-Point Probe Cards - A Neglected Resource for Hybrid Probing". Hybrid Circuit Technology August 1989, p. 17.

[8.16] G. Zoepette: "Minis and Mainframes." IEEE Spectrum, vol. 27, 1990, p. 30.

[8.17] L. Hyden et al.: "Silicon Circuit Boards: Off - The - Shelf Convenience". Electronic Packaging and Production, April 1988, p. 70.

[8.18] a): A. Kabe and I. Morooka: "Polymer Thick Film Circuits in Japan". Hybrid Circuits no. 6, January 1985, p. 24.
b): I. Morooka: "Polymeric Thick Film Additive Multilayer". Proc. Printed Circuit World Convention IV, Tokyo, June 1987,
p. 78 - 1.

[8.19] W. Martin et al.: "Thermal Resistance and Temperature Cycling Endurance of DCB Substrates." Hybrid Circuits no. 22, May 1990, p. 29.

[8.20] J. Blum et al. "Aluminum Nitride Substrates for Hybrid Microelectronic Applications." Hybrid Circuit Technology, August 1989, p. 7.

[8.21] R. Wayne Johnson et al., eds.: "Multichip Modules - Systems Advantages, Major Constructions, and Materials Technologies". Selected reprints, IEEE Press 1991.

[8.22] J. L. Sprague: "Multilayer Ceramic Packaging Alternatives." IEEE Trans. Comp., Hybrids and Manuf. Technology. vol. 13, no. 2 June 1990, p. 390.

[8.23] R. R. Tummala and S. Ahmed: "Packaging Technology for the IBM Enterprise System/9000 Based on Glass-Ceramic Copper/Thin film Thermal Conduction Module." IEEE Trans. Comp., Hybrids and Manuf. Technology. vol. 15, no. 4, August 1992, p. 426.

[8.24] H. Murano and T. Watari: "Packaging Technology for the NEC SX-3 Supercomputers." IEEE Trans. Comp., Hybrids and Manuf. Technology. vol. 15, no. 4, August 1992, p. 411.

[8.25] B. E. Flaten et al.: "Combifilm Hybrids for High Performance Multichip Modules." Proceedings IEPS 1991, p.49.

[8.26] J. M. Segelken et al.: "Ultra-Dense: An MCM-Based 3-D Digital Signal Processor." IEEE Trans. Comp., Hybrids and Manuf. Technology. vol. 15, no. 4, August 1992, p. 438.

[8.27] R. Wayne Johnson et al.: "Plated Cu on Ceramic Substrates for Power Hybrid Circuits." IEEE Trans. Comp., Hybrids and Manuf. Technology. vol. 12, no. 4, December 1989, p. 530.

[8.28] F. Miyashiro et al.: "High Thermal Conductivity AlN Ceramic Packages and Substrates." IEEE Trans. Comp., Hybrids and Manuf. Technology. vol. 13, no. 2, June 1990, p. 313

[8.29] W. Zhu et al.: "Growth and Characterization of Diamond Films on Nondiamond Substrates for Electronic Applications." Proc. IEEE, vol. 79, no. 5, May1991.

[8.30] A. Bjørneklett: "Plasma Spray Technology for Power Electronic Hybrid Circuits." Ph. D. Thesis, University of Oslo, 1993.

[8.31] A. Bjørneklett, L. Halbo et al.: "Hybrid Substrates for Power Electronic Applications: An Investigation of Thermal Resistance and Mechanical Stress." Hybrid Circuits no. 30, January 1993, p. 53.

CHAPTER 9

MICRO STRUCTURE TECHNOLOGY AND MICROMACHINED DEVICES

Abstract

Micro structure technology and micromachined device technology have emerged during the three last decades. At first they were mainly technological spin-offs from microelectronics/integrated circuit technology. Sensor applications gave the main market pull, batch processing the key to high quality at low cost. Silicon micromachining established itself as a unique process technology with distinctive features. Today, these technologies and these devices have matured into a separate industry sector with their own market and manufacturing infrastructure, also with the use of other materials than silicon. The devices are used in microelectronic systems with widespread use, ranging from low cost, high volume automotive applications to high cost, low volume instrumentation applications. The micro structure technology and micromachined devices have during these years shown a much slower learning curve than microelectronics in general, making them to bottlenecks for performance and cost improvements in their systems. The herald of the rapid development of integrated circuit technology - batch processing - is one of the important keys to ease these bottlenecks. The basics of the micro structure technology and micromachined devices are introduced. The most important batch processes for micromachined devices are also highlighted and recommendations for future batch processing developments for micromachined devices are given.

9.1. INTRODUCTION AND MOTIVATION: DEFINITIONS, AN EXAMPLE OF A MICROMACHINED DEVICE AND THE MAIN DRIVING FORCES

MICRO STRUCTURE TECHNOLOGY can be defined as a group of three-dimensional micromachining techniques enabling feature dimensions with accuracy in the micrometer range.

MICROMACHINED DEVICES can be defined as devices made by Micro Structure Technology.

These micromachining techniques are mainly based upon batch organised microelectronic process technology, either directly adapted techniques like photolithographics, or modified techniques such as anisotropic etching techniques. Some micromachining techniques are specially developed for this field, e.g., anodic bonding of micromachined devices.

Today, these devices have matured into a separate industry sector with their own market and manufacturing infrastructure, also with micromachining of other materials than silicon. They are used in microelectronic systems with widespread applications, ranging from low cost, high volume automotive applications to high cost, low volume instrumentation applications.

The micromachined devices have during these years shown a much slower learning curve than microelectronics in general, making them to bottlenecks for performance and cost improvements in their systems. The herald of the rapid development of integrated circuit technology - batch processing - is one of the important keys to ease these bottlenecks. This paper will therefore focus on the batch organised processes.

Photolithographic etching techniques are excellent examples. These techniques have become feasible as a result of the advanced solid state technology developed to manufacture silicon integrated circuits. In this way high-quality and inexpensive manufacturing processes have become available to produce high-performance, miniaturised and inexpensive micromachined devices.

Single crystal silicon is by far the most used material for micromachined devices. We will later show that this is both due to the unique features of this material and the strong infrastructure support from the field of silicon integrated circuit technology. Several other materials and material systems are used, e.g. gallium arsenide, quartz and polymers. This author will focus on silicon micromachined sensors, partly because this is the most important, and partly because this is the application area I know best.

Applications areas are mainly within sensors for sensing mechanical quantities such as pressure, force, flow and acceleration, but sensors for other measurands such as for example light or chemical quantities can also benefit from this technology. Actuator applications and miniaturised precision assembly parts are also important. We are still at the innovative stage of development of these devices, and new ways of using this technology will emerge which will increase the feasibility and expand the application area. At present, the potentials of this technology seem to be restricted by the ability of device designers to come up with innovative new designs.

The field can of course be divided into many sub fields. An example could be: By combining sensor elements made by micromechanics in silicon with silicon integrated circuits on the same chip set, a new sensor concept has emerged, the MICROMECHANICAL SMART SENSOR. A smart sensor is a device in which one or more sensing elements and signal conditioning electronics are integrated on the same silicon (or gallium arsenide) chip. By including micromechanics in this concept, we have the MICROMECHANICAL SMART SENSOR. This kind of sensors combines the features of silicon both as an electronic material, as a micromachinable material and as a sensor material, and is by many expected to have a great impact on the sensor market as well as the electronic instrument system market in the coming years.

Example

As an example of a typical micromechanical sensor, we will explain the design, processing and main features of the SP80 Pressure Sensor, developed at SINTEF (earlier Center for Industrial Research), Norway and manufactured by SensoNor A/S (earlier ame), Norway. This sensor visualises the main features and limitations of micromechanical sensors, and points out pressure sensing as the main application for these kinds of sensors.

The SP80 is a piezoresistive integrated pressure sensor with the pressure-sensitive diaphragm micromachined in a silicon chip by anisotropic etching and with ion implanted piezoresistors in a full Wheatstone bridge configuration as the electronic sensing element. In addition, a temperature measuring resistor and a heating resistor are implanted on the same chip, making it possible to thermostat the chip to minimise thermal drifts. By varying the area and the thickness of the diaphragm, the family of these sensors comprises a number of pressure ranges from 0.5 Bar full scale pressure up to 60 Bar full scale pressure, all with equally high full scale output signal.

The device is packaged in a transistor header, and main application areas are within general instrumentation, metrology and aerospace application.

The silicon chip set is shown in Figure 9.1, and consists of diaphragm chip sealed to a support chip which is mounted on top of a glass tubing acting as a mounting stand as well as a pressure port.

The size of the chips is 4*4 mm, chip thickness approximately 0.3 mm, the diaphragm area is typical 2*2 mm and the diaphragm thickness is typical 30 micrometers. The diaphragm is manufactured by stripping off the surface oxide of the silicon wafer by means photolithographic technique in the areas we want the diaphragm cavity. Then the wafer is etched in an anisotropic etching solution with the remaining oxide as masking film. This etching solution attacks the single crystal silicon with different speed in the different crystal directions. The etch is extremely slow in the <1-1-1> direction, meaning that the etch is stopped towards the (1-1-1) planes. The chip material is (1-0-0) silicon, and this means that the etch cavity is surrounded by four (1-1-1) planes which have an angle of inclination of 54.7 degrees relative to the (1-0-0) surface plane, rendering a cavity with four sloped walls as indicated on Figure 9.1.

In this way we can control the diaphragm area, but we also need a technique to control the thickness of the diaphragm, and in this design this is done by doping the silicon with a high concentration boron stopping layer. The etching speed is slowed considerately with increased boron concentration, thereby making it possible to remove the wafer from the etching solution when the slow-etching mode is reached and a well-defined diaphragm thickness is obtained.

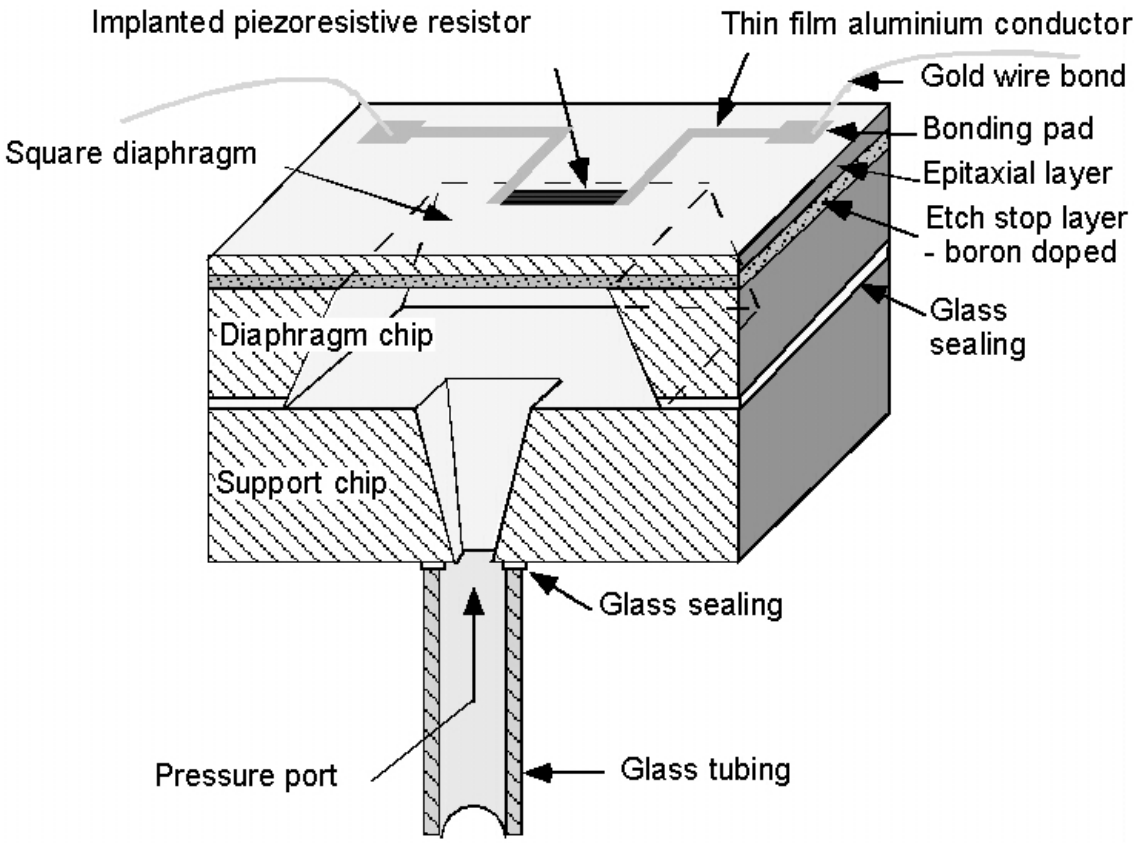


Fig. 9.1: Cross-sectioned view of the silicon chip set of the SP80 Pressure Sensor.

However, the process for the ion-implanted piezoresistors is not possible in the boron-doped stopping layer, therefore an additional layer of single crystal silicon has been deposited by epitaxial technique at an earlier stage of the processing. The thickness of the epitaxial layer can be tailored with great accuracy, and together with the stopping layer this gives the total thickness of the diaphragm. The sensing electronics including the piezoresistors is processed on top of the epitaxial layer. This is done by standard techniques well known from the silicon integrated circuit processing technology. The piezoresistors are located along the edges of the diaphragm midway between the corners. This is where we have maximum diaphragm stress due to applied pressure, and by orienting two of them with current direction parallel with the edges and two of them transversal to the edges, two and two will change value with opposite sign as a function of applied pressure. In this way we get a full Wheatstone bridge with four active arms, having a full scale output signal at approximately 30 mV/V. The schematic of the device is shown in Figure 9.2.

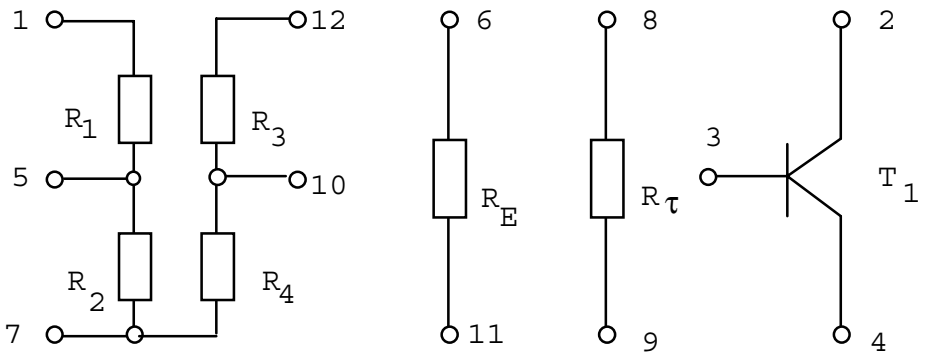


Fig. 9.2: Electrical schematic of the SP80 Pressure Sensor.

The device is mounted and packaged in a transistor header as shown in Figure 9.3. The glass tubing is epoxy sealed to the pressure connection tubing in such a way that the chip set is free-standing on top of the glass tubing and therefore well mechanically and thermally isolated from the transistor header. Mechanical isolation is crucial to obtain isolation from handling and mounting strain, a must to obtain good short-term and long-term stability, and good thermal isolation enhances the temperature accuracy as well as reduces the power requirements when thermostating the device.

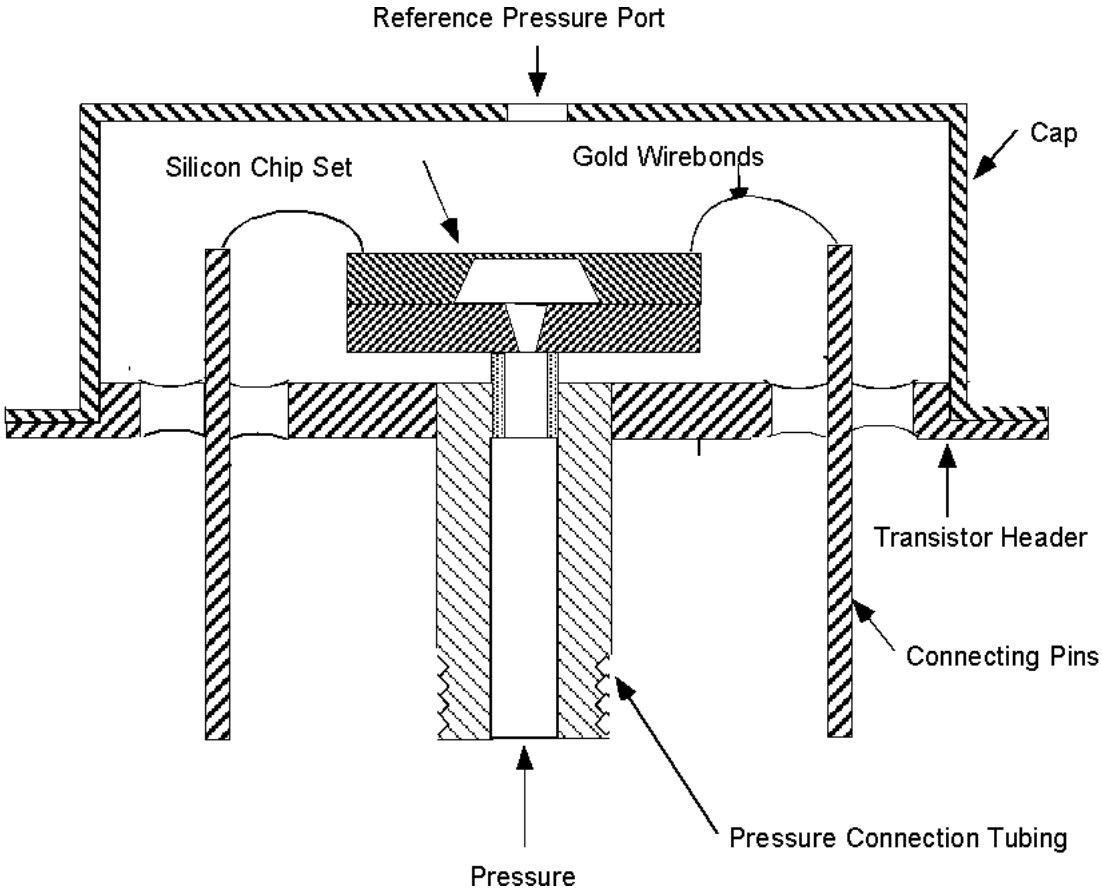


Fig. 9.3: Cross-sectioned view of the SP80 Pressure Sensor packaged in a transistor header.

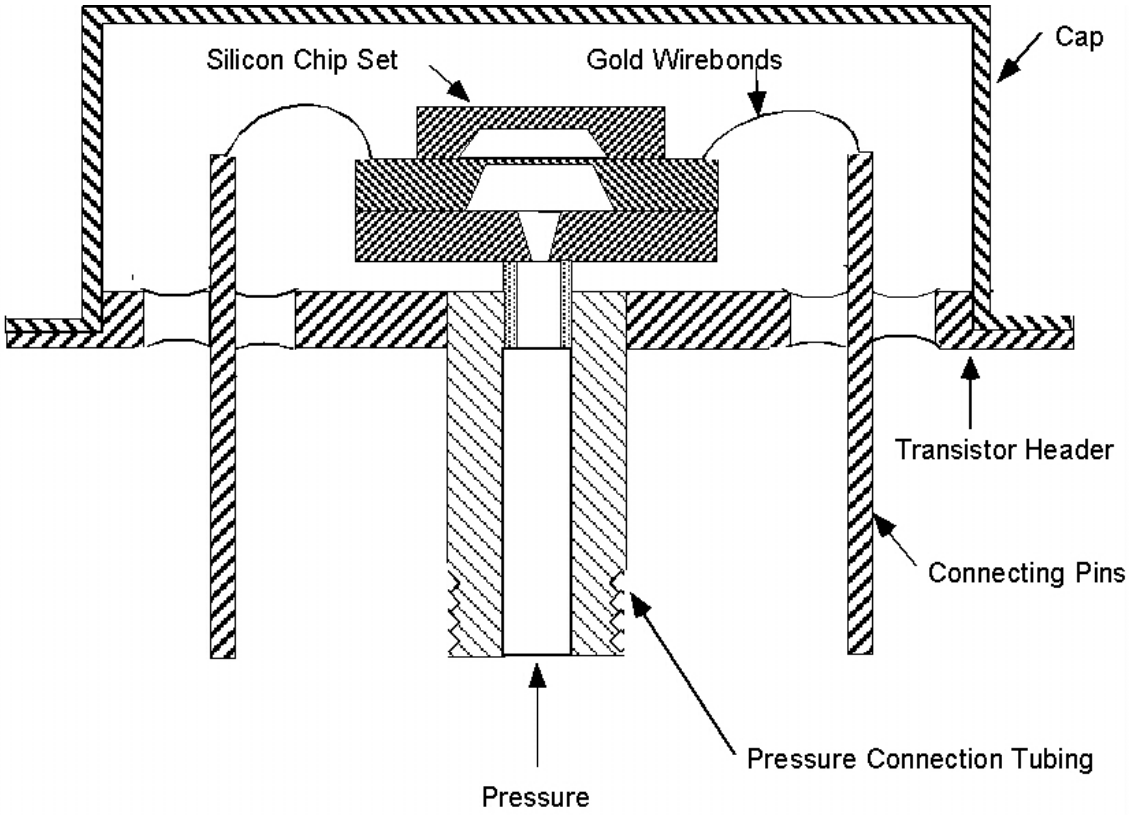


Fig. 9.4: Cross-sectioned view of the SP80 Pressure Sensor with a top chip containing a vacuum reference chamber.

The Reference Pressure Port makes this sensor a differential pressure sensor. If gauge pressure measurement is wanted, the Reference Pressure Port is omitted, and the absolute pressure sensor version has an extra chip sealed on top of the chip set with an etched vacuum reference chamber, as shown in Figure 9.4.

A picture of the assembled unit is given in Figure 9.5, and as can be seen, this sensor is more a system component than a transducer, as electrical connection and interfacing are necessary, as well as mechanical mounting, before the device is ready to measure pressure.

Main features of this sensor are:

- Low non-linearity (< +- 0.1%)
- Negligible hysteresis (< +- 0.005% of full scale output)
- Low long term drift (typical less than 0.1% per year)
- Active thermal compensation by utilising the on-the-chip heating resistor.
- Small size.

Of course, there are drawbacks too:

- Reference pressure medium must be non-conducting and non-corrosive to be compatible with the on-chip sensing elements and electronics.
- Safe overload is limited to 3 times rated pressure as no mechanical overload stop is implemented.
- The devices have no normalised output signal meaning each device has to be individually calibrated when system installed. The output signal in the millivolt range must be amplified and signal conditioned to be converted

to standard output signal form like, e.g. 0 - 5 Volts from zero to full scale pressure.

- Temperature range is limited (-55 - +125 °C) and uncompensated thermal sensitivity drift is relative high (= -0.2%/°C).

The bottom line is whether such a device has the preferred price/- performance ratio. At present, this is not always true for micromechanical sensors compared to more traditional sensors or other competing technologies. However, based upon the excellent qualities of silicon as a sensor material combined with its micromachining capabilities and low cost silicon technology batch processing, these sensors are by many believed to be future winners. The main challenge will probably be to come up with sensor designs that combines mechanics, electronics and processing in such a way that high quality, low-priced device are achieved.

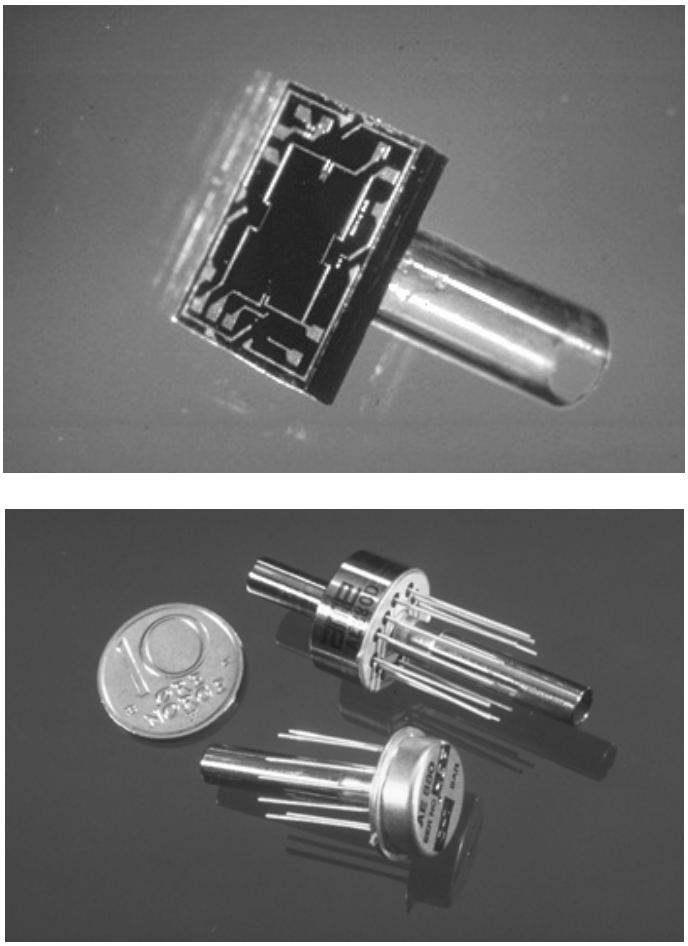


Fig. 9.5: Picture of the SP80 Pressure Sensor.

<u>Rapid advances in silicon planar technology have made micromachined devices competitive</u>

The planar silicon technology has been the busiest workhorse in the advancement and expansion of the integrated circuit technology during the past three decades. This technology is the basis for the modern electronics with all its

advanced computers, measurement & control systems, etc. There has been a heavy technology push as well as a strong market pull, the first visualised by Moore`s law saying that the maximum number of components per IC chip doubles approximately every 18 months, and a market growth for the semiconductor industry of about 20% per year. This growth has declined somewhat lately as the industry and market mature, but there still exists strong growth potentials to fuel further technological advances and price/- performance improvements.

Milestones in the planar silicon processing technology:

- 1948: The invention of the transistor.
- 1959: The invention of the planar silicon processing and the invention of the integrated circuit.
- 1971: The invention of the microprocessor.
- 1985: 1 Megabit random-access-memory chips available.
- 1991: 4 Megabit random-access-memory chips available.
- 1994: 64 Megabit random-access-memory chips available.
- 1995: Microprocessors with more than 3 million transistors available.

Micromachined devices are to a large extent based on silicon planar technology because this technology is suitable for these devices, but first of all because these methods are developed to an advanced stage with the strong market pull from the integrated circuit market. This has resulted in a well-assorted choice of advanced processing techniques as well as comparatively inexpensive and diversified processing equipment for manufacturing micromechanical sensors.

Silicon, and first of all single crystal silicon, has been drawing the attention of material researchers in order to push planar silicon processing advances, and therefore silicon is one of the best known materials with both mechanical, chemical and electronic characteristics well known and documented. The low impurity, low-defect single crystal silicon wafers manufactured for the IC industry are, for example, a strong, almost perfect elastic material well suited as spring element in sensors for mechanical quantities.

Based mainly on silicon, the IC world market is more than $60 billions today with still a high growth potential making the IC industry one of the most important industries of the future, not only by its own size, but also because its impact in almost every other industry. An example could be office automation based on electronic information systems built with cheap and powerful silicon integrated silicon chips giving dramatic productivity improvements, or the automobile industry turning from an almost mechanical basis into more and more use of electronics.

The demand for micromachined devices with sensors as area of example

Mainly as a result of the success of the integrated circuit industry, electronic measurement & control systems have become cheap and powerful and gained new markets as technology acceptance has matured.

The central unit of such system with signal conditioning, data processing and communication administration has a record of success, and data presentation systems such as monitors and printers are also reaching an advanced technological level, giving an ever increasing performance increase per $.

These systems need input signals from sensors to handle their tasks, and sensors are more and more becoming the expensive and critical part of such systems because both performance and price have not progressed in the right direction with the same speed. Sensor designs dated back more than two decades are still on the market and competitive, often based on complicated and laborious assembling techniques making them bulky, fragile and expensive.

New sensor designs are often hard to achieve, having to be compatible with harsh environments, rough handling and stringent demands on measuring accuracy, and a lot of consideration, testing and redesign is more the rule than the exception before market acceptance is achieved. This is giving a time lag from idea to running high- volume production that can be several years and sometimes a decade. This time lag severely hampers technological advances within sensor technology, and has also a frightening effect on entrepreneurs, who often prefers to invest their money in less speculative fields with faster investment returns.

This is a tremendous challenge for the sensor industry, and as the market grows and technological advances are made, things are beginning to move with faster speed, and an increasing quality at a declining price is expected in the coming years, though not so dramatic as in the IC industry. Micromechanical sensors are heralded as one of the main roads to achieve these goals in the future as such sensors both have promising high-quality features and can be inexpensively manufactured by silicon batch processing and packaging technology.

Market and applications for micromachined devices with sensors as area of example

Business opportunities for micromechanical sensors have until recently been almost exclusively been in high-tech fields such as medical technology and industrial process control technology. These are fields with long traditions as pioneers in high-tech both from a technological and a funding point of view, fuelling ideas from the university laboratories into manufactured and marketed high-volume products.

These two markets still are the most important with a multitude of applications and increasing numbers of new business opportunities, but as technology acceptance is achieved, new markets sectors are emerging for micromechanical sensors. The following market sectors with applications examples give an indication on how widespread and diversified the business opportunities for micromechanical sensors are:

- The industrial process control sector market. Application examples:
  - Flow sensors in gas pipelines.
  - Tank level measurements by pressure measurement.
- The medical sensor market. Application examples:
  - Blood pressure sensors.
  - Brain pressure sensors.
  - Microphones for hearing aids.
- The measurement instrumentation market. Application examples:
  - Electronic barometers.
  - Infrared light detectors.
  - Vibration sensors.
- The automotive market. Application examples:
  - Carburettor manifold absolute pressure sensor.
  - Accelerometers as crash sensors in air bag systems.
  - Suspension control accelerometer.
  - Air flow sensor.
- The consumer market. Application examples:
  - Level measurement in white goods appliances.
  - Pressure and flow sensors in air condition systems.
- The agriculture electronics market. Application examples:
  - Automotive sensors used in tractors, harvesters, etc.
- The off-shore oil exploitation market. Application examples:
  - High pressure measurement in oil wells.
  - Sea wave sensor.
- The avionics, space & military markets. Application examples:
  - Accelerometers for rocket navigation.
  - Micro gravity sensors.

Among these markets the automotive market has drawn a lot of attention during the last years as electronics has entered under the hood and into the cabin. The automotive industry has reluctantly started to use more electronics, partly to meet governmental legislation and partly as a result of market pull, and with some and thirty millions cars produced each year, suppliers are tempted with high-volume orders of for instance carburettor manifold absolute pressure sensors. This is the most high-volume application of micromechanical sensors, and it is believed that research efforts and manufacturing facilities set up to produce these sensors will have a major technological impact. This is also leading to reduced prices, which again will open up new markets and new applications for micromechanical sensors.

Competing technologies for micromachined devices with sensors as area of example

The competing sensor technologies for micromechanical sensors are multiple and diversified, some based one more traditional hand-crafted technology and some based on modern manufacturing technologies with both general and specific application areas.

Most of them have in common that they are based on old, but fine-tuned technology meaning they are harder to beat than expected from a theoretical

evaluation of their advantages and drawbacks compared to silicon micromechanical sensors.

Those sensor technologies that are based on modern manufacturing technologies have almost all just like micromechanical sensors emerged as spin-offs from modern solid state technology and/or general electronics, where large markets have attracted a lot of research efforts.

Among the competing technologies we could mention:

- Metal-diaphragm capacitive pressure sensors. These sensors use the gap variance between a pressure sensitive metal diaphragm and an electrode plate as an air dielectric capacitance pressure sensor. This sensor principle has been used for years with excellent results. Among its features is high thermal stability, while one of its main drawbacks is the need for sophisticated signal conditioning electronics. This drawback is no longer a problem with state-of-the-art advanced and inexpensive electronics, and for instance in the automotive sector these sensors are very competitive.
- Strain gage pressure sensors. The pressure is by way of a pressure sensitive diaphragm converted into mechanical strain, which is sensed as a resistance change. The resistance changing element is either an unbonded wire gage, or a deposited-metal-film (mostly thin film), or a bonded semiconductor gage.

Most often there are four, sometimes two strain gages in each sensor making up the four (two) arms in a Wheatstone bridge. The Wheatstone bridge configuration has several advantages compared to a single gage sensor, among these we would point out better thermal stability, increased linearity and higher sensitivity. Most of today's micromechanical pressure sensors are based on this principle, as the next logical step was to integrate piezoresistive strain gages in a micro- machined pressure-sensitive diaphragm.

- Piezoelectric accelerometers and vibration sensors.
  Accelerometers and vibration sensors are based on the acceleration of a seismic mass restrained by a spring element and with a sensing element either based on strain or position detection. A piezoelectric crystal material such as quarts or a ceramic material such as barium titanate is very attractive to use in such sensors. Strain in the material produces an electrical charge displacement in the material, giving the possibility to let a disc of the crystal material act as the seismic mass, the spring element and the sensing element.

  However, since such a sensor is based on charge redistribution, they can only measure dynamic acceleration. Steady-state acceleration will give a fixed charge on the electrodes that is lost in short time due to leakage current and input current in the detecting electronics.

To summarise there is a large number of sensor technologies competing on the same or parts of the same market as micromechanical sensors. A rough estimate of the world market for sensors could be $2 billions in 1995, with micromechanical sensor having a market share of some twenty per cent. This market as well as this share is expected to increase in the coming years, but the bottom line is that micromechanical sensors are facing stiff competition from other sensor technologies emphasising the need for improved designs, cost-effective manufacturing and aggressive marketing.

Manufacturers of micromachined devices with sensors as area of example

The industry structure within micromechanical sensors is highly diversified both in size, technological basis and organisation type. Some typical examples can visualise this:

- Traditional sensor manufacturers have seen micromechanical sensors as a natural expansion of their technological basis, and have taken up research and production of these sensors as a part of their activity.
- Semiconductor companies have entered this market as a logical expansion of their integrated circuit activity, since they already have most of the needed equipment and the appropriate marketing channels.
- System companies or original equipment manufacturers, which see micromechanical sensors as a way to boost their systems to higher performance, levels. This includes even companies with their main activity outside the electronics field; e.g. the auto maker GM is using its subsidiary company Delco to produce micromechanical pressure sensors for cars.
- "Start ups", companies having micromechanical sensors (some- times as a part of micromechanics in silicon) as their main business idea.

There are of course companies that do not fit into any of these types and some are somewhere in between these types.

Manufacturers of micromechanical sensors are spread all over the world, with USA and especially Silicon Valley as the main location, but also companies in Western Europe and Japan are active as manufacturers of micromechanical sensors. In Table 9.1, several of the manufacturers world-wide are listed.

Since this is a growing field there are many business opportunities and a good guess is that the number of manufacturers will increase in the coming years. Some companies are, according to rumours having problems because they have underestimated the technological difficulties needed to be solved to get market-accepted products. However, a shake-out will probably not occur in a long time since the market is growing and a lot of special products with market niches rather than standard products are asked for in the market.

Honeywell	**USA**
Microswitch	**USA**
SenSym	**USA**
IC Sensors	**USA**
Motorola	**USA**
Delco	**USA**
Foxboro/ICT	**USA**
Endevco	**USA**
Kulite	**USA**
Lucas NovaSensors	**USA**
Michigan Microsensors	**USA**
Hitachi	**Japan**
Toshiba	**Japan**
NEC	**Japan**
Yokagawa Hokushin	**Japan**
Toyota Motor Company	**Japan**
Siemens	**Germany**
Philips	**The Netherlands**
Microtel	**The Netherlands**
Xensor Integration	**The Netherlands**
Druck	**UK**
Keller	**Switzerland**
Vaisala	**Finland**
Radi Medical System	**Sweden**
SensoNor	**Norway**

Table 9.1: Examples of manufacturers of micromachined sensors

Research activity in micromachined devices with sensors as area of example

Research activity in this field is very intensive as this a relative new field with the need for a lot more basic research as well as more product and process oriented development to establish a matured technological basis for the involved manufacturers. There is a rather sharp division between scientific research and company research:

- Pioneering research was done and still is done by several universities and research institutions, often sponsored by governmental funding agencies. In Table 9.2 some of the most well known examples are listed. Stanford University in California should be honoured as the pioneer centre, being the first to establish micromechanical sensors as an independent research field, and later several universities and research centres have taken up micromachined sensors as research activity.

Stanford University	**USA**
Case Western Reserve University	**USA**
University of Michigan	**USA**
University of California, Berkeley	**USA**
University of Wisconsin	**USA**
MIT	**USA**
Tohoku University	**Japan**
Kyoto University	**Japan**
Fudan University	**Peoples Republic of China**
Delft University	**The Netherlands**
Twente University	**The Netherlands**
IMEC	**Belgium**
Catholic Un of Leuven	**Belgium**
University of Neuchâtel	**Switzerland**
CSEM	**Switzerland**
Fraunhofer Institute, IFT Munich	**Germany**
Fraunhofer Institute, IMT Berlin	**Germany**
Techn. Un of Berlin	**Germany**
Techn. Un of Denmark	**Denmark**
VTT	**Finland**
Uppsala University	**Sweden**
KTH/IMC	**Sweden**
SINTEF	**Norway**

Table 9.2: Examples of research centres for micromachined sensors

As the technology has matured it has attracted entrepreneurs that have seen its potential for commercial exploitation, and more of the research and development of micromechanical devices have taken place in the laboratories of the manufacturers rather than at the universities. This has lead to a substantial increase of research resources, but also to a less open scientific communication, as companies want to keep their acquired technology in secret. However, this field is still characterised by an unusual open scientific communication even from the manufacturing companies, as all parties see the advantage of exchanging their results to fertilise further technological progress. Some processes and designs are patented, but most of these patents are of minor value since technological progress is moving faster than the patent bureaucracy, meaning that the patent often is old- fashioned already before it is properly protected. Therefore, most innovations are not patent protected, but commercial exploited by the innovators simply by keeping it confidential until products are marketed and using the time advantage to make money before the innovation are copied or further developed by competitors.

Research in this field is calling for resources at a lower level than present-day silicon integrated circuit technology, and this has lead to that several centres earlier involved with IC research have taken up micromechanical sensors as their speciality. This has given the field a lot of talented people with academic background in solid state physics using solid state physics in a very successful manner in micromechanical sensor research.

On the other hand, micromechanical sensor research calls for a lot of innovative and competent research related to the field of mechanical engineering, and it looks very obvious that this part has not been given proper attention. This has resulted in a critical need for the micromechanical sensor field to attract talented mechanical engineers to implement state-of-the-art mechanical engineering in new product designs. All in all, research in the field of micromachined devices is a multi-disciplinary research field calling for talents from many fields. The centres that are able to meet this challenge will probably have a better chance to be successful than others in their research efforts.

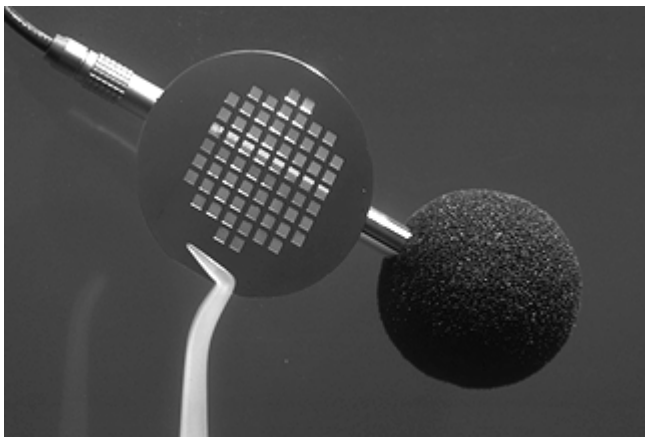


Fig. 9.6: A silicon wafer with micromachined diaphragms for condenser microphones made at SINTEF. Batch organised planar processing and micromachining is used to make microphones that have low zero pressure distortion. Controlling the initial mechanical stress by doping the material, 4x4 mm^2 diaphragms of thickness 1 micrometer have been made with a resonant frequency of 10-13 kHz for an initial stress of 10-15 MPa. (Photo: Jan D. Martens, SINTEF)

9.2. KEY FACTORS TO SUCCESSFUL INDUSTRIAL INNOVATION OF MICROMACHINED DEVICES

Micromachined device technology is a true-born offspring from integrated circuit technology with silicon as the most used material. Micromachined devices are mostly used as sensors and actuators in microelectronics systems, with sensors being the most important. There are several key success factors specific for micromachined devices are [9.1], [9.2]. We suggest the following subjective list:

The top ten success factors of micromachined devices

1. Batch organised planar processing technology offers high quality, low cost, batch organised ways to manufacture micromachined devices. This

includes both subtractive techniques such as etching and additive techniques such as thin film deposition.

2. Microelectronics manufacturing infrastructure offers a wide range of advanced services for the manufacture of micromachined devices, e.g. high quality materials such as silicon wafers and photo masks, and sophisticated equipment such as aligners and implanters.

3. Research results from solid state technology and other related fields of microelectronics. This is first of all the accumulated research results of silicon microelectronics, making silicon by far the most investigated electronic material. Advanced research results are also available for other materials used for micromachined devices.

4. Micromachining. Anisotropic, isotropic and selective etching techniques combined with photolithography make high-precision, miniaturised three dimensional structuring feasible. This micromachining capability is first of all achievable with single crystal silicon, but both in principle and practice other materials can be used, e.g. gallium arsenide, quarts or polysilicon.

5. Wafer and chip bonding. To assemble into packaged units, bonding on wafer level or chip level is necessary. Main techniques are silicon-to-silicon bonding, silicon-to-glass bonding and silicon-to-thin film bonding. The techniques can be used for both chips and wafers. Silicon-to-silicon fusion bonding is a high temperature process giving high strength, used primarily for wafers. Anodic bonding is a low temperature process used both for chips and wafers. Other available processes are gluing, soldering and welding.

6. Mechanical material characteristics. The used materials feature favourable characteristics as mechanical materials. Single crystal silicon is here an excellent example, with its high strength and almost perfect elasticity, making it an excellent spring element for sensors and actuators.

7. Sensor effects. The materials used has a large number of physical effects that can be used for signal conversion for sensors, for instance piezoresistivity for sensing in the mechanical signal domain and Hall effect for magnetic signal.

8. Actuator functions. The technology facilitates microscale actuating functions such as micromotors and micropumps.

9. Integrated electronics. Many of the used materials have excellent properties as electronic materials. By combining micromachined devices with on-chip, integrated signal-conditioning electronics, so-called micromachined smart devices, improved or new sensing and actuating methods can be used. For instance, silicon capacitive sensors are very

hard to make without on-chip circuit, because both capacitance and capacitance change are in the picofarad range.

10. Combination of features can make very competitive products. Single crystal silicon is in this respect as outstanding. E.g., a silicon micromachined smart pressure sensor [9.2] makes extensive use of these features.

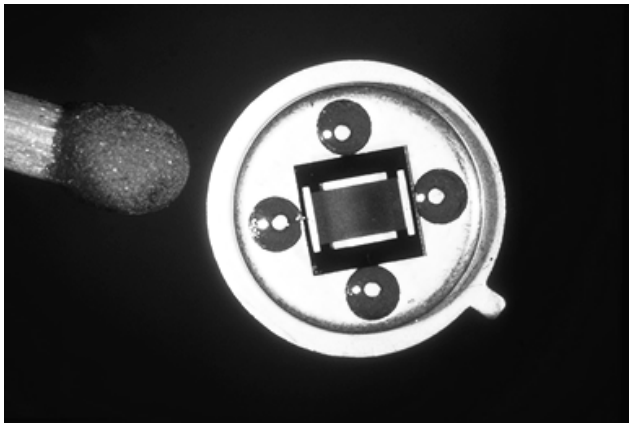


Fig. 9.7: The SINTEF/Simrad Optronics Silicon Micromachined Infrared Source as an example of an actuator. This is used in a gas monitoring system, using the absorption of infrared light as sensing principle. Due to the low thermal mass, this actuator can be electrically chopped up to 1 kHz, replacing a bulky electromechanical chopper. (Photo: Jan D. Martens, SINTEF)

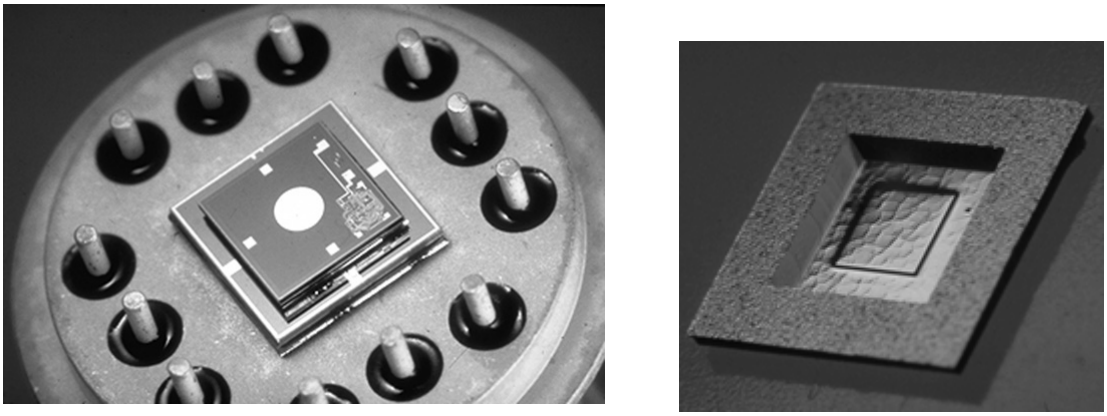


Fig. 9.8. The SINTEF Smart Capacitive Silicon Pressure Sensor, demonstrating the power of combination of features. [9.3] This sensor is using many of the listed features. It has a micromachined diaphragm made by batch processing, as shown in the detail photograph of the diaphragm chip. It uses the variable air gap capacitive sensing principle, has integrated electronics and is assembled by silicon-to-silicon anodic bonding. (Photo: Jan D. Martens, SINTEF)

Micromachined device technology is a part of the microelectronics field. World-wide, microelectronics is recognised as a basic technology commanding the

performance and market success of both present and future electronics systems. These are systems that constitute one of the most important key factors determining the effectiveness and competitiveness of most business fields and public administration services. Microelectronics has and will dramatically improve performance both in a revolutionary and an evolutionary way, and this is giving corresponding impacts in those areas using electronics systems based upon microelectronics.

However, the field of micromachined devices is having a much slower development in performance increase, cost improvements and market impact compared to other fields of microelectronics [9.4], [9.5] There are many bottlenecks slowing this development. These trends have motivated us to suggest the following list:

The bottom ten list of inhibiting factors

1. Slow market acceptance. Micromachined devices are not well known in the market, and users are hesitant to use products with a very short track record.

2. Low production volumes. With a few exemptions, most products are produced in low production volumes, giving high cost and low market penetration.

3. Immature industrial infrastructure. Most of the industry is still very young and very fragmented both from a geographical and technological point of view. Strong industrial clusters as we know from other industry, e.g., like Silicon Valley in microelectronics, have not yet been established

4. Poor reliability. Complex products and processed produced in low volumes for a relative short time can give questionable reliability.

5. Complex designs and processes optimised for performance, not cost. Sophisticated designs and high complexity of the production process for most of the devices call for large development and manufacturing resources, and long lead times from the idea to successful commercial production.

6. Immature processing technology. Most often, many individual device process steps with an early transition from batch processing are used giving yield problems and high cost.

7. Immature packaging and interconnection technologies. Interfacing of the device with the medium it senses or actuates on is most often difficult and expensive, since several individual device packaging fabrication steps are needed.

8. Limited research resources. The industry is still small with limited commercial success. Therefore, research resources, both financial and technological, are limiting the progress of the technology.

9. Limited human resources. The industry has only a limited number of seasoned first-class experts, and the education system has with only a few exemptions yet to recognise to full extent the need to train students in the field of micromachined devices.

10. High cost. Generally, as a consequence of inhibiting factors as those mentioned above, the industry is generally still manufacturing high-cost products. This gives a negative feedback to those same factors, e.g., slows down the market acceptance of the products.

The performance versus cost is a key issue for success in the market for micromachined devices. With competitive performance versus cost ratio, micromachined devices will both replace traditional sensors and open up new applications such as microactuators. Batch processing of micromachined devices used the right way has a strong effect in this respect. At some stage in the production, batch processing is taken over by individual processing such as packaging. The rule of the thumb is that cost per device is very low until individual device processing starts. A good way to visualise this is the price level of commodity integrated circuits, where advanced batch processing technology is driving the cost per transistor into the nano-ECU range [9.4], [9.5], and [9.6]. The most aggressively priced micromachined devices such as airbag crash sensors have price targets less than 10 ECU, [9.7], indicating that the batch processing costs are only a few percents of the total production costs.

Extensive and appropriate batch processing methods are very important for successful industrial innovation of micromachined devices. SensoNor, a Norwegian silicon micromachined sensor producer, is focusing on silicon batch processes as their competitive edge. [9.8] They have an annual production of several millions silicon accelerometers used as crash sensors in automotive airbag systems.

Therefore efforts should be made to develop devices that to a larger extent than today is made by batch processing instead of individual device processes. In this review, the most important batch processing technologies appropriate for micromachined devices are presented, together with some examples and recommendations for future work in this area. We have divided these batch processes into 4 groups:

- Batch processes adapted from microelectronics/IC technology with no or minor modifications.
- Batch processes modified from microelectronics/IC technology processes.
- Batch processes adapted or modified from other technologies than microelectronics/IC technology
- Batch processes mainly developed for micromachined devices

These groups will be described in more detail in the following chapters.

9.3. BATCH PROCESSES ADAPTED FROM MICROELECTRONICS/IC TECHNOLOGY WITH NO OR MINOR MODIFICATIONS

As earlier pointed out, manufacturing methods from microelectronics, primarily developed for silicon integrated circuit manufacturing, are very important

cornerstones for the micromachined device technology. They are well developed, commercial processing equipment is available at modest prices, and they have the important feature of batch processing, all ending up in high-quality, cost-effective ways of manufacturing micromachined devices.

We will mention some of these methods and discuss their versatility for micromachined device manufacturing. Their technological fundamentals are rather complex; therefore this overview has to be rather summarising, giving no room for in-depth explanations and analyses. We refer to textbooks [9.9], [9.10], and [9.11] for a more comprehensive overview.

Photolithography

Photolithography in IC manufacturing, is the art of photoengraving, which means the process of transferring geometric shapes on a mask to the surface of the semiconductor wafer so that all its surface is protected except where following processes such as etching, implantation or diffusion will take place.

By means of photo artwork a geometric pattern giving the mask openings are transferred from a hand-crafted or computer-aided-designed large-scale layout to the desired pattern on a mask. These steps are most of them very critical calling for high-precision and ultra clean processing until the mask is ready for use. Errors like stepping mismatch or dust contamination must be minimised, as mask errors are copied down on the wafers giving device problems and failures. The mask is usually a right-sized and repeated pattern for use in contact/proximity aligners, or a single enlarged pattern as a reticle that is stepped during registration with a projection aligner.

Pattern is transferred to the wafer by photo registration on the photoresist layer on the wafer that is deposited before registration by spin coated and further processed by selective removal of patterned area. The resulting openings of the developed photoresist are then subject to further processing like etching of the surface oxide or thin film metallisation, and afterwards the remaining hardened photoresist is removed.

A silicon micromachined pressure sensor is an example on how photolithography is used to manufacture micromachined device. Photolithography is used to make an etch opening in the surface oxide for anisotropic etching of the diaphragm.

Spin coating

Spin coating is primarily used for photoresist deposition in photolithography, but has also proved itself as a versatile technique for different polymer and glass coatings, with the material to be deposited spin coated in a low viscosity form,

e.g., polyimide in its monomer form imide or glass particles, both in solvents to tailor the appropriate viscosity.

Etching techniques

Etching techniques are used in combination with photolithography and other processing techniques to give patterned geometrical and electronic features of the processed device.

Wet etching techniques are mostly based upon organic solutions tailored for photoresist removal and acid or alkali solutions for etching off surface films such as oxides, nitrides and metal films. For photoresist, a selective resist removal of exposed/not exposed photoresist is used, at first to remove the resist in the patterned areas for subsequent processing, then after appropriate processing of patterned areas to strip off the remaining hardened resist from the unpatterned areas. The wet etching techniques of micromachining originated from silicon IC processing.

Dry etching techniques have gained popularity the recent years, both because they for some applications have added features, but also because of cost advantages and environmental issues. Physical etching techniques by sputter etching or ion milling are used to some extent, but combined physical and chemical plasma techniques are most popular. Reactive plasma etching is the most used technique for hardened resist removal. Physical/chemical plasma etching is also much used - e.g., RIE (Reactive Ion Etching) has high flexibility in etching selectivity and is to some extent anisotropic. RIE is extensively used for etching polycrystalline silicon films, e.g., for surface micromachined motor processing.

Diffusion of dopants

The thermal diffusion technique as a way of introducing electrical active impurities in a controlled way into silicon is the most important way to alter the electrical characteristics of silicon and other semiconductors. Impurity levels in the range of one/tenth of a percentage and down to parts per million are used to alter the resistivity and type of main conduction mechanism (p-type or n-type) giving the possibility to make resistors, transistors, etc.

Diffusion of impurities takes place in diffusion ovens, operating in the range from approximately 800°C to 1200 °C with tight temperature regulation and gas as impurity source.

Implantation

The implantation technique is an alternative way of introducing dopants into a semiconductor. This is done by accelerating the desired impurity ions to high energies and focus them at the semiconductor surface. To cover the whole surface, the ion beam is scanned, and in this way ions enter the semiconductor wafer wherever it is not protected by a mask that can withstand the high energy of the ions. The characteristics of an implantation process are dependent upon type of ionised dopant, ion energy and ion dose per area. The ion energy can be several hundred KeV and the impact creates excessive damage of the substrate material, calling for an annealing step after implantation. This is a heat treatment

where the crystal heals itself of the damage and the implanted ions move into substitutional lattice positions and become electrical active.

Ion implantation is often followed by a diffusion step to get the wanted impurity profile going deeper than the few parts of a micron normally achieved by implantation. In this way ion implantation is used as a predeposition technique, using its high dose accuracy to improve the accuracy of the doping. E.g., ion implanted resistors have a resistance value accuracy down to one per cent with excellent matching, and this is many times better than what is achievable with the thermal diffusion technique, and making ion implantation of boron in silicon the dominating way of making piezoresistive micromachined sensors.

SIMOX (Separation by IMplanted OXygen) is a fascinating specialised implantation process applicable for micromachined devices. [9.12] With this technique, a buried dielectric SiO_2 layer is made by O_2 implantation and subsequent annealing. The dielectric layer can be used for component isolation and/or selective etch stop for micromachined devices.

Epitaxy

Epitaxy is used to grow a single crystal (semiconductor) layer of controlled thickness, composition and doping on top of a single crystal (semiconductor) substrate in such a way that the crystal structure of the substrate is extended unperturbed into the epitaxial layer.

Epitaxial growth is done when semiconductor atoms from vapour or liquid phase are deposited on a hot substrate. In order to obtain single crystal growth, an almost perfect match of lattice constants is necessary, otherwise polycrystallinity will result.

Silicon-on-silicon epitaxy is used extensively in silicon micromachined device manufacturing. E.g., a selective etch stopping layer for a silicon micromachined pressure sensor is obtained by first doping the substrate with boron at high concentration, then growing an epitaxial silicon layer with phosphorus doping (n-type) defining the diaphragm thickness and giving a substrate layer for the boron doped piezoresistors. Silicon epitaxy is done in the temperature range from 950°C to 1250°C using for instance silane (SiH_4) as vapour source.

Recently molecular beam epitaxy (MBE) has been given much attention from the semiconductor scientific community as a way of making new electronic devices by bombarding a substrate with evaporated material to be deposited. In this way ultra thin single crystal layers with specific doping and electrical characteristics can be tailored. Such structures could also have several applications in micromachined devices, but much basic research needs to be done before this is feasible.

Chemical vapour deposition (CVD)

This is a process where vapour phase reaction products are deposited on a substrate as a thin film. Contrary to epitaxial films, these films are either polycrystalline or amorphous. For micromachined devices, two kinds of CVD-films are dominant, either polycrystalline silicon film as piezoresistive element or as surface microstructure in surface micromachining, or silicone nitride film as a masking film for anisotropic and selective etching.

Among the different CVD process techniques Low-Pressure CVD (LPCVD) is known to be the best choice in most cases, with advantages such as precise control of composition and structure, and fast deposition rates.

Plasma enhanced CVD - PECVD allows for lower processing temperatures, e.g., silicon nitride deposition around 300°C for PECVD instead of above 700°C for LPCVD. This gives greater flexibility, e.g., deposition after metallisation, with increased pinhole density as the main penalty.

Thin film technology

Thin film technology, or physical vapour deposition (PVD), is a way to deposit solid material on a substrate by vaporising in a vacuum chamber a target material to be deposited by heating (evaporation) or ion bombardment (sputtering). The substrates, when placed in the irradiation field of the vaporised material, will be covered by a uniform polycrystalline or amorphous film of the target material.

In micromachined device processing, PVD is extensively used to deposit dielectric films such as SiO_2 for surface passivation, or deposit metals such as aluminium or gold as electronic interconnection conductors and bonding pads.

Resistive films such as tantalum nitride or chromium-nickel can be used when manufacturing micromachined devices by placing thin film trimming resistors on the chip. These are trimmed by laser to obtain specified performance, e.g., zero balance or normalised sensitivity for micromachined sensors.

One special application of PVD in the micromachined device field is deposition of borosilicate glass ("Pyrex") as a bonding material when two silicon wafers or chips are sealed together.

Thin film hybrid technology is often used in connection with micromachined devices. With this technique, some degree of miniaturised electronics can be achieved without putting it on-chip. With this technology, chips, interconnections between chips and high-accuracy resistors are all placed on a substrate.

Thick film technology

Thick film technology is the technique to make interconnections and electronic components such as resistors and capacitors on a ceramic or insulated steel substrate by means of screen printing technique. This is a versatile way of making cheap and miniaturised electronics for micromachined sensors, e.g. used as trimming network.

9.4 BATCH PROCESSES MODIFIED FROM MICROELECTRONICS/IC TECHNOLOGY PROCESSES

In this category, we have batch processes that are modified versions of microelectronics/IC technology batch processes. This classification should be seen as the intermediate between the above mentioned adapted processes and the later mentioned specialised processes. There are in this classification also a multitude of processes in use and/or being developed. We will in highlight some examples.

Double-sided photolithography

Many micromachined devices need precisely aligned double-sided patterning during the production process, e.g., silicon piezoresistive micromachined pressure sensors have their resistor network processed on one side of the wafer and the micromachined diaphragm processed from the other side. This calls for methods for precise double sided alignment. Mechanical alignment systems ensuring correct x-y positioning by using the circumference of the substrate or wafer as reference is one way to do it, but infrared see-through-wafer aligners are most popular. These aligner are mostly standard aligners with an infrared camera as add-on equipment. At SINTEF we have a Karl Süss MA56 aligner with infrared camera as add-on equipment, and we achieve a side-to-side alignment precision within a few microns.

Standard wafer handling equipment for IC manufacturing are generally made to use the unpatterned backside as attachment side, e.g., attachment to the chuck in spin coaters - with little or no concern for scratches or unwanted deposits on the backside during the process steps. Wafers with double-sided patterning have no backside; therefore equipment and processes must be modified to ensure that both sides of the wafer are properly handled during processing. Somehow, both sides of the wafers must allow for some areas where chuck attachment, manual handling with tweezers, gripping by equipment handling arms, etc., can be done.

Wafer fusion bonding

The wafer fusion bonding process [9.13] is mainly targeted for silicon-on-insulator fabrication of junction isolated integrated circuits with radiation hardened circuits and high-temperature circuits as focused applications. Nevertheless, the method is an already well established batch process technology for silicon micromachined devices. Clearly, process modifications are needed to optimise the process for micromachined devices.

Wafer bonding proceeds via two steps: Mating of the precleaned hydrophilic surfaces of two mirror-grade polished silicon wafers at room temperature and subsequent annealing at elevated temperatures. During the room temperature step, the final position of the wafers is fixed by attractive interactions between the hydrophilic surfaces. At elevated temperatures (between 400°C and 1200°C) condensation and oxidation reactions take place at the adjacent SiO_2 surfaces, which increases the bond strength at the interface.

LIGA and LIGA-like techniques

The LIGA process, which is based on deep etch X-ray lithography, electroplating, and moulding, allows for fabrication of three-dimensional micro structures with high aspect ratios. [9.14], [9.15], [9.16]. LIGA is an acronym abbreviated from the German words LIthographie, GAlvanoformung, ABformung. Its main feature is the ability to make high-precision moulds for micro structures with high aspect ratio that is then used for high volume moulding production, e.g., for plastic parts. The aspect ratio can be as high as 100, e.g., making a structure with width 3 µm and depth 300 µm. Its main drawback is that a synchrotron as X-ray source is needed during the lithographic process. LIGA-like techniques circumvent this drawback by using photolithographics optimised for high aspect ratio instead of X-ray lithographics. [9.17]

Laser micromachining

Laser micromachining can be defined as processes using lasers the remove, deposit or weld materials in microscale. Laser micromachining is now available as commercial subcontractor services. [9.18]

9.5 BATCH PROCESSES ADAPTED OR MODIFIED FROM OTHER TECHNOLOGIES THAN MICROELECTRONICS/IC TECHNOLOGY

Batch processing is in widespread use in many industries, and many of these process technologies can be adapted or modified for manufacture of micromachined devices. Below, we have given two examples:

Micro stereo lithography

Micro stereo lithography can be defined [9.19] as a way to make a 3-D microstructure by using ultraviolet radiation curing polymer, starting from the construction of 2-D sliced thin planes hardened from liquid by UV radiation, which are added to each other as a sequential process resulting in the final 3-d structure. In practice, this is done with a computer controlled set-up of a UV laser and an XYZ alignment system, focusing the laser in the UV curing liquid where hardening into solid state is wanted.

Micro electro discharge machining

Micro electro discharge machining can be defined [9.20] as micromachining of structures by erosion of material by means of a controlled electric discharge between an electrode and the material. Aspect ratio can be up to 5, with typical width down towards a few tens of micrometers.

9.6 BATCH PROCESSES MAINLY DEVELOPED FOR MICROMACHINED DEVICES

In this category, we have batch processes that are specialised processes for micromachined devices. These processes were developed mainly for micromachined device processing, even though it is easy to see their principal resemblance with microelectronics/IC technology batch processing methods. Some of them are developed from earlier microelectronics/IC technology batch

processing methods, but the main development work has been done by the community of micromachined devices. We will here highlight some examples.

Bulk micromachining

Bulk micromachining can be defined as three-dimensional micromachining in a bulk material by means of photolithographic etching techniques. This definition covers most bulk techniques used to make micromachined devices, although in some cases mechanical drilling or other machining methods are used. Bulk micromachining in single crystal silicon based on wet chemical etching is the dominating technique, and the way it is done illustrates the concept of in a very informative way. The most popular materials for bulk micromachining in addition to single crystal silicon are glass, quartz and gallium arsenide.

The etching techniques used in bulk micromachining of silicon are most often wet chemical etching, some isotropic and some anisotropic attacking the different crystal direction with different speed. By impurity doping selective etching can be obtained with etching speed dependent upon doping configuration. The anisotropic etching technique is the dominating, as this method, especially when combined with selective etching behaviour, gives the highest dimensional accuracy and repeatability with an accuracy down towards 1μmeter. High accuracy is crucial as this opens up for miniaturisation giving performance and cost improvements for products based on this technology.

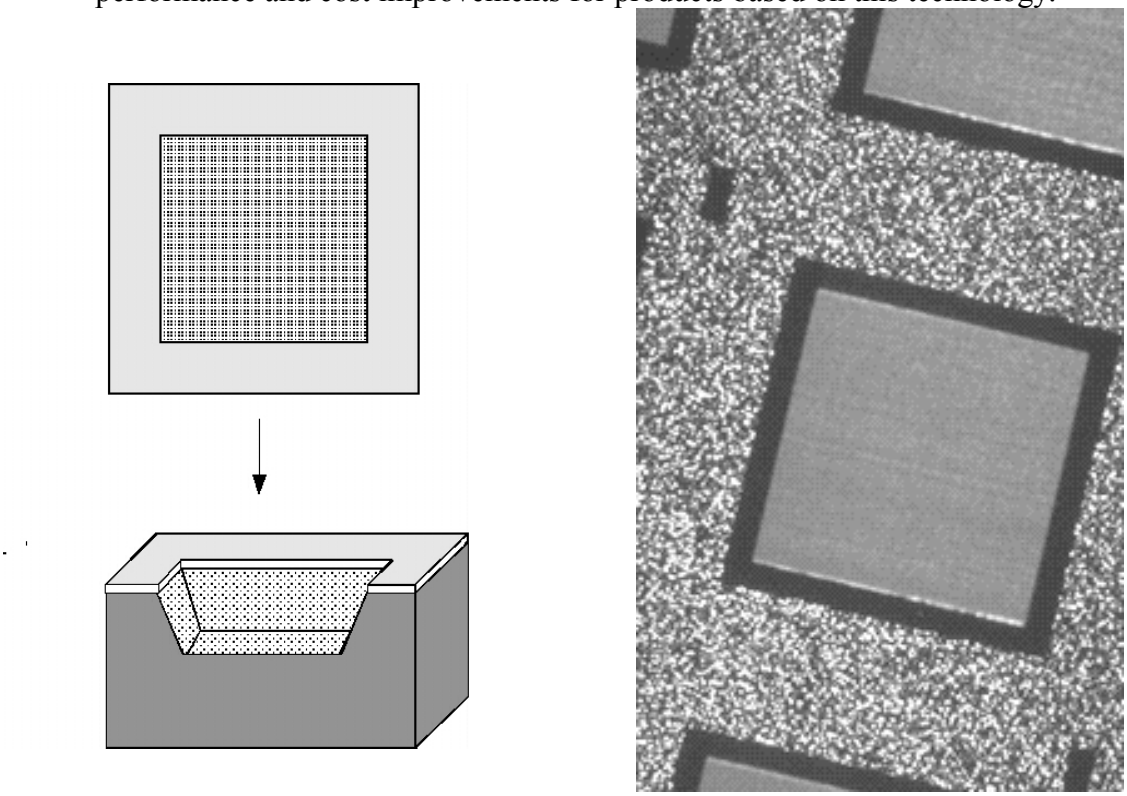


Fig. 9.9: Anisotropic etch cavity in (100) silicon with a square masking film opening oriented in parallel with the direction. Due to the four-fold symmetry of the slow-etching (111) planes, sideways etching is stopped giving a cavity with four sloped side walls. The photography shows such an etched cavity.

Surface micromachining

Surface micromachining [9.21] can be defined as a set of methods to make three-dimensional surface structures, with deposition of thin films as additive technique and selective etching of the thin films as subtractive technique. The thin film system usually consists of a structural layer on top of a sacrificial layer. The sacrificial layer facilitates highly underetched or free-standing patterns of the structural layer.

In practice, single crystal silicon wafer is the dominant substrate material, while chemical vapour deposited (CVD) polysilicon and silicon nitride are most used as the structural layers making up the three-dimensional surface structures on top of a sacrificial layer of silicon dioxide.

A main advantage of surface micromachining, compared to bulk micromachining, is that it does not need double sided processing of the wafers to make three-dimensional structures.

The main additive deposition techniques are evaporation, sputtering, chemical vapour deposition (CVD), and variants of these. The main subtractive methods are selective wet etching and dry plasma etching. Photolithography is used for pattern definition.

The use of sacrificial layers is an important part of surface micromachining. With these methods, etching of the sacrificial layers underneath non-etched thin film structures can be done. In this way several three-dimensional surface structures can be made, such as cavities, supported microbeams, microstrings, diaphragms, lateral mobile microelements, etc.

Anodic wafer bonding

Anodic wafer bonding is based upon the anodic bonding sealing process that can be defined as a method of electrostatically bonding two dissimilar materials together to form a strong, hermetic seal that involves little alteration in the shape, size, and dimensions of the members making up the joint. It is a high yield wafer-to-wafer sealing method that makes it possible to obtain hermetic seals. The technique was first developed for silicon-to-glass anodic wafer bonding, and has later been further developed to silicon-to-silicon anodic wafer bonding and silicon-to-thin film anodic wafer bonding.

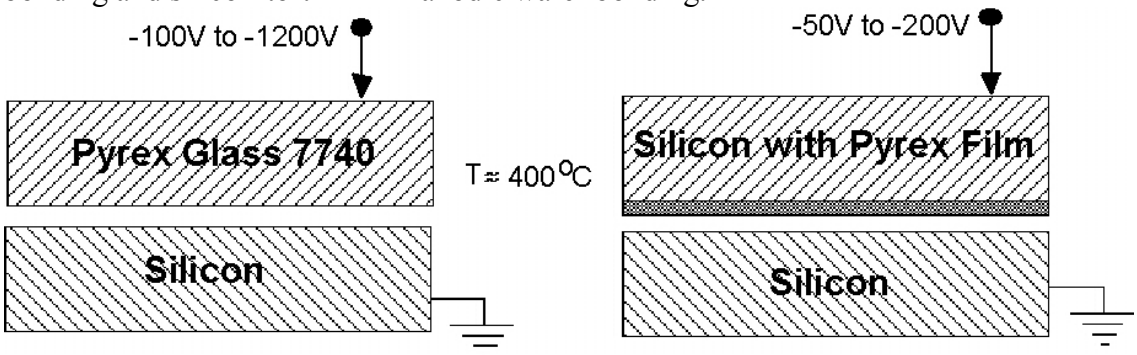


Fig. 9.10: Schematic view of silicon-to-silicon anodic bonding and silicon-to-glass anodic bonding.

The method is further visualised in the below given example from SINTEF.

9.7 HIGHLIGHT EXAMPLE: SINTEF`S SILICON-TO-SILICON ANODIC WAFER BONDING PROCESS

SINTEF have developed a silicon-to-silicon anodic wafer bonding process with high potential of application within both sensor and actuator applications [9.22], [9.23], [9.24], [9.25], [9.26], [9.27], [9.28]. The method was first implemented on chip level, but was later further developed for wafer bonding, making it a batch process.

By choosing proper materials the bonding adds only a small amount of mechanical stress in the structure. This motivated us to develop a silicon-to-silicon anodic bonding for silicon micromachined pressure sensors.

The method is using a sputtered borosilicate glass as a thin film layer on one of the silicon surfaces. The silicon-to-silicon anodic bonding process is similar to the silicon-to-glass process with a few exceptions. Due to the thinner glass layer, the electric field required to drift the mobile ions in the glass can in general be obtained at a lower voltage. Nevertheless, the sputtered glass film will most often suffer from dielectric breakdown unless a dielectric with better isolation properties is deposited on the wafers before sputtering the glass layer.

Sputtered glass films can be used not only as a sealing material, but also as a combined spacer and sealing material. Pattern definition in the glass is best done by gold masking and etching in HF. To avoid etching of the underlying dielectric and thereby dielectric breakdown during bonding, Si_3N_4 could be used as dielectric (Figure 9.11).

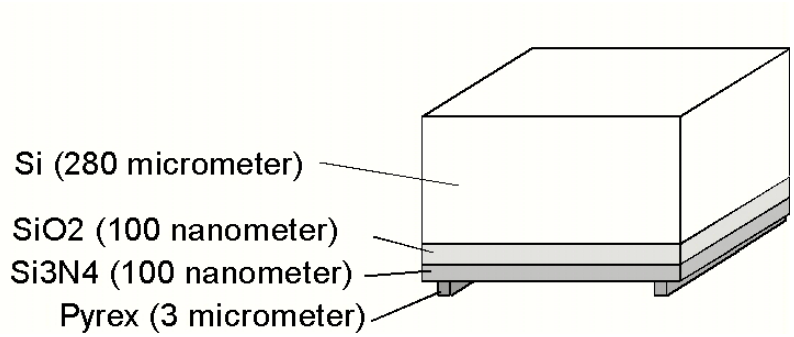


Fig. 9.11: Silicon chip with deposited thin films. The Pyrex is pattern defined by photolithography.

A process with the following parameters is developed:

- Growing (thermal oxidation) a thin layer of approximately 100-500 nm of SiO_2 to obtain the needed dielectric strength during the electrostatic sealing.
- Depositing (LPCVD) a thin layer of approximately 100 nm of Si_3N_4 to increase photolithographic selectivity for later pattern definition of the sputtered glass film.

- Using 1-5 µm sputter-deposited Pyrex #7740® borosilicate glass as sealing and spacer material between the silicon wafers to be bonded.
- Sealing wafers together by anodic bonding at approximately 400°C with an electrostatic voltage of 50 - 200 VDC with the negative electrode connected to the sputter-coated wafer. The voltage should be applied for a time period long enough to allow the current to settle at steady state leakage current to complete the bonding process, typically 10 minutes for a set of 3 inch wafers.

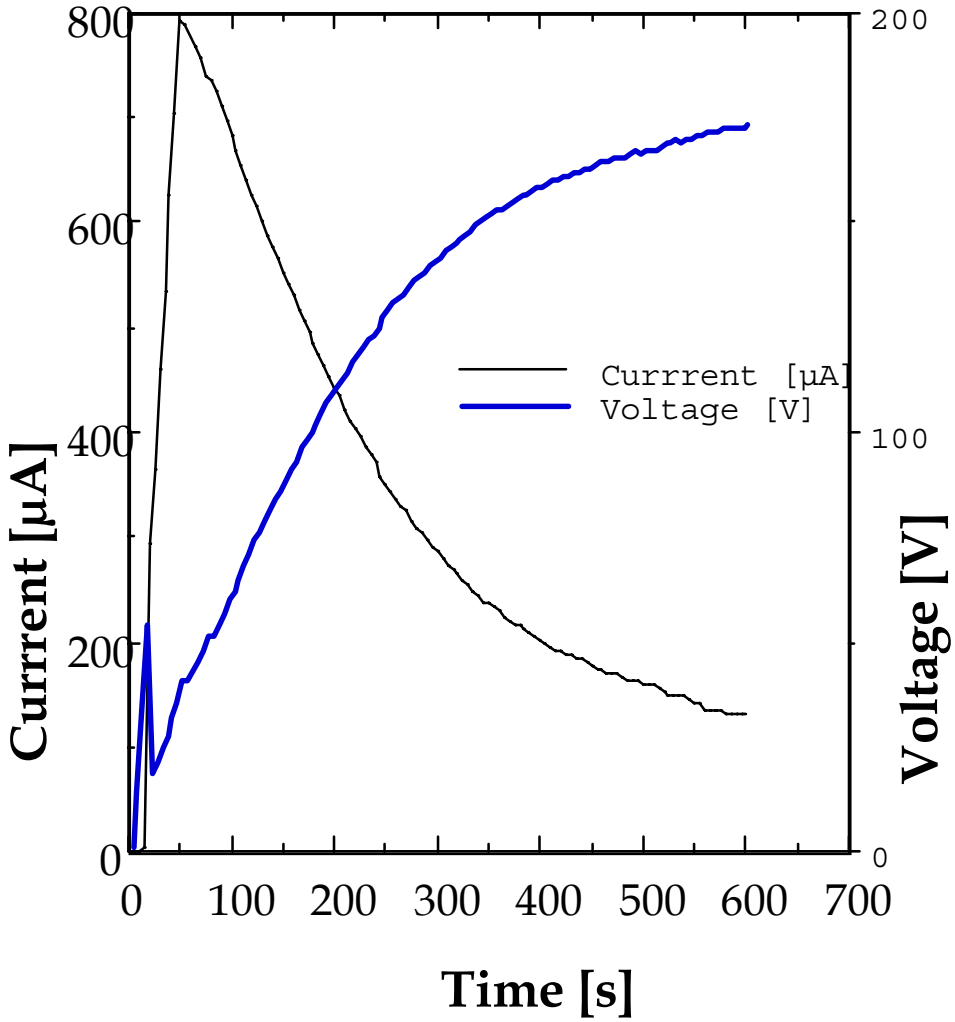


Fig. 9.12: A typical current/voltage versus time relationship during the anodic bonding of two 3 inch wafers.

A typical current/voltage versus time relationship during the anodic bonding of two 3 inch wafers is shown in Figure 9.12.

A crucial parameter for the bonding process is the ratio between bonded and not bonded areas giving the yield of the process. This parameter is dependent of the cleanliness of the wafers and the glass film quality. Poor film quality may cause dielectric breakdown during the bonding process, and unclean areas will not be bonded.

To obtain successful seals, the sealing surfaces should be polished, and utmost care should be taken to avoid particle contamination - proper cleaning

procedures and clean room environments (e.g. Class 100) are mandatory to avoid low yield.

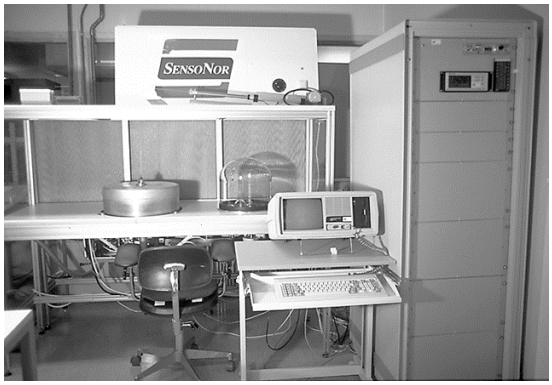


Fig. 9.13: The SensoNor/SINTEF Anodic Bonder. This equipment has a computer controlled bonding chuck for silicon wafers, facilitating flexible set up of bonding temperature and bonding voltage versus time with ramping. The equipment is built inside a flow box to avoid particle contamination. (Photograph courtesy of SensoNor, Horten, Norway)

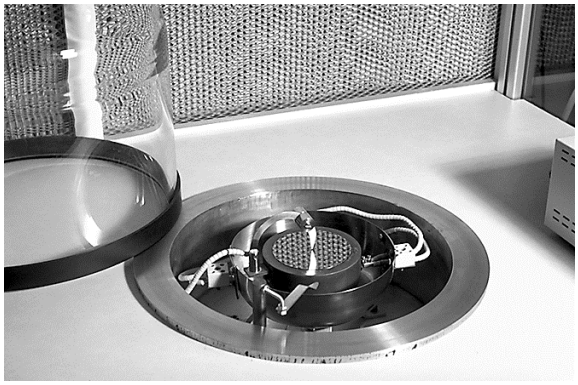


Fig. 9.14: Detail view of the bonding chuck of the SensoNor/SINTEF Anodic Bonder. The chuck is placed inside an air tight chamber to ensure controlled gas environment during bonding, e.g., vacuum or inert gas. (Photograph courtesy of SensoNor, Horten, Norway)

To our knowledge, this batch process is not yet been implemented in full scale commercial use even though the method clearly has advantageous features and has been extensively reported to the international scientific community. This visualises that industrialisation of specialised batch processes for micromachined devices indeed is a difficult task.

9.8 COMPANY PROFILE: SENSONOR IS FOCUSING ON APPLICATION SPECIFIC SENSORS

SensoNor A.S is an independent company operating as an OEM-supplier located in Horten, Norway. The business idea is to develop, manufacture and market microsensors, preferably for high volume applications, based on silicon

micromechanics technology. The company has a range of some standard products and offers application specific sensors such for mechanical quantities such as pressure and accelerometers. Over the past 30 years SensoNor has been in the technological forefront to offer microelectromechanical systems (MEMS) solutions to customers. Over these years a broad technological base has been built up. SensoNor has been able to service the demanding task of introducing MEMS solutions to replace traditional sensors in the filed of avionics and precision metrology. Even more so, significant advances have been made in high volume applications such as automotive and medicine. SensoNor is today the world's largest independent manufacturer of crash sensors for automotive applications and a leading supplier of sensors for medical applications.

By 1995 SensoNor employs approximately 300 people, out of which 60 are university graduates including engineers. The company possesses 3 production plants with a total floor space of 8000 square meters. The production lines are built by using a high degree of automation in order to meet customers' expectations for low cost and high reliability. Carefully developed control-plans are utilised to safeguard the production.

SensoNor commits 100% to OEM partners in the challenge to solve application specific need in an optimum way. With a complete authority in both development and manufacturing a focus on the goals with respect to Application Specific Integrated Sensors (ASIS) is given.

Concurrent engineering principles are used in the development of new products. SensoNor's strategy is to complete the development cycle within 2,5 years from the sensor concept is defined until volume shipment takes place. To be able to achieve this goal, parallel exercise of the various engineering disciplines in a given project is a must. This parallel performance is systemised in our engineering approach.

It is of great importance to be self contained when it comes to specialist and tools. The technology group is focused in the core areas of semiconductor processes, 3-D structuring and wafer lamination. A second group is focused in the area of die- and wire-bonding, transfer- and injection-moulding, electroplating as well as trim, form and test. A third group is concentrating on the issues of communicating with the customers and constructing the right type of device for the particular application. As part of the production departments, special engineering groups are focused on specifying and building automatic production lines.

The most advance tools, such as field emission scanning electron microscope, acoustic microscope and chemical element analyses are available to designers and analysts. To be able to optimise designs and to shorten product development time, modelling tools are our daily working environment. They include tools like non-linear FEM and advanced semiconductor process and device modelling. Environmental testing, and "overstressing" play an important role in prototype evaluations. For this purpose there is an in-house laboratory with a range of equipment including combined vibration/temperature testing, autoclaving as well as temperature shock testing.

To further strengthen the engineering position, SensoNor has developed strategic alliances with long term partners within supporting fields, such as basic research, special process development, ASIC design, etc.

SensoNor is self-contained with their own local wafer-FAB and therefore has no need of shopping processing on the market, making the cost structure, delivery security and quality control predictable and reliable. SensoNor has the strategy to develop in house purpose built automatic assembly- and test lines. By doing so, advantage can be taken of applying the right customised packaging concept for a given sensor design. For the purpose of effectiveness in communication there is a short link between engineering support and the production. The company has adopted a Total Quality Management, TQM philosophy, and several quality approvals including ISO 9001 are being granted during 1995.

An example of an application specific integrated sensor from SensoNor is the third generation crash sensor SA30. This accelerometer is optimised to be a low cost crash sensor for airbag systems, with versions for frontal impacts and side impacts. SA30 is a two chip solution with the sensor on one chip and signal conditioning on another chip, packed in a small outline package for surface mount. Mounting on PCB can be normal or horizontal with respect to the sensitive direction. SA30 is completely self-contained with no need for any additional components or trimming.

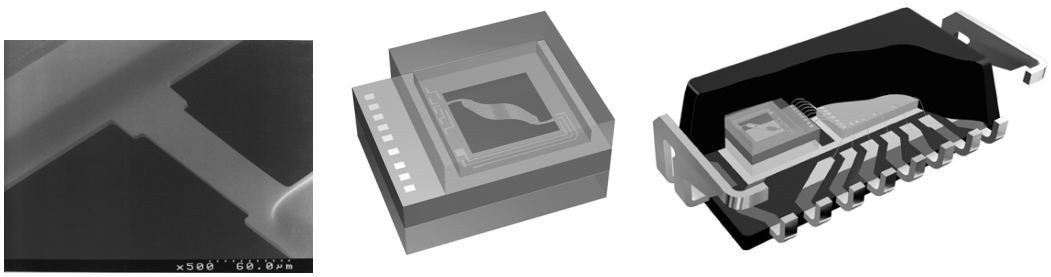


Fig. 9.15: The silicon micromachined resonator beam, the chip set and exploded view of the assembled transfer moulded packaged SA30 Crash Sensor.

The output signal can be either PWM (Pulse-Width-Modulated) for innovative system designs, with respect to noise, EMI or A/D conversion, or analog (ratiometric) for traditional interfacing. A threshold signal is available for designers to improve the system reliability and performance. Due to the intrinsic continuous self-test of the sensor, monitoring of a status signal is all that is needed to check the reliability of the sensor signal. This solution makes it possible to check the sensor at all times, even during a crash without interrupts and loss of information. SA30 utilises a small single crystal silicon resonator, which shifts its frequency due to change in acceleration. The innovative concept for self-test has been made possible due to the development of a new sensing principle. Since all parts of the resonator (both "springs" and "mass") are in flexure during operation, the consistency of the function can be monitored continuously. For additional information see ref. [9.29]:

9.9 SOME GENERAL RECOMMENDATIONS FOR FURTHER WORK WITH BATCH PROCESSES FOR MICROMACHINED DEVICES

- The transition from batch processing to individual device process steps should be done late in the process flow. Individual device process steps should be scrutinised to be replaced by batch processing or modified to batch processing to increase performance and/or reduce costs.

In practice, wafer dicing is a the critical process step; from then cost-effective, high quality batch processing is difficult or impossible. This bottleneck for industrial innovation of micromechanical devices is a main challenge for this industry. The pioneering costs are extensive, but success here will increase the competitive edge of the individual company and the whole industry. This aspect should therefore be given more attention by the scientific community.

- Updated transfer of suitable state-of-the-art batch processing technologies from microelectronics/IC technology to reach competitive performance versus cost ratio. It is important to stress that the development/pioneering costs of these methods will and should as often as possible be taken by players outside the micromachined device industry. In this way advanced, but mature technologies can be put to work with low costs.

Examples of typical candidates in this category are general IC processing technologies such as photolithographics, diffusion techniques and thin film deposition techniques. SIMOX is an example of a feasible technology that is questionable to put in this category - this technology is clearly driven by IC industry for SOI circuits, but major modifications might be needed for micromachined device applications.

- Development of general batch processing technologies for micromachined devices not readily available from the microelectronics industry that are easy to re-engineer by competitors. The main justification of these methods is to increase the competitiveness of the whole industry, and generally, the costs of such developments are very high. We recommend therefore that these technologies mostly are developed as collaborations in the industry, e.g., collaborative projects sponsored by EU.

Examples of typical candidates in this category are micromachining processing methods and wafer-to-wafer bonding techniques.

- Development of specialised batch processing technologies for micromachined devices that are product specific and difficult to copy by re-engineering. These methods are critical to give the company a competitive edge in the market. We recommend that such processes are aggressively sought for, carefully scrutinised to assure the development costs are justified and can be financed, and carefully protected by stringent confidentiality measures and/or legal actions such as patenting.

Examples of typical candidates in this category are product designs and individual specialised process steps tailored to improve the performance or reduce the cost of the specific product, e.g. replacing individual device filling of

silicone oil for vibration damping with batch-processable air damping systems in micromachined accelerometers.

- New designs should be made as simple as possible from a manufacturing point of view. This means that the numbers of needed processing steps are minimised and allowed process variations are generous. In this way efficient, high yield fabrication can be made at low cost. Designs should be based upon design rules established to facilitate such production, instead of first doing a design optimised for technical features and then establish the needed manufacturing processes.

A lot of fascinating micromechanical devices have been developed and reported. However, very few have succeeded as industrial innovations. One important reason is their very sophisticated designs calling for very complex manufacturing technology. Some smart sensor designs are clearly in this category even though they in principle are extensively based upon batch processing. Often, a hybrid approach is much better from a commercial point of view.

- Improved batch organised packaging technologies should be developed.

The main costs for micromachined devices are generally packaging, mainly since batch organised processing at this stage is difficult or impossible. The needed micro assembly techniques are in general rather immature, giving high cost and poor reliability. New techniques need to be developed, adapted or improved by multidisciplinary teams able to handle the different aspects of packaging technology for micromachined devices.

9.10 CONCLUSIONS

This overview shows that the field of micromachined devices is a very strong and growing industrial fields with a strong market pull from a multitude of applications in different fields and a strong technology push from advanced production technologies, with batch organised process technologies, mainly adapted or modified from corresponding technologies used for silicon integrated circuits. In addition, some specialised processes have been developed for the field.

Batch processing is a key success factor to increase the performance and reduce the costs of micromachined devices. Appropriate batch processes should therefore be used to a larger extent than today to avoid the high cost of individual processing. New devices should be designed and existing devices modified to fulfil this goal. Excellent and suitable batch processes can and should be transferred with no or minor modifications at relative low cost from microelectronics/IC technology. There is an increased use of specialised batch processes for micromachined devices, with micromachining etching processes and wafer-to-wafer bonding as distinct examples. The micromachined device industry should collaborate on the development of generic batch processes to increase the competitiveness of the whole industry, while each company should

strengthen their individual competitive edge by developing and implement critical product-specific batch processes.

REFERENCES

[9.1] Per Ohlckers & al: "State of the Art of Silicon Sensor Technology" Proceedings of the 2nd Nordic Space Science Technology Workshop. Storefjell, Norway. Oslo, November 23-25, 1992.

[9.2] S. Middelhoek: "Quo vadis silicon sensors?" Sensors & Actuators, 8, 1985, pp. 39-48.

[9.3] A. Hanneborg, T.E. Hansen, P.A. Ohlckers, E. Carlson, B. Dahl and O. Holwech: "An Integrated Capacitive pressure Sensor with Frequency-modulated Output" Sensors and Actuators, 9 (1986) pp. 345-351.

[9.4] S. Middelhoek and A. C. Hoogerwerf: "Smart Sensors: When and Where" Sensors & Actuators A, 41-42, 1994, pp. 1-8.

[9.5] J. E. Brignell: "Quo vadis smart sensors?" Sensors & Actuators A, 37-38, 1993, pp. 6-8.

[9.6] Wojciech Maly: "Growth of Silicon Cost and Resulting Changes in Manufacturing Paradigms", Semiconductor International, No. 6, June 1994, pp. 158-164.

[9.7] Frank Goodenough: "Airbags Boom when IC Accelerometer Sees 50 g" Electronic Design, Volume 39, No. 15, August 8, 1991, pp.45-56.

[9.8] "Micromachined Sensors. The European Source" Brochure from SensoNor, May 1991.

[9.9] Gary E. McGuire (editor): "Semiconductor Materials and Process Technology Handbook" Noyes publications, New Jersey, USA, 1988. ISBN 0-8155-1150-7.

[9.10] R. A. Levy (editor): "Microelectronic Materials and Processes" NATO ASI Series E: Applied Sciences - Vol. 164. Kluwer Academic Publishers, Dordrecht, The Netherlands, 1989. ISBN 0-7923-0147-1.

[9.11] S. M. Sze (editor): "VLSI Technology" McGraw-Hill Book Company, New York, USA, 1983. ISBN 0-07-062686-3.

[9.12] B. Diem, R. Truche, S. Viollet-Boson and G. Delapierre: "SIMOX (Separation by Ion Implantation of Oxygen): A Technology for High-temperature Silicon Sensors" Sensors & Actuators A 21-23, 1990, pp. 1003-1006.

[9.13] Christine Harendt, Wolfgang Appel, Heinz-Gerd Graf, Bernd Höfflinger and Elizabeth Penteker: "Wafer fusion bonding and its application to silicon-on-insulator fabrication", Journal of Micromechanical Engineering, 1 (1991) pp. 145-151.

[9.14] E. W. Becker, W. Ehrfeld, P. Hagmann, A. Maner, D. Munchmeyer: Fabrication of microstructures with high aspect ratio and great structural heights by synchrotron radiation, lithography, galvanoforming and plastic molding (LIGA Process)" Microelectron Eng. 4, 1986, pp. 35-56.

[9.15] W.K. Schomburg, D. Maas, W. Bacher, B. Büstgens, J. Fahrenberg, W. Menz, D. Seidel: "Assembly for Micromechanics and LIGA" Workshop Digest, Micro Mechanics Europe 1994, Pisa, Italy, September 5-6, 1994. pp. 17-27.

[9.16] P. Dario, M.C. Carrozza, N. Croce, M.C. Montesi, M. Cocco: "Non-traditional Technologies for Microfabrication" Workshop Digest, Micro Mechanics Europe 1994, Pisa, Italy, September 5-6, 1994. pp. 86-98.

[9.17] J. Gobet, F. Cardot, F. Rudolf: "Electrodeposition of 3D microstructures on silicon", Journal of Micromechanical Engineering, 3 (1993) pp. 123-130.

[9.18] Advertisement from Resonetics in Solid State Technology, Volume 37, No.5, May 1994, page 7.

[9.19] K. Ikuta, K. Hirowatari: "Real three dimensional micro fabrication using stereo lithography and metal moulding" Proceedings of MEMS 1994, Kanagawa, Japan, January 25-28, 1994, pp. 1-6.

[9.20] T. Masaki, K. Kawata, T. Masuzawa: Micro electro-discharge machining and its applications" Proc. of MEMS 1990, Napa Valley, California, USA, February 11-14, 1990, pp. 21-26.

[9.21] C. Linder, L. Paratte, M.-A. Grétillat, V.P. Jaecklin and N. F. de Rooij: "Surface Micromachining" Proceedings of the MICROMECHANICS EUROPE 1992, Leuven, Belgium, June 1-2, 1992.

[9.22] A. Hanneborg and P. Ohlckers: “Silicon-to-Silicon Bonding Using Sputtered Borosilicate Glass” Proceedings, MICRO MECHANICS EUROPE 1990, Berlin, 26-27 Nov. 1990.

[9.23] Anders Hanneborg, Martin Nese and Per Ohlckers: "Silicon-to-Silicon Anodic Bonding " Journal of Micromechanical Engineering, 1 (1991) pp. 139-144.

[9.24] Per Ohlckers and Anders Hanneborg: "Silicon-to-Silicon Anodic Bonding " Proc of the 14th Nordic Semiconductor Meeting, Århus, June 1990.

[9.25] Anders Hanneborg: “Silicon Wafer Bonding Techniques for Assembly of Micromechanical Elements” (Invited speaker) Proceedings of the MEMS 1991, Nara, Japan, January 1991.

[9.26] Reidar Holm, Terje Kvisteroy, Henrik Jakobsen, Anders Hanneborg and Per Ohlckers: "Stability and Common Mode Sensitivity of Piezoresistive Silicon Pressure Sensors Made by Different Mounting Methods" Proc. of Transducers ´91, June 1991, San Francisco, USA.

[9.27] A. Hanneborg, M. Nese, H. Jakobsen and R. Holm: "Silicon-to-Thin Film Bonding", Proceedings from MicroMechanics Europe (MME) 1992, Leuven, Belgium, June 1-2, 1992. J. of Micromechanics and Microengineering, 2 (1992), pp. 117-121.

[9.28] Per Ohlckers, Anders Hanneborg and Martin Nese: "Batch Processing for Micromachined Devices" Invited paper, Technical Digest of the MME `94, Micromechanics Europe 1994, Pisa, September 5-6, pp 2-16. Appeared in Journal of Micromechanics and Microengineering 5(1995) pp. 47-56.

[9.29] Data sheet: SA30 Crash Sensor; SensoNor A.S, P.O.Box 196, N-3192 Horten, Norway.

ELECTRONIC COMPONENTS, PACKAGING AND PRODUCTION

Leif Halbo and Per Ohlckers

The book is primarily meant for university education in introductory electronic packaging technology. An overview is given, that encompasses aspects of material technology, metallurgy, chemistry, physical properties, and mechanical properties. An understanding of the interplay of all these basic fields is necessary for choosing and using the available packaging technologies optimally, making a good design that can result in a product with the right quality. Component technologies are described, basic processing methods, printed wiring boards, design guidelines, the production of printed circuit boards and the common hybrid technologies, including multichip modules.

The book is based on a course presented at the University of Oslo over the last 6 years. It is written with financial support from the European COMETT program, as part of the project COMETT INSIGHT.

The first edition was published in 1993. The most important change in this revised edition from 1995 is an additional chapter on micromachined devices. (Chapter 9) The other chapters have only minor changes.

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