Ultra-low power electronics for energy harvesting node

by

Tra Nguyen Phan

Thesis submitted for the degree of
Master of Science

Department of Micro and Nano Systems Technology, IMST
Buskerud and Vestfold University College (HBV), Norway

Spring 2015

Abstract

There face challenges to build power management circuit for microscale electrostatic vibration energy harvesting. Small capacitance variation limited by standard fabrication process is a common obstacle to obtain sufficient transduction for power conversion. The electronic circuit encounters an issue of compatibility to MEMS integration based on available techniques. A key function of the built interface circuit is able to drive and to power the whole system with only power extracted from ambient vibration. Thus, the energy harvesting system becomes completely autonomous without using any extra suppliers or biases.

This work is to build an ASIC interface circuit for the MEMS electrostatic energy harvester where range of transducer capacitance is below ∼10 pF. The designed circuit is therefore proper for typical comb-drive overlapping capacitive transducers. The circuit topology consists of three main elements: double charge pump, flyback path and controlling switch. Among them, the switch plays an extremely important role to control the harvesting system. Optimization of switching sequence has significant effect on harvested power from electrostatic transducer. A control circuit is proposed to detect moments and then to turn on/off switch optimally. As a result, the designed circuit is automatic to control the switch during vibration cycles. To be the self-sustaining system, the circuit draws obtained energy stored in reservoir capacitor to power the entire interface circuit. With the current topology including clocking, a net energy of 7.97 nJ is achieved during 1 second when capacitance variation of the transducer has $C_{\min} = 2.156$pF and $C_{\max} = 8.624$ pF.

Alternatively, a voltage-quadrupler circuit topology is designed to be adaptive to the comb-drive overlapping capacitive transducers. A major advantage of this self-sustaining configuration is that by integration of transducer to series-connected rectifier-capacitor combination, output voltage is boosted to infinite value in principle. For example, with an initial voltage 3 V applied for transducer with nominal capacitance of 30 pF, the obtained voltage ramps up to about 14 V after only 40 ms.

Acknowledgments

I would like to express my sincere gratitude to my supervisors Prof. Eirnar Halvorsen and Assoc. Prof. Mehdi Azadmehr for their enthusiastic support during my thesis work. They has given me precious advices and continual guidance with their patience and deep knowledge. Without their help, I would not be able to complete the thesis.

I am thankful to Cuong Phu Le, Binh Duc Truong, Cuong Hung Nguyen, Hoa Le Thanh, Hai Le The for all of their support towards my works.

I also want to show my grateful thanks to my fellow master students in HBV and my close friends for encouraging me to finish this thesis.

Last but not least, I am truly grateful to my family for their love and support which help me to overcome any obstacles in my life.

Contents

1 Introduction **11**

1.1 Motivation 11

1.2 Application 13

1.3 Working principle 14

1.3.1 Piezoelectric transducer 15

1.3.2 Electromagnetic transducer 16

1.3.3 Electrostatic transducer 17

1.4 Power management circuit: literature review 18

1.5 Scope of the thesis 20

1.6 Thesis outline 21

2 MEMS Electrostatic Vibration Energy Harvesting **23**

2.1 MEMS electrostatic transducer geometry 23

2.2 Transducer biasing 24

2.3 Continuous system 25

2.4 Switched system 27

2.5 Charge-constrained operation 28

2.6 Voltage-constrained operation 30

2.7 Synchronous and asynchronous systems 33

3 Circuit Design and Simulation Results **35**

3.1 Transducer model 36

3.2 Capacitance variation 38

3.3 Circuit topology 40
3.4 Charge pump 40
3.4.1 Basic charge pump 40
3.4.2 Double charge pump 43
3.5 Double charge pump with flyback path 47
3.6 Switching time optimization 50
3.6.1 Flip-flop level shifter 51
3.6.2 Circuit detecting *off* event 52
3.6.3 Circuit detecting *on* event 58
3.7 Consumed-power estimation and optimization 66
3.7.1 Power consumption 66
3.7.2 Elimination of external power supplies 67
3.7.3 Clocking technique 69
3.7.4 Self-sustaining topology 70
3.7.5 Power enhancement 71
3.8 Discussion 71
3.9 Voltage quadrupler circuit 72
3.9.1 Operation principle 72
3.9.2 Simulation results 72
3.9.3 Discussions 73

4 Conclusions **75**

Bibliography **77**

Acronyms

ASIC	Application-Specific Integrated Circuit
AIN	Aluminum Nitride
DC	Direct Current
IC	Integrated Circuit
MEMS	Microelectromechanical System
PZT	Lead Zirconate Titanate
SSHI	Synchronized Switch Harvesting on Inductor
VEH	Vibration Energy Harvesting
WSNs	Wireless Sensor Networks

Chapter 1

Introduction

1.1 Motivation

Nowadays, with growing demand in collecting data everywhere i.e. environment, infrastructures, equipment, and even ourselves, more and more sensors are used in many sectors such as transportations, aerospace and industry. Unfortunately, it is difficult to install the sensors due to technical issues. A significant reason is difficulty and cost of cabling which supplies power and transfers the signal to remote location. Moreover, for many wireless applications such as sensors used in moving components, embedded systems, or human body, battery is required to power the sensor. Using battery seems to have some limitations due to the limited lifetime and need for replacement. Their disposal poses an environmental hazard since batteries contain chemicals which are harmful to environment and human. To overcome these problems, engineers and researchers are focusing on development of an alternative power source: ambient energy [1].

Scavenging or harvesting energy from environment is not a new concept and has been used widely in various applications. This concept is related to the process of converting energy from ambient environment into electrical energy to power small and autonomous electronic devices such as wireless sensing nodes, mobile phones or medical devices. This deployment has been seen in large-scale systems such as windmills or waterwheels from the ancient time. With tremendous development in using

small-scale and low-power devices today, the field of energy harvesting has attracted more interest and consideration from many research groups than ever. The main reason is that energy harvesting can help these kinds of device to be self-replenished in order to extend their life time without any human intervention.

Energy harvesting can be classified based on the form of energy extracted. Energy sources exist in our environment in various forms like mechanical energy, thermal energy, radiant energy and chemical energy. Each kind of source has its own advantages and disadvantages [2] and then receives different level of attention. Their power densities are demonstrated clearly in Figure 1-1. It is obvious that solar cells offer the most power density in outside sun. While solar energy is the most well-known source for energy harvester and employed in a wide range of size scales and power levels [3,4], its limitations are the cost for large-scale generators and the light availability for small-scale devices. Power harvested from thermal gradients is also exploited in a wide range of work [5,6]. In thermoelectric generator, a large temperature variation is required to generate useful power. However, it is difficult to find temperature differences greater than 10°C in a microsystem. As a result, high power levels are hard to achieve. In the case of vibration generation, mechanical vibration energy present in the environment or surrounding system is converted into electrical energy. Since the potential power from this conversion is available and abundant to use, that attracts more studies and investigations [7,8].

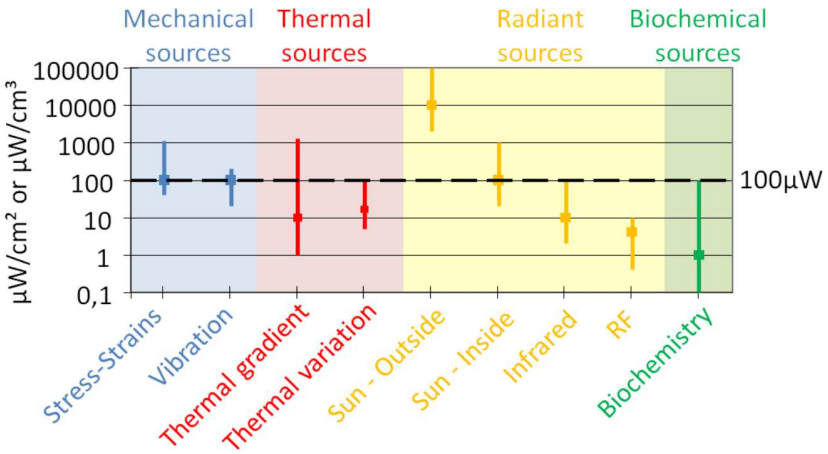

Figure 1-1: Power densities of ambient sources before conversion [9]

1.2 Application

The typical application of energy harvesting is to be embedded into wireless sensor networks (WSNs) as shown in Figure 1-2. In this system, power generated from the harvester is stored to an energy storage and power management before being utilized by microcontroller or other electronic components to transmit data from sensors to host centres. Some detail applications for WSNs can be seen in many reports [10, 11]

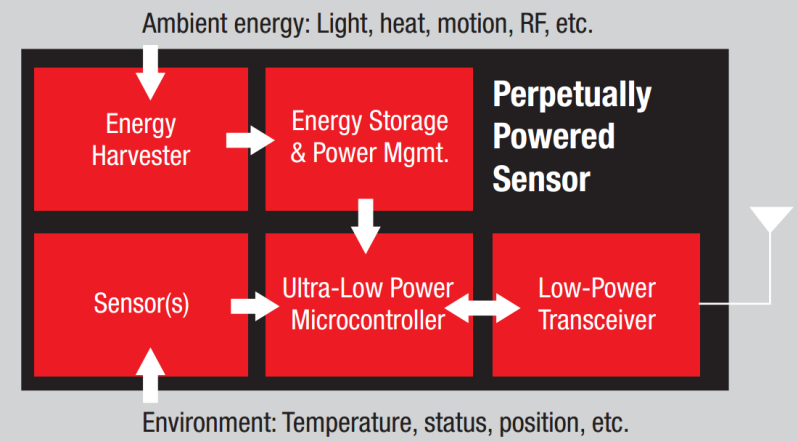

Figure 1-2: Schematic drawing of an energy harvester embedded into a wireless sensor node [12]

Among fields of application, energy harvesting technique has been used widely in remotely monitoring the status of mechanical structures such as bridges, aircraft, tunnels and buildings. With the support of this monitoring system which is self-powered by harvesters, failure and expensive maintenance cost of these structures can be reduced. Figure 1-3 shows an example where piezoelectric generator is used for structural health monitoring of a bridge [13].

Energy harvesting technique has also been applied in many diagnostic and implantable biomedical devices where using or replacement of battery can be disadvantage and expensive. An example of this application can be seen in Figure 1-4 where an electrostatic energy harvester actuated by blood pressure in the heart to generate power for intra-cardiac implants [14]. The innovative multilayer out-of-plane electrostatic energy harvester with 6-mm diameter and 1-mm thickness is able to provide an electrical energy about 20J per heartbeat.

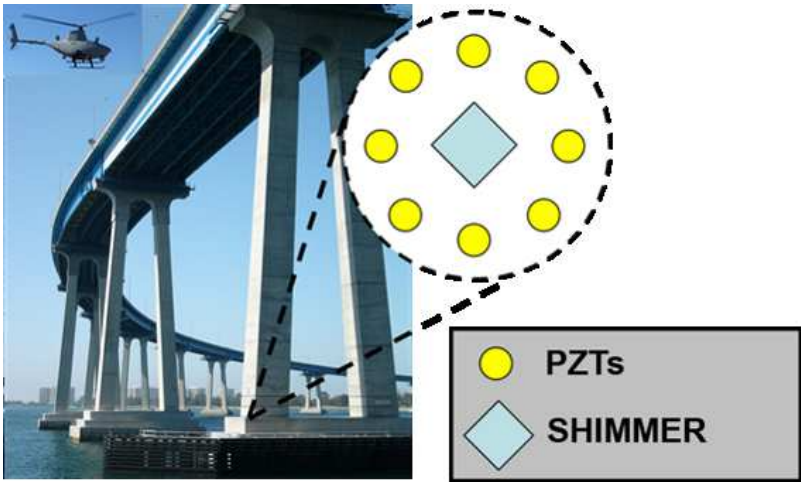

Figure 1-3: Piezoelectric generator for structural health monitoring developed by SHIMMER group [13]

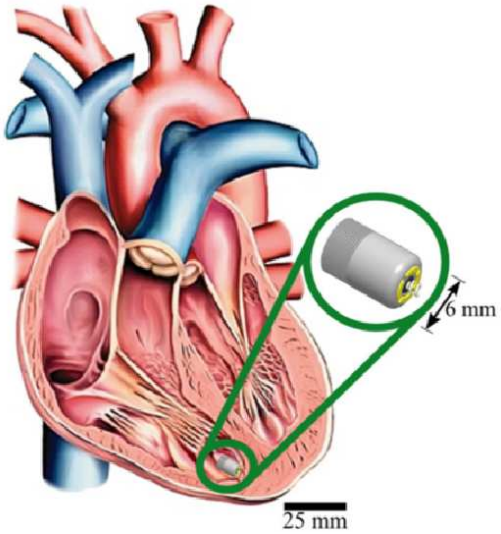

Figure 1-4: An electrostatic energy harvester for powering intra-cardiac implants [14]

1.3 Working principle

A typical vibration generator is shown in Figure 1-5. The model was presented by Williams and Yates [15] at the first time. It consists of a proof mass m, suspended from the package frame by a mechanical spring with stiffness k. Under surrounding kinetic energy, the mass is vibrated with the displacement x relative to the device package position. The relative displacement of proof mass drives transducer to generate electrical power. For a sinusoidal excitation $y(t) = Y_0\cos(\omega t)$, the inertial force

can be found from equation (1.1)

$$f(t) = -m\ddot{y} = mA\sin(\omega t) = mY_0\omega^2\sin(\omega t) \tag{1.1}$$

where Y_0 is the amplitude of vibration, ω is the angular frequency of vibration and A is the amplitude of acceleration

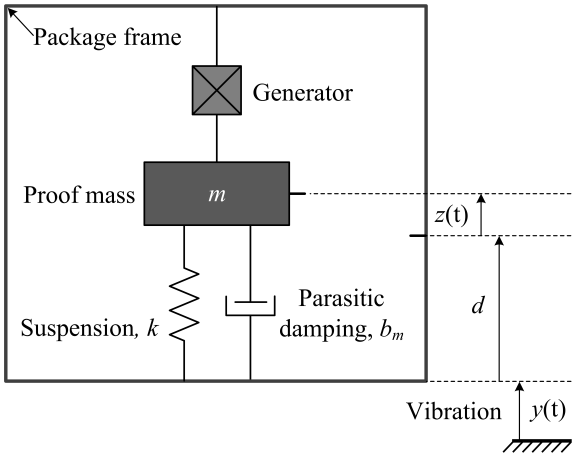

Figure 1-5: General schematic of vibration energy harvester

There are three prevalent conversion mechanism of vibration energy harvesting, i.e. electromagnetic, piezoelectric and electrostatic, which are introduced as follows.

1.3.1 Piezoelectric transducer

Piezoelectric generator makes used of piezoelectric effect of piezoelectric materials (such as PZT and AIN). Piezoelectric effect is a phenomenon that exhibits the relationship between mechanical properties and electrical properties. Specifically, a strain applied to piezoelectric material produces electric field in that material and conversely, the material will deform when exposed to electric field. Common design of piezoelectric harvester has piezoelectric film attached to cantilever beam in different configurations as shown in Figure 1-6. Among these, the third configuration (c) is said to generate the highest power under lower excitation frequencies and load resistances [16].

Many works have been done on designing and fabricating MEMS-based piezo-

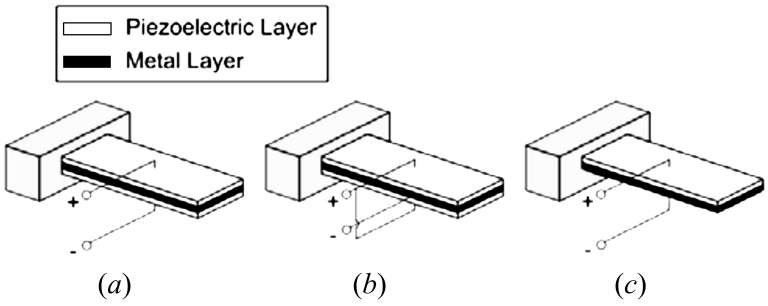

Figure 1-6: *a*) A series triple layer type cantilever, *b*) A parallel triple layer type cantilever, *c*) A unimorph cantilever [16]

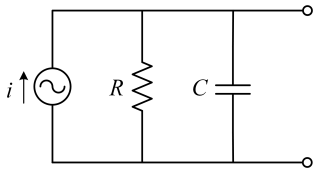

Figure 1-7: Equivalent circuit of piezoelectric transducer

electric energy harvesters. For instance, a thin film AIN cantilever micro generator designed by Marzencki *et al.* [17] can produce power of 2 μW at vibration amplitude and frequency of 4 g and 1368 Hz respectively. A PZT-based harvester proposed by M.Renaud *et al.* [18] can generate 40 μW at vibration frequency of 1.8 kHz and displacement amplitude of 180 nm. These piezoelectric transducers can be modelled as a sinusoidal current source in parallel with a high value of resistance R and capacitance C as shown in Figure 1-7.

An advantage of piezoelectric conversion is that it can generate high output voltages. No external voltage source is required to initiate the process and also no mechanical limit stops are needed. However, piezoelectric materials are expensive and highly dependent on operating temperature. Another drawback is difficulty of implementation on micro-scale and integration with microelectronics.

1.3.2 Electromagnetic transducer

Electromagnetic energy harvesting involves a coil of wire moving in a magnetic field. The relative motion between the coil and the magnetic field results an induced current to flow in the coil in accordance to the principle of Faradays law as illustrated in Figure

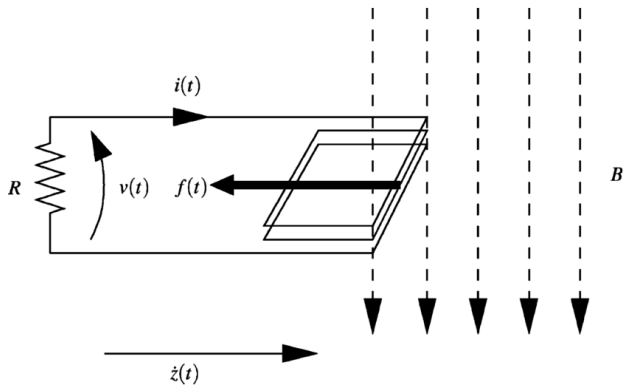

Figure 1-8: Principle of operation of electromagnetic transducer [19]

1-8.

In general, electromagnetic energy harvesting devices are classified into resonant, rotational and hybrid [20]. Several types of small-scale electromagnetic generators have been designed and developed. Williams *et al.* [21] has fabricated one type of resonant generator which could generate 0.3 μW at an excitation frequency of 4 KHz. Holmes *et al.* [22] developed an axial-flux permanent magnet electromagnetic generator that could deliver an output power of 1.1 mW per stator at a rotation speed of 30000 rpm. Although electromagnetic devices offer high output currents and do not require external voltage source to get started, there still exist some challenges to electromagnetic implementation. First, the output voltages are low due to limitation in the number of coil turns. Second, it is hard to develop MEMS devices.

1.3.3 Electrostatic transducer

Electrostatic converters are capacitive structures which consist of two plates separated by a dielectric. These two plates move relative to each other, resulting in a capacitance variation and change in electric charge. In electrostatic generators, external mechanical force applied to vibrate electrode plates performs work against electrostatic force. These devices are split into two types, which are electret-free electrostatic converters and electret-based electrostatic converters. Electret (formed from electricity magnet) is a dielectric material that has a quasi-permanent electric charge or dipole polarization. While the first one uses conversion cycles made of charge and

discharge of the capacitor, the rest uses electrets to convert mechanical energy into electricity directly. Two common conversion cycles are charge-constrained conversion and voltage-constrained conversion, which will be discussed further in Chapter 2.

A drawback of electrostatic transducer is that operation requires bias. Also a mechanical limit stop is required in some designs to prevent electrodes coming into contact. However, compared to piezoelectric and electromagnetic systems, electrostatic converters have an advantage that they are the most compatible with IC and MEMS technology. Therefore, a lot of studies on designs, simulations and experiments [23–25] have been conducted on MEMS electrostatic energy harvesters.

1.4 Power management circuit: literature review

It is clear from the literature that most of investigation focuses on mechanical components and transducers, while there still exist dramatic issues need to be addressed in terms of power conditioning system. Only simple resistive or simple processing circuit by bridge rectifiers and capacitor are used to estimate output power from the transducer, while the power processing stage is required more than that in order to store and transfer energy from transducer to electronic applications as shown in Figure 1-9. Interface circuit enables impedance matching between transducer and the electrical system. Voltage regulation is required to convert output current and voltage from the harvester to the forms compatible with load electronics. Energy storage ensures the continuous operation of the system.

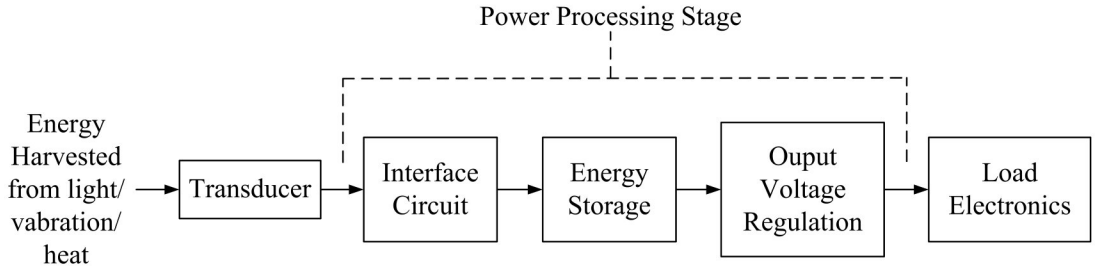

Figure 1-9: Power electronics topology for energy harvesting system [26]

Difficulty in design of power electronics system is that generated power must be

maximized. Moreover, energy used by the circuitry should be as low as possible so that the system can both self-sustain from energy harvester and supply power to the load at the same time. Thus, power management techniques are required as discussed in following sections.

It has to be acknowledged that most of works on power electronics have been done for piezoelectric transducer. Since output voltage from transducer is time varying, a diode bridge rectifier followed by a capacitor is used to convert that voltage into DC form which is suitable to power electronic loads. This standard interface circuit is simple and popular but not a good choice for implementation due to two key reasons. First, the maximum power cannot be extracted, resulting in low power conversion efficiency. Second, using diodes causes voltage drops, leading to significant power loss in the system. Instead of that, several techniques were proposed to deal with these issues. In order to reduce the power loss, Le *et al.* [27] proposed MOSFET synchronous rectifiers in the replacement of diodes. To increase the efficiency, switching connection between generator and processing circuit is necessary to maximize harvested energy. Ottman *et al.* [28] used a step-down dc-dc converter with optimal duty cycle to achieve maximum power transfer. Another solution was given by Lefeuvre *et al.* [29] and D'Hulst *et al.* [30] in which a buck boost converter was used to track the generators optimal working points through tuning active resistive loads and to generate a proper DC voltage for output sensors. Guyomar and Liang *et al.* presented a technique called synchronized switch harvesting on inductor (SSHI) [31] and modified SSHI [32], which helps to increase coupling electromechanical and then results in a significant increase of the electromechanical conversion capability of piezoelectric material.

Power electronics for electrostatic generator is also attractive but less literature was proposed. Mur-Miranda *et al.* [33] discussed charge-constrained and voltage-constrained operation. He proposed a synchronous capacitive energy harvester consisting of two active switches to charge and discharge variable capacitor through an inductor. The drawbacks of this architecture are that the complexity of control circuitry and the expense of power dissipation for synchronization, which reduced net power delivered to the load. Based on the topology presented by Mur-Miranda *et al.*,

Miyazaki *et al.* [34] has made some improvement by using timing capture instead of programmable controller with DLL feedback. In these two architectures, the problem of energy injection from clock signal to harvested energy remains concern. This problem is pointed out by Yen [35], in which he used a charge pump followed by a flyback circuit to store and transfer extracted energy. This topology was investigated further by Galayko, Basset *et al.* [36] with the focus on designing control circuit to optimize the flyback switching sequence. Other architectures come from Torres *et al.* [37] with voltage-constrained topology and Kempitya *et al.* [38] with the modification of storage capacitor in the charge pump part.

1.5 Scope of the thesis

The previous researches have focused on the interface circuit for capacitive transducers with large capacitor variation. There are limited researches studying the circuit for comb-drive transducer with small capacitor variation. Furthermore, with the goal of designing a circuit that not only harvests the maximum power from the harvester but also consumes as low power as possible in order to both self-sustain from energy harvested and supply to the load at the same time, the proposed circuit in this thesis is demonstrated to be promising compared to other previous works due to two main reasons:

- Most of previous ones use external signals to control the operation of the circuit. Distinguishing from the others, this thesis builds an autonomous circuit which generates the control signals from monitoring the state of the circuit.

- While it is not shown in many works that whether harvested power can be used to power each block in the interface circuit, this thesis tries to deal with power consumption of the control circuit and suggests some solutions so that the circuit can be self-sustained from generated power.

1.6 Thesis outline

This chapter has just presented the motivation, application, working principle of energy harvesting and a general description of research direction. The next chapter focuses on MEMS electrostatic vibration energy harvesting in terms of operation modes. A review of various circuit implementation for each of operation modes is also included. Chapter 3 deeply investigates working principle of charge pump and flyback path circuit. Based on this fundamental topology, necessary modification has been discussed to adapt to comb-drive transducer. The most importantly, the process of building the circuit controlling the switch is presented step by step together with simulation results. Power consumption and several suggestions to improve performance of presented circuit are also mentioned. Final chapter summaries the key results of the thesis and future work.

Chapter 2

MEMS Electrostatic Vibration Energy Harvesting

As briefly discussed, electrostatic energy harvesters seem to be more promising compared to other transducers technologies thanks to the ability of miniaturization and MEMS integration. In addition, this branch of energy harvesting technique is less exploited compared to macro-scale piezoelectric and electromagnetic devices which are mature and investigated in many research literature. This thesis focuses on small-scale electrostatic energy harvester. A major challenge when working with this kind of devices is that output power is very low, in the range of μW. It makes design of power electronic interface circuit more difficult and complicated. In this chapter, device principles and circuit implementation for different operation modes will be discussed in detail.

2.1 MEMS electrostatic transducer geometry

Electrostatic energy harvesters, as quickly introduced in the previous chapter, generally use capacitor structures with moving electrodes. Based on the relative motion between proof mass and electrode plates, they can be classified into different varieties such as in-plane overlap, in-plane gap closing, out-of-plane gap closing and in-plane converter with variable surface [9] as shown in Figure 2-1. Compared to in-plane gap

closing or out-of-plane gap closing, the in-plane overlap varying converters are able to offer a large proof mass displacement [39]. Due to their ability to be integrated in microsystems, many MEMS-based electrostatic harvesters have been fabricated successfully. Some of the examples can be found in [40,41]

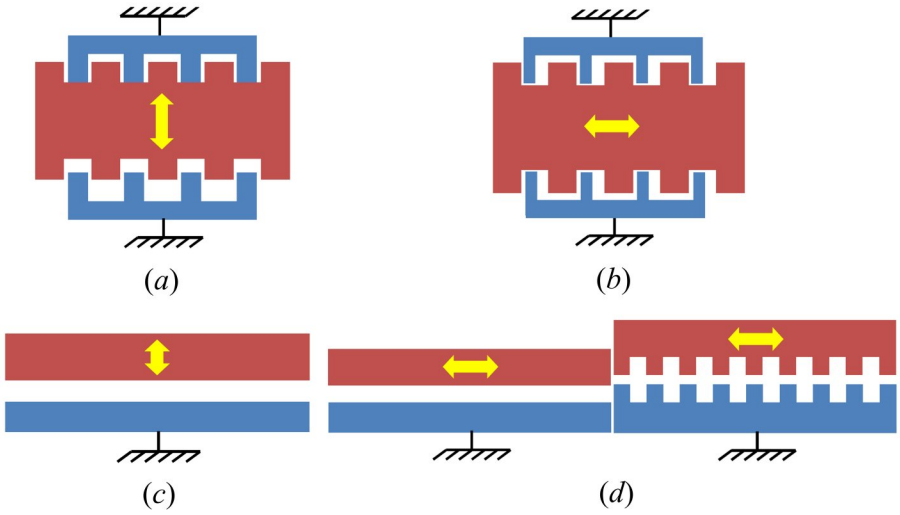

Figure 2-1: Electrostatic vibration energy harvester geometry: *a*) In-plane overlap, *b*) In-plane gap closing, *c*) Out-of-plane gap closing, *d*) In-plane converter with variable surface [9]

2.2 Transducer biasing

There are two ways to operate an electrostatic harvester, in which the transducer is biased either by external or internal source. While the first type uses external voltage/ charge source or power control circuit for harvester operation, the second one utilizes electrets, floating electrodes or material work function differences instead. Each kind of biases has its own benefits and drawbacks. The common method to provide internal bias, use of electrets, for instance, can facilitate the microsystem integration but it is costly and induces stability problem. Whilst, the use of external voltage/charge source is much simpler but causes problem with integration. Beside bias based classification, the electrostatic energy harvesters are also categorized into two types of operation modes i.e. switched mode and continuous mode [19] which are illustrated in Figure 2-2 and Figure 2-3 and will be explained in the next section.

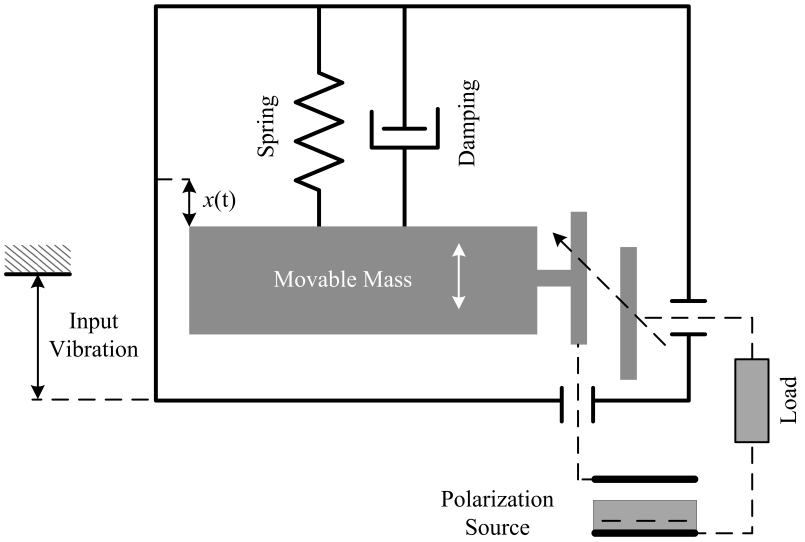

Figure 2-2: Continuous operation

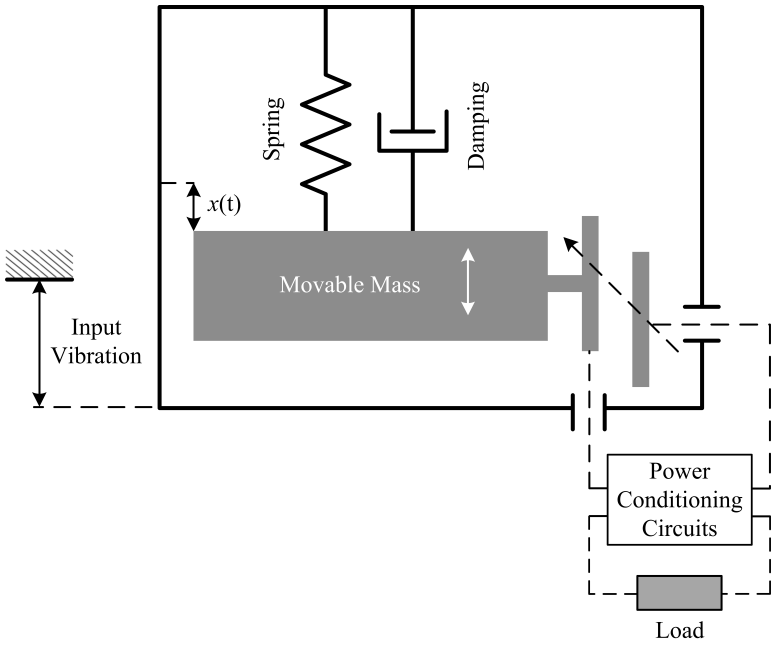

Figure 2-3: Switched operation

2.3 Continuous system

In continuous system, the variable capacitor is continuously connected to the load circuitry with a polarization source. A well-known example of this is the use of electret layers as a built-in bias source to keep permanent charge and polarize the harvesting capacitors. This makes the electrostatic energy harvester like the piezoelectric one.

The operation of an electrostatic generator in continuous mode can be displayed in Q-V plane as shown in Figure 2-4. The curve (1-3-1), (1-2-1) and (1-4-1) are corresponding to the cases when the capacitor is operated in a constant voltage mode, constant charge mode and optimized load mode respectively.

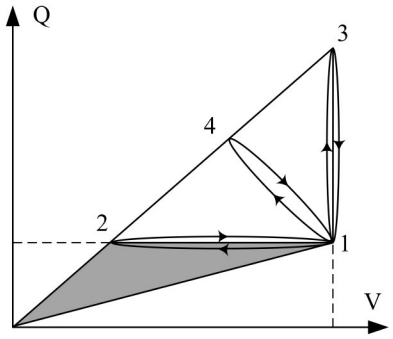

Figure 2-4: Operation of an electrostatic generator in continuous mode [26]

One example of continuous system is connecting a capacitive transducer to a voltage source in series with a load resistor as shown in Figure 2-4. In this circuit, the variable capacitor is continuously connected to the load, thus the generated charge induced by capacitor change will be continuously delivered to the load resistance. Other example can be the use of electret layer in corporation with variable capacitor as a bias in continuous generator. Sterken *et al.* [42] proposed a micromachined electrostatic converter consisting of variable capacitor polarized by a charged electret layer. The device is a two-wafer stack, where the top wafer contains lateral comb capacitor, suspended by clamped beams, the second wafer contains a charged dielectric. This charge distribution results in an electric field between plates of the variable capacitor, which is equivalent to the field generated by a voltage source. The variation of the capacitance induces a current through the load resistor, R, as shown in Figure 2-6. In this configuration, the load resistor plays a role as a conditioning circuit for the harvester. The device generates 50 μW with a 5 μm vibration amplitude.

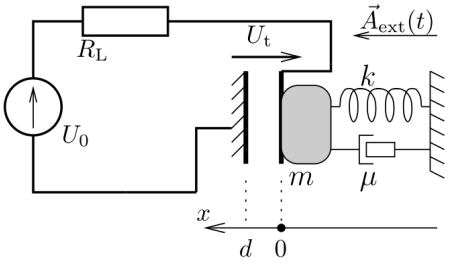

Figure 2-5: Schematic view of the continuous conditioning circuit [43]

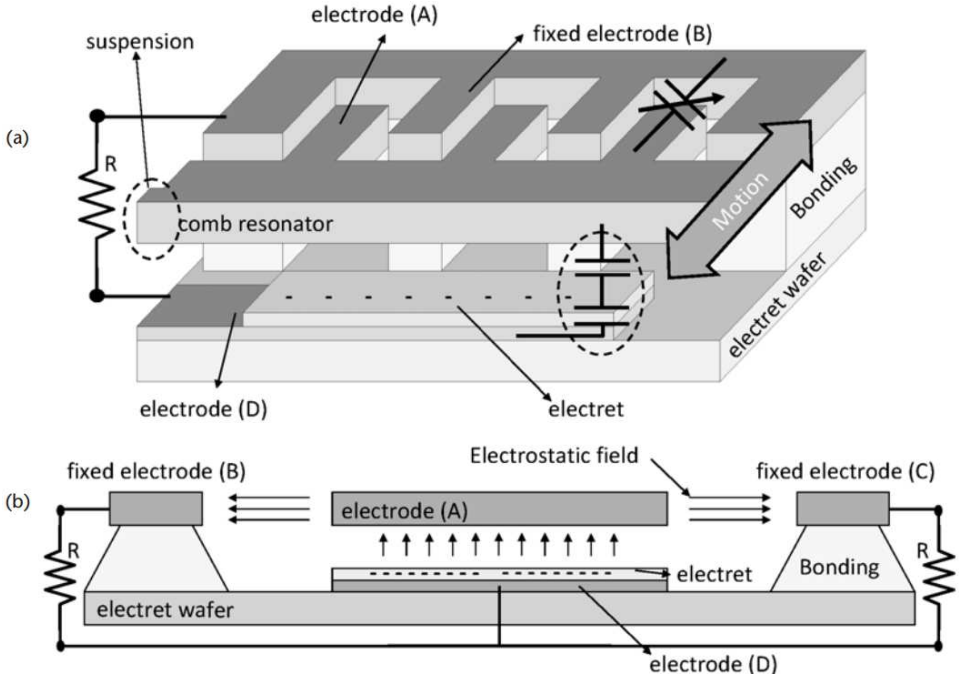

Figure 2-6: *a*) Cross-section and *b*) side view of electrostatic harvester [42]

2.4 Switched system

In the switched systems, the transducer is connected to the circuitry to reconfigure the system at different parts of the generation of cycle through the operation of switches. Thus, in this operation, an initial temporary bias voltage is used and the power conditioning circuit is required to charge and discharge the variable capacitor. The operation of switched transducer is divided into two prevalent types i.e constant charge and constant voltage. These cycles are plotted in the Q-V plane as shown in Figure 2-7 where either charge on or voltage across variable capacitor is kept constant during the conversion cycle. The principle and circuit implementation of

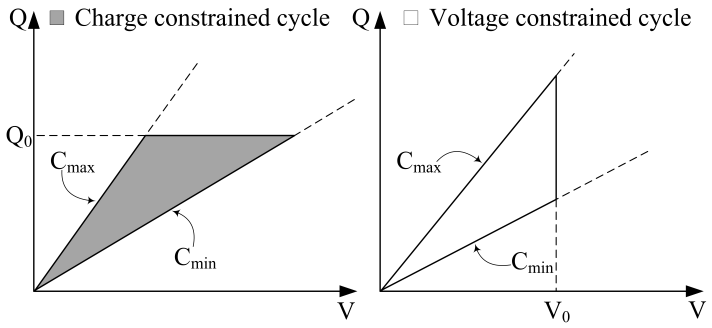

Figure 2-7: *a*) Charge-constrained conversion *b*) Voltage-constrained conversion

these conversion cycles will be discussed further in this chapter.

While in switched mode operation, the complicated electronic circuits are required to reconfigure the system at different phases of energy conversion, there is no need of any smart electronics to operate continuous system. It is a trade-off between the cost and the efficiency of the system, wherein the later lower the cost but also reduce the efficiency compared to the first. Continuous conditioning circuit is often used when the research purpose is to test the device [44] or when the transducers use electret layer for biasing [45].

2.5 Charge-constrained operation

The charge-constrained cycle starts when the capacitance reaches its maximum value $C_{\max}$. At this point, it is pre-charged by external circuitry to a certain level Q_{cst}. The device is then disconnected and let in open circuit to keep the charge constant. Under mechanical vibration, the capacitance decreases to minimum value $C_{\min}$. As the charge is kept constant during this time, the decrease of capacitance leads to increase of voltage across the capacitor. This means an additional energy is generated and stored in electric field between the electrodes. The whole cycle is illustrated in Figure 2-8. Total converted energy can be calculated as in equation (2.1)

$$E = \frac{1}{2} Q_{\text{cst}}^2 \left(\frac{1}{C_{\min}} - \frac{1}{C_{\max}}\right) \tag{2.1}$$

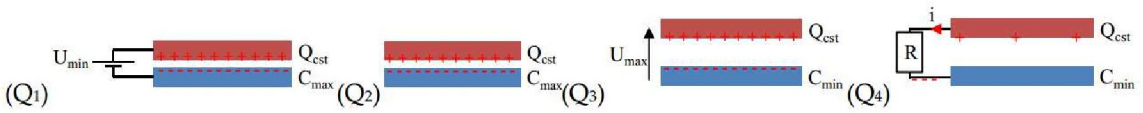

Figure 2-8: Charge-constrained cycle [9]

One typical example of charge-constrained operation is shown in Figure 2-9 *a*). As the cycle starts, the capacitor is charged up to an initial voltage at its maximum value. This is done by driving the MOSFET M_1 and M_2 act as the switches in a boost converter. Specifically, M_2 is pulsed to pump the energy from battery to capacitor through drain body diode of $M1$. Next, both switches turn off, leaving the capacitor open circuit. During this phase, electrodes of the variable capacitor C_{var} are separated, reducing the capacitance to minimum value. The voltage across C_{var} is then increased since the charge on it is kept constant. Finally, the generated energy is transferred from C_{var} to battery by controlling the MOSFET M_1 and M_2 act as buck converter. Once all energy is transferred, the harvested phase ends and the cycle repeats.

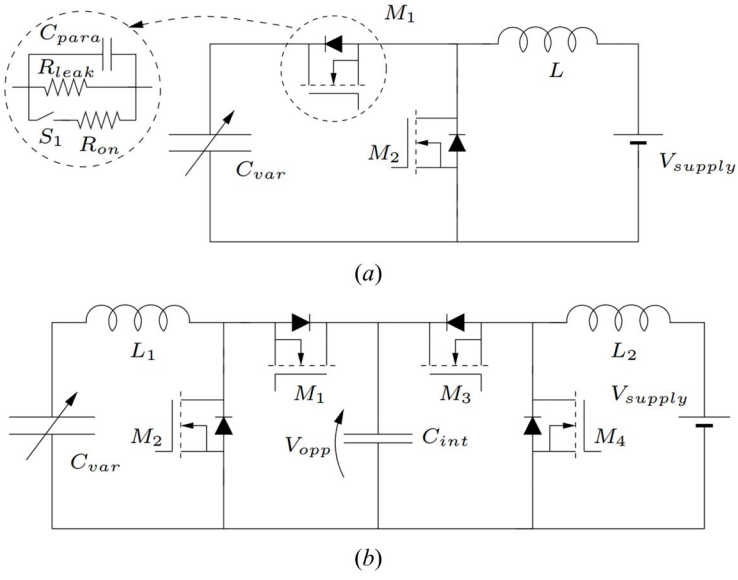

Figure 2-9: *a*) Constant charge mode generator; *b*) Constant voltage mode generator [46]

Meninger *et al.* [47] proposed a charge-constrained electrostatic energy harvester involving two active switches as shown in Figure 2-10. The variable capacitor C_{mems}

with the comb structure was used as transducer. At startup, there is no voltage across C_{mems} and the transducer needs to wait until C_{mems} reaches $C_{\max}$ to start conversion process under external vibration. During the pre-charge process, SW2 is on, SW1 is off and the energy is stored into the inductor L. This energy is then pumped into harvesting capacitor C_{mems} by turning on and off SW1 and SW2 respectively. Both switches are then turned off, leaving the capacitor in charge-constrained mode. When C_{mems} drops to minimum capacitance $C_{\min}$, SW1 is on to charge the inductor from the variable capacitor. Then, SW1 is off and SW2 is on till all the charge is transferred into C_{res}. The conditioning circuit utilizes programmable controller to turn on/off switches. The fabricated controller and associated power electronics are enabled to synchronize the conversion process with the phase of the plate motion by applying an energy feedback control. The feedback method chosen is Delay Lock Loop (DLL) architecture where an appropriate delay line and a reference clock which shares the same frequency as desired vibration motion frequency are implemented. The drawbacks of this architecture are the complexity of control circuitry and the expense of power dissipation for synchronization.

Based on the topology proposed by Meninger *et al.*, Miyazaki *et al.* [34] has made some improvement by using timing capture (see Figure 2-11) instead of programmable controller with DLL feedback. A converted power of 120 nW is achieved from a 45 Hz vibration.

2.6 Voltage-constrained operation

Figure 2-12 shows all steps of voltage-constrained cycle. As can be seen, the capacitor is first pre-charged to initial value Q at its maximum capacitance using an external supply source. This constant voltage U_{cst} is connected to the capacitor throughout the conversion cycle. During this time, the relative motion of the plates causes the capacitance to decrease. As the voltage across the capacitor is constant, the charge of the capacitor decreases, resulting in an increase of energy stored in the source. This converted energy can be calculated by

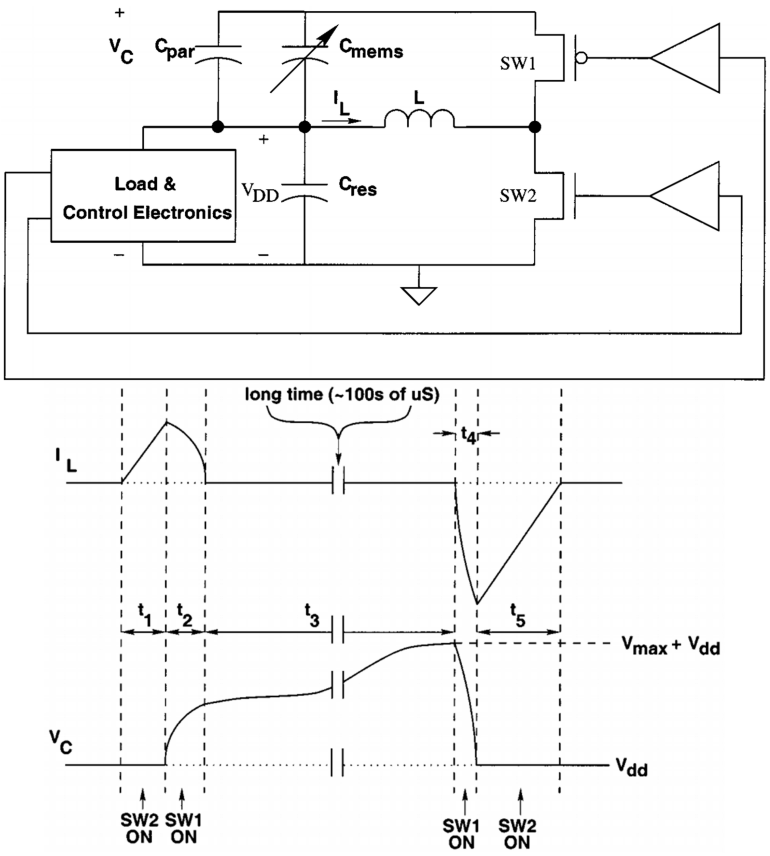

Figure 2-10: Mur-Miranda *et al.*'s proposed circuit and timing waveform [47]

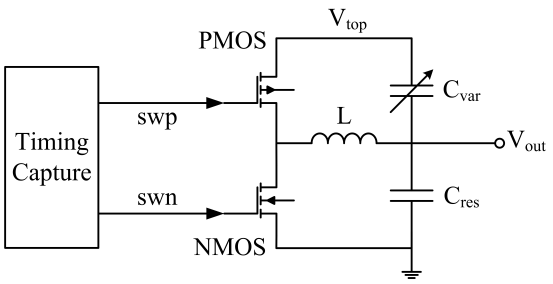

Figure 2-11: Miyazaki *et al.*'s circuit topology [34]

$$E = U_{\text{cst}}^2 (C_{\max} - C_{\min}) \tag{2.2}$$

Figure 2-9 *b*) shows an example of constant voltage mode. At first, intermediate capacitor C_{int} is pre-charged to the operating voltage through L_2 by boost action of M_3 and M_4. After that, M_3 and M_4 remain off and the variable capacitor C_{var} is

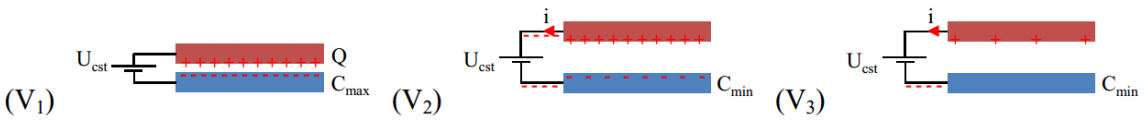

Figure 2-12: Voltage-constrained cycle [9]

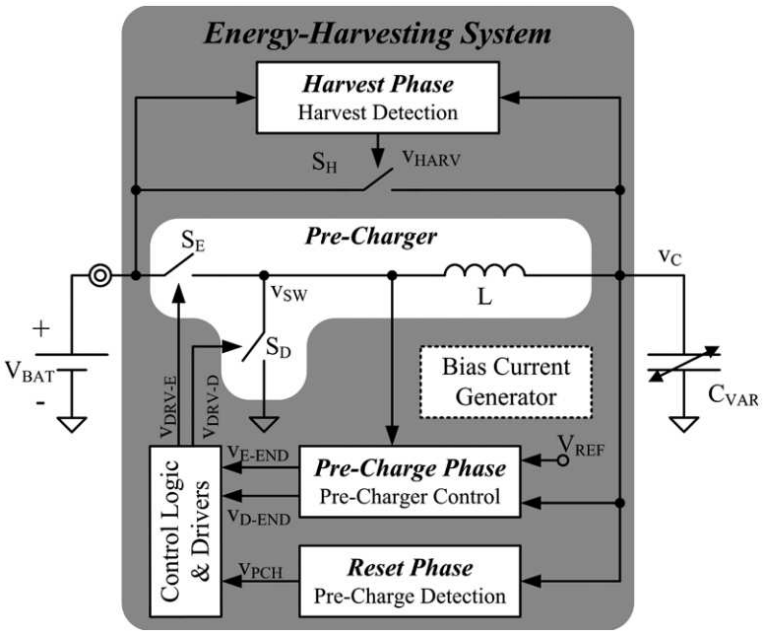

Figure 2-13: Torres *et al.*'s circuit topology [37]

then charged through L_1 due to buck action of M_1 and M_2. As voltage across C_{var} reaches the operating value, M_2 turns off and M_1 turns on to hold the voltage across C_{var} constant. During this time, C_{var} is reduced by separation of plates, leading to a charge pushed into C_{int} . Finally, M_1 and M_2 turn off and the increased electrical energy stored in C_{int} is transferred to the battery through L_2 in a buck operation. One drawback of charge-constrained configuration is that voltage across capacitor can increase to a value that exceeds the breakdown limit of high-volume semiconductor process. Thus, that kind of circuit requires higher voltage transistor, resulting in more expensive technologies. Torres *et al.* proposed a voltage-constrained configuration that uses the systems already-existing battery to avoid additional source, as shown in Figure 2-13. The system undergoes three phases, including precharge, harvest and reset phase. At first, C_{var} is charged to battery voltage before connected to battery to

avoid conduction loss. The harvest phase then starts when C_{var} is connected to the battery and the capacitance drops from maximum to minimum value, charging the battery. As C_{var} reaches C_{min}, it is disconnected from the battery, leaving the circuit in reset phase. During this time, C_{var} increases while charge on it is constrained, leading the voltage across C_{var} to drop to lower value. Finally, the reset phase ends when $C_{\text{var}}$is equal to C_{max} and the cycle repeats. The advantage of circuit is the usage of low cost transistors for sub-5V operation. On the other hand, designing of proposed circuit also confronts several challenges. Specifically, requirement of pre-charge energy and power consumption of monitoring and control circuitry to detect C_{max} and C_{min} during each phase reduce harvested energy.

2.7 Synchronous and asynchronous systems

As discussed above, during operation cycle, the variable capacitor is charged and discharged by controlling of switches. These events can be synchronized or unsynchronized with the mechanical cycles. In the synchronous electrostatic energy harvesting circuit [47] [38], the switches are turned on and off to charge and discharge the variable capacitor when its capacitance reaches maximum and minimum value respectively. Thus, a complex control circuitry with accurate gate clocking is required to achieve this synchronization. On the other hand, in asynchronous circuits [48], the charge and discharge event of capacitor do not need to be synchronized with mechanical motion of plates. The energy can be stored into an intermediate capacitor and then transferred to battery after a number of vibration cycles. With this topology, the difficulties in gate clocking requirements could be eliminated.

Chapter 3

Circuit Design and Simulation Results

Chapter 2 has presented the general principle of electrostatic energy harvesting technique and power electronic interface circuits for this kind of mechanism. There are quite a large number of circuit implementation and techniques proposed, which have their own benefits and drawbacks. However, most of the works concentrate on interface circuit design for capacitive transducers with large capacitance values which are hardly obtained in MEMS standard fabrication process. In addition, these introduced circuits also show the lack of capability to be implemented in ASIC technology. In this chapter, a proposed circuit design for MEMS electrostatic transducer with very small capacitance values and compatible with ASIC implementation will be further investigated. This circuit is based on the one introduced by Yen *et.al* [48] with some modifications in topology to adapt to the two-variable-capacitor structure of the harvester. Furthermore, the matter of how to control the switch to harvest the maximum power from the transducer, which has not been mentioned in Yen' paper will be figured out. The obtained circuit is demonstrated to have the self-autonomous characteristic through simulation results. Some additional techniques and adjustment necessary to optimize power consumption of the circuit are also discussed in this Chapter. All the simulations have been done with the support of Tanner Tools package and models from AMS035 CMOS technology library.

3.1 Transducer model

The overlap varying capacitive transducer is focused in this thesis. This kind of transducer is typical for MEMS VEH. A design of such harvester is shown in Figure 3-1. In this design, a movable proof mass is suspended by four springs with folded shape which are all connected to two fixed electrode supports.

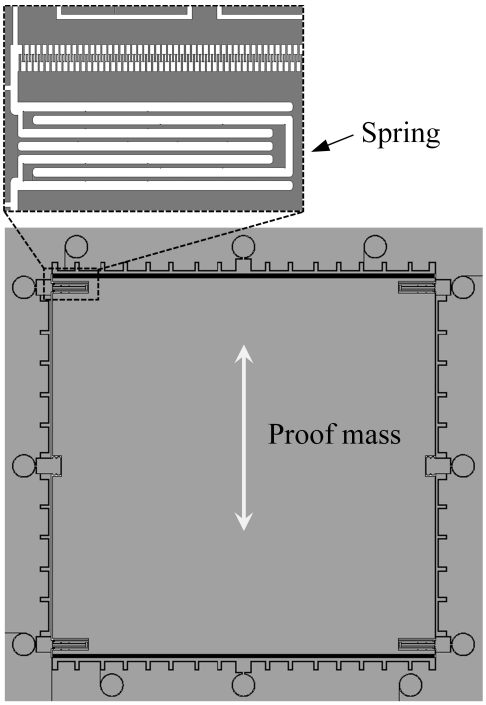

Figure 3-1: In-plane overlap varying capacitive transducer

The lumped-model of the electrostatic energy harvester is illustrated in Figure 3-2 in which the mechanical system including a mass m, a spring with stiffness k and a damper with damping factor b is represented together with electrical system including variable capacitors and resistive loads. The differential equations of the system in mechanical and electrical domains can be expressed as:

$$m\ddot{x} + b\dot{x} + kx + F_{\mathrm{e}} = ma \tag{3.1}$$

$$V_{\mathrm{b}} = -\frac{q_{1/2}}{C_{1/2}(x) + C_{\mathrm{p}}} + V_{1/2} \tag{3.2}$$

where q_1 and q_2 are the charges on the transduction 1 and 2 respectively, F_{e} is the

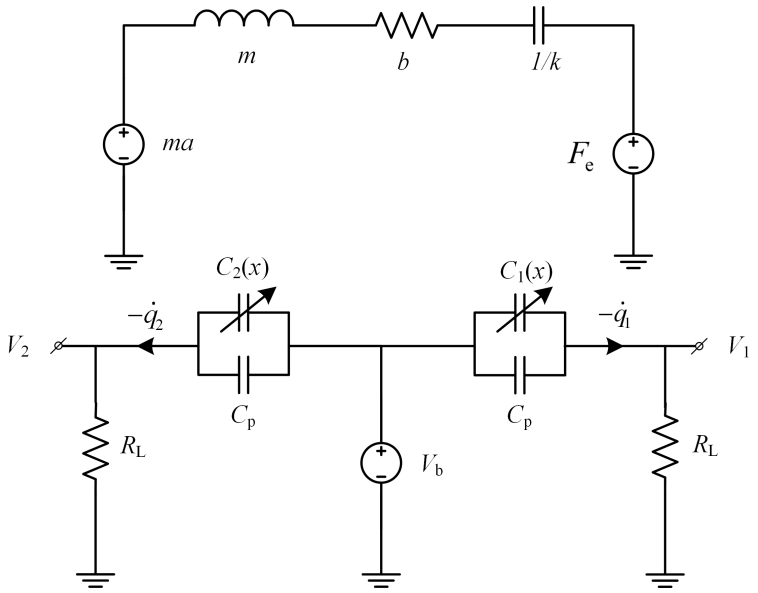

Figure 3-2: Energy harvester model in mechanical and electrical domains

electrostatic force and V_b is the bias voltage for the transducer

The electrostatic force is presented by

$$F_e = \frac{1}{2}q_1^2\frac{d}{dx}(\frac{1}{C_1(x)+C_p}) + \frac{1}{2}q_2^2\frac{d}{dx}(\frac{1}{C_2(x)+C_p}) \tag{3.3}$$

where

$$C_{1/2}(x) = C_0(1 \pm \frac{x}{x_0}) = 2N_f\varepsilon_0\frac{x_0 h}{g_0}(1 \pm \frac{x}{x_0}) \tag{3.4}$$

where N_f is the number of capacitor fingers on each electrode, ε_0 is the permittivity, g_0 is the gap between the capacitor, x_0 is the initial capacitor finger overlap and h is the finger thickness.

A parasitic capacitance C_p in parallel with the variable capacitor is also included in the model. At the interface of the transducer, a simply circuit topology consisting of resistive load is used for the purpose of testing the device concept only. Practically, in order to power for electronic applications, a more complicated interface circuit is required, which is also the main focus of the thesis.

3.2 Capacitance variation

As mentioned above, the comb-drive transducer can be modelled as two anti-phase variable capacitors whose capacitances vary between the maximum and minimum values alternatively. The variation range of these two variable capacitors can be asymmetric or symmetric depending on whether the in-plane overlap transducer are linear-spring harvester, angled-spring harvester or curved-spring harvester. The parameters of these kinds of harvesters have been derived from several research [49–51]. Consider those parameters for reference, a parameter set of the transducer is chosen for simulation as shown in Table 3.1 where two variable capacitors have the same variation range but anti-phase.

Table 3.1: Parameters of a MEMS electrostatic transducer

Parameters	**Value**
Initial capacitance, C_0	2.3 pF
Initial overlap, x_0	16 μm
Maximum displacement, $x_{\max}$	15 μm
Parasitic capacitance, C_{p}	2 pF
Resonant frequency, f_0	650 Hz

Under acceleration, the displacement has sinusoidal form as

$$x(t) = x_{\max} \sin(2\pi f_0 t) \tag{3.5}$$

Hence, the variable capacitance is obtained by substituting (3.5) into (3.4) with taking into account the parasitic capacitance.

$$C(t) = C_{\mathrm{p}} + C_0(1 \pm \frac{x_{\max} \sin(2\pi f_0 t)}{x_0}) \tag{3.6}$$

For simplicity, (3.6) can be modified as

$$C(t) = C_{\mathrm{p}} + \triangle C \sin(2\pi f_0 t) \tag{3.7}$$

where $\triangle C$ is a function of C_0, $x_{\max}$ and x_0

Rename C_{DC} to C_{p} and C_{AC} to $\triangle C$, the variable capacitance can be rewritten as

$$C = C_{\mathrm{DC}} + C_{\mathrm{AC}} \sin(2\pi f_0 t) \tag{3.8}$$

Thus, the maximum and minimum capacitance are $C_{\mathrm{max}} = C_{\mathrm{DC}} + C_{\mathrm{AC}}$ and $C_{\mathrm{min}} = C_{\mathrm{DC}} - C_{\mathrm{AC}}$ respectively.

The detailed capacitance values of variable capacitors are obtained in Table 3.2

Table 3.2: Capacitance values of variable capacitors

Capacitances	**Value**
C_{DC}	4.3 pF
C_{AC}	2.156 pF
C_{max}	6.456 pF
C_{min}	2.144 pF

To model the variable capacitor in S-Edit, a sinusoidal voltage source is utilized. This source should have the offset and the amplitude equal to C_{DC} and C_{AC} in unit of pF respectively. Its frequency is also set to be the same as the resonant frequency of vibration. Since two variable capacitors are anti-phased to each other, two sinusoidal voltage sources which are out-of-phase by 180^0 are employed as shown in Figure 3-3.

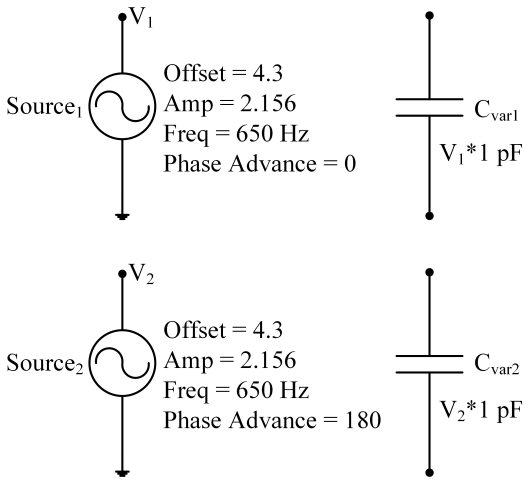

Figure 3-3: Model of variable capacitors implemented in S-Edit

3.3 Circuit topology

The whole circuit topology is illustrated in Figure 3-4 with several adjustments compared to Yen's proposal. The MEMS electrostatic transducer is integrated into a double charge pump instead of basic charge pump. This part is then connected to a flyback path through a switch. The control circuit block is added to control the switch operation in replacement of using external clock. More details about schematic, working principle and simulation results of each block will be discussed in the following sections.

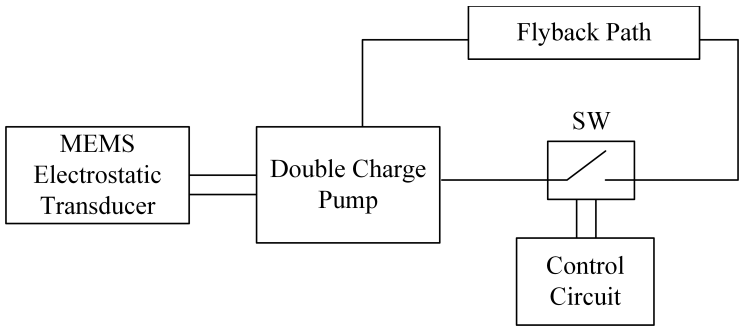

Figure 3-4: Block diagram of circuit topology

3.4 Charge pump

Charge pump circuit is one type of DC-DC converter that converts the supply voltage V_{dd} to DC output voltage higher than V_{dd}. While traditional DC-DC converters uses inductors to function the operation, charge pump is only made of capacitors and switches (or diodes), which facilitates the integration.

3.4.1 Basic charge pump

One typical charge pump is one-stage topology as shown in Figure 3-5 which consists of a pumping capacitance C, two switches S_1, S_2 and a load. By opening and closing the switches S_1 and S_2 respectively, the charge from power supply is pumped into the output load via the capacitor C, resulting in an increase in the output voltage.

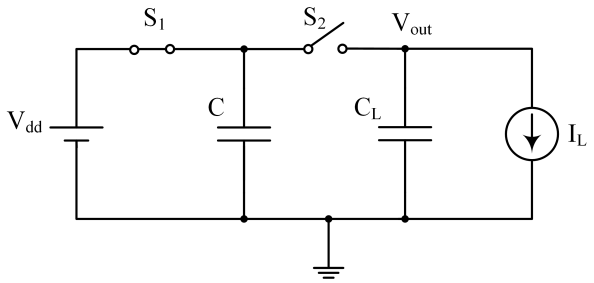

Figure 3-5: Ideal one-stage charge pump

In practice, these switches are not ideal and thus several ways to implement them are presented. The integrated implementation of charge pump, for instance, was demonstrated for the first time by Dickson in 1976 [52]. Like previous discrete implementations by Crockcroft and Walton [53], the Dickson charge pump makes use of diodes instead of switches. Other solution such as MOS diodes can be implemented on silicon [54]. The main benefit of the topology with diodes is that there is no need for switch control signals. However, the drawback of that is the reduction of charge pump output voltage due to forward drop voltage on diodes.

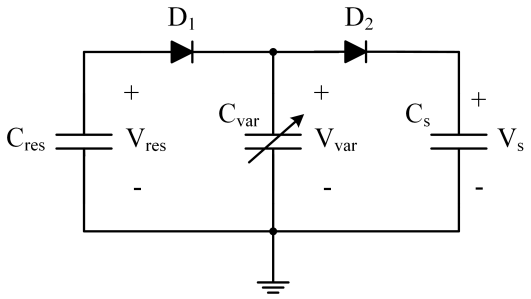

Figure 3-6: Basic charge pump circuit with diodes as switches

Yen *et al.* [48] employed the one-stage charge pump circuit to charge and discharge the variable capacitor as shown in Figure 3-6. The function of this section is to move charge from reservoir capacitor C_{res} into variable capacitor C_{var} and then push energized charge into storage capacitor C_{s}, converting the vibration energy to electrical energy. An initial assumption is made so that $V_{\text{var}} = V_{\text{res}} = V_{\text{s}}$ and $C_{\text{var}} = C_{\max}$. Since the potentials between two terminals of each diodes are equal, D1 and D2 are turned off, keeping the charge on C_{var} constant. One harvesting cycle is defined as one variation of C_{var} from $C_{\max}$ to $C_{\min}$ and back to $C_{\max}$. It is represented in $Q-V$ plane as

shown in Figure 3-7. At first, the resonator vibration separates the capacitive plates, reducing the variable capacitance C_{var} to minimum value C_{min}. For a given constant charge on C_{var}, a drop in capacitance value will lead to increase of V_{var} according to the equation $Q = CV$. As a result, the diode D2 is forward biased and turned on, transferring the charge from C_{var} into C_{s}. As C_{var} reaches C_{min} and starts to increase, V_{var} will decrease, turning off the diode D2 and ending the discharge process of C_{var}. When V_{var} drops to a certain level enough to forward bias D1, the charge will flow from C_{res} into C_{var} through D1. The cycle repeats corresponding to the variation of capacitor. When multiple harvesting cycles take place, the large amount of charge will be transferred into C_{s} and the voltage across it will raise up to a so high level that the variation in C_{var} cannot switch on the diode D2. In other words, the charge cannot be pumped from C_{res} to C_{s} anymore and V_{s} is said to be saturated.

According to (8) and (9) from [48], the value of V_{s} after n energy harvesting cycles and the saturation value are derived as

$$V_{\text{s,n}} = V_{\text{res}}[(1 - \frac{C_{\text{max}}}{C_{\text{min}}})(\frac{C_{\text{s}}}{C_{\text{min}} + C_{\text{s}}})^n + \frac{C_{\text{max}}}{C_{\text{min}}}] \tag{3.9}$$

$$V_{\text{s},\infty} = (\frac{C_{\text{max}}}{C_{\text{min}}})V_{\text{res}} \tag{3.10}$$

It can be seen that the saturation value of V_{s} depends on the ratio of C_{max} to C_{min}.

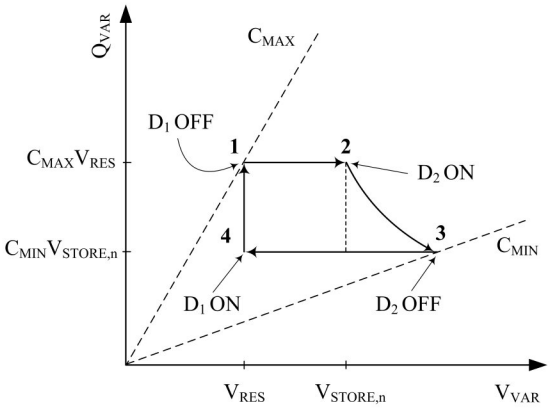

Figure 3-7: One harvesting cycle in Q-V plane for the charge pump part

3.4.2 Double charge pump

Now, to apply for capacitive transducer, the double charge pump is used as shown in Figure 3-8. The double charge pump is achieved by using two pumping capacitors instead of one. The reservoir capacitance and storage capacitance are chosen so that they satisfy the relationship $C_{\mathrm{s}} \ll C_{\mathrm{res}}$. At start, these values are chosen $C_{\mathrm{s}} = 110$ pF and $C_{\mathrm{res}} = 0.01$ μF. In simulation, an initial voltage on C_{res} is set to be 3V as the bias voltage for the harvester, which is necessary to start the conversion process. Practically, the voltage source, a battery for instance, is connected to reservoir voltage node to pre-charge C_{res} for a very short time.

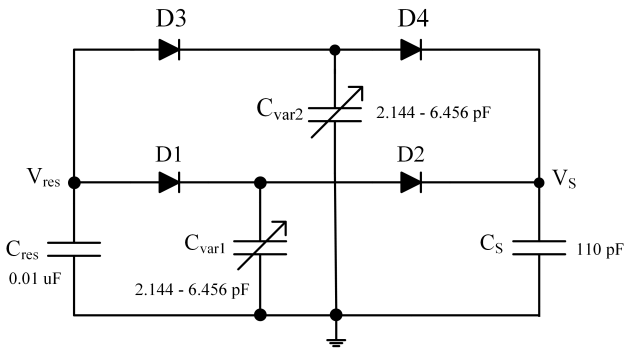

Figure 3-8: Double charge pump circuit

The operation of double charge pump is similar to the case of one pumping capacitor except the fact that the charge is now pumped into C_{s} continuously during the first half and the second half of the cycle as shown in Figure 3-9. Meaning that the time interval between two charge transfer into C_{s} is now only T/2 where T is the period of the one complete harvesting cycle. Consequently, V_{s} now increases faster and quickly reaches saturation value. The value of V_{s} after n energy harvesting cycles for double charge pump circuit can be derived as

$$V_{\mathrm{s,n}} = V_{\mathrm{res}}[(1 - \frac{C_{\mathrm{max}}}{C_{\mathrm{min}}})(\frac{C_{\mathrm{s}}}{C_{\mathrm{min}} + C_{\mathrm{s}}})^{2n} + \frac{C_{\mathrm{max}}}{C_{\mathrm{min}}}] \tag{3.11}$$

It is clear that equation (3.10) can be applied to calculate the saturation value of V_{s} in this circuit topology also.

To illustrate the operation of the double charge pump integrated with the trans-

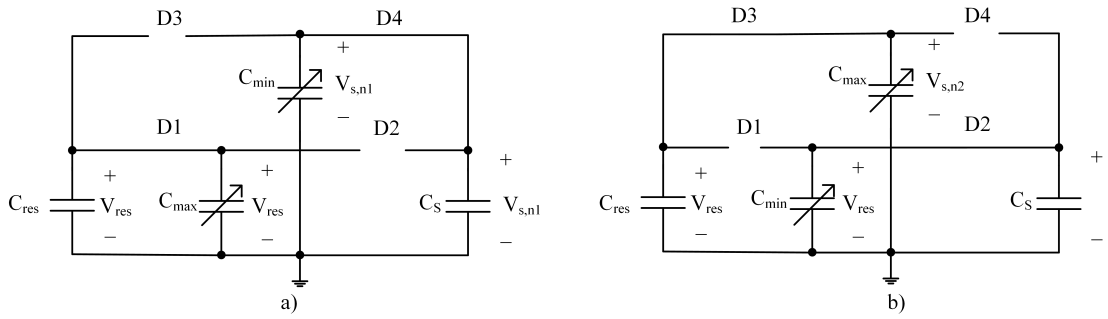

Figure 3-9: *a*) Start of first half of the cycle *b*) Start of second half of the cycle

ducer, the currents flowing through the diodes are observed and displayed as in Figure 3-10. The simulation denotes that during the first half of the cycle, the diodes $D1$ and $D4$ conduct while in the second half of the cycle, the diodes $D2$ and $D3$ conduct instead. This result is in agreement with what is just described above. It is also noticed that there are time intervals during that none diodes conduct. This is because the diodes are non-ideal and need time to be forward biased.

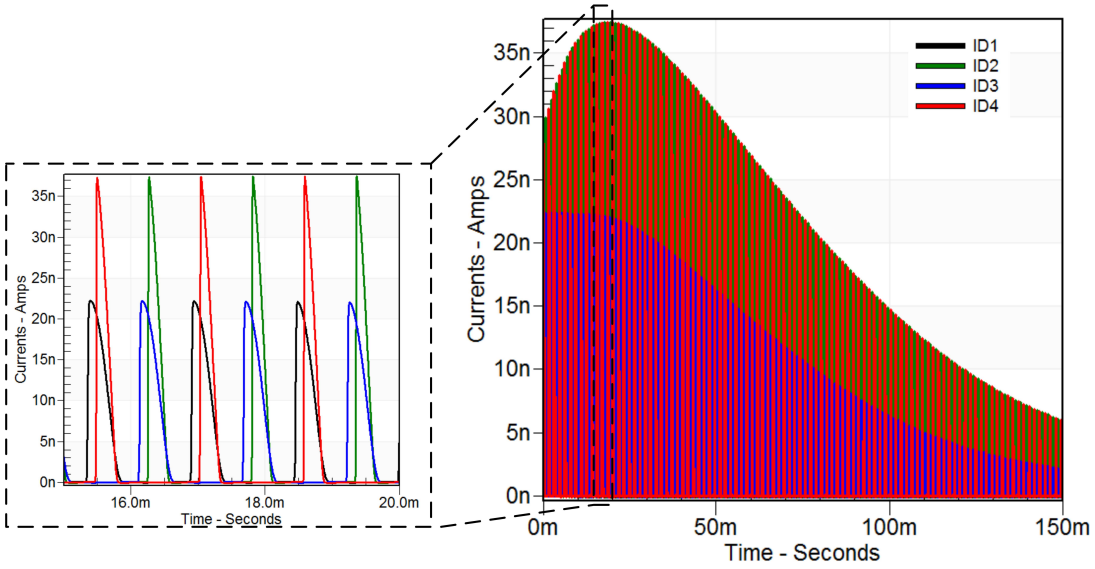

Figure 3-10: Waveforms of currents passing through the diodes in double charge pump circuit

Figure 3-11 demonstrates the behaviour of voltages across capacitors C_{res}, $C_{\text{var1,2}}$ and C_{s}. It is shown that these voltage waveforms behave as predicted. Since the capacitances of variable capacitors vary, voltages across them oscillate. During con-

version process, the charge is pumped from C_{res} into C_{s} through the variation of C_{var}, which causes V_{s} to increase and V_{res} to drop. However, as $C_{\text{res}} \gg C_{\text{var}}$, V_{res} does not decrease so much and can be considered as constant voltage. The increase of V_{s} reduced over time because the higher voltage across C_{s}, the more obstacle in placing additional charge on C_{var}. The theoretical saturation value of V_{s} is calculated from

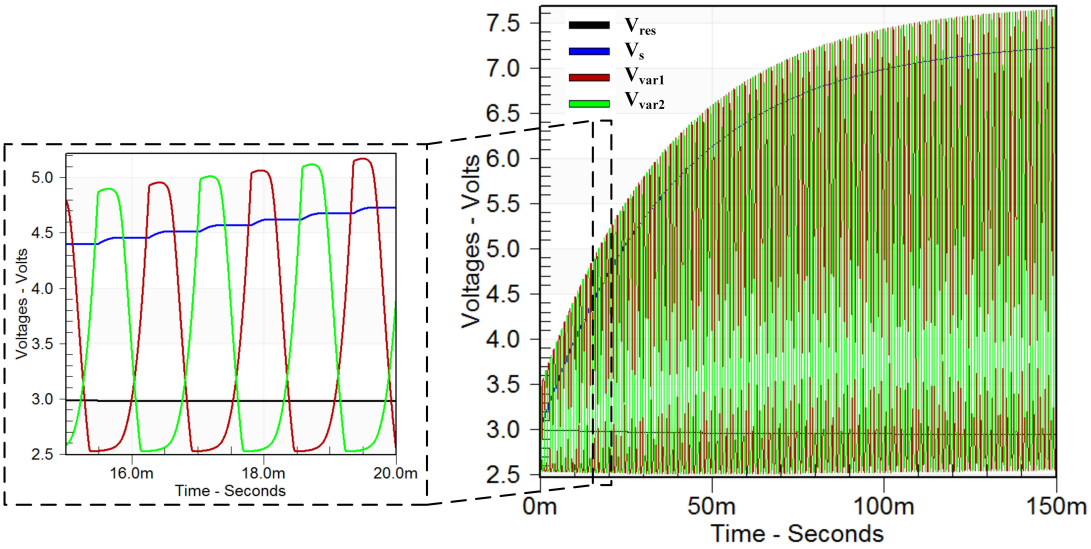

Figure 3-11: Voltage waveforms for double charge pump circuit

equation (3.10)

$$V_{\text{s,sat}} = \frac{C_{\text{max}}}{C_{\text{min}}} V_{\text{res}} = \frac{6.456 \text{ pF}}{2.144 \text{ pF}} \times 3 \text{ V} = 9 \text{ V} \tag{3.12}$$

Figure 3-12 plots the V_{s} waveform for double charge pump circuit over a long period of time. It indicates that saturation value of V_{s} is about 7.65 V which is lower than the theoretical one. The difference here is because when deriving the formula for saturation storage voltage, the diode is assumed to be ideal for simplicity. In fact, the forward bias voltage drop of the diodes should be taken into account.

When considering current and voltage waveforms for double charge pump circuit in the same time axis, it is clear that V_{s} increases whenever there is current passing through $D2$ or $D4$. Otherwise, this voltage remains unchanged. This is reasonable since the charge is only transferred into C_{s} when $D2$ or $D4$ conducts. It is also noticed that when V_{s} ramps up, the conducted currents through $D2$ and $D4$ decrease,

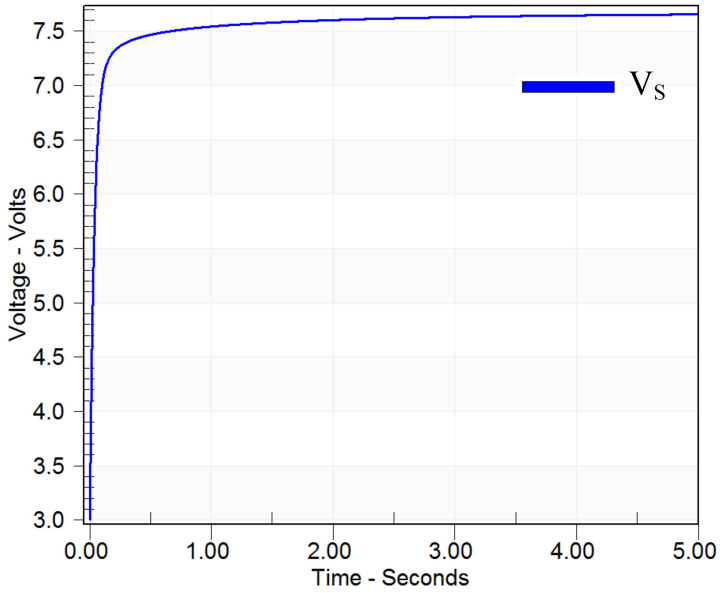

Figure 3-12: Waveform of V_s for double charge pump circuit over a long period of time

meaning that less charge is transferred into C_s.

To estimate the generated power, the net energy is calculated. The change in stored energy for any capacitor according to the change in voltage is

$$\triangle W = \frac{1}{2}C(V_1^2 - V_0^2) \tag{3.13}$$

where V_0 and V_1 are voltages across capacitor C at $t = 0$ and $t = t_1$ respectively

During the first 30 ms, V_{res} drops from 3 V to 2.974 V while V_s increases from 3 V to 5.32 V. Using formula (3.13), the net energy obtained is

$$\begin{aligned} \triangle W &= \frac{1}{2}C_{res}(V_{res1}^2 - V_{res0}^2) + \frac{1}{2}C_s(V_{s1}^2 - V_{s0}^2) \\ &= \frac{1}{2} \times 10^{-8}\ \text{F}\ (2.974^2\ \text{V}^2 - 3^2\ \text{V}^2) + \frac{1}{2} \times 110 \times 10^{-12}\ \text{F}\ (5.32^2\ \text{V}^2 - 3^2\ \text{V}^2) \\ &= 0.285\ \text{nJ} \end{aligned} \tag{3.14}$$

The net energy is positive, meaning that the system can generate the power from vibrational energy.

3.5 Double charge pump with flyback path

Next, flyback path element is connected to the double charge pump part. One limitation of the double charge pump without flyback path is that V_s keeps rising til the saturation value. At that time, the charge can not be pumped from C_{res} into C_s anymore. In order to prevent V_s from saturation, a flyback circuitry section is added as feedback circuit to power the load and recharge C_{res}, which enables the next conversion cycle as shown in Figure 3-13.

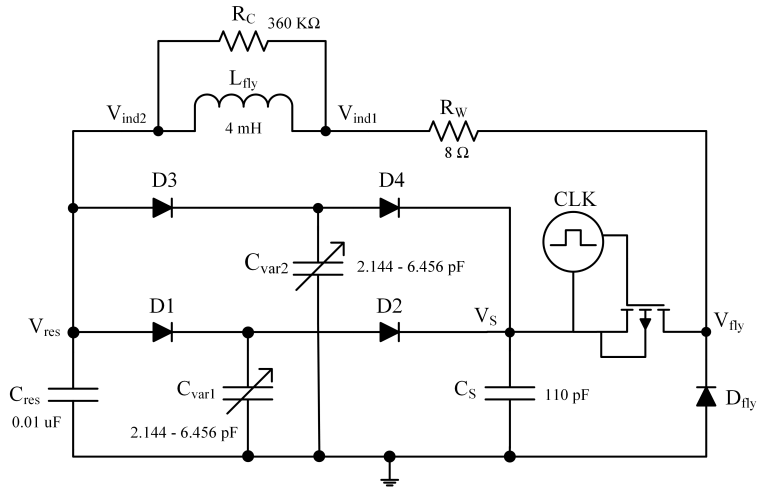

Figure 3-13: Double charge pump circuit with flyback path under external control clock

The flyback path consists of a MOSFET switch, a freewheeling diode D_{fly} and a real model of an inductor L_{fly}. The MOSFET plays a significantly important role in initiating the energy flyback whenever V_s increases to a threshold value. When the switch turns on, the current through L_{fly} ramps up and the energy is accumulated into the inductor. After a certain time, the switch turns off, leaving the inductor to commutate to the freewheeling diode. Consequently, the energy is transferred back to C_{res} until the diode D_{fly} turns off due to zero current through. At the first attempt, an external clock is connected to the gate of the MOSFET switch to control its on/off state for simplicity. In this topology, core loss R_C and winding loss R_W of L_{fly} are taken into account, choosing R_C=360 KΩ, R_W=8 Ω and L=4 mH.

To avoid effect of charge injection, the clock pulse at the gate of the MOSFET

switch should be referenced to the drain. The clock parameters in simulation are given in Table 3.3.

Table 3.3: Parameters of external control clock

Parameters	**Value**
High Voltage	3 V
Low Voltage	0 V
Rise time	5 ns
Fall time	5 ns
Clock frequency	25 Hz
Duty cycle	225×10^{-5} %

Figure 3-14 shows V_{res} waveform for double charge pump circuit with flyback path under external control clock. It is observed that V_{res} initially drops since the charge on C_{res} is transferred to C_{var} to start the conversion process. After couple cycles of vibration, the switch is turned on, pushing the charge on C_{s} back to C_{res} through fly-back path, resulting in an increase in V_{res}. Once stored energy in C_{s} is delivered to C_{res} successfully, the switch is turned off and the process repeats. Consequently, the charge is built up on C_{res} over time. For example, during the first 1s, the harvested energy and corresponding power on C_{res} can be calculated as follows.

$$\triangle W_{\text{har}} = \frac{1}{2} C_{\text{res}} (V_{\text{res1}}^2 - V_{\text{res0}}^2) = \frac{1}{2} \times 10^{-8} \text{ F } (3.2^2 \text{ V}^2 - 3^2 \text{ V}^2) = 6.2 \text{ nJ} \quad (3.15)$$

$$P_{\text{har}} = \triangle W_{\text{har}} / \triangle t = 6.2 \text{ nJ} / 1 \text{ s} = 6.2 \text{ nW} \quad (3.16)$$

Figure 3-15 and Figure 3-16 plot the voltages across capacitors and currents through diodes respectively for circuit topology in Figure 3-13.

As can be seen from Figure 3-15, V_{s} behaves as expected wherein it increases over time due to the charge built up on C_{s} after every cycle of vibration until the switch turns on. At that moment, this voltage drops due to the discharge process through L_{fly}. In terms of the current, Figure 3-16 illustrates that by using the flyback path, the peaks of conducted currents passing through the diodes are prevented from

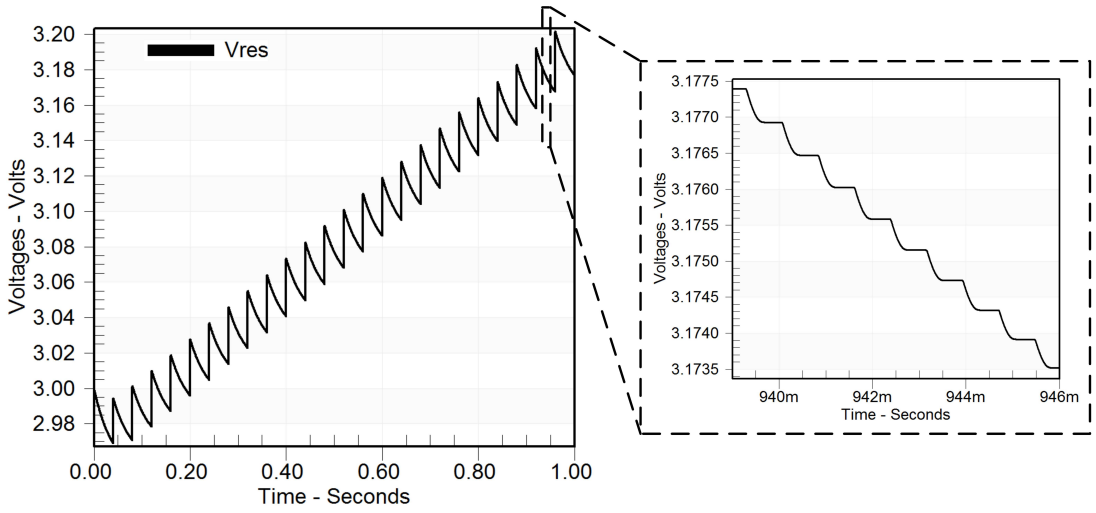

Figure 3-14: Waveform of V_{res} for double charge pump circuit with flyback path under external control clock

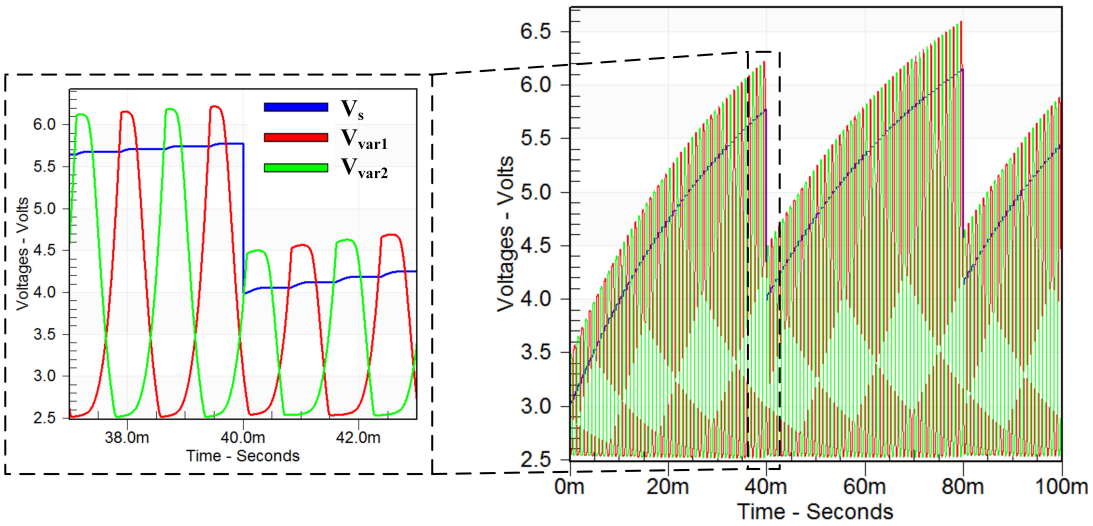

Figure 3-15: Voltages across capacitors for double charge pump circuit with flyback path under external control clock

continuously decreasing. It is also attractive to know the effect of switching operation on harvested power. The harvested power on C_{res} under different clock parameter sets are thus observed as shown in Table 3.4.

It is apparent from the results that not in all the cases, the mechanical energy can be injected successfully into the circuit. Depending on the clock parameters, the harvested energy can be higher, lower or even negative. If the clock frequency is too high, the switch is turned on when the charge built up on C_{s} is still low, resulting

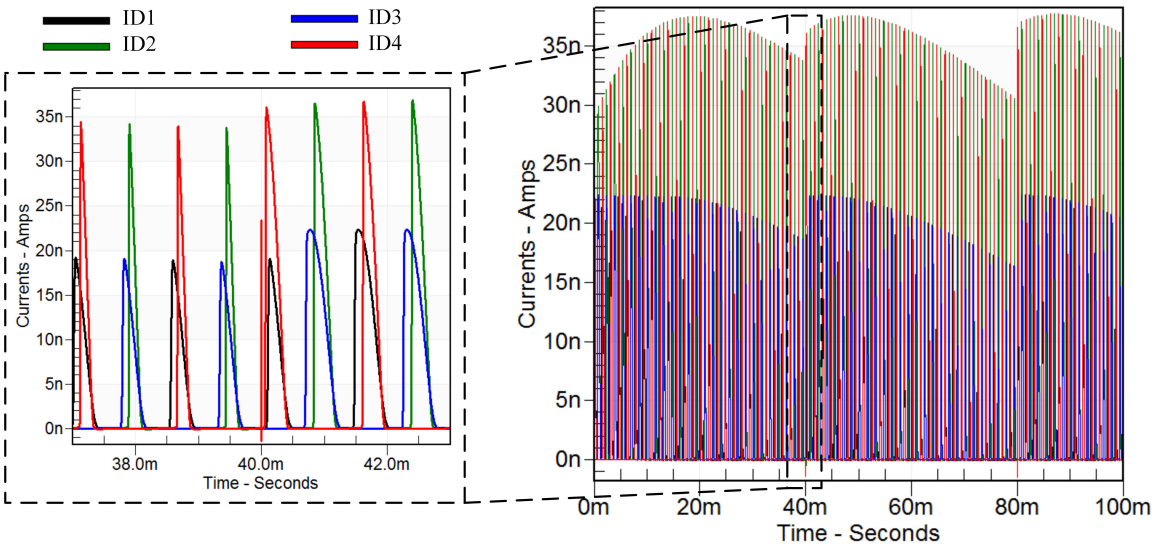

Figure 3-16: Currents flowing through diodes for double charge pump circuit with flyback path under external control clock

Table 3.4: Harvested power on V_{res} for circuit topology in Figure 3-13 under different clock parameter sets

Frequency f_{clk}	**Duty cycle D**	$V_{\text{res}}(t=0)$	$V_{\text{res}}(t=1s)$	**Harvested power** P_{har}
100 Hz	225×10^{-5} %	3 V	3.13 V	3.98 nW
10 Hz	225×10^{-5} %	3 V	3.18 V	5.56 nW
25 Hz	225×10^{-5} %	3 V	3.2 V	6.20 nW
25 Hz	25×10^{-5} %	3 V	2.97 V	-0.90 nW

lower harvested power. If the duty cycle is too low, the switch is turned off before all the charge is transferred to the inductor, meaning that less power harvested. This confirms the fact that there should be optimal switching time so that the harvested energy is maximum. Next parts focus on determining these optimal values.

3.6 Switching time optimization

In previous section, an external clock is employed to control the operation of the switch which has effect on harvested power. This section discusses an approach of using electronic circuit to control the switch. The main idea is to build an autonomous

circuit without existence of external control signals. The block diagram of circuit topology is presented in Figure 3-17.

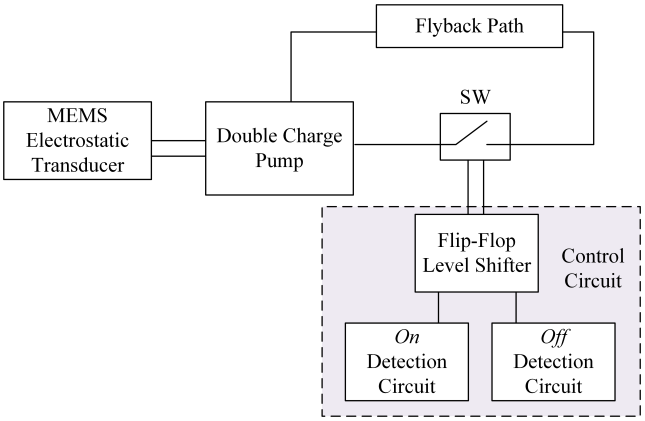

Figure 3-17: Block diagram of circuit topology with detail of control block

The control block consists of three main elements which are flip-flop level shifter, *on* detection circuit and *off* detection circuit. Each element is described in detail as follows.

3.6.1 Flip-flop level shifter

A flip-flop is integrated into the circuit and works as a memory element. It holds the switch state right after receiving the *on* or *off* signal at the inputs. For circuit with double charge pump and flyback path, it is noticed that voltage levels at drain and source of MOSFET switch are high. To enable or disable this switch using input signals at low voltage level, a level shifter is needed. Dudka *et al.* [55] proposed a flip-flop level shifter (see Figure 3-18) that fulfils these requirements and has a zero static power consumption.

The circuit receives pulses *on* and *off* at the input stage to open and close MOSFET switch at the output stage. The flip-flop consists of two state-holding capacitors C_1, C_2 and two high voltage pull-up transistors M_{P4}, M_{P5}. MOS diodes M_{P1}-M_{P3} are used to limit the voltage drop across the capacitors. Two switches M_{P6}-M_{P7}, M_{P8}-M_{P9} are used to prevent the capacitors from discharge and to keep the circuit stable. The operation of the flip-flop level shifter is described as follows. At first,

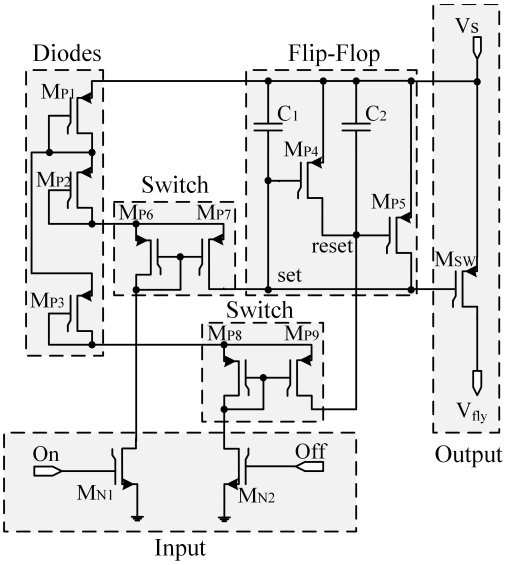

Figure 3-18: Flip-flop level shifter [55]

when the pulses *on* and *off* do not trigger, the voltage levels at set node and reset node are equal to V_s and V_s - 3 V respectively. When pulse *on* triggers, C_1 is charged. M_{P4} is turned on, which discharges C_2 and thus turns M_{P5} off. As a result, voltage levels at set node and reset node are swapped, which turns on the MOSFET switch. Things happen similarly when pulse *off* triggers.

The integration of the flip-flop level shifter into the main circuit is shown in Figure 3-19. The external clock is now replaced by the flip-flop level shifter controlled by external pulses *on* and *off*. Figure 3-20 shows V_s waveform for this topology. It demonstrates that when pulse *on* is high, V_s decreases, implying the *on* state of MOSFET switch. This voltage increases again when pulse *off* is high, indicating that the switch is turned off.

3.6.2 Circuit detecting *off* event

The purpose of the *off* detection circuit is to detect the optimal moment to turn off the switch. Output from this circuit is then used to replace for the external *off* signal at the input of the flip-flop level shifter. The following circuit analysis helps to determine this optimal moment.

Consider double charge pump circuit with flyback path when the switch is turned

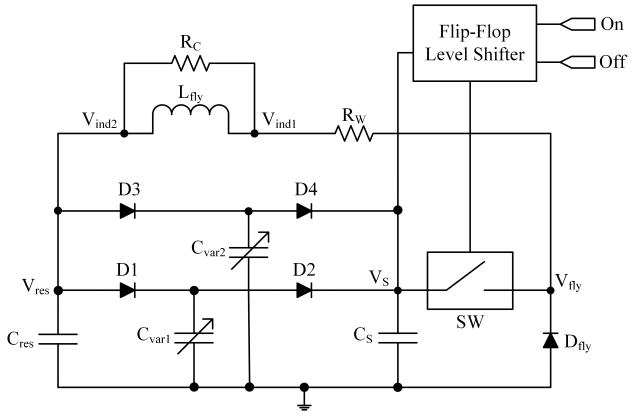

Figure 3-19: Integration of the flip-flop level shifter controlled by external signals into the circuit

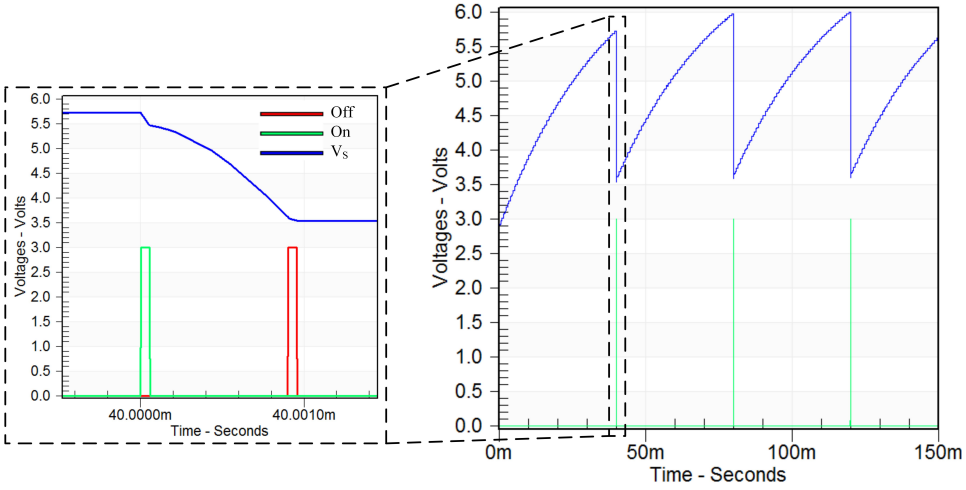

Figure 3-20: Waveform of V_s for circuit topology shown in Figure 3-19

on. At that time, C_{var1} and C_{var2} are either connected to C_s or C_{res} but since their capacitances are so small, their contribution can be ignored. The effects of core resistance and wire resistance of the inductor to the circuit are also neglected. The resulting equivalent circuit then comprises C_s , C_{res} and L_{fly} in series. As $C_{res} \gg C_s$, V_{res} is considered to be constant. Thus, the differential equation of the inductor current $i_L(t)$ can be derived as

$$\frac{1}{C_s}\int_0^{t_{on}} i_{L_{fly}}(t)dt - V_{s0} + L_{fly}\frac{di_{L_{fly}}(t)}{dt} + V_{res} = 0 \tag{3.17}$$

where V_{s0} is V_s at the moment the switch is turned on, t_{on} is the on-time duration of the switch

The current through and the charge on L_{fly} can be deduced from (3.17) using Laplace Transform

$$i_{L_{fly}}(t) = \frac{V_{s0} - V_{res}}{L_{fly}} \cos\left(\frac{1}{\sqrt{L_{fly}C_s}}t\right) \tag{3.18}$$

$$q_{L_{fly}}(t) = (V_{s0} - V_{res})\sqrt{\frac{C_s}{L_{fly}}} \sin\left(\frac{1}{\sqrt{L_{fly}C_s}}t\right) \tag{3.19}$$

Due to the on/off action of the switch, energy built up on V_s is stored in L_{fly} before being transferred to C_{res} through the charge and discharge process of L_{fly}. To maximize the charge delivered, the switch should be turned off once all the charge is transferred into L_{fly}. This occurs when the current through L_{fly} reaches maximum value. In other words, the switch should be turned off when voltage across L_{fly} is equal to zero. To detect this moment, the similarity of voltage levels at two terminals of L_{fly} of the switch is observed using bump circuit.

Bump circuit

Bump circuit [56] is the circuit that computes the similarity and dissimilarity of two voltage signals. The output current of bump circuit is large when two input voltages are close to each other. The bump circuit comprises a differential pair and a current correlator as shown in Figure 3-21a). The input is the differential voltage $\triangle V = V_1 - V_2$ and the output is the current I_{out}. The operation of the circuit is described as follows. When the differential input $\triangle V$ is near zero, the bias current I_b set by the bias voltage V_b will be divided equally between two legs of differential pair, I_1 and I_2. These two currents are mirrored to the currents through Q_2 and Q_3 respectively by current mirrors. As a result, output current is forced to reach its maximum value. If $\triangle V$ is different from zero, the current in one of two legs will shut off and the output current will be zero. In order to get the voltage signal from I_{out}, an additional mosfet Q8 connected between output of the bump circuit and the ground

is used. This mosfet is biased by V_{L}. The output voltage V_{out} is either equal to V_{dd} or zero depending on the value of I_{out}. The behaviour of output current I_{out} is displayed in Figure 3-21*b*).

The sensitivity of the bump circuit can be adjusted by balancing the current of the bump circuit through Q_7 and the bias current through Q_8.Compared to traditional opamp comparator which generates output signal at positive or negative level, the bump circuit results in an output voltage of high or zero level. The output from bump circuit is thus suitable to be used as a pulse to trigger an event. The proposed circuit takes this advantage by choosing bump circuit to detect similarity of two signals.

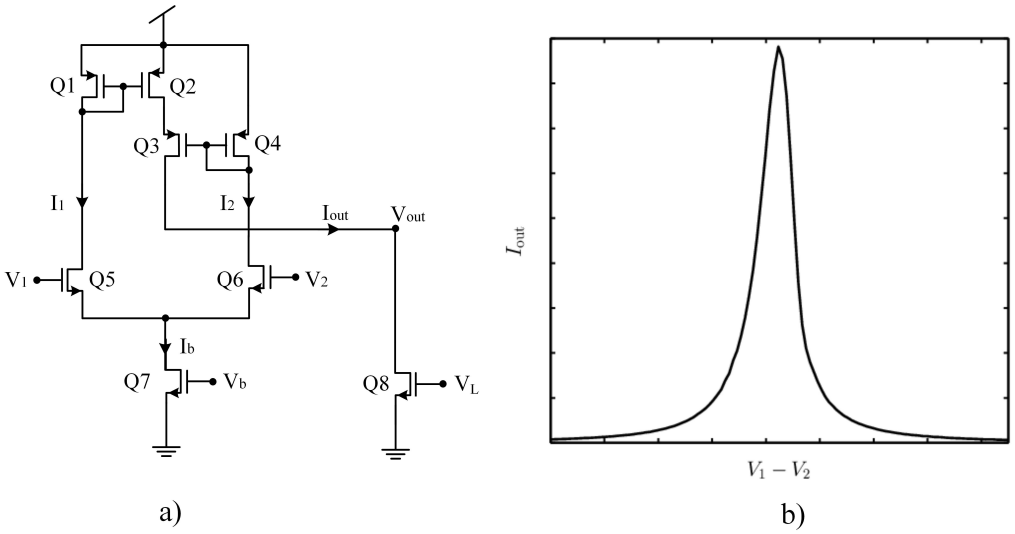

Figure 3-21: *a*)Schematic of bump circuit, *b*)Output waveform of bump circuit

Figure 3-22 shows the implementation of the bump circuit to detect *off* event. The bump circuit is named as bump circuit 1 which receives V_{ind1} and V_{ind2} as two inputs and generates output voltage V_{out1}. The waveform of V_{out1} is displayed in Figure 3-23. It demonstrates that V_{out1} is high when two inputs are equal. Otherwise, V_{out1} is low. The *off* event happens when V_{out1} is high during the on-time of the switch. Thus, an enable/disable signal is added to activate the bump circuit during the on-time of the switch only. This can be achieved by connecting an extra MOSFET Q9 in series with bias MOSFET Q7 as shown in Figure 3-24. MOSFET Q9 is then controlled by a clock signal EN that is on and off synchronously with the switch state. The modified

bump circuit is named as bump circuit 1*.

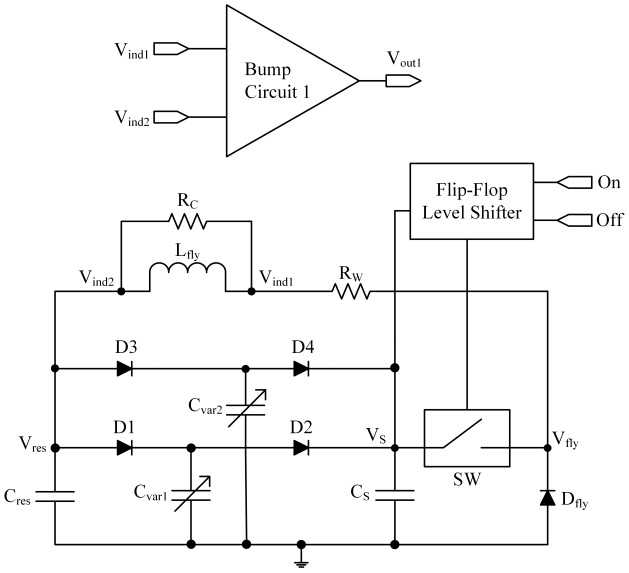

Figure 3-22: Implementation of the bump circuit in the proposed circuit to monitor the similarity of voltages at two terminals of L_{fly}

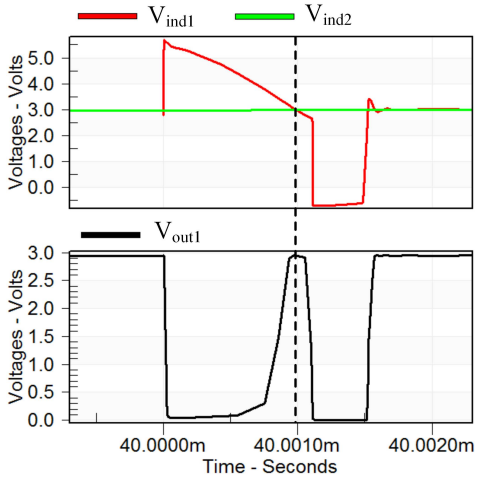

Figure 3-23: Output waveform of bump circuit when computing the similarity of voltages at two terminals of L_{fly}

SR latch

A SR latch circuit which holds the states of input pulses is utilized to generate the EN signal. The schematic of SR latch is illustrated in Figure 3-25. Its operation when S and R are connected to pulses *on* and *off* respectively is demonstrated in Figure 3-26.

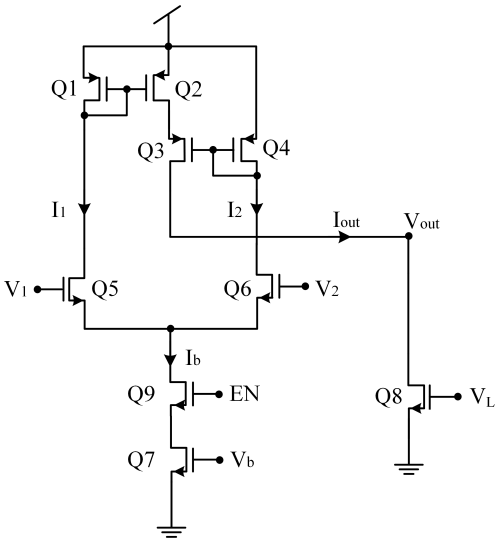

Figure 3-24: Bump circuit with enable/disable control input

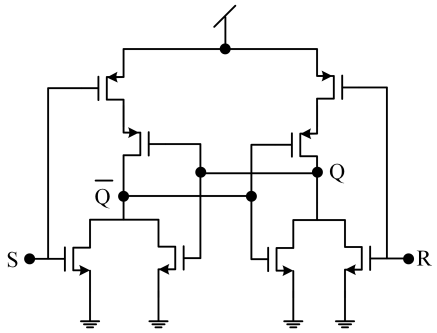

Figure 3-25: Schematic of SR Latch

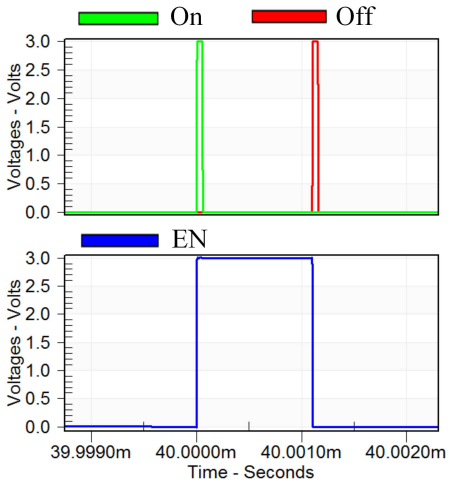

Figure 3-26: Inputs and corresponding output of the SR latch

Figure 3-27 shows the circuit topology which detects *off* event. $V_{\mathrm{out1}*}$ is the output from bump circuit 1*. The obtained $V_{\mathrm{out1}*}$ is sharpened by a buffer stage consisting of two inverters cascaded. Figure 3-28 plots the waveform of $V_{\mathrm{out1}*}$ and $V_{\mathrm{out1}*-\mathrm{buffer}}$. Compared to V_{out1} which is high whenever V_{ind1} is equal to V_{ind2}, $V_{\mathrm{out1}*}$ is high when these two voltages are equal during the enabled time only. It is also shown that waveform of $V_{\mathrm{out1}*-\mathrm{buffer}}$ is sharper than that of $V_{\mathrm{out1}*}$.

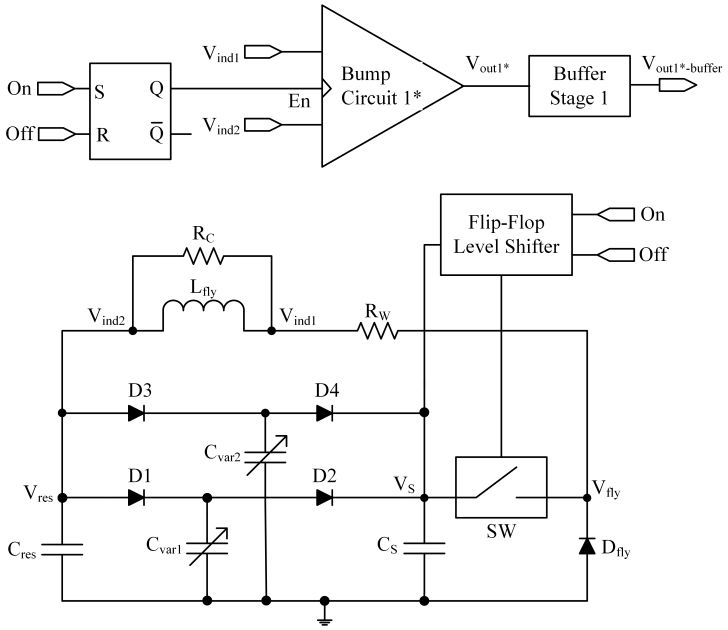

Figure 3-27: Block diagram of the circuit which detects *off* event

Output from buffer stage 1 is now used to replace for external pulse *off*, completing the *off* detection circuit as shown in Figure 3-29. The flip-flop level shifter and SR latch are now controlled by two signals. One is the external pulse *on*, the other is output from the *off* detection circuit. Next part discusses a circuit topology to remove the remaining external pulse.

3.6.3 Circuit detecting *on* event

The *on* detection circuit is used to generate the pulse triggering the moment the switch should be turned on. By using this sub-circuit, external pulse *on* can be eliminated. The *on* event is determined as follows.

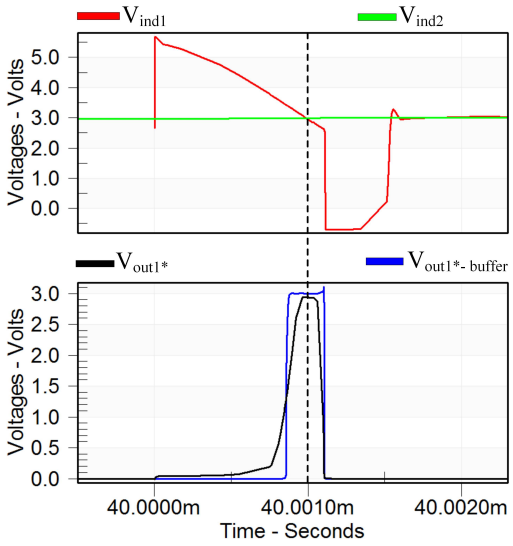

Figure 3-28: Waveform of$V_{\text{out1}*}$ and $V_{\text{out1}*-\text{buffer}}$

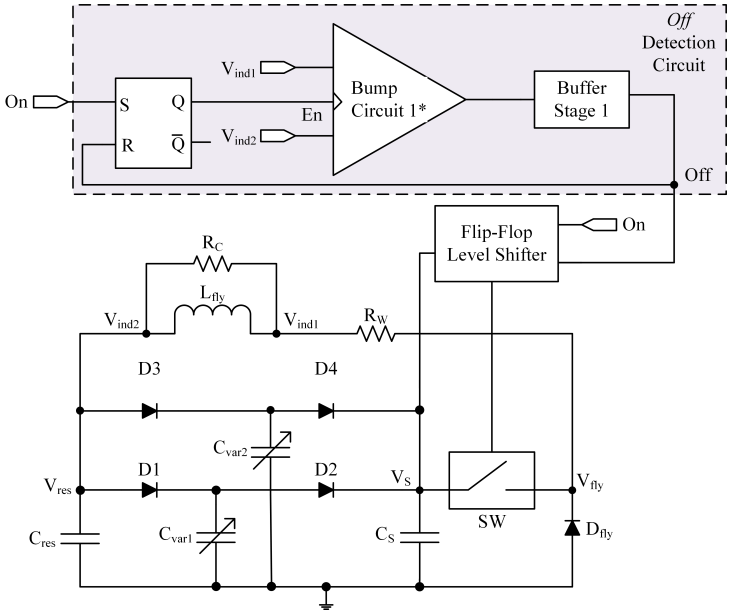

Figure 3-29: Integration of the *off* detection circuit to main circuit

Assume $V_{\text{s}} = V_{\text{res}} = V_0$ at startup ($t = 0$). Define $V_{\text{s}} = V_1$ ($t = t_1$) as the optimal V_{s} at which the switch should be turned on. The harvested energy during the period of time from t_0 to t_1 is [36]

$$\triangle W = \frac{1}{2} C_{\text{s}} \left(\frac{1 + C_{\text{s}}}{C_{\text{res}}}\right)(V_1 - V_{\text{res}}(t = t_1))^2 \tag{3.20}$$

Thus, the generated power can be calculated as

$$P = \frac{\triangle W}{n(V_1)T} \tag{3.21}$$

where $n(V_1)$ is the number of energy harvesting cycles needed for V_s to reach V_1 and T is the period of the variation. From equation (3.11) we have

$$n = \frac{1}{2}\log_{\frac{C_s}{C_{min}+C_s}} \frac{V_1/V_0 - C_{max}/C_{min}}{1 - C_{max}/C_{min}} \tag{3.22}$$

Substitute n into (3.21) and introduce $\theta = V_1/V_0$, $\alpha = C_{max}/C_{min}$, we have

$$P = H\frac{(1-\theta)^2}{\ln\frac{\theta-\alpha}{1-\alpha}} \tag{3.23}$$

where

$$H = \frac{C_s(1+\frac{C_s}{C_{res}})V_0^2}{T\log_{\frac{C_s}{C_{min}+C_s}} e} \tag{3.24}$$

It is obvious from (3.23) that for a given transducer with constant α, power is a function of variable θ. Thus, there is an optimal value of θ named as θ_{opt} at which the power is maximum. This value is the root θ of the derivative of power equation, which is

$$2\ln\frac{\theta-\alpha}{1-\alpha} = \frac{\theta-1}{\theta-\alpha} \tag{3.25}$$

Solving equation (3.25) with respect to $\alpha = \frac{C_{max}}{C_{min}} = \frac{6.456\text{ pF}}{2.144\text{ pF}} = 3.01$ results in $\theta_{opt} = 2.43$. Since $\theta = V_1/V_0$, the optimal value of V_s is larger than V_{res} by a factor of θ_{opt}. The switch should be turned on when V_s reaches the optimal value. To detect this event, V_s is first divided by θ_{opt}, then the bump circuit is used to trigger the moment when the obtained value is equal to V_{res}.

Capacitive divider

An approach to divide the voltage by a desired factor is the use of capacitive

divider. Capacitor C_s is replaced by two capacitors in series (C_1=153 pF, C_2=219 pF). The voltage level at the middle point of divider, V_{s-cap}, is then equal to V_s divided by 2.43. Figure 3-30 shows the integration of the *on* detection circuit and the *off* detection circuit to the main circuit. The bump circuit 2 computes similarity of V_{s-cap} and V_{res}. The output signal is made sharper by using buffer stage 2 consisting of four inverters cascaded. The obtained output is used to replace for external pulse *on* at the inputs of the flip-flop level shifter and SR latch. All the external control signals can be dismissed and the whole system is autonomous in controlling the switch to optimize harvested power.

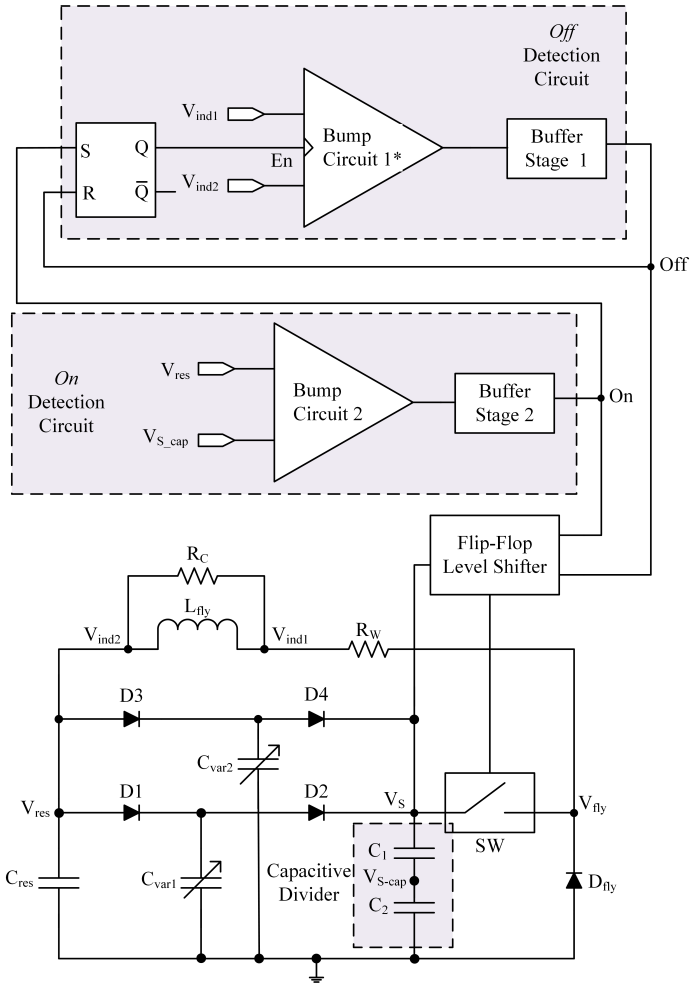

Figure 3-30: Integration of the *on* detection circuit and the *off* detection circuit to the main circuit using capacitive divider

Figure 3-31 plots the waveforms of V_{s-cap} and V_{res} in the same time axis. It is

obvious that the switch is turned on when V_{s-cap} ramps up to near V_{res}. The sensitivity of the bump circuit determines how close these two values are.

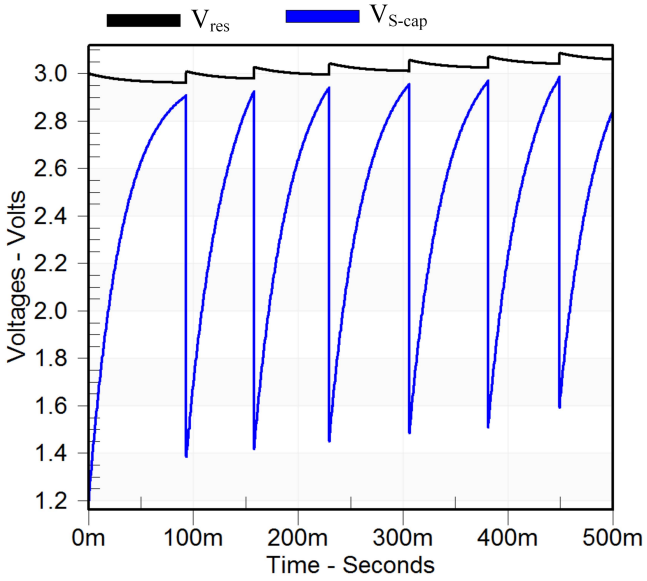

Figure 3-31: Output waveform of V_{s-cap} and V_{res} for the circuit topology shown in Figure 3-30

One drawback of capacitive divider approach is the problem with DC and operating point convergence when running simulation. A conductance is added for each capacitor which will effect the charge and discharge process of the capacitor over time.

Diode connected voltage divider

There are several other alternative techniques to implement voltage divider such as resistive divider, diode divider. Although the first approach gives higher accuracy, it consumes a lot of power and space which is unacceptable for integrated low power system. Thus, diode divider method is considered. A diagram of voltage divider using a set of diode connected MOSFETs is shown in Figure 3-32. As shown in the diagram, all the bodies of the transistors are connected to their source nodes, so that all the MOSFETs have identical bias conditions. The down scale ratio depends on the position of output voltage node.

Since voltage levels at the inputs of bump circuits increase over time due to charge built up on capacitors, it is worth to down scale all these voltages by the same ratio in order to sustain the operation of circuit over time. The chosen factor is 2 for instance.

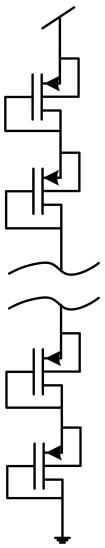

Figure 3-32: Diagram of diode connected voltage divider

Thus, V_{s} should be divided by $2.43 \times 2 = 4.86$. Others including V_{res}, V_{ind1}, V_{ind2} are divided by 2. Figure 3-33 shows the integration of the *on* detection circuit and the *off* detection circuit to the main circuit using diode connected voltage divider.

The output voltage and current of the bump circuit 2 is illustrated in Figure 3-34. It can be seen that output voltage ramps up gradually when the two inputs are going to close to each other until it reaches 733.78 mV which is large enough to turn on the MOSFET of the buffer stage.

Figure 3-35 plots the waveform of V_{s} and V_{res} during the first 1s and corresponding ratio between them. It is obvious that the switch is turned on whenever this ratio reaches the value of 2.33 which is close to the ideal value of 2.43 as calculated in previous part. The difference here is due to the sensitivity of the bump circuit.

Figure 3-36 displays the waveform of V_{res} over a long period of time. It is shown that V_{res} increases from 3V to 6.1V during 5s. Thus, it is demonstrated that this circuit topology can work properly as expected in terms of controlling the switch autonomously. To evaluate the performance of proposed circuit in terms of power consumption, more analyses will be carried out.

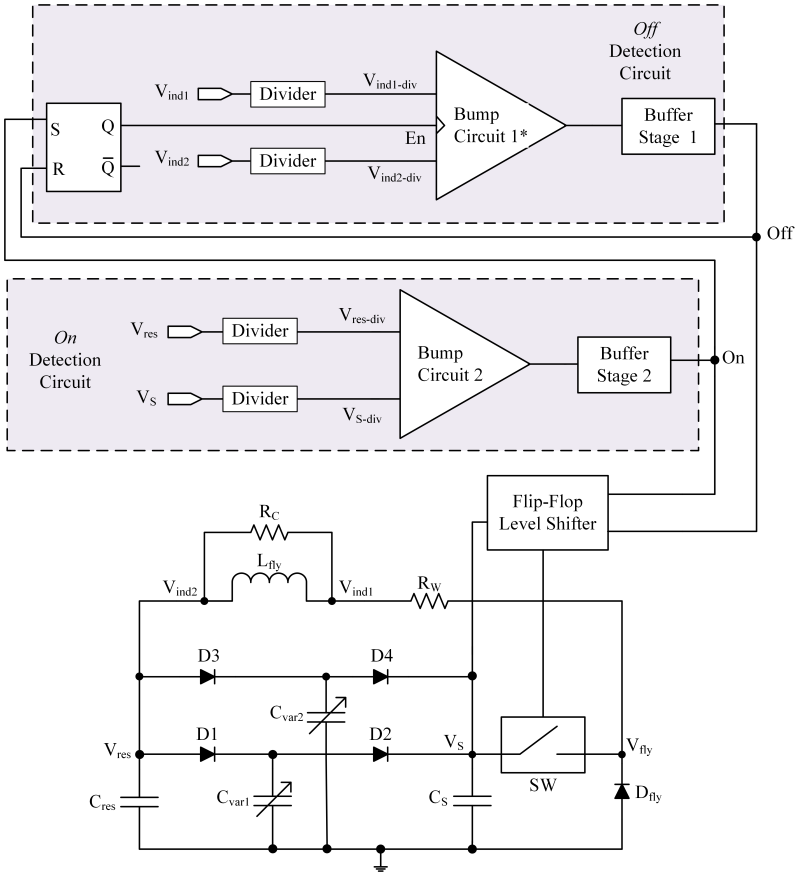

Figure 3-33: Integration of the *on* detection circuit and the *off* detection circuit to the main circuit using diode connected voltage divider

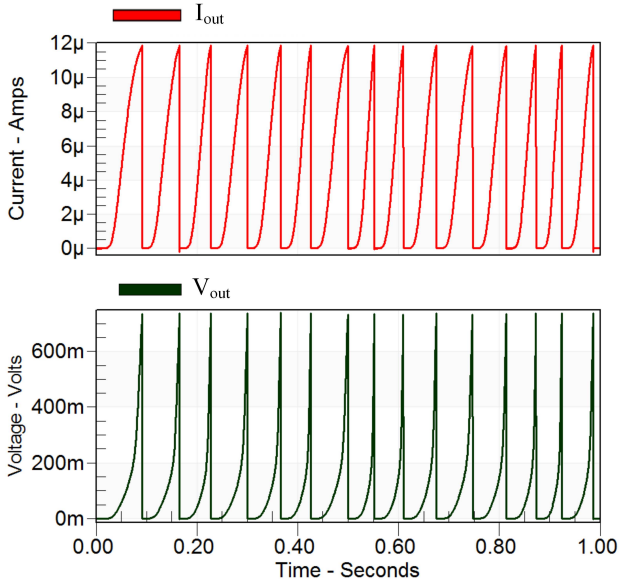

Figure 3-34: Waveform of output current and voltage of the bump circuit 2

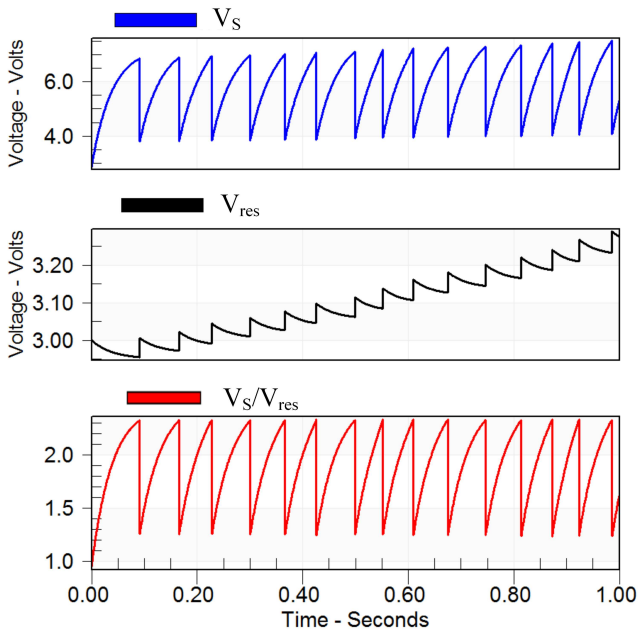

Figure 3-35: Waveform of V_s and V_{res} corresponding ratio between them for circuit topology shown in Figure 3-33

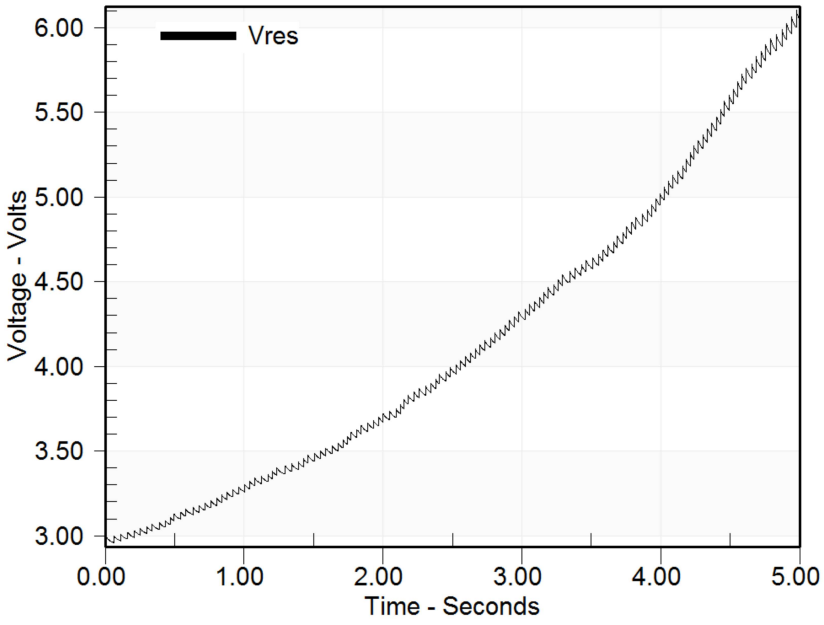

Figure 3-36: Waveform of V_{res} for circuit topology shown in Figure 3-33 over a long period of time

3.7 Consumed-power estimation and optimization

3.7.1 Power consumption

One of the most important criteria that needs to be considered when designing electronic interface circuit for energy harvesting is power consumption. Energy consumed by the control circuit must satisfy two requirements:

• Power consumption should be less than power generated from the transducer so that net energy can be obtained.

• The source of energy needs to be extracted directly from the harvested energy.

This part focuses on power consumption of autonomous circuit proposed in Figure 3-33. The circuit is then optimized to fulfil these two requirements.

Aside from bias voltages V_{b} and V_{L} for bump circuits, the control circuit needs external supply voltages to sustain its operation as shown in Figure 3-37. Power consumption on each supply voltage can be estimated during the time 1s as shown in Table 3.5.

Table 3.5: Power consumption on each supply voltage

Voltage supplier	**Voltage (V)**	**Power consumption (nW)**
V_{dd1} (Bump circuit 1*)	3.5	96.45
V_{dd2} (Bump circuit 2)	3.5	96.6×10^3
V_{dd3} (Buffer stage 1)	3	269.78
V_{dd4} (Buffer stage 2)	3	4.77×10^3
V_{dd5} (SR latch)	3	501.6

It can be seen that power consumption on bump circuit 2 and buffer stage 2 seems to overwhelm the rests. The reason for this is that while the bump circuit 1 is only enabled during a short period of time, the bump circuit 2 is activated all the time to monitor the state of the circuit. Figure 3-38 shows waveform of current out from V_{dd2}. It is clear that there is always a current of at least 23 μA consumed by bump circuit 2. This current increases when two inputs are close to each other. Since two inputs have ladder waveform and change slowly, the output voltage takes a transition time before reaching the trigger value. As a result, the transition time of inverters at

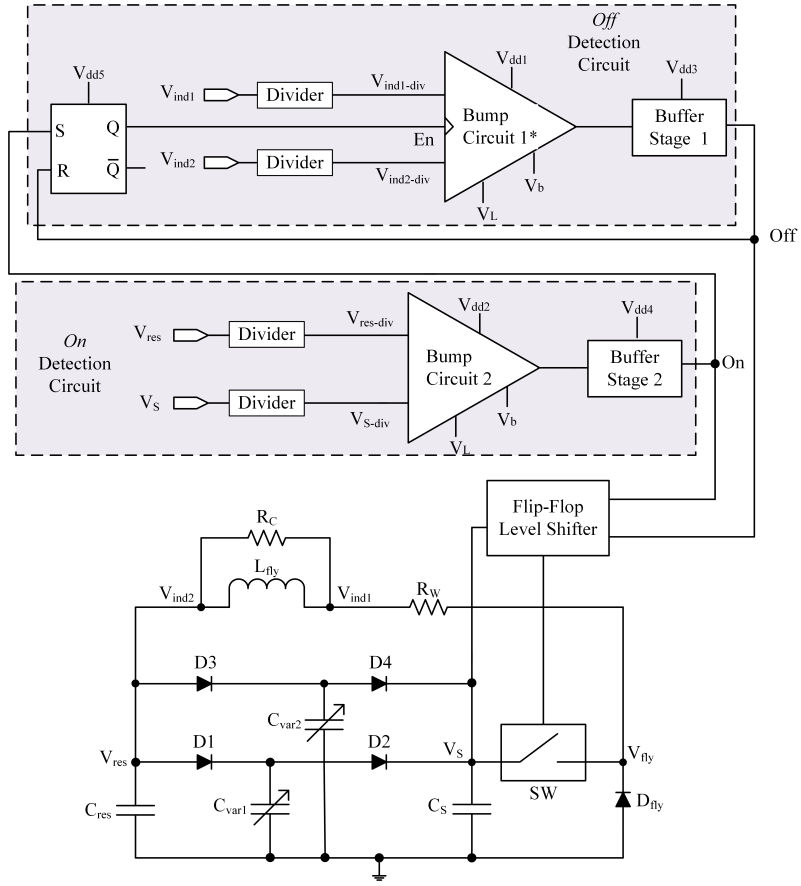

Figure 3-37: Block diagram of the proposed circuit with indicated external voltage supplies

buffer stage 2 is longer, which causes this block to consume the second highest power.

3.7.2 Elimination of external power supplies

The next attempt is to try to power each control block by energy from reservoir capacitor. This is done by replacing external power supplies by V_{res}. Table 3.6 shows the result of harvested power on C_{res} after step by step replacing each power supply. At this stage, the divided voltages from V_{res} which are equal to V_{b} and V_{L} will be used to bias bump circuits.

It can be seen from Table 3.6 that after replacing power supply for bump circuit 1* (V_{dd1}), harvested power on C_{res} is positive, meaning that V_{res} can power bump circuit 1*. When replacing more power supplies which are V_{dd3} and V_{dd5}, harvested

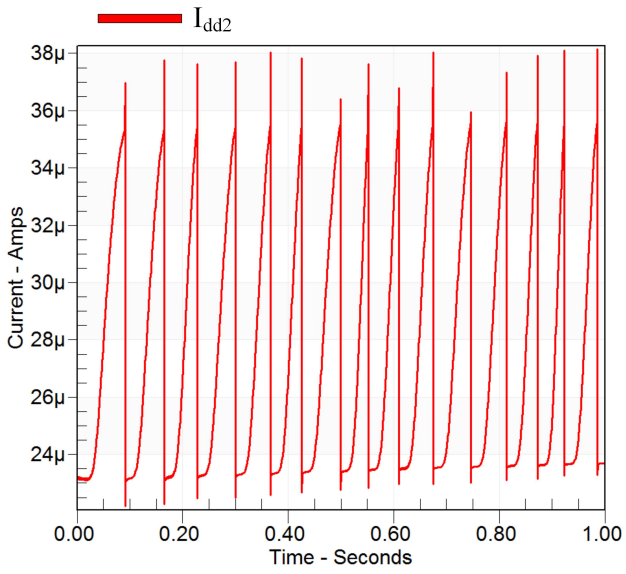

Figure 3-38: Current out from V_{dd2}

Table 3.6: Harvested power on C_{res} after replacing power supplies step by step

Removed power supplies	$V_{\text{res}}(t = 1s)$ (V)	**Harvested power (nW)**
V_{dd1}	3.262	8.2
V_{dd1}, V_{dd3}	3.2583	8.083
V_{dd1}, V_{dd3}, V_{dd5}	3.258	8.073
V_{dd1}, V_{dd3}, V_{dd5}, V_{dd4}	2.03	-24.4

power on C_{res} is reduced but still positive. This demonstrates that V_{res} now can power the bump circuit 1*, buffer stage 1 and SR latch. When continuing to replace V_{dd4}, harvested power is negative, indicating that V_{res} is fail to power the buffer stage 2. When trying to replace V_{dd2} by connecting V_{res} to power the bump circuit 2, V_{res} drops to zero right away and the circuit stops working. This is because the bump circuit 2 drives a large current from V_{res}.

In summary, for current circuit topology, V_{res} can power the bump circuit 1*, buffer stage 1 and SR latch. While V_{dd2} and V_{dd4} are still required to power the bump circuit 2 and buffer stage 2. Next parts discuss some modifications to eliminate these remaining ones.

3.7.3 Clocking technique

The bump circuit 2 consumes the most power since it is activated all the time. In addition, its long time transition from low voltage level to high voltage level at the output also causes the following circuit block which is buffer stage 2 consume more power. A clock should be integrated into the bump circuit 2 in order to reduce the enabled time of this block, resulting in less power consumption. To apply this approach, bias voltage V_{b} for the bump circuit 2 is replaced by a clock pulse with low clocking frequency compared to vibration frequency and small pulse width. By doing that, the monitoring just takes place after several vibration cycles and during a short period of time.

With a clock pulse width of as small as 0.5 μs the bump circuit still works well. Different clock frequencies with the same pulse width of 0.5 μs are applied to the circuit. Table 3.7 shows the power consumption of the bump circuit 2 and buffer stage 2 corresponding to different clock frequencies with the pulse width of 0.5 μs.

Table 3.7: Power consumption on V_{dd2} and V_{dd4} corresponding to different clock frequencies with the pulse width of 0.5 μs

Clock frequency (Hz)	**Power consumption on V_{dd2} (nW)**	**Power consumption on V_{dd4} (nW)**
200	308.94	417.05
100	206.2	388.7
50	158.14	354.7

For a clock frequency of 200 Hz, the power consumption on V_{dd2} can be reduced by a factor of 312 while this value is 11 for V_{dd4}. This is because in ordinary condition without clock, the bump circuit 2 consumes the energy during the whole operation time of the circuit while the buffer stage 2 just consumes the energy during a short period of time around trigger point. Thus, the use of the clock has a great impact on the power consumed by the bump circuit 2. It is clear that the smaller clock frequency, the lower power consumption due to less activation time.

3.7.4 Self-sustaining topology

With the implementation of the clock, a step of replacing V_{dd2} and V_{dd4} by V_{res} is performed. Figure 3-39 shows the harvested power on C_{res} corresponding to different clock frequencies with the pulse width of 0.5 μs for this step. The harvested power is positive when replacing V_{dd4} by V_{res} at clock frequencies of 100 Hz and 200 Hz only. This value is negative in other cases. Meaning that V_{res} can power buffer stage 2 at proper clock frequencies. When clock frequency is too high, power consumption of bump circuit 2 and buffer stage 2 is not decreased so much, which reduced harvested power. When clock frequency is too low, it might miss or capture the *on* moment wrongly, leading to lower harvested power. Thus, choosing clock frequency is a trade-off between power consumption and the sensitivity of the *on* detection circuit.

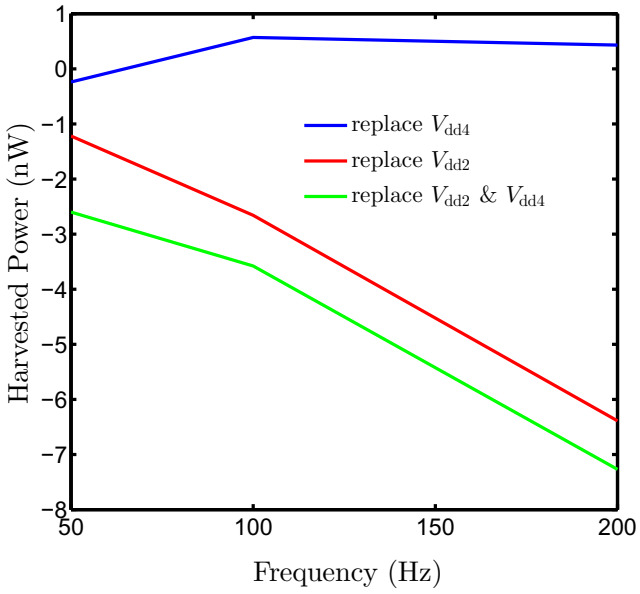

Figure 3-39: Harvested power on C_{res} corresponding to different clock frequencies with the pulse width of 0.5 μs when replacing V_{dd2} and V_{dd4} by V_{res}

It is noticed that there are several drawbacks of using the clock. That are the clock itself consumes the power and a low power clock generator is required.

3.7.5 Power enhancement

With the enhancement of the clock for the current circuit topology, it is still unable to power the bump circuit 2 from V_{res}. Therefore, adjustment on transducer parameters can be considered to see if this issue can be solved. One solution is to increase the ratio α between $C_{\max}$ and $C_{\min}$ of MEMS electrostatic transducer from $\alpha = 3.01$ to $\alpha = 4$ while keeping $C_{\min}$ constant. The new value of C_{DC} and C_{AC} are 5.39 pF and 3.234 pF respectively. The corresponding θ_{opt} is 3.15 as recalculated from 3.25. Under these changes, the ability of the circuit to self-power is tested. Table 3.8 presents the harvested power corresponding to different clock frequencies with the pulse width of 0.5 μs when removing all external power sources.

Table 3.8: Harvested power on C_{res} corresponding to different clock frequencies with the pulse width of 0.5 μs when replacing all external power supplies by V_{res} for the device with the ratio $\alpha = 4$

Clock frequency (Hz)	**Harvested power (nW)**
200	3.09
100	5.98
50	7.97

It is shown that the system can generate energy while powering control circuit. At a clock frequency of 50 Hz, the generated power can be up to 7.97 nW. With the adjustment in terms of transducer parameters, the control circuit is now powered from the harvested energy without the need of external power supplies except the requirement of clock generator.

3.8 Discussion

The first attempt to design a circuit that is autonomous in controlling the operation in order to achieve maximum power harvested have been done successfully. However, this control circuit still needs some external voltage supplies to power its control blocks. With the use of clocking technique, the number of required supply sources is reduced. The drawback of this approach is expressed in two points. Firstly, a clock

generator that consumes low power is required. Secondly, using the clock reduces the time monitoring the state of the circuit and thus affects the sensitivity of the bump circuit. Further modification can be made by combining this approach with the necessary adjustment of the device, which helps to eliminate all external voltage supplies. Increasing the ratio α between $C_{\max}$ and $C_{\min}$ results in increase of harvested power.

3.9 Voltage quadrupler circuit

This part presents an alternative topology to build interface circuit for MEMS overlap varying capacitive transducer.

3.9.1 Operation principle

The circuit topology is shown in Figure 3-40 where two variable capacitors are integrated into a voltage quadrupler circuit. An initial voltage placed on the variable capacitors can be multiplied infinitely through the series-connected rectifier-capacitor combination. The capacitors C2 and C3 charges to double the value of input voltage which results the output voltage across the series combination of these two capacitor a DC level of four times the value of input voltage.

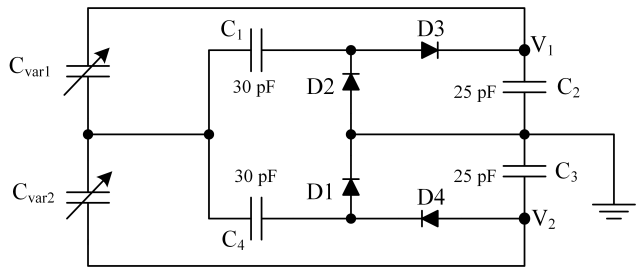

Figure 3-40: Voltage quadrupler circuit

3.9.2 Simulation results

An initial voltage of ±3V is placed on V_1 and V_2 to start the conversion process. With the values of capacitors C_1-C_4 shown in the figure 3-40 and the chosen value

of variable capacitors varying from 10 to 50 pF, the resulting simulation of output voltage at V1 and V2 can be seen in Figure 3-41

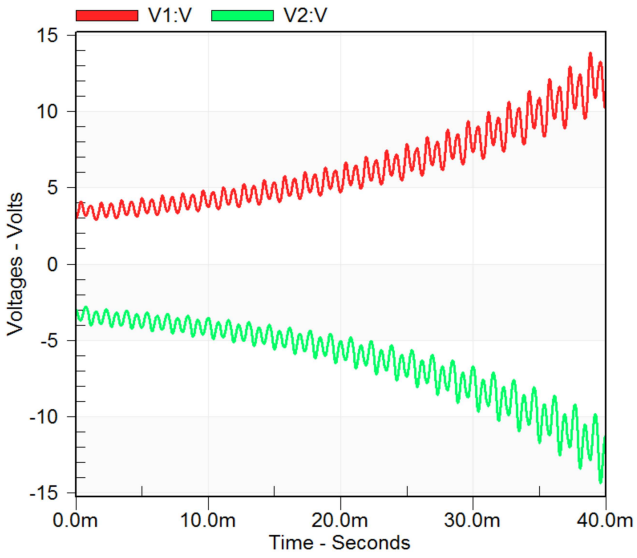

Figure 3-41: Output waveform of the voltage quadrupler circuit integrated with capacitive transducer with nominal capacitance of 30 pF

It is shown that the output voltage at V1 can reach to 14 V after 40 ms. When apply this circuit topology for transducer used in previous parts, there is no increase of voltage at the output.

3.9.3 Discussions

A major advantage of using this topology is that the output voltage is boosted to infinite value in principle without the need of complicated control circuit. However, this proposed circuit is just suitable for large variable capacitance. In addition, too high voltage can exceeds breakdown voltage of electronics components in the circuit. Also, the voltage level useful to power electronics applications is not that high. Thus, an additional circuit should be investigated to store and regulate output voltage from voltage quadrupler circuit so that it can be used.

Chapter 4

Conclusions

The thesis presented design and simulation of the power electronic interface circuit for MEMS electrostatic energy harvesters. The achieved goal of the circuit is to make the electrostatic harvester self-sustaining and generating electrical power from mechanical vibrations even the variable capacitance is in range of several pF. The circuit is built on ASIC platform, which is completely compatible to MEMS integration of chip-level system. The circuit includes three main features: double charge bump, flyback path and switch. There are two main challenges solved when designing the circuit controlling the switch.

The first is how to determine moments to open and close the switch so that harvested power can be maximized. The criteria for optimal switching time are presented in which the switch should be turned on when $V_{\mathrm{s}} > V_{\mathrm{res}}$ by a certain optimal value depending on the ratio between C_{max} and C_{min}. Then, the switch should be turned off when current through the flyback inductor reaches maximum value. By using the bump circuit, flip-flop level shifter and diode connected voltage divider, the circuit is proved to detect the *on* and *off* events accurately.

The second is how to power the control circuit from harvested energy. It is shown that with the current circuit configuration, the harvested power can be used to raise all control block except power supply for bump circuit 2 and buffer stage 2. Hence, the clocking technique is recommended to reduce power consumption of these blocks, which helps to eliminate remaining power supplies. A sufficient ratio α between C_{max}

and $C_{\min}$ is necessary to power all control blocks in the circuit. For example with the proposed switching technique, the harvesting system is fully self-sustaining and then generates power of 7.97 nW when increasing from $\alpha = 3.01$ to $\alpha = 4.00$.

A circuit configuration using voltage quadrupler is a promising alternative for the small-scale capacitive transducers. This topology requires less complicated circuit with a benefit that the output voltage is boosted to high level during a short period of time. For example, a value of 14 V is achieved from initial voltage 3 V after 40 ms for capacitance varying from 10 pF to 50 pF.

There remains a room for improving the circuit topology in future work. A design of ultra-low power clock generator for the bump circuit 2 should be considered to perfect the whole designed circuit. It is also interesting to realize the circuit design for complete energy harvesting system. Effort of applying the current circuit topology for other kinds of capacitive transducer is recommended. Finally, the transducer parameters and dimensions of electrical components in the circuit should be optimized to further enhance harvested power.

Bibliography

[1] A. Kansal and M. Srivastava, "An environmental energy harvesting framework for sensor networks," in *Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on*, pp. 481–486, Aug 2003.

[2] S. J. Roundy, *Energy Scavenging for Wireless Sensor Nodes with a Focus on Vibration to Electricity Conversion.* PhD thesis, The University Of California, Berkeley.

[3] J. Lee, Z. Chen, M. Allen, A. Rohatgi, and R. Ayra, "A high voltage solar cell array as an electrostatic mems power supply," in *Micro Electro Mechanical Systems, 1994, MEMS '94, Proceedings, IEEE Workshop on*, pp. 331–336, 1994.

[4] H.-C. Lu and T.-L. Shih, "Design of dc/dc boost converter with fnn solar cell maximum power point tracking controller," in *Industrial Electronics and Applications (ICIEA), 2010 the 5th IEEE Conference on*, pp. 802–807, June 2010.

[5] H. Bottner, "Thermoelectric micro devices: current state, recent developments and future aspects for technological progress and applications," in *Thermoelectrics, 2002. Proceedings ICT '02. Twenty-First International Conference on*, pp. 511–518, Aug 2002.

[6] R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill, and C. Caylor, "Energy harvesting for electronics with thermoelectric devices using nanoscale materials," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pp. 367–370, Dec 2007.

[7] P. Mitcheson, T. Green, E. Yeatman, and A. Holmes, "Architectures for vibration-driven micropower generators," *Microelectromechanical Systems, Journal of*, vol. 13, pp. 429–440, June 2004.

[8] S. P. Beeby, M. J. Tudor, and N. M. White, "Energy harvesting vibration sources for microsystems applications," *Measurement Science and Technology*, vol. 17, no. 12, p. R175, 2006.

[9] M. Lallart, *Small-Scale Energy Harvesting.* Intech, 2012.

[10] R. Van Schaik, R. Elfrink, V. Pop, and R. Vullers, "Energy harvesting for self powered sensor systems–case study: Vibration energy harvesting for intelligent

tireapplication," in *Proceedings of the 17th Workshop on Synthesis And System Integration of Mixed, Information Technologies (SASIMI)*, pp. 141–146, 2012.

[11] S. Roundy, P. K. Wright, and J. Rabaey, "A study of low level vibrations as a power source for wireless sensor nodes," *Computer Communications*, vol. 26, no. 11, pp. 1131 – 1144, 2003. Ubiquitous Computing.

[12] M. Raju, "Energy harvesting. ULP meets energy harvesting: a game-changing combination for design engineers," *TI, http://focus. ti. com/lit/wp/slyy018/slyy018. pdf*, 2008.

[13] D. Musiani, K. Lin, and T. Rosing, "Active sensing platform for wireless structural health monitoring," in *Information Processing in Sensor Networks, 2007. IPSN 2007. 6th International Symposium on*, pp. 390–399, April 2007.

[14] M. Deterre, S. Risquez, B. Bouthaud, R. D. Molin, M. Woytasik, and E. Lefeuvre, "Multilayer out-of-plane overlap electrostatic energy harvesting structure actuated by blood pressure for powering intra-cardiac implants," *Journal of Physics: Conference Series*, vol. 476, no. 1, p. 012039, 2013.

[15] "Analysis of a micro-electric generator for microsystems," *Sensors and Actuators A: Physical*, vol. 52, no. 13, pp. 8 – 11, 1996. Proceedings of the 8th International Conference on Solid-State Sensors and Actuators Eurosensors {IX}.

[16] S. Saadon and O. Sidek, "Ambient vibration-based mems piezoelectric energy harvester for green energy source," in *Modeling, Simulation and Applied Optimization (ICMSAO), 2011 4th International Conference on*, pp. 1–6, April 2011.

[17] M. Marzencki, Y. Ammar, and S. Basrour, "Integrated power harvesting system including a mems generator and a power management circuit," in *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pp. 887–890, June 2007.

[18] M. Renaud, K. Karakaya, T. Sterken, P. Fiorini, C. V. Hoof, and R. Puers, "Fabrication, modelling and characterization of MEMS piezoelectric vibration harvesters," *Sensors and Actuators A: Physical*, vol. 145146, no. 0, pp. 380 – 386, 2008.

[19] P. Mitcheson, E. Yeatman, G. Rao, A. Holmes, and T. Green, "Energy harvesting from human and machine motion for wireless electronic devices," *Proceedings of the IEEE*, vol. 96, pp. 1457–1486, Sept 2008.

[20] A. Khaligh, P. Zeng, and C. Zheng, "Kinetic energy harvesting using piezoelectric and electromagnetic technologies–state of the art," *Industrial Electronics, IEEE Transactions on*, vol. 57, pp. 850–860, March 2010.

[21] C. Williams, C. Shearwood, M. Harradine, P. Mellor, T. Birch, and R. Yates, "Development of an electromagnetic micro-generator," *Circuits, Devices and Systems, IEE Proceedings* -, vol. 148, pp. 337–342, Dec 2001.

[22] A. Holmes, G. Hong, and K. Pullen, "Axial-flux permanent magnet machines for micropower generation," *Microelectromechanical Systems, Journal of*, vol. 14, pp. 54–62, Feb 2005.

[23] G. De Pasquale, E. Brusa, and A. Soma, "Capacitive vibration energy harvesting with resonance tuning," in *Design, Test, Integration Packaging of MEMS/MOEMS, 2009. MEMS/MOEMS '09. Symposium on*, pp. 280–285, April 2009.

[24] G. Altena, D. Hohlfeld, R. Elfrink, M. Goedbloed, and R. van Schaijk, "Design, modeling, fabrication and characterization of an electret-based mems electrostatic energy harvester," in *Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011 16th International*, pp. 739–742, June 2011.

[25] C. P. Le and E. Halvorsen, "Evaluation of parameters for electrostatic energy harvesters," in *Design, Test, Integration Packaging of MEMS/MOEMS, 2009. MEMS/MOEMS '09. Symposium on*, pp. 286–291, April 2009.

[26] S. Beeby and N. White, *Energy Harvesting for Autonomous Systems*. Artech House Series Smart Materials, Structures, and Systems, Artech House, Incorporated, 2014.

[27] T. Le, J. Han, A. von Jouanne, K. Mayaram, and T. Fiez, "Piezoelectric micro-power generation interface circuits," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 1411–1420, June 2006.

[28] G. Ottman, H. Hofmann, and G. Lesieutre, "Optimized piezoelectric energy harvesting circuit using step-down converter in discontinuous conduction mode," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 696–703, Mar 2003.

[29] E. Lefeuvre, D. Audigier, C. Richard, and D. Guyomar, "Buck-boost converter for sensorless power optimization of piezoelectric energy harvester," *Power Electronics, IEEE Transactions on*, vol. 22, pp. 2018–2025, Sept 2007.

[30] R. D'hulst and J. Driesen, "Power processing circuits for vibration-based energy harvesters," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pp. 2556–2562, June 2008.

[31] D. Guyomar, A. Badel, E. Lefeuvre, and C. Richard, "Toward energy harvesting using active materials and conversion improvement by nonlinear processing," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 52, pp. 584–595, April 2005.

[32] J. Liang and W.-H. Liao, "Improved design and analysis of self-powered synchronized switch interface circuit for piezoelectric energy harvesting systems," *Industrial Electronics, IEEE Transactions on*, vol. 59, pp. 1950–1960, April 2012.

[33] M. Miranda, *Electrostatic Vibration-to-Electric Energy Conversion*. PhD thesis, Massachusetts Institute of Technology.

[34] M. Miyazaki, H. Tanaka, G. Ono, T. Nagano, N. Ohkubo, T. Kawahara, and K. Yano, "Electric-energy generation using variable-capacitive resonator for power-free lsi: efficiency analysis and fundamental experiment," in *Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on*, pp. 193–198, Aug 2003.

[35] B. C.-H. Yen, "Vibration-to-electric energy conversion using a mechanically-varied capacitor," Master's thesis, Massachusetts Institute of Technology.

[36] D. Galayko, R. Pizarro, P. Basset, and A. Paracha, "Ams modeling of controlled switch for design optimization of capacitive vibration energy harvester," in *Behavioral Modeling and Simulation Workshop, 2007. BMAS 2007. IEEE International*, pp. 115–120, Sept 2007.

[37] E. Torres and G. Rincon-Mora, "Self-tuning electrostatic energy-harvester ic," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 57, pp. 808–812, Oct 2010.

[38] A. Kempitiya, D. Borca-Tasciuc, and M. Hella, "Low-power asic for microwatt electrostatic energy harvesters," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 5639–5647, Dec 2013.

[39] S. Roundy, P. K. Wright, and K. S. J. Pister, "Micro-electrostatic vibration-to-electricity converters," in *ASME 2002 International Mechanical Engineering Congress and Exposition*, pp. 487–496, Nov 2002.

[40] D. Hoffmann, B. Folkmer, and Y. Manoli, "Fabrication, characterization and modelling of electrostatic micro-generators," *Journal of Micromechanics and Microengineering*, vol. 19, no. 9, p. 094001, 2009.

[41] R. Guilllemet, P. Basset, D. Galayko, F. Cottone, F. Marty, and T. Bourouina, "Wideband mems electrostatic vibration energy harvesters based on gap-closing interdigited combs with a trapezoidal cross section," in *Micro Electro Mechanical Systems (MEMS), 2013 IEEE 26th International Conference on*, pp. 817–820, Jan 2013.

[42] T. Sterken, P. Fiorini, K. Baert, R. Puers, and G. Borghs, "An electret-based electrostatic /spl mu/-generator," in *TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003*, vol. 2, pp. 1291–1294 vol.2, June 2003.

[43] D. Galayko, E. Blokhina, P. Basset, F. Cottone, A. Dudka, E. O'Riordan, and O. Feely, "Tools for analytical and numerical analysis of electrostatic vibration energy harvesters: Application to a continuous mode conditioning circuit," *Journal of Physics: Conference Series*, vol. 476, no. 1, p. 012076, 2013.

[44] L. Tvedt, D. S. Nguyen, and E. Halvorsen, "Nonlinear behavior of an electrostatic energy harvester under wide- and narrowband excitation," *Microelectromechanical Systems, Journal of*, vol. 19, pp. 305–316, April 2010.

[45] M. Renaud, G. Altena, M. Goedbloed, C. De Nooijer, S. Matova, Y. Naito, T. Yamakawa, H. Takeuchi, K. Onishi, and R. van Schaijk, "A high performance electrostatic mems vibration energy harvester with corrugated inorganic sio2-si3n4 electret," in *Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS EUROSENSORS XXVII), 2013 Transducers Eurosensors XXVII: The 17th International Conference on*, pp. 693–696, June 2013.

[46] P. Mitcheson and T. Green, "Maximum effectiveness of electrostatic energy harvesters when coupled to interface circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, pp. 3098–3111, Dec 2012.

[47] S. Meninger, J. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, and J. H. Lang, "Vibration-to-electric energy conversion," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 9, pp. 64–76, Feb 2001.

[48] B. Yen and J. H. Lang, "A variable-capacitance vibration-to-electric energy harvester," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, pp. 288–295, Feb 2006.

[49] S. D. Nguyen, E. Halvorsen, and G. Jensen, "Wideband mems energy harvester driven by colored noise," *Microelectromechanical Systems, Journal of*, vol. 22, pp. 892–900, Aug 2013.

[50] D. S. Nguyen, E. Halvorsen, G. U. Jensen, and A. Vogl, "Fabrication and characterization of a wideband mems energy harvester utilizing nonlinear springs," *Journal of Micromechanics and Microengineering*, vol. 20, no. 12, p. 125009, 2010.

[51] C. H. Nguyen, "Modeling and characteristic of nonlinear energy harvester," Master's thesis, BUSKERUD AND VESTFOLD UNIVERSITY COLLEGE.

[52] J. Dickson, "On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique," *Solid-State Circuits, IEEE Journal of*, vol. 11, pp. 374–378, Jun 1976.

[53] J. D. Cockcroft and E. T. Walton, "Production of high velocity positive ions," in *Proc. R. Soc. A Math. Phys. Eng. Sci.*, vol. 129, p. 477489, Nov 1930.

[54] J. Witters, G. Groeseneken, and H. Maes, "Analysis and modeling of on-chip high-voltage generator circuits for use in eeprom circuits," *Solid-State Circuits, IEEE Journal of*, vol. 24, pp. 1372–1380, Oct 1989.

[55] A. Dudka, P. Basset, F. Cottone, E. Blokhina, and D. Galayko, "Wideband electrostatic vibration energy harvester (e-veh) having a low start-up voltage

employing a high-voltage integrated interface," *Journal of Physics: Conference Series*, vol. 476, no. 1, p. 012127, 2013.

[56] T. Delbruck, "'Bump' circuits for computing similarity and dissimilarity of analog voltages," in *Neural Networks, 1991., IJCNN-91-Seattle International Joint Conference on*, vol. i, pp. 475–479 vol.1, Jul 1991.